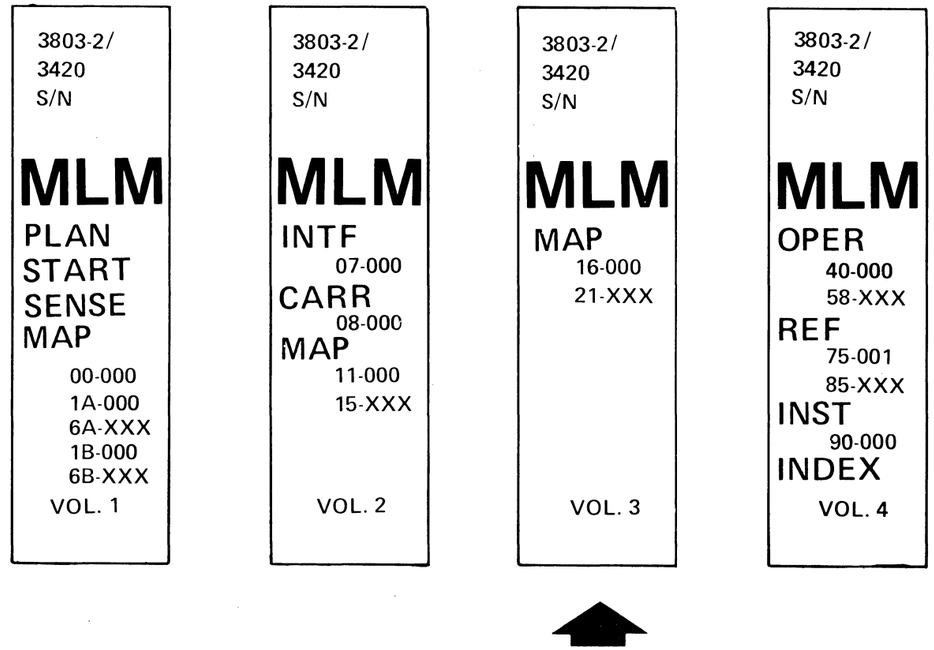
IBM Maintenance Library



3803-2/3420

Magnetic Tape Subsystem Maintenance Manual

3803-2/3420

XF0005 Seq 1 of 2	2735740 Part Number	See EC History	845958 1 Sep 79					

SAFETY

PERSONAL

The importance of personal safety cannot be over emphasized. To ensure personal safety and the safety of co-workers, follow established safety practices and procedures at all times.

Look for an obey the **DANGER**notices found in the maintenance documentation. All CEs must be familiar with the general safety practices and the procedures for artificial respiration outlines in IBM Form 229-1264. For convenience, this form is duplicated to the right.

MACHINE

To protect machines from damage, turn off power before removing or inserting circuit cards of components. Do not leave internal machine areas needlessly exposed, avoid shorting panel pins when scoping, and handle machine parts carefully, in addition, look for and observe the **CAUTION** notices found in maintenance documentation.

CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power, ac and dc, when removing or assembling major components, working in immediate areas of power supplies, performing mechanical inspection of power supplies, or installing changes in machine circuitry.
3. After turning off wall box power switch, lock it in the Off position or tag it with a "Do Not Operate" tag, Form 229-1266. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, observe the following precautions:
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Do not wear rings, wrist watches, chains, bracelets, or metal cuff links.
   c. Use only insulated pliers and screwdrivers.
   d. Keep one hand in pocket.
   e. When using test instruments, be certain that controls are set correctly and that insulated probes of proper capacity are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc.). Use suitable rubber mats, purchased locally if necessary.
5. Wear safety glasses when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power or hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Cleaning parts with solvents, sprays, cleaners, chemicals, etc.
   f. Performing any other work that may be hazardous to your eyes. REMEMBER – THEY ARE YOUR EYES.
6. Follow special safety instructions when performing specialized tasks, such as handling cathode ray tubes and extremely high voltages. These instructions are outlined in CEMs and the safety portion of the maintenance manuals.
7. Do not use solvents, chemicals, greases, or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Lift by standing or pushing up with stronger leg muscles – this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
11. After maintenance, restore all safety devices, such as guards, shields, signs, and grounding wires.
12. Each Customer Engineer is responsible to be certain that no action on his part renders products unsafe or exposes customer personnel to hazards.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. Ensure that all machine covers are in place before returning machine to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it; for example, under desk or table.
16. Avoid touching moving mechanical parts when lubricating, checking for play, etc.
17. When using stroboscope, do not touch ANYTHING – it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CEs and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machine while performing and after completing maintenance.

Knowing safety rules is not enough.
An unsafe act will inevitably lead to an accident.
Use good judgment - eliminate unsafe acts.

ARTIFICIAL RESPIRATION

General Considerations

1. Start Immediately – Seconds Count
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim, or apply stimulants.
2. Check Mouth for Obstructions
   Remove foreign objects. Pull tongue forward.
3. Loosen Clothing – Keep Victim Warm
   Take care of these items after victim is breathing by himself or when help is available.
4. Remain in Position
   After victim revives, be ready to resume respiration if necessary.
5. Call a Doctor
   Have someone summon medical aid.
6. Don't Give Up
   Continue without interruption until victim is breathing without help or is certainly dead.

Rescue Breathing for Adults

1. Place victim on his back immediately.
2. Clear throat of water, food, or foreign matter.
3. Tilt head back to open air passage.
4. Lift jaw up to keep tongue out of air passage.
5. Pinch nostrils to prevent air leakage when you blow.
6. Blow until you see chest rise.
7. Remove your lips and allow lungs to empty.
8. Listen for snoring and gurglings – signs of throat obstruction.
9. Repeat mouth to mouth breathing 10-20 times a minute. Continue rescue breathing until victim breathes for himself.

Thumb and finger positions

Final mouth-to-mouth position

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MICROPROCESSOR DIAGNOSE, LOOP, AND SCOPING PROCEDURES

This section contains general information that is useful in analyzing the errors covered in Section 16.

TO DETERMINE THE FAILING INSTRUCTION ADDRESS

The best way to get the failing address is to stop the ALU on the error. To do this, turn the Control Check Switch to the ON position. See **Caution** on this page. Also see stop procedure on 12-010, Seq 3. When the ALU stops, the Instruction Counter contains the address of the *next* (sometimes second) instruction to be executed. Remember that the Instruction Counter and the ROS Register are updated during the execution of the failing instruction.

It is possible that some red light errors are the result of a failure that took place several instructions earlier. For example, bad parity can be stored in an LSR and not be caught until the LSR is read out. This situation results in a B Bus Parity Error, but the real problem exists with the action that loaded the LSR or the LSR itself.

TO MAKE THE ALU LOOP ON AN ERROR

There are two positions on the ROS Mode switch that can be used to make the ALU loop: the RST/ERR and RST/CMPR.

If the RST/CMPR position is used, the ALU is reset before the instruction at the Compare Register address is executed.

The RST/ERR position gives a better loop in most cases. When the RST/ERR position is used, the instruction executing during the error is completed before the General Reset. It may be necessary to add a jumper from +General Reset Chan AB to +Start NB LTH (CE Start Latch) (B2Q2S10 to A1T2G05) if an I/O operation is included in the loop. The jumper isn't needed if the error occurs during ALU Checkout or Idlescans.

GENERAL REFERENCE INFORMATION

The following items should be kept in mind when troubleshooting a microprocessor problem:

- The CE SELECT REG PULSE (COMPARE EQUAL) line (A1U2U07) goes minus just before the execution of the instruction. The Stop On switches must be OFF to allow a compare.
- If the failure is at address 000, RESET OR TRAP ALU2 (A2K2D10, AA011) is a good sync point.
- When displaying ALU execution on the scope, make sure that a complete cycle is shown. The 0 ns taps for the ALU are:

  ALU1 B2F2G12
  ALU2 A2K2G12

- BU, BOC, and ADD instructions require a long cycle, 200 ns. All other instructions execute in a short cycle, 150 ns.
- Slow fall time of a pulse might be caused by a missing external load. Check the tape control ALDs for their locations.
- Always remember that you are troubleshooting lines as well as cards. If you find a bad net and the card or cards driving the line have been ruled out, something else must be wrong within the net.
- If an I/O command is involved in troubleshooting a problem offline, a contingent connection might occur. This condition is apparent if ALU1 stops with address 301 in the Instruction Counter. To break the connection, follow each failing command with a sense command.
- Random ALU failures can be caused by the ALU oscillator card, A1C2.
- Use the timing charts for a better understanding of an operation, as well as reference when a timing check is called for. Timing chart is on 16-001.
- If cards are changed and the outputs are still bad with good inputs, check for proper voltages at the card socket.
- The CE Panel lights indicate the ROS data bits, not the ROS Register bits.

Caution: Trapping ALU errors online with the control check switch ON may cause severe impact on customer operations. Make use of the channel retry feature on System/370 CPUs. Place the CPU in hard-stop mode before activating the control check switch. Use the hard-stop mode that ignores recoverable storage errors. When the ALU stops (1) obtain the required information from the CE panel, (2) turn OFF the control check switch, (3) switch the CPU to Process, and (4) start the CPU. This allows the channel retry hardware and software to recover. Recovery is only possible on intermittent ALU errors.

MICROPROCESSOR CARD INTERCHANGE LIST

The following is a list of cards that can be interchanged between ALUs:

ALU1	ALU2
B2J2	A2G2 (change program jumper 2 as shown on 52-030)
B2C2	A2N2
B2D2	A2M2 (watch for program jumpers)
B2E2	A2L2
B2F2	A2K2

The following is a list of cards that can be interchanged if the two-channel switch feature is installed:

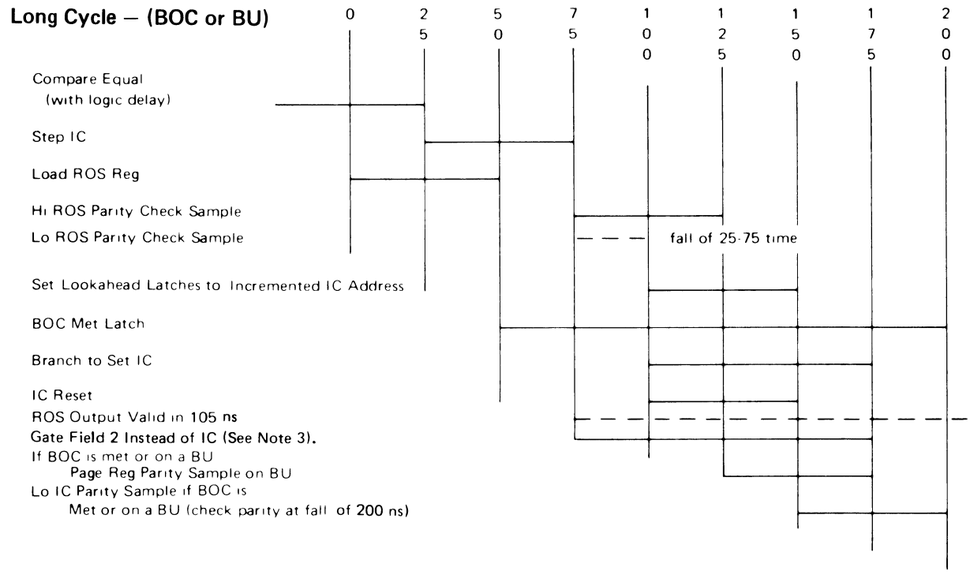
Caution: Removing these cards may cause channel errors, even with power off. Put CPU in single cycle mode before removing cards.

B2Q2	B2P2
B2R2	B2S2

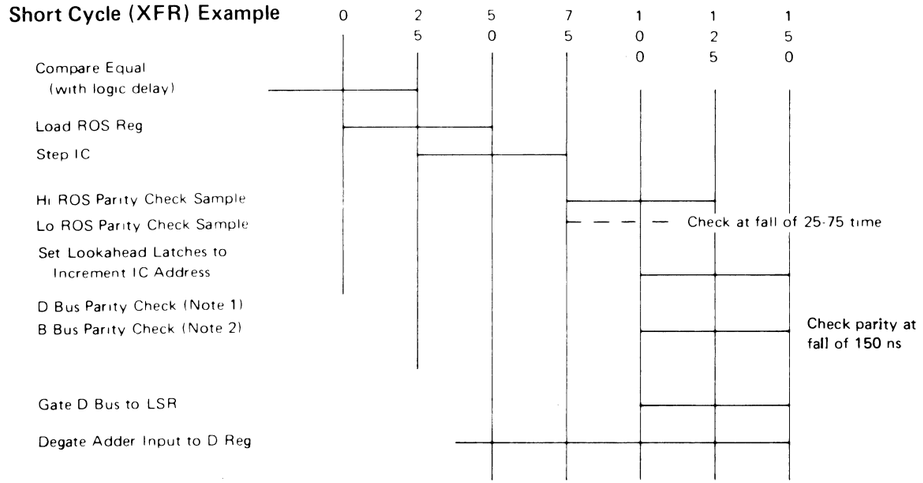
Notes:

1. *Only when data is being taken from Ext. Reg. and is being stored in an LSR.*
2. *Only when data is being transferred from an LSR.*
3. *On a BOC Met or on a BU, the contents of Field 2 are gated to ROS address while the IC is being updated.*

Long Cycle — (BOC or BU)



Short Cycle (XFR) Example



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LOW ROS/IC PARITY ERROR ON A BRANCH INSTRUCTION (ALU1)

From 13-000 or 14-000

ERROR DESCRIPTION:

Sense Byte 11, Bit 2 is set:

1. If incorrect parity is detected in ROS register bits 8 through 15.
2. If incorrect parity is detected in instruction counter (IC) bits 8 through 15 while executing a branch unconditional (BU) or branch on condition (BOC) (branch instruction).

Parity is checked at the output of the low order IC (instruction counter) and the low order ROS (read-only storage) register. Even parity sets a hardware error latch and CE panel indicator. Low IC parity is checked on a BU (branch unconditional) or a succdessful BOC operation. Low ROS parity is checked on every insturction cycle.

The low-order ROS registers in each microprocessor hold the eight low-order bits of the microprogram instruction. The registers in ALU1 and ALU2 are indentical. The output of the registers goes to the 'A' bus, Transfer Decode circuits, or Instruction Counter, depending on the instruction being executed.

Most Probable Causes:

A. B2H2 (first choice-intermittent failures)
B. B2E2 (first choice-solid failures)
C. B2L2 (B2M2 w/o EC733814) (second choice-intermittent failures)
D. A2P4
E. B2F2
F. B2D2
G. B2J2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problems or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Is the failure intermittent or accompanied by a high ROS register error?	Change in order: 1. With EC733814, B2L2 Without EC733814, B2M2 2. B2D2
2	Put ALU1 in a loop that includes the failing instruction. See 16-000 for instructions on setting up an ALU loop. 16-000 contains a timing chart and a list of the ALU cards that can be interchanged. Is -IC ROS REG PARITY ERROR (A2P4J10) always plus?	Change A2P4.
3	Does the line in Seq 2 go minus at 75 ns?	Go to Seq 9.
4	Is the failing operation a BU or BOC?	Go to Seq 7.
5	Scope -BOC MET ALU1 (B2E2U04). Is this line minus at any time during the failing instruction?	Change B2D2.
6	If not:	Change B2F2.
7	Scope −150 NS TAP ALU1 (B2E2B09). Does pulse occur at the correct time?	Change B2E2.
8	If not:	Change B2F2.
9	Is the parity of ROS bits 8-15 and P2 odd at the input to the ROS Register at 50 ns time? See Chart A for pin locations.	Go to Seq 11.
10	If not:	Change B2H2 or B2J2.
11	Is + CLK 1 NOT CE CYCLE ALU1 (B2E2M12) plus from 0 ns−50 ns?	Change B2D2.
12	If not:	Change B2F2.

Chart A

LINE NAME	TEST POINT
+ROS Bit P2	B2E2D05
+ROS Bit 8	B2E2J06
+ROS Bit 9	B2E2J05
+ROS Bit 10	B2E2G05
+ROS Bit 11	B2E2J03
+ROS Bit 12	B2E2B05
+ROS Bit 13	B2E2D09
+ROS Bit 14	B2E2B04
+ROS Bit 15	B2E2D02

HIGH ROS/IC REGISTER PARITY/BRANCH CONDITION (ALU1)

From 13-000 or 14-000

ERROR DESCRIPTION:

Sense Byte 11, Bit 3 is set:

1. On every cycle, if ROS data bits 0-7 were not transferred properly to the ROS Register.
2. On a Branch Unconditional (BU) or a Branch On Condition (BOC) operation (when the condition is met), the Page Register contents are compared to the ROS Register contents to ensure that the high order address bits were transferred properly.
3. On a BOC operation (when the condition is met), a check is made to ensure that only one of the 32 possible conditions is met.

The high-order ROS register in each microprocessor holds the eight high order bits of the microprogram instruction. The registers in ALU1 and ALU2 are identical. Bits 0-3 contain the code and bits 3-7 contain a Branch Condition or Local Storage Register (LSR) address. Bit 3 serves different purposes depending on the instruction being executed.

Most Probable Causes:

A. B2H2 (first choice—intermittent failures)
B. B2D2 (first choice—solid failures)
C. B2L2, with EC733814
   B2M2, without EC733814
D. A2P4
E. B2F2
F. B2D2
G. B2J2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problem or maintenance calls by going to map 00-030.

Seq	Condition/Instruction	Action
1	Put the ALU in a loop that includes the failing instruction. See 16-000 for instructions on scope syncing and ALU looping. 16-001 contains a timing chart and a list of the ALU cards that can be interchanged. Is the failure intermittent or accompanied by a Low ROS/IC Register error?	Change B2D2.
2	Does -INST CARD ERROR ALU1 (A2P4B13) ever go minus?	Go to Seq 4.
3	If not:	Change A2P4. This is a false error.
4	Does -INST CARD ERROR ALU1 (A2P4B13) become minus at 75 ns (125 ns w/o EC733838)?	Go to Seq 6. This is a ROS Register parity error.
5	If not:	Go to Seq 10.
6	Is the parity of ROS bits 0-7 and P1 **odd** at the input to the ROS Register at 50 ns time? See Chart A for pin locations.	Go to Seq 8.
7	If not:	Change B2H2 or B2J2.
8	Is +CLK1 NOT CE CYCLE ALU1 (B2F2J05) plus from 0 to 50 ns?	Change B2D2.
9	If not:	Change B2F2.
10	Is this a BU operation?	Change B2D2.
11	Is +BRANCH COND MET ALU1 (B2D2D11) minus?	Change B2D2.
12	Is −ROS REG 4 ALU1 (B2D2B13) plus? With EC733814, change B2L2. Without EC733814, change B2M2.	
13	If not:	Change B2D2.

Chart A

LINE NAME	TEST POINT
+ROS Bit P1	B2D2G10
+ROS Bit 0	B2D2G07
+ROS Bit 1	B2D2G05
+ROS Bit 2	B2D2J06
+ROS Bit 3	B2D2J02
+ROS Bit 4	B2D2U04
+ROS Bit 5	B2D2U11
+ROS Bit 6	B2D2S12
+ROS Bit 7	B2D2U09

B BUS PARITY ERROR (ALU1)

From **14-003, 14-000, 16-110, 13-001**

ERROR DESCRIPTION:

Sense Byte 11, Bit 0 is set when even B bus parity is detected while transferring the contents of a local storage register (LSR) to any external register (except the A register).

LSRs serve as buffers to hold command codes, addresses, error conditions and any other data the ALU may use. Each ALU has 32 LSRs. Each LSR has one byte (eight bits) of data plus one parity bit. LSRs are numbered 0-31. The output from the LSRs goes to the A register and the B bus.

Note: If tape control has EC733838 (ECA 039) installed, EC734873 (ECA 069) must also be installed. EC734873 changes the time at which data is written into the LSRs from 75 - 125 ns to 100 - 150 ns, during a Store operation.

Most Probable Causes:

A. B2C2
B. A2P4
C. B2F2
D. B2E2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problem or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Put the ALU in a loop that includes the failing instruction. See 16-000 for instructions on scope syncing and ALU looping. 16-001 contains a timing chart and a list of the ALU cards that can be interchanged. Scope –B BUS PARITY ERROR ALU1 (B2C2B11). Is this line a constant plus level?	Change A2P4.
2	Is the failing instruction an external transfer? (An external transfer is a transfer in which –ROS REG 8 ALU1 (B2E2S04) is plus.)	Go to Seq 4.
3	If not:	Go to AB181 and follow –CHK B BUS ON EXT XFR back to failing point.
4	Scope –CHK B BUS ON EXT XFR (B2C2G12). Is this line only minus at 100 - 150 ns of the failing instruction?	Go to Seq 6.
5	If not:	Go to AB181 and follow –CHK B BUS ON EXT XFR back to failing point.
6	Go to microcode listing and find the last point at which data was modified in the failing LSR. Scope –CLK 15 (B2C2J13) at this address. Is line minus at the correct time: 100 - 150 ns on a short cycle; 100 - 200 ns on a long cycle	Change B2C2. If this does not correct problem, refer to Chart A and scope B BUS test points for possible problem in nets.
7	See Note at top of MAP. This EC affects the –CLK 15 time on a store operation. Is timing bad?	Change B2F2.
8	If not:	Recheck symptoms.

Chart A

LINE NAME	TEST POINT
–B Bus 0 ALU1	B2C2G07
–B Bus 1 ALU1	B2C2G04
–B Bus 2 ALU1	B2C2G03
–B Bus 3 ALU1	B2C2J07
–B Bus 4 ALU1	B2C2J06
–B Bus 5 ALU1	B2C2J04
–B Bus 6 ALU1	B2C2J05
–B Bus 7 ALU1	B2C2G02

D BUS PARITY ERROR (ALU1)

From 13-000 or 14-000

ERROR DESCRIPTION:

Sense Byte 11, Bit 5 is set when even parity is detected on the D bus in ALU1.

The D Register parity is sampled each time data from an external register is being transferred into a LSR (Local Storage Register). The parity is compared to the parity bit associated with the data being transferred into the LSR.

Most Probable Causes:

A. B2C2
B. A2Q2
C. B2M2 with EC733814
   B2L2 without EC733814
D. A2P4
E. B2F2
F. B2E2

Additional Cards Referenced:

A. B2N2
B. A1T2

Note: If this is a 1x8 configuration with 8-F, change address plugging to 0-7 before continuing (see 90-130). When troubleshooting is complete, return the address plugging to 8-F. (Failure to do so can cause "D" Bus Parity Error.)

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problem or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Do you also have a B BUS PARITY ERROR ALU2?	Go to 16-100 and fix this problem first.
2	Put the ALU in a loop which includes the failing instruction. See 16-000 for instructions on scope syncing and ALU looping. 16-001 contains a timing chart and a list of ALU cards that can be interchanged. Scope D BUS PARITY ERROR ALU1 (A2P4G12). Is this line a constant plus level?	Change A2P4.
3	Is the failing instruction an internal transfer? (An internal transfer is one in which ROS REG 8 ALU1 (B2E2S04) is minus.)	Go to Seq 5.
4	If not:	Change B2F2.
5	Scope +CLK 16 ALU1 (B2C2D06). Is this line plus at 100 - 150 ns of the failing instruction?	Go to Seq 7.
6	If not:	Change B2F2.
7	Scope the following pins and compare the data on the D BUS with data on the REGISTER IN BITS at the fall of +CLOCK 16 as scoped in Seq 5: BIT / +REGISTER IN BIT / −D BUS 0 B2C2S05 B2C2G09 1 B2C2M13 B2C2U04 2 B2C2M09 B2C2P13 3 B2C2P04 B2C2P12 4 B2C2G13 B2C2M05 5 B2C2G08 B2C2M02 6 B2C2J03 B2C2G11 7 B2C2B12 B2C2J09 P B2C2D09 ------- Are bits 0-7 the same? (opposite levels)	Go to Seq 9.
8	If not:	Change B2C2.
9	Do REGISTER IN BITS 0-7 and P as scoped in Seq 7 have odd parity?	Go to Seq 17.
10	Is −GATE CHNL BUS OUT TO ALU (B2E2M08) minus when +CLK 16 is plus? (See Seq 5).	Go to Seq 13.
11	Is the parity of the following pins **even** when +CLK 16 is plus (See Seq 5)? +REGISTER IN BIT 0 ALU1 A2Q2B05 +REGISTER IN BIT 1 ALU1 A2Q2B02 +REGISTER IN BIT 2 ALU1 A2Q2D03 +REGISTER IN BIT 3 ALU1 A2Q2D06 +REGISTER IN BIT 4 ALU1 A2Q2G12 +REGISTER IN BIT 5 ALU1 A2Q2J11 +REGISTER IN BIT 6 ALU1 A2Q2G11 +REGISTER IN BIT 7 ALU1 A2Q2G13 +REGISTER IN BIT P ALU1 A2Q2S12 Change A2Q2.	
12	If not: With EC733814, change B2M2. Without EC733814, change B2L2.	
13	Is the failing instruction 4XA0 or 5XA0? Go to Seq 15.	
14	If not: Change B2E2.	
15	Is the parity of the following pins **even** when +CLK 16 is plus? (See Seq 5). BUS OUT BIT / With EC733814 / Without EC733814 −BUS OUT BIT 0 B2M2B05 B2L2B05 −BUS OUT BIT 1 B2M2D06 B2L2D06 −BUS OUT BIT 2 B2M2B07 B2L2B07 −BUS OUT BIT 3 B2M2B09 B2L2B09 −BUS OUT BIT 4 B2M2G10 B2L2G10 −BUS OUT BIT 5 B2M2J02 B2L2J02 −BUS OUT BIT 6 B2M2G04 B2L2G04 −BUS OUT BIT 7 B2M2G05 B2L2G05 −BUS OUT BIT P B2M2M04 B2L2M04	Go to FC081 and follow ALD page lines back to failing point.
16	If not:	With EC733814, change B2M2. Without EC733814, change B2L2.
17	Is +CLK 21 (B2C2P05) plus when +CLK 16 is plus? (See Seq 5)	Go to Seq 19.
18	If not:	Change B2F2.
19	Is +CLK 22 (B2C2J11) plus when +CLK 16 is plus? (See Seq 5)	Change B2C2.
20	If not:	Change B2F2.

BRANCH CONDITION ERROR ALU1

From 13-000 or 14-000

ERROR DESCRIPTION:
Sense Byte 11, Bit 7 is set when an even number of the branch conditions on the B2L2 (B2M2 without EC733814) card are met at the same time.

Most Probable Causes:
A. B2L2 with EC733814
   B2M2 without EC733814
B. A2P4
C. B2D2
D. B2F2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problem or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Put the ALU in a loop that includes the failing instruction. See 16-000 for details on scope syncing and ALU looping. 16-001 contains a timing chart and list of the ALU cards that can be interchanged. Scope –BRANCH ERROR ALU1 (A2P4J11). Is this line minus during the failing instruction?	Go to Seq 3.
2	If not:	Change A2P4.
3	Scope –CLK 17 DLYD ALU1 (B2F2M02). Does this line go plus during the 75 ns to 125 ns portion of the failing ins truction?	Go to Seq 5.
4	If not:	Change B2F2.
5	Scope the following pins: –ROS REG 5 ALU1 (B2D2D05) +ROS REG 5 ALU1 (B2D2P04). Are these lines opposite levels?	Go to Seq 7.
6	If not:	Change B2D2.
7	Scope –ROS REG 6 ALU1 With EC733814—B2L2S07 Without EC733814—B2M2S07 and Scope +ROS REG 6 ALU1 With EC733814—B2L2S03 Without EC733814—B2M2S03 Are these lines at opposite levels?	With EC733814, change B2L2. Without EC733814, change B2M2.
8	If not:	Change B2D2.

Chart A

This chart identifies the correct branch condition for the possible ROS Register contents. Determine the binary value of ROS Register bits 3 through 7 by using Chart B (minus=active level). Then, use the binary value of bits 3 through 7 to determine the branch condition to be made.

ROS Register Bits					Line Tested for Correct BOC
3	4	5	6	7	
0	1	0	0	0	ADDRESS OUT A, B, CE
0	1	0	0	1	COMMAND OUT A, B, CE
0	1	0	1	0	STAT A ALU1
0	1	0	1	1	STAT B ALU2
0	1	1	0	0	SELECTIVE RESET
0	1	1	0	1	SERVICE IN OR SERVICE OUT
0	1	1	1	0	SWITCHED TO CHAN B
0	1	1	1	1	MACH OR GENERAL RESET CHAN A B
1	1	0	0	0	OPERATIONAL IN
1	1	0	0	1	SUPPRESS OUT A B
1	1	0	1	0	STAT C ALU2 TO ALU1
1	1	0	1	1	ALU2 LOCKED STATUS
1	1	1	0	0	NOT GENERAL RESET CHAN A, B
1	1	1	0	1	INITIAL SEL A, B, CE
1	1	1	1	0	NOT CUE PENDING CHAN B
1	1	1	1	1	OVERRUN, ONES, RD BFR BRANCH

Note: These are the branch conditions tested on B2L2 (B2M2 without EC733814.)

Chart B

–ROS REG BITS	PIN
3	B2D2D10
4	B2D2B13
5	B2D2D05
6	B2D2D09
7	B2D2D07

ALU1 MICROPROGRAM DETECTED ERROR (ADDR 52D THROUGH 576, 300 AND 3AC)

Seq	Condition/Instruction	Action
From 14-000, 13-400, 13-001		
ERROR DESCRIPTION: Sense Byte 11, Bit 4 is set when the microprogram detects a hardware-type error during Arithmetic Logic Unit (ALU) checkout. The following MP1 instruction counter addresses are programmed traps. When a microprogram detected error occurs, the microprocessor stops at one of these trap addresses, if the microprocessor is in Stop mode and the Control Check switch is ON. If extended sense data is available, check the FRU code in Sense Byte 23.		
The following is a list of FRU codes from Sense Byte 23, and the traps and FRUs that go with them.		
FRU CODE	**TRAP**	**FRU LIST**
3	ZONKA ZONKC	A2T2 B2L2 (B2M2 w/o EC733814) A2Q2 B2E2 * A2N2 *
4	TRAP4 thru 11 CCTRAP TRAP1 TRAP2	B2C2 * B2D2 * B2E2 *
5	TRAP106 TRAP107 TRAP108 TRAP109 ZONKXA	B2C2 * B2D2 * B2F2 * A2L2 B2E2 * A2Q2
7	ZONKA	A2T2 B2L2 (B2M2 w/o EC733814) A2Q2 B2E2 * A2N2 * A2P4 B2D2 *
8	ZONKC ZONKXA ZONKXB	A2T2 B2L2 (B2M2 w/o EC733814) A2Q2 B2E2 * A2L2 B2D2 * B2C2 *
* The marked cards can be interchanged between microprocessors. MP1—MP2 B2C2—A2N2 B2D2—A2M2 B2E2—A2L2 B2F2—A2K2		

MICROPROGRAM ERROR LABELS

See 16-000 for general procedures for looping the microprocessor and scoping. If pin A2P4G11 is a constant minus, this is a false error. Change the A2P4 card.

ERROR LABEL	LINE NAME OR CONDITION	FRU	LOGIC PAGE
TROUBLE	This normally indicates a hardware error in MP2. If no red lights are on in MP2, the –ANY HARDWARE ERR ALU2 line could be on when it shouldn't be.	A2P4	AB121
	ALU2 ERROR BOC MET is on in error	B2D2	
	ALU ERROR BOC MET is on in error	B2D2	AB121
HARDWER	ALU2 ERROR BOC MET is on in error	B2D2 A2P4	AB121
ZONKA	–STATA ALU1 is on in error	A2T2	AB151
	STATA BOC MET is on in error	B2L2*	AB151
	–STATB ALU2 is on in error or failed to reset	A2Q2 B2E2	AB151 AB181
	STATB BOC MET ON in error (B from MP2)	B2L2*	AB151
	STATB failure could be an ALU failure in MP2	A2N2	
	–STATA ALU1 didn't come on	A2T2	AB151
	STATA BOC MET is off in error	B2L2*	AB151
ZONKC	–STATC ALU2 is on in error	A2T2	AB151
	STATC BOC MET is on in error	B2L2* AB151	
	STATC (MP2) didn't reset on a trap	A2Q2 B2E2	AA411 AB181
	No MP2 hard error and MP2 finished its ALU CHECKOUT routine.		
	–STATC ALU2 is off in error	A2T2	AB151
	STATC (MP2) BOC MET is off in error	B2L2* A2Q2	AB151
	STATC failure could be an ALU2 adder failure	A2N2	
TRAP11	–D BUS 0 ALU1 is on in error	B2C2	AB121
	D REG 0 BOC MET is on in error	B2D2	AB121
	–D BUS 0 ALU1 is off in error	B2C2	
	D REG 0 BOC MET is off in error	B2D2	
TRAP10	–D BUS 1 ALU1 is on in error	B2C2	AB121
	D REG 1 BOC MET is on in error	B2D2	AB121
	–D BUS 1 ALU1 is off in error	B2C2	
	D REG 1 BOC MET is off in error	B2D2	
* B2M2 without EC733814			

ERROR LABEL	LINE NAME OR CONDITION	FRU	LOGIC PAGE
TRAP9	–D BUS 2 ALU1 is on in error	B2C2	AB121
	D REG 2 BOC MET is on in error	B2D2	AB121
	–D BUS 2 ALU1 is off in error	B2C2	
	D REG 2 BOC MET is off in error	B2D2	
TRAP8	–D BUS 3 ALU1 is on in error	B2C2	AB121
	D REG 3 BOC MET is on in error	B2D2	AB121
	–D BUS 3 ALU1 is off in error	B2C2	
	D REG 3 BOC MET is off in error	B2D2	
TRAP7	–D BUS 4 ALU1 is on in error	B2C2	AB131
	D REG 4 BOC MET is on in error	B2D2	AB131
	–D BUS 4 ALU1 is off in error	B2C2	
	D REG 4 BOC MET is off in error	B2D2	
TRAP6	–D BUS 5 ALU1 is on in error	B2C2	AB131
	D REG 5 BOC MET is on in error	B2D2	AB131
	–D BUS 5 ALU1 is off in error	B2C2	
	D REG 5 BOC MET is off in error	B2D2	
TRAP5	–D BUS 6 ALU1 is on in error	B2C2	AB131
	D REG 6 BOC MET is on in error	B2D2	AB131
	–D BUS 6 ALU1 is off in error	B2C2	
	D REG 6 BOC MET is off in error	B2D2	
TRAP4	–D BUS 7 ALU1 is on in error	B2C2	AB131
	D REG 7 BOC MET is on in error	B2D2	AB131
	–D BUS 7 ALU1 is off in error	B2C2	
	D REG 7 BOC MET is off in error	B2D2	
CCTRAP	No carry occurred when adding FF to FF. –NOT ALU CARRY is on in error	B2C2	AB121
	NALCO BOC MET is on in error	B2D2	AB121
	XFR LSR 4 to A REG failure	B2E2 B2C2	AB181 AB301
	–NOT ALU CARRY is off in error	B2C2	AB121
	NALCO BOC MET is off in error	B2D2	
TRAP1	R0 should have FF before executing TEST1 which adds 1. Adder failure if any bits are on the D BUS.	B2C2	AB341
	–ALU OUTPUT ALL ZERO is off in error	B2C2	AB121
	D BUS = 0 BOC MET is off in error	B2D2	AB121
	False carry occurred the first time NALCO was tested at address 52B.	B2C2	AB121

MICROPROGRAM ERROR LABELS (Cont'd)

ERROR LABEL	LINE NAME OR CONDITION	FRU	LOGIC PAGE
TRAP2	R4 should equal 00. –NOT ALU CARRY is off in error	B2C2	AB121
	NALCO BOC MET is off in error	B2D2	AB121
TRAP106	AND operation failed	B2D2	AB111
	Wrong reset to A REG, +CLK 4	B2F2	AB301
	–D BUS 2 ALU1 is off in error	B2C2	AB121
	D REG 2 BOC MET is off in error	B2D2	AB121
TRAP107	ADD operation failed	B2D2	AB111
	–D BUS 1 ALU1 is off in error	B2C2	AB121
	D REG 1 BOC MET is off in error	B2D2	AB121
TRAP108	OR operation failed	B2D2	AB111
	–D BUS 2 ALU1 is off in error	B2C2	AB121
	D REG 2 BOC MET is off in error	B2D2	AB121
TRAP109	Exclusive OR operation failed	B2D2	AB111
	–ALU OUTPUT ALL ZERO is off in error	B2C2	AB121
	D BUS = ZERO BOC MET is off in error	B2D2	AB121
ZONK	MP2 had an error, check MP2		
	–ANY HARDWARE ERROR ALU2 is on in error	A2P4	AB121
	ALU2-ALU1 ERROR BOC MET is on in error	B2D2	AB121
	After STATD is received from MP2, check for errors again		
ZONKXA	XINA should have all bits on. +XFR LSR 2 TO XOUTA should be ON during an XFR operation. MP2 address 589.	A2L2	AA381
	–XFR XINA TO LSR1 should be ON when executing MP1 instruction at address 55B.	B2E2	AB441
	If the two previous conditions are correct, all bits (REGISTER IN) should be ON during an XFR instruction in MP1. Address 55B.	A2Q2	AB441
	NALCO BOC MET is on in error	B2D2 B2C2	AB121
ZONKXB	XINB should have all bits ON. +XFR LSR2 TO XOUTB should be ON during an XFR operation.	A2L2	AA391
	–XFR XINB TO LSR1 is off during execution on MP1 55E (XFR).	B2E2	AB441
	If the two previous conditions are correct, all bits (REGISTER IN) should be ON during the XFR instruction at MP1 address 55E.	A2Q2	AB441
	NALCO BOC MET ON in error.	B2D2 B2C2	AB121

ERROR LABEL	LINE NAME OR CONDITION	FRU	LOGIC PAGE
ZONKXA	When the XFR instruction is executed there should be no bits ON in REGISTER IN. This is set up by MP2.	A2Q2	AB441
	NALCO BOC MET is off in error	B2D2 B2C2	AB121
ZONKXB	When the XFR instruction is executed there should be no bits ON in REGISTER IN. This is set up by MP2.	A2Q2	AB441
	NALCO BOC MET is off in error	B2D2 B2C2	AB121
no name	Test DISCONNECT IN flag. This should come on only during online operation. It isn't allowed during offline operation.		
	MP2 can cause MP1 microprogram error if any of the following conditions occurs: MP2 fails to trap	A2D2 A2P4 B2E2	AA451 XC561 AB181
	MP2 decodes an instruction wrong	A2M2	
	MP2 has an undetected branch error	A2D2 A2M2	
	The MP2 clock fails	A2K2	
	An even number of bits are received from the MAL.	B2H2	QB091

LOW ROS/IC PARITY ON A BRANCH CONDITION (ALU2)

From 13-000 or 14-000

ERROR DESCRIPTION:

Sense Byte 12, Bit 2 is set:

1. If incorrect parity is detected in ROS register bits 8 through 15.
2. If incorrect parity is detected in instruction counter (IC) bits 8 through 15 while executing a branch instruction (BU or BOC).

The Low IC Parity/Low ROS Parity register checks the parity of the low order Instruction Counter (IC) and the low order Read-Only Storage (ROS) register. Even parity sets a hardware error latch and CE panel indicator. Low IC parity is checked on a Branch Unconditional (BU) or a successful Branch On Condition (BOC) operation. Low ROS parity is checked on every instruction cycle.

The low-order ROS registers in each microprocessor hold the eight low-order bits of the microprogram instruction. The registers in ALU1 and ALU2 are identical. The output of the registers goes to the A bus, Transfer Decode circuits, or Instruction Counter, depending on the instruction being executed.

Most Probable Causes:

A. A2L2 (first choice—solid failures)
B. A2H2 (first choice—intermittent failures)
C. A2D2 or A2M2 (second choice—intermittent failures)
D. A2P4
E. A2K2.
F. A2G2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problem or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Is the failure intermittent, or accompanied by a High ROS Register error?	Change in order: 1. A2D2 2. A2M2
2	Put the ALU in a loop that includes the failing instruction. See 16-000 for details on ALU looping. 16-001 contains a timing chart and a list of the ALU cards that can be interchanged. Is IC ROS REG PARITY ERROR (A2P4D02) always plus?	Change A2P4.
3	Does the above line go minus at 75 ns?	Go to Seq 9.
4	Is the failing operation a BU or BOC?	Go to Seq 7.
5	Scope BOC MET ALU2 (A2L2U04). Is this line minus at any time during the failing instruction?	Change A2M2.
6	If not:	Change A2L2.
7	Scope 150 ns TAP (A2L2B09). Does pulse occur at the correct time?	Change A2L2.
8	If not:	Change A2K2.
9	At 50 ns, is the parity of the ROS bits 8-15 and P2 odd at the input to the ROS Register? See Chart A for pin locations.	Go to Seq 11.
10	If not:	Change A2H2 or A2G2.
11	Is +CLK1 NOT CE CYCLE ALU2 (A2L2M12) plus from 0 - 50 ns?	Change A2L2.
12	If not:	Change A2K2.

Chart A

LINE NAME	TEST POINT
+ROS BIT P2	A2L2D05
+ROS BIT 8	A2L2J06
+ROS BIT 9	A2L2J05
+ROS BIT 10	A2L2G05
+ROS BIT 11	A2L2J03
+ROS BIT 12	A2L2B05
+ROS BIT 13	A2L2D09
+ROS BIT 14	A2L2B04
+ROS BIT 15	A2L2D02

HIGH ROS/IC REGISTER PARITY BRANCH CONDITION (ALU2)

From 13-000 or 14-000

ERROR DESCRIPTION:

Sense Byte 12, Bit 3 is set as follows:

1. A check is made on every cycle to ensure that ROS data bits 0-7 were transferred properly to the ROS Register.
2. On a BU or BOC operation (when the condition is met), IC bits 4 through 7 (Page Register) contents are compared to the ROS Register contents to ensure that the address bits were transferred properly.
3. On a BOC operation (when the condition is met), a check is made to ensure that only 1 of the 32 possible conditions were met.

The high-order ROS register in each ALU holds the eight high-order bits of the microprogram instruction. The registers in ALU1 and ALU2 are identical. Bits 0-3 contain the operation code and bits 3-7 contain a branch condition or LSR (Local Storage Register) address. Bit 3 serves different purposes depending on the instruction being executed.

Most Probable Causes:

The cards are listed with the highest probability first.

A. A2K2
B. A2D2
C. A2H2
D. A2M2
E. A2P4
F. A2G2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problem or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Put the ALU in a loop that includes the failing instruction. See 16-000 for details on scope syncing and ALU looping. 16-001 contains a timing chart and a list of the ALU cards that can be interchanged. Is the error intermittent?	Change A2M2.
2	Is there also a Low ROS/IC error?	Change A2M2.
3	Does INSTRUCTION CARD ERROR ALU2 (A2P4B04), ever go minus?	Go to Seq 5.
4	If not:	Change A2P4.
5	Does INSTRUCTION CARD ERROR ALU2 occur at 75 ns (125 ns w/o EC7338380?	Go to Seq 7. This is a ROS Register Parity error.
6	If not:	Go to Seq 11.
7	Is the parity of ROS bits 0-7 and P1 odd at the input to the ROS Register at 50 ns? See Chart A for pin locations.	Go to Seq 9.
8	If not:	Change A2H2 or A2G2.
9	Does +CLK 1 NOT CE CYC L1 ALU2 (A2M2J11), go plus at 0-50 ns?	Change A2M2.
10	If not:	Change A2K2.
11	Is the failing operation a BU?	Change A2M2.
12	Is +BRANCH MET ALU2 (A2M2D11) minus?	Change A2M2.
13	Is ROS REG 4 ALU2 (A2M2B13) plus?	Change A2D2.
14	If not:	Change A2M2.

Chart A

LINE NAME	TEST POINT
+ROS BIT P1	A2M2G10
+ROS BIT 0	A2M2G07
+ROS BIT 1	A2M2G05
+ROS BIT 2	A2M2J06
+ROS BIT 3	A2M2J02
+ROS BIT 4	A2M2U04
+ROS BIT 5	A2M2U11
+ROS BIT 6	A2M2S12
+ROS BIT 7	A2M2U09

B BUS PARITY ERROR ALU2

From 14-004, 16-040, 13-001

ERROR DESCRIPTION:

Sense Byte 12, Bit 0 is set when incorrect B bus parity is detected while transferring the contents of an local storage register (LSR) to any external register (except the A Register).

The B Bus Parity Register checks the output of an LSR for odd B bus parity on such transfers. Even parity sets Sense Byte 12, Bit 0 and a hardware error latch.

LSRs serve as buffers to hold command codes, addresses, error conditions and any other data the microprocessors may use. Each microprocessor has 32 LSRs. Each register has one byte (eight bits) of data plus one parity bit. Registers are numbered LSR 0 to LSR 31. The output from the LSRs goes to the A register and the B bus.

Note: If the tape control has EC733838 (ECA 039) installed, EC734873 (ECA 069) must also be installed. EC734873 changes the time at which data is written into the LSRs from 75-125 ns to 100-150 ns on a Store operation.

Most Probable Causes:

The cards are listed with the highest probability first.

A. A2M2
B. A2K2
C. A2N2
D. A2P4

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problem or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Put the ALU in a loop that includes the failing instruction. See 16-000 for details on scope syncing and ALU looping. 16-001 contains a timing chart and a list of the ALU cards that can be interchanged. Scope –B BUS PARITY ERROR ALU2 (A2N2B11). Is this line a constant plus level?	Change A2P4.
2	Is the failing instruction an external transfer? An external transfer is a transfer in which –ROS REG 8 ALU2 (A2L2S04) is plus.	Go to Seq 4.
3	If not:	Go to ALD AA171 and follow –CHK B BUS ON EXT XFR (A2L2U10) back to isolate failure.
4	Scope –CHK B BUS ON EXT XFR (A2N2G12). Is this line only minus at 100-150 ns of the failing instruction?	Go to Seq 6.
5	If not:	Go to ALD AA171 and follow –CHK B BUS ON EXT XFR (A2L2U10) back to isolate failure.
6	Find in the microcode the last point at which the data was modified in the failing LSR. Scope –CLK 15 (A2N2J13) at this address. Does pulse occur at the correct time? 100-150 ns on a short cycle 150-200 ns on a long cycle.	Change A2N2. If this does not correct problem, refer to Chart A to scope B BUS for possible net problems.
7	See Note in heading. If timing is bad:	Change A2K2.
8	If not:	Recheck symptoms.

Chart A

LINE NAME	TEST POINT
–B BUS 0 ALU2	A2N2G07
–B BUS 1 ALU2	A2N2G04
–B BUS 2 ALU2	A2N2G03
–B BUS 3 ALU2	A2N2J07
–B BUS 4 ALU2	A2N2J06
–B BUS 5 ALU2	A2N2J04
–B BUS 6 ALU2	A2N2J05
–B BUS 7 ALU2	A2N2G02

D BUS PARITY ERROR (ALU2)

From 14-004, 13-001

ERROR DESCRIPTION:

Sense Byte 12, Bit 5 is set when even parity is detected on the D bus.

The D bus parity circuit checks the parity of information to be stored in an LSR (Local Storage Register). Even parity sets Sense Byte 12, Bit 5 and a hardware error latch. This error condition is checked only during transfer of data to the ALU (Arithmetic Logic Unit) from an external source.

An ALU (Arithmetic Logic Unit) performs all arithmetic and logic operations (AND, OR, exclusive OR, and ADD).

Most Probable Causes:

A. A2N2 (interchange with B2C2)
B. A2T2
C. A2P4
D. A2K2 (interchange with B2F2)

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problem or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Do you also have a B BUS PARITY ERROR ALU1?	Go to 16-030 and fix this failure first, then return here.
2	Put the ALU in a loop that includes the failing instruction. See 16-000 for details on scope syncing and ALU looping. 16-001 contains a timing chart and a list of cards that can be interchanged. Scope –D BUS PARITY ERROR ALU2 (A2P4D04). Is this line a constant plus level?	Change A2P4.
3	Is the failing instruction an internal transfer? An internal transfer is one in which –ROS REG 8 ALU2 (A2L2S04) is minus.	Go to Seq 5.
4	If not:	Change A2K2.
5	Scope +CLK 16 ALU2 (A2N2D06). Is this line plus at 100-150 ns of the failing instruction?	Go to Seq 7.
6	If not:	Change A2K2.
7	Scope the +REGISTER IN BITS in Chart A and compare to the –D BUS BITS in Chart B. Compare at the fall of +CLK 16 scoped in Seq 5. Do bits 0-7 of both charts A and B compare (opposite levels)?	Go to Seq 9.
8	If not:	Change A2N2.
9	Do the REGISTER IN BITS 0-7 and P scoped in Seq 7 have odd parity?	Go to Seq 11.
10	If not:	Change A2T2.
11	Is +CLK 21 ALU2 (A2N2P05) plus while +CLK 16 is plus? (See Seq 5.)	Go to Seq 13.
12	If not:	Change A2K2.
13	Is +CLK 22 (A2N2J11) plus while +CLK 16 is active? (See Seq 5.)	Change A2N2.
14	If not:	Change A2K2.

Chart A

LINE NAME	TEST POINT
+REGISTER IN BIT P ALU2	A2N2D09
+REGISTER IN BIT 0 ALU2	A2N2S05
+REGISTER IN BIT 1 ALU2	A2N2M13
+REGISTER IN BIT 2 ALU2	A2N2M09
+REGISTER IN BIT 3 ALU2	A2N2P04
+REGISTER IN BIT 4 ALU2	A2N2G13
+REGISTER IN BIT 5 ALU2	A2N2G08
+REGISTER IN BIT 6 ALU2	A2N2J03
+REGISTER IN BIT 7 ALU2	A2N2B12

Chart B

LINE NAME	TEST POINT
–D BUS 0 ALU2	A2N2G09
–D BUS 1 ALU2	A2N2U04
–D BUS 2 ALU2	A2N2P13
–D BUS 3 ALU2	A2N2P12
–D BUS 4 ALU2	A2N2M05
–D BUS 5 ALU 2	A2N2M02
–D BUS 6 ALU2	A2N2G11
–D BUS 7 ALU2	A2N2J09

BRANCH ON CONDITION ERROR (ALU2)

From 13-000 or 14-000

ERROR DESCRIPTION:
Sense Byte 12, Bit 7 is set when more than one of the branch conditions on the A2D2 card are active at the same time.

Most Probable Causes:
A. A2D2
B. A2M2
C. A2P4
D. A2K2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problem or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Put the ALU in a loop that includes the failing instruction. See 16-000 for details on scope syncing and ALU looping. 16-001 contains a timing chart and a list of the ALU cards that can be interchanged. Scope +BRANCH ERROR ALU2 (A2P4J04). Is this line a constant minus level?	Change A2P4.
2	Scope –CLK 17 (A2D2P02). Does this line go plus from 75-125 ns of the failing instruction?	Go to Seq 4.
3	If not:	Change A2K2.
4	Scope the following two pins: –ROS REG 5 ALU2 (A2D2P07) +ROS REG 5 ALU2 (A2D2P11) Are these lines opposite levels?	Go to Seq 6.
5	If not:	Change A2M2.
6	Scope the following two pins: –ROS REG 6 ALU2 (A2D2U06) +ROS REG 6 ALU2 (A2D2U11) Are these lines opposite levels?	Change A2D2.
7	If not:	Change A2M2.

Chart A

This chart identifies the correct branch condition for the possible ROS Register contents. Determine the binary value of ROS Register bits 3-7 by using Chart B. Use the binary value to determine which branch condition should be used.

ROS Register Bits					LINE TESTED FOR CORRECT BOC	TEST POINT (–ACTIVE)
3	4	5	6	7		
0	1	0	0	0	EOD OR CRK OK	A2D2S12
0	1	0	0	1	NOT DCC OR SAGC BRANCH	A2D2M09
0	1	0	1	0	STAT A ALU2	A2D2P12
0	1	0	1	1	STAT B ALU1	A2D2S05
0	1	1	0	0	NOT TRK P ENV OR 556	A2D2S03
0	1	1	0	1	FB DATA OR ALL ONES	A2D2U04
0	1	1	1	0	BOR OR DT BRANCH CONDITION	A2D2U12
0	1	1	1	1	IBG BRANCH	A2D2U13
1	1	0	0	0	6250 BRANCH	A2D2U10
1	1	0	0	1	NOT TRK 1 ENV OR 200 BPI	A2D2S13
1	1	0	1	0	STAT C ALU1 MARK ON WALL	A2D2S02
1	1	0	1	1	STAT D ALU1	A2D2U03
1	1	1	0	0	NOT BLOCK OR ENV LOSS BRANCH	A2D2M08
1	1	1	0	1	NOT TM CONFIGURATION	A2D2S10
1	1	1	1	0	BUSY OR TACH	A2D2J13
1	1	1	1	1	INTERRUPT	A2D2S11

Note: These are the branch conditions on A2D2.

Chart B

LINE NAME	TEST POINT
–ROS REG 3 ALU2	A2M2D10
–ROS REG 4 ALU2	A2M2B13
–ROS REG 5 ALU2	A2M2D05
–ROS REG 6 ALU2	A2M2D09
–ROS REG 7 ALU2	A2M2D07

From 14-00X, 13-001

The following MP2 Instruction Counter addresses are programmed traps. When a microprogram error occurs, the microprocessor stops at one of these addresses if the microprocessor is in STOP MODE and the Control Check Stop Switch is ON.

If extended sense data is available, check the FRU code in Sense Byte 23.

Cards A2K2, A2L2, A2M2, A2N2, and B2C2 have duplicates in the other microprocessor. (See 16-250)

The B2C2 card is included because this error can be caused by an undetected ALU failure in MP1.

ERROR DESCRIPTION:

Sense Byte 12, Bit 4 is set when the microprogram detects a hardware-type error during ALU (Arithmetic Logic Unit) checkout.

Note: AA361 without EC733838, AA261 with EC733838

SENSE BYTE 23 FRU CODE	ZONK or TRAP	FRUs	COMMENTS
AA	ZONK2	A2T2 A2N2 A2M2 B2C2 A2L2	XOUTA is missing or has extra bits. The STOP STAT is on. Using wrong LSRs.
AA or 00	ZONKA	A2Q2 A2D2	MP2 STAT A failed ON or OFF.
AA or 00	ZONKB	A2T2 A2D2 B2C2	MP1 STATs B, C, and D failed.
AA or 00	ZONKC	A2T2 A2D2 B2C2	MP1 STATs B, C, and D failed.
AA or 00	ZONKD	A2T2 A2D2 B2C2	MP1 STATs B, C, and D failed.
AA	TRAP4 thru TRAP11	A2N2 A2M2	D Register failure.
AA	ZONK	A2L2 A2M2 A2N2 A2Q2	High LSR control or STATD can't be set.
AA	no name	A2N2 A2M2	High/Low LSR control.
AA	TRAP1	A2N2 A2M2	D Bus 0 and adder failure.
AA	TRAP2	A2N2 A2M2	D Bus 0 and adder failure.
AA	CCTRAP	A2N2 A2M2	D Bus 0 and adder failure.
hot TU BUS IN	ZONK10	A2T2 A2D2 A2N2	Hot bits on the Tape Unit BUS IN.

If the problem isn't fixed, go to the next table.

ZONK OR TRAP	COMMENTS	FRU	LOGIC PAGE
ZONK2	SET HI/LO LSR line is on in error	A2L2	AA171
	One or more XINA bits are missing. Bits are missing in REGISTER IN at A2N2.	A2T2	AA211 AA431
	One or more XINA bits are missing. No Bits missing in REGISTER IN at A2N2.	A2N2	AA211
	NALCO BOC met condition is on in error	A2M2	AA121
	–NOT ALU CARRY ALU2 is on in error	A2N2	AA261
	STAT BIT 0 ALU1 TO ALU2 is on in error	A2T2	AB141
	STOP BOC met condition is on in error	A2M2	AA131
	Extra bits on in MP1 XOUTA (MP2 XINA). Extra bits on in REG IN at A2N2.	A2N2 A2T2	AA211 AA432
	Extra bits on in MP1 XOUTA (MP2 XINA). No extra bits on in REG IN at A2N2.	A2N2	AA341
ZONKA	STATA is on in error	A2Q2	AA141
	STATA BOC MET is on in error	A2D2	XC041
	STATA is off in error	A2Q2	AA401
	STATA BOC MET is on in error	A2D2	XC041
ZONKB	STATB (from MP1) is on in error	A2T2	AB141
	STATB BOC MET is on in error	A2D2	XC041
	STATB (from MP1) is off in error	A2T2	AB141
	STATB BOC MET is off in error	A2D2	XC041
ZONKC	STATC (from MP1) is on in error	A2T2	AB141
	STATC BOC MET is on in error	A2D2	XC041
	STATC (from MP1) is off in error	A2T2	AB141
	STATC BOC MET is off in error	A2D2	XC041
ZONKD	STATD (from MP1) is on in error	A2T2	AB141
	STATD BOC MET is on in error	A2D2	XC041
	STATD (from MP1) is off in error	A2T2	AB141
	STATD BOC MET is off in error	A2D2	XC041
TRAP4	D REG BIT 7 is on in error	A2N2	AA341
	D REG BIT 7 BOC MET is on in error	A2M2	AA131
	D REG BIT 7 is off in error	A2N2	AA341
	D REG BIT 7 BOC MET is off in error	A2M2	AA131

ZONK OR TRAP	COMMENTS	FRU	LOGIC PAGE
TRAP5	D REG BIT 6 is on in error	A2N2	AA341
	D REG BIT 6 BOC MET is on in error	A2M2	AA131
	D REG BIT 6 is off in error	A2N2	AA341
	D REG BIT 6 BOC MET is off in error	A2M2	AA131
TRAP6	D REG BIT 5 is on in error	A2N2	AA341
	D REG BIT 5 BOC MET is on in error	A2M2	AA131
	D REG BIT 5 is off in error	A2N2	AA341
	D REG BIT 5 BOC MET is off in error	A2M2	AA131
TRAP7	D REG BIT 4 is on in error	A2N2	AA341
	D REG BIT 4 BOC MET is on in error	A2M2	AA131
	D REG BIT 4 is off in error	A2N2	AA341
	D REG BIT 4 BOC MET is off in error	A2M2	AA131
TRAP8	D REG BIT 3 is on in error	A2N2	AA331
	D REG BIT 3 BOC MET is on in error	A2M2	AA121
	D REG BIT 3 is off in error	A2N2	AA331
	D REG BIT 3 BOC MET is off in error	A2M2	AA121
TRAP9	D REG BIT 2 is on in error	A2N2	AA331
	D REG BIT 2 BOC MET is on in error	A2M2	AA121
	D REG BIT 2 is off in error	A2N2	AA331
	D REG BIT 2 BOC MET is off in error	A2M2	AA121
TRAP10	D REG BIT 1 is on in error	A2N2	AA331
	D REG BIT 1 BOC MET is on in error	A2M2	AA121
	D REG BIT 1 is off in error	A2N2	AA331
	D REG BIT 1 BOC MET is off in error	A2M2	AA121
TRAP11	D REG BIT 0 is on in error	A2N2	AA331
	D REG BIT 0 BOC MET is on in error	A2M2	AA121
	D REG BIT 0 is off in error	A2N2	AA331
	D REG BIT 0 BOC MET is off in error	A2M2	AA121
no name	An STOH or XFRH instruction went to a low LSR instead of high (ROS REG 3)	A2N2 A2M2	AA281
	Exclusive OR didn't work	A2M2	AA111
	–ALU 0 is off in error	A2N2	See Note.
	BOC MET is off in error	A2M2	AA121

ALU2 MICROPROGRAM ERROR (Cont'd)

ZONK OR TRAP	COMMENTS	FRU	LOGIC PAGE
ZONK	Set High LSR didn't work	A2L2 A2M2	AA171 AA281
	–ALU 0 is on in error	A2N2	See Note.
	BOC MET is on in error	A2M2	AA121
	STATD didn't come on to finish –STATD ALU2 to ALU1	A2Q2	AA451
no name	Low op codes don't work when in high mode. Should use high LSRs.	A2N2	AA281
TRAP1	A carry occurred with bits left on the D Bus. Should be 0.	A2N2	AA361
	ALU 0 (D BUS) BOC MET is off in error	A2M2	AA121
	–ALU 0 line is off in error	A2N2	AA361
TRAP2	NO ALU CARRY is off in error	A2N2	AA361
	NALCO BOC MET is off in error	A2M2	AA121
CCTRAP	No carry, should have carried	A2N2	AA361
	NALCO BOC MET is on in error	A2M2	AA121
	Carry, should not have carried	A2N2	AA361
	NALCO BOC MET is off in error	A2M2	AA121
ZONK10	Hot Tape Unit BUS IN bits or hot BUSY TACH line	A2T2 A2D2 A2N2	FD011 XC031

ANALYZING MICROPROGRAM ERRORS

See 16-000 for general instructions in analyzing microprocessor errors. 16-000 describes looping and scope syncing techniques. It also contains a list of duplicate cards used in the microprocessors.

During the ALU CHECKOUT routine, microprogram errors can be caused by missing or extra bits in the REGISTER IN, BOC failures, adder failures, and setting high or low LSRs.

It is important to know exactly which microprogram instruction is at fault before developing sync if the CE COMPARE REGISTER is used.

The following is a list of the conditions that lead to the error:

1	MP1 placed a byte of all ones in XOUTA and trapped MP2 to address 000. Instruction 'NDXTST3,' MP2 branched unconditionally to 'EXECTST3.'
2	MP2 turned on the microprogram error with the XFR HDWERR instruction somewhere in the MP2 checkout.
3	The Instruction Counter is updated by one during the execution of the XFR HDWERR instruction.
4	Enable the CE Panel, disable the interface, turn the Control Check switch on, and turn the ALU1/2 switch to ALU1. Execute a failing type instruction (reset switch or I/O function). If MP1 has any error other than the microprogram error, analyze the other error first.
5	Assuming no MP1 failure, turn the ALU1/2 to the ALU2 position.
6	Again perform the failing type operation. If any other error besides the microprogram error occurs, analyze the other error first.
7	Not all LSRs are cleared before the checkout routine is performed immediately after power on.
8	Rule out a false error by checking pin A2P4J02 for minus level or a pulse. If this pin is a constant plus level, change the A2P4 card.
9	The tables on 16-030 are a list of the conditions that turn on microprogram errors.

From 14-00X, 00-040

ERROR DESCRIPTION:

Sense Byte 10, Bit 0 is set when the tape unit fails to return, or the control unit fails to recognize, the proper command status information to the tape control in response to a command tag and byte. The failing command must be identified by using the sense bytes from LOGREC or OLTs. Sense byte 23 provides the status which the tape control received from the tape unit. (See Chart A on 16-163.)

The first part of this procedure is used to resolve some single tape unit failures. If it is not known which command is failing, test them all by starting at Seq 2 assuming a write-type and then a read-type command. Use Chart C on 16-163 as a guide. Be sure there are no "hot" BUS IN lines along with the correct response for each command.

Most Probable Causes: The following is a list of known cards which cause the problems covered in this procedure. The cards are listed with the highest probability first. Lines with multiple cards have the same probability.

Tape Control (Multiple Drive Failure)	**Tape Unit 4, 6 8** (Single Drive Failure)	**Tape Unit 3, 5, 7** (Single Drive Failure)
A. A2Q2, B3F2	A. T-A1M2, T-A1L2, T-A1K2	A. T-A1H2, T-A1L2, T-A1K4
B. A2D2, A2R2	B. T-A1K6, T-A1J2, T-A1C2	B. T-A1J2, T-A1C2

Interface voltage levels are:
+ 4.5 V inactive
0 V active

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problem or maintenance calls by going to MAP 00-030. The bits mentioned in this procedure are from Sense Byte 23, FRU list for MP2. (See Chart A on 16-163.)

Seq	Condition/Instruction	Action
1	Does the failure occur on more than one tape unit?	Go to Seq 120.
1A	Is this a Model 3, 5 or 7?	Go to 6A-160.
2	If the failure is isolated to a single tape unit, it may be diagnosed without the tape control. The failing command may be duplicated by performing the following steps: 1. Disconnect the I/O cable from tape unit. 2. Reset, load, and ready the failing tape unit with a work tape. 3. Ground (D08) the COMMAND tag (T-A1K6D12). 4. Ground the appropriate BUS OUT bit (see Chart D on 16-163 for location.) 5. Switch tape unit online to allow scoping BUS IN. Charts A, B, and C on 16-163 are used to determine the proper response.	
3	Is the failing operation a: Write (01, 0F, 07, LWR)	Go to Seq 4.
	Read (02, 37, 3F, 0C, 27, 2F)	Go to Seq 20.
	Interrupt (Not ready to READY)	Go to Seq 120.
	Interrupt (Set Pulse)	Go to Seq 123.
	Interrupt (SAGC Check)	Go to Seq 140.
	Tach Busy (Writing)	Go to Seq 145.
	Tach Busy (Rewinding)	Go to Seq 157.
	Meter (Writing)	Go to Seq 145.
4	The failure is on a write-type command (01, 1F, 17, or LWR). Ground −BUS OUT 4 I/O (T-A1K6D06). This forces the tape unit into Write status. If an LWR, also ground −BUS OUT 2 (T-A1K6B04). After putting on test jumpers, ground −BUS OUT 6 (T-A1K6D07) momentarily.	
5	Are any of the following lines at the level indicated? +CONTROL TAG (T-A1K6D10) plus? −COMMAND TAG (T-A1K6D09) plus? −MOVE TAG (T-A1K6B12) minus?	Change T-A1K6.
6	Is −BUS IN 0 (T-A1L2D02) minus?	Go to Seq 34.
7	Is −BUS IN 1 (T-A1L2D04) minus?	Go to Seq 47.
8	Is failing command an LWR (hex 8B)?	Go to Seq 68.
9	Is −BUS IN 2 (T-A1L2D05) minus?	Go to Seq 57.
10	Is −BUS IN 3 (T-A1L2D06) minus?	Go to Seq 75.
11	**Note**: Bus In 4 (Byte 23, Bit 4) should be ON for a write-type command. Example: 01, 1F, or 17. Is −BUS IN 4 (T-A1L2D07) minus?	This is a normal response to a Write Command. Go to Seq 16.
12	Is +STATUS BUS 4A (T-A1L2P12) plus?	Change T-A1L2.
13	Is −WRITE STATUS (T-A1M2U04) plus?	Go to Seq 40.
14	Is +STATUS BUS 4 (T-A1M2J09) minus?	Change T-A1M2.
15	If not:	Change T-A1K2.
16	Is −BUS IN 5 (T-A1L2D09) minus?	Go to Seq 83.
17	Is −BUS IN 6 (T-A1L2D10) minus?	Go to Seq 89.
18	Is −BUS IN 7 (T-A1L2D11) minus?	Go to Seq 104.
19	If not:	This is a normal BUS IN 4 response to a write-type command. Turn power off, remove test jumpers, and check with a meter: Y1D06, N4B06 to K6D06 Y1B12, N4B12 to K6D12 L2D07, N2B06 to Y1J06 If LWR, this is a normal BUS IN 2 response. Check with a meter: Y1D04, N4B04 to K6B04 (B02) L2D05, N2B04 to Y1J04 (B12) Go to Seq 118.
20	Ground −BUS OUT 1 I/O (T-A1K6B03). This forces the tape unit into Forward Read status. After installing the test jumper, ground −BUS OUT 6 (T-A1K6D07) momentarily.	
21	Is −BUS IN 0 (T-A1L2D02) minus?	Go to Seq 107.
22	Is −BUS IN 1 (T-A1L2D04) minus?	Go to Seq 47.
23	Is −BUS IN 2 (T-A1L2D05) minus?	Go to Seq 57.
24	Is −BUS IN 3 (T-A1L2D06) minus?	Go to Seq 75.
25	Is −BUS IN 4 (T-A1L2D07) minus?	Go to Seq 113.
26	Is −BUS IN 5 (T-A1L2D09) minus?	Go to Seq 83.
27	Is −BUS IN 6 (T-A1L2D10) minus?	Go to Seq 89.
28	Is −BUS IN 7 (T-A1L2D11) minus?	Go to Seq 104.
29	Remove jumper from T-A1K6B03 and put on T-A1K6B02. This forces backward status. BUS IN 0 is normal response to Read Backward commands (i.e., 0C, 27, 2F). Is −BUS IN 0 (T-A1L2D02) minus?	Turn power off and check continuity: Y1D02, N4B02 to K6B02 Y1B03, N4D03 to K6B03 L2D02, N2B02 to Y1J02 Go to Seq 118.
30	Is −BUS OUT 0 (T-A1J2D11) plus?	Change T-A1K6.
31	Is +BKWD STATUS (T-A1J2P11) minus?	Change T-A1J2.
32	Is +STATUS BUS 0 (T-A1M2B05) minus?	Change T-A1M2.
33	If not:	Change T-A1L2.
34	Is +BKWD STATUS (T-A1M2G04) plus?	Go to Seq 38.
35	Is +STATUS BUS 0 (T-A1M2B05) plus?	Change T-A1M2.
36	Is −BUS IN 0 (T-A1L2D02) minus?	Change T-A1L2.
37	If not:	Recheck at Seq 6.
38	Is −WRT STATUS (T-A1J2M12) plus?	Go to Seq 40.
39	If not:	Remove test jumper and change T-A1J2.

Seq	Condition/Instruction	Action
40	Is +REW OP (T-A1J2D09) plus?	Go to Seq 43.
41	Is −BUS OUT 4 (T-A1J2S07) plus?	Remove test jumper and change T-A1K6.
42	If not:	Remove test jumper and change T-A1J2.
43	Is +LOAD RWD (T-A1C2J05) plus?	Remove test jumper and change T-A1D4.
44	Is −SET RWD COMMAND (T-A1C2B05) minus?	Change T-A1J2.
45	Is −GATED LOAD REWIND PB (T-A1C2D05) minus?	Change T-A1C2.
46	If not:	Remove test jumper and change T-A1C2.
47	Is −GAP CONTROL (T-A1M2D06) minus?	Go to Seq 51.
48	Is +STATUS BUS 1 (T-A1M2B07) plus?	Change T-A1M2.
49	Is −BUS IN 1 (T-A1L2D04) minus?	Change T-A1L2.
50	If not:	Remove test jumper and see Note 7 on 16-163.
51	Is −TO (T-A1F2G04) pulsing?	Go to Seq 53.
52	If not:	Remove test jumper and change T-A1H2.
53	Is +GO INT (T-A1F2S07) minus?	Change T-A1F2.
54	Is −GATE RWD (T-A1F2U02) minus?	Go to Seq 40.
55	Is −MOVE COMMAND B (T-A1F2P12) minus?	Go to Seq 87.
56	If not:	Remove test jumper and change T-A1H2.
57	Is −DIAGNOSTIC MODE (T-A1M2D10) minus?	Go to Seq 62.
58	Is +STATUS BUS 2 (T-A1M2G10) plus?	Change T-A1M2.
59	Is +STATUS BUS 2A (T-A1K2D06) plus?	Change T-A1K2.
60	Is −BUS IN 2 (T-A1L2D05) minus?	Change T-A1L2.
61	If not:	Recheck Seq 9 or 23.
62	Is −BUS OUT 2 (T-A1J2M04) minus?	Change T-A1K6.
63	Ground −BUS OUT 6 I/O (T-A1M2P02). Does +SENSE RESET (T-A1J2P05) go plus?	Go to Seq 66.
64	Is −BUS OUT 6 (T-A1M2P02) plus?	Change T-A1K6.
65	If not:	Remove test jumper and change T-A1M2.
66	Is −DIAGNOSTIC MODE (T-A1M2D10) minus?	Change A1J2.
67	If not:	Check with a meter: Y1B08, N4B08 to K6D07
68	BUS IN 2 is normal response to LWR command. **Note:** Bit 4 will also be ON, but it will not cause a failure on LWR.	
69	Is −BUS IN 2 (T-A1L2D05) minus?	Go to Seq 10.
70	Is +STATUS BUS 2A (T-A1L2M04) plus?	Change T-A1L2.
71	Is +STATUS BUS 2 (T-A1K2D05) plus?	Change T-A1K2.
72	Is −DIAGNOSTIC MODE (T-A1M2D10) minus?	Change T-A1M2.
73	Is −BUS OUT 2 (T-A1J2M04) minus?	Change T-A1J2.
74	If not:	Change T-A1K6.
75	Is +TIE UP (T-A1M2U10) minus?	Check for open TIE UP circuit (ALD FT115).
76	Is +STATUS BUS 3 (T-A1M2B04) plus?	Change T-A1M2.
77	Is +GATED OPPOSITE DIRECTION (T-A1K2J11) plus?	Go to Seq 81.
78	Is +STATUS BUS 3A (T-A1K2J07) plus?	Change T-A1K2.
79	Is −BUS IN 3 (T-A1L2D06) minus?	Change T-A1L2.
80	If not:	Recheck Seq 10 or 24.
81	Is +GO INT (T-A1F2S07) minus?	Change T-A1F2.
82	If not:	Go to Seq 54.
83	Is +STATUS BUS 5 (T-A1M2P06) plus?	Change T-A1M2.
84	Is +LONG STOP RESPONSE (T-A1H2M10) plus?	Change T-A1H2.
85	Is −BUS IN 5 (T-A1L2D09) minus?	Change T-A1L2.
86	If not:	Recheck Seq 16 or 26.
87	Is −MOVE COMMAND (T-A1K2D13) minus?	Change T-A1J2.
88	If not:	Remove test jumper and change T-A1K2.
89	Ground −BUS OUT 6 I/O (T-A1K6D07). Does +SENSE RESET (T-A1M2P11) go plus?	Go to Seq 92.
90	Is −BUS OUT 6 (T-A1M2P02) plus?	Change T-A1K6.
91	If not:	Change T-A1M2.
92	Remove jumper at T-A1K6D07. Is −BUS IN 6 (T-A1L2D10) plus?	Go to Seq 18 for Write, or Seq 28 for Read.
93	Is +WRITE CURRENT U.K. (T-A1M2P10) plus? This information is obtained by checking Sense Byte 6, Bit 1.	Go to 15-090.
94	Is +ERASE U.K. (T-A1M2S05) plus? Check Sense Byte 7, Bit 5 to obtain this information.	Go to 15-090.
95	Is +RESET KEY (T-A1M2S03) plus?	Change T-A1M2.
96	Is +LAMP OFF (T-A1M2S07) plus?	Check the lamp. If lamp is on, change T-A1D2. If the lamp is off, change the lamp.
97	Is +TAPE BOTTOM LEFT (T-A1M2U02) plus?	Be sure tape is not bottomed in the left column. If tape is bottomed, go to 2B-170 or 3B-110. If tape is not bottomed, change T-A1C2.
98	Is +TAPE BOTTOM RIGHT (T-A1M2U05) plus?	Be sure tape is not bottomed in the right column. If tape is bottomed go to 2B-170 or 3B-110. If tape is not bottomed, change T-A1C2.
99	Is −LOSS OF AIR OR OVUV (T-A1M2S02) minus?	Change T-A1M2.
100	Is +STATUS BUS 6 (T-A1M2B12) plus?	Change T-A1M2.
101	Is +STATUS BUS 6A (T-A1K2G12) plus?	Change T-A1K2.
102	Is −BUS IN 6 (T-A1L2D10) minus?	Change T-A1L2.
103	If not:	Recheck Seq 17 (write) or 27 (read).
104	Is +STATUS BUS 7 (T-A1M2J02) plus?	Change T-A1M2.
105	Is −BUS IN 7 (T-A1L2D11) minus?	Change T-A1L2.
106	If not:	Recheck Seq 18 (write) or 28 (read).
107	Is +BKWD STATUS (T-A1M2G04) plus?	Go to Seq 111.
108	Is +STATUS BUS 0 (T-A1M2B05) plus?	Change T-A1M2.
109	Is −BUS IN 0 (T-A1L2D02) minus?	Change T-A1L2.
110	If not:	Recheck Seq 21.
111	Is −BUS OUT 1 (T-A1J2G04) minus?	Change T-A1K6.
112	If not:	Remove test jumper and change T-A1J2.
113	Is −WRITE STATUS (T-A1M2U04) minus?	Change T-A1J2.
114	Is +STATUS BUS 4 (T-A1M2J09) plus?	Change T-A1M2.
115	Is +STATUS BUS 4A (T-A1K2S12) plus?	Change T-A1K2.
116	Is −BUS IN 4 (T-A1L2D07) minus?	Change T-A1L2.
117	If not:	Recheck Seq 25.

COMMAND STATUS REJECT (Cont'd)

Seq	Condition/Instruction	Action
118	Ground –MOVE TAG I/O (T-A1K6D13). Tape may run away. Is –MOVE TAG (T-A1K6B12) plus?	Change T-A1K6.
119	If not:	Turn power off. Remove test jumpers, and check continuity from Y1D13 and N4D13 to K6D13.
120	Reset and load-rewind the tape unit. Do not make it ready.	
121	Is –INTERRUPT 2A (T-A1K2G09) a solid plus?	Go to Seq 125.
122	Is –INTERRUPT 2 (T-A1J2U10) a solid plus?	Change T-A1K2.
123	Is –INTERRUPT 1 (T-A1J2S10) a solid minus?	Change T-A1M2.
124	If not:	Change T-A1J2.
125	Is –INTERRUPT IN (T-A1L2B05) +0.1V or more above ground? This line is not terminated when the device cable is removed, but should be almost ground when not active and +0.1V when active.	Change T-A1L2.
126	Make the tape unit ready.	
127	Is –INTERRUPT 2A (T-A1K2G09) a solid minus?	Go to Seq 131.
128	Is –INTERRUPT 2 (T-A1K2U10) a solid minus?	Change T-A1K2.
129	Is –INTERRUPT 1 (T-A1J2S10) a solid plus?	Change T-A1M2.
130	If not:	Change T-A1J2.
131	Is –INTERRUPT IN (T-A1L2B05) about +0.1V?	Go to Seq 133.
132	If not:	Change T-A1L2.
133	The following sequences check the Set Pulse command. Reset and load-rewind the tape unit. Do not make it ready.	
134	Ground the following pins: –COMMAND TAG I/O (T-A1K6D12) –BUS OUT 3 I/O (T-A1K6B05)	
135	Does –INTERRUPT 2A (T-A1K2G09) have a symmetrical square wave at an approximate rate of 330 ns?	Go to Seq 138.
136	Is –BUS OUT 3 (T-A1J2S09) plus?	Change T-A1K6.
137	If not:	Change T-A1J2.
138	Does –INTERRUPT IN (T-A1L2B05) have a symmetrical square wave about +0.1V above ground with ring on the down level?	Go to Seq 141.
139	If not:	Change T-A1L2.
140	The following sequences check that a SAGC Check from the Read Card will cause an Interrupt (Models 4, 6, and 8 only).	
141	Reset, rewind, and ready the tape unit.	
142	Ground the following lines at the same time and in the order specified: –COMMAND TAG I/O (T-A1K6D12) –BUS OUT 4 I/O (T-A1K6D06) Now move the test jumpers from the above lines and ground the following lines at the same time and in the order specified: –MOVE TAG I/O (T-A1K6D13) –SAGC CHECK (T-A1K2G08) Tape should be moving.	
143	Is –INTERRUPT 2A (T-A1K2G09) a solid plus?	Change T-A1K2.
144	Turn power off. Remove test jumpers, and check continuity from L2B05 and N2D11 to Y1J11.	Go to 00-030.
145	The following sequences check the TACH/BUSY and METER OUT lines. Reset, load-rewind and make the tape unit ready.	
146	Ground the following lines at the same time and in the order specified: –BUS OUT 4 I/O (T-A1K6D06) –COMMAND TAG I/O (T-A1K6D12) Now move the test jumpers and ground: –MOVE TAG I/O (T-A1K6D13) –METER OUT I/O (T-A1L2P05) Tape should be moving.	
147	Are there any tach pulses on –TACH/BUSY IN (T-A1L2B04)? This is an unloaded line with the device cable disconnected. The pulses should be approximately 0.1v above ground.	Go to Seq 152.
148	Are there any tach pulses on on –PHASE B GATED (T-A1L2J12)?	Go to Seq 150.
149	If not:	Change T-A1H2.
150	Is +SUM OF TAGS (T-A1L2J13) minus?	Change T-A1J2.
151	If not:	Change T-A1L2.
152	Is –RUN METER (T-A1L2M08) approximately at ground? (This is a +12v to 0v line.)	Meter should be running. If not, refer to ZT001. Go to Seq 156.
153	Is +LP STATUS DELAYED (T-A1L2B09) plus?	Change T-A1G2.
154	Is –SET METER ENABLE (T-A1L2J07) plus?	Change T-A1J2.
155	If not:	Change T-A1L2.
156	Turn power off. Remove test jumpers, and check continuity from L2B04 and N2B12 to Y1G12 for TACH/BUSY and/or Y1J13 and N2D13 to L2P05 for METER OUT.	
157	The following sequences check for BUSY during a rewind operation. Reset, rewind and ready the tape unit with a work tape.	
158	Ground the following lines at the same time and in the order specified: –BUS OUT 4 I/O (T-A1K6D06) –COMMAND TAG I/O (T-A1K6D12) Move the jumper on K6D12 to K6D13 (–MOVE TAG I/O). Tape should start moving.	
159	With tape away from load point, remove the two test jumpers.	
160	Pull the capstan motor plug from the capstan motor control board. **DANGER: Never connect the capstan motor plug with power ON.**	
161	Ground the following lines in the order specified: –BUS OUT 7 I/O (T-A1K6B09) –CONTROL TAG I/O (T-A1K6D11).	
162	Remove the test jumper from –CONTROL TAG I/O (T-A1K6D11). (If the capstan motor is connected, the tape is rewinding.)	
163	Is –TACH/BUSY IN (T-A1L2B04) about +0.1v?	Go to Seq 167.
164	Is –BUSY STATUS (T-A1L2J11) plus?	Change T-A1J2.

Seq	Condition/Instruction	Action
165	Is +SUM OF TAGS (T-A1L2J13) plus?	Change T-A1J2.
166	If not:	Change T-A1L2.
167	Turn power off. Connect the capstan motor to the capstan motor control board, remove the test jumpers, and check for continuity from L2B04 and N2B12 to Y1G12.	Go to 00-030.
168	Using the failing commands, set up the CE panel to stop ALU2 after executing TUBODOWN to check for 'hot' TUBOs. Rotate selectable register switch to ALU2 Device Bus Out. When the TC stops at this address, check for 'hot' TUBOs. Are there any BUS OUT lights on? (See 12-000 for CE panel information.)	Go to Seq 236.
169	Set up the CE panel to stop ALU2 after executing STATSNOW. If the tape control stops, the active bits may be looked at in a static status. If it is not possible to analyze the problem in a static status, sync the scope minus on –TU TAG BIT 6 COMMAND (A-A2R2J06) and follow the procedure. Does the ALU stop at this address?	Go to Seq 171.
170	If not:	Set up the CE panel to stop ALU2 after executing address MSKSTS. Go to Seq 172.
171	Is the tape control in Read Status? (Check Sense Byte 1, Bit 5; if the bit is ON, the tape control is in Write Status).	Go to Seq 221.
172	Is Byte 23, Bit 0 ON? (This bit indicates the tape control is in Backward Status.)	Go to Seq 182.
173	Is Byte 23, Bit 1 ON?	Go to Seq 188.
174	Is Byte 23, Bit 2 ON?	Go to Seq 193.
175	Is Byte 23, Bit 3 ON?	Go to Seq 198.
176	Is Byte 23, Bit 4 ON?	This is a normal response to Set Write. Recheck Sense Data.
177	Is Byte 23, Bit 5 ON?	Go to Seq 204.
178	Is Byte 23, Bit 6 OFF?	Go to Seq 209.
179	Is Byte 23, Bit 7 ON?	Go to Seq 215.
180	Is Sense Byte 23 = hex 00?	Check the –TU TAG BIT 6 COMMAND line (A2R2J06) to be sure it is minus. Change A2R2 if it is not minus.
181	If not:	Recheck Sense Data.

Seq	Condition/Instruction	Action
182	Is –DEVICE BUS IN 0 TO DF (A2T2M04) minus?	Change A2D2; if problem still exists, see Note 7.
183	Is –TUBO BIT 0 (A2R2S03) plus?	Change A2E2.
184	Is +0 PCT AMPL CTRL TRK 0 (A1H2P11) plus?	Change Y1D2, then Y1Q2.
185	Is +TUBO BIT 0 (A2R2D12) plus?	Change A1H2.
186	Is –B BUS 0 ALU2 (A2R2J07) minus?	Change A2N2.
187	If not:	Change A2R2.
188	Is –DEVICE BUS IN 1 TO DF (A2T2P03) minus?	Change A2D2; if problem still exists, see Note 7 on 16-163.
189	Is –TUBO BIT 1 (A2R2B12) plus?	Change A2E2.
190	Is +TUBO BIT 1 (A2R2B13) plus?	Change A1H2.
191	Is –B BUS 1 ALU2 (A2R2G05) minus?	Change A2N2.
192	If not:	Change A2R2.
193	Is –DEVICE BUS IN 2 TO DF (A2T2M02) minus?	Change A2D2; if problem still exists, see Note 7 on 16-163.
194	Is –TUBO BIT 2 (A2R2D05) plus?	Change A2E2.
195	Is +TUBO BIT 2 (A2R2B05) plus?	Change A1H2.
196	Is –B BUS 2 ALU2 (A2R2J05) minus?	Change A2N2.
197	If not:	Change A2R2.
198	Is –DEVICE BUS IN 3 TO DF (A2T2J10) minus?	Change A2D2; if problem still exists, see Note 7.
199	Is –TUBO BIT 3 (A2R2G02) plus?	Change A2E2.
200	Is +0 PCT AMPL CTRL TRK 3 (A1H2M11) plus?	Change Y1D2, then Y1Q2.
201	Is +TUBO BIT 3 (A2R2D13) plus?	Change A1H2.
202	Is –B BUS 3 ALU2 (A2R2J03) minus?	Change A2N2.
203	If not:	Change A2R2.
204	Is –DEVICE BUS IN 5 TO DF (A2T2M10) minus?	Change A2D2; if problem still exists, see Note 7 on 16-163.
205	Is –TUBO BIT 5 (A2R2B10) plus?	Change A2E2.
206	Is +TUBO BIT 5 (A2R2B09) plus?	Change A1H2.
207	Is –B BUS 5 ALU2 (A2R2M09) minus?	Change A2N2.
208	If not:	Change A2R2.

Seq	Condition/Instruction	Action
209	Is –DEVICE BUS IN 6 TO DF (A2T2P07) minus?	Change A2D2; if problem still exists, see Note 7 on 16-163.
210	Is –TUBO BIT 6 line (T-A2R2G13) minus?	Change A2E2.
211	Is +0 PCT AMPL CNTRL TRK 6 (A1H2P06) plus?	Change Y1D2, then Y1Q2.
212	Is +TUBO BIT 6 (A2R2G12) plus?	Change A1H2.
213	Is –B BUS 6 ALU2 (A2R2U03) plus?	Change A2N2.
214	If not:	Change A1R2.
215	Is –DEVICE BUS IN 7 TO DF (A2T2P09) minus?	Change A2D2; if problem still exists, see Note 7 on 16-163.
216	Is –TUBO BIT 7 (A2R2S02) plus?	Change A2E2.
217	Is +0 PCT AMPL CTRL TRK 7 (A1H2P02) plus?	Change Y1D2, then Y1Q2.
218	Is +TUBO BIT 7 (A2R2M03) plus?	Change A1H2.
219	Is –B BUS 7 ALU2 (A2R2P13) minus?	Change A2N2.
220	If not:	Change A2R2.
221	Is Byte 23, Bit 0 ON?	If the tape control is performing a Read Backward command, this is a normal response. A BUS OUT 0 to the tape unit sets the tape unit to Backward Status. BUS IN notifies the tape control that the tape unit is in Backward Status. If the command is not a Read Backward, go to Seq 182.
222	Is Byte 23, Bit 1 ON?	Go to Seq 188.
223	Is Byte 23, Bit 2 ON?	Go to Seq 193.
224	Is Byte 23, Bit 2 ON?	Go to Seq 198.
225	Is Byte 23, Bit 4 ON?	Normal response to a Set Write; go to Seq 231.
226	Is Byte 23, Bit 5 on?	Go to Seq 204.
227	Is Byte 23, Bit 6 ON?	Go to Seq 209.
228	Is Byte 23, Bit 7 ON?	Go to Seq 215.
229	Is the FRU = 00?	If the command is a Read Forward, this is a normal response; recheck Sense Data. If the command is a Read Backward, check –TU TAG BIT 6 COMMAND (A2R2J06) to be sure it is active.
230	If not:	Recheck Sense Data.

COMMAND STATUS REJECT (Cont'd)

Seq	Condition/Instruction	Action
231	Is –DEVICE BUS IN 4 TO DF (A2T2P11) minus?	Change A2D2; if problem still exists, see Note 7 on 16-163.
232	Is –TUBO BIT 4 (A2R2B07) plus?	Change A2E2.
233	Is +TUBO BIT 4 (A2R2D09) plus?	Change A1H2.
234	Is –B BUS 4 ALU2 (A2R2M12) minus?	Change A2N2.
235	If not:	Change A2R2.
236	Is the BUS OUT 0 indicator ON?	Go to Seq 183.
237	Is the BUS OUT 1 indicator ON?	Go to Seq 189.
238	Is the BUS OUT 2 indicator ON?	Go to Seq 194.
239	Is the BUS OUT 3 indicator ON?	Go to Seq 199.
240	Is the BUS OUT 4 indicator ON?	Go to Seq 234.
241	Is the BUS OUT 5 indicator ON?	Go to Seq 205.
242	Is the BUS OUT 6 indicator ON?	Go to Seq 209.
243	Is the BUS OUT 7 indicator ON?	Go to Seq 216.
244	If not:	Recheck symptoms.

Notes:

1. This command is sent to a tape unit after a Rewind/Unload is initiated or if a Start I/O is issued to a Not Ready tape unit in which the Interrupt In line is not previously pulsing. To test statically, enter a Rewind/Unload command (hex 0F). If a Rewind/Unload is executed and ROS is set to Stop, the tape unit will execute the operation.
2. On Set Pulse commands, the tape control samples the tape unit Interrupt In line instead of Bus In. Refer to ALD FT131. Ensure the Interrupt In line has a symmetrical square wave approximately 500 ns wide.
3. This command is issued only on Read Backward or Backspace Block commands in 6250 mode.
4. If this command is suspected as failure, do a Compare Equal on ALU2 address 775.
5. The TC does not require any response from the tape unit for a Reset command and, therefore, no Command Status Reject can be set.
6. If active, troubleshoot tape unit first on tape unit logic FT114.
7. Interchange tape unit signal cable to another TU if possible. If there is a path failure (same address fails), go to 18-000 for Selection (1x8) logic or go to 18-010 for Device Switch feature.

Chart A

When this bit is set with a write-type channel command word, the ALU2 FRU ID sense byte (byte 23) has the following meaning:

FRU Bit 0 On: TU failed to set forward status.
FRU Bit 1 On: Gap control is active in TU.
FRU Bit 2 On: TU is in diagnostic mode and Reset command was ineffective. (Normal response to LWR.)
FRU Bit 3 On: Opposite direction—should not be on.
FRU Bit 4 On: Normal response to Write command.
FRU Bit 5 On: Possible—will not cause error.
FRU Bit 6 On: Unit Check condition in TU or Reset command was ineffective.
FRU Bit 7 On: Unused—Active BUS IN bit at command time.
FRU=00: TU failed to respond or failed to recognize BUS OUT bit 4.
FRU≠00: Possible that the TU failed to recognize command tag.

When this bit is set with a read-type channel command word, the ALU2 FRU ID sense byte (byte 23) has the following meaning:

FRU Bit 0 On: Normal response to set read backward. TU is in backward status.
FRU Bit 1 On: Gap control is active.
FRU Bit 2 On: TU is in diagnostic mode and Reset command was ineffective.
FRU Bit 3 On: Opposite direction—should not be on.
FRU Bit 4 On: TU failed to reset write status.
FRU Bit 5 On: Possible—will not cause error.
FRU Bit 6 On: Unit Check condition in TU or Reset command was ineffective.
FRU Bit 7 On: Unused—Active Bus In bit at command time.
FRU=00: Normal response to Set Read Forward command.
FRU≠00: Possible that the TU failed to recognize the command tag.

Chart B: Tape Unit Commands and Command Status Byte

Bit	Command Bus Out	Status Byte Bus In
0	Set backward read.	Normal response to backward read.
1	Set forward read.	Gap control is hot.
2	Set diagnostic (LWR).	TU is in diagnostic mode.
3	Set pulse.	Opposite direction (hot Bus In at command time).
4	Set write.	Write status (normal response to a Write command).
5	Set extended stop.	Extended stop (hot Bus In at command time).
6	Reset tape unit.	Unit check (unit check not being reset in tape unit).
7	Unused.	Positioning.

Chart C

Command	Hex Command	ALU2 Stop	Tape Unit Bus Out	Tape Unit Bus In
Write	01	170	08	08
Write Tape Mark	1F	170	08	08
Erase Gap	17	170	08	08
Read Forward	02	170	40	00
Forward Space Block	37	170	40	00
Forward Space File	3F	170	40	00
Read Backward	0C	170	80	80
Backspace Block	27	170	80	80
Backspace File	2F	170	80	80
Set Diag (LWR)	8B	170	28	28
Set Pulse*	(1)	11D	10	(2)
Set Extended Stop*	(3)	775(4)	04	04
Reset*	(5)	37E	02	Unit Check (6)

* Refer to Notes for commands that cause these conditions.

Chart D

Line Name	Test Point
BUS OUT 0	T-A1K6B02
BUS OUT 1	T-A1K6B03
BUS OUT 2	T-A1K6B04
BUS OUT 3	T-A1K6B05
BUS OUT 4	T-A1K6D06
BUS OUT 5	T-A1K6B07
BUS OUT 6	T-A1K6D07
BUS OUT 7	T-A1K6B09

TACH START FAILURE (SENSE BYTE 10, BIT 5)

From 14-011 or 00-040

ERROR DESCRIPTION:

Sense Byte 10, Bit 5 is set when no change is detected in the tach status within a specified length of time during START DELAY. START DELAY is the interval from the receipt of a MOVE command at the tape unit until the time when the tape is up to speed.

An Local Storage Register (LSR) WORK3 uses the Read Time pulse to measure the time between tach pulses generated by the capstan, phototransistor and capstan squaring circuit. If 256 bit cells (read time pulses) produced by the Read Time oscillator in the tape control occur without a tach pulse, the microprogram velocity subroutine sets Sense Byte 10, Bit 5.

Tach Start failure can also be set during repositioning if the tach is not detected within a specified length of time while reversing direction.

Most Probable Causes:
The following is a list of the known or components that can cause the problems covered in this procedure The cards are listed with the highest probability first. Lines with multiple cards have the same probability.

	Control Unit	Tape Unit
A.	A2D2	A. BOT/EOT Adjustment (08-580)
B.	A1K2	B. A1L2
C.	A1G2	C. A1J2
D.	A2Q2	D. A1L6, A1M2 (Models 4, 6, 8) A1M2 (Models 3, 5, 7)
E.	A1H2	E. Capstan Board
F.	A2E2	F. Capstan Tachometer
G.	B2D2	G. Capstan Motor
H.	B2M2 with EC733814 B2L2 without EC733814	H. Check upper stubby bar adjustment
I.	A2T2 2R2	I. Glass beaded tape on stubby bar loose
J.	A2R2	J. A1G2
K.	A2N2	
L.	A2H2	
M.	B3K2, B3H2, B3J2, B3L2	

If this MAP procedure is exhausted, and problem is not fixed, do the following:
1. Interchange A2N2 and B2C2.
2. Change A2H2.

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise.
Remember to END all problem or maintenance calls by going to MAP00-030.

Seq	Condition/Instruction	Action
1	Did you come here from 14-011?	Go to Seq 11.
2	Is –BUSY STATUS (T-A1L2J11) minus?	Change T-A1J2.
3	Is –INTERFACE DISABLE (T-A1L2B02) plus (0 to +6 v)?	Go to Seq 6.
4	Is –PICK ONLINE RELAY (T-A1L6B10) minus (0 V)?	Change T-A1L6.
5	If not:	Investigate Online/Offline switch. Begin on ALDFT910.
6	Switch the tape unit OFFLINE. Set up the field tester for a write, start/stop operation. Sync the scope of –MOVE TAG (T-A1J2B09).	If –MOVE TAG is not active, go to Seq 11.
7	Is T-A1L2J12) failing to pulse?	Go to 6A-000 for Models 3, 5, and 7. Go to 6B-000 for Models 4, 6, and 8.
8	Is +SUM OF TAGS (T-A1L2J13) minus during the sync?	Change T-A1J2.
9	Is +READ GATE (T-A1L2P04) failing to pulse?	Change T-A1J2.
10	Is +Sense Reset plus? T-A1M2P11 for Models 4,6,8 T-A1H2P11 for Models 3,5,7	Change: T-A1M2 for Models 4,6,8 T-A1H2 for Models 3,5,7
10A	If not;	Change T-A1L2, capstan board, capstan tach, capstan motor.
11	Are all tape units failing?	Go to Seq 13.
11A	Is –MOVE minus? T-A1K6D13 for Models 4,6,8 T-A1K4D13 for Models 3,5,7	Change: T-A1K6 for Models 4,6,8 T-A1K4 for Models 3,5,7
12	If not:	If this is a 1x8 switch, go to 18-001, Chart D and follow the line TAG C MOVE back to the origin in the 3803. If this is a 2x8, 3x8, or 4x8 switch, refer to 18-010 through 18-013 and follow the instructions. Also check BOT/EOT voltage checks adjustment. See 08-580.
13	CE Panel set up (if CE panel fails to operate go to 12-000): 1. Enable the CE Panel: Turn the Panel Enable switch On. Set ROS Mode switch to Norm and operate Set ROS Mode. 2. Turn the meter switch to Disabled, then wait for the Intf's Disabled light to come on. 3. Turn off the Stop On Control Check and Stop On Data Flow Check switches. 4. Use the Data Entry Select switch to enter the following commands, in the CE register. Operate the Set CE/Cmpr switch to load each command: CMND1 - 8BX (LWR) CMND2 - 8BX (LWR) CMND3 - 8BX (LWR) CMND4 - 8BX (LWR) Byte Count - FEF Write Data/Go Down - FF0 (X=tape unit address) 5. Add jumper between A1S2G08 and A1S2J08 to allow LWR to terminate. 6. Set switches: ALU1/ALU2 switch to ALU2 Mple/Single switch to Mple Display Select switch to IC 7. Rewind tape to load point.	
14	Operate Start switch. Does ALU2 IC indicator indicate 63F?	Go to Seq 20.
15	Is only the UPGM Data Flow Check indicator On?	Go to Seq 34.
16	Are only the MTE, ENV, and UPGM Data Flow Check indicators On?	Go to Seq 40.
17	Are only the WR TGR and UPGM Data Flow Check indicators On?	Go to Seq 43.
18	Does the tape control run without errors?	Go to Seq 45.
19	If not:	Change in order: 1. A2N2 2. A2H2
20	Is EC733838 installed?	Go to Seq 23.
21	Is –LSR DECODE 7B ALU1 (B2D2U06) pulsing?	Go to Seq 23.
22	If not:	Change B2D2.
23	Is –USEC FREQ (A1K2J07) pulsing?	Go to Seq 25.
24	If not:	Change A1K2.
25	Is –STOP STAT TO DF minus? With EC733814—B2M2U09 Without EC733814—B2L2U09	With EC733814, change B2M2. Without EC733814, change B2L2.
26	Is –STAT BIT 1 START WR/RD (A2Q2B03) minus?	Go to Seq 28.
27	If not:	Change A2Q2.
28	Set ROS Mode Switch to Norm, operate Set ROS Mode, then operate Reset. Is –XOUTA BIT 5 ALU2 to DF (A2Q2J04) pulsing?	Go to Seq 30.
29	If not:	Change A2T2.
30	Is –XOUTA BIT 4 ALU2 TO DF (A1K2D09) pulsing?	Go to Seq 32.
31	If not:	Change A1K2.
32	Is –WRITE CONDITION (A1G2G07) minus?	Go to Seq 13 and recheck setup.
33	If not:	Change A1G2.
34	Set ROS Mode Switch to Norm, operate Set ROS Mode, turn off the Stop On Control Check and Stop On Data Flow Check switches, and operate Start switch. Is –6250 BRANCH (A1K2U05) minus?	Change A1K2.
35	Is –XOUTA BIT 2 ALU2 TO DF (A2Q2S11) pulsing?	Go to Seq 37.
36	If not:	Change A2Q2.

TACH START FAILURE (SENSE BYTE 10, BIT 5) (Cont'd)

Seq	Condition/Instruction	Action
37	Is +INHIBIT WRITE (A1K2B11) pulsing?	Change A1K2.
38	Is –GATE WRITE (A1G2M10) pulsing?	Go to Seq 13 and recheck setup.
39	If not:	Change A1G2.
40	Set the ROS Mode Switch to Norm, operate Set ROS Mode, turn off the Stop On Control Check and Start On Data Flow Check Switches, and operate the Start switch. Is –TU TAG BIT 7 MOVE (A2E2P13) pulsing?	Go to 18-001, Chart D, and find out why MOVE is not reaching the tape unit.
41	Is –TU TAG BIT 7 MOVE (A2R2D03) pulsing?	Go to Seq 13 and recheck setup.
42	If not:	Change A2R2.
43	Set the ROS Mode Switch to Norm, operate Set ROS Mode, turn off the Stop On Control Check and Start On Data Flow Check Switches, and operate the Start switch. Is –WR TRIGGER GATE (A1G2P10) pulsing?	Go to Seq 13 and recheck setup.
44	If not:	Change A1G2.
45	Set the ROS Mode Switch to Norm, operate Set ROS Mode, turn off the Stop On Control Check and Start On Data Flow Check Switches, and operate the Start switch. Is –WC9 (A1G2P04) pulsing?	Go to Seq 47 on 16-171.
46	If not:	Change A1G2.
47	CE Panel set up: 1. Turn off the Stop On Control Check and Stop On Data Flow Check switches. 2. Use the Data Entry Select switch to enter the following commands in the CE register. Operate the Set CE/Cmpr switch to load each command. CMND1—07X (Rewind) CMND2—01X (Write 6250) CMND3—01X (Write 6250) CMND4—01X (Write 6250) 3. Take off jumper between A1S2G08 and A1S2J08. 4. Set switches: Mple/Single switch to Single Display Select switch to IC. 5. Operate Reset, then operate START switch twice.	**Note:** The UPGM ERROR light may be on.

Seq	Condition/Instruction	Action
48	Set Mple/Single switch to MPLE and operate Stop/Start switch to START. Is –WRITE CNTR0 (A1H2S05) pulsing?	Change A1H2.
49	Reload tape unit if tape has pulled off the reel. Scope –TACH VELOCITY (A2D2B02). Does line pulse when operating the Start switch?	Change A2D2.
50	If not:	Go to 18-001 and find out why BUSY TACH is not reaching A2D2.

–BUSY TACH Line Test Points

TU	LOCATION
0	A-A2E2U03
1	A-A2E2J11
2	A-A2E2U07
3	A-A2E2D12
4	A-A2E2M12
5	A-A2E2J04
6	A-A2E2U04
7	A-A2E2B07

From 14-000

ERROR DESCRIPTION:

PE OR NRZI

Velocity Check (Sense Byte 10, Bit 7)

The tape control does not check the first four tach pulses after GAP CONTROL becomes active. If the tape control counts 24 tach pulses without finding four consecutive tach pulses within specifications, Velocity Check is set.

Velocity Change During Write (Sense Byte 9, Bit 1)

Velocity is checked on PE records of more than 220 bytes and NRZI records of more than 120 bytes. If any tach pulse is out of specification, Velocity Change During Write is set.

GCR (6250)

Velocity Check (Sense Byte 10, Bit 7)

The tape control does not check the first tach pulse after GAP CONTROL becomes active. If the tape control counts 32 half tach pulses without finding one full tach pulse in specification, Velocity Check is set.

Velocity Change During Write (Sense Byte 9, Bit 1)

Velocity is checked on 6250 bpi records or more than 824 bytes. If any tach pulse is out of specification, Velocity Change During Write is set.

Most Probable Causes:

Control Unit	Single Tape Unit
A. Y1C2	A. Low Air Bearing Pressure
B. A2D2	B. Tape Sticking
C. A2E2	C. Loose Stubby Bar
D. A2R2	D. T-A1K2 (Models 3, 5, 7) T-A1G2 (Models 4, 6, 8)
E. A2N2	
F. A2H2	

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problem or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Does failure occur on a 1x8 subsystem configuration?	Go to Seq 5.
2	Does only one tape unit operate correctly through one path and one tape control?	Go to 18-010.
3	Do all tape units fail from one tape control?	Go to Seq 5.
4	If not:	Go to 6A-000 for Models 3, 5, and 7. Go to 6B-000 for Models 4, 6, and 8.
5	Are all tape units attached to the tape control Models 3, 4, 7, or 8?	Go to Seq 7.
6	Do all the 3420 Model 5 and 6 tape units run OK?	Go to Seq 10.
7	Is Velocity Change During Write (Byte 9, Bit 1) On?	Go to Seq 15.
8	Do all the tape units fail?	Go to Seq 10.
9	If not:	Go to Seq 4.
10	Set CE panel: 1. Set Cmpr Reg to 2F0 (HUP2 ALU2). 2. Set Commands 1, 2, 3, and 4 to perform a write operation on one of the failing tape units. 3. Set the ROS Mode switch to Stop and operate Set ROS Mode. Make sure the Stop on Control Check and Stop on Data Flow Check switches are down. 4. Set the ALU1/ALU2 switch to ALU2. 5. Set the Display Select switch to IC. 6. Operate Reset then Start (make sure IC indicators indicate 2F0).	
11	Set the Display Select switch to BUS IN. Do indicators 4, 5, 6, 7 indicate correct tape unit model? (Bit 4 ON indicates 6250 bpi.) X = 6250 bpi	Change in order: 1. A2N2. 2. A2M2. 3. A2H2.
12	If any of the following bits are plus? +TUBO BIT 0 A2R2D12 +TUBO BIT 1 A2R2B13 +TUBO BIT 2 A2R2B05 +TUBO BIT 3 A2R2D13 +TUBO BIT 4 A2R2D09 +TUBO BIT 5 A2R2B09 +TUBO BIT 6 A2R2G12 +TUBO BIT 7 A2R2M03	Go to ALD FD021 and follow line back
12A	If not:	Go to Seq 13.
13	Is TUBO BIT 6 the only line minus in the following group? −TUBO BIT 0 A2R2S03 −TUBO BIT 1 A2R2B12 −TUBO BIT 2 A2R2D05 −TUBO BIT 3 A2R2G02 −TUBO BIT 4 A2R2B07 −TUBO BIT 5 A2R2B10 −TUBO BIT 6 A2R2G13 −TUBO BIT 7 A2R2S02	Change A2D2. If this does not fix the problem, go to 18-010.
14	If not:	Change in order: 1. A2R2. 2. A2N2.
15	Do all the tape units fail?	Change in order: 1. A2D2. 2. A2N2. 3. A2H2.
16	If not:	Go to Seq 4.

75 IPS	125 IPS	200 IPS
Bit 4 = X	X	X
Bit 5 = 0	1	1
Bit 6 = 1	0	0
Bit 7 = 1	0	1

From 14-000

ERROR DESCRIPTION (Sense Byte 10, Bit 3):
This bit is set when data or beginning of record (BOR) has not been detected on a write or write tape mark operation.

Most Probable Causes:
The following is a list of cards that can cause the problems covered in this procedure. The cards are listed with the highest probability first. Lines with multiple cards have the same probability.

Control Unit

A. A2T2
B. Y1P2

Tape Unit

A. Read/Write Head

Additional Cards Referenced

Control Unit

A. A1K2
B. B2E2
C. Y1Q2
D. A2Q2
E. A2L2
F. Y1T2
G. Y1S2
H. Y1R2
I. A2E2
J. D2D2
K. Y1H2
L. A2R2
M. Y1C2
N. Y1D2
O. A1G2
P. A1E2

Tape Unit

A. T-A1L2
B. T-A1J2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise.
Remember to END all problem or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Is this a single tape unit failure?	One of the following could cause this problem: • Model 3, 5, 7 rewind plunger stuck or leaking. • Head is contaminated. • Creased Tape. • Tape is sticking. • Card(s) T-A1L2 or T-A1J2 (Read/Write). Go to 5A-000 if Model 3, 5, 7. Go to 5B-000 if Model 4, 6, 8.
1A	Did the failure occur in NRZI mode? Sense Byte 6, Bit 3 on and Bit 4 off?	Go to Seq 39.
2	Sync negative on –STAT BIT 0 TAPE OP TO DF (A1K2U06) and look at –IBG BRANCH (A2D2U13) while the sync is minus. Does it ever go plus?	Go to Seq 5.
3	Is –TAPE OP A (A1K2B10) the same as the sync?	Go to Seq 5.
4	If not:	Change A1K2.
5	Is +NRZI (Y1T2J12) plus?	Go to Seq 10.
6	Check all lines. Do these lines become active while the sync is minus for the proper model and mode being operated? –WRITE SLD LEVEL Y1Q2D12 –6250 DENSITY SLD Y1Q2J02 –6250 Y1Q2M07 –PE Y1Q2P05 –6250 Y1Q2P06 –PE Y1Q2M05 –6250 Y1Q2P04 –PE Y1Q2M04 +NRZI Y1Q2U13 +LOW GAIN Y1Q2B02 This line is always minus. –PE SLD level Y1Q2D03	
	This line is always plus. –SLD "6250 Y1Q2D05	
	These lines are minus for 75 and 200 ips models. –PE1 SLD Y1Q2G05–6250 SLDY1Q2D11 SLD	
	These lines are minus for 75 and 125 ips models. –6250 SLD Y1Q2D07–PE2 SLDY1Q2G03 SLD –BY1Q2B03MST	
	This line is minus for 125 and 200 ips models. –A Y1Q2B05MST Are all levels correct?	Go to Seq 20.
7	Is +P.E. WRITE AND TAPE OP (Y1Q2B12) plus while the sync is minus?	Go to Seq 13.
8	Is –XOUTA BIT 5 ALU1 TO DF (A1K2U07) minus when the sync goes minus?	Change A1K2.
9	If not:	Change in order: 1. A2T2 2. B2E2
10	Is –NRZI MODE (Y1Q2S13) plus when the sync is minus?	Change Y1Q2.
11	Is either –XOUTA BIT 4 ALU2 TO DF (A1K2D09) or –XOUTA BIT 0 ALU2 TO DF (A1K2S13) minus when the sync is minus?	Change A1K2.
12	If not:	Change in order: 1. A2Q2 2. A2L2
13	Are the following lines minus while the sync is minus for the model being used? **IPS** **75 125** **200** –XOUTA BIT 7 ALU2 TO DF (Y1Q2B07) ON OFF ON –XOUTA BIT 5 ALU2 TO DF (Y1Q2B10) OFF ON ON	Go to Seq 15.
14	If not:	Change in order: 1. A2Q2 2. A2L2
15	Scope +PE MODE (Y1Q2D02) for the proper level during the time the sync is minus. Is it good?	Go to Seq 18.
16	–XOUTA BIT 0 ALU2 TO DF (A1K2S13) should be minus while the sync is minus if you are in PE mode. Is this line good for the Mode being operated in?	Change A1K2.
17	If not:	Change in order: 1. A2Q2 2. A2L2
18	+STAT BIT 2 ALU WR ID BRST (Y1Q2D06) should be minus when the sync is minus, except for a portion of the time during an operation at load point. Is it good?	Change Y1Q2.
19	If not:	Change in order: 1. A2Q2 2. A2L2
20	The following lines should become minus during the sync, except for 1, 3, and 4 on a Write Tape Mark operation. Are they all good? **Zone 1** –TIME SENSE P Y1P2P03 –TIME SENSE 0 Y1P2P09 –TIME SENSE TK 5 Y1P2D10 **Zone 2** –TIME SENSE 2 Y1P2G13 –TIME SENSE 6 Y1P2M12 –TIME SENSE TK 7 Y1P2G12 **Zone 3** –TIME SENSE 1 Y1P2P02 –TIME SENSE 3 Y1P2P10 –TIME SENSE TK 4 Y1P2S12	Go to Seq 31.

Seq	Condition/Instruction	Action
21	The following lines should pulse during the sync, except for 1, 3, and 4 on a Write Tape Mark operation. Are they all good? **Zone 1** –DEVICE BUS IN 0 TO DF Y1T2M04 –DEVICE BUS IN P TO DF Y1T2S04 –DEVICE BUS IN 5 TO DF Y1T2D13 **Zone 2** –DEVICE BUS IN 2 TO DF Y1S2M04 –DEVICE BUS IN 6 TO DF Y1S2S04 –DEVICE BUS IN 7 TO DF Y1S2D13 **Zone 3** –DEVICE BUS IN 1 TO DF Y1R2M04 –DEVICE BUS IN 3 TO DF Y1R2S04 –DEVICE BUS IN 4 TO DF Y1R2D13	Change the card in the zone that was bad in Seq 20. The following cards are interchangeable: Zone 1—change Y1T2 Zone 2—change Y1S2 Zone 3—change Y1R2
22	Compare the following DEVICE BUS OUT lines with the DEVICE BUS IN lines in Seq 21. Do the same lines pulse while the sync is minus? –TUBO BIT P A1H2U07 –TUBO BIT 0 A2R2S03 –TUBO BIT 1 A2R2B12 –TUBO BIT 2 A2R2D05 –TUBO BIT 3 A2R2G02 –TUBO BIT 4 A2R2B07 –TUBO BIT 5 A2R2B10 –TUBO BIT 6 A2R2G13 –TUBO BIT 7 A2R2S02	Go to Seq 52.
23	Is this a 1x8 machine?	Go to Seq 29.
24	Is the tape unit being used to troubleshoot the failure, physically connected to the tape control being used?	Go to Seq 27.
25	Check the following lines to see if they match the TUBO lines in Seq 22. Do they match while the sync is minus?	
	Voltage 0v to +6v	
	–BUS OUT P PRIMARY A2E2J07 –BUS OUT 0 PRIMARY A2E2G09 –BUS OUT 1 PRIMARY A2E2D03 –BUS OUT 2 PRIMARY A2E2D04 –BUS OUT 3 PRIMARY A2E2B09 –BUS OUT 4 PRIMARY A2E2D09 –BUS OUT 5 PRIMARY A2E2P07 –BUS OUT 6 PRIMARY A2E2M09 –BUS OUT 7 PRIMARY A2E2P02	Go to 18-010.
26	If not:	Change A2E2.

Seq	Condition/Instruction	Action
27	Check the following lines to see if they match the TUBO lines in Seq 22. Do they match while the sync is minus?	
	Voltage 0v to +6v	
	–BUS OUT P SECONDARY A2E2G07 –BUS OUT 0 SECONDARY A2E2G08 –BUS OUT 1 SECONDARY A2E2B03 –BUS OUT 2 SECONDARY A2E2B04 –BUS OUT 3 SECONDARY A2E2B12 –BUS OUT 4 SECONDARY A2E2D13 –BUS OUT 5 SECONDARY A2E2M07 –BUS OUT 6 SECONDARY A2E2M08 –BUS OUT 7 SECONDARY A2E2U11	Go to 18-010.
28	If not:	Change A2E2.
29	Check the following lines to see if they match the TUBO lines in Seq 22. Do they match while the sync is minus?	
	Voltage 0v to +5v	
	–BUS OUT P A2E2G07 –BUS OUT 0 A2E2G08 –BUS OUT 1 A2E2B03 –BUS OUT 2 A2E2B04 –BUS OUT 3 A2E2B12 –BUS OUT 4 A2E2D13 –BUS OUT 5 A2E2M07 –BUS OUT 6 A2E2M08 –BUS OUT 7 A2E2U11	Go to 18-010.
30	If not:	Change A2E2.
31	Does –IBG BRANCH (Y1P2M07) go plus and +BLOCK OR ENV LOSS BRANCH (A2D2M08) go minus while the sync is minus?	Go to Seq 33.
32	If not:	Change Y1P2.
33	Does –BOR 27 COMB OR DT BRANCH COND (Y1P2J13) become minus while the sync is minus?	Go to Seq 35
34	If not:	Change Y1P2.
35	Is the failure on a Write Tape Mark (WTM) operation?	Go to Seq 37.
36	If not:	Change A2D2.
37	Sync positive on –IBG BRANCH (Y1P2M07) and look at +TM CONFIGURATION (Y1P2M02). Assure +TM CONFIGURATION becomes plus during the sync and stays plus until the sync goes negative. Is it good?	Change A2D2.
38	If not:	Change Y1P2.
39	Sync negative on –TAPE OP A (Y1H2D10) and look at –FB DATA OR ALL ONES (Y1H2U09). Does it go minus at least twice while the sync is minus?	Change A2D2.

Seq	Condition/Instruction	Action
40	Does +NRZI CHAR GATE (Y1H2S10) go plus at least twice while the sync is minus?	Change Y1H2.
41	Is –NRZI MODE (Y1C2M03) minus when the sync is minus?	Go to Seq 44
42	Is either –XOUTA BIT 4 ALU2 TO DF (A1K2D09) or –XOUTA BIT 0 ALU2 TO DF (A1K2S13) minus when the sync is minus?	Change in order. 1. A2Q2 2. A2L2
43	If not:	Change A1K2.
44	Does +DEGATE NRZI SELECT (Y1C2U02) go minus while the sync is minus?	Go to Seq 46.
45	If not:	Change A2R2.
46	Does –STAT BIT 1 START WR RD (Y1C2S11) go minus while the sync is minus?	Go to Seq 48.
47	If not:	Change in order: 1. A2Q2 2. A2L2
48	Does –SET NRZI FIRST BIT (Y1C2G03) go minus at least twice while the sync is minus?	Change Y1C2.
49	Is either +PE MODE (Y1D2U04) or +6250 bpi mode (Y1D2U05) plus while the sync is minus?	Go to Seq 42.
50	Sync negative on –NRZI MODE (Y1C2M03) and assure at least one of the following lines change level while the sync is minus. Were they good? –DEVICE BUS IN P TO DF Y1D2U12 –DEVICE BUS IN 0 TO DF Y1D2U07 –DEVICE BUS IN 1 TO DF Y1D2U02 –DEVICE BUS IN 2 TO DF Y1D2P05 –DEVICE BUS IN 3 TO DF Y1D2P02 –DEVICE BUS IN 4 TO DF Y1D2J09 –DEVICE BUS IN 5 TO DF Y1D2D13 –DEVICE BUS IN 6 TO DF Y1D2D09 –DEVICE BUS IN 7 TO DF Y1D2D04	Change Y1D2.
51	If not:	Go to Seq 22.
52	Does –GATE WRITE (A2H2D03) go minus while the sync is minus?	Go to Seq 54.
53	Does +INHIBIT WRITE (A1G2S12) go plus while the sync is minus?	Go to Seq 70
54	Does –GATE WRITE NOT TM (A1H2J06) go minus while the sync is minus?	Go to Seq 58.
55	Is the failure on a Write Tape Mark command?	Go to Seq 58.
56	Does –XOUTA BIT 3 ALU1 TO DF (A1G2B03) go minus while the sync is minus?	Change in order: 1. A2T2 2. B2E2

NO BLOCK DETECTED ON WRITE/WRITE TAPE MARK (Cont'd)

Seq	Condition/Instruction	Action
57	If not:	Change A1G2.
58	Is the failure on a Write Tape Mark command?	Change in order: 1. A2T2 2. B2E2
59	Does −WR TRIGGER GATE (A1G2P10) pulse while the sync is minus?	Go to Seq 61.
60	If not:	Change A1G2.
61	Is the failure in 6250 bpi mode?	Go to Seq 67.
62	Does +WRITE TIME GATE (A1G2G03) pulse while the sync is minus?	Change in order: 1. A1G2. 2. Y1Q2 3. A1E2 (7-track feature) cards.
63	Is −6250 bpi mode (A1G2M07) minus when the sync is minus?	Go to Seq 65.
64	If not:	Change A1G2.
65	Is −XOUTA BIT 0 ALU2 TO DF (A1K2S13) minus when the sync is minus?	Change in order: 1. A2Q2 2. A2L2
66	If not:	Change A1K2.
67	Is +WRITE TIME GATE (A1G2G03) plus while the sync is minus?	Change A1G2.
68	Is −XOUTA BIT 0 ALU2 TO DF (A1K2S13) minus when the sync is minus?	Change A1K2.
69	If not:	Change in order: 1. A2Q2 2. A2L2
70	Does −STAT BIT 3 DIAGNOSTIC MODE (A1K2G08) or −STAT BIT 2 TO DF (A1K2U09) go minus while the sync is minus?	Go to Seq 72.
71	If not:	Change A1K2.
72	Is the failure on a NRZI Write Tape Mark Command?	Change A2R2.
73	If not:	Change in order: 1. A2T2 2. B2E2

NOTES:

From 14-000

ERROR DESCRIPTION(Sense byte 10, Bit 4):

This bit is set when the turnaround counter overflows before the tape direction is reversed during a dynamic reversal of direction. A dynamic reversal takes place only when changing from read to write status and when changing from backward to forward direction. This bit is set when the beginning-of-tape (BOT) marker isn't found in the specified time after the tape control recognizes the SAGC burst during a read backward operation.

Most Probable Cause:

A. A2D2
B. Y1P2 (Y1 location, see 19-001)
C. A2E2

Always start with Seq 1 and follow the procedure in sequence unless otherwise directed.
Remember to END all problem or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Failure on more than one tape unit?	Change A2D2, Y1P2, A2E2.
2	This is a tape unit motion problem?	Go to 6B-000.
3	If not:	Recheck symptoms.

From 14-000 or 00-040

ERROR DESCRIPTION: (Sense Byte 10, Bit 2)

Sense Byte 10, Bit 2 is set when the tape unit fails to return the proper control status information to the tape control in response to a control tag and byte.

It is possible to get a CONTROL STATUS REJECT on a non-control command (Example: a write command). If you have this indication, try all control commands first.

When this bit is set, FRU ID sense byte 23 has the following meaning.

FRU Bit 0 On: Normal response to Rewind Unload command.
FRU Bit 1 On: Spare
FRU Bit 2 On: High sense level PE - 120%.
FRU Bit 3 On: Normal response to Set Alternate Density Command.
FRU Bit 4 On: Low sense level PE - 80%.
FRU Bit 5 On: Normal response to DSE command.
FRU Bit 6 On: Normal response to Set Erase command.
FRU Bit 7 On: Normal response to Rewind command.

FRU=00 Possible that the tape unit failed to recognize a control tag.
FRU/00 TU failed to respond to and/or recognize Bus Out bit
FRU=12 Valid response to Set SAGC on 6250 Write from Load Point.
Any other multi-bit response, excluding bit 2 or 4, is invalid.

The first part of this procedure is used to resolve some single tape unit failures as diagnosed in 00-040. If the failing command is not known, all control commands should be tried one at a time using Charts A through E on 16-213 as a guide. Be sure there are no hot bits on lines along with the correct response for each command.
If you have finished checking the CONTROL TAG responses without finding the error, go to 16-160 and check the COMMAND TAG responses.

Most Probable Cause:

The following is a list of the cards which can cause the problems covered in this procedure. The cards are listed with the highest probability first. Lines with multiple cards have the same probability.

Tape Control Cards: (multiple tape unit failures)
A. A1H2, A2R2 B. Y1Q2

Tape Unit Cards: (single tape unit failures)
Models 4, 6, 8
A. T-A1M2 D. T-A1J2 G. Read Card
B. T-A1L2 E. T-A1K2
C. T-A1K6 F. T-A1C2
Models 3, 5, 7
A. T-A1H2
B. T-A1L2
C. T-A1K4
D. T-A1J2
E. T-A1C2

Tape Control Unit: (Additional Cards Referenced)
A. A2N2
B. A2E2
C. Y1D2
D. A2D2
E. A2T2

Notes:

1. An MST line −0.85/−1.85 Vdc that is approximately at v-ref level (approx. −1.3 Vdc) is not terminated. This line is terminated on T-A1J2.
2. Special levels = minus (down) level is 0.0 Vdc and plus (up) level is +4.4 Vdc.

Always start with Seq 1 and follow the procedure in sequence unless directe d otherwise.
Remember to END all problem or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Does failure occur on more than one tape unit?	Go to Seq 89.
1A	Is this a Model 3, 5, or 7 tape unit?	Go to 6A-160.
2	In order to analyze the problem offline, the OLTs or LOGREC must be used to determine the failing command. When this error occurs, Sense Byte 23 contains the response byte from the tape unit. Perform the following steps to duplicate the failing command and allow scoping in a static condition: 1. Take tape unit offline and unload. 2. Disconnect I/O cable. 3. Switch tape unit online to allow scoping Bus In. 4. Reload and make tape unit Ready. 5. Ground −Control Tag I/O (T-A1K6D11) and the appropriate Bus Out pin (See Charts A and F, 16-213) Sense Byte 23 contains information to analyze this error.	
3	Are any of the following lines at the level indicated below? +Control Tag (T-A1K6D10) minus? −Command Tag (T-A1K6D09) minus? −Move Tag (T-A1K6B12) minus?	Change T-A1K6.
4	Use Charts B, C, and D on 16-213 to determine starting sequence. Use Charts E and F to determine correct response.	
5	**Note:** BUS IN 0 (Sense Byte 23, Bit 0) is normal response to a Rewind/Unload command. Is +Rwd Unload (T-A1M2D13) plus?	Go to Seq 9.
6	Is +Status Bus 0 (T-A1M2B05) plus?	Change T-A1M2.
7	Is −Bus In 0 (T-A1L2D02) minus?	Change T-A1L2.
8	If not:	Remove test jumpers.
9	Is +Set Rwd Unld Command (T-A1C2D06) minus?	Change T-A1C2.
10	Is −Bus Out 0 (T-A1J2D11) minus?	Change T-A1K6.
11	If not:	Recheck symptoms. Go to ALD pages to resolve.
12	Ground +Tape Present (T-A1C2S08).	
13	Is −Bus Out 0 (T-A1J2D11) plus? See Note 1.	Change T-A1K6.
14	Is +Set Rew Unload (T-A1C2D06) minus?	Change T-A1J2.
15	Is +Status Bus 0 (T-A1M2B05) minus?	Change T-A1M2.
16	Is −Bus In 0 (T-A1L2D02) plus? See Note 2.	Change T-A1L2.
17	If not:	Turn power off. Remove test jumpers and check continuity with a meter from T-A1: L2D02 to N2B02 and tailgate Y1J02, then K6B02 to N4B02 and tailgate Y1D02.
18	**Note:** Bus In 1 (Byte 23, Bit 1) is unused on a control command. Is +Status Bus 1 (T-A1M2B07) plus?	Change T-A1M2.
19	Is −Bus In 1 (T-A1L2D04) minus?	Change T-A1L2.
20	If not:	Remove test jumpers. Recheck symptoms. Go to ALD pages to resolve.
21	This bit is not used with Control Tag.	Recheck your symptoms.
22	**Note:** Bus In 2 Bit (Byte 23, Bit 2) is normal response to a Set High Sense PE. 120% Is +Status Bus 2 (T-A1M2G10) plus?	Change T-A1M2.
23	Is −Bus Out 2 (T-A1K2G10) minus?	Change T-A1K6.
24	Is +Status Bus 2A (T-A1K2D06) plus?	Change T-A1K2.
25	Is −Bus In 2 (T-A1L2D05) minus?	Change T-A1L2.
26	If not:	Remove test jumpers. Recheck symptoms. Go to ALD pages to resolve.
27	Is −Bus Out 2 (T-A1J2M04) plus?	Change T-A1K6.
28	Is +Status Bus 2A (T-A1K2D06) minus?	Change T-A1K2.
29	Is −Bus In 2 (T-A1L2D05) plus?	Change T-A1L2.
30	If not:	Turn power off. Remove test jumpers. Check continuity with a meter from T-A1: L2D05 to N2B04 and tailgate Y1J04, then K6B04 to N4B04 and tailgate Y1D04.
31	**Note:** Bus In 3 (Byte 23, Bit 3) is normal response to a Set Alt. Density command. Is +Gated 6250 BPI (T-A1M2D12) plus?	Change T-A1K2.
32	Is +Status Bus 3 (T-A1M2B04) plus?	Change T-A1M2.
33	Is +ARA On (T-A1K2U11) plus?	Scope +Initiate ARA (T-A1K2P12). If T-A1K2P12 is plus, change T-A1K2. If T-A1K2P12 is minus, change the read card.
34	Is +Status Bus 3A (T-A1K2J07) plus?	Change T-A1K2.
35	Is −Bus In 3 (T-A1L2D06) minus? See Note 2.	Change T-A1L2.
36	If not:	Remove test jumpers. Recheck symptoms. Go to ALD pages to resolve.

Seq	Condition/Instruction	Action
37	Is −Bus Out 3 (T-A1J2S09) plus? See Note 1.	Change T-A1K6.
38	Is +Initiate ARA (T-A1K2P12) minus?	Change T-A1K2.
39	Is + ARA On (T-A1K2U11). minus?	Check the read card cables. Change the read card.
40	Is + Status Bus 3A (T-A1K2J07) minus?	Change T-A1K2.
41	Is −Bus In 3 (T-A1L2D06) plus?	Change T-A1L2.
42	If not:	Turn power off. Remove test jumpers. Check continuity with a meter from T-A1: L2D06 to N2D05 and tailgate Y1G05, then K6B05 to N4D05 and tailgate Y1B05.
43	**Note:** Bus In 4 (Byte 23, Bit 4) is normal response to Set Low Sense PE 80% command. Is +Status Bus 4 (T-A1M2J09) plus?	Change T-A1M2.
44	Is −Bus Out 4 (T-A1K2G04) minus?	Change T-A1K6.
45	Is +Sum Of Tags (T-A1K2B05) minus?	Change T-A1J2.
46	Is +Status Bus 4A (T-A1K2S12) plus?	Change T-A1K2.
47	Is −Bus In 4 (T-A1L2D07) minus?	Change T-A1L2.
48	If not:	Remove test jumpers. Recheck symptoms. Go to ALD pages to resolve.
49	Is −Bus Out 4 (T-A1J2S07) plus? (see note.)	Change T-A1K6.
50	Is +Status Bus 4A (T-A1K2S12) minus?	Change T-A1K2.
51	Is −Bus In 4 (T-A1L2D07) plus?	Change T-A1L2.
52	If not:	Turn power off. Remove test jumpers. Check continuity with a meter from T-A1: L2D07 to N2B06 and tailgate Y1J06, then K6D06 to N4B06 and tailgate Y1D06.
53	**Note:** Bus In 5 (Byte 23, Bit 5) is normal response to Data Security Erase command. Is −Data Security Erase Latch (T-A1M2J05) minus?	Go to Seq 59.
54	Is +Status Bus 5 (T-A1M2P06) plus?	Change T-A1M2.
55	Is + Long Stop Response (T-A1H2M10) plus?	Change T-A1H2.
56	Is +Status Bus 7A (T-A1K2G13) plus?	Change T-A1K2.
57	Is −Bus In 5 (T-A1L2D09) minus?	Change T-A1L2.
58	If not:	Remove test jumpers. Recheck symptoms. Go to ALD pages to resolve.
59	Is −Bus Out 5 (T-A1J2M08) minus? (see note.)	Change T-A1K6.
60	If not:	Remove test jumpers and change T-A1J2.
61	Is −Bus Out 5 (T-A1J2M08) plus? (see note.)	Change T-A1K6.
62	Is −Data Security Erase Latch (T-A1M2J05) plus?	Change T-A1J2.
63	Is +Status Bus 5 (T-A1M2P06) minus?	Change T-A1M2.
64	Is + Long Stop Response (T-A1H2M10) minus?	Change T-A1H2.
65	Is −Bus In 5 (T-A1L2D09) plus?	Change T-A1L2.
66	If not:	Turn power off. Remove test jumpers. Check continuity with a meter from T-A1: L2D09 to N2D07 and tailgate Y1G06, then K6B07 to N4D07 and tailgate Y1B06.
67	**Note:** Bus In 6 (Byte 23, Bit 6) is normal response to a Set Erase command (Models 4, 6 and 8). Is +Status Bus 6 (T-A1M2B12) plus?	Change T-A1M2.
68	Is −Bus Out 6 (T-A1K2D04) minus?	Change T-A1K6.
69	Ground +Sense Reset (T-A1K2P09). Is T-A1K2M10 plus?	Remove test jumpers and change T-A1K2.
70	Remove test jumper (T-A1K2P09 to ground). Is +Status Bus 6A (T-A1K2G12) plus?	Change T-A1K2.
71	Is −Bus In 6 (T-A1L2D10) minus?	Change T-A1L2.
72	If not:	Remove test jumpers. Recheck symptoms. Go to ALD pages to resolve.
73	Is −Bus Out 6 (T-A1J2M10) plus? (see note.)	Change T-A1K6.
74	Is +Ststus Bus 6A (T-A1K2G12) minus?	Change T-A1K2.
75	Is −Bus In 6 (T-A1L2D10) plus?	Change T-A1L2.
76	If not:	Turn power off. Remove test jumpers. Check continuity with a meter from T-A1: L2D10 to N2B08 and tailgate Y1G08, then K6D07 to N4B08 and tailgate Y1B08.
77	**Note:** Bus In 7 (Byte 23, Bit 7) is normal response to a Rewind command. Is +Tie Up (T-A1M2U10) minus?	Change T-A1M2.
78	Is +Rwd Op (T-A1M2M04) plus?	Change T-A1C2.
79	Is +Status Bus 7 (T-A1M2J02) plus?	Change T-A1M2.
80	Is −Bus In 7 (T-A1L2D11) minus?	Change T-A1L2.
81	If not:	Remove test jumpers. Recheck symptoms. Go to ALD pages to resolve.
82	Is −Bus Out 7 (T-A1J2M07) plus? (see note.)	Change T-A1K6.
83	Is +Rewind/Unload (T-A1M2D13) plus?	Change T-A1C2.
84	Is −Set Rewind (T-A1C2B05) plus?	Change T-A1J2.
85	Is +Rewind Op (T-A1M2M04) minus?	Change T-A1C2.
86	Is +Status Bus 7 (T-A1M2J02) minus?	Change T-A1M2.
87	Is −Bus In 7 (T-A1L2D11) plus?	Change T-A1L2.
88	If not:	Turn power off. Remove test jumpers. Check continuity with a meter from T-A1: L2D11 to N2D09 and tailgate Y1J09, then K6B09 to N4D09 and tailgate Y1D09.
89	To check for hot TUBOs, set up the CE panel to stop ALU2 after executing 'Tubodown' on the failing command. Rotate the Selectable Register switch to DEVICE BUS OUT. The hot TUBOs will be displayed in this register and may be analyzed in a static condition while ALU2 is stopped at this address.	Go to Seq 90.
90	Is the TUBO Bit 0 indicator (A2R2S03) On?	Go to Seq 99.
91	Is the TUBO Bit 1 indicator (A2R2B12) On?	Go to Seq 103.
92	Is the TUBO Bit 2 indicator (A2R2D05) On?	Go to Seq 106.
93	Is the TUBO Bit 3 indicator (A2R2G02) On?	Go to Seq 110.
94	Is the TUBO Bit 4 indicator (A2R2B07) On?	Go to Seq 114.
95	Is the TUBO Bit 5 indicator (A2R2B10) On?	Go to Seq 126.
96	Is the TUBO Bit 6 indicator (A2R2G13) On?	Go to Seq 128.
97	Is the TUBO Bit 7 indicator (A2R2S02) On?	Go to Seq 130.
98	If not:	Go to Seq 132.
99	Is the tape unit executing a Rewind/Unload operation?	This is normal Bus Out status for a Rewind Unload operation. Recheck sense data.
100	Is +TUBO Bit 0 (A2R2D12) plus?	Change A1H2.
101	Is −B Bus 0 ALU2 (A2R2J07) plus?	Change A2N2.

Seq	Condition/Instruction	Action
102	If not:	Change in order: 1. A-A2R2 2. A-A2E2
103	Is +TUBO Bit 1 (A2R2B13) plus?	Change A1H2.
104	Is −B Bus 1 ALU2 (A2R2G05) minus?	Change A2N2.
105	If not:	Change in order: 1. A-A2R2 2. A-A2E2
106	Is +0 Pct Ampl Ctrl Trk 2 (A1H2U06) plus?	Change in order: 1. Y1D2 2. Y1Q2
107	Is +TUBO Bit 2 (A2R2B05) plus?	Change A1H2.
108	Is −B Bus 2 ALU2 (A2R2J05) minus?	Change A2N2.
109	If not:	Change in order: 1. A-A2R2 2. A-A2E2
110	Is +0 Pct Ampl Ctrl Trk 3 (A1H2M11) plus?	Change Y1Q2.
111	Is +TUBO Bit 3 (A2R2D13) plus?	Change A1H2.
112	Is −B Bus 3 ALU2 (A2R2J03) minus?	Change A2N2.
113	If not:	Change in order: 1. A-A2R2 2. A-A2E2
114	Is +TUBO Bit 4 (A2R2D09) plus?	Change A1H2.
115	Is −B Bus 4 ALU2 (A2R2M12) minus?	Change A2N2.
116	If not:	Change in order: 1. A-A2R2 2. A-A2E2
117	Is +TUBO Bit 5 (A2R2B09) plus?	Change A1H2.
118	Is −B Bus 5 ALU2 (A2R2M09) minus?	Change A2N2.
119	If not:	Change in order: 1. A-A2R2 2. A-A2E2
120	Is +TUBO Bit 6 (A2R2G12) plus?	Change A1H2.
121	Is −B Bus 6 ALU2 (A2R2U03) minus?	Change A2N2.
122	If not:	Change in order: 1. A-A2R2 2. A-A2E2
123	Is +TUBO Bit 7 (A2R2S02) plus?	Change A1H2.
124	Is −B Bus 7 ALU2 (A2R2P13) minus?	Change A2N2.

Seq	Condition/Instruction	Action
125	If not:	Change in order: 1. A-A2R2 2. A-A2E2
126	Is the tape control executing a Data Security Erase command? See Tape Unit Control Lines and Control Status Byte Response Chart E on 16-213.)	This is normal Bus Out status for a Data Security Erase command; recheck sense data.
127	If not:	Go to Seq 117.
128	Is the tape control executing an ERG command? (See Tape Unit Control Lines and Control Status Byte Response Chart E on 16-213.)	This is normal Bus Out status for an ERG command; recheck sense data.
129	If not:	Go to Seq 120.
130	Is the tape control executing a Rewind command? (See Tape Unit Control Lines and Control Status Byte Response Chart E on 16-213.)	This ia normal Bus Out status for a Rewind command; recheck sense data.
131	If not:	Go to Seq 123.
132	Using the failing commands, set up the CE panel to stop ALU2 after executing MSKSTS and press START. ALU2 should stop after MSKSTS to allow the Bus Out and Bus In lines to be scoped in a static condition. See Section 12-000 for instructions on CE panel use.	
133	Does ALU2 stop at this address?	Go to Seq 135.
134	Set up the CE panel to stop ALU1 one instruction after executing DLYTIME.	Go to Seq 135.
135	Is Bus In Bit 0 indicator On at Control time?	Go to Seq 144.
136	Is Bus In Bit 1 indicator On at Control time?	Go to Seq 147.
137	Is Bus In Bit 2 indicator On at Control time?	Go to Seq 149.
138	Is Bus In Bit 3 indicator On at Control time?	Go to Seq 151.
139	Is Bus In Bit 4 indicator On at Control time?	Go to Seq 153.
140	Is Bus In Bit 5 indicator On at Control time?	Go to Seq 155.
141	Is Bus In Bit 6 indicator On at Control time?	Go to Seq 158.
142	Is Bus In Bit 7 indicator On at Control time?	Go to Seq 161.
143	If not:	Recheck sense data.
144	Is the tape control executing a Rewind/Unload command?	This is normal response to a Rewind Unload command; recheck sense data.

Seq	Condition/Instruction	Action
145	Is −Device Bus In 0 To DF (A2T2M04) minus?	Change A2D2; if problem still exists, go to 18-010.
146	If not:	Change A2T2.
147	Is −Device Bus In 1 TO DF (A2T2P03) minus?	Change A2D2; if problem still exists, go to 18-010.
148	If not:	Change A2T2.
149	Is −Device Bus In 2 TO DF (A2T2M02) minus?	Change A2D2; if problem still exists, go to 18-010.
150	If not:	Change A2T2.
151	Is −Device Bus In 3 TO DF (A2T2J10) minus?	Change A2D2; if problem still exists, go to 18-010.
152	If not:	Change A2T2.
153	Is −Device Bus In 4 TO DF (A2T2P11) minus?	Change A2D2; if problem still exists, go to 18-010.
154	If not:	Change A2T2.
155	Is the tape control executing a Data Security Erase command?	This is a normal response at Control time; recheck sense data.
156	Is −Device Bus In 5 TO DF (A2T2M10) minus?	Change A2D2; if problem still exists, go to 18-010.
157	If not:	Change A2T2.
158	Is the tape control executing an Erase Record Gap command?	This is a normal response to an ERG command; recheck sense data.
159	Is −Device Bus In 6 TO DF (A2T2P07) minus?	Change A2D2; if problem still exists, go to 18-010.
160	If not:	Change A2T2.
161	Is the tape control executing a Rewind command?	This is a normal response to a Rewind command; recheck sense data.
162	Is −Device Bus In 7 To DF (A2T2P09) minus?	Change A2D2; if problem still exists, go to 18-010.
163	If not:	Change A2T2.

TAPE UNIT CONTROL LINES CHARTS

CHART A			CHART B			CHART C	CHART D
						Bus In Bit ON when should be OFF	Bus In Bit OFF when should be ON
Cntrl Tag	T-A1	K6D11					
Bus Out 0	T-A1	K6B02	Bus In 0	T-A1	L2D02	Go to Seq 5	Go to Seq 12
Bus Out 1	T-A1	K6B03	Bus In 1	T-A1	L2D04	Go to Seq 18	Go to Seq 21
Bus Out 2	T-A1	K6B04	Bus In 2	T-A1	L2D05	Go to Seq 22	Go to Seq 27
Bus Out 3	T-A1	K6B05	Bus In 3	T-A1	L2D06	Go to Seq 31	Go to Seq 37
Bus Out 4	T-A1	K6D06	Bus In 4	T-A1	L2D07	Go to Seq 43	Go to Seq 49
Bus Out 5	T-A1	K6B07	Bus In 5	T-A1	L2D09	Go to Seq 53	Go to Seq 61
Bus Out 6	T-A1	K6D07	Bus In 6	T-A1	L2D10	Go to Seq 67	Go to Seq 73
Bus Out 7	T-A1	K6B09	Bus In 7	T-A1	L2D11	Go to Seq 77	Go to Seq 82
	+4.4 is inactive 0.5 V is active			+4.4 is inactive 0.5 V is active			

CHART F

Failing Command	TU Bus Out Bits	TU Bus In Bits
Rewind Unload	0	0
Space	1	1
Set Diagnostic Mode (High Sense)	2	2
Set Alternate Density (Note 1)	3	3
Set Low (Diagnostic) Sense	4	4
DSE, Erase to TI	5	5
Set Erase Mode	6	6
Rewind	7	7

Notes: 1. Tape unit must be at load point.
2. Tape unit must be away from load point.

CHART E

Tape Unit Control Lines and Control Status Byte

Response Chart

Bit	Control Bus Out	Status Byte Bus In
0	Rewind Unload	Rewind Unload. Normal response to a Rewind Unload command.
1	Not used with a control tag.	Not used on Models 4, 6, and 8. Hot Bus In on Models 3, 5, and 7.
2	Set High Sense.	High Used in diagnostic program to check high setting of PE amp sensors on Models 4, 6, and 8. Hot Bus In on Models 3, 5, and 7.
3	Set Alternate Density and SAGC (Tape unit must be at load point.)	Alternate Density. Models 3, 5, and 7 tape units set to NRZI mode. Models 4, 6, and 8 tape units set to 6250 BPI mode. This bit is active after SAGC is set up.
4	Set Low Sense.	Low. Used in diagnostic program to check low setting of PE amp sensors on Models 4, 6, and 8. Hot Bus In on Models 3, 5, and 7.
5	Erase to TI (Data Security Erase) (See Note)	Erase. Normal response to DSE command.
6	Set erase mode.	Erase mode. Used only when going to a write status from a read status on Models 4, 6, and 8. Hot Bus In on Models 3, 5, and 7.
7	Rewind	Rewind. Normal response to a rewind command.

Note: To perform a DSE offline, see 12-000.

From: 14-000 or 15-060

ERROR DESCRIPTION:
Sense Byte 8, Bit 4 is set if the self-adjusting gain control (SAGC) cannot compensate for variations which cause read signal output in any track to remain below threshold. The SAGC Burst consists of six inches (15.24mm) of consecutive ones in all nine tracks. There is an 0.3-inch (7.62mm) interblock gap (IBG) between the SAGC Burst and the first data block. An inverse 6250 BPI tape mark approximately two inches long with consecutive ones in tracks 1, 2, 3, 4, 6, and 7 with no data in tracks P, 0, and 5 is added to the end of the burst to allow the tape unit to recognize the SAGC Burst when reading backwards.

6250 bpi Read Operation

During a 6250 BPI read operation when tape is at load point, the tape unit attempts to adjust the gain for each track while reading the SAGC Burst.

The following BOR and Interrupt conditions set sense bits for error recovery.

1. If BOR and Interrupt are both Off, Sense Byte 0, Bit 3 (Equipment Check) an are set.
2. If BOR if Off and Interrupt is On, Sense Byte 1, Bit 7 (Not Capable) and Sense Byte 8, Bit 4 (SAGC Check) are set.
3. If BOR is On and Interrupt is Off, no sense bits are set (normal condition).
4. If BOR and Interrupt are both On, Sense Byte 1, Bit 0 (Noise) and Sense Byte 8, Bit 4 (SAGC Check) are set and an attempt is made to read the first data block.

   Sense Byte 1, Bit 7 (Not Capable) is also set (without Sense Byte 8, Bit 4) if the inverse 6250 BPI tape mark (TM) is not recognized.

6250 bpi Write Operation During a 6250 BPI write operation when tape is at load point, the tape unit attempts to adjust the gain for each track while writing the SAGC Burst.

The following BOR and Interrupt conditions set sense bits for error recovery.

1. If BOR and Interrupt are both Off, Sense Byte 0, Bit 3 (Equipment Check) and Sense Byte 8, Bit 4 (SAGC Check) are set.
2. If BOR is Off and Interrupt is On, Sense Byte 5, Bit 3 (ID Burst Check) and Sense Byte 8, Bit 4 (SAGC Check) are set.
3. If BOR and Interrupt are both On, Sense Byte 5, Bit 3 (ID Burst Check) and Sense Byte 8, Bit 4 (SAGC Check) are set.
4. If BOR is On and Interrupt is Off, no sense bits are set (normal condition).

   Sense Byte 5, Bit 3 (ID Burst Check) and Sense Byte 8, Bit 4 (SAGC Check) are also set if the inverse tape mark (TM) is bad for consecutive 0.25-inch (6.35mm) segments over an approximate two-inch (50.8mm) distance.

Beginning of record (BOR) is defined as data detected in all tracks of one zone and data detected in at least one track in each of the other two zones.
Interrupt is defined as a Tape Unit Interrupt caused by one or more read head amplifiers having reached the gain limit for a write or read operation without Data Detected and/or Ready becoming inactive while Move was active.

Most Probable Cause:
The following cards can cause the problems covered in this procedure. The cards are listed with the highest probability first. Lines with multiple cards have the same probability.

A. A1H2
B. A1K2
C. A1G2
D. A2Q2, A2R2, A2T2, Y1P2, Y1T2
E. A1L2, Y1Q2

Additional Cards Referenced:
A. Y1S2
B. Y1R2
C. A2D2
D. Y1Q2
E. A2E2

EXPLANATION:
When writing from load point in 6250 BPI mode:

Ⓐ Tape is moved backward from load point for a distance of 150 capstan tach pulses.

Ⓑ Tape is erased forward.

Ⓒ Velocity is checked.

Ⓓ ALU2 writes the 6250 ID burst in track 1.

Ⓔ ID burst validity is verified.

Ⓕ ALU1 writes the SAGC burst. During the read-back of the SAGC burst, the SAGC circuits are adjusted for each track.

Ⓖ Near the end of the SAGC burst, the tape control tests for BOR. If BOR is not active, the tape control checks whether a TU Interrupt occurred. If both BOR and TU Interrupt are inactive, SAGC Check and Equipment Check are set. If BOR is inactive and TU Interrupt is active, ID Burst Check and SAGC Check are set.

Ⓗ The SAGC identification mark (inverse tape mark) is written by ALU1. If an early stop is detected, ID Burst Check and SAGC Check are set.

Ⓘ When the SAGC identification mark is recognized and a normal stop occurs, a test is made for a TU Interrupt condition. If TU Interrupt is active, ID Burst Check and SAGC Check are set.

When reading from load point in 6250 BPI mode:

Ⓓ Tape is read forward.

Ⓔ Recognizing the 6250 BPI ID burst sets the tape unit and tape control to operate in 6250 BPI mode.

Ⓕ The SAGC burst is read and the SAGC circuits adjust for each track.

Ⓖ Near the end of the SAGC burst, a test is made for BOR. If BOR is not recognized, a test is made for a TU Interrupt. When both are inactive, SAGC Check and Equipment Check are set. If TU Interrupt is active, SAGC Check and Not Capable are set.

Ⓗ When BOR has been recognized, ALU waits for the SAGC identification mark to be recognized. After the SAGC identification mark is recognized, a test is made for a TU Interrupt condition. If TU Interrupt is active, the SAGC Check and Noise bits are set.

BOR is defined as data detected in all tracks on one zone, and at least in one track of the other two zones.

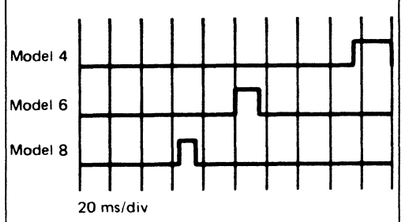
A TU Interrupt results if one or more amplifiers in the TU read card have reached the maximum gain limit without detecting data, or if the TU drops Ready with Move active.

Note: There may be some signal dropout that will not cause an error, depending upon how well the track(s) are written and read.

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise.
Remember to END all problem or maintenance calls by going to MAP 00-030.

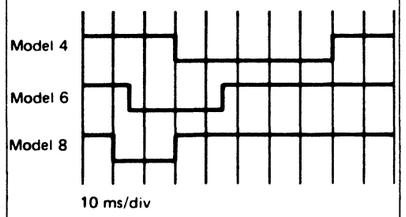
Seq	Condition/Instruction	Action
1	Is this a single tape unit failure?	Go to 5B-000.
1A	Mount a prewritten 6250 BPI tape on a Model 4, 6, or 8 tape unit. Reset, Load, and Ready the tape unit.	
2	Perform the following commands offline: 07 Rewind 02 Read 04 Sense 04 Sense Byte Cnt = 6A6 Wrt Data/Go Dwn = FF0	
3	Run with the Stop On Data Flow Check switch up. Press the RESET switch, set the ROS Mode switch to Norm, and press the START switch.	
4	Do the commands operate error-free? (No red light stop)	Go to Seq 12.
5	Set up an ALU1 Compare Stop on address 20A. Set the ROS Mode switch to Stop. Set Display Select switch to IC Reset and Start.	
6	After an error, turn off the Stop On Data Flow switch. Set the Mple/Single switch to Single. Press the START switch once. IC should indicate address 20A.	
7	Set Display Select switch to BUS IN for first sense byte. Record sense data.	
8	Set Display Select switch to IC. Press the Start/Step switch once.	
9	By repeating Seq 7 and Seq 8, all sense bytes can be checked. The following sense bits are significant in this procedure: Sense Byte 0, Bit 3 Equipment Check Sense Byte 1, Bit 0 Noise Sense Byte 1, Bit 7 Not Capable Sense Byte 5, Bit 3 ID Burst Check Sense Byte 8, Bit 4 SAGC Check	
10	Is Sense Byte 8, Bit 4 On?	An SAGC error occurred while reading the 6250 BPI tape. Go to Seq 30.
11	Is Sense Byte 1, Bit 7 On?	Go to Seq 37.
12	Mount a CE work tape on a Model 4, 6 or 8 tape unit.	
13	Set the Mple/Single switch to Mple. Perform the following commands offline: 07 Rewind 01 Write 04 Sense 04 Sense Byte Cnt = 6A6 Wrt Data/Go Dwn = FF0	

Seq	Condition/Instruction	Action
14	Run with the Stop On Data Flow Check Switch up.	
15	Do the commands operate error free? (No red light stop)	Go to Seq 22.
16	Set up an ALU1 Compare Stop on address 20A. Set the ROS Mode switch to Norm. Set the Display Select switch to IC, press the RESET switch and then the START switch.	
17	After an error, turn off the Stop On Data Flow switch. Set the ROS Mode switch to STOP and SET ROS MODE. Set the Mple/Single switch to Single. Press START once. IC should indicate address 20A.	
18	Set Display Select switch to BUS IN for first sense byte. Record sense data.	
19	Set Display Select switch to IC. Press the Start/Step switch once.	
20	By repeating Seq 18 and Seq 19, all sense bytes can be displayed. The following sense bits are significant in a write operation: Sense Byte 0, Bit 3 Equipment Check Sense Byte 5, Bit 3 ID Burst Check Sense Byte 8, Bit 4 SAGC Check	
21	Is Sense Byte 8, Bit 4 ON?	An SAGC error occurred while writing a 6250 BPI tape. Go to Seq 75.
22	If the SAGC error has not occurred in the above testing the failure may be intermittent, or false. If you suspect a false error, proceed to Seq 23; otherwise recheck the symptoms.	
23	If a tape unit is available with PE capability, mount a prewritten 1600 BPI tape on it. Reset, Load, and Ready the tape unit.	
24	Perform the following commands offline: 07 Rewind C3 PE Mode Set 02 Read 04 Sense Byte Cnt = 6A6 Wrt Data/Go Dwn = FF0	
25	Sync plus on +P Track Env Branch (A1K2U02).	
26	Is +1 Track Env Branch (A1K2P13) minus?	Change A2Q2.
27	Is –Time Sense 1 (A1K2U13) plus?	Change A1K2.
28	Is Bus In 1 TO DF (A2D2J02) pulsing?	Change A2D2.
29	If not:	Change Y1R2.
30	Set ROS Model to Norm. Set Mple/Single to Mple. Sync plus on +Tape Op Delayed (A1K2P03).	

Seq	Condition/Instruction	Action
31	The SAGC portion of the first record should have the following minimum width when operating correctly: Model 4 200 ms Model 6 120 ms Model 8 75 ms	
32	Scope +1 Track Env Branch (A1K2P13) (see Note on 16-220).	
33	+1 Track Env Branch should go plus after the sweep starts and stay plus for approximately: See Note on 16-220) Model 4 85 ms Model 6 48 ms Model 8 30 ms When the Track 1 ID Burst is recognized, the tape control is set to 6250 BPI mode.	
34	Is Sense Byte 0, Bit 3 or Sense Byte 1, Bit 7 On?	BOR is not being recognized. Go to Seq 46.
35	**Scope +SAGC 6 Combination (Y1P2S11).**	
36	Is this signal going plus and staying plus approximately as follows: 	SAGC Burst ID is being recognized. Go to Seq 59.
37	Set up an ALU2 Compare on address 299 (RESET BOR). Set ROS Mode switch to Norm. Set Mple/Single switch to Mple.	
38	Sync minus on –CE Select Reg Pulse (A1U2U07). This sync occurs before the SAGC ID. Set sweep to 5 ms/div.	
39	Is +DCC Error Or SAGC Branch (A2D2M09) going plus approximately as follows: Model 4 from 8 ms to 36 ms after the sync. Model 6 from 5 ms to 21 ms after the sync. Model 8 from 3 ms to 13 ms after the sync. See Note on 16-220.	Change A2D2.
40	**Is +SAGC 6 Combination (Y1P2S11) going plus approximately the same as in Seq 41.**	Recheck Seq 41. (same line after dot OR)

Seq	Condition/Instruction	Action
41	Scope the –Time Sense lines for the level as indicated: **Zone 1:** TRK P Y1P2P03 (plus) 0 Y1P2P09 (plus) 5 Y1P2D10 (plus) **Zone 2:** TRK 2 Y1P2G13 (minus) 6 Y1P2M12 (minus) 7 Y1P2G12 (minus) **Zone 3:** TRK 1 Y1P2P02 (minus) 3 Y1P2P10 (minus) 4 Y1P2S12 (minus)	
41	(continued) (See Note on 16-220). The above levels should be observed approximately: Model 4 from 8 ms to 36 ms Model 6 from 5 ms to 21 ms Model 8 from 3 ms to 13 ms	
42	Do all of the above line levels have the indicated duration and level?	Change in order: 1. Y1P2 2. A1L2
43	Scope Device Bus In X to DF lines for the following conditions during the SAGC ID: **Zone 1: NOT PULSING** TRK P A2D2P06 0 A2D2J05 5 A2D2D07 **Zone 2: PULSING** TRK 2 A2D2J03 6 A2D2B07 7 A2D2B09 **Zone 3: PULSING** TRK 1 A2D2J02 3 A2D2J04 4 A2D2B10 (See Note on 16-220.) Model 4 from 8 ms to 36 ms Model 6 from 5 ms to 21 ms Model 8 from 3 ms to 13 ms	
44	Are all of the above lines correct?	Change the VFC cards for any lines failing in Seq 41: Zone 1—Y1T2 Zone 2—Y1S2 Zone 3—Y1R2
45	If not:	Change A2D2. If failure still occurs, try another prewritten 6250 BPI tape. Then try another tape unit.
46	Set up an ALU2 Compare on address 290. (NORMDONE +2)	

Seq	Condition/Instruction	Action
47	Sync minus on –CE Select Reg Pulse (A1U2U07). 10 ms/div.	
48	This sync occurs at the beginning of the SAGC burst.	
49	Are the following –Time Sense lines at a minus level for at least 10 ms between the following: See Note on 16-220. Model 4 from 20 ms to 70 ms Model 6 from 11 ms to 40 ms Model 8 from 7 ms to 25 ms **Zone 1:** TRK P Y1P2P03 0 Y1P2P09 5 Y1P2D10 **Zone 2:** TRK 2 Y1P2G13 6 Y1P2M12 7 Y1P2G12 **Zone 3:** TRK 1 Y1P2P02 3 Y1P2P10 4 Y1P2S12	Go to Seq 57.
50	Scope the following –Device Bus In X To DF lines for a pulsing condition: Model 4 from 17 ms to 70 ms Model 6 from 11 ms to 40 ms Model 8 from 7 ms to 25 ms **Zone 1:** TRK P A2D2P06 0 A2D2J05 5 A2D2D07 **Zone 2:** TRK 2 A2D2J03 6 A2D2B07 See Note 7 A2D2B09 on 16-220. **Zone 3:** TRK 1 A2D2J02 3 A2D2J04 4 A2D2B10	
51	Are all of the lines in Seq 50 pulsing correctly? Are all of the lines in Seq 49 plus when they should be minus?	Go to Seq 55.
52	Are all of the lines in Seq 50 pulsing correctly? Are all of the lines in one zone at a plus level in Seq 49, when they should be minus?	Change the card for the failing zone: Zone 1, Y1T2 Zone 2, Y1S2 Zone 3, Y1R2 Then change Y1Q2.
53	Are all of the lines in Seq 50 pulsing?	Change the cards for any lines failing in Seq 49: Zone 1—Y1T2 Zone 2—Y1S2 Zone 3—Y1R2

Seq	Condition/Instruction	Action
54	If not:	Change A2D2. If failure still occurs, try another prewritten 6250 BPI tape. Then try another tape unit.
55	Is –XOUTA Bit 4 ALU2 To DF (A1K2D09) at a minus level from sync 0 ms to 40 ms?	Change: 1. A1K2 2. Y1Q2
56	If not:	Change A2Q2.
57	Set the horizontal sweep to 10 ms/cm. Set the vertical sweep to 1 volts/cm. Scope –BOR 27 Comb or DT Branch Cond (Y1P2J13) for a signal going minus approximately as indicated:  	Change A2D2.
58	If not:	Change Y1P2.
59	Is Sense Byte 1, Bit 0 (Noise) On?	Go to Seq 61.
60	If not:	Go to Seq 39.
61	Set up an ALU2 Compare on address 29D. (BRSTCK3)	
62	Sync minus on –CE Select Reg Pulse (A1U2U07). Set sweep to 1 usec.	
63	Does the tape control have a 2x8, 3x8 or 4x8 Device Switch feature?	Go to Seq 68.
64	Is –Interrupt (A2D2S11) plus?	Change A2D2.
65	Scope the –DE Interrupt X line corresponding to the tape unit being used. **Tape Unit Test Point** 0 A2E2S12 1 M03 2 S05 3 J13 4 S02 5 P03 6 U06 7 G04 (Line level is +4v to 0v.)	
66	Was the line corresponding to the tape unit in use at a minus level?	Go to Seq 72.
67	If not:	Change A2E2.

Seq	Condition/Instruction	Action
68	Is –Interrupt (A2D2G12) plus?	Change A2D2.
69	Is –DE Irpt PRI (A2D2P03) minus? (Line level is +4v to 0v.)	Go to Seq 72.
70	Is –DE Irpt Sec (A2D2U07) minus? (Line level is +4v to 0v.)	Go to Seq 72.
71	If not:	Change A2D2.
72	Is the interrupt occurring during a write operation?	Go to Seq 74.
73	This is a valid interrupt signal, but may be due to a tape unit failure, selection logic, or switch path failure. Try another tape unit and/or path.	Go to 18-000, 18-010, or 5B-000.
74	This is a valid interrupt signal, but may be due to a failure to send write pulses to the tape unit. Do not proceed to Seq 75.	Go to Seq 106.
75	A SAGC error occurrs only when writing a tape from load point in 6250 BPI mode. Set ROS to Normal Mode. Set Mple/Single switch to Mple. Press RESET and then operate START.	
76	Set up an ALU2 Compare on address 70B (WRT6) and use ALU "Babysitter" Setup Number 4 on 12-010 for this and the following sequences.	
77	Does the Cmpr Equal light come On during every write operation?	Go to Seq 79.
78	If not:	Go to Seq 12 and recheck your work.
79	Set up an ALU2 Compare on address 72C (ID 14).	
80	Does the Cmpr Equal light come On during every write operation?	SAGC ID is being recognized. Go to Seq 90 to check for an interrupt from the tape unit.
81	Set up an ALU2 Compare on address 725 (ID5 +1), and use "babysitter".	
82	Does the Cmpr Equal light come On during every write operation?	BOR is being recognized. Go to Seq 97 to check SAGC ID failure.
83	Set up ALU2 Compare on address 71F (WRT90) and use "babysitter".	
84	Does the Cmpr Equal light come On during every write operation?	BOR is being recognized. Change A2D2.
85	Set up an ALU2 Compare on address 71B (DTASAGC) and use "babysitter".	
86	Does the Cmpr Equal light come On during every write operation?	BOR is not being recognized and an interrupt is occurring. Go to Seq 106 to check BOR failure.
87	Set up an ALU2 Compare on address 719 (EQSAGC) and use "babysitter"	
88	Does the Cmpr Equal light come On during every write operation?	BOR is not recognized, and no interrupt is occurring. Go to Seq 106 to check BOR failure.

SAGC CHECK (Cont'd)

Seq	Condition/Instruction	Action
89	If not:	Recheck your symptoms. Go to Seq 1.
90	Set up an ALU2 Compare on address 71B (DTASAGC) and use "babysitter".	
91	Does the Cmpr Equal light come On?	An interrupt is recognized after SAGC ID. Go to Seq 94 to check for an interrupt from the tape unit.
92	Set up an ALU2 Compare on address 72D (ID145) and use "babysitter".	
93	Does the Cmpr Equal light come On? This is beyond where a SAGC check can be set. Do not proceed to Seq 94.	Go to Seq 12 and recheck your work.
94	Set up an ALU Compare on address 72C (ID14).	
95	Sync minus on –CE Select Reg Pulse (A1U2U07). Set sweep at 1 usec/div.	
96	Using the above sync, a check will be made for an interrupt from the tape unit, starting at Seq 63. Observe the following lines within 3 usec of sync. Do not proceed to Seq 97.	Go to Seq 63.
97	Set up an ALU1 Compare on address 649. (SAGCNTM1) Sync minus on –CE Select Reg Pulse (A1U2U07). Set sweep at 5 ms/div.	
98	The following sequences are to determine if an SAGC identification mark is being written.	
99	Ensure that all of the following write trigger lines are at the condition indicated: **Zone 1: Should be at indicated level** at beginning of sweep. A1H2U07 –TUBO BIT P (plus) M10 +TUBO BIT 0 (minus) J07 +TUBO BIT 5 (minus) **Zone 2: SHOULD** pulse at beginning of sweep. A1H2U05 +TUBO BIT 2 M04 +TUBO BIT 6 J13 +TUBO BIT 7 **Zone 3: SHOULD** pulse at beginning of sweep. A1H2S10 +TUBO BIT 1 P09 +TUBO BIT 3 J03 +TUBO BIT 4	This is the correct output for a SAGC identification mark (inverse TM). Go to Seq 104.
100	Are any of the following lines plus? +0 PCT Ampl Ctrl Trk P A1H2S09 + PCT Ampl Ctrl Trk 0 A1H2P11 + PCT Ampl Ctrl Trk 5 A1H2J10 + PCT Ampl Ctrl Trk 2 A1H2U06 + PCT Ampl Ctrl Trk 6 A1H2P06 + PCT Ampl Ctrl Trk 7 A1H2P02 + PCT Ampl Ctrl Trk 1 A1H2U11 + PCT Ampl Ctrl Trk 3 A1H2M11 + PCT Ampl Ctrl Trk 4 A1H2J05	Change Y1Q2.
101	Is only one line failing in Seq 99?	Change A1H2.
102	Are all the following control lines at a minus level at the beginning of the sweep? A1H2G04 –XOUTA Bit 2 To DF J06 –Gate Write Not TM D03 –Gate Write	Change in order: 1. A1H2 2. A1G2
103	If not:	Change in order: 1. A1G2 2. A1K2 3. A2T2
104	Are all of the following lines at the condition indicated: **Zone 1: Should NOT** pulse at beginning of sweep. A2E2J06 –TUBO BIT P J09 –TUBO BIT 0 P06 –TUBO BIT 5 **Zone 2: SHOULD** pulse at beginning of sweep. A2E2D05 –TUBO BIT 2 P09 –TUBO BIT 6 S10 –TUBO BIT 7 **Zone 3: SHOULD** pulse at beginning of sweep. A2E2D02 –TUBO BIT 1 D07 –TUBO BIT 3 D10 –TUBO BIT 4	Change A2E2.
105	If not:	Change A2R2.
106	Set up an ALU2 Compare on address 70B (WRT 6).	
107	Sync minus on –CE Select Reg Pulse (A1U2U07). Set sweep at 20 ms/div.	
108	Are all of the write trigger lines pulsing? **Zone 1:** A1H2U07 –TUBO BIT P M10 +TUBO BIT 0 J07 +TUBO BIT 5 **Zone 2:** A1H2U05 +TUBO BIT 2 M04 +TUBO BIT 6 J13 +TUBO BIT 7 **Zone 3:** A1H2S10 +TUBO BIT 1 P09 +TUBO BIT 3 J03 +TUBO BIT 4	This is the correct output for the SAGC Burst. Go to Seq 114.
109	Are any of the following lines plus? +0 PCT Ampl Ctrl Trk P A1H2S09 + PCT Ampl Ctrl Trk 0 A1H2P11 + PCT Ampl Ctrl Trk 5 A1H2J10 + PCT Ampl Ctrl Trk 2 A1H2U06 + PCT Ampl Ctrl Trk 6 A1H2P06 + PCT Ampl Ctrl Trk 7 A1H2P02 + PCT Ampl Ctrl Trk 1 A1H2U11 + PCT Ampl Ctrl Trk 3 A1H2M11 + PCT Ampl Ctrl Trk 4 A1H2J05	Change Y1Q2.
110	Is only one line failing in Seq 108?	Change A1H2.
111	Is only Zone 1 failing in Seq 108?	Change: 1. A2T2 2. A1H2
112	Are all the following control lines at the condition indicated? **Line Name** **Test Point** **State** +Mark2 A1H2U03 Solid + +Mark11 D13 Solid + +Format J11 Solid + –Gate Write Not TM J06 Solid – –Gate Write D03 Solid – –Write Condition B02 Solid – The above levels should be observed approximately as follows: Model 4 from 0 ms to 70 ms Model 6 from 0 ms to 40 ms Model 8 from 0 ms to 25 ms	Change in order: 1. A1H2 2. A1G2
113	If not:	Change in order: 1. A1G2 2. A1K2 3. A2T2
114	Are all of the following lines pulsing? –TUBO BIT P A2E2J06 –TUBO BIT 0 J09 –TUBO BIT 5 P06 –TUBO BIT 2 D05 –TUBO BIT 6 P09 –TUBO BIT 7 S10 –TUBO BIT 1 D02 –TUBO BIT 3 D07 –TUBO BIT 4 D10	Change A2E2.
115	If not:	Change A2R2.

NOTES:

3803-2/3420

XF1700 Seq 2 of 2	2735913 Part Number	See EC History	845958 1 Sep 79					

P COMPARE OR C COMPARE ERRORS

From 14-000, 17-510, 17-590

ERROR CONDITIONS:

Sense Byte 3, Bit 7 is set by P Check Channel Buffer, Write Data Parity Error, Buffer Error, CRC Set P Compare error or C Compare error.

A. P Check Channel Buffer is set when parity of the byte sent to the Channel Buffer is even.

B. Write Data Parity error is set when there is no match between Channel Buffer Out P and Write Bit P which is encoded and written on tape.

C. Buffer error is set by Buffer Overrun or Write Address error, or if Service Response count does not equal Channel Read Out Counter (CROC) after all data has been read from the Channel Buffer.
   1. Buffer Overrun is set when the Write Group Buffer is empty while more data is read out.
   2. Write Address Error is set when Channel Read in Counter (CRIC) is even and Service Response pulses are odd, or CRIC is odd and Service Response pulses are even.

D. CRC Set P compare error is set when CRC-A does not match CRC-B. CRC-A is a CRC character generated from accumulated data in the channel buffer. CRC-B is a CRC character generated from accumulated data from the Read register.

E. C Compare error is set only when operating in 7-track data convert mode.
   Read: C Compare is set when combined data P does not match read data track P.
   Write: C Compare is set when Channel Buffer Out P does not match Write Bus P.
   C Compare checks that correct parity (odd or even) is maintained by the tape control while processing 7-track NRZI data. C compare is set under the following conditions:
   1. Translator off and Data Converter off: If parity of an individual byte changes within the tape control while reading or writing.
   2. Data Converter on and Translator off:
      a. During 7-track read operations, if the parity of a group of 4 BCD characters changes within the tape control.
      b. During 7-track write operations, if the parity of a group of 3 EBCDIC bytes changes within the tape control.
   3. Translator on and Data Converter off: During 7-track operations with translator on and data converter off, C Compare is always off.

F. Bus Out Parity Error can cause C Compare.

G. Data converter check blocks C compare if the DCC occurs first.

MOST PROBABLE CAUSE:

The following list is of the known cards which can cause the problems covered in this procedure. The cards are listed with the highest probability first. Lines with multiple cards have the same probability.

A. A1F2
B. A1E2
C. A1G2
D. A1C2
E. A1L2
F. A1D2
G. A1K2
H. Y1F2, Y1G2
I. A2Q2
J. A1H2, A2L2, A2T2, B2E2, Y1D2, Y1H2, Y1J2, Y1T2

ADDITIONAL CARDS AFFECTED:

A. B2M2
B. B2L2
C. Y1C2

Seven-track and nine-track NRZI do not require a timing chart for this procedure.

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problems or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Take the tape control offline and try the following commands in the order listed. The Stop On Data Flow switch should be on so that a P/C Compare error can be recognized. 1. Rewind 2. LWR with gaps (6250 and PE mode) 3. Write (all modes) 4. Read Forward (all modes using prewritten test tape). 5. Read Backward (6250, PE, and 9-Track NRZI modes). **Note:** Operation may fail on only certain byte counts.	
2	Does the tape control fail from the CE panel on one of the operations in Seq 1?	Go to Seq 4.
3	If the system is available, set up the system to loop on error, and use the OLT FRIEND program to determine the failing operation.	
4	Is a P/C Compare error occurring during a rewind operation?	Go to Seq 135.
5	Sync the scope minus on –P or –C COMPARE (A1K2B13).	
6	Is the tape control failing in 7-track mode only? See Mode Chart on 17-013.	Go to Seq 113.
7	If 7-track feature is installed, is +C COMP ERROR (A1K2M13) plus at sync time?	Change A1L2.
8	Is –BUFFER ERROR TP (A1C2S05) minus at sync time?	Go to Seq 86.
9	Execute a Read Forward and a Read Backward on a previously written tape. Then execute a write operation. Do both read-type and write-type operations fail?	Go to Seq 70.
10	Does the tape control fail only on write operations?	Go to Seq 28.
11	Is +P COMPARE CHECK (A1F2M11) minus at sync time?	Go to Seq 65.
12	Is –READ & TAPE OP (A1K2U12) plus?	Change A1K2.
13	Is +SET WRITE REG (A1D2P12) minus?	Change A1D2.
14	Is –25-75 CLOCK BUS A1 DELAYED (A1C2U12) pulsing?	Go to Seq 16.
15	If not:	Change A1C2.
16	Is –0-50 CLOCK BUS A1 DELAYED (A1C2S10) pulsing?	Go to Seq 18.
17	If not:	Change A1C2.
18	Are you operating in 9-track NRZI mode? See Mode Chart on 17-013.	Go to Seq 24.
19	Is –NRZI MODE (A1K2D10) minus?	Change A1K2.
20	Did a CRC error occur (Sense Byte 3, Bit 3)?	Go to Seq 22.
21	If not:	Change A1F2.
22	Did a read/Write VRC Error occur (Sense Byte 3, Bit 0)?	Go to 17-168.
23	If not:	Change in order: 1. Y1G2 2. A1F2
24	Is –NRZI MODE (A1K2D10) plus?	Change A1K2.
25	Did a CRC Error occur (Sense Byte 3, Bit 3) in 9-track NRZI read?	Change in order: 1. Y1D2 2. Y1C2
26	Is an odd number of –RD DATA TK x lines minus at sync time? See Test Points Chart for –RD Data TRK x on 17-013.	Change A1F2.
27	If not:	Change Y1D2.
28	Is +P COMPARE CHECK (A1F2M11) plus at sync time?	Go to Seq 59.
29	Sync the scope minus on –WRT AND TAPE OP (A1F2G13).	
30	Is –CRC GATE (A1G2P03) pulsing? (See timing chart on 17-015.)	Go to Seq 32.
31	If not:	Change in order: 1. A1F2 2. A1C2
32	Is –RESIDUAL GATE (A1G2J04) good? (See 6250 timing chart on 17-015.) This line should be at a solid plus level for PE or NRZI operations.	Go to Seq 34.
33	If not:	Change in order: 1. A1F2 2. A1C2
34	Is –ORC GATE (A1G2J07) good? (See 6250 timing chart on 17-015.) This line should be at a solid plus level for PE or NRZI operations.	Go to Seq 36.
35	If not:	Change in order: 1. A1F2 2. A1C2
36	Is –READ CYCLE (A1F2B05) good? (See timing chart on 17-015.)	Go to Seq 47.

P COMPARE OR C COMPARE ERRORS (Cont'd)

Seq	Condition/Instruction	Action
37	Does –0-50 CLOCK BUS A1 DELAYED (A1C2S10) fail to pause?	Change A1C2.
38	Does –25-75 CLOCK BUS A1 DELAYED (A1C2U12) fail to pulse?	Change A1C2.
39	Is +READ CYCLE RESET (A1F2D10) always a solid plus or minus level?	Change A1F2.
40	Does –FULL FRAME (A1F2J10) shift from plus to minus during the time-Write Condition (A1G2S07) is minus?	Go to Seq 43.
41	Is ALLOW CRIC (A1F2B04) plus all the time that –WRITE CONDITION (A1G2G07) is minus?	Change Y1H2.
42	If Not:	Change A1F2.
43	Does –WRITE GROUP BUFFER EMPTY (A1F2G05) remain plus all the time that –WRITE CONDITION is minus?	Change A1C2.
44	Does –BUFFER EMPTY TO CHANNEL (A1E2G07) fail to go minus while –WRITE CONDITION is minus?	Change A1E2.
45	Does –READ BYTE BUFFER EMPTY (A1C2S07) fail to go from plus to minus during the time –WRITE CONDITION is minus?	Change A1C2.
46	If not:	Change in order: 1. A1F2 2. A1C2 3. A1E2 4. A1G2
47	Is –SET ANY BYTE (A1G2U03) good? See timing chart on 17-015.	Go to Seq 56.
48	Is –25-75 CLOCK BUS A1 DELAYED (A1C2U12) failing to pulse?	Change A1C2.
49	Is +SET WRITE DATA A (A1F2P03) good?	Go to Seq 52.
50	Is –25-75 CLOCK BUS A1 DELAYED (A1C2U12) pulsing?	Change A1F2.
51	If not:	Change A1C2.
52	If the 7-track feature is installed, are the signals seen in Seq 49 also on +SET WR DATA FEEDBACK (A1L2G12)?	Go to Seq 54.
53	If not:	Change A1L2.
54	Are all of the following lines good? See timing chart on 17-014. +SET BYTE 1 A1F2J07 +SET BYTE 2 A1F2B13 +SET BYTE 3 A1F2G08 +SET BYTE 4 A1F2D13	Change A1H2.
55	If not:	Change A1F2.
56	Sync scope negative on –P OR C COMPARE (A1K2B13). Use this sync for steps 57 through 76.	
57	Are –WRT BUS BIT P (A1G2B11) and –CHANNEL BUFFER P (A1G2M02) at the same level (plus or minus) at sync time?	Change in order: 1. A1G2 2. A1F2
58	If not:	Review symptoms. Go to Seq 1.
59	Is –READ AND TAPE OP (A1K2U12) minus at sync time?	Change A1K2.
60	Is +SET WRITE REG (A1D2P12) minus at sync time?	Change A1D2.
61	Is –WRITE DATA READY (A1C2S04) a plus level at sync time?	Change A1C2.
62	Is +WRITE CYCLE DELAYED (A1F2J09) plus at sync time?	Change A1F2.
63	Is an odd number of BUS OUT BIT lines active at sync time? (See Test Point Chart on 17-013.)	Change A1F2.
64	If not:	With EC733814, change B2M2. Without EC733814, change B2L2.
65	Using a previously written test tape, do a 6250 bpi Read Forward from the CE panel with the Stop on Error switch ON.	
66	Using 12-012, Seq 15, obtain the sense after a Stop on Error.	
67	Did a CRC error occur (Sense Byte 3, Bit 3)?	Change A1C2.
68	Does OLT Section D run without Error?	Change A1D2.
69	If not, or don't know:	Change in order: 1. A1F2 2. A1D2
70	Is +P COMPARE CHECK (A1F2M11) plus at sync time?	Change A1F2.
71	Using a previously written tape, do a 6250 bpi Read Forward from the CE panel with the Stop on Error switch ON.	
72	Use 12-012, Seq 15, to obtain the sense data after a Stop on Error.	
73	Did a CRC error occur (Sense Byte 3, Bit 3)?	Go to Seq 76.
74	Does OLT Section D run without error?	Change A1D2.
75	If not:	Change in order: 1. A1F2 2. A1D2
76	Is –B EQUAL A TP (A1D2J10) minus at sync time?	Change A1D2.
77	Sync negative on –TAPE OP (A1C2M11).	
78	Is the tape control failing on a write operation?	Go to Seq 83.
79	Is –READ AND TAPE OP (A1K2U12) plus during the time the sync signal is minus?	Change A1K2.
80	Does –ALLOW CRIC (A1D2P03) remain plus all the time the sync signal is minus?	Change Y1H2.
81	Does –CB WRITE PULSE (A1F2D05) remain plus all the time the sync signal is minus?	Change A1F2.
82	If not:	Change A1D2.
83	Is –READ AND TAPE OP (A1K2U12) minus any time that the sync is minus?	Change A1K2.
84	Does –SET WRT REGISTER (A1C2G05) stay plus all the time that the sync is minus?	Change A1C2.
85	If not:	Change A1D2.
86	Is –WRT ADDRESS ERROR TP (A1C2P04) minus at sync time?	Go to Seq 97.
87	Is –WRT BUFFER OVERRUN (A1G2J09) minus at sync time? Look for 50 ns pulse.	Go to Seq 105.
88	Is –WR AND TAPE OP NOT CTL (A1K2P09) minus at sync time?	Change A1K2.
89	Is –SPARE XFR 18 (A2L2G11) a solid minus?	Change A2L2.
90	Sync negative on –SPARE XFR 18 (A1C2J11)	
91	Using the CE panel, do a LWR (8B) away from load point. Use a byte count of 1D0 (hex) from the CE panel.	
92	Scope the following lines: –CROC REG 1 A1C2D10 –CROC REG 2 A1C2D09 –CROC REG 4 A1C2B09 –CROC REG 8 A1C2B07 –CROC REG 16 or NOT READ CYCLE A1C2D07	
93	Is one or more of the lines in Seq 92 plus at sync time?	Change A1F2.
94	Using the CE panel, do a LWR (8B) operation with tape away from load point. Use a byte count of 1E0 (hex).	
95	Scope the lines in Seq 92. Is one or more of the lines plus at sync time?	Change A1E2.
96	If not:	Change A1C2.
97	Sync negative on –WRT CONDITION (A1G2G07).	

COMPARE OR C COMPARE ERRORS (Cont'd)

Seq	Condition/Instruction	Action
98	Is +CRIC REG 1 POWERED (A1F2G03) good? (See Timing Chart on 17-014.)	Go to Seq 102.
99	Is −ALLOW CRIC (A1F2B04) failing to go minus?	Change Y1H2.
100	Does +READ CHAN BFR (A1F2P11) remain a solid plus?	Change A1F2.
101	Does −END WRITE SEQUENCE (A1F2G07) remain at a solid minus during sync time?	Change A1F2.
102	Does −FULL FRAME (A1F2J10) fail to go minus during the time the sync is minus?	Change A1F2.
103	Does −CB WRITE PULSE (A1F2D05) fail to pulse?	Change A1F2.
104	If not:	Change A1C2.
105	Sync negative on −WRT CONDITION (A1G2G07).	
106	Is +SET BYTE 2 (A1F2B13) good? (See Timing Chart on 17-015.)	Go to Seq 108.
107	If not:	Change A1F2.
108	If the 7-track feature is installed, does +SET BYTE 2 FROM DCA (A1E2G02) have the same signal as in Seq 106?	Go to Seq 110.
109	If not:	Change A1E2.
110	Is +SET BYTE 4 (A1F2D13) good? (See Timing Chart on 17-015.)	Go to Seq 112.
111	If not:	Change A1F2.
112	Then:	Change in order: 1. A1G2 2. A2T2
113	Is machine in Translate mode?	Change A1L2.
114	Does the tape control fail on both Read and Write operations?	Change A1L2.
115	Does the tape control fail on both read and write operations?	Go to Seq 128.
116	Is −READ AND TAPE OP (A1L2S04) minus?	Change A1K2.
117	Sync minus on +FOURTH BYTE (A1L2U03) with sweep at 1 us/div.	
118	Does +C COMPARE ERROR (A1L2S13) go from minus to plus at the beginning of the sync?	Change A1E2. If that doesn't fix the problem, change A1L2.
119	Write a record using failing byte count determined in Seq 1. Sync positive on and display +SET BYTE 2 (A1L2S08).	
120	Count the number of +SET BYTE 2 pulses while −CHANNEL BUFFER OUT P (A1L2U06) is plus.	
121	Sync positive on and display +SET BYTE 2 FROM DCA (A1L2S07).	
122	Count the number of +SET BYTE 2 FROM DCA pulses while −WRITE BUS BIT P (A1L2U05) is plus.	
123	Is the number of pulses in Seq 120 and 122 equal?	Change A1L2.
124	Is +EVEN PARITY (A1G2M04) plus?	Go to ALD BN311DM2 and follow the line back to the failing point.
125	Is −DATA CONVERTER ON (A1E2M12) plus?	Go to ALD BN311DK6 and follow the line back to the failing point.
126	Is −STAT BIT 3 7-TRACK (A1E2P09) plus?	Go to ALD AA141EG6 and follow the line back to the failing point.
127	If not:	Change A1E2.
128	Write a tape using failing byte count; then read it to analyze failure.	
129	Sync negative on and display −REG CB WRITE CYCLE (A1L2U07).	
130	Count number of −REG CB WRITE CYCLES while −COMBINED ECC DATA P (A1L2S02) is plus.	
131	Sync minus on and display −CB WRITE PULSE (A1L2M04).	
132	Count the number of −CB WRITE PULSES while −RD DATA TK P (A1L2S05) is plus.	
133	Is the number of pulses in Seq 130 and Seq 132 equal?	Change A1L2.
134	If not:	Go to Seq 124.
135	Is +RESET SENSE DATA (A1K2D12) always minus? (Pulses are very short and very hard to see.)	Change A1K2.
136	Is +C COMPARE ERROR (A1K2M13) always plus?	Change A1L2.
137	Is +SET P COMP (A1K2M03) always minus?	Change A1K2.
138	Is +BUFFER CRC P COMP TP (A1D2J05) always plus?	Change A1D2.
139	Is −BUFFER ERROR TP (A1C2S05) always minus?	Change A1C2.
140	Is +P COMP CHK (A1F2M11) always plus?	Change A1F2.
141	If not:	Change in order: 1. A1G2 2. A1K2 3. A1D2 4. A1C2 5. A1F2 6. A2T2

COMPARE OR C COMPARE ERRORS

Test Points For P Compare Errors

BITS	BUS OUT BIT x		BUS OUT x CHANNEL B		CHANNEL BUFFER OUT x
	with EC733814	without EC733814	with EC733814	without EC733814	
P	B2M2M04	B2L2M04	B2M2J11	B2L2J11	A1F2U02
0	B2M2B05	B2L2B05	B2M2J04	B2L2J04	A1F2P13
1	B2M2D06	B2L2D06	B2M2J03	B2L2J03	A1F2M13
2	B2M2B07	B2L2B07	B2M2P05	B2L2P05	A1F2U03
3	B2M2B09	B2L2B09	B2M2G13	B2L2G13	A1F2D09
4	B2M2G10	B2L2G10	B2M2J12	B2L2J12	A1F2D07
5	B2M2J02	B2L2J02	B2M2M03	B2L2M03	A1F2B07
6	B2M2G04	B2L2G04	B2M2J06	B2L2J06	A1F2B10
7	B2M2G05	B2L2G05	B2M2G08	B2L2G08	A1F2D12

Test Points For –RD Data TRK x

TRK X LOCATION	
P	Y1D2J04
0	Y1D2G02
1	Y1D2B11
2	Y1D2M02
3	Y1D2G13
4	Y1D2J13
5	Y1D2J11
6	Y1D2G07
7	Y1D2G09

Mode Chart Sense Byte 6

MODE BITS	0	2	3	4
7-Track	X			
1600 (Mod 4, 6, 8)		X		X
6250		*	X	X
1600 (Mod 3, 5, 7)		*		
9-Track NRZI		X	X	

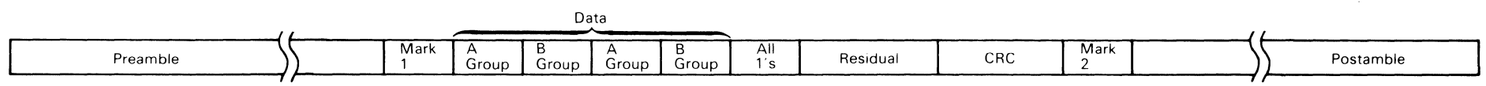
* Can be on or off. On for Dual Density, off for single density.

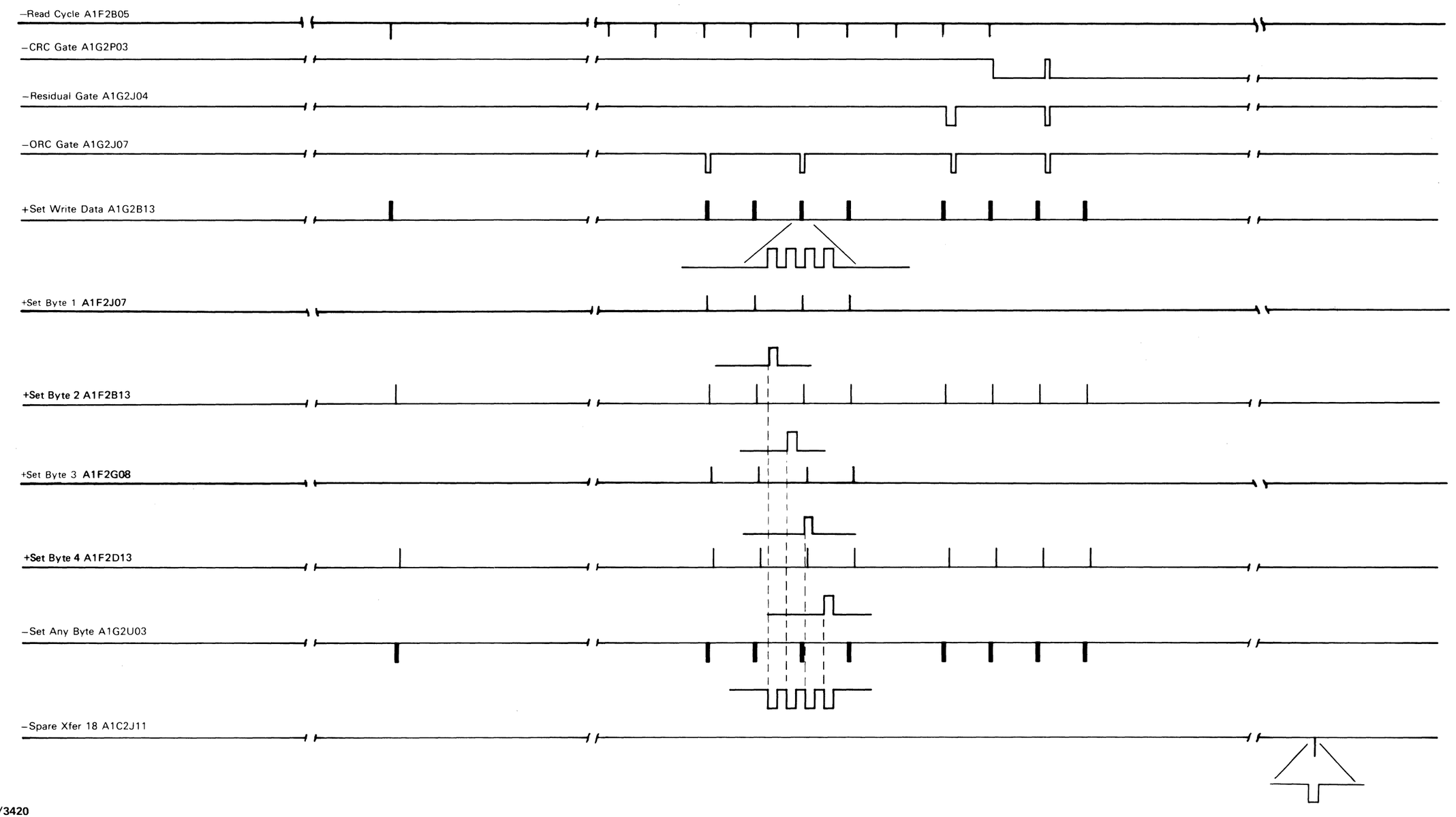
6250 BPI TIMING CHART

If a 6250 or 1600 bpi mode failure occurs when moving tape these timing charts can be used. Keep in mind there are delays from TAPE OP until data is on the TUBOs, and that these delays vary with the tape unit model being used.

6250 TIMING CHART

If a 6250 or 1600 bpi mode failure occurs when moving tape, these timing charts can be used. Keep in mind there are delays from TAPE OP until data is on the TUBOs, and that these delays vary with the tape model being used.





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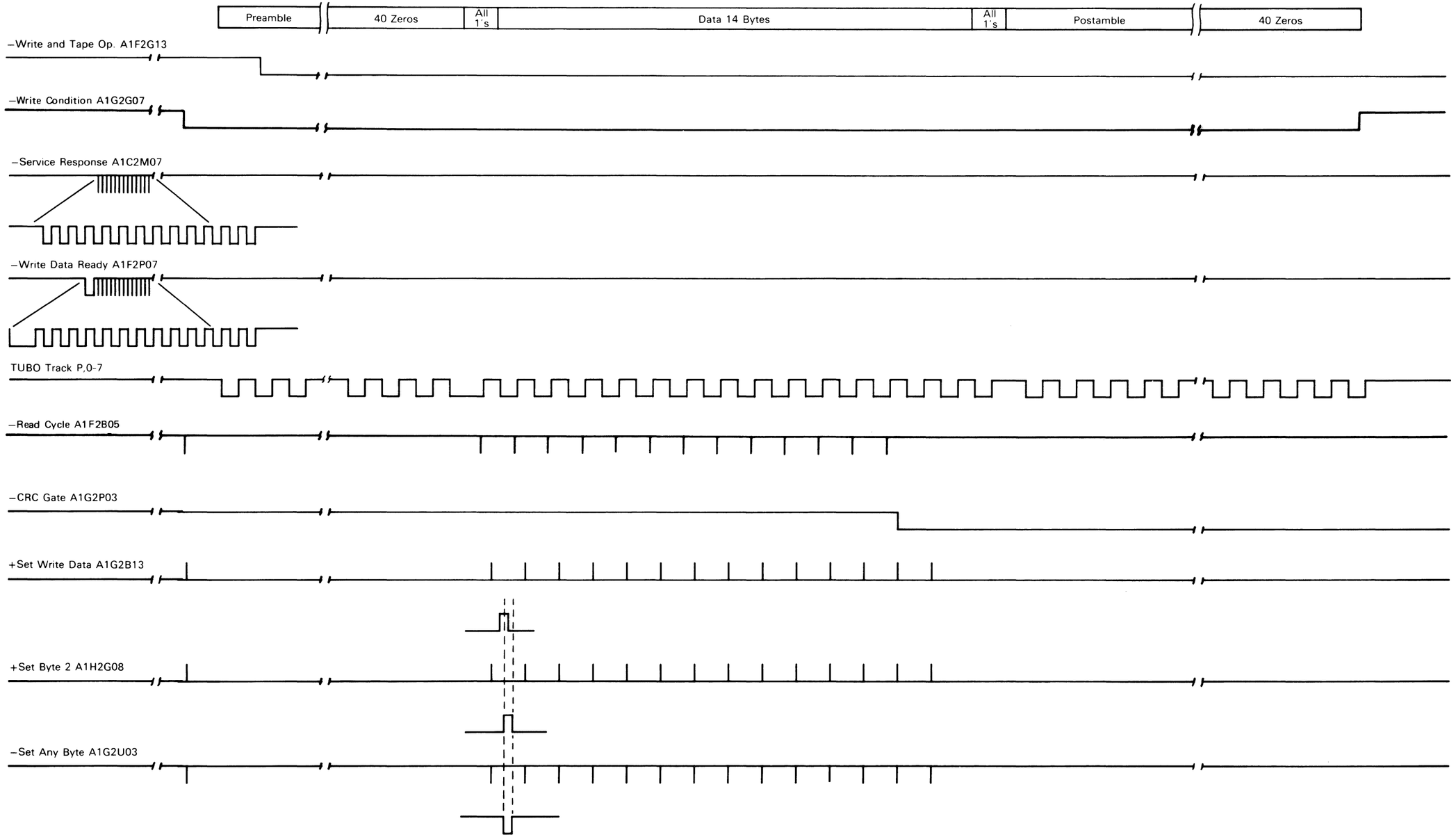
PE TIMING CHART

If a 6250 or 1600 bpi mode failure occurs when moving tape, these charts can be used. Keep in mind there are delays from TAPE OP until data is on the TUBOs, and that these delays vary with the tape unit model being used.



P OR C COMPARE

Sense byte 3, bit 7 is set by P Check Buffer, Write Data Parity Error, Buffer Error, CRC Set P Compare Error, or C Compare Error.

A. P Check Channel Buffer is set when parity of the byte sent to channel is even.

B. Write Data Parity Error is set when there is not compare between Channel Buffer Out P and Write Bit P, which is encoded and written on tape.

C. Buffer Error is set by a buffer overrun, a write address error, or if the service response count does not equal Channel Read-Out Counter (CROC), after all data has been read out of the channel buffer.

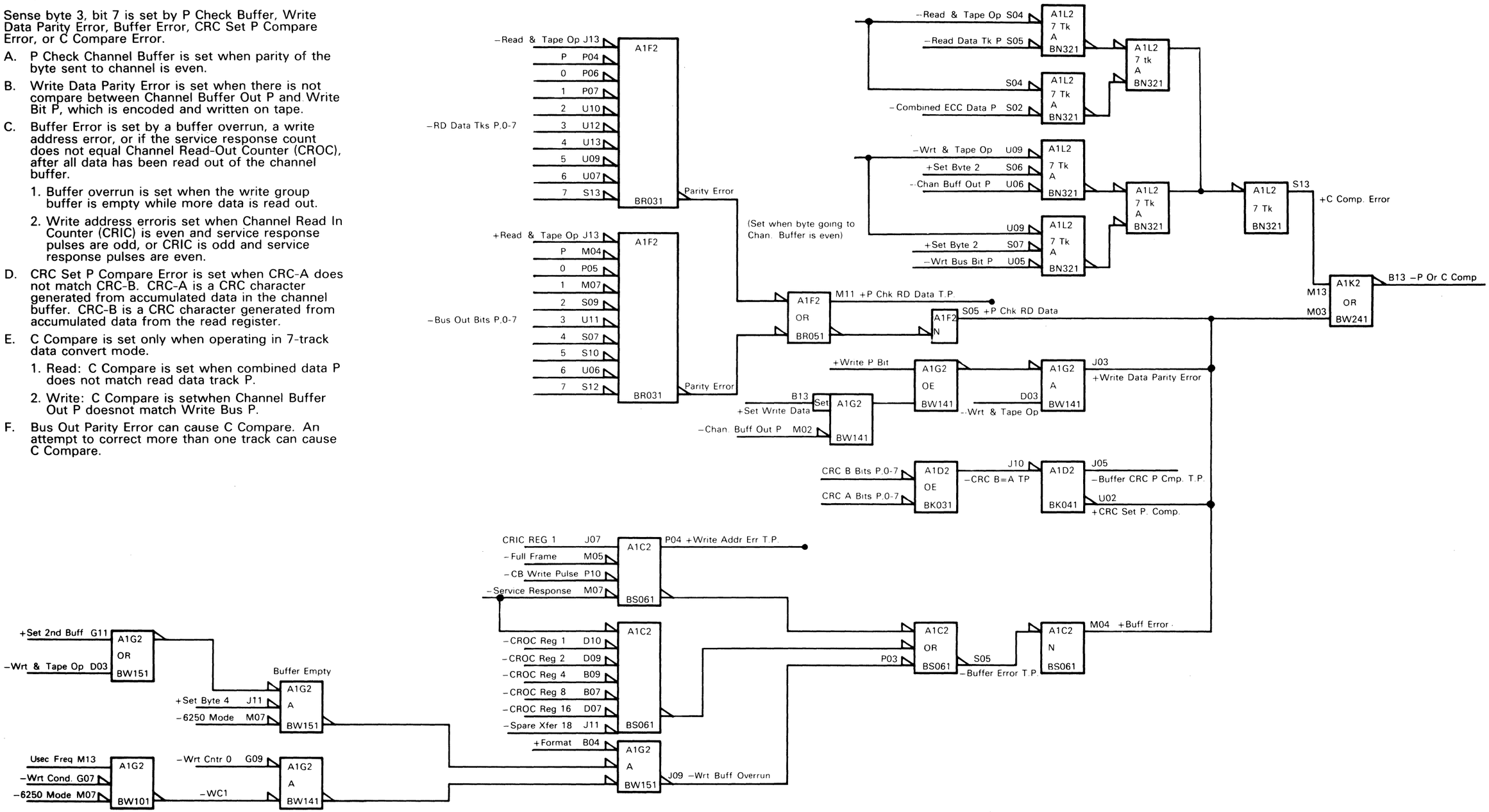
   1. Buffer overrun is set when the write group buffer is empty while more data is read out.
   2. Write address erroris set when Channel Read In Counter (CRIC) is even and service response pulses are odd, or CRIC is odd and service response pulses are even.

D. CRC Set P Compare Error is set when CRC-A does not match CRC-B. CRC-A is a CRC character generated from accumulated data in the channel buffer. CRC-B is a CRC character generated from accumulated data from the read register.

E. C Compare is set only when operating in 7-track data convert mode.

   1. Read: C Compare is set when combined data P does not match read data track P.
   2. Write: C Compare is setwhen Channel Buffer Out P doesnot match Write Bus P.

F. Bus Out Parity Error can cause C Compare. An attempt to correct more than one track can cause C Compare.



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XF2100 Seq 2 of 2	**2735917** Part Number	**See EC History**	**845958** 1 Sep 79					

WRITE TRIGGER VERTICAL REDUNDANCY CHECK (VRC) ERROR

From 14-000

ERROR DESCRIPTION:

Sense Byte 4, Bit 3 is set when data sent to the tape unit has incorrect parity.

A. In 6250 bpi mode - Parity is checked on the total number of one bits in a 6250 bpi encoded group. Even parity is used for a data group and A2 format group or any combinations using the A2 format group, odd parity for all other groups.

B. In PE mode - Parity is **even** at Write clock 3 (WC3) and **odd** at Write clock 11 (WC11).

C. In 9-track NRZI mode - Parity is even before the first byte is written. After the first byte, parity then alternates between odd and even.

D. In 7-track NRZI mode - if even parity is written, parity remains even. If odd parity is written, parity alternates between odd and even after the first byte is written.

Most Probable Causes:

The following list of cards can cause the problems covered The cards are listed with the highest probability first. Lines with multiple cards have the same probability. Cards separated by slashes are interchangeable.

A. A1G2
B. A1T2
C. Y1J2
D. A1H2
E. Y1H2, Y1K2/Y1L2/Y1M2
F. A1K2, A1L2, Y1C2, Y1G2, Y1N2, Y1P2

ADDITIONAL CARDS AFFECTED:

A. Y1S2
B. A1E2
C. A2Q2
D. A1F2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise.
Remember to END all problems or maintenance calls by going to MAP 00-030.
Refer to 17-022 through 17-025 for timing charts and to 17-021 for test points.

Seq	Condition/Instruction	Action
1	From the CE panel, use a LWR 8B command with gaps (jumper A1S2G08 to ground), or Write 01 command to write all ones in the failing mode. For 6250 bpi, move tape away from load point. Use byte count of 0B0 hex.	
2	Sync the scope negative on –WRT CONDITION (A1G2G07).	
3	Is sync pulse bad? (See 17-022.)	Go to ALD BW151 GF6 and follow line back to failing point.
4	Is tape unit operating in 7- or 9-track NRZI mode?	Go to Seq 45.
5	Scope all the +TUBOs (see test point charts on 17-021 and timing charts on 17-025). Check all of the record. Is one or more TUBO bad? (See 17-021.)	Go to Seq 8.
6	Is +WRITE TRIGGER VRC ODD (A1G2D10) correct? See timing chart on 17-022.	Go to Seq 90.
7	If not:	Change A1H2. Suspect a bad parity generator.
8	Are +TUBOs for all tracks bad? (See 17-022.)	Go to Seq 17.
9	If not:	Change A1H2. If in 7-track mode, change A1E2.
10	Does –WRITE TRIGGER VRC ERROR (A1G2P13) occur while +FORMAT (A1H2J11) is plus?	Change card A1H2. The serializer or one of the write triggers is bad.
11	Is only track P bad?	Go to Seq 26.
12	Are all Write Buses good? See timing chart on 17-022.	Change A1H2. The write buffer or encoder is bad.
13	Is –RESIDUAL GATE (A1G2J04) bad? See timing chart on 17-023.	Go to ALD BW121 and follow line back to failing point.
14	Is –CRC GATE (A1G2P03) bad? See timing chart on 17-023	Go to ALD BW121 and follow the line back to failing point.
15	Is –ORC GATE (A1G2J07) bad? See timing chart on 17-023	Go to ALD BW121 and follow the line back to failing point.
16	If not:	Recheck analysis. Any error before this point in the machine should have been found in P Compare Map on 17-010. Go to 17-010.
17	Is +WRITE TIME GATE (A1H2B12) bad?	Go to Seq 28.
18	Is –WRITE TRIGGER GATE (A1H2G02) bad?	Go to Seq 53.
19	Are all tracks dead at TUBOs?	Change A1H2. The serializer or a write trigger is bad.
20	Is tape unit operating in 7-track Mode?	Go to Seq 62.
21	Are the TUBOs good through the preamble? See the timing charts on 17-022 through 17-025.	Go to Seq 32.
22	Is the +FORMAT line (A1H2J11, 17-023) either a solid minus or pulsing at the beginning of the record?	Go to Seq 84.
23	Are both –WRITE CNTR 0 (A1G2G09) and –WRITE CNTR 4 (A1G2G08) See timing chart on 17-024.	Go to Seq 41.
24	Are both –WC9 (A1H2U10) and –WC11 (A1H2U09) good?	Change A1H2.
25	If not:	Change A1H2.
26	Is either –NRZI (A1G2P06) or –STAT BIT 3 7 TRACK (A1G2P07) minus?	Go to ALD BW141 and follow active line back to failing point.
27	If not:	Change A1G2. The parity generator is bad.
28	Are you running in 6250 bpi mode?	Go to Seq 69.
29	Is –WC0 (A1G2M05), –WC9 (A1H2U10), or –WC11 (A1H2U09) bad?	Change A1G2.
30	Is –6250 MODE (A1G2M07) minus?	Go to ALD BW141 and follow line back to failing point.
31	If not:	Change A1G2.
32	Is +FORMAT (A1H2J11) bad?	Go to 86.
33	Does the error occur while +FORMAT is plus?	Go to Seq 23.
34	Are +SET BYTE 1 (A1H2M07), 2 (A1H2G08), 3 (A1H2G03), or 4 (A1H2D02) bad? See 17-023.	Go to Seq 72.
35	Is +SET SECOND BUFFER (A1H2G10) bad? See 17-023.	Go to ALD BW091 and follow line back to failing point.
36	Is –STAT BIT 3 DIAGNOSTIC MODE A (A1H2D10) minus?	Go to ALD BW091 and follow line back to failing point.
37	Are +A1 (A1H2B13), +A2 (A1H2S02), +MARK1 (A1H2D13), and +MARK2 (A1H2U03) good? See timing chart on 17-024.	Go to Seq 10.
38	Are –XOUTA BITs 0, 4, 5, 6, or 7 minus while –WC0 (A1G2M05) and –CNTR 0 (A1G2G09) a	This appears to be a microprocessor problem. Change A2Q2.
39	Are +MARK1 (A1H2D13) and +MARK2 (A1H2U03) the only active format conditions?	Go to ALD BW151 and follow lines back to failing point.
40	If not:	Change A1G2. (Format control is bad.)
41	Are +A1 (A1H2B13), +A2 (A1H2S02), +MARK1 (A1G2M12), and +MARK2 (A1H2U03) good? See timing chart on 17-024.	Change A1H2. (The serializer is bad.)
42	Is –WRITE GROUP B BRANCH (A1G2J06) bad? See timing chart on 17-024.	Change A1G2.
43	Scope –XOUTA BITS for the desired format character. Bits are gated by adding –WC0 (A1G2M05) with –WRITE CNTR 0 (A1G2G09). Is bit line good (pulsing, not solid level)? See 17-021.	Change A1G2.
44	If not:	Go to ALD BW151 EA6 and follow line back to failing point.
45	Does the failure occur in 7-track mode?	Go to Seq 57.
46	Is +FORMAT (A1G2B04) plus?	Go to ALD BW151 EA6 and follow line back to failing point.
47	Is +Write Trigger VRC ODD (A1G2D10) a constant minus or plus?	Change A1H2.
48	Is –STAT BIT 3 7-TRK (A1G2P07) minus?	Go to ALD AA144 EG6 and follow line back to failing point.
49	Is –NRZI MODE (A1G2P06) plus?	Go to ALD BW231 GK6 and follow line back to failing point.
50	Is –6250 mode (A1G2M07) minus?	Go to ALD BW231 CH6 and follow line back to failing point.

WRITE TRIGGER VERTICAL REDUNDANCY CHECK (VRC) ERROR(Cont'd)

Seq	Condition/Instruction	Action
51	Is +PARITY EVEN (A1G2M04) plus?	Go to ALD BN311 DM2 and follow line back to failing point.
52	If not:	Change in order: 1. A1G2 2. A1K2
53	Is –WC0 (A1G2M05), –C9 (A1H2U10), or –WC11 (A1H2U09) line bad? See 17-024.	If the microfrequency (A1K2M13) is good, change the A1G2 card. If not, change A1K2.
54	Is failing mode 7-Track NRZI?	Change A1G2.
55	Is –NRZI MODE (A1K2D10) minus?	Go to ALD BW231 and follow line back to failing point.
56	If not:	Change A1G2.
57	Is –NRZI (A1G2P06) plus?	Go to ALD BW231 and follow back to failing point.
58	Is tape unit operating in even parity?	Go to Seq 60.
59	If not:	Go to Seq 5.
60	Are one or more +TUBO lines bad? See 17-022.	Go to Seq 8.
61	Is +WRITE TRIGGER VRC ODD (A1H2M09) always minus?	Change A1G2.
62	Are any of the following lines plus? +A1(A1H2B13) +A2 (A1H2S02) +MARK1 (A1H2D13) +MARK2 (A1H2U03)	Change A1G2.
63	Is –XOUTA BIT 4 ALU2 (A1H2S12) minus?	Go to ALD AA141CC2 and follow back to failing point.
64	Is +FORMAT (A1H2J11) plus at time of VRC ERROR (A1G2P13)?	Go to ALD BW151 EA6 and follow line back to failing point.
65	Is +SET 2ND BUFFER (A1H2G10) bad?	Go to ALD BW251 EH2 and follow line back to failing point.
66	Is +SET BYTE 2 (A1H2G08) good?	Change A1H2.
67	Is –6250 MODE (A1F2G09) minus?	Go to ALD BW231 GH6 and follow line back to failing point.
68	If not:	Change A1F2.
69	Is –6250 MODE (A1G2M07) minus?	Change A1G2.
70	Are –XOUTA BIT 4 ALU2 (A1K2D09) and –STAT BIT 0 TAPE OP (A1K2U06) ever minus at the same time?	Change A1K2.
71	If not:	Go to ALD AA141 and follow line back to failing point.
72	Is tape unit operating in 6250?	Go to Seq 76.
73	Is –6250 MODE (A1F2G09) minus?	Go to Seq 79.
74	Is +SET WRITE DATA (A1F2P03) good? See timing chart on 17-023.	Change A1F2.
75	If Not:	Go to ALD BR041 GM2 and follow line back to failing point.
76	Is –6250 MODE (A1F2G09) plus?	Go to Seq 81.
77	Is +SET WRITE DATA (A1F2P03) good? See timing chart on 17-023.	Change A1F2.
78	If not:	Go to ALD BR041 GM2 and follow line back to failing point.
79	Is –XOUTA BIT 4 ALU2 TO DF (A1K2D09) minus?	Change A2Q2.
80	If not:	Change A1K2.
81	Is –XOUTA BIT 4 ALU2 TO DF (A1K2D09) minus?	Change A2Q2.
82	Is –STAT BIT 0 TAPE OP TO DF (A1K2U06) plus?	Change A2Q2.
83	If not:	Change A1K2.
84	Are –XOUTA BIT 0 ALU1 to DF (A1G2S05) on 17-025 and –WRITE CNTR 0 (A1G2G09) good? (See timing chart on 17-024.)	Change A1G2.
85	If not:	Change A2Q2.
86	Is +FORMAT (A1H2J11) bad during the preamble? See timing chart on 17-023.	Go to Seq 41.
87	Is +END ONES LATCH (A1G2U02) good at end of data? See timing chart on 17-022.	Change A1G2.
89	If not:	Go to ALD BW151 and follow line back to failing point.
90	Is –WC0 (A1G2M05) or –WC11 (A1G2D09) bad (not pulsing)?	Change A1G2.
91	Is –WRITE COUNTER 4 (A1G2G08) bad? See timing chart on 17-024.	Change A1H2.
92	Suspect a defective error circuit.	Change A1G2.

Test Point Charts

Track No.	Channel Buffer or DC (A1G2 card)	Write Bus (A1H2 card)	TUBO (A1H2 card)
P		G11	U07
0	U10	D04	M10
1	S13	B04	S10
2	D12	M13	U05
3	G02	J04	P09
4	D07	B07	J03
5	B10	D07	J07
6	U11	D09	M04
7	M11	P07	J13

Set Byte	(A1H2 card)
1	M07
2	G08
3	G03
4	D02

Format Character	–XOUTA BITS	A1G2 Card
A1	7	U07
A2	6	U06
MARK1	5	S07
MARK2	4	S04

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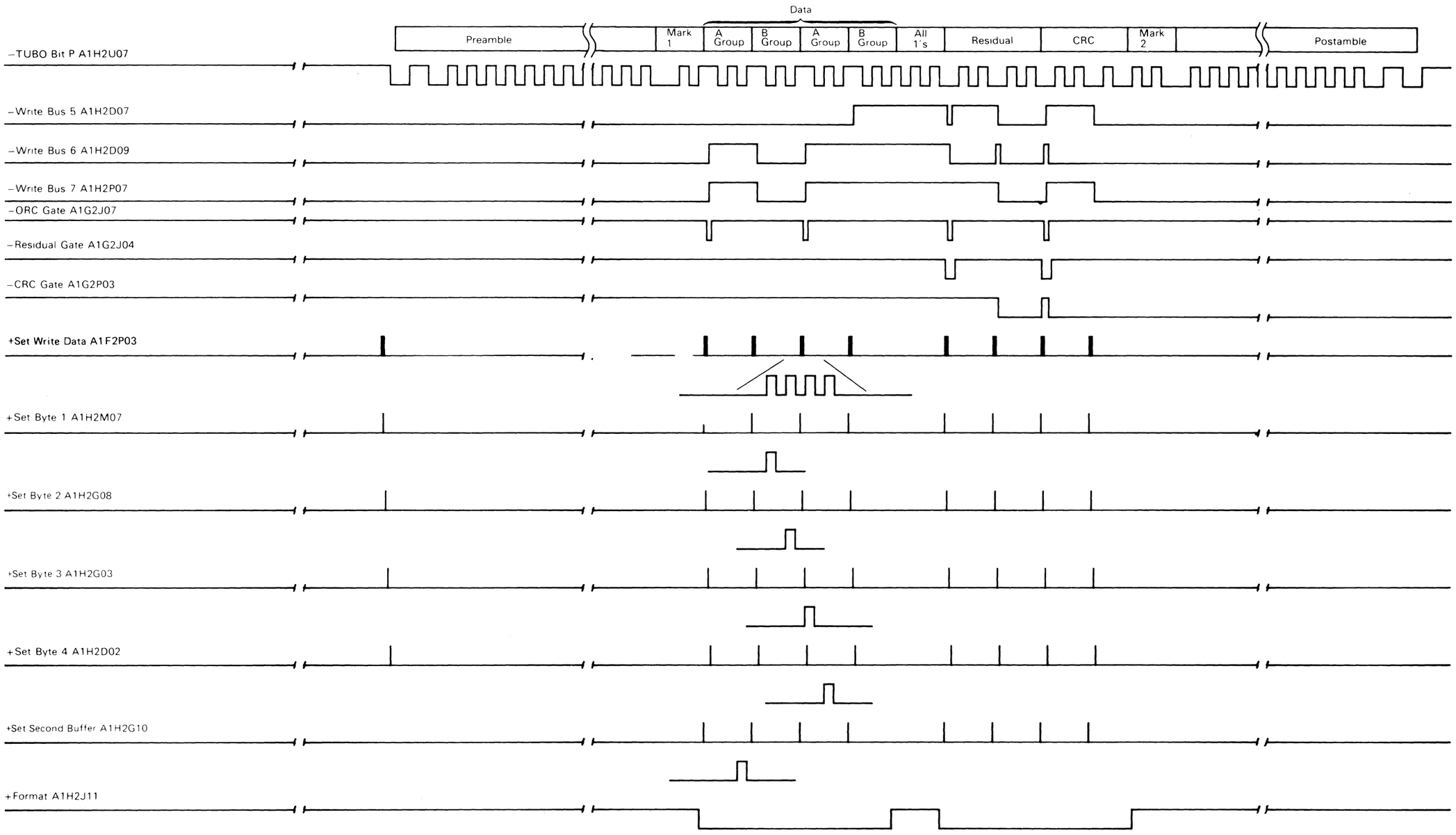

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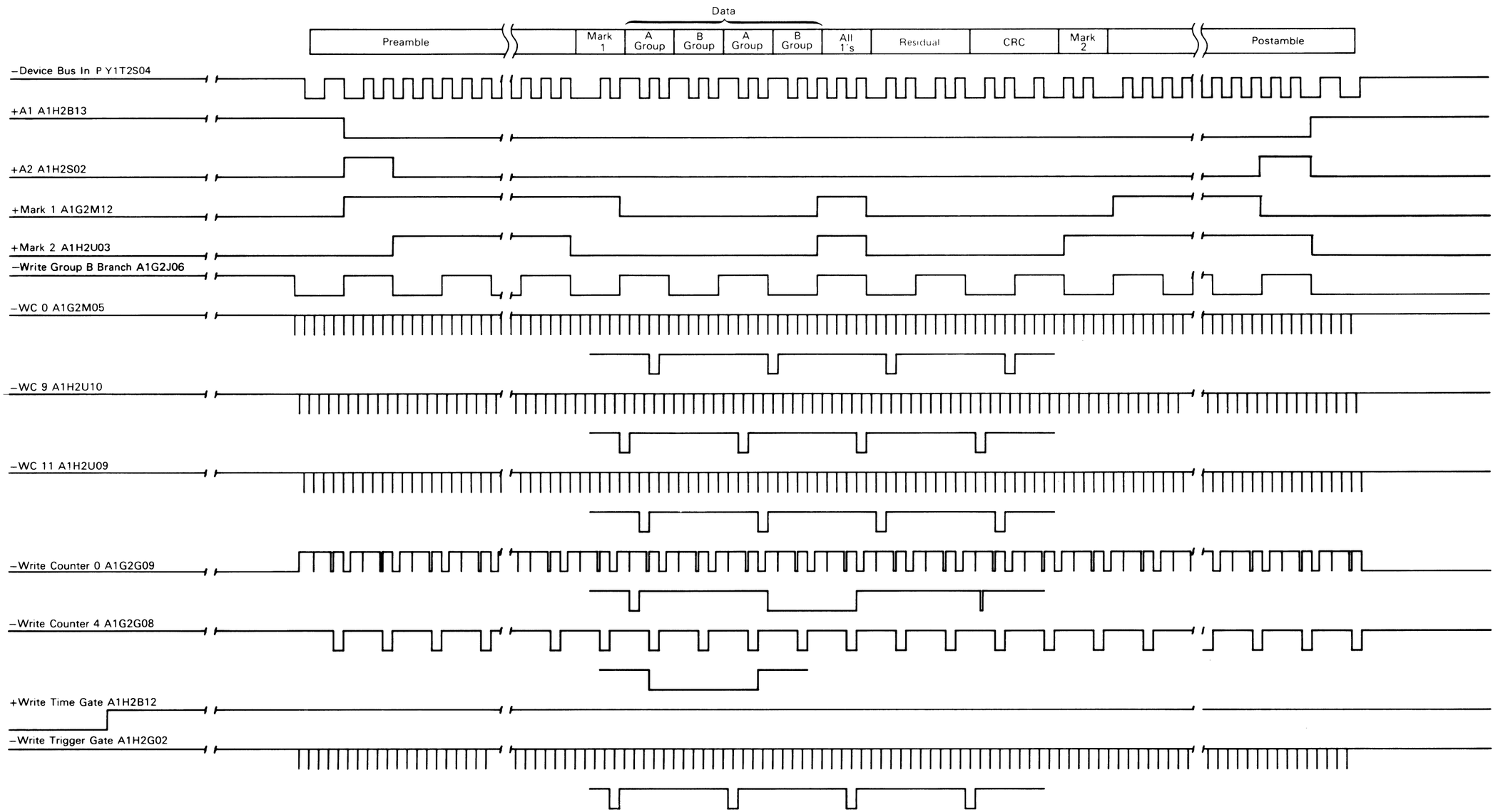
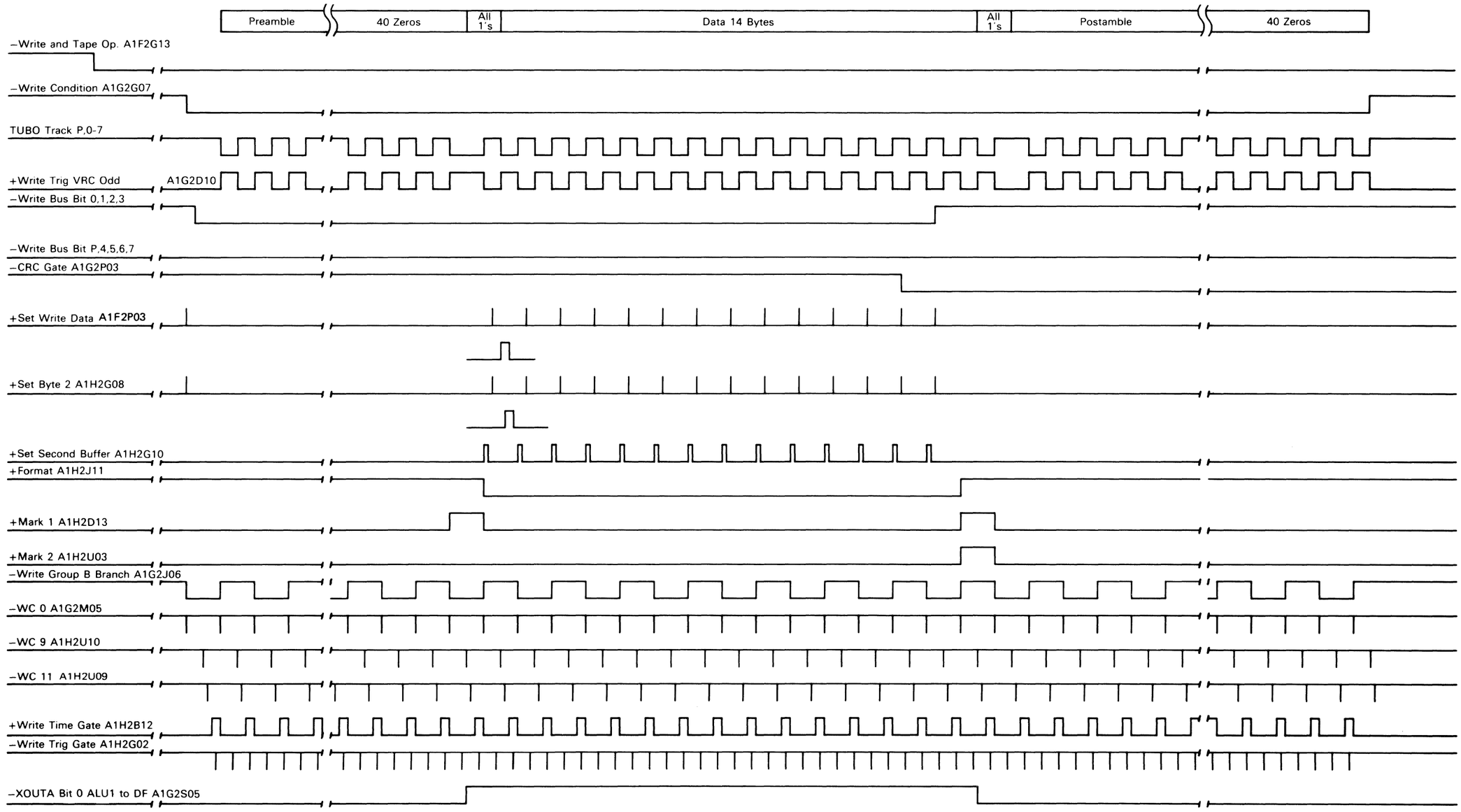
XF2300 Seq 2 of 2	2735919 Part Number	See EC History	845958 1 Sep 79					



PE TIMING CHART



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XF2400 Seq 2 of 2	2735920 Part Number	See EC History	845958 1 Sep 79					

WRITE TRIGGER VRC

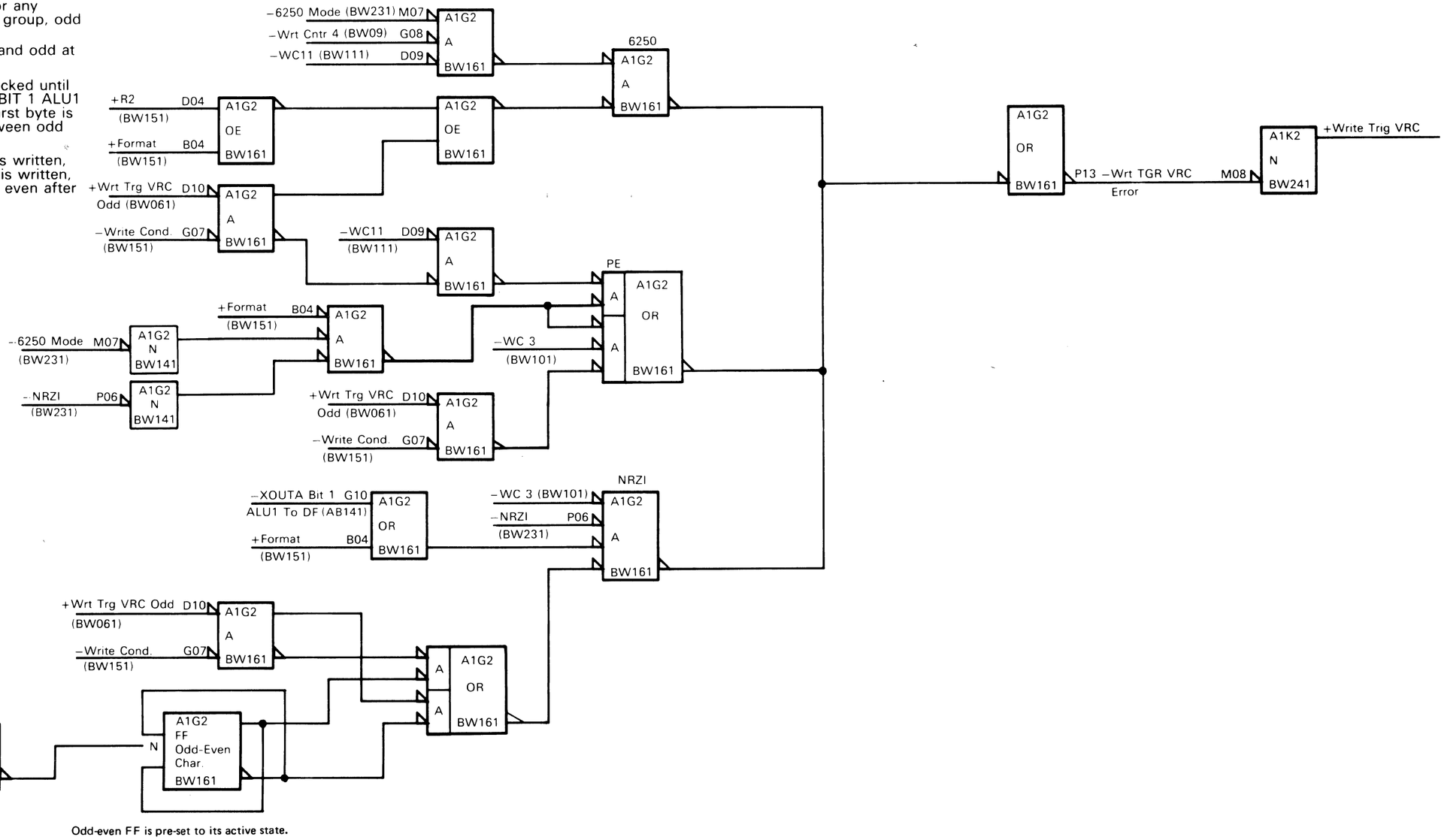
Sense byte 4, bit 3 is set:

A. 6250 Write - parity is checked on the total number of one bits in a 6250 encoded group (five 9-bit bytes). Even parity is used for a data group and A2 fromat group or any combinations using the A2 format group, odd parity is used all other groups.

B. PE Mode - parity is even at WC3 and odd at WC11.

C. Nine-track NRZI - parity is not checked until the first byte is written (–XOUTA BIT 1 ALU1 to DF; 'ALLOW EOD'). After the first byte is written, parity then alternates between odd and even.

D. Seven-track NRZI - if even parity is written, parity remains even. If odd parity is written, parity alternates between odd and even after the first byte is written.



Odd-even FF is pre-set to its active state.

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XF2500 Seq 1 of 2	2735921 Part Number	See EC History	845958 1 Sep 79					

ID BURST CHECK

From 14-000

ERROR DESCRIPTION:

Sense Byte 5, Bit 3 is set if the 6250 bpi or PE Identification Burst is not written correctly from load point. The SAGC Check (Sense Byte 8, Bit 4) is OFF at this time. The identification burst consists of 3200 flux changes per inch recorded in the 1-track for 6250 bpi and 1600 flux changes per inch in track P for PE while all other tracks are erased

Sense Byte 8, Bit 4 is set if the SAGC (self-adjusting gain control) cannot compensate for variations which cause read signal output in any track to remain below threshhold. The SAGC Burst consists of six inches of consecutive ones in all nine tracks. There is a .3-inch (7.6 mm) IBG (interblock gap) between the SAGC Burst and the first data block. An identification character with consecutive ones in tracks 1, 2, 3, 4, 6 and 7 is added to the end of the burst to allow the tape unit to recognize the SAGC Burst when reading backwards.

During a 6250 bpi Write-from-Load-Point operation, the tape unit attempts to a writing the SAGC Burst.

The following beginning of record (BOR) and INTERRUPT conditions create sense bits for error recovery.

1. If BOR and INTERRUPT are OFF, Sense Byte 0, Bit 3 (Equipment Check) and Sense Byte 8, Bit 4 (SAGC Check) are set.
2. If BOR is OFF and INTERRUPT is ON, Sense Byte 5, Bit 3 (ID Burst Check) and Sense Byte 8, bit 4 (SAGC Check) are set.
3. If BOR and INTERRUPT are ON, Sense Byte 5, Bit 3 (ID Burst Check) and Sense Byte 8, Bit 4 (SAGC Check) are set.
4. If BOR is ON and INTERRUPT is OFF, no sense bits are set (normal condition).

   Sense Byte 5, Bit 3 (ID Burst Check) and Sense Byte 8, Bit 4 (SAGC Check) are also set if the inverse tape mark (TM) is bad for consecutive .250-inch (6.3 mm) segments over an approximate two-inch(50.8 mm) distance.

A Beginning of Record (BOR) is defined as data detected in all tracks of one zone and data detected in at least one track in each of the other two zones. INTERRUPT is a tape unit Interrupt caused by one or more read head amplifiers having reached the gain limit for a Write or Read operation without DATA DETECTED and/or READY becoming inactive while MOVE was active.

Most Probable Causes:

The following list of FRUs can cause the problems covered in this procedure. The cards are listed with the highest probability first. Lines with multiple cards have the same probability.

Control Unit	Single Tape Unit
A. A1K2	A. Autocleaner (Models 4, 6, 8)
B. A2Q2	B. Rewind plunger (Models 3, 5, 7)
C. Y1Q2	C. T-A1J2
D. A1L2	D. T-A1L2
E. Y1R2	
F. A1C2, A1H2, A2R2, Y1P2	

ADDITIONAL CARDS AFFECTED:

Control Unit	Single Tape Unit
A. Y1D2	A. T-A1G2
B. A2T2	
C. A1S2	
D. A2E2	
E. A2D2	
F. Y1T2	

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise.
Remember to END all problems or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Bad tape at load point may cause this error. Be sure tape has not been damaged.	
2	Does the error occur on only one tape unit? This error may be model sensitive.	Go to 5A-000 for Models 3, 5, and 7. Go to 5B-000 for Models 4, 6, and 8.
3	Are you trying to write or do an ERG (17) in 6250 bpi mode? If no Mode Set command is issued, a Model 4, 6, or 8 tape unit is in 6250 bpi mode when writing from BOT.	Go to Seq 32.
4	Switch tape control offline and enter the following command sequence at the tape control CE panel: Rewind 07 Mode Set C3 Write 01 Test I/O 00	
5	Sync negative on –STAT BIT 2 WRT ID BURST (A1H2S13).	
6	Is the sync line at a solid level?	Change A2O2.
7	Does the sync pulse, but at a bad level?	Change A1H2.
8	Does –TUBO BIT P (A1H2U07) pulse at the following rate? Model 3 or 4 –8.3 usec Model 5 or 6 –5 usec Model 7 or 8 –3.12 usec	Go to Seq 61.
9	Is +0 PCT AMPL CTRL TRK P (A1H2S09) plus?	Go to Seq 19.
10	Is +PE MODE (A1H2D05) minus?	Go to Seq 24.
11	Is +PE P BURST (A1H2G05) pulsing at the rate given in Seq 8?	Go to Seq 27.
12	Is –XOUTA BIT 4 ALU2 to DF (A1K2D09) minus when the sync is minus?	Change A2O2.
13	Is +556 or 200 bpi 7 TRK (A1K2J10) plus? **NOTE**: This line should float below V-reference level (–1.32V) on tape controls without the 7-track NRZI feature.	Go to ALD BN311 EN6 and follow line back to failing point. Probable cause is A1L2 then A2O2.
14	Check –XOUTA BIT 5 ALU2 to DF (A1K2B07) and –XOUTA BIT 7 ALU2 to DF (A1K2D11) for proper speed decode during sync time as follows: **TU Model** / **(Speed)** / **XOUTA Bit 5** / **XOUTA Bit 7** 3, 4 / OFF / ON 5, 6 / ON / OFF 7, 8 / ON / ON Is either line wrong?	Change A2O2.
15	Is failing tape unit a Model 7 or 8?	Go to Seq 17.
16	If not:	Change A1K2.
17	Scope –5.12 mHz (A1K2G02). Is it pulsing?	Change A1K2.
18	If not:	Change A1C2.
19	Is –GATE TIE (Y1Q2B13) minus?	Go to Seq 30.
20	Is –6400 POINTER MODE (Y1Q2D10) minus?	Go to Seq 22.
21	If not:	Change in order: 1. Y1Q2 2. Y1D2 (NRZI)
22	Is +WRITE AND TAPE OP (Y1P2P06) plus?	Change Y1P2.
23	Go to ALD BW231 GF2 and follow line back to failing point.	
24	Is –PE MODE (A1K2G13) minus?	Change A1K2.
25	Are –XOUTA BIT 0 ALU2 to DF (A1K2S13) and –STAT BIT 0 TAPE OP TO DF (A1K2U06) both minus when the sync is minus?	Change A1K2.
26	If not:	Change A2Q2.
27	Is –WRITE CONDITION (A1H2B02) plus?	Change A1H2.
28	Is –STAT BIT 1 START WR RD (A1G2G05) minus?	Change A2Q2.
29	If not:	Change A1G2.
30	Is –STAT BIT 1 SENSE (A1S2U09) minus?	Change A2T2.
31	If not:	Change A1S2.
32	Go offline and do the following command sequence: Rewind 07 Write 01 Rewind 07 Write 01	
33	Sync minus on –STAT BIT 2 WRT ID BURST (A1H2S13).	
34	Is the sync line at a solid level?	Change A2Q2.
35	Does sync puise, but at a bad level?	Change A1H2.
36	Does –TUBO BIT 1 (A1H2S10) pulse at the following rate: Model 4 –4.42 usec Model 6 –2.65 usec Model 8 –1.66 usec	Go to Seq 43.

ID BURST CHECK (Cont'd)

Seq	Condition/Instruction	Action
37	Is +0 PCT AMPL CTRL TK1 (A1H2U11) plus?	Go to Seq 19.
38	Is −XOUTA BIT 4 ALU2 to DF (A1K2D09) plus when the sync if minus?	Change A2Q2.
39	Is −WRITE OSCILLATOR (A1H2U12) pulsing at the rate given in Seq 36?	Go to Seq 27.
40	Is +556 or 200 bpi 7 TRK (A1K2J10) plus? **NOTE:** This line should float below the inactive V-reference level (−1.32V) on tape controls without the 7-track NRZI feature.	Go to ALD BN311 EN6 and follow line back to failing point. Probable cause is A1L2, then A2Q2.
41	Check −XOUTA BIT 5 ALU2 to DF (A1K2B07) and −XOUTA BIT 7 ALU2 to DF (A1K2D11) for proper speed decode during sync time as follows: **TU Model (Speed)** / **XOUTA Bit 5** / **XOUTA Bit 7** 4 / OFF / ON 6 / ON / OFF 8 / ON / ON Is either line wrong?	Change A2Q2
42	If not:	Change A1K2.
43	Does the tape control have "Selection logic" (1x8) feature?	Go to Seq 45.
44	Is the primary interface being used?	Go to Seq 56.
45	Is −BUS OUT 1 SECONDARY (A2E2B03) pulsing at the rate given in Seq 36? **CAUTION:** Interface level (+5V to ground)	Go to Seq 47.
46	If not:	Change A2E2.
47	Sync negative on −STAT BIT 2 WRT ID BURST (A1H2S13). Does +1 TRACK ENV BRANCH (A1K2P13) become plus during the sync?	Change A2D2.
48	Does −DEVICE BUS IN 1 SECONDARY (A2D2D10) pulse at the rate given in Seq 36? **CAUTION:** Interface level (+5V to gnd)	Go to Seq 50.
49	Failure appears to be cabling or device switch problem.	Go to 18-010.
50	Is +NRZI (Y1Q2U13) plus?	Go to Seq 79.
51	Does −DEVICE BUS IN 1 to DF (Y1R2M04) pulse at the rate given in Seq 36?	Go to Seq 53.
52	If not:	Change A2D2.
53	Does −TIME SENSE 1 (Y1R2M03) become minus while the sync is minus?	Go to Seq 81.
54	Are +WRITE AND TAPE OP (Y1Q2B12) and +PE MODE (Y1Q2D02) both minus at sync time?	Go to ALD BW231 GF2 or ALD BW231 GJ2 and follow failing line back to point of failure
55	If not:	Change Y1R2. **Note:** You can interchange Y1R2 with either Y1S2 or Y1T2. If problem is not fixed, change Y1Q2.
56	Is −BUS OUT 1 PRIMARY (A2E2D03) pulsing at the rate given in Seq 36? **CAUTION:** Interface level (+5V to gnd)	Go to Seq 58.
57	If not:	Change A2E2.
58	Sync negative on −STAT BIT 2 WRT ID BURST (A1H2S13). Does +1 TRACK ENV BRANCH (A1K2P13) become plus during the sync?	Change A2D2.
59	Does −DEVICE BUS IN 1 PRIMARY (A2D2J09) pulse at the rate given in Seq 36? **CAUTION:** Interface level +5V to gnd)	Go to Seq 50.
60	Failure appears to be cabling or device switch problem.	Go to 18-010.
61	Does the tape control have selection logic (1x8) feature?	Go to Seq 63.
62	Are you using the primary interface?	Go to Seq 74.
63	Is −BUS OUT P SECONDARY (A2E2G07) pulsing at the rate given in Seq 8? **CAUTION:** Interface level (+5V to gnd)	Go to Seq 65.
64	If not:	Change A2E2.
65	Sync negative on −STAT BIT 2 WRT ID BURST (A1H2S13). Does +P TRACK ENV BRANCH (A1K2U02) become plus during the sync?	Change A2D2.
66	Does −DEVICE BUS IN P SECONDARY (A2D2M03) pulse at the rate given in Seq 8? **CAUTION:** Interface level (+5V to gnd)	Go to Seq 68.
67	Failure appears to be a cabling or device switch problem. Go to 18-010.	
68	Is +NRZI (Y1Q2U13) plus?	Go to Seq 79.
69	Does −DEVICE BUS IN P to DF (Y1T2S04) pulse at the rate given in Seq 8?	Go to Seq 71.
70	If not:	Change A2D2.
71	Does −TIME SENSE (Y1T2U05) become minus while the sync is minus?	Go to Seq 81.
72	Is +PE WRITE AND TAPE OP (Y1Q2B12) minus at sync time?	Go to ALD CB471 FD2 and follow failing line back to point of failure.
73	If not:	Change Y1T2. **Note:** You can interchange Y1T2 with either Y1R2 or Y1S2. If problem is not fixed, change Y1Q2.
74	Is −BUS OUT P PRIMARY (A2E2J07) pulsing at the rate given in Seq 8? **CAUTION:** Interface level (+5V to gnd)	Go to Seq 76.
75	If not:	Change A2E2.
76	Sync negative on −STAT BIT 2 WRT ID BURST (A1H2S13). Does +P TRACK ENV BRANCH (A1K2U02) become plus during the sync?	Change A2D2.
77	Does −DEVICE BUS IN P PRIMARY (A2D2S07) pulse at the rate given in Seq 8? **CAUTION:** Interface level (+5V to gnd)	Go to Seq 68.
78	Failure appears to be a cabling or device switch problem. Go to 18-010.	
79	Is −NRZI MODE (A1K2D10) minus?	Go to ALD BW231 GK6 and follow line back to failing point.
80	If not:	Change Y1Q2.
81	Does +BLOCK OR ENV LOSS BRANCH (A1K2U10) become plus while the sync is minus?	Go to ALD CC011 GC6 and follow line back to failing point.
82	If not:	Change A1K2.

From 14-000

ERROR DESCRIPTION:

In PE mode, Sense Byte 5, Bit 4 is set when IBG becomes active before the beginning ones marker is sensed and after BOR is sensed. It is set also when the beginning ones marker is not recognized within 56 bit cells after BOR is detected on a Read operation.

In 6250 bpi mode, Sense Byte 5, Bit 4 is set when IBG becomes active before the beginning mark 1 is sensed and after BOR is sensed. It is set also when the beginning mark 1 is not recognized within 140 bytes after BOR is detected in a Read operation.

Sense Byte 8, Bit 5 (Slow Begin Read Back Check) is also set if one byte is not read out of the deskew buffers (Write operation only).

Most Probable Causes:

The following list of cards can cause the problems covered in this procedure. The cards are listed with the highest probability first. Lines with multiple cards have the same probability. Cards separated by slashes are interchangeable.

Control Unit	Single Drive Failure
A. Y1P2	
B. Y1N2	
C. A1C2, A1K2, Y1Q2	Models (4, 6, 8) = T-A1K2
D. Y1K2/Y1L2/Y1M2, A2L2, A2Q2, Y1D2	Models (3, 5, 7) = T=A1K4
E. A1G2, B2E2, Y1H2	

ADDITIONAL CARDS AFFECTED:

Control Unit
A. Y1J2
B. Y1G2
C. A2D2
D. A2M2
E. Y1D2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problems or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Take the tape control offline. Do a RWD (07), WRT (01), RD BKWD (0C), RD FWD (02), in both PE and 6250 mode. Does the error occur on only one tape unit?	Go to 5B-000 for Models (4, 6, 8) Go to 5A-000 for Models (3, 5, 7)
2	Does the failure occur on a LWR or Write operation?	Go to Seq 6.
3	Try reading another previously written tape. If that tape can be read without errors, the original tape is bad.	
4	Can a previously written tape be read without read check errors?	Go to Seq 6.
5	If not:	Go to Seq 36.
6	Is IBG DROP sense bit (Sense Byte 8, Bit 0) ON?	Go to 17-080.
7	Is SLOW BEGIN RD BACK sense bit (Sense Byte 8, Bit 5) ON?	Go to Seq 30.
8	Is failure occurring in 6250 bpi mode?	Go to Seq 20.
9	Sync minus on −PE DECODE A7, (Y1H2U04). Is the sync present?	Go to Seq 12.
10	Sync minus on −GB FULL (Y1N2G08). Is the sync present?	Change Y1J2.
11	If not:	Go to ALD CB 441 and follow line back to failing point.
12	Scope −COMBINED ECC DATA 0-7 and −CRC DATA TRK 8. Were all points minus at first −PE DECODE A7 time? (Scope points are listed in Chart 1 on this page.)	Go to Seq 18.
13	Did any of the lines scoped in Seq 12 go minus?	Go to Seq 16.
14	Is +NRZI DEGATE ECC PH (Y1G2G11) plus?	Go to Seq 40.
15	If not:	Change Y1J2.
16	From Seq 12, determine the points not minus at the first −PE DECODE A7. Then interchange the cards in Y1K2, Y1M2, and Y1L2 and rescope the points listed in chart 2 on this page. Are the same points wrong?	Change Y1G2.
17	If not:	Isolate the defective card, then go to 00-030.
18	Does −FB DATA OR ALL ONES (Y1H2U09) go minus?	Change A2D2.
19	If not:	Change Y1H2.
20	Does −FB DATA OR ALL ONES (Y1H2U09) go minus?	Change A2D2.
21	Sync scope plus on +SET FORMAT CHAR (Y1J2P04). Is the sync present?	Go to Seq 24.
22	Sync scope minus on −GB FULL (Y1J2J04). Is the sync present?	Change Y1J2.
23	If not:	Go to Seq 10.
24	This sync should show pairs of plus pulses 50 ns long and 200 ns apart from leading edge to leading edge. Is either pulse missing?	Change Y1J2.
25	Scope −FORMAT CHAR TRK X, for a minus level at first sync time. (Scope points are on Chart 2 on this page.) Are any of the format lines wrong?	Change: Y1K2 for tracks 1, 3, or 4 Y1L2 for tracks 2, 6, or 7 Y1M2 for tracks P, 0, or 5
26	Is +A1 or B2 (Y1H2G12) plus between the 1st and 2nd pulses of the sync?	Change Y1J2.
27	Is +A3 or B3 (Y1H2G09) plus after the second sync pulse?	Change Y1J2.
28	Change sync to −GB FULL (Y1J2J04). Does −FB DATA OR ALL ONES (Y1H2U09) go minus during the sync?	Change A2D2.
29	If not: Change Y1H2.	
30	Do a PE Write operation. Is SKEW ERROR (Sense Byte 3, Bit 2) ON?	Go to 17-160.
31	Now do a Write or LWR operation (LWR if it fails) in the failing mode (6250 bpi or PE).	
32	Is −25 to 75 CLOCK BUS YB (Y1N2J13) a constant plus or minus? (Line should have 50 ns pulses).	Change A1C2.
33	Is −0 to 50 CLOCK BUS YB (Y1N2J12) a constant plus or minus? (Line should have 50 ns pulses).	Change A1C2.
34	Does −ROC ROTATIONS BRANCH (Y1N2D02) go minus?	Change A2M2.
35	If not:	Change in order: 1. Y1N2 2. Y1D2
36	Write up the tape in the failing mode with an '0E' Byte count and then do a RD or RD BKWD command, sync negative on −IBG (Y1P2M07). Is −BOR 27 COMB or DT BRANCH CONDITION (Y1P2J13) minus during sync pulse?	Change in order: 1. Y1P2 2. A2D2
37	Sync negative on −DEVICE BUS IN 0 TO DF (Y1T2M04). Does −ROC ROTATION (Y1N2D02) branch go minus during data time.	Change A2D2.
38	Is −TAPE OP (Y1N2G02) plus?	Change A1K2.
39	If not:	Change in order: 1. Y1N2 2. Y1D2
40	Is −NRZI MODE (Y1C2M03) minus?	Change A1K2.
41	If not:	Change Y1G2.

START READ CHECK (Cont'd)

Chart 1: ECC/CRC Scope Points

Zone	Trk	Line Name	Location
1	P	–CRC DATA TRK 8	Y1H2U03
	0	–ECC COMBINED DATA 0	Y1H2P13
	5	–ECC COMBINED DATA 5	Y1H2S05
2	2	–ECC COMBINED DATA 2	Y1H2S02
	6	–ECC COMBINED DATA 6	Y1H2S07
	7	–ECC COMBINED DATA 7	Y1H2U05
3	1	–ECC COMBINED DATA 1	Y1H2M13
	3	–ECC COMBINED DATA 3	Y1H2S03
	4	–ECC COMBINED DATA 4	Y1H2U02

Chart 2: Format Character Trk x

Zone	Trk	Location
1	P	Y1H2B04
	0	Y1H2J09
	5	Y1H2D05
2	2	Y1H2G11
	6	Y1H2D02
	7	Y1H2B03
3	1	Y1H2J10
	3	Y1H2J12
	4	Y1H2D03

NOTES:

17-076

From 14-000

IBG Detected On Write (Sense Byte 8, Bit 0)

Sense Byte 8, Bit 0 is set when writing 6250 or 1600 bpi if interblock gap (IBG) is detected while writing the data portion or if beginning of record (BOR) is not detected within a specified time after one track in each zone is detected.

Most Probable Causes:

The following list of cards can cause the problems covered in this procedure. The cards are listed with the highest probability first. Lines with multiple cards have the same probability.

Control Unit
A. A1C2, A1K2, Y1P2

Single Tape Unit
A. Dirty head
B. Tape creased

ADDITIONAL CARDS AFFECTED:

A. A2D2
B. A2T2
C. A2R2
D. B2E2
E. A2Q2
F. A2L2
G. Y1Q2
H. Y1T2
I. Y1S2
J. Y1R2
K. A2E2
L. A1G2
M. A1E2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problems or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Is this a single tape unit failure?	For Models (4, 6, 8), go to 5B-000. For Models (3, 5, 7), go to 5A-000.
2	Is the failure on a write tape mark operation?	Go to Seq 8.
3	Sync negative on –STAT BIT 0 TAPE OP TO DF (A1K2U06). During a Write command with 'fixed length records,' display on the scope the time period when the sync becomes minus to the time +END OF DATA PWR (Y1H2M09) becomes plus.	
4	Does –IBG BRANCH (Y1P2M07) ever become minus after it first went plus in the time period displayed in Seq 3 or 8?	Go to Seq 9.
5	Does –BOR 27 COMB OR DT BRANCH COND (Y1P2J13) ever become plus after it first became minus during the time period setup in Seq 3 or 8?	Go to Seq 9.
6	Does +BLOCK OR ENV LOSS BRANCH (Y1P2S10) ever become minus after it first became plus during the time period setup in Seq 3 or 8?	Go to Seq 9.
7	If not:	Change A2D2.
8	Sync negative on –STAT BIT 0 TAPE OP to DF (A1K2U06). During a Write Tape Mark operation, display on the scope the time period from the minus sync during the time DCC ERROR OR SAGC BRANCH (A2D2M09) becomes active.	Go to Seq 4.

Seq	Condition/Instruction	Action
9	Check all lines. Do these lines become active while the sync is minus for the proper model and mode being operated? –Write SLD Level Y1Q2D12 SLD –6250 Density SLD Y1Q2J02 SLD –6250 Y1Q2M07 MST –PE Y1Q2P05 MST –6250 Y1Q2P06 MST –PE Y1Q2M05 MST –6250 Y1Q2P04 MST –PE Y1Q2M04 MST +NRZI Y1Q2U13 MST +Low Gain Y1Q2B02 MST This line is always minus. –PE SLD Level Y1Q2D03 SLD This line is always plus. –SLD - 6250 Y1Q2D05 SLD These lines are minus for 75 and 200 ips models. –PE1 SLD Y1Q2G05 SLD –6250 SLD Y1Q2D11 SLD –B Y1Q2B03 MST These lines are minus for 75 and 125 ips models. –6250 SLD Y1Q2D07 SLD –PE2 SLD Y1Q2G03 SLD This line is minus for 125 and 200 ips models. –A Y1Q2B05 MST Are all levels correct?	
10	Is +P.E. WRITE AND TAPE OP (Y1Q2B12) plus while the sync is minus?	Go to Seq 13.
11	Is –XOUTA BIT 5 ALU1 TO DF (A1K2U07) minus when the sync is minus?	Change A1K2.
12	If not:	Change in order: 1. A2T2 2. B2E2
13	Are the following lines minus while the sync is minus for the model being used? 75 IPS 125 IPS 200 IPS –XOUTA BIT 7 ALU2 TO DF Y1Q2B07 ON OFF ON –XOUTA BIT 5 ALU2 TO DF Y1Q2B10 OFF ON ON	Go to Seq 15.
14	If not:	Change in order: 1. A2Q2 2. A2L2
15	Scope +PE MODE (Y1Q2D02) for the proper level during the time the sync is minus. It should be plus if you are operating in PE Mode. Is it good?	Go to Seq 18.

Seq	Condition/Instruction	Action
16	–XOUTA BIT 0 ALU2 TO DF (A1K2S13) should be minus while the sync is minus if it is in PE mode. Is this line good during the operating mode?	Change A1K2.
17	If not:	Change in order: 1. A2Q2 2. A2L2
18	+STAT BIT 2 ALU WR ID BRST (Y1Q2D06) should be minus when the sync is minus, except for a portion of the time during an operation at load point. Is it good?	Change Y1Q2.
19	If not:	Change in order: 1. A2Q2 2. A2L2
20	The following lines should be minus during the time the sync is minus, except for tracks 1, 3, and 4 on a Write Tape Mark operation. Are they all good? **Zone 1** –DEVICE BUS IN 0 to DF Y1T2M04 –DEVICE BUS IN P TO DF Y1T2S04 –DEVICE BUS IN 5 TO DF Y1T2D13 **Zone 2** –DEVICE BUS IN 2 TO DF Y1S2M04 –DEVICE BUS IN 6 TO DF Y1S2S04 –DEVICE BUS IN 7 TO DF Y1S2D13 **Zone 3** –DEVICE BUS IN 1 TO DF Y1R2M04 –DEVICE BUS IN 3 TO DF Y1R2S04 –DEVICE BUS IN 4 TO DF Y1R2D13	Replace these cards one at a time: 1. Y1P2 2. Y1T2 (ZONE 1) 3. Y1S2 (ZONE 2) 4. Y1R2 (ZONE 3) Y1T2, Y1S2, Y1R2 are interchangeable.
21	Check the following Tape Unit Bus Out lines to see if they match the Device Bus In lines. Do they match while the sync is minus? –TUBO BIT P A1H2U07 –TUBO BIT 0 A2R2S03 –TUBO BIT 1 A2R2B12 –TUBO BIT 2 A1R2D05 –TUBO BIT 3 A2R2G02 –TUBO BIT 4 A2R2B07 –TUBO BIT 5 A2R2B10 –TUBO BIT 6 A2R2G13 –TUBO BIT 7 A2R2S02	Go to Seq 30.
22	Is this a 1x8 machine?	Go to Seq 28.
23	Is the tape unit being used to troubleshoot the failure connected directly to the tape control you are using?	Go to Seq 26.
24	Check the following lines to see if they match the TUBO lines in Seq 21. Do they match while the sync is minus? Voltage 0V to +5V –BUS OUT P PRIMARY A2E2J07 –BUS OUT 0 PRIMARY A2E2G09 –BUS OUT 1 PRIMARY A2E2D03 –BUS OUT 2 PRIMARY A2E2D04 –BUS OUT 3 PRIMARY A2E2B09 –BUS OUT 4 PRIMARY A2E2D09 –BUS OUT 5 PRIMARY A2E2P07 –BUS OUT 6 PRIMARY A2E2M09 –BUS OUT 7 PRIMARY A2E2P02	Go to 18-010.

IBG DETECTED ON WRITE (Cont'd)

Seq	Condition/Instruction	Action
25	If not:	Change A2E2.
26	Check the following lines to see if they match the TUBO lines in Seq 21. Do they match while the sync is minus? −BUS OUT P SECONDARY A2E2G07 −BUS OUT 0 SECONDARY A2E2G08 −BUS OUT 1 SECONDARY A2E2B03 −BUS OUT 2 SECONDARY A2E2B04 −BUS OUT 3 SECONDARY A2E2B12 −BUS OUT 4 SECONDARY A2E2D13 −BUS OUT 5 SECONDARY A2E2M07 −BUS OUT 6 SECONDARY A2E2M08 −BUS OUT 7 SECONDARY A2E2M08	Go to 18-010.
27	If not:	Change A2E2.
28	Check the following lines to see if they match the TUBO lines in Seq 21. Do they match while the sync is minus? Voltage 0V to +5V −BUS OUT P A2E2G07 −BUS OUT 0 A2E2G08 −BUS OUT 1 A2E2B03 −BUS OUT 2 A2E2B04 −BUS OUT 3 A2E2B12 −BUS OUT 4 A2E2D13 −BUS OUT 5 A2E2M07 −BUS OUT 6 A2E2M08 −BUS OUT 7 A2E2U11	Go to 18-010.
29	If not:	Change A2E2.
30	Does −GATE WRITE (A1H2D03) go minus while the sync is minus?	Go to Seq 32.
31	Does +INHIBIT WRITE (A1G2S12) go plus while the sync is minus?	Go to Seq 47.
32	Does −GATE WRITE NOT TM (A1H2J06) go minus while the sync is minus?	Go to Seq 36.
33	Is the failure on a Write Tape Mark command?	Go to Seq 36.
34	Does −XOUTA BIT 3 ALU1 to DF (A1G2B03) go minus while the sync is minus?	Change in order: 1. A2T2 2. B2E2
35	If not:	Change A1G2.
36	Does −WR TRIGGER GATE (A1G2P10) pulse while the sync is minus?	Go to Seq 38.
37	If not:	Change A1G2.
38	Does the failure occur while operating in 6250 bpi?	Go to Seq 44.
39	Does +WRITE TIME GATE (A1G2G03) pulse while the sync is minus?	Change in order: 1. A1G2 2. Y1Q2 3. A1E2 (7-track)
40	Is −6250 MODE (A1G2M07) minus when the sync is minus?	Go to Seq 42.
41	If not:	Change A1G2.
42	Is −XOUTA BIT 0 ALU2 TO DF (A1K2S13) minus when the sync is minus?	Change in order: 1. A2Q2. 2. A2L2
43	If not:	Change A1K2.
44	Is +WRITE TIME GATE (A1G2G03) plus when the sync is minus?	Change A1G2.
45	Is −XOUTA BIT 0 ALU2 TO DF (A1K2S13) minus when the sync is minus?	Change A1K2.
46	If not:	Change in order: 1. A2Q2 2. A2L2
47	Does −STAT BIT 3 DIAGNOSTIC MODE (A1K2G08) or −STAT BIT 2 TO DF (A1K2U09) go minus while the sync is minus?	Go to Seq 49.
48	If not:	Change A1K2.
49	Is the failure on a NRZI Write Tape Mark command?	Change A2R2.
50	If not:	Change in order: 1. A2T2 2. B2E2

17-081

EARLY BEGIN READBACK CHECK

From 14-000

ERROR DESCRIPTION:

Sense Byte 8, Bit 3 is set when beginning of block (BOB) is active too soon during a Write or Write Tape Mark operation, or the interval

from writing the last zero until interblock gap (IBG) is sensed (TU FAST) is too short. In 1600 bpi mode, Sense Byte 8, Bit 3 sets Data Check. In 6250 bpi Write mode, Sense Byte 8, Bit 3 sets Equipment Check.

Most Probable Causes:

The following list of cards can cause the problems covered in this MAP. The cards are listed with the highest probability first. Lines with multiple cards have the same probability. Cards separated by slashes are interchangeable.

Control Unit	Single Tape Unit
A. Y1P2	A. Air leak
B. Y1T2/S2/R2	B. Erase head
C. Y1D2, Y1H2	C. Magnetized read head
D. Y1C2, A2D2	

ADDITIONAL CARDS AFFECTED:

A. A2D2
B. Y1Q2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise.
Remember to END all problems or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Is this a single tape unit failure? For Models (4, 6, 8), go to 5B-000. For Models (3, 5, 7), go to 5A-000.	
1A	Is failure in NRZI mode (Sense Byte 6, Bit 4 OFF and Bit 3 ON)? Go to Seq 8.	
2	Sync negative on –TAPE OP A (A1K2B10) and scope the following DEVICE BUS IN to DF lines. Does +BLOCK OR ENV LOSS BRANCH (A2D2M08) become plus before any of the DEVICE BUS IN to DF lines pulse? **Zone 1** –DEVICE BUS IN 0 TO DF Y1T2M04 –DEVICE BUS IN P TO DF Y1T2S04 –DEVICE BUS IN 5 TO DF Y1T2D13 **Zone 2** –DEVICE BUS IN 2 TO DF Y1S2M04 –DEVICE BUS IN 6 TO DF Y1S2S04 –DEVICE BUS IN 7 TO DF Y1S2D13 **Zone 3** –DEVICE BUS IN 1 TO DF Y1R2M04 –DEVICE BUS IN 3 TO DF Y1R2S04 –DEVICE BUS IN 4 TO DF Y1R2D13	Go to Seq 4.
3	If not:	Change A2D2.
4	Are any of the following time sense lines minus before the corresponding DEVICE BUS IN to DF line begins to pulse? **Zone1** –TIME SENSE P Y1P2P03 –TIME SENSE 0 Y1P2P09 –TIME SENSE TK 5 Y1P2D10 **Zone 2** –TIME SENSE 2 Y1P2G13 –TIME SENSE 6 Y1P2M12 –TIME SENSE TK 7 Y1P2G12 **Zone 3** –TIME SENSE 1 Y1P2P02 –TIME SENSE 3 Y1P2P10 –TIME SENSE TK 4 Y1P2S12	Go to Seq 6.
5	If not:	Change Y1P2.
6	Referring to Seq 4, are all the time sense lines minus before the corresponding DEVICE BUS IN to DF line begins to pulse?	Change Y1Q2.
7	If not: Replace the card in the zone that was bad in Seq 4. Zone 1, change Y1T2. Zone 2, change Y1S2. Zone 3, change Y1R2. These cards are interchangeable.	
8	Sync negative on –STAT BIT 1 START WR RD (Y1C2S11) and look at –FB DATA OR ALL ONES (A2D2U04). Is –FB DATA OR ALL ONES (A2D2U04) ever minus during the window created from the time the sync becomes minus until the time period listed expires? Model 7 — .55 msec. Model 5 — .9 msec. Model 3 — 1.5 msec. Go to Seq 10.	
9	If not: Change A2D2.	
10	Is +NRZI CHAR GATE (Y1H2S12) ever plus in the window from Seq 8? Go to Seq 12.	
11	If not: Change Y1H2.	
12	Is –SET NRZI FIRST BIT (Y1C2G03) ever minus in the window from Seq 8? hange Y1D2.	
13	If not: Change Y1C2.	

From 14-000

ERROR DESCRIPTION:

Sense Byte 3, Bit 1 is set:

1. During a 6250 bpi Write operation at the end of data (EOD) time, if two or more tracks have required correction, or if hardware pointers have been set in two or more tracks between resync bursts and no time sensors have dropped.
2. During a 6250 bpi Read operation at the end of data (EOD) time, if more than two tracks have required correction.
3. During a PE Read operation, if hardware pointers have been set (Phase Errors occurred) in two or more tracks and a vertical redundancy check (VRC) error occurred.

Note: If any tracks dropped below an acceptable amplitude level, Envelope Error (Sense Byte 3, Bit 4) would also be set.

Most Probable Cause:

The following list of cards can cause the problems covered in this procedure. The cards are listed with the highest probability first. Lines with multiple cards have the same probability.

A. Y1J2
B. A1K2, Y1D2, Y1F2, Y1G2, Y1H2

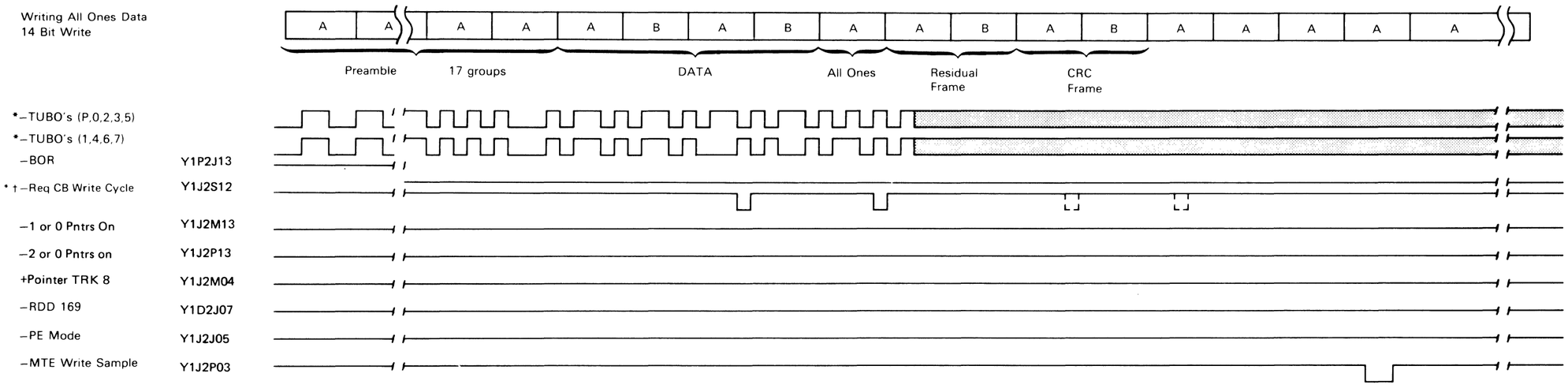
Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problems or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Write all ones data in the failing mode. Use the LWR command if the tape unit fails with this command, otherwise use the Write command. Write 14 byte, 0B0 (Hex), records in 6250 bpi mode or eight byte records in PE mode.	
2	If the tape unit is failing on a Write operation, continue following this procedure. If it is failing on a Read operation, read the prewritten tape and proceed.	
3	Sync the scope positive on −IBG (Y1P2M07).	
4	Is +MTE OR LRCR ERROR (A1K2S02) always minus?	Change A1K2.
5	Is the tape unit failing in NRZI mode? (See the Mode Chart on this page.)	Go to 17-310.
6	Is the unit failing on a Write operation (Byte 1, Bit 5 ON)?	Go to Seq 15.
7	Is the unit failing in PE mode? (See the Mode Chart on this page.)	Go to Seq 15.
8	Is −PE MODE (Y1J2J05) minus?	Go to ALD BW231GJ6 and follow line back to failing card.
9	Does −RDD169 (Y1D2J07) ever go minus?	Go to ALD CN221CG6 and follow line back to failing card.
10	Is +WRITE AND TAPE OP (Y1J2M11) minus?	Go to ALD BW231GF2 and follow line back to failing card.
11	Is −MTE WRT SAMPLE (Y1J2P03) bad? (See timing chart on 17-111.)	Go to ALD CH131 and follow line back to failing card.
12	Is −REQ CB WRITE CYCLE (Y1J2S12) good? (See timing chart on 17-111.)	Change in order: 1. Y1J2 2. Y1D2
13	Is +NRZI WRITE REQ (Y1J2S10) plus?	Go to ALD CN291DC6 in logic and follow line back to failing card.
14	If not:	Go to ALD CH021GE2 and follow the −REQ CB WRT CYCLE line back to the failing card.
15	Do two or more + POINTER TRACK x lines go plus during the record? (See 17-701 for test points)	Go to 17-701.
16	Is one of these lines ever active during the record? −2 OR 0 POINTERS ON—Y1F2P05 −1 OR 0 POINTERS ON—Y1F2P02 +POINTER TRK 8—Y1G2M04	Change Y1F2.
17	Does −RDD169 (Y1D2J07) ever go minus?	Go to ALD CN221CG6 and follow line back to failing card.
18	If not:	Go to Seq 11.

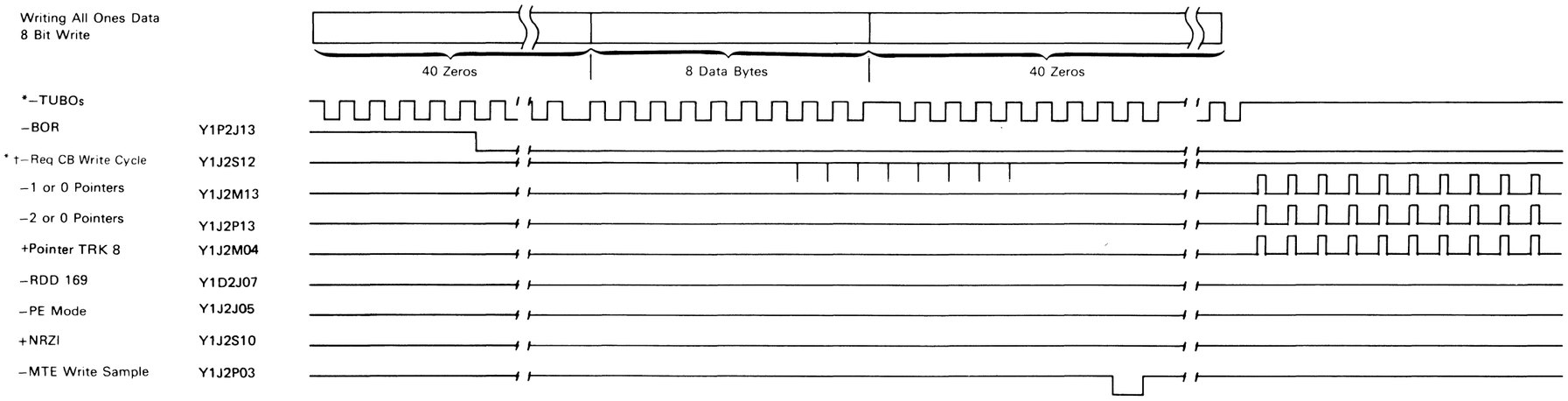
Mode Chart Sense Byte 6

TU FEATURE	MODE BITS			
	0	2	3	4
7 Track NRZI	X			
1600 bpi (Mod 4, 6, 8)		X		X
6250 bpi		*	X	X
1600 bpi (Mod 3, 5, 7)		*		
9 Track NRZI		X	X	

* Can be on or off. ON for Dual Density, OFF for single density.



PE MODE



* Number of pulses will change with byte count.
† No fixed timing relationship with TUBO units.
± 700 ns long regardless of tape unit speed

MULTI-TRACK ERROR (MTE)

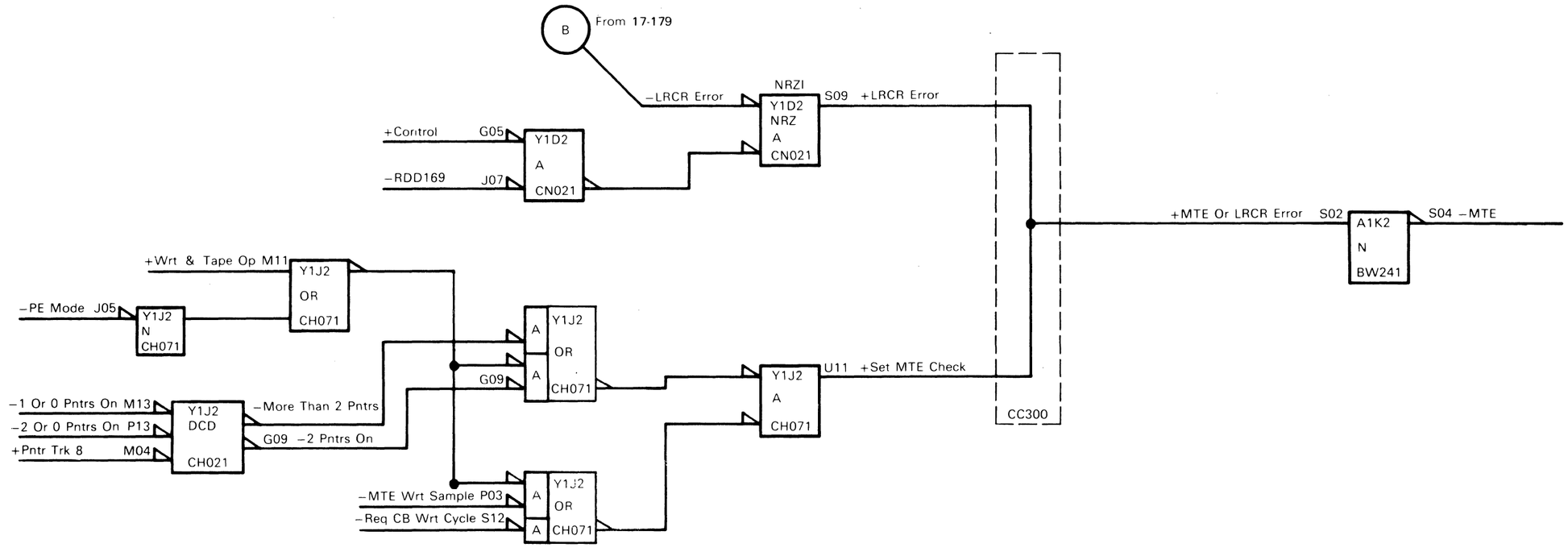
Sense byte 3, bit 1 is set:

A. 6250 Write - when two or more tracks require correction at end of data time (MTE Write Sample), or when hardware pointers are set in two or more tracks between resync bursts and no time sensors drop.

B. 6250 Read - if hardware pointers are set in more than two tracks.

C. PE - if hardware pointers are set in two or more tracks.

D. NRZI - MTE will be set on a longitudinal redundancy check register (LRCR) error.



3803-2/3420

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SLOW END READ BACK CHECK

From 14-000

ERROR DESCRIPTION:

Sense Byte 8, Bit 6 is set if End of Data (EOD) is not detected during a write operation. This sense bit is also set when the interval from the writing of the last TM (Tape Mark) character until the detection of IBG (Interblock Gap) exceeds 267 bit cell times.

Most Probable Causes:

The following list is of the known cards which can cause the problems covered in this procedure. The cards are listed with the highest probability first. Lines with multiple cards have the same probability.

A. Y1H2, Y1Q2
B. A1H2, Y1C2, Y1J2, Y1N2

ADDITIONAL CARDS AFFECTED:

A. A2D2
B. A1C2
C. Y1P2
D. Y1T2
E. Y1S2
F. Y1R2
g. A1G2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problems or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Is this a single tape unit failure?	For Models (4, 6, 8), go to 5B-000. For Models (3, 5, 7), go to 5A-000.
1A	Take the tape control offline and set up the CE panel to perform the failing command (Write or Write Tape Mark) in the failing mode (6250, PE, or NRZI).	
2	Is the failure occurring in NRZI Mode (Sense Byte 6, bit 4, OFF, bit 0 or 3, ON)?	Go to Seq 8.
3	Is the failure occurring on a Write Tape Mark operation?	Go to Seq 12.
4	Sync negative on –TAPE OP A (Y1H2D10) and reference the time there is Read Data (–DEVICE BUS IN P TO DF–Y1T2S04). Does –EOD OR CRC OK DOT (A2D2S12) become minus before the end of the Read Data?	Change A2D2.
5	Scope the following lines to ensure they pulse: +SET FORMAT CHARACTER Y1H2D04 +RESET FORMAT LTHs Y1H2B02 +RESET VOTE LTHs Y1H2G08 +A1 OR B1 Y1H2G12 +A3 OR B3 Y1H2G09 Do they all pulse?	Change Y1H2.
6	Scope the following lines to ensure they pulse: –25-75 CLOCK BUS YA Y1J2D09 –0-50 CLOCK BUS YA Y1J2J11 Do they both pulse?	Change Y1J2.
7	If not:	Change A1C2.
8	Sync negative on –TAPE OP A (Y1H2D10). Does +EOD NRZI (Y1C2P10) become plus during the sync and stay plus until the sync falls?	Go to Seq 10.
9	If not:	Change Y1C2.
10	Does –EOD or CRC OK DOT (A2D2S12) become minus during the sync and stay minus until the sync falls?	Change A2D2.
11	If not:	Change Y1H2.
12	Sync negative on –TAPE OP A (Y1H2D10) and reference the time there is Read Data (–DEVICE BUS IN P TO DF–Y1T2S04). Does –IBG BRANCH (A2D2U13) become minus shortly (under ten bit periods) after the end of Read Data?	Change A2D2.
13	Ensure all the following time sense lines are plus shortly after the end of Read Data: **Zone 1** –TIME SENSE P Y1P2P03 –TIME SENSE 0 Y1P2P09 –TIME SENSE TK 5 Y1P2D10 **Zone 2** –TIME SENSE 2 Y1P2G13 –TIME SENSE 6 Y1P2M12 –TIME SENSE TK 7 Y1P2G12 **Zone 3** –TIME SENSE 1 Y1P2P02 –TIME SENSE 3 Y1P2P10 –TIME SENSE TK 4 Y1P2S12 Are they all plus at the end of Read Data?	Change Y1P2.
14	Ensure that all pulsing DEVICE BUS IN to DF lines stop at the same time, and that the corresponding time sense is minus more than ten bits after data on the DEVICE BUS IN to DF ended. **Zone 1** –DEVICE BUS IN 0 TO DF Y1T2M04 –DEVICE BUS IN P TO DF Y1T2S04 –DEVICE BUS IN 5 TO DF Y1T2D13 **Zone 2** –DEVICE BUS IN 2 TO DF Y1S2M04 –DEVICE BUS IN 6 TO DF Y1S2S04 –DEVICE BUS IN 7 TO DF Y1S2D13 **Zone 3** –DEVICE BUS IN 1 TO DF Y1R2M04 –DEVICE BUS IN 3 TO DF Y1R2S04 –DEVICE BUS IN 4 TO DF Y1R2D13 Do the time sense lines stay minus too long?	Change the card that contains the Zone in which the line was bad. If there were bad lines in more than one Zone, change Y1Q2 first. Zone 1, change Y1T2. Zone 2, change Y1S2. Zone 3, change Y1R2.
15	If not:	Change A1G2.

SKEW — RIC EQUALS ROC

From 14-000, 14-012, 17-070, 17-700

ERROR DESCRIPTION:

Sense Byte 3, Bit 2 is set when excessive skew (any RIC is equal to the ROC) is detected during a PE Write, PE Read or Read Backward, 6250 bpi Read or Write or a NRZI Write operation.

A. For a PE Write operation, this sense bit is set if the RIC (Read In Counter) exceeds the ROC (Read Out Counter) by 4 counts on any track.

B. For a PE Read or Read Backward operation, this sense bit is not set under normal conditions. ALMOST SKEW is recognized when RIC is greater than ROC by 14 counts. This condition sets the dead track register which does not recognize RIC for that track and allows ROC to cycle. If the dead track register recognizes RIC or is not set, Skew Error is then set when RIC is greater than ROC by a 30-count difference.

C. For a 6250 bpi Write operation, this sense bit is set if there is no envelope before the residual frame time.

D. For a 6250 bpi Read operation, this sense bit is not set under normal conditions. ALMOST SKEW is recognized when RIC is greater than ROC by 26 counts. This conditions sets the dead track register which does not recognize RIC for that track and allows ROC to cycle. If the dead track register recognizes RIC or is not set, Skew Error is then set when RIC is greater than ROC by a 30-count difference.

E. NRZI skew is the time lapse between the receipt of the first and the last bit of a data byte. For a NRZI Write operation, this sense bit is set when a set first bit comes after 9 time (about 28% of the total bit period time elapsed).

Most Probable Causes:

The following list is of the known cards which can cause the problems covered in this procedure. The cards are listed with the highest probability first. Lines with multiple cards have the same probability. Cards separated by slashes are interchangeable.

Control Unit

A. Y1Q2
B. Y1R2/Y1S2/Y1T2
C. Y1P2
D. Y1N2
E. Y1K2/Y1L2/Y1M2
F. Y1J2
G. A1C2
H. A1K2
I. A2Q2
J. Y1C2, Y1D2
K. (7-Track only) A1E2, A1L2

Single Tape Unit

A. Skew improperly adgusted
B. T-A1J2
C. T-A1J2
D. Dirty head
E. Read/write card
F. Read/write head

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise.
Remember to END all problems or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Is this a single tape unit failure?	For Models 4, 6, 8, go to 5B-000. For models 3, 5, 7, go to 5A-000.
1A	Take the tape control offline. Operate the Reset switch. Is the SKEW ERROR light on after a reset?	Change A1K2.
2	Do a Write (01) operation using the failing mode. Count of FC0. Write data FF0. Does +SKEW CHK (A1K2S12) pulse?	Go to Seq 9.
3	Is +SKEW CHK (A1K2S12) always minus?	Change A1K2.
4	Does the tape control have NRZI feature?	Go to Seq 7.
5	Remove Y1N2. Does +SKEW CHK (A1K2S12) go minus?	Change Y1N2.
6	If not: Put Y1N2 back in the tape control.	Change in order: 1. Y1M2 2. Y1L2 3. Y1K2
7	Remove Y1C2. Does the +SKEW CHK (A1K2S12) go minus?	Change A1K2.
8	If not: Put Y1C2 back in the tape control.	Go to Seq 5.
9	Do a LWR (with gaps, count 0B0, write data FF0). Use the failing mode (PE, 6250). (If NRZI mode fails, use a Read Op.)	
10	Check the following clock timings: A1C2S10 A1C2S12 A1C2S13 A1C2U09 A1C2U11 Are any clock timing lines at a solid level?	Change A1C2.
11	Does the tape control fail in 6250 mode? (Check sense byte 6 for mode.)	Go to Seq 19.
12	Does the tape control fail in PE mode? (Check sense byte 6 for mode.)	Go to Seq 72.
13	Does the tape control fail in NRZI mode? (Check sense byte 6 for mode.)	Go to Seq 15.
14	If not:	Recheck symptoms.
15	Do a write command (Data FF0, byte count 0B0) in NRZI mode.	
16	Sync the scope minus on −WRT AND TAPE OP (Y1C2U06). Set time base to display a complete record. Is −WRITE AND TAPE OP failing to pulse?	Change A1K2.
17	Does +NRZI CHAR GATE FREQ (Y1C2D04) go plus during the time −WRT AND TAPE OP is plus?	Change Y1C2.
18	If not:	Change in order: 1. Y1D2 2. Y1N2 3. Y1M2/L2/K2
19	Does the tape control fail in a 6250 bpi write operation? (Check sense bytes 6 and 1.)	Go to Seq 37.
20	Do a Read or LWR (with gaps, count 0B0, write data FF0) in the failing mode (PE or 6250). LWR should be used if it fails.	
21	Sync the scope minus on −BOR (Y1P2J13). Does the scope fail to sync? Set time base to display the complete record.	Go to ALD CC001 GM6 and follow line to point of failure.
22	Is +SOME TRACK MARG ZN 1 (DOT OR) (Y1M2S02) plus during sync time (−BOR)?	Go to Seq 26.
23	Is +EXCESSIVE SKEW (DOT OR) (Y1M2P13) minus all the time?	Change A1K2.
24	Is −WRITE AND TAPE OP minus all the time?	Go to ALD BW231 GF6 and follow Y1N2J09 line back to point of failure.
25	If not:	Change in order: 1. Y1M2/L2/K2 2. Y1N2 3. Y1C2
26	Are any +DEAD TRACK REGISTERS set after the +SOME TRACK MARG ZN 1 (DOT OR) (Y1M2S02) becomes plus? See test point chart on 17-162.	Go to Seq 31.
27	Does −SKEW ERROR (A1K2P11) become active before −ROC CYCLED (Y1G2P11) is minus?	Go to Seq 33.
28	Is the −POINTER BUS and +ALMOST SKEW lines active at the same time for the failing tracks? See test point chart on 17-162.	Change Y1P2.
29	Is −Gated PGM SYNC (Y1G2M11) good? See 6250 or timing chart on 17-163 or PE write timing chart on 17-165, depending on the mode of operation.	Change Y1P2.
30	If not:	Go to ALD CC121 BM6 and follow line to point of failure.
31	Check the −NO COMP lines. Is one of the zones coming up late? See test point chart on 17-162, and the PE timing chart on 17-165 or 6250 timing chart on 17-163, depending on mode of operation.	Change card for late zone. Zone 1 - Y1M2 Zone 2 - Y1L2 Zone 3 - Y1K2
32	If not:	Go to Seq 28.
33	Are more than two +PE WRITE SKEW lines plus? See test point chart on 17-162.	Go to Seq 28.
34	Are all the +PE WRT SKEW lines plus all the time? See test point chart on 17-162.	Change Y1M2.

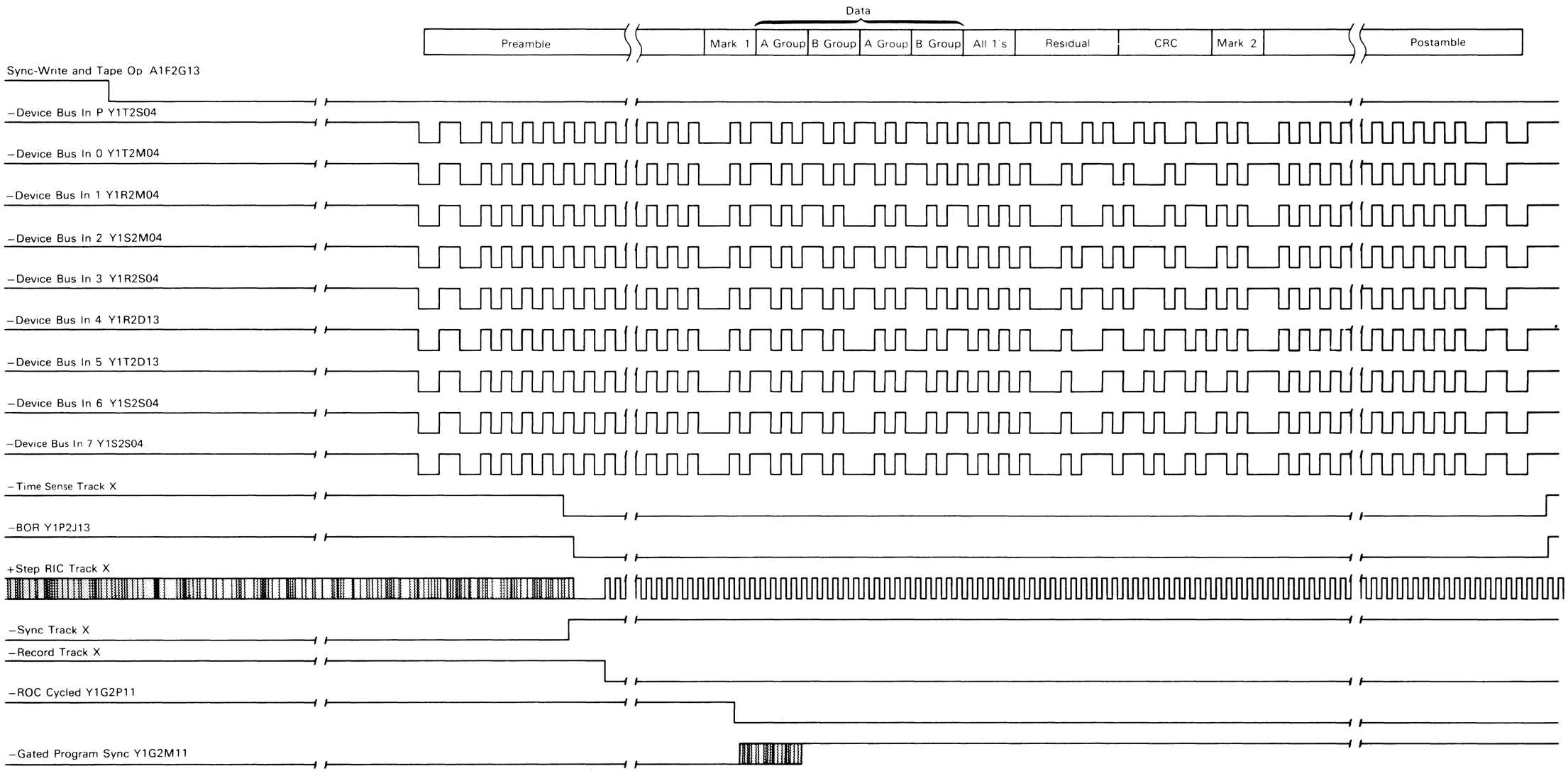
Seq	Condition/Instruction	Action
35	Is the –POINTER BUS minus at the time of the error for the failing track? See test point chart on 17-162.	Change Y1P2.
36	If not:	Go to Seq 29.
37	Do a Write or LWR (with gaps, count 0B0, write data FF0) in 6250 mode. Sync the scope minus on –WRITE CONDITION (A1G2G07) 20 microseconds per division. When doing a 6250 LWR, tape must be away from load point.	
38	Are the –PE lines (Y1Q2P05, Y1Q2M05, and Y1Q2M04) all plus?	Go to Seq 40.
39	If not:	Change Y1Q2.
40	Are the –6250 lines (Y1Q2M07, Y1Q2P06, and Y1Q2P04) all minus?	Go to Seq 42.
41	If not:	Change Y1Q2.
42	Is +6250 WRT SKEW (DOT OR) (Y1M2M04) solid plus during the entire record?	Change in order: 1. Y1M2 2. Y1K2 3. Y1L2
43	Do all the –VFC DATA lines pulse? See test point chart on 17-162.	Go to Seq 48.
44	Check the –DEVICE BUS IN to DF lines for the failing tracks. Are they good? See 6250 timing chart on 17-163, and test point chart on 17-162.	Go to Seq 62.
45	Compare the –BUS IN lines from the tape unit to the –DEVICE BUS IN TO DF timing charts. Are they the same? See 6250 timing chart on 17-162.	Change in order: 1. Y1C2 2. A2D2
46	Does the tape control have the device switch feature?	Change in order: 1. Y1C2 2. A2D2
47	If not:	Go to 18-010.
48	Do all the –VFC PRIME DATA lines pulse? See test point chart on 17-162.	Go to Seq 50.
49	Change cards for bad zone group.	Zone 1 - Y1T2 Zone 2 - Y1S2 Zone 3 - Y1R2
50	Check +RIC RESET lines for all tracks. Are any bad? See timing chart on 17-165 and test point chart on 17-162.	Go to Seq 84.
51	Compare the –NO COMP lines for each zone to the +6250 WRT SKEW (DOT OR) (Y1L2M04). See test point chart on 17-162.	
52	Are the –NO COMP lines minus at the time +6250 WRT SKEW (DOT OR) (Y1L2M04) goes plus?	Go to Seq 55.
53	Check +STEP RIC for all tracks of the failing zone. Do they pulse? See test point chart on 17-162.	Go to Seq 81.
54	If not:	Change the bad zone: Zone 1 - Y1T2 Zone 2 - Y1S2 Zone 3 - Y1R2
55	Is +GB FULL (Y1N2G08) bad? See 6250 timing chart on 17-164 or timing chart on 17-165, depending on mode.	Change Y1N2.
56	Is +ECC GROUP FULL (Y1J2U07) bad? See 6250 timing chart on 17-164 or PE timing chart on 17-165, depending on mode.	Change Y1J2.
57	Is –TAPE OP (Y1P2M03) plus?	Change A1K2.
58	Is +A+B 3 25-75 (Y1N2J04) at a solid level?	Change Y1J2.
59	Does –WRITE OSCILLATOR (Y1P2U12) pulse during the first part of the preamble?	Go to Seq 81.
60	Does –CLOCK SYNC FREQUENCY OSC (Y1P2U07) pulse?	Change Y1P2.
61	If not:	Change A1K2.
62	Are all –VFC DATA lines failing to pulse? See test point chart on 17-162.	Go to Seq 66.
63	If not:	Change the failing zone: Zone 1 - Y1T2 Zone 2 - Y1S2 Zone 3 - Y1R2
64	Does +LOW GAIN (Y1P2U12) go plus during the preamble and stay plus through the postamble?	Change A2Q2.
65	If not:	Go to Seq 90.
66	Does –WRITE OSCILLATOR (Y1Q2B10) pulse?	Go to Seq 68.
67	If not:	Change A2Q2.
68	Are the –RECORD TRACK X lines for all tracks the same? See test point chart on 17-162.	Change the failing zone: Zone 1 - Y1T2 Zone 2 - Y1S2 Zone 3 - Y1R2
69	If not:	Change in order: 1. Y1P2 2. Y1Q2
70	Do a Write or LWR (byte count 0B0, data FF0, with gaps) in PE mode. Sync the scope minus on –WRITE CONDITION (A1G2G07) 50 microseconds per division. Use LWR if it will fail.	
71	Are the –6250 lines (Y1Q2M07, Y1Q2P06, and Y1Q2P04) (all three) plus?	Go to Seq 73.
72	If not:	Change Y1Q2.
73	Are the –PE lines (Y1Q2P05, Y1Q2M05, and Y1Q2M04) (all three) minus?	Go to Seq 75.
74	If not:	Change Y1Q2.
75	Is +PE WRT SKEW (DOT OR) (Y1M2P06) plus all the time?	Change in order: 1. Y1M2 2. Y1L2 3. Y1K2
76	Check the –VFC PRIME DATA lines for all tracks. Do they pulse? See 17-162.	Go to Seq 79.
77	Do all tracks fail to pulse?	Go to Seq 64.
78	Change the bad zone.	Zone 1 - Y1T2 Zone 2 - Y1S2 Zone 3 - Y1R2
79	Do all the –VFC DATA lines pulse? See test point chart on 17-162.	Go to Seq 81.
80	If not:	Go to Seq 88.
81	Compare the –RECORD TRACK X lines for all tracks. Are any different? See test point chart on 17-162.	Go to Seq 92.
82	Does –STEP CTR LTH (Y1J2P12) pulse?	Change in order: 1. Y1M2 2. Y1L2 3. Y1K2
83	If not:	Change Y1J2.
84	Are all +RIC RESETS bad? See 17-162.	Go to Seq 64.
85	Is +RESET I CNT (Y1J2P10) at a solid level?	Change Y1J2.
86	Is +RESET FORMAT LTCHS (Y1J2S09) at a solid level?	Change Y1J2.

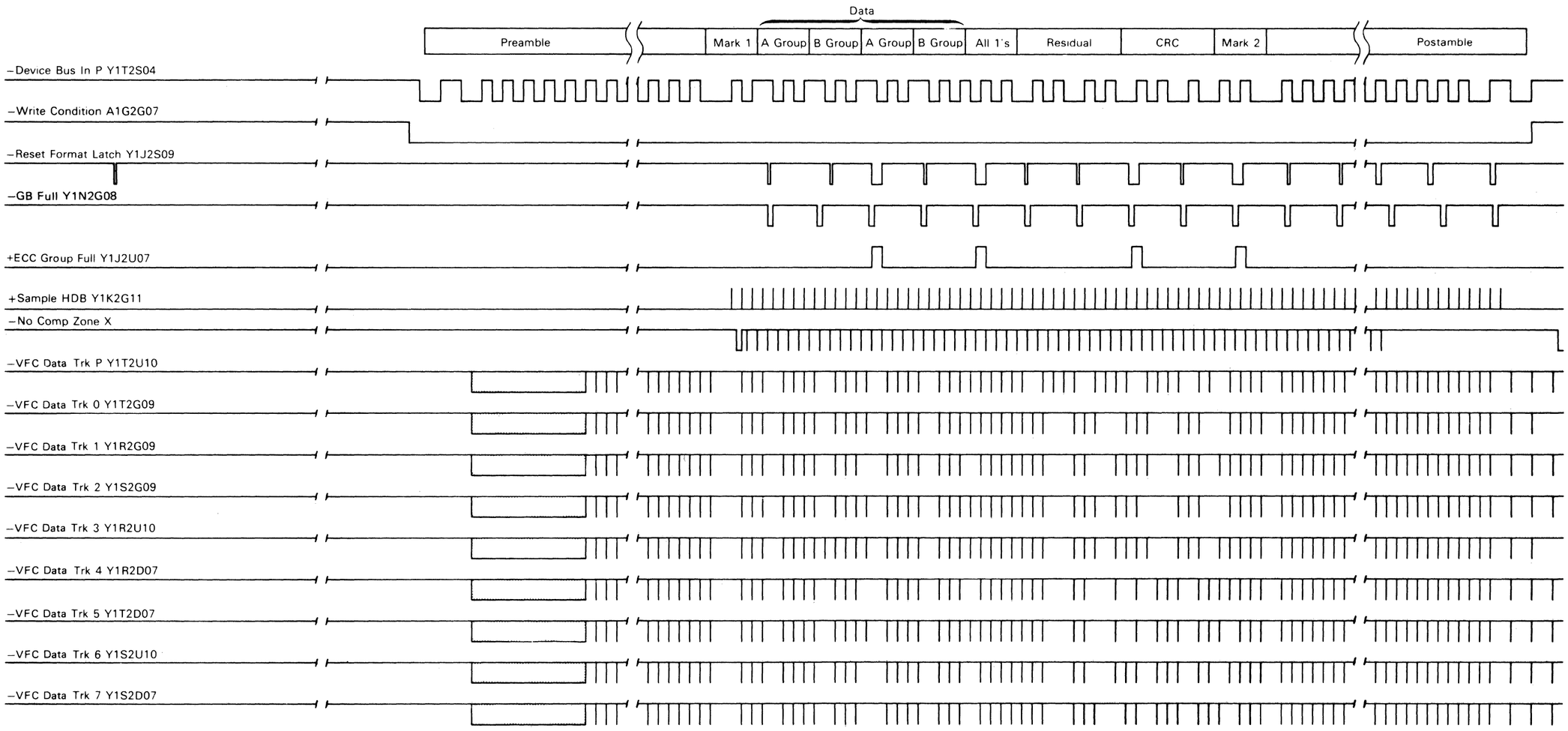
Seq	Condition/Instruction	Action
87	If not:	Change the bad zone: Zone 1 - Y1T2 Zone 2 - Y1S2 Zone 3 - Y1R2
88	Are any +DEAD TRACK REGISTERS set? See test point chart on 17-162.	Go to Seq 90.
89	If not:	Change the bad zone: Zone 1 - Y1T2 Zone 2 - Y1S2 Zone 3 - Y1R2
90	Check –RECORD TRACK X lines. Are any lines at solid level? See test point chart on 17-162.	Change in order: 1. Y1Q2 2. Y1P2
91	If not:	Change the bad zone: Zone 1 - Y1M2 Zone 2 - Y1L2 Zone 3 - Y1K2
92	Are any at a solid plus or solid minus level?	Change in order: 1. Y1Q2 2. Y1P2
93	Is –SAMPLE HDB (Y1N2D06) pulsing?	Change the bad zone: Zone 1 - Y1T2 Zone 2 - Y1S2 Zone 3 - Y1R2
94	Is –NO COMP P-5 (Y1M2D03) failing to pulse?	Change Y1M2.
95	Is –NO COMP 1-4 (Y1K2D03) failing to pulse?	Change Y1K2.
96	Is –NO COMP 2-7 (Y1L2D03) failing to pulse?	Change Y1L2.
97	If not:	Change Y1N2.

TEST POINT CHART FOR SKEW ERRORS

ALL CARDS ARE IN THE Y1 PANEL UNLESS OTHERWISE NOTED	ZONE 1			ZONE 2			ZONE 3		
	P	0	5	2	6	7	1	3	4
–DEVICE BUS IN TO DF	T2S04	T2M04	T2D13	S2M04	S2S04	S2D13	R2M04	R2S04	R2D13
–SYNC TRK X	P2J06	P2D02	P2U02	P2U13	P2D05	P2J03	P2S04	P2M08	P2P12
–VFC DATA	T2U10	T2G09	T2D07	S2G09	S2U10	S2D07	R2G09	R2U10	R2D07
–VFC PRIME DATA	T2U13	T2G08	T2B05	S2G08	S2U13	S2B05	R2G08	R2U13	R2B05
+STEP RIC	T2U12	T2M02	T2D12	S2M02	S2U12	S2D12	R2M02	R2U12	R2D12
+RIC RESET	M2P10	M2U13	M2U07	L2P10	L2U13	L2U07	K2P10	K2U13	K2U07
–POINTER BUS	G2P10	G2B12	G2M08	G2D13	G2M05	G2M07	G2M02	G2P02	G2P05
–ALMOST SKEW	G2P09	G2J13	G2P07	G2G12	G2P03	G2P06	G2B13	G2G04	G2P04
–NO COMP	M2D03			L2D03			K2D03		
–RECORD TRACK X	P2P04	P2P11	P2U05	P2U10	P2D07	P2D11	P2S05	P2G11	P2U09
+PE WRITE SKEW	M2M09	M2P07	M2P04	L2M09	L2P07	L2P04	K2M09	K2P07	K2P04
+DEAD TRACK REGISTER	P2G03	P2B05	P2U03	P2U11	P2B02	P2D04	P2S09	P2S13	P2M09
–BUS IN (from primary device interface) (*A2 PANEL) (See Note)	*D2S07	*D2M05	*D2G10	*D2J06	*D2M10	*D2D06	*D2J09	*D2G12	*D2G08
–BUS IN (from secondary device interface) (*A2 PANEL)	*D2M03	*D2P05	*D2P04	*D2P10	*D2J12	*D2B04	*D2D10	*D2M12	*D2D04
–TIME SENSE X	Y1T2 U05	Y1T2 M03	Y1T2 D10	Y1S2 M03	Y1S2 U05	Y1S2 D10	Y1R2 M03	Y1R2 U05	Y1R2 D10
–IBG BRANCH	P2M07								
+SOME TRACKS MARG ZN 1	M2S02								
+EXCESSIVE SKEW (DOT OR)	M2P13								
–WRT AND TAPE OP	N2J09								
–ROC CYCLED	G2P11								
–GATED PGM SYNC	G2M11								
+PE WRT SKEW (DOT OR)	M2P06								
+WRT SKEW ERROR	N2B12								
+6250 BPI WRT SKEW (DOT OR)	M2M04								
+NRZI WRT SKEW (DOT OR)	C2J04								

Note: Scope these same pins if the tape control has selection logic.





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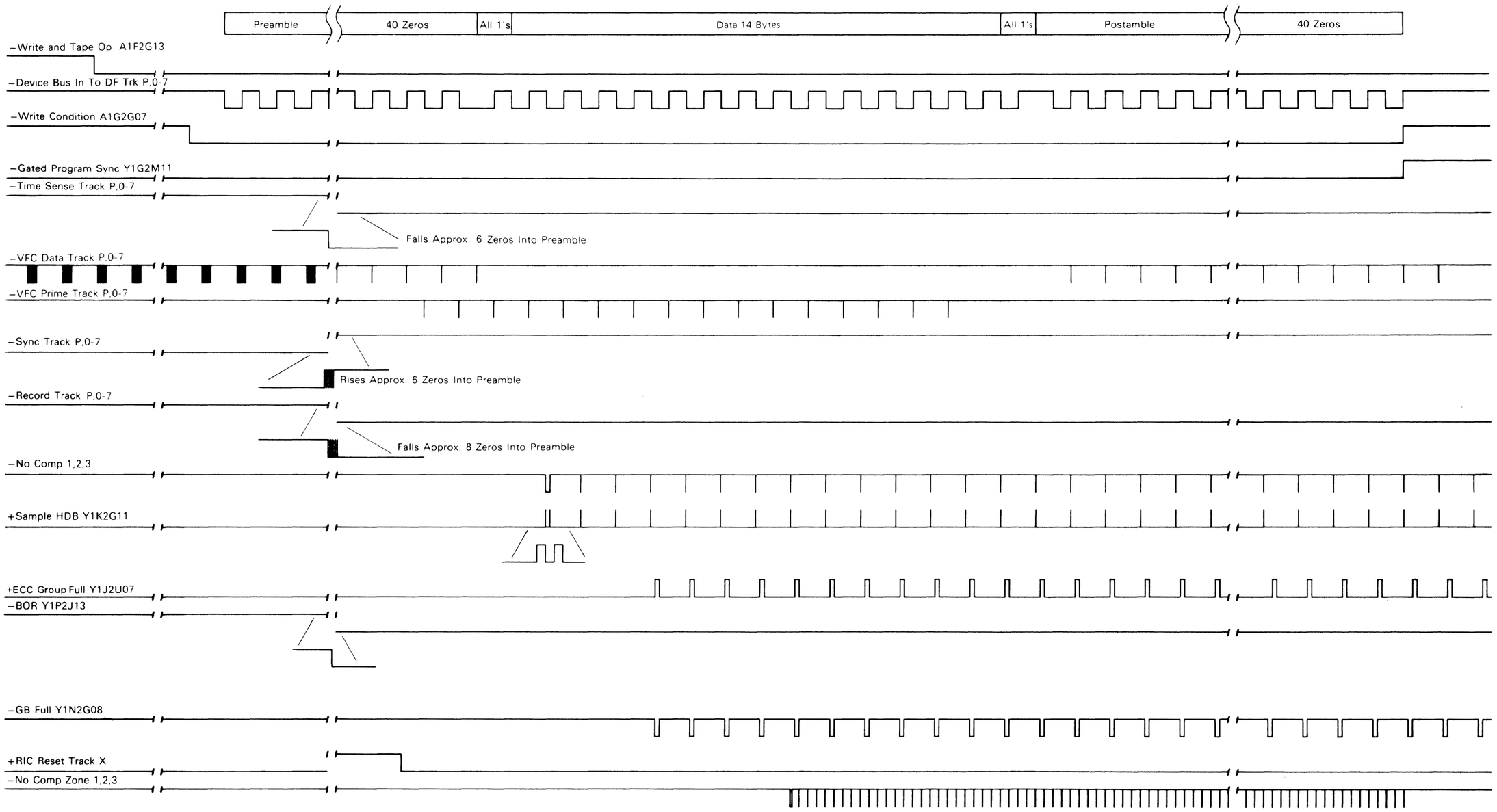
PE WRITE TIMING CHART



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XF3300 Seq 1 of 2	2735929 Part Number	See EC History	845958 1 Sep 79					

SKEW ERROR

Sense byte 3, bit 2 is set when excessive skew (any RIC is equal to the ROC), is detected during a PE Write, PE Read or Read Backward, 6250 BPI Read or Write, or a NRZI Write operation.

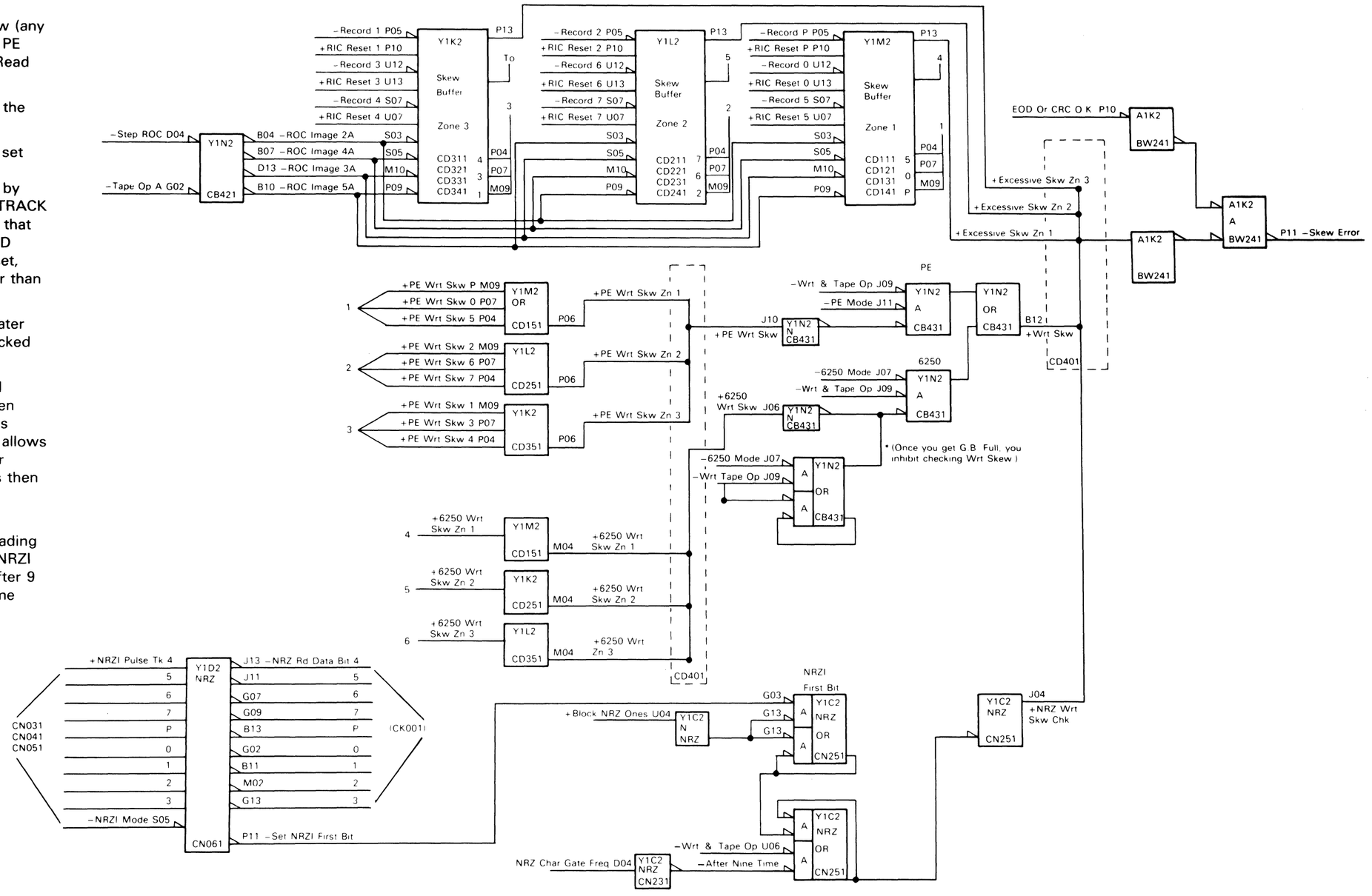
A. PE Write - skew is set if the RIC exceeds the ROC by four counts on any track.

B. PE Read or Read Backward - skew is not set under normal condition. Almost skew is recognized when RIC is greater than ROC by 14 counts. This condition sets the DEAD TRACK register which does not recognize RIC for that track and allows ROC to cycle. If the DEAD TRACK register recognizes RIC or is not set, skew error is then set when RIC is greater than ROC by 30 counts.

C. 6250 Write - skew is set when RIC is greater than ROC by 14 counts. Skew is only checked during the preamble.

D. 6250 Read - skew is not set under normal condtions. Almost skew is recognized when RIC is greater than ROC by 26 counts. This does not recognize RIC for that track and allows ROC to cycle. If the DEAD TRACK register recognizes RIC or is not set, skew error is then set when RIC is greater than ROC by 30 counts.

E. NRZI - skew is the time lapse between reading the first and last bit of a data byte. On a NRZI Write, skew is set when first bit comes after 9 time (about 28% of the total bit period time clapsed).



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XF3300 Seq 2 of 2	2735929 Part Number	See EC History	845958 1 Sep 79					

From 14-000, 17-010, 17-410

ERROR DESCRIPTION:
Sense Byte 3, Bit 0 is set:

1. During a 6250 bpi Read operation, when two track error pointers are not set and the ECC (Error Correction Code) cannot find the track to correct.
2. During a 6250 bpi Write operation, when the hardware error pointer and the ECC do not point to the same track on a single track error.
3. During a PE operation, when a VRC (Vertical Redundancy Check) is detected without dead track or pointer information.
4. During a NRZI Read or Read Backward operation, when a VRC that cannot be corrected occurred.

The VRCR (Vertical Redundancy Check Register) is an error detection circuit that checks the vertical parity (across the width of the tape) of each byte.

Most Probable Causes:
The following list of cards can cause the problems covered in in this procedure. The cards are listed with the highest probability first. Lines with multiple cards have the same probability. Cards separated by slashes are interchangeable.

Control Unit

A. Y1F2
B. **Y1K2**/Y1L2/Y1M2
C. Y1J2
D. Y1N2
E. A1F2
F. Y1R2/Y1S2/Y1T2
G. Y1H2
H. Y1G2, Y1C2, Y1P2
I. A1K2, Y1D2, A1C2, A1G2
J. A1E2, A1H2, A1L2, A2Q2, A2T2, Y1Q2
K. A2R2 (NRZI)

Single Tape Unit

A. Erase head
B. Read card

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise.
Remember to END all problems or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Is this a single tape unit failure?	For Models (4, 6, 8), go to 5B-000. For Models (3, 5, 7), go to 5A-000.
1A	Can the tape control read a prewritten tape forward and backward without a VRC error? Use Read Only tape (first seven files only).	Go to Seq 31.
2	Does the tape control fail only on the Read Backward command?	Go to Seq 88.
3	Does the tape control fail only on the Read Forward command?	Go to Seq 83.
4	Does the tape control fail only in PE mode?	Go to Seq 37.
5	Does the tape control fail only in NRZI mode?	Go to 17-310.
6	Do a LWR (8B) with gaps with tape away from load point or a Write operation (01) in 6250 bpi mode (byte count of 0B0) at the CE panel. Write data FF0. For gaps, jumper A1S2G08 to ground.	
7	Does the tape control run without a VRC error?	Change Y1J2.
8	Is −PE2 SLD (Y1Q2G03) at +6 volts?	Go to Seq 11.
9	Is +PE MODE (A1K2U11) minus?	Change Y1Q2.
10	If not:	Go to Seq 111.
11	Is +SET R/W VRC ERROR (Y1J2U09) always plus and not pulsing? (A plus 100 ns pulse is a normal set pulse.)	Change in order: 1. Y1J2 2. Y1C2.
12	Is +SET R/W VRC ERROR (Y1J2U09) always minus?	Change in order: 1. A1K2 2. Y1N2
13	Sync minus on −SET I CNT CMPR (Y1J2G03).	
14	Are there eight or more pulses in the first group of pulses on +SET I CNT (Y1F2U02)?	Go to Seq 16.
15	If not:	Go to Seq 22.
16	Does the last +SHIFT S2 (Y1J2J13) of the first group stay plus for a longer duration than the previous pulses (up to eight plus transitions) or are there more than eight plus transitions?	Go to Seq 107.
17	Is −WRITE OR READ FORWARD (Y1H2U07) plus?	Go to Seq 85.
18	Is +READ FORWARD (Y1J2D03) minus?	Change Y1J2.
19	Sync plus on −IBG BRANCH (Y1P2M07) (20 us/division).	
20	Is +SET XLT BUFFER (Y1N2G04) bad? Should be 26 groups of four pulses followed by a large group of pulses (approximately 150) when using LWR with gaps and a byte count of 0B0.	Go to Seq 74.
21	If not:	Go to Seq 62.
22	Is there only one pulse on −SET I CNT COMPARE (Y1J2G03)?	Go to Seq 27.
23	Adjust time base on the scope so all pulses on −COUNT EQUAL I (Y1F2S03) can be seen for one record. Place the scope on X10 magnifier and look at the second minus transition.	
24	Does −COUNT EQUAL I (Y1F2S03) fail to pulse?	Change Y1F2.
25	Does −COUNT EQUAL I (Y1F2S03) go minus when +SHIFT S2 (Y1J2J13) goes plus and stays plus?	Change Y1J2.
26	If not:	Go to Seq 16.
27	Sync plus on −IBG BRANCH (Y1P2M07).	
28	Are you getting −GB PTR for any track? (See Chart 1 on 17-171.)	Go to 17-700.
29	Are you getting −6250 bpi check for any track? (See Chart 2 on 17-171.)	Go to 17-700.
30	If not:	Change Y1J2.
31	Do a LWR (8B) with gaps with tape away from load point. Byte count 0B0. Write data FF0. For gaps, jumper A1S2G08 to ground.	
32	Sync plus on −IBG BRANCH (Y1P2M07).	
33	Is −ORC GATE (A1G2J07) good? (See timing chart on 17-023.)	Change A1G2.
34	Is −READ AND TAPE OP (A1F2J13) plus?	Change A1F2.
35	Is −STAT BIT 2 TO DF (A1K2U09) minus?	Change A2T2.
36	If not:	Change A1K2.
37	Do a LWR (8B) with gaps with the tape at load point, or a PE Mode Set (C3) followed by a Write (01) from the CE panel. Byte count 0B0. Write data 'FF0'. (LWR with gaps, jumper A1S2G08 to ground.)	
38	Sync minus on −WRITE CONDITION (A1G2G07) (50 ns per division).	
39	Is −PE2 SLD (Y1Q2G03) at +6 volts?	Change Y1Q2.
40	Is +SET R/W VRC (Y1J2U09) always plus (+100 ns pulse on error)?	Change in order: 1. Y1J2 2. Y1C2
41	Is +SET R/W VRC (Y1J2U09) always minus (+100 ns pulse on error)?	Change A1K2.
42	Is −CORRECT TRACK 8 ONLY (Y1J2M02) minus at time SET R/W VRC (Y1J2U09) is plus?	Change Y1J2.
43	Is −READ CYCLE (A1F2B05) bad? (See PE timing chart on 17-178-2.)	Change A1F2.
44	Is −FB DATA OR ALL ONES (Y1H2U09) good? (See PE timing chart on 17-178-2.)	Go to Seq 59.
45	Is +SAMPLE HDB (Y1K2G11) bad? (See PE timing chart on 17-177.)	Change Y1N2.
46	Is −ECC GB ADR 4 (Y1J2S03) bad? (See PE timing chart on 17-178-2.)	Change Y1J2.
47	Is +END OF DATA PWR (Y1H2M09) bad? (Goes plus approximately 550 ns after end one on DEVICE BUS IN TO DF.)	Go to Seq 53.
48	Is −GB ADR CTR 1 (Y1K2J06) bad? (See PE timing chart on 17-177.)	Change Y1N2.
49	Is −GB ADR CTR 2 (Y1N2G07) bad? (See PE timing chart on 17-177.)	Change Y1N2.

READ/WRITE VERTICAL REDUNDANCY CHECK (VRC) (Cont'd)

Seq	Condition/Instruction	Action
50	Is –ECC GB ADR 1 (Y1J2U10) bad? (See PE timing chart on 17-178-2.)	Change Y1J2.
51	Is –ECC GB ADR 2 (Y1J2S11) bad? (See PE timing chart on 17-178-2.)	Change Y1J2.
52	If not:	Go to Seq 66.
53	Scope –FORMAT CHAR TRK x. (See Chart 7 on 17-171 and PE timing chart on 17-176.)	
54	Does one or more fail to pulse?	Go to Seq 56.
55	If not:	Change Y1H2.
56	Scope +DEVICE BUS IN to DF (see Chart 6 on 17-171 and PE timing chart on 17-176.)	
57	Is one or more bad?	Change bad card per Chart 6.
58	If not:	Change bad card per Chart 7 on 17-171 and Seq 53.
59	Is –XOUTA BIT 1 ALU2 to DF (A2Q2G09) plus?	Change A2Q2.
60	Is –STAT BIT 1 START WR RD (A2Q2B03) plus?	Change A2Q2.
61	If not:	Change Y1H2.
62	Scope –XLATE BFR TK test points (see Chart 4 on 17-171 and 6250 timing chart on 17-174).	
63	Is data from –ZLATE BFR TK good?	Go to Seq 81.
64	Is data from –XLATOR BUFFER OUT bad in more than one track?	Go to Seq 107.
65	If not:	Change bad Xlator buffer card per Chart 4.
66	Scope –SR2 REG test points (Chart 5 on 17-171). All bit lines should be plus.	
67	Are all bits bad?	Go to Seq 69.
68	If not:	Change Y1F2.
69	Scope –RESET S1 AND S2 (Y1J2S07). Is this line pulsing?	Change Y1F2.
70	If not:	Change Y1F2.
71	Is +SAMPLE HDB (Y1K2G11) bad? (See PE timing chart on 17-177.)	Change Y1N2.
72	Is +GT ROC ADDR TO HDB (Y1N2D09) bad? (See timing chart on 17-173.)	Change Y1N2.
73	If not:	Change Y1N2.
74	Is +ECC GROUP FULL (Y1J2U07) good? (Should be only four plus pulses during data time.)	Change Y1N2.
75	Scope and compare –VFC DATA for all tracks (Chart 3).	
76	Are any tracks bad?	Change bad card per Chart 3.
77	Scope +EOD OR PE (Y1H2P04). Is it bad? (Should go plus before –IBG (Y1P2M07).)	Go to Seq 79.
78	If not:	Go to Seq 62.
79	Is +RESET VOTE LATCHES (Y1J2U13) good? Check from –IBG to –IBG (see 6250 timing chart on 17-173).	Go to Seq 71.
80	If not:	Go to Seq 96.
81	Scope –SR2 BITS (Chart 5). Are any bits bad?	Go to Seq 92.
82	If not:	Go to Seq 102.
83	Do a READ FORWARD command. Is +READ FWD (Y1J2D03) plus?	Change Y1F2.
84	Is –WRITE OR READ FORWARD (Y1J2M12) minus?	Change Y1J2.
85	Is –XOUTA BIT 1 ALU2 TO DF (Y1H2M12) plus?	Change A2Q2.
86	Is –STAT BIT 1 START WR RD (Y1H2P12) plus?	Change A2Q2.
87	If not:	Change Y1H2.
88	Do a READ BACKWARD (0C) command.	
89	Is +READ FORWARD (Y1J2D03) minus?	Change Y1F2.
90	Is –WR OR RD FWD (Y1J2M12) plus?	Change Y1J2.
91	If not:	Change Y1H2.
92	Are all SR2 bits bad?	Go to Seq 94.
93	If not:	Change bad card per Chart 5.
94	Is –RESET S1 AND S2 (Y1J2S07) pulsing?	Change Y1F2.
95	If not:	Change Y1F2.
96	Does +A3 or B3 (Y1J2B10) fail to pulse?	Change Y1J2.
97	Does +A1 or B1 (Y1J2B07) fail to pulse?	Change Y1J2.
98	Is +SAMPLE HDB (Y1K2G11) bad? (See 6250 timing chart on 17-175.)	Change Y1N2.
99	Is +GT ROC ADDR TO HDB (Y1N2D07) bad? (See 6250 timing chart on 17-173.)	Change in order: 1. Y1N2 2. Y1K2
100	Is +RESET VOTE LATCHES (Y1J2U13) pulsing?	Change in order: 1. Y1J2 2. Y1P2
101	If not:	Change in order: 1. Y1P2 2. Y1J2
102	Scope –FORMAT CHAR TRK x (See Chart 7 this page and 6250 timing chart on 17-175.)	
103	Are any FORMAT CHAR TRKS bad?	Go to Seq 105.
104	If not:	Change Y1N2.
105	Is more than one FORMAT CHAR TRK bad?	Change Y1N2.
106	If not:	Change bad card per Chart 7.
107	Is –ECC GB ADR 1 (Y1J2U10) bad? (See 6250 timing chart on 17-172.)	Change Y1J2.
108	Is –ECC GB ADR 2 (Y1J2S11) bad? (See 6250 timing chart on 17-172.)	Change Y1J2.
109	Is –ECC GB ADR 4 (Y1J2S03) bad? (See 6250 timing chart on 17-172.)	Change Y1J2.
110	If not:	Go to Seq 74.
111	Is +COMBINED R/W VRC ERROR (Y1N2P13) solid minus?	Change A1K2.
112	Is +SET R/W VRC (DOT OR) (Y1J2U09) solid minus?	Change Y1N2.
113	If not:	Change Y1C2.

READ/WRITE VERTICAL REDUNDANCY CHECK (Cont'd)

Chart 1

–GB PTR	
TRACK	TEST POINT
P	Y1M2G12
0	Y1M2J12
1	Y1K2G12
2	Y1L2G12
3	Y1K2J12
4	Y1K2J11
5	Y1M2J11
6	Y1L2J12
7	Y1L2J11

Chart 2

–6250 BPI	
TRACK	TEST POINT
P	Y1H2J02
0	Y1H2J03
1	Y1H2J04
2	Y1H2M07
3	Y1H2M03
4	Y1H2G10
5	Y1H2J11
6	Y1H2D12
7	Y1H2D13

Chart 3

–VFC DATA	
P	Y1T2U10
0	Y1T2G09
1	Y1R2G09
2	Y1S2G09
3	Y1R2U10
4	Y1R2D07
5	Y1T2D07
6	Y1S2U10
7	Y1S2D07

Chart 4

XLATOR BFR TK	
Bit	XLATOR Buffer Card and Pin
P	Y1M2G02
0	Y1M2B13
1	Y1K2G02
2	Y1L2G02
3	Y1K2B13
4	Y1K2D13
5	Y1M2D13
6	Y1L2B13
7	Y1L2D13

–SR2 REG	
CARD Y1F2	
BIT	PINS
P	None
0	G02
1	G05
2	G08
3	G11
4	G07
5	G09
6	G10
7	G12

Chart 6

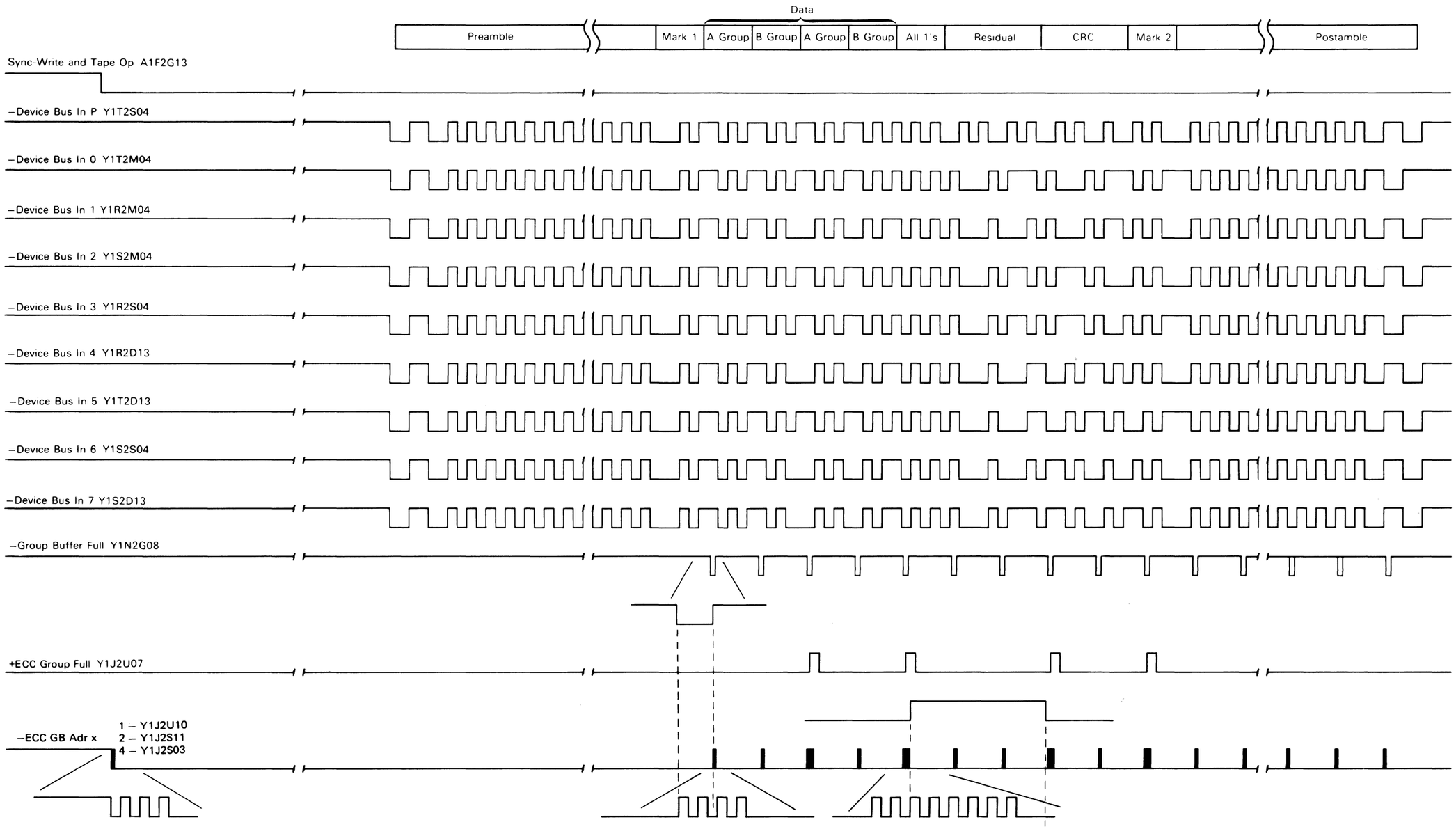
–DEVICE BUS IN TO DF	
BIT	TEST POINT
P	Y1T2S04
0	Y1T2M04
1	Y1R2M04
2	Y1S2M04
3	Y1R2S04
4	Y1R2D13
5	Y1T2D13
6	Y1S2S04
7	Y1S2D13

Chart 7

–FORMAT CHAR	
TRK	TEST POINT
P or 8	Y1M2G07
0	Y1M2M07
1	Y1K2G07
2	Y1L2G07
3	Y1K2M07
4	Y1K2M03
5	Y1M2M03
6	Y1L2M07
7	Y1L2M03

NOTES:

6250 TIMING CHART



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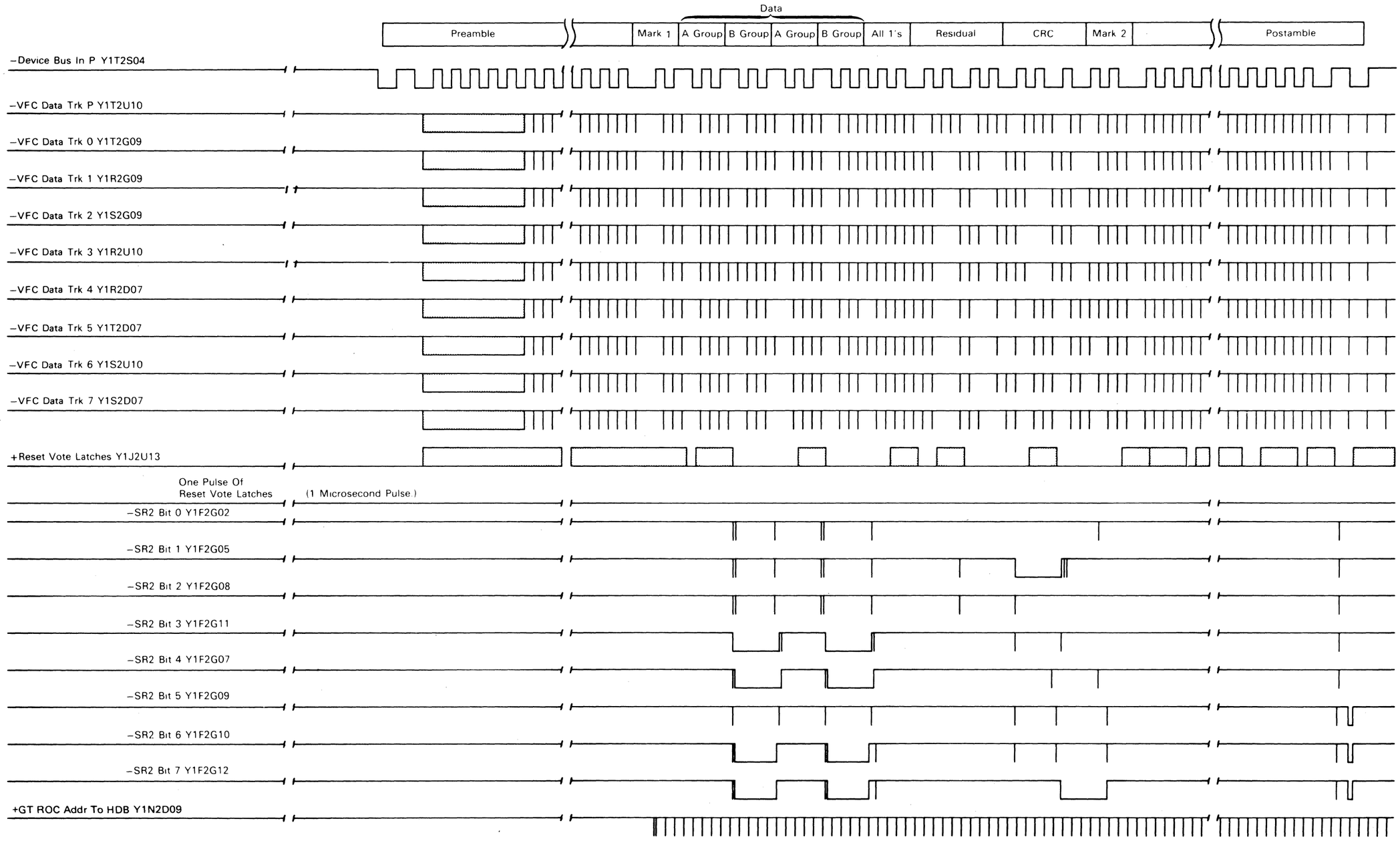
XF3500 Seq 1 of 2	**2735931** Part Number	**See EC History**	**845958** 1 Sep 79					



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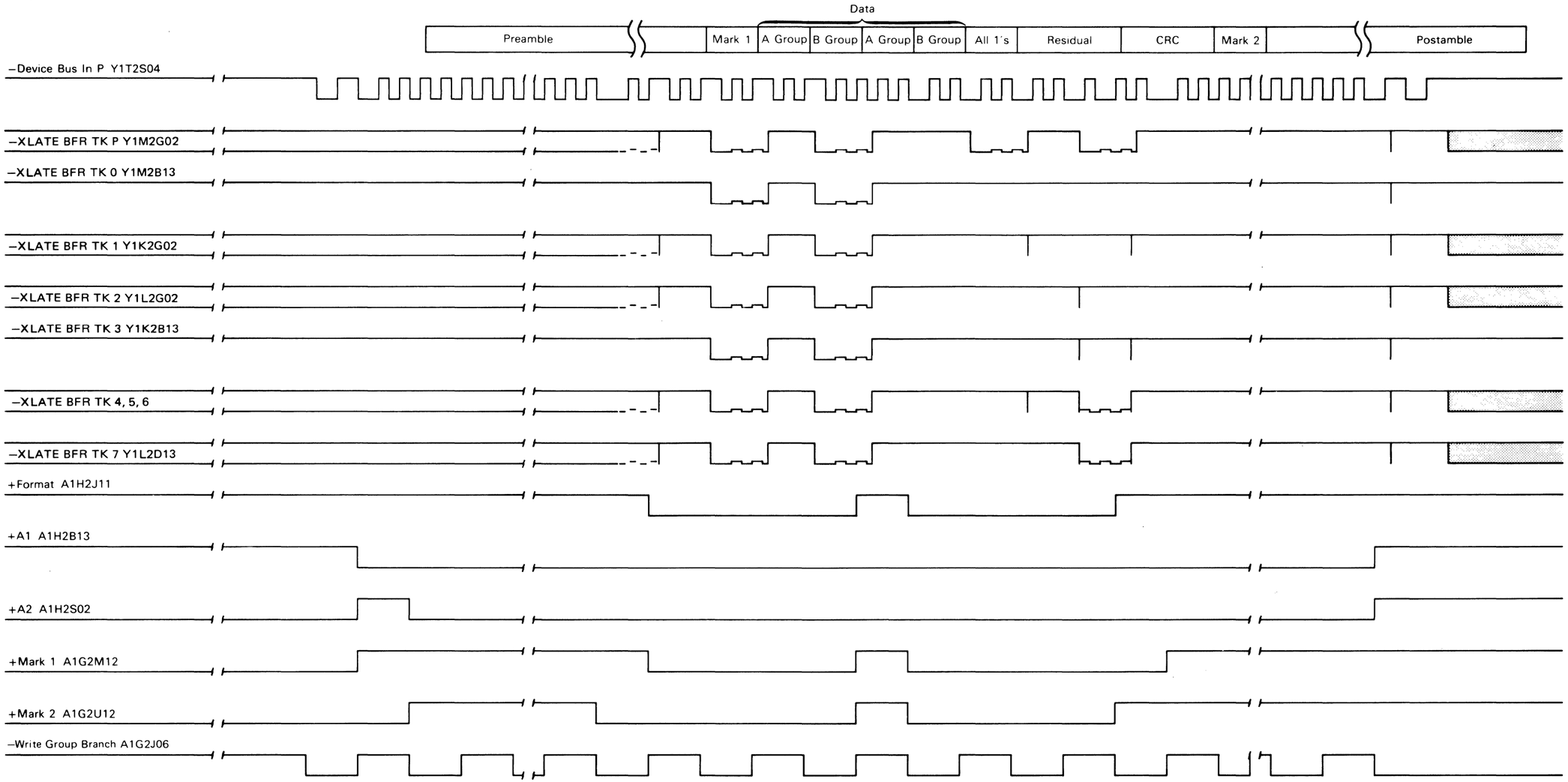
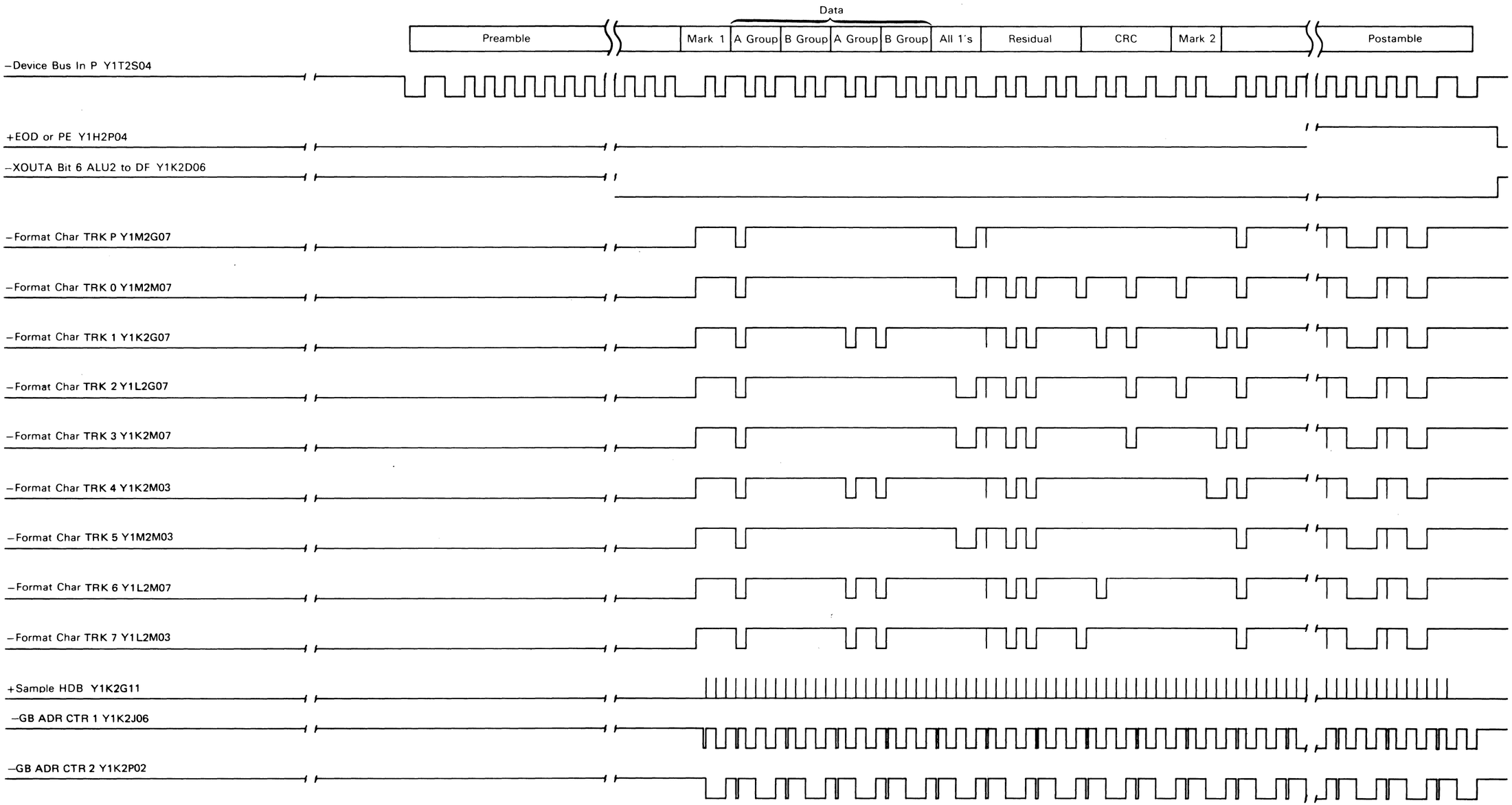
XF3500 Seq 2 of 2	2735931 Part Number	**See EC History**	**845958** 1 Sep 79					





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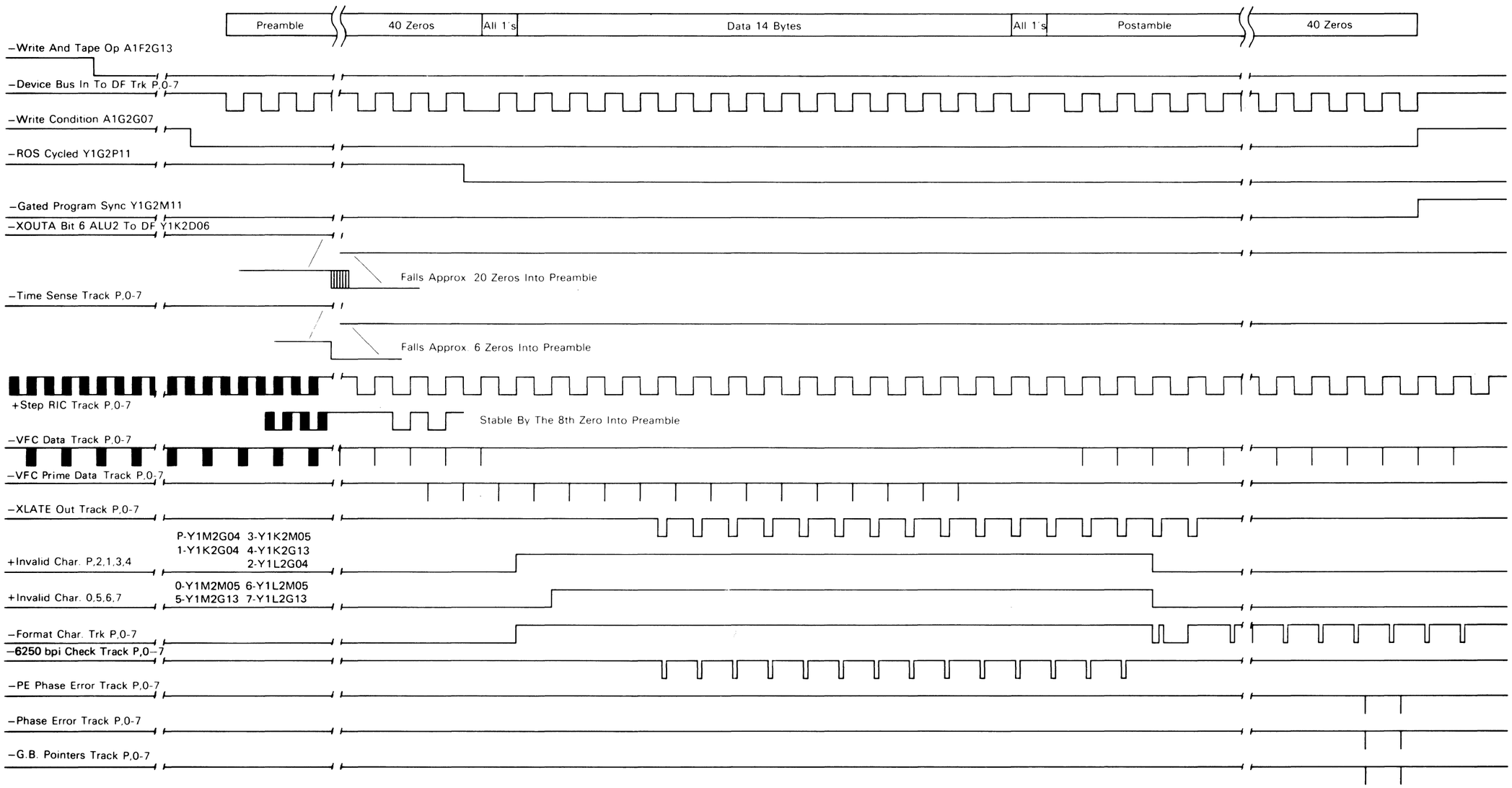
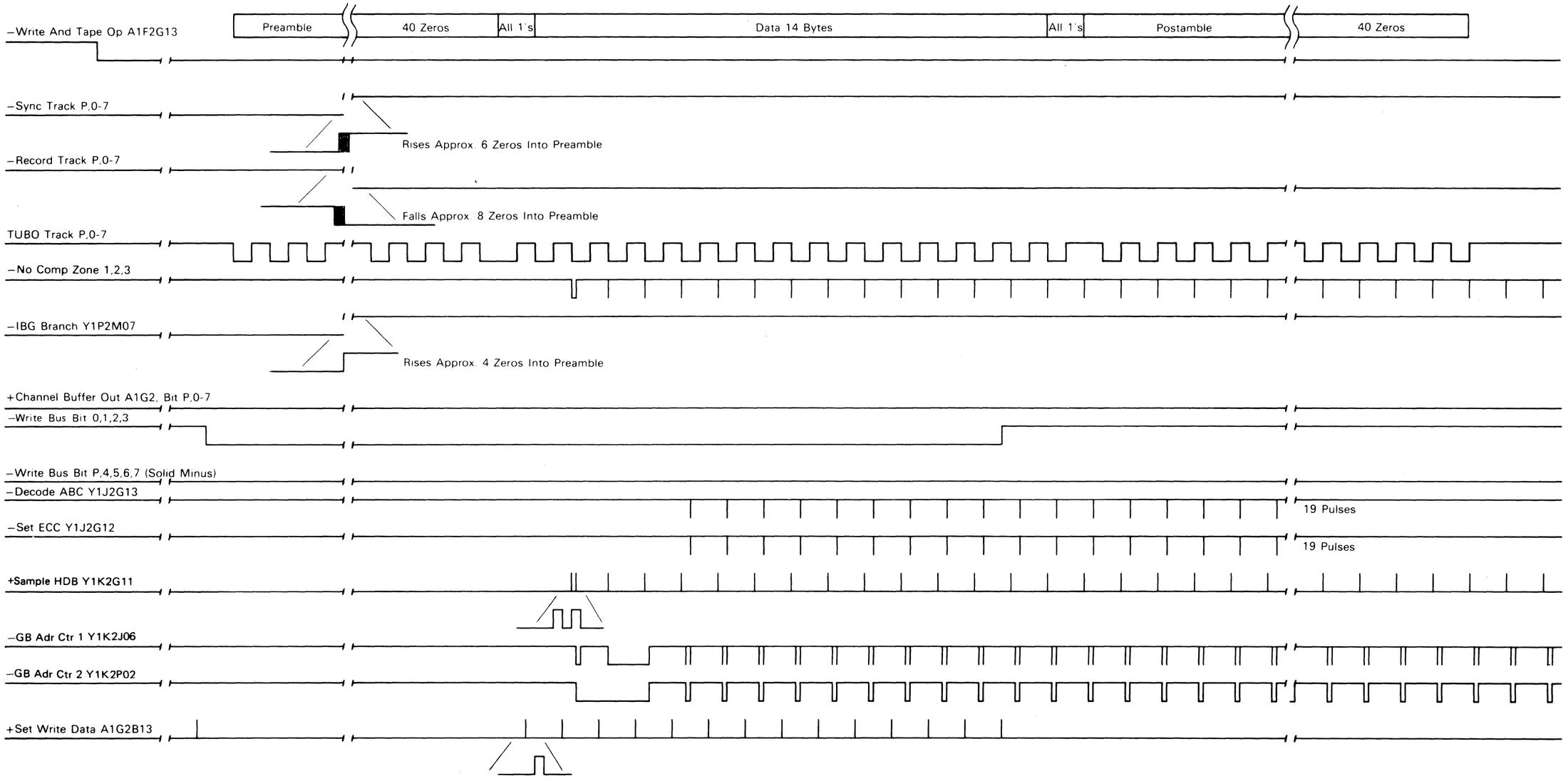
XF3600 Seq 2 of 2	2735932 Part Number	See EC History	845958 1 Sep 79					

PE TIMING CHART





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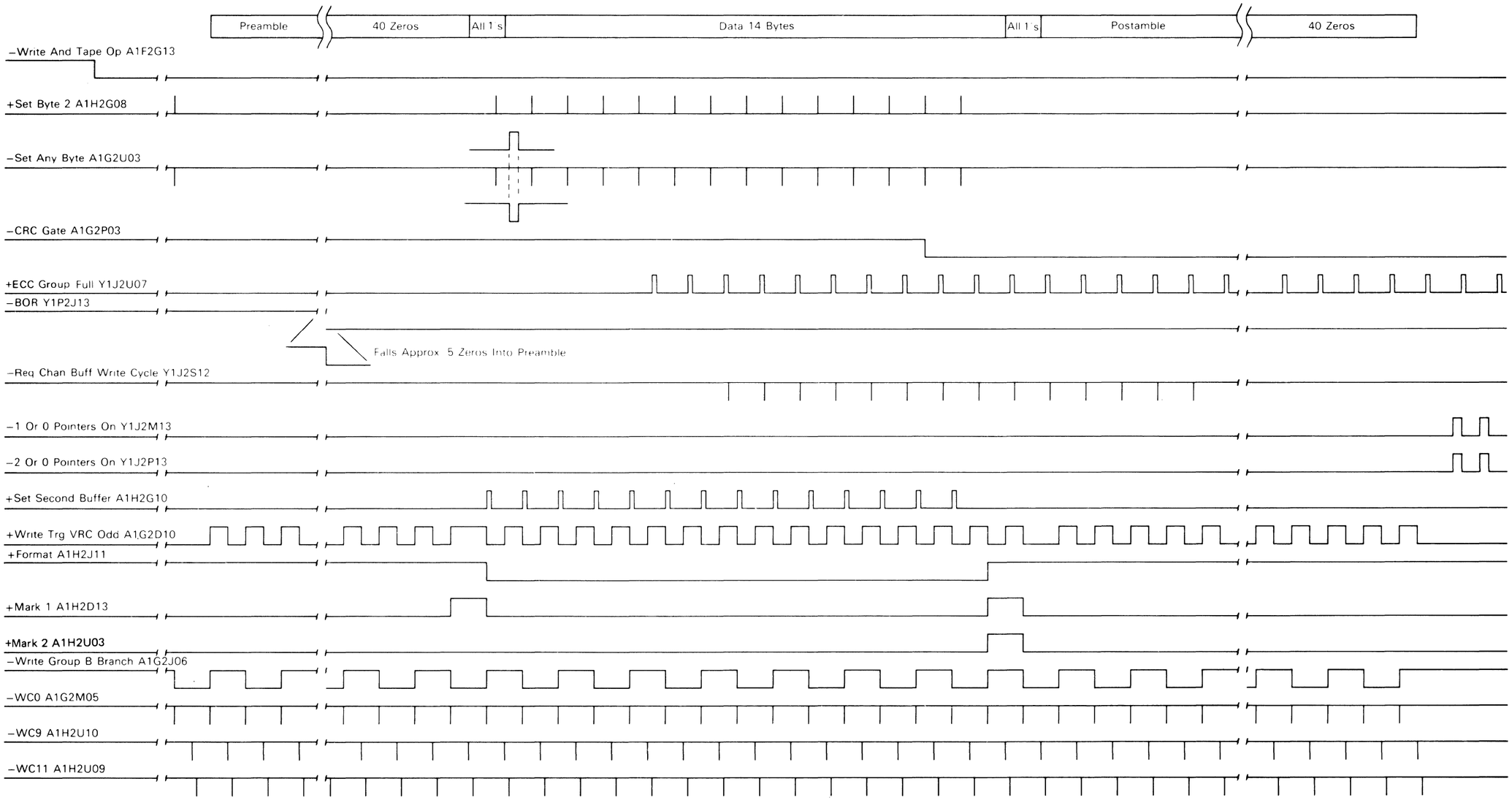
XF3700 Seq 2 of 2	**2735933** Part Number	**See EC History**	**845958** 1 Sep 79					

PE TIMING CHART (Cont'd)



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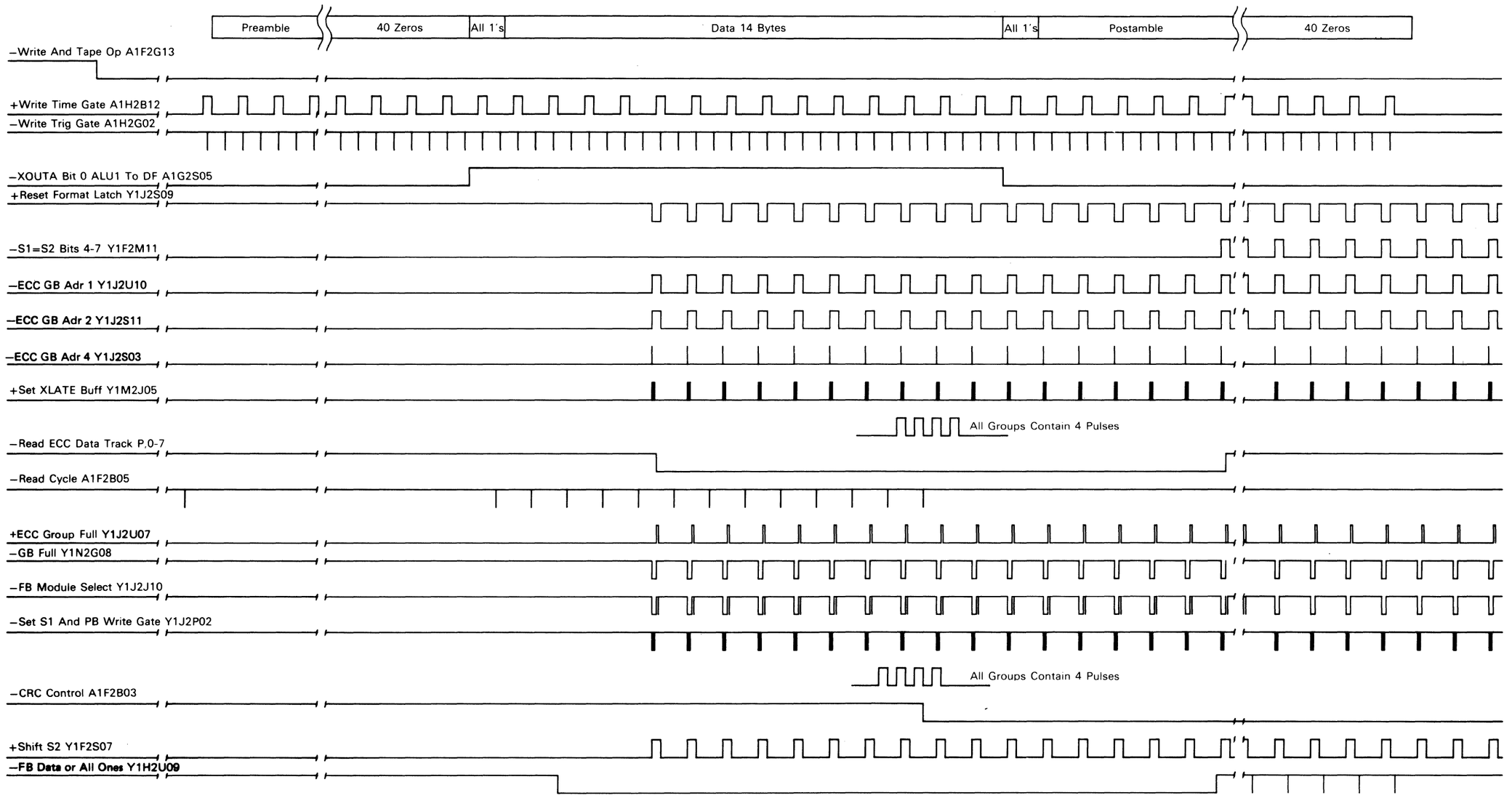
XF3800 Seq 1 of 2	**2735934** Part Number	**See EC History**	**845958** 1 Sep 79					



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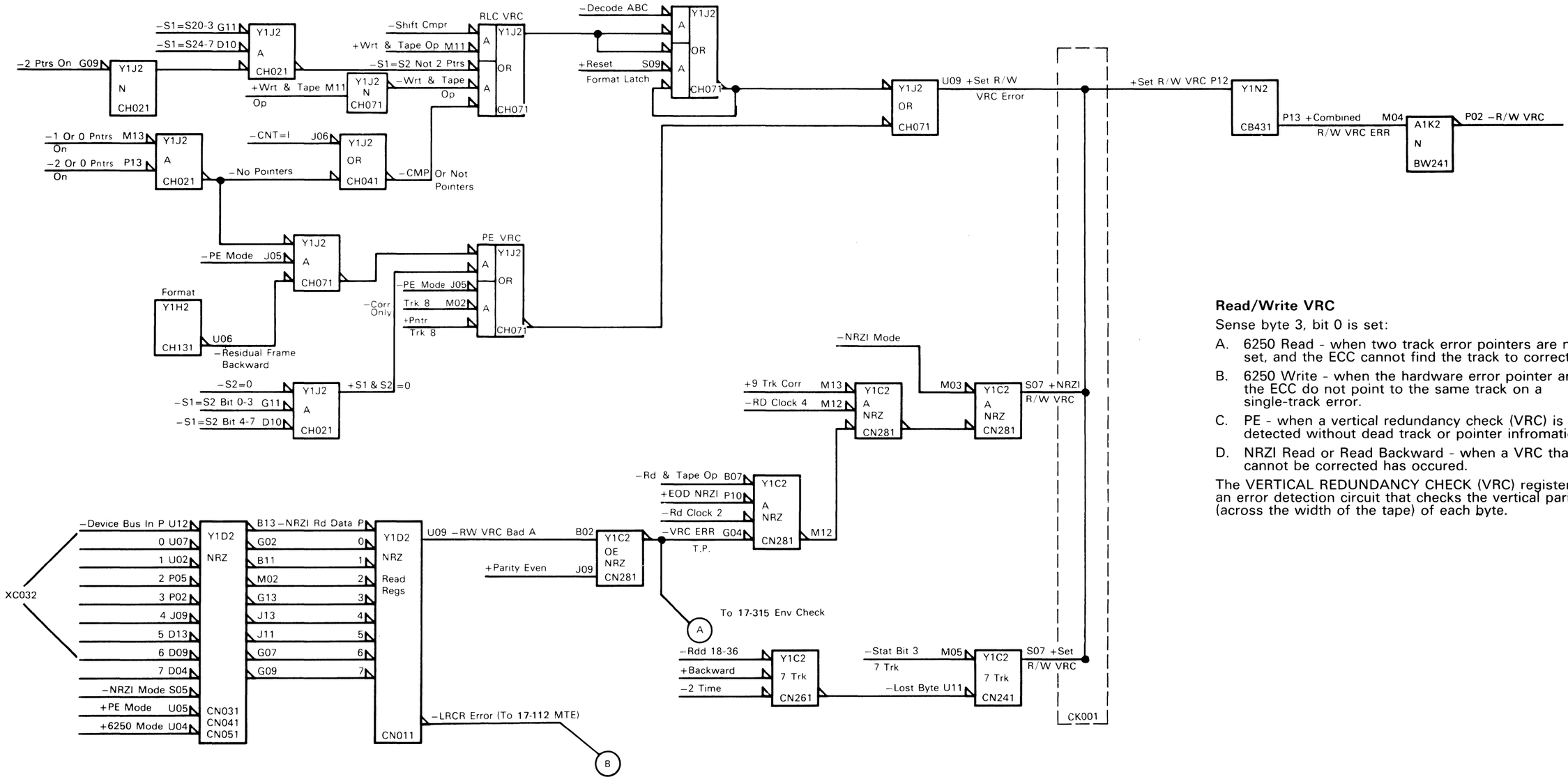
XF3800 Seq 2 of 2	2735934 Part Number	See EC History	845958 1 Sep 79					



Read/Write VRC

Sense byte 3, bit 0 is set:

A. 6250 Read - when two track error pointers are not set, and the ECC cannot find the track to correct.

B. 6250 Write - when the hardware error pointer and the ECC do not point to the same track on a single-track error.

C. PE - when a vertical redundancy check (VRC) is detected without dead track or pointer infromation.

D. NRZI Read or Read Backward - when a VRC that cannot be corrected has occured.

The VERTICAL REDUNDANCY CHECK (VRC) register is an error detection circuit that checks the vertical parity (across the width of the tape) of each byte.

From 14-000

ERROR DESCRIPTION:
Sense Byte 5, Bit 2 is set when tape mark is not written properly. This bit is also set if any byte fails to activate TAPE MARK (TM) DETECTED during the time when ROS2 does a readback check of 35 consecutive tape mark bytes.

MOST PROBABLE CAUSES:
The following list of cards can cause the problems covered in this procedure. The cards are listed with the highest probability first. Lines with multiple cards have the same probability. Cards separated by slashes are interchangeable.

A. Y1R2/Y1S2/Y1T2
B. A1G2, A1H2, A1K2, A2Q2, Y1C2, Y1P2

ADDITIONAL CARDS AFFECTED:

A. A2D2
B. A2E2
C. A2L2
D. A2T2
E. B2E2
F. A2R2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise
Remember to END all problems or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Is this a single tape unit failure?	For Models 4, 6, 8, go to 5B-000. For Models 3, 5, 7, go to 5A-000.
1A	Does the failure occur while operating in NRZI Mode (Sense Byte 6, Bit 0 ON or Sense Byte 6, bit 4 OFF and Bit 3 ON)?	Go to Seq 31.
2	Sync negative on –TAPE OP A (A1K2B10). Does +TM CONFIGURATION (A2D2S10) become plus while the sync is minus in a WTM (1F) operation?	Change A2D2.
3	The following lines should become minus during the sync, except for 1, 3, and 4 on a Write Tape Mark operation. Are they all good? **Zone 1** –TIME SENSE P Y1P2P03 –TIME SENSE 0 Y1P2P09 –TIME SENSE TK 5 Y1P2D10 **Zone 2** –TIME SENSE 2 Y1P2G13 –TIME SENSE 6 Y1P2M12 –TIME SENSE TK 7 Y1P2G12 **Zone 3** –TIME SENSE 1 Y1P2P02 –TIME SENSE 3 Y1P2P10 –TIME SENSE TK 4 Y1P2S12	Change Y1P2.
4	The following lines should pulse during the sync, except for 1, 3, and 4 on a Write Tape Mark operation. Are they all good? **Zone 1** –DEVICE BUS IN 0 TO DF Y1T2M04 –DEVICE BUS IN P TO DF Y1T2S04 –DEVICE BUS IN 5 TO DF Y1T2D13 **Zone 2** –DEVICE BUS IN 2 TO DF Y1S2M04 –DEVICE BUS IN 6 TO DF Y1S2S04 –DEVICE BUS IN 7 TO DF Y1S2D13 **Zone 3** –DEVICE BUS IN 1 TO DF Y1R2M04 –DEVICE BUS IN 3 TO DF Y1R2S04 –DEVICE BUS IN 4 TO DF Y1R2D13	Change the card in the zone that was bad in Seq 3. Zone 1, change Y1T2. Zone 2, change Y1S2. Zone 3, change Y1R2. These cards are interchangeable. If there were bad lines in more than one zone, change Y1Q2 first.
5	Do the same TAPE UNIT BUS OUT lines pulse as the DEVICE BUS IN TO DF lines (Seq 4) did during the sync? –TUBO BIT P A1H2U07 –TUBO BIT 0 A2R2S03 –TUBO BIT 1 A2R2B12 –TUBO BIT 2 A2R2D05 –TUBO BIT 3 A2R2G02 –TUBO BIT 4 A2R2B07 –TUBO BIT 5 A2R2B10 –TUBO BIT 6 A2R2G13 –TUBO BIT 7 A2R2S02	Go to Seq 14.
6	Is this a 1x8 machine?	Go to Seq 12.
7	Is the tape unit being used to troubleshoot the failure connected directly to the tape control you are using?	Go to Seq 10.
8	Check the following lines to see if they match the TUBO lines in Seq 5. Do they all match while the sync is minus? Voltage 0v to +5v –BUS OUT P PRIMARY A2E2J07 –BUS OUT 0 PRIMARY A2E2G09 –BUS OUT 1 PRIMARY A2E2D03 –BUS OUT 2 PRIMARY A2E2D04 –BUS OUT 3 PRIMARY A2E2B09 –BUS OUT 4 PRIMARY A2E2D09 –BUS OUT 5 PRIMARY A2E2P07 –BUS OUT 6 PRIMARY A2E2M09 –BUS OUT 7 PRIMARY A2E2P02	Go to 18 010.
9	If not:	Change A2E2.
10	Check the following lines to see if they match the TUBO lines in Seq 5. Do they all match while the sync is minus? Voltage 0v to +5v –BUS OUT P SECONDARY A2E2G07 –BUS OUT 0 SECONDARY A2E2G08 –BUS OUT 1 SECONDARY A2E2B03 –BUS OUT 2 SECONDARY A2E2B04 –BUS OUT 3 SECONDARY A2E2B12 –BUS OUT 4 SECONDARY A2E2D13 –BUS OUT 5 SECONDARY A2E2M07 –BUS OUT 6 SECONDARY A2E2M08 –BUS OUT 7 SECONDARY A2E2U11	Go to 18-010.
11	If not:	Change A2E2.
12	Check the following lines to see if they match the TUBO lines in Seq 5. Do they all match while the sync is minus? Voltage 0v to +5v –BUS OUT P A2E2G07 –BUS OUT 0 A2E2G08 –BUS OUT 1 A2E2B03 –BUS OUT 2 A2E2B04 –BUS OUT 3 A2E2B12 –BUS OUT 4 A2E2D13 –BUS OUT 5 A2E2M07 –BUS OUT 6 A2E2M08 –BUS OUT 7 A2E2U11	Go to 18-010.
13	If not:	Change A2E2.
14	Does –GATE WRITE (A1H2D03) become minus while the sync is minus?	Go to Seq 26.

Seq	Condition/Instruction	Action
15	Does +INHIBIT WRITE (A1G2S12) become plus while the sync is minus?	Go to Seq 21.
16	Does –STAT BIT 1 START WR RD (A1G2G05) become minus while the sync is minus?	Go to Seq 18.
17	If not:	Change in order: 1. A2Q2 2. A2L2
18	Does –WRITE AND TAPE OP (A1G2D03) become minus while the sync is minus?	Change A1G2.
19	Does –XOUTA BIT 5 ALU1 TO DF (A1K2U07) become minus while the sync is minus?	Change A1K2.
20	If not:	Change in order: 1. A2T2 2. B2E2
21	Is –NRZI MODE (A1K2D10) minus while the sync is minus?	Go to Seq 24
22	Does –XOUTA BIT 2 ALU2 TO DF (A1K2D13) become minus while the sync is minus?	Change in order: 1. A2Q2 2. A2L2
23	If not:	Change A1K2.
24	Is either –XOUTA BIT 4 ALU2 TO DF (A1K2D09) or –XOUTA BIT 0 ALU2 TO DF (A1K2S13) minus while the sync is minus?	Change A1K2.
25	If not:	Change in order: 1. A2Q2 2. A2L2
26	Is –GATE WRITE NOT TM (A1H2J06) ever minus while the sync is minus?	Go to Seq 29
27	Sync negative on –GATE WRITE (A1G2M10). Is –XOUTA BIT 2 ALU1 TO DF (A1H2G04) ever minus while the sync is minus?	Change in order: 1. A2T2 2. B2E2
28	If not:	Change A1H2.
29	Sync negative on –GATE WRITE (A1G2M10). Is –XOUTA BIT 3 ALU1 TO DF (A1G2B03) ever plus while the sync is minus?	Change in order: 1. A2T2 2. B2E2
30	If not:	Change A1G2.
31	Sync negative on –TAPE OP A (Y1C2J11). Is –NRZI MODE (Y1C2M03) minus while the sync is minus?	Go to Seq 34.
32	Are both –XOUTA BIT 4 ALU2 TO DF (A1K2D09) and –XOUTA BIT 0 ALU2 TO DF (A1K2S13) always plus while the sync is minus?	Change A1K2.
33	If not:	Change in order: 1. A2Q2 2. A2L2
34	Once +TM CONFIGURATION (A2D2S10) becomes plus, does it stay plus until the fall of the sync?	Change A2D2.
35	Is –NRZI TM (Y1C2D13) minus twice and only twice during the sync?	Go to Seq 44
36	Is +NRZI CHAR GATE (Y1C2J12) plus twice and only twice during the sync?	Go to Seq 46
37	Is –SET NRZI FIRST BIT (Y1C2G03) minus twice and only twice during the sync?	Change Y1C2.
38	Rewind the tape unit, then perform the following command sequence using all ones data. Mode Set — CB (or a 7-track mode set) Write — 01 Read Bkwd — 0C Read forward — 02 Turn the STOP ON DATA FLOW ERROR switch ON. Does a failure occur?	Take sense, then go to 14.000 to analyze it. Probable cause is Y1D2.
39	Reload the failing Write Tape Mark operation. Does +INHIBIT WRITE (A1G2S12) become plus while the sync is minus?	Change in order: 1. A2R2 2. A1G2
40	Is –STAT BIT 2 TO DF (A1K2U09) minus during the sync?	Go to Seq 42
41	If not:	Change in order: 1. A2T2 2. B2E2
42	Does –STAT BIT 1 START WR RD (A1K2B09) become minus while the sync is minus?	Change A1K2.
43	If not:	Change in order: 1. A2Q2 2. A2L2
44	Is +NRZI CHAR GATE (Y1C2J12) plus twice and only twice during the sync?	Change Y1C2.
45	If not:	Go to Seq 37.
46	Are you operating in 7-track mode?	Go to Seq 49.
47	Is –STAT BIT 3 7-TRACK (Y1D2J02) ever minus while the sync is minus?	Change in order: 1. A2Q2 2. A2L2
48	If not:	Change Y1D2.
49	Is –STAT BIT 3 7-TRACK (Y1D2J02) minus when +NRZI CHAR GATE (Y1C2J12) plus?	Change Y1D2.
50	If not:	Change in order: 1. A2T2 2. B2E2

POSTAMBLE ERROR

From 14-000

ERROR DESCRIPTION:
Sense Byte 5, Bit 6 is set when the interval from the reading of ending all ones until the IBG (Interblock Gap) is sensed is either too long or too short.

1. During a 6250 bpi Read operation, this bit is set when a 6250 bpi postamble contains more or less than eight consecutive groups of ones in at least six tracks.
2. During a PE Write operation, this bit is set when the postamble contains less than thirty or more than fifty bytes.
3. During a PE Read operation, this bit is set when the postamble contains more than 50 bytes.

Most Probable Causes:
The following list is of the known cards which can cause the problems covered in this procedure. The cards are listed with the highest probability first. Lines with multiple cards have the same probability.

A. Y1H2
B. A1D2, Y1Q2

ADDITIONAL CARDS AFFECTED:

A. A1H2
B. A1G2
C. Y1T2
D. Y1S2
E. Y1R2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise
Remember to END all problems or maintenance calls by going to MAP 00-030

Seq	Condition/Instruction	Action
1	Does the error occur on only one tape unit?	Check for noise on TUBI just before time sense dropout Go to 5A-000 for Models 3, 5, and 7 or 5B-000 for Models 4, 6, and 8
2	Does the error occur during 6250 bpi operation?	Change in order 1. A1H2 2. A1G2
3	Does the error occur during a Write operation?	Go to Seq 7
4	If not:	This is an Excessive Postamble error for a PE Read operation Go to Seq 5.
5	Is Sense Byte 3, Bit 3 (End Data Ck) ON?	This is a false End Data check. Go to 17-530.
6	Are there any bits OFF in the TIE Byte (Sense Byte 2)?	Tracks P, 0, or 5 OFF—change Y1T2. Tracks 2, 6, or 7 OFF—change Y1S2. Tracks 1, 3, or 4 OFF—change Y1R2.
7	Can other tapes be read without a Postamble error?	Go to Seq 9.
8	If not:	Go to Seq 4.
9	Is the +FORMAT line (A1H2J11) minus at the end of the 40 zeros?	Change A1H2.
10	If not:	Change A1G2.

ENVELOPE CHECK WITHOUT SKEW ERROR

From 14-000

ERROR DESCRIPTION:
Sense Byte 3, Bit 4 is set:

1. During a PE Write operation, when a phase error pointer is set because a phase shift is detected which exceeds the capabilities of the Variable Frequency Control (VFC) circuits on read back data from the tape unit. This bit also sets Data Check.
2. During a PE Read operation, when any two or more of the nine read head amplitude sensors detects a signal that is acceptable amplitude (dead track).

   Note: If a single dead track is detected, the track information is recovered by a parity check of the eight remaining tracks, and is not an error condition.
3. During a 6250 bpi Write operation, when any time sensor(s) become inactive. If time sensor(s) have become inactive, the microprogram routine which assembles and sends the sense bits from ALU2 and/or the tape unit to ALU1 sets Envelope Error. Data Check is not set.

Most Probable Causes:
The following list of cards can cause the problems covered in this procedure. The cards are listed with the highest probability first. Lines with multiple cards have the same probability. Cards separated by slashes are interchangeable.

Control Unit

A. Y1H2
B. Y1G2
C. Y1R2/Y1S2/Y1T2
D. Y1K2/Y1L2/Y1M2
E. Y1N2
F. A1K2, Y1C2, Y1F2, Y1J2, Y1D2

Single Tape Unit

A. Dirty head
B. T-A1J2
C. Read/Write head

ADDITIONAL CARD AFFECTED:

A. A2Q2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise.
Remember to END all problems or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Is this a single tape unit failure?	For Models (4, 6, 8), go to 5B-000 For Models (3, 5, 7), go to 5A-000
1A	Sync positive on –IBG BRANCH (Y1P2M07). Write all ones in the failing mode with the LWR or Write command. If the LWR command is used, ground pin A1S2G08. The LWR command sets PE mode if the tape is at load point. Write 14 bytes in 6250 bpi mode or eight bytes in PE mode. (See timing chart on 17-111.)	
2	Is the failure in NRZI mode? (See the Mode Chart on this page.)	Go to 17-310
3	Is the NRZI feature installed? (See Feature Chart on this page.)	Go to Seq 12
4	Is +SET PE WRT ENV CHECK (Y1J2U02) always plus?	Change Y1J2
5	Is one of the following lines plus during the record (see Timing Chart on 17-111): –1 OR 0 PNTRS ON (Y1J2M13), –2 or 0 PNTRS ON (Y1J2P13), or +POINTER TRACK 8 (Y1J2M04)?	Go to Seq 15
6	Is –PE MODE (Y1J2J05) plus?	Go to Seq 10
7	Is –NRZI MODE (Y1C2M03) minus?	Change A1K2.
8	Is +SET WRITE ENV CHK (Y1J2U02) plus?	Change in order 1. Y1J2 2. Y1C2
9	If not:	Change A1K2.
10	Is –XOUTA BIT 0 ALU2 TO DF (A1K2S13) minus?	Change A2Q2
11	If not:	Change A1K2
12	Remove Y1C2 and Y1D2.	
13	Does tape control run error-free with cards Y1C2 and Y1D2 removed?	Change Y1C2 and replug Y1D2
14	If not:	Replug Y1C2 and Y1D2 and go to Seq 4
15	Scope +POINTER TRK X (See the Pointer Probe List on 17-701.)	
16	Is one or more +POINTER TRK line(s) plus during the record?	Go to 17-700
17	If not	Change Y1F2

Feature Chart for Sense Byte 6

TU FEATURE	0	2	3	4
Models 4, 6, 8 Single Density			*	X
Models 4, 6, 8 Dual Density		X	*	X
Models 3, 5, 7 PE-Only Models 3, 5, 7 Dual Density		X	*	
Models 3, 5, 7 7-Track	X		*	

* Bit 3 will be OFF when operating at 1600 bpi, ON when operating at other densities.

Mode Chart for Sense Byte 6

TU FEATURE	MODE BITS			
	0	2	3	4
7 Track NRZI	X			
1600 bpi (Mod 4, 6, 8)		X		X
6250 bpi		*	X	X
1600 bpi (Mod 3, 5, 7)		*		
9 Track NRZI		X	X	

* Can be on or off. ON for Dual Density, OFF for single density.

LRCR ERRORS, SENSE BYTE 3 BITS 0, 1, or 4

From 14-000, 17-590, 17-110

Sense Byte 3, Bit 0 — 9-Track R/W VRC
Sense Byte 3, Bit 1 — 7-or 9-Track LRC
Sense Byte 3, Bit 4 — NRZI Hi-Clip VRC (Write Only) or 7-Track Lost Byte (Read or Write)

ERROR DESCRIPTION:

Longitudinal Redundancy Check (LRC) (Sense Byte 3, Bit 1) is set during 7- or 9-track NRZI operations when a block has an odd number of bits in any track.

The Longitudinal Redundancy Check Register (LRCR) is an error detection circuit that checks the longitudinal parity of each track in a block. The LRCR is used only when operating with 7 or 9-track NRZI tape units. The total number of bits in any track of a block should be even. If the total number of one bits in the track is even, the Write trigger for that track is OFF at Write Longitudinal Redundancy Check Byte (LRCB) time and no bit is written in the LRCB for that track. If the total number of one bits in the track is odd, the Write trigger for that track, which is ON at Write LRCB time, is reset to write a one bit in the LRCB.

Vertical Redundancy Check (VRC) (Sense Byte 3, Bit 0) is set:

1. During a 6250 bpi Read operation, when two track error pointers are not set and the Error Correction Code (ECC) cannot find the track to correct.
2. During a 6250 bpi Write operation, when the hardware error pointer and the ECC do not point to the same track on a single track error.
3. During a PE operation, when a VRC is detected without pointer information (single dead track).
4. During a NRZI Read or Read Backward operation, when a VRC occurred that cannot be corrected.

The VRC Register (VRCR) is an error detection circuit that checks the vertical parity (across the width of the tape) of each byte.

NRZI High Clip VRC (Sense Byte 3, Bit 4) is set during a NRZI Write or Write Tape Mark operation, when a byte has incorrect parity.

Most Probable Causes:
The cards are listed with the highest probability first. Lines with multiple cards have the same probability.

A. Y1D2 (Y1 location, see 19-001)
B. Y1C2 (7-Track only - A1E2, A1L2)

ADDITIONAL CARDS AFFECTED:

A. A1H2
B. A2D2
C. Y1K2
D. A1K2
E. A1L2
F. A1E2
G. A2Q2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise.
Remember to END all problems or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Write a 14-byte record of all ones in the failing mode. Sync scope negative on −SET NRZI FIRST BIT (Y1C2G03). Is the failing mode 7-track?	Go to Seq 54.
2	Does the error occur on only one tape unit?	Go to 5A-000 for Models 3, 5, and 7. Go to 5B-000 for Models 4, 6, and 8.
3	Is the error a Hi-Clip VRC (Byte 3, bit 4)?	Go to Seq 9.
4	Is the error an LRC alone (Byte 3, bit 1)?	Go to Seq 6.
5	Does a Read/Write VRC error occur (Byte 3, bit 0)?	Go to Seq 23.
6	Does the data on any track coming into the tape control have an odd number of bits? See the TUBI table for test points on 17-312.	Go to Seq 48.
7	Does the −RDD 169 line go minus after the LRC character? (See Y1D2J07 on ALD CN021.)	Change Y1D2.
8	If not:	Go to ALD CN021 and follow the −RDD 169 line back to the failing point.
9	Is the unit failing during a Read operation?	Go to Seq 38.
10	Is +NRZI CHAR GATE (Y1C2J12) operating incorrectly? (See timing chart on 17-313.)	Go to Seq 15.
11	Is the data correct at the −DEVICE BUS IN x TO DF lines? See the DEVICE BUS IN x TO DF table for test points on 17-312.	Change Y1C2.
12	Does the tape control have a device switch feature installed?	Go to Seq 40.
13	Is the data incorrect on the TUBIs? See the TUBI table for test points on 17-312.	Go to Seq 18.
14	If not:	Recheck symptoms.
15	Is +RESET FIRST BIT (Y1C2G13) a constant plus?	Change Y1C2.
16	Is −SET NRZI FIRST BIT (Y1C2G03) pulsing correctly?	Change Y1C2.
17	Is there any data on the TUBIs? See the TUBI table for test points on 17-312.	Go to Seq 21.
18	Move the scope sync to −WRT CONDITION (A1G2G07).	
19	Is data going out to the tape unit on the TUBOs? See the TUBO table for test points on 17-312.	Go to 18-000.
20	If not:	Change A1H2. If the problem still exists find out why the Write Triggers aren't working. See ALD pages BW061, BW071, and BW081.
21	Does the tape control have a device switch feature installed?	Go to Seq 40.
22	If Not:	Change A2D2.
23	Is +NRZI CHAR GATE (Y1C2J12) operating incorrectly? (See timing chart on 17-313.)	Go to Seq 27.
24	Is unit failing during a Write operation?	Go to Seq 31.
25	Is the data incorrect at the −DEVICE BUS IN x TO DF lines? See the DEVICE BUS IN x TO DF table for test points on 17-312.	Go to Seq 35.
26	If not:	Change Y1C2.
27	Is pin Y1C2G13 a constant plus?	Go to Seq 29.
28	Is −SET NRZI 1ST BIT (Y1C2G03) pulsing correctly?	Change Y1C2.
29	Is there any data on the TUBIs? See the TUBI table for test points on 17-312.	Go to Seq 35.
30	If not:	Check the TUBI cables.
31	Is −RD AND TAPE OP (Y1C2B07) minus?	Go to ALD and follow the line back to the failing point.
32	Is −R/W VRC (Y1C2M12) minus?	Change Y1C2.
33	Is +NRZI R/W VRC (Y1C2S07) minus?	Change Y1K2.
34	If not:	Change Y1C2.
35	Does the tape control have a device switch feature installed?	Go to Seq 40.
36	Is the data incorrect on the TUBI? See the TUBI table for test points on 17-312.	Go to 5A-000 for Models 3, 5, and 7. Go to 5B-000 for Models 4, 6, and 8.
37	If not:	Change A2D2.
38	Is −WRT AND TAPE OP (Y1C2U06) plus?	Change Y1C2.
39	If not:	Change A1K2.
40	Is the data incorrect on the TUBI? See the TUBI table for test points on 17-312.	Check the TUBI cables and the tape unit.
41	Is the tape unit operating on the secondary interface?	Go to Seq 45.
42	Is −GATE SECONDARY RECEIVERS (A2D2D13) minus?	Go to ALD XC021 and follow the line back to the failing point.
43	Is −GATE PRIMARY RECEIVERS (A2D2D11) minus?	Change A2D2.
44	If not:	Go to ALD XC011 and follow the −GATE PRIMARY RECEIVERS line back to the failing point.
45	Is −GATE PRIMARY RECEIVERS (A2D2D11) minus?	Go to ALD XC011 and follow the line back to the failing point.
46	Is −GATE SECONDARY RECEIVERS (A2D2D13) minus?	Change A2D2.
47	If not:	Go to ALD XC021 and follow the −GATE SECONDARY RECEIVERS line back to the failing point.
48	Is the data incorrect? (Refer to timing chart 17-314.)	Go to Seq 4 if in a Write operation or Seq 6 if in a Read operation.

LRCR ERRORS, SENSE BYTE 3 BITS 0, 1, OR 4 (Cont'd)

Seq	Condition/Instruction	Action
49	Is the CRC incorrect?	Go to 17-590.
50	Is the tape control doing a Read operation?	Go to 5A-000 for Models 3, 5, and 7. Go to 5B-000 for Models 4, 6, and 8.
51	Sync the scope on –WRT CONDITION (A1G2G07).	
52	Check the TUBO bits, are the Write Triggers being turned off at the fall of WRT CONDITION? See the TUBO table for test points on 17-312.	Go to 5A-000 for Models 3, 5, and 7. Go to 5B-000 for Models 4, 6, and 8.
53	If not:	Go to ALD BW061, BW071, and BW081 and find out why the Write Triggers are not turned off.
54	If the failing 7-track mode is unknown, write the tape and read it back in the various 7-track modes to determine the failing mode. (See 40-008 for 7-track mode set commands.) Byte Count Dialed 00 through FE FF — Byte Count Written count dialed plus three 2	
55	Is the failure a Hi Clip VRC (Byte 3, bit 4)?	Go to Seq 59.
56	Is the failure a READ VRC error (Byte 3, bit 0)?	Go to Seq 106.
57	Is the failure a LRC error (Byte 3, bit 1)?	Go to Seq 108.
58	If not:	Recheck symptoms.
59	While writing the tape in the failing mode and failing data pattern sync minus on –SET NRZI FIRST BIT (Y1C2G03). Is the sync present?	Go to Seq 65.
60	Is +RESET FIRST BIT (Y1C2G13) always plus?	Change Y1C2.
61	Is –SET NRZI 1ST BIT (Y1C2G03) pulsing correctly?	Change Y1C2.
62	Is NRZI CHARACTER GATE FREQ (Y1C2D04) a constant plus or minus?	Change A1K2.
63	Check the DEVICE BUS IN x TO DF lines. See –DEVICE BUS IN x TO DF chart on 17-312 for test points. Are any of these lines pulsing?	Change Y1D2.
64	If not:	Go to 18-020.
65	Does the failure occur while the tape control is writing in Data Convert or Translate mode?	Go to Seq 92.
66	Does the failure occur while the tape control is writing in an even parity mode?	Go to Seq 87.

Seq	Condition/Instruction	Action
67	Is there a Wr Tgr VRC error?	Go to 17-170.
68	Does the failure occur while writing in 200 bpi only (23 mode set)?	Change A1K2.
69	Does the failure occur while writing in 556 bpi only (73 mode set)?	Change A1K2.
70	Does the failure occur while writing in 800 bpi only (83 mode set)?	Change A1K2.
71	Does the tape control fail in 800 bpi, 556 bpi, and 200 bpi modes?	Go to Seq 73.
72	If not:	Recheck symptoms.
73	When writing a 7-track record with the Data Converter (DC) off, the data shifts of NRZI CHAR GATE should equal the number of data bytes in the records (see 7-track timing chart on 17-313). In the example given, there are seven shifts of +NRZI CHAR GATE (there is one more shift for the LRCC character in an odd byte record for 7-track mode). Does NRZI CHAR GATE shift as explained above?	Go to Seq 76.
74	Is –DATA CONVERTER ON (A1L2B13) minus?	Change A1L2.
75	If not:	Change A1E2.
76	Is –STAT BIT 3 7-TRACK (Y1C2M05) plus?	Change A2Q2.
77	Is –XLATE ON (A1L2D09) minus?	Change A1L2.
78	Is +PARITY EVEN (A1L2G04) minus?	Change A1L2.
79	Scope the –DEVICE BUS IN x TO DF lines (see chart on 17-312 for test points). Check each byte for odd parity (for the first byte in the record, ensure that an odd number of tracks shift plus back to minus). See 7-track timing chart on 17-313 for an example of how line shifts look when there is a one on a track and the –DEVICE BUS IN x TO DF line shifts plus for a short time and then goes back to a minus level.	
80	Does any byte in the record have even parity?	Go to Seq 84.
81	Is +RESET RD REG 1 (Y1C2S05) always plus?	Change Y1C2.
82	Is –R/W VRC BAD A (Y1D2U09) always minus?	Change Y1D2.
83	If not:	Change Y1C2.
84	Sync on –WRT CONDITION (A1G2G07).	

Seq	Condition/Instruction	Action
85	See 7-track timing chart on 17-313. In NRZI mode, a one bit is written for each shift of the write triggers. Scope the –TUBO BIT P line and +TUBO BITS 0 through 7. See TUBO Test Point Chart on 17-312. Check each byte being written for odd parity. Does any byte have even parity?	Change A1H2.
86	If not:	Go to 18-010.
87	Set the tape control to odd parity. Xlate off, Data Conver (DC off, set mode to the failing bit density: 800 bpi — B3 556 bpi — 73 200 bpi –– 33 B3, 73, and 33 are 7-track mode sets for different bit densities. Does the failure occur while writing in odd parity?	Go to Seq 68.
88	Set IC back to writing even parity, Data Converter (DC) off, and Xlate off in the failing bit density: 800 bpi — A3 556 bpi — 63 200 bpi — 23 A3, 63 and 23 are the mode sets for the different densities.	
89	Is –PARITY EVEN (A1L2D13) plus?	Change A1L2.
90	Is +PARITY EVEN (A1L2G04) minus?	Change A1L2.
91	If not:	Change Y1C2.
92	Does the error occur with Data Converter (DC) on, and the failing bit density? 800 bpi — 93 556 bpi — 53 200 bpi — 13 93, 53 and 13 are the mode sets for the different densities.	Go to Seq 96.
93	Does the error occur with Xlate on, Data Converter (DC) off, even parity in the failing bit density? 800 bpi — AB 556 bpi — 6B 200 bpi — 2B AB, 6B and 2B are the mode sets for the different bit densities.	Go to Seq 99.

LRCC ERROR SENSE BYTE 3 BITS 0, 1 OR 4 (Cont'd)

Seq	Condition/Instruction	Action
94	Does the error occur with Xlate on, Data Converter (DC) off, odd parity in the failing bit density? 800 bpi — BB 556 bpi — 7B 200 bpi — 3B BB, 7B and 3B are the mode sets for the different bit densities.	Go to Seq 104.
95	If not:	Recheck symptoms.
96	Is –DATA CONVERTER ON (A1L2B13) plus?	Change A1L2.
97	Enter one of the following mode set commands at the tape control CE panel: 800 bpi — A3 556 bpi — 63 200 bpi — 23 Does the error occur with the Data Converter (DC) off, Xlate off, and odd parity?	Go to Seq 67.
98	If not:	Change A1E2.
99	Is +PARITY EVEN (A1L2G04) minus?	Change A1L2.
100	Is –PARITY EVEN (A1L2D13) plus?	Change A1L2.
101	Is –XLATE ON (A1L2D09) plus?	Change A1L2.
102	Enter one of the following mode set commands at the tape control CE panel: 800 bpi — A3 556 bpi — 63 200 bpi — 23 Does the error occur with the Data Converter (DC) off, Xlate off, and even parity?	Go to Seq 87.
103	If not:	Change A1E2.
104	Is –XLATE ON (A1L2D09) plus?	Change A1L2.
105	If not:	Go to Seq 97.
106	While writing the tape in the failing mode, is the tape control flagging a Hi Clip VRC error?	Go to Seq 59.
107	If not:	Change Y1C2.
108	Analyze this error while doing a write in the failing mode set. Sync the scope on –WRITE CONDITION (A1G2G07).	
109	Check the –TUBO BIT P line and the +TUBO BIT 0 through 7 lines (see TUBO test points on chart 17-312). Are any TUBO bits active after the end of write condition (see 7-track timing chart on 17-313)?	Change A1H2.
110	If not:	Change A1D2.

TUBI Test Points

BUS IN	WITHOUT COMMUNICATOR	WITH COMMUNICATOR	
		PRIMARY	SECONDARY
–DEVICE BUS IN P	A2D2M03	A2D2S07	A2D2M03
–DEVICE BUS IN 0	A2D2P05	A2D2M05	A2D2P05
–DEVICE BUS IN 1	A2D2D10	A2D2J09	A2D2D10
–DEVICE BUS IN 2	A2D2P10	A2D2J06	A2D2P10
–DEVICE BUS IN 3	A2D2M12	A2D2G13	A2D2M12
–DEVICE BUS IN 4	A2D2D04	A2D2G08	A2D2D04
–DEVICE BUS IN 5	A2D2P04	A2D2G10	A2D2P04
–DEVICE BUS IN 6	A2D2J12	A2D2M10	A2D2J12
–DEVICE BUS IN 7	A2D2B04	A2D2D06	A2D2B04

Device Bus In x To DF Test Points

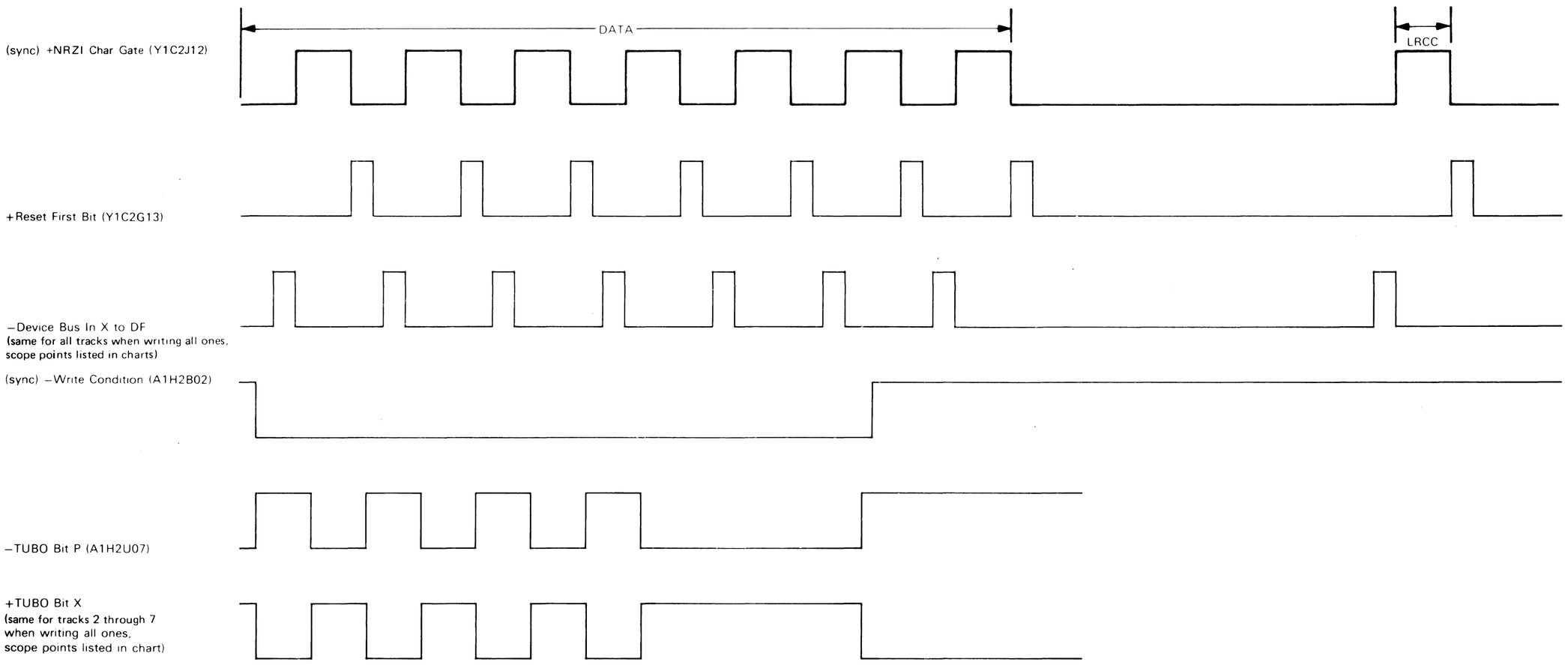
TRAC	PIN
P	Y1D2U12
0	Y1D2U07
1	Y1D2U02
2	Y1D2P05
3	Y1D2P02
4	Y1D2J09
5	Y1D2D13
6	Y1D2D09
7	Y1D2D04

TUBO Test Points

TRAC	PIN
P	A1H2U07
0	A1H2M10
1	A1H2S10
2	A1H2U05
3	A1H2P09
4	A1H2J03
5	A1H2J07
6	A1H2M04
7	A1H2J13

7-TRACK TIMING CHART

7 Character Record, All Ones, 7 Trk, Odd Parity
800 bpi,** DC Off, XLATE Off



Notes:

1. The timing for all ones, even parity, 800 bpi DC off, Xlate off, will look the same except there will be no –TUBO Bit P for track P and nothing on –Device Bus In P to DF for track P.
2. The timings for 200 bpi and 556 bpi will look the same as 800 bpi. However, the actual timings will change in duration.

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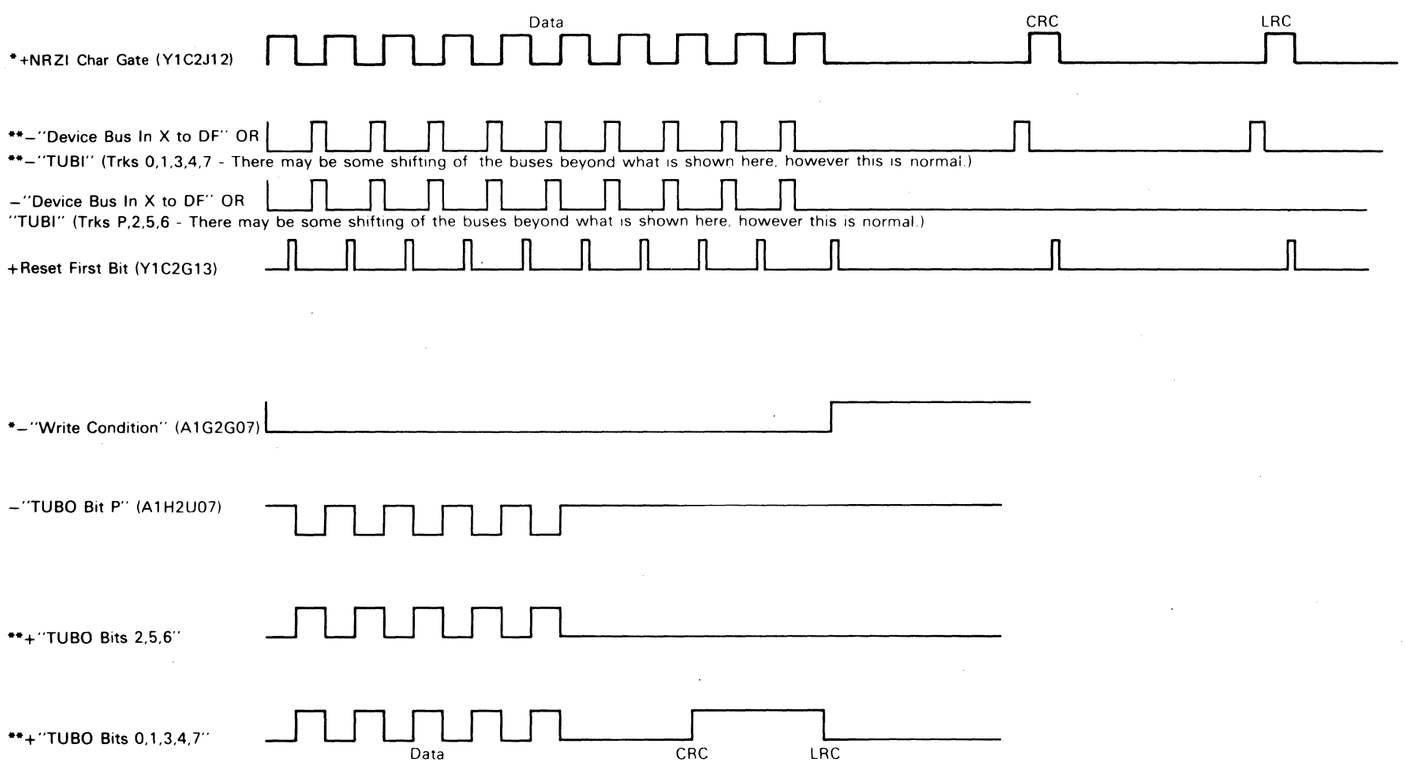
TIMING CHART, NRZI R/W VRC, HI CLIP VRC, LRC ERRORS



*Sync Points

**These test points are in the test point charts on 17-312

17-314

ENVELOPE CHECK

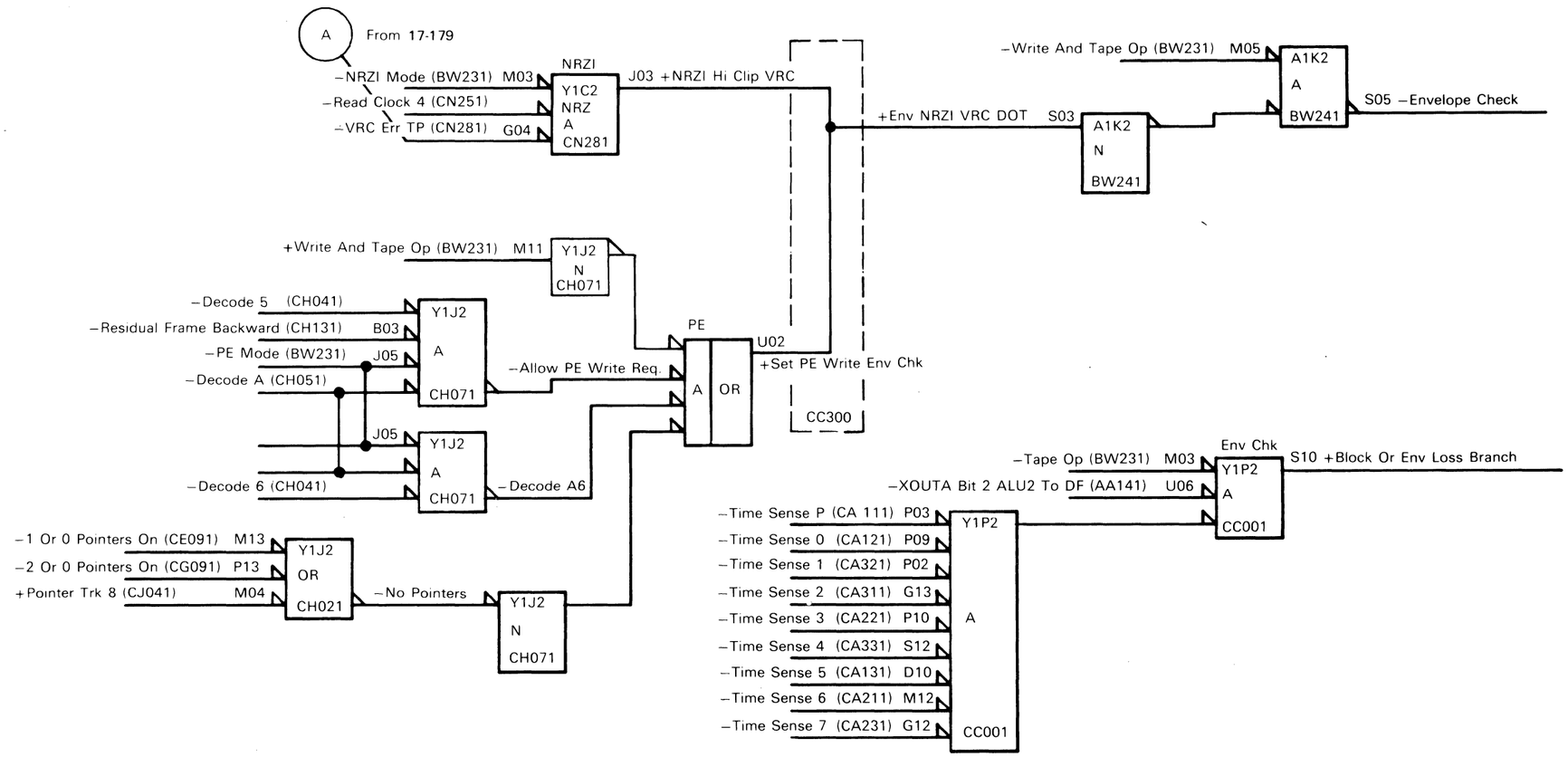
Sense byte 3, bit 4 is set:

A. PE Write - when a phase error pointer is set because a phase shift is detected which exceeds the capability of the VFC circuits on read back data from the tape unit. This also sets data check.

B. NRZI - when a NRZI Hi Clip VRC error occurs.

C. PE Read, 6250 Read, 6250 Write - when any time sensor becomes inactive. The microprogram sets ENVELOPE ERROR.

ENV Check Block or ENV Loss



From 14-000

ERROR DESCRIPTION:
Sense Byte 1, Bit 0 is set:

A. On any Data Check condition during 6250 bpi or PE Read or Read Backward operations.
B. When data is not transferred to channel during 6250 bpi, PE, or NRZI Read or Read Backward operations.
C. When data is detected during Read Stop Delay in NRZI Read operations.
D. When data is detected during 6250 bpi, PE, or NRZI Erase Gap operations.
E. When data is detected during the Erase Gap portion of 6250 BPI, PE, or NRZI Write Tape Mark operations.

Most Probable Causes:
The following list of cards can cause the problems covered in this procedure. The cards are listed with the highest probability first. Lines with multiple cards have the same probability.

Control Unit

A. Y1D2, Y1C2, Y1P2
B. A1K2
C. (7-Track only) A1E2, A1L2

Single Tape Unit

A. Erase head
B. Read/write head
C. Write head card

ADDITIONAL CARDS AFFECTED:

Control Unit

A. B2L2
B. B2M2
C. A1C2
D. B2D2
E. Y1N2
F. A1D2
G. Y1H2
H. A1F2
I. Y1J2
J. A2D2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise.
Remember to END all problems or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Is this a single tape unit failure?	For Models (4, 6, 8), go to 5B-000. For Models (3, 5, 7), go to 5A-000.
1A	Does the failure occur only during an ERG operation?	Go to Seq 61.
2	Does the failure occur only during a WTM operation?	Go to Seq 61.
3	Does the failure occur only during a NRZI Read operation?	Go to Seq 50.
4	Does the failure occur only during a PE Read operation?	Go to Seq 60.
5	Mount a work tape that is correctly written in the failing density. tape unit. Reset, Load, and Ready the tape unit.	
6	With the failing tape control offline, set up the following operations from the CE panel: NOP or Mode Set RDF RDF RDB Byte Cnt = F5F Wrt Data and Go Dwn = FF0 Reset the tape control.	
7	Set up a Compare Stop on ALU1 address 3BF (NO SVC +3).	
8	Turn the ROS Mode switch to Stop. Operate the Set ROS Mode switch. Operate the Start or Step switch.	
9	Was there a '3BF' Read Forward Compare Stop?	Go to Seq 18.
10	Was there a '3BF' Read Backward Compare Stop?	Go to Seq 18.
11	Data is being transferred to channel.	
12	Set up a Compare Stop on ALU1 address at '3E2' (DATCHECK).	
13	Set ROS mode to step.	
14	Is there a Read Forward Compare Stop?	Go to Seq 27.
15	Is there a Read Backward Compare Stop?	Go to Seq 27.
16	Is this a verification check after replacing a FRU?	If no Compare Stop occurs in Seq 9 through 15, the fix was successful.
17	Failure has not been identified with the test setup being used. Run the operations set up in Seq 6 in Run Mode, rather than Step Mode. The failure may be intermittent; the Compare Equal light will come on if address compare setup is used. If no failure occurs, go to Seq 60 and try the test in PE Mode, if available.	
18	Set up a Compare Stop on ALU1 address '3B5' (SVCWATE+1).	
19	Do the operations set up in Seq 6 in Run Mode.	
20	Sync minus on −CE SELECT REG PULSE (A1U2U07).	
21	Is +BRANCH COND MET ALU1 (B2L2M11) at a plus MST level, or going to a plus MST level within 100 ns of sync time?	
22	Is +DATA SERVICE ACTIVE (B2L2D13) pulsing?	Change B2L2.
23	Is +SERVICE OUT CHAN A B CE (B2L2G03) PULSING?	Change B2L2.
24	Is +SERVICE IN FOR DATA (B2M2U12) pulsing?	Change B2M2.
25	Is −SERVICE OUT (A1C2M08) pulsing?	Change A1C2.
26	If not:	Go to Seq 36.
27	Set up a Sync Compare of ALU1 address 3D4 (CHKUNCHK+3—A1U2U07).	
28	Do the operations set up in Seq 6 in Run mode then return here.	
29	Sync minus on −CE SELECT REQ PULSE (A1U2U07).	
30	Is −DATA CHECK BRANCH (A1K2S07) at a plus MST level?	Change B2D2.
31	Is +TAPE OP DELAYED (A1K2P03) at a minus MST level?	Change Y1N2.
32	Is −EOD OR CRC OK DOT (A1K2P10) at a plus MST level?	Go to Seq 34.
33	If not:	Change A1K2.
34	Is −ALLOW CRIC (A1D2P03) at a minus MST level?	Change A1D2.
35	If not:	Change Y1H2.
36	Is +READ CYCLE RESET (A1F2D10) failing to pulse?	Change A1F2.
37	Is −READ AND TAPE OP (A1F2J13) at a plus MST level?	Change A1F2.
38	Is −ALLOW CRIC (A1F2B04) at a plus MST level?	Change Y1H2.
39	Is −REQ CB WRITE CYC DOT (A1F2D03) at a minus MST level?	Change A1F2.
40	Is this test being run in 7-track NRZI mode?	Go to Seq 47.
41	Is this test being run in 9-track NRZI mode?	Go to Seq 44.
42	Is −REQ CB WRT CYCLE (Y1J2S12) at a plus MST level?	Change in order: 1. Y1J2 2. A1E2 (if 7-track feature is installed). Go to Seq 5 to verify fix.
43	If not:	Change A1E2 (if 7-track feature is installed)
44	Is +NRZI WRT REQ (Y1J2S10) at a minus MST level?	Change Y1C2.
45	Is −REQ CB WRT CYCLE (Y1J2S12) at a plus MST level?	Change Y1J2.
46	If not:	Change A1E2 (if 7-track feature is installed).

NOISE DETECTION (Cont'd)

Seq	Condition/Instruction	Action
47	Is –REQ CB WRT CYCLE (A1E2P02) at a minus MST level?	Change A1E2.
48	Is +NRZI WRITE REQ (Y1J2S10) at a minus MST level?	Change Y1C2.
49	If not:	Change Y1J2.
50	Mount a work tape that on a 3420 Model 3, 5, or 7 has been written correctly in the failing NRZI density. Reset, Load, and Ready the tape unit.	
51	With the failing tape control offline, set up the following operations from the CE panel: MODE SET required to read the CE work tape in Seq 50 RDF RDF RDB Byte Cnt = FXX Wrt Data and Go Down = FF0 Reset the tape control.	
52	Set up a Compare Stop on ALU2 address '42F' (MOVEUP). Set the ROS Mode switch to NORM and operate the Set ROS Mode switch. Press START.	
53	Did the tape control stop on ROS2 address '42F'?	Go to Seq 55.
54	There was no NRZI data detected during STOP DELAY.	Go to Seq 7.
55	Set up a Sync Compare of ALU2 address '425' (CNTLOOP+1).	
56	Sync minus on –CE SELECT REQ PULSE (A1U2U07) and run operation set up in Seq 51.	
57	Is –FB DATA OR ALL ONES (Y1H2U09) at a plus MST level at sync time?	Change A2D2.
58	Is +NRZI CHAR GATE (Y1H2S12) at a minus MST level at sync time?	Change Y1H2.
59	If not:	Change Y1C2.
60	Mount a prewritten PE tape on a PE tape unit. Reset, Load, and Ready the tape unit.	Go to Seq 6.
61	Mount a CE work tape on the tape unit to be tested. Reset, Load and Ready the tape unit.	
62	With the failing tape control offline, set up the following operations from the CE panel. (The first command is a NOP or Mode Set depending on the failing mode.) NOP or Mode Set ERG ERG ERG Byte Cnt = F5F Wrt Data and Go Dwn = FF0 Reset the tape control.	
63	Set up a Sync Compare of ALU2 address 21F (NOT LPRD).	
64	Sync minus on –CE SELECT REG PULSE (A1U2U07) while running operations in Seq 62.	
65	Is +BLOCK OR ENV LOSS BRANCH (Y1P2S10) at a plus MST level at sync time?	Change A2D2.
66	If not:	Change Y1P2. +BLOCK OR ENV LOSS BRANCH (Y1P2S10) should be a plus level to verify fix.

PARTIAL RECORD (SENSE BYTE 5, BIT 5)

From 14-010

ERROR DESCRIPTION:
Sense Byte 5, Bit 5 is set when an Interblock Gap (IBG) is sensed before End of Data (EOD) is recognized.

Most Probable Causes:
The following list is of the known cards which can cause the problems covered in this procedure. The cards are listed with the highest probability first. Lines with multiple cards have the same probability.

A. A1G2, Y1G2
B. Y1N2, Y1P2
C. Y1Q2

ADDITIONAL CARDS AFFECTED:

A. A2C3
B. A2D2
C. Y1H2
D. Y1J2
E. A1C2

After replacing a FRU, run the diagnostics or the customer program.

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problems or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Is TU CHECK (Sense Byte 4, Bit 6) ON?	Go to 15-090.
1A	Is this a single tape unit failure?	Clean capstan. If problem still exists, go to 6A-000 for Models (3, 5, 7). Go to 6B-000 for Models (4, 6, 8).
2	Write a tape, do a Read operation, sync negative on −TAPE OP A (Y1H2D10). Is sync missing?	Go to ALD BW231 EK6 and follow line back to failing point.
3	Sync minus −DEVICE BUS IN P TO DF (Y1T2S04) as a reference (see Pointer System Probe Point List on 17-701). Is −EOD OR CRC OK (Y1H2J13) minus before the end of the postamble?	Go to Seq 15.
4	Do a Read operation and sync negative on −TAPE OP A (Y1H2D10). Using −DEVICE BUS IN P TO DF (Y1T2S04) as a reference (see Pointer System Probe Point List on 17-701), is −IBG BRANCH (Y1P2M07) plus shortly after the beginning of the preamble and minus shortly after the end of the postamble?	−IBG BRANCH is a bad level. Change A2C3. If not fixed, go to Seq 7.
5	Using the setup from Seq 3, is +BLOCK OR ENV LOSS BRANCH (Y1P2S10) ever minus during the period that −IBG BRANCH should be plus?	Change Y1Q2.
6	If not:	Change in order: 1. Y1P2 2. A2D2
7	During a Read operation, scope the following points: +SET FORMAT CHARACTER Y1H2D04 +A1 OR B1 Y1H2G12 +A3 OR B3 Y1H2G09 +RESET FORMAT LTHs Y1H2B02 Do all pulse?	Change Y1H2.
8	Does tape unit fail in PE Mode? (Is Sense Byte 3, Bit 5 ON?)	Go to Seq 12.
9	Do the following points pulse? −0−50 CLOCK BUS YA Y1J2J11 −25−75 CLOCK BUS YA Y1J2D09	Change Y1J2.
10	If not:	Change A1C2.
11	Referring to Seq 7, did any of the following lines fail to pulse? +SET FORMAT CHARACTER Y1H2D04 +A3 OR B3 Y1H2G09 +RESET FORMAT LTHs Y1H2B02	Go to Seq 9.
12	While reading a PE block, sync negative on −PE DECODE A7 (Y1H2U04). Does −DETECTED ALL ONES DATA (Y1H2P06) go minus at END OF DATA time? Add 2 to the number of data bytes being read to determine the number of sync pulses to END OF DATA time. If the tape was written from the CE panel use the following guide to determine the number of data bytes actually written. Hex 00 — writes 3 bytes Hex 01 to FE — writes 3 more bytes than hex value Hex FF — writes 2 bytes	Change Y1H2.
13	Is −R/W VRC ERROR (A1K2P02) minus before END OF DATA goes minus? Refer to Seq 12.	Go to 17-168.
14	If not:	Change Y1G2.
15	Do a Read operation and stop with error on. Scope +BLOCK OR ENV LOSS BRANCH (Y1P2S10). Is it plus?	Change Y1Q2.
16	Do a Read operation and sync negative on −TAPE OP A (Y1H2D10). Using −DEVICE BUS IN TO DF (Y1T2S04) as a reference (see Pointer System Probe Point List on 17-701), is −IBG BRANCH (Y1P2M07) plus shortly after the beginning of the preamble and minus shortly after the end of the postamble?	If −IBG BRANCH is a bad level, change A2C3. Otherwise, change A2D2.
17	If not:	Change Y1P2.

END DATA CHECK

From 14-000 and 17-190

ERROR DESCRIPTION:

Byte 3, bit 3 is set during PE Read operation if the ending ones marker is not detected, or if the postamble contains less than six or more than 50 bytes.

This bit has different meanings depending on the subsystem operating mode and the status of Sense Byte 5, Bits 5 and 6.

In PE mode:
1. If Bits 5 and 6 are OFF, Short Postamble is indicated.
2. If Bit 5 is ON and Bit 6 is OFF, a Partial Record is indicated.
3. If Bit 5 is OFF and Bit 6 is ON, an Excessive Postamble is indicated.

The only time Byte 3, Bit 3 indicates an End Data Check is during a PE Read operation. For all other operations, Byte 3, Bit 3 indicates a CRC error.

Most Probable Causes:

The following list is of the known cards which can cause the problems covered in this procedure. Cards are listed with the highest probability first. Lines with multiple cards have the same probability.
A. A1D2
B. Y1H2, Y1G2

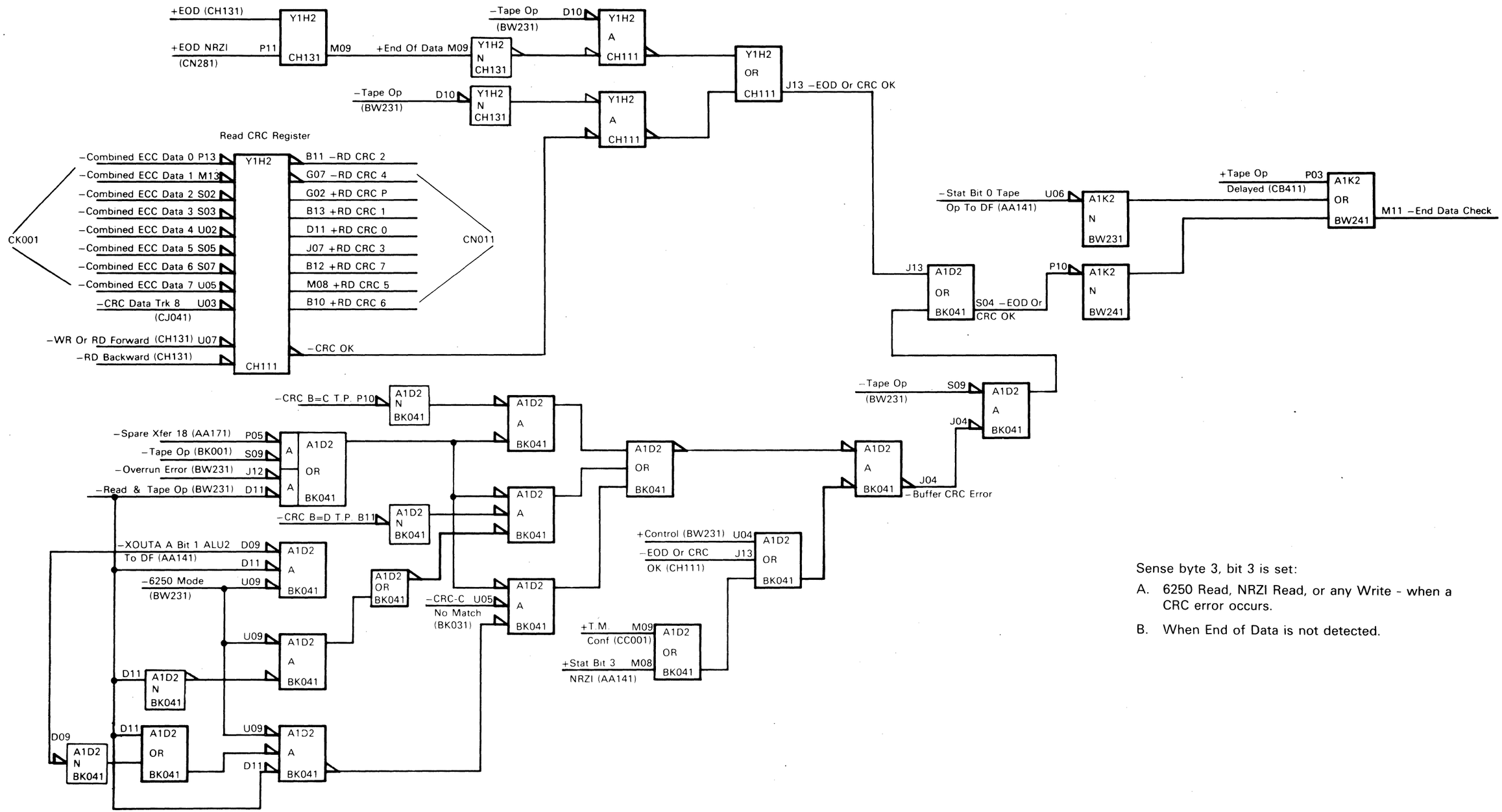
ADDITIONAL CARDS AFFECTED:

A. A1K2
B. A2Q2
C. A2L2
D. A2D2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problems or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Take the tape control offline and set up the CE panel to perform the failing command sequence with Stop On Data Flow Check switch ON.	
2	Is –EOD OR CRC OK DOT (A1K2P10) minus?	Go to Seq 9.
3	Is +9 TRACK CHECK CRC (Y1H2M11) plus?	Go to Seq 13.
4	Sync negative on –STAT BIT 0 TAPE OP TO DF (A1K2U06). Is –6250 MODE (Y1H2S09) minus while the sync is minus?	Go to Seq 7.
5	Is –XOUTA BIT 4 ALU2 TO DF (A1K2D09) minus while the sync is minus?	Change A1K2.
6	If not:	Change in order: 1. A2Q2 2. A2L2
7	Is –BUFFER CRC ERR (A1D2J04) minus?	Go to Seq 11.
8	If not:	Change in order: 1. Y1H2 2. A1D2
9	Sync negative on –STAT BIT 0 TAPE OP TO DF (A1K2U06). Does –EOD OR CRC OK DOT (A1K2P10) become minus while the sync is minus?	Change A2D2.
10	If not:	Change Y1H2.
11	Is –SPARE XFR 18 (A1D2P05) always minus?	Change A2L2.
12	If not:	Change A1D2.
13	Is –NRZI MODE (Y1C2M03) minus?	Change A1K2.
14	If not:	Change Y1C2.

END DATA CHECK



Sense byte 3, bit 3 is set:

A. 6250 Read, NRZI Read, or any Write - when a CRC error occurs.

B. When End of Data is not detected.

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From 14-011, 14-012

ERROR DESCRIPTION:

Sense Byte 9, Bit 3 or Sense Byte 3, Bit 3 (except PE Read Op) is set when a Cyclic Reundancy Check (CRC) error is detected durin a 6250 bpi Read or Write operation.

The CRC-D byte is the check byte written on tape and stored in the D compare register. The CRC-B byte is generated in the CRC-B register during the write operation. During a 6250 bpi Write or Read Forward operation, this bit is set when there is no match between the CRC-B and CRC-D bytes.

The contents of the CRC GENERATOR A register are written on tape as a Check CRC byte during 6250 bpi mode. The CRC-C byte is generated from accumulated data bytes stored in the CRC GENERATOR C register. During a 6250 bpi Read Backward operation, this bit is set when there is no match between the combined data bytes, the Check CRC byte in the A register and the CRC-C byte in the C register.

During a PE Write operation, CRC III Error (Sense Byte 9, Bit 3) is set when there is no match between the data bytes stored in the CRC-C register and the byte previously generated in the CRC-B register.

This error sets Sense Byte 3, Bit 3.

Most Probable Causes:
The following list is of the known cards which can cause the problems covered in this procedure. The cards are listed with the highest probability first. Lines with multiple cards have the same probability. Cards separated by slashes are interchangeable.

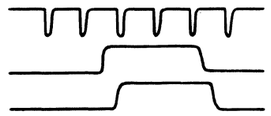
A. Y1J2
B. Y1H2
C. A1D2
D. Y1G2, Y1D2
E. A1F2, Y1F2
F. A1E2
G. Y1K2/Y1L2/Y1M2
H. Y1C2, Y1N2
I. A1K2, A2L2
J. A1G2
K. A1L2, A2Q2, A2T2, Y1P2, Y2R2/Y1S2/Y1T2

ADDITIONAL CARDS AFFECTED:

A. A1B2
B. A1S2
C. B2M2
D. B2L2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise.
Remember to END all problems or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Take the tape control offline. Enter the failing command sequence. It may be record length or data sensitive, Loop write-to-read (LWR) (write data FF, byte count FFF) may be used instead of a write operation if it is the only command performed. A LWR from load point will be performed in PE mode. Jumper A1S2G08 to ground to cause the LWR command to operate with IBGs between data blocks. If LWR runs error-free, use the failing mode.	
2	Turn Stop On Data Flow switch on. Use the following commands: Write (01), Read Backward (0C), Read (02), Backspace Block (27). LWR (8B) may be used if it will fail. Use various byte counts. **Note:** You must have a CRC error and have Stop On Data Flow switch on to proceed.	
3	Check for false error. Is −EOD or CRC OK (A1K2P10) plus?	Go to Seq 9.
4	Is −End Data Check (A1K2M11) minus?	Go to Seq 7.
5	With the CRC Error light ON, is −End Data Check (A1B2D07) plus?	Change A1B2.
6	If not:	Change A1S2.
7	Is +Tape Op Delayed (Y1N2M05) minus?	Change A1K2.
8	If not:	Change Y1N2.
9	Does the failure occur during an Erase Record Gap operation?	Go to Seq 117.
10	Does CRC ERROR (sense byte 3, bit 3) occur only in PE mode (sense byte 3, bit 5)?	Change Y1J2.
11	Use single step mode. Turn Stop On Data Flow Check switch off. Do a 6250 bpi command sequence: WRITE — '01' READ BACKWARD — '0C' READ FORWARD — '02' BACKSPACE BLOCK — '27' (Write data FF0, byte count FF0)	
12	Does CRC error occur on all but the Backspace Block command?	Go to Seq 20.
13	Does CRC error occur only on a Read Backward?	Go to Seq 94.
14	Does CRC error occur only on a Read Forward?	Go to Seq 90.
15	Does CRC error occur only on a Write?	Change in order: 1. A1D2 2. A1E2 Go to Seq 53 if problem not fixed.
16	Does CRC error occur only on a Write and Read Forward?	Go to Seq 61.
17	Does CRC error occur only on a Backspace Block?	Go to Seq 63.
18	Does CRC error occur only on a Read Forward and a Read Backward?	Go to Seq 75.
19	Recheck the symptoms and make sure that another error didn't occur. Also, try other byte counts.	
20	Do a Read Forward and a Read Backward on your READ ONLY tape (6250 bpi). Do both commands run error-free? Ensure failure is CRC.	Go to Seq 49.
21	Did only the Read Forward command in Seq 20 fail?	Go to Seq 59.
22	Did only the Read Backward command in Seq 20 fail?	Change in order: 1. A1D2 2. Y1H2
23	Turn Stop On Data Flow Check switch on. Do a Read Backward on your READ ONLY tape (6250 bpi).	
24	Is −CRC C No Match (A1D2U05) minus? **Note:** This line is data sensitive and may not be active for some data configurations and length even though CRC error is active. Try various data lengths and data.	Go to Seq 33.
25	Turn STOP ON DATA FLOW CHECK switch off. Use LWR with gaps (tape must be away from load point) or write a tape (byte count 0B0, write data FF0) in 6250 BPI mode. If tape was written, rewind then read forward. Sync the scope plus on +Shift CRC (Y1J2D05). Check for the proper number of pulses (should be 23 for this operation). Byte count 0B0 (see timing chart). Are they good? **Note:** The groups of seven SHIFT CRC pulses may appear as one pulse.	Go to Seq 114.
26	Is NRZI feature installed?	Go to Seq 28.
27	If not:	Change Y1J2.
28	Sync the scope minus on −Tape Op A (Y1C2J11) and check +Shift EPR (Y1C2S09) and +Step CRC pulse (Y1C2S10).	
29	Was either plus while the sync was minus?	Go to Seq 31.
30	If not:	Change Y1J2. If NRZI feature is installed, and Y1J2 did not fix the problem, change Y1C2.
31	Was +SHIFT EPR (Y1C2S09) plus (Seq 28)?	Change Y1C2.
32	If not:	Change A2L2.
33	Is +NRZI Degate ECC PH (Y1C2M02) plus?	Change Y1C2.
34	Turn Stop On Data Flow Check switch to Stop On. Stop with CRC error lamp on. Is +1 or 2 Trk Corr (Y1N2P06) plus? Is sense byte 9, bit 0 on?	Change in order: 1. Y1F2 2. Y1J2 3. Y1G2

Seq	Condition/Instruction	Action
35	Turn Stop On Data Flow Check switch off. Do a LWR with gaps (tape must be away from load point) in 6250 bpi mode (count 0B0). Sync on and look at −Set ECC Buffer (Y1J2G12). Does it fail to pulse? **Note:** This pulse is extremely narrow.	Go to Seq 81.
36	Scope −EPI (Y1G2U03) and −EPJ (Y1G2S03). Does either go minus while −Set ECC Buffer (sync) is minus?	Change Y1F2.
37	Do a LWR (byte count 000) in 6250 bpi mode. Scope −Frame Buffer Out (see test points in Seq 38). Do any fail to pulse?	Go to Seq 45.
38	Set time base to 1 microsecond per division. Sync on and look at −Set ECC Buffer (Y1J2G12). Use X10 magnifier (there should be eight pulses). Scope the Frame Buffer and ECC Reg. test points. Look at the test points in relation to the minus portion of −SET ECC BUFFER. Ensure that the Frame Buffer data is set in the ECC Register.  **Test Points** P Y1G2P12 Y1G2J09 0 Y1G2S11 Y1G2S13 1 Y1G2U13 Y1G2S09 2 Y1G2U10 Y1G2U11 3 Y1G2U12 Y1G2S12 4 Y1G2U04 Y1G2U07 5 Y1G2U06 Y1G2S07 6 Y1G2U05 Y1G2S05 7 Y1G2U09 Y1G2G09 **−Frame Buffer OUT** **−ECC Reg. OUT**	
39	Does the ECC Register contain the same data as the Frame Buffer?	Go to Seq 98.
40	Is NRZI feature installed?	Go to Seq 43.
41	Scope −NRZI Mode (Y1D2S05). Is it plus or level bad?	Change Y1G2. If bad level, change Y1F2.
42	If not:	Change A1K2.
43	Change cards.	Change in order: 1. Y1G2 2. Y1D2
44	Is NRZI feature installed?	Go to Seq 109.

Seq	Condition/Instruction	Action
45	Change the Y1K2, Y1L2, and Y1M2 cards. These are the same type card and may be replaced one at a time using one new card. Rerun tests after replacing each card. Is the problem fixed?	Go to 00-030.
46	Change the Y1R2, Y1S2, and Y1T2 cards. These are the same type card and may be replaced one at a time with one new card. Rerun tests after replacing each card. Is the problem fixed?	Go to 00-030.
47	Is 7-Track feature installed (sense byte 13, bit 1 on)?	Change in order: 1. A1E2 2. A1D2
48	If not:	Change A1D2.
49	Do a LWR (with gaps, count 0B0, data FF0, and with tape away from load point) in 6250 bpi mode. Sync plus on +Set Write Data (A1F2P03). Set time base to 20 microseconds per division. Is sync bad or does scope fail to sync (see timing chart on 17-544)? **Note:** Try different byte counts until you have a CRC error.	Go to Seq 135.
50	Set time base to 20 microseconds per division, if your count is 0B0. Compare −CRC Gate (A1F2G10) to +Set Write Data (A1F2P03). Check near the end of the record to allow for a byte count other than 0B0. Is it good (see timing chart on 17-545 and 17-544)?	Go to Seq 135.
51	Do a Write or LWR (use byte count used in Seq 50), and scope +Stop to Data Flow (A1F2G11). Is it plus before the time −CRC Gate (A1G2P03) should go minus? See timing chart on 17-545.	Change A1F2.
52	If not:	With EC733814, change B2M2. See Caution. Without EC733814, change B2L2. See Caution. (A)
53	Do a write operation (byte count 0B0, data FF0). Compare −CRC Control (A1D2S07) to −CRC Gate (A1G2P03).	
54	Is −CRC Control minus at least as long as −CRC Gate, and does it go plus?	Go to Seq 56.
55	If not:	Change A1F2.

Seq	Condition/Instruction	Action
56	Sync minus on −CRC Control (A1D2S07). Ensure that the input data to WRITE CRC OR RESIDUAL logic match the data out. **Card A1D2** **Input Pin** **Output Pin** 0 S02 M13 1 S03 U03 2 M05 P04 3 M07 P07 4 M10 P09 5 M12 M11 6 S11 S10 7 S13 U13	
57	Do the inputs match the outputs, or is input level bad?	If input level is bad, change A1F2. Go to Seq 67.
58	If not:	If input level is bad, change A1F2. Otherwise, change A1D2.
59	Sync plus on −IBG Branch (Y1P2M07). Does −Residual Frame Fwd (Y1J2U12) go minus during or after reading the ALL ONES marker? See timing chart on 17-545.	Change in order: 1. Y1J2 2. A1F2
60	If not:	Change Y1H2.
61	Do an LWR with gaps (at 6250 bpi with tape away from load point, byte count 0B0) and sync plus on +Shift CRC (Y1J2D05). Check for proper number of SHIFT CRC pulses (23). Are they good? See timing chart on 17-545. **Note:** The groups of seven SHIFT CRC may appear as one pulse.	Go to Seq 101.
62	If not:	Go to Seq 98.
63	Is +Control (A1K2M07) plus?	Go to Seq 65.
64	If not:	Change A1K2.
65	Try to sync plus on +Shift CRC (Y1J2D05). Are any pulses present?	Change Y1J2.
66	If not:	Change in order: 1. Y1H2 2. A1D2
67	Do a write or LWR operation (at 6250 bpi with tape away from load point) and sync plus on +Set Write Data (A1F2P03). Scope −Residual Gate (A1F2P02). Is it good? See timing chart on 17-544. **Note:** Reference −Residual Gate to the +Set Write Data line at the end of the record to allow for a record length other than 0B0 which is used on timing chart.	Go to Seq 87.

(A) **CAUTION:** Removing this card may cause channel errors even with power off. Put CPU in the Single Cycle mode before removing card.

CYCLIC REDUNDANCY CHECKS (Cont'd)

Seq	Condition/Instruction	Action
68	If not:	Change A1F2.
69	Do a write or LWR operation (at 6250 bpi with tape away from load point, byte count 0B0). Sync minus on −ROC Cycled (Y1G2P11). Scope −ECC GB ADR 1 (Y1J2U10), −ECC GB ADR 2 (Y1J2S11), and −ECC GB ADR 4 (Y1J2S03). See timing chart on 17-544 and 17-546. Are all three lines good?	Go to Seq 71.
70	If not:	Change Y1J2.
71	Do a write or LWR (with tape away from load point) with gaps, count 0B0 in 6250 bpi mode. Sync and display −GB Full (Y1N2G08). Is it bad? See timing chart on 17-546.	Change Y1J2.
72	Is −FB Module Select (Y1J2J10) bad? See timing chart on 17-546.	Change Y1J2.
73	Is −Set S1 and FB Write Gate (Y1J2P02) bad? See timing chart on 17-546.	Change Y1J2.
74	If all are good:	Go to Seq 44.
75	Do a LWR (with gaps, byte count 0B0) in 6250 bpi mode. Sync plus on +Shift CRC (Y1J2D05).	
76	Is −CRC Control (A1F2B03) bad? See timing chart on 17-545.	Change A1F2.
77	Write a tape in 6250 bpi mode (write data FF0, byte count 0B0). Rewind the tape then Read Forward. Sync minus on −Tape Op (A1K2B10).	
78	Is −Read and Tape Op (A1K2U12) minus when sync is minus?	Go to Seq 105.
79	Is −Stat Bit 2 to DF (A1K2U09) minus during −Tape Op?	Change A1K2.
80	If not:	Change A1Q2.
81	Sync plus on −IBG Branch (Y1P2M07).	
82	Is −Format Character Vote (Y1H2M05) good? See timing chart on 17-546.	Change Y1J2.
83	Is +EOD or PE (Y1H2P04) good? See timing chart on 17-544.	Change Y1H2.
84	Is −PE Mode (Y1H2J05) minus?	Change Y1H2.
85	Is −XOUTA Bit 0 ALU2 TO DF (A1K2S13) minus?	Change A2Q2.
86	If not:	Change A1K2.
87	Sync minus on −Write Condition (A1G2G07).	
88	Are −ECC GB ADR 1 (Y1J2U10), −ECC GB ADR 2 (Y1J2S11), and −ECC GB ADR 4 (Y1J2S03) all good? See timing chart on 17-546.	Change in order: 1. A1G2 2. A1D2

Seq	Condition/Instruction	Action
89	If not:	Change Y1J2.
90	Write a tape in 6250 bpi mode (count 0B0, data FF0). Rewind, then do a Read Forward operation. Sync minus on −ROC Cycled (Y1G2P11). Set time base to 10 microseconds per division.	
91	Is +Set Check Byte (Y1J2D12) good? See timing chart on 17-545.	Go to Seq 112.
92	Is −Residual Frame Bkwd (Y1H2U06) ever minus?	Change Y1H2.
93	If not:	Change Y1J2.
94	Do a LWR (count 0B0, data FF0) with gaps in 6250 bpi mode.	
95	Sync minus and display −ABC2-C7 (Y1J2D02).	
96	Set time base to 10 microseconds per division. Are there four negative pulses on −ABC2-C7?	Change in order: 1. A1D2 2. Y1H2 3. A1F2
97	If not:	Change Y1J2.
98	Do a LWR (byte count 0B0, data FF0) with gaps. Sync plus on +Shift CRC (Y1J2D05) and check for correct number of pulses. (There should be 23 for this operation.) Set time base to 5 microseconds per division (use X10 magnifier). Are they bad? See timing chart on 17-545. **Note:** The groups of seven SHIFT CRC pulses may appear as one pulse.	Go to Seq 119.
99	Turn X10 magnifier off. Is +Set Check Byte (Y1J2D12) good (only one pulse)? See timing chart on 17-545.	Go to Seq 69.
100	If not:	Change Y1J2.
101	Is +Set Check Byte (Y1J2D12) good? See timing chart on 17-545.	Change in order: 1. A1D2 2. Y1H2
102	Is −Set Residual Frame Forward (Y1J2U12) good? See timing chart on 17-545.	Change Y1J2.
103	Is −XOUTA Bit 1 ALU2 to DF (Y1H2M12) good? See timing chart on 17-544.	Change Y1H2.
104	If not:	Change A2Q2.
105	Sync plus on +Shift CRC (Y1J2D05). Set time base to 10 microseconds per division.	
106	Is +Set Residual Cnt (Y1J2J03) bad? See timing chart on 17-545.	Change Y1J2.

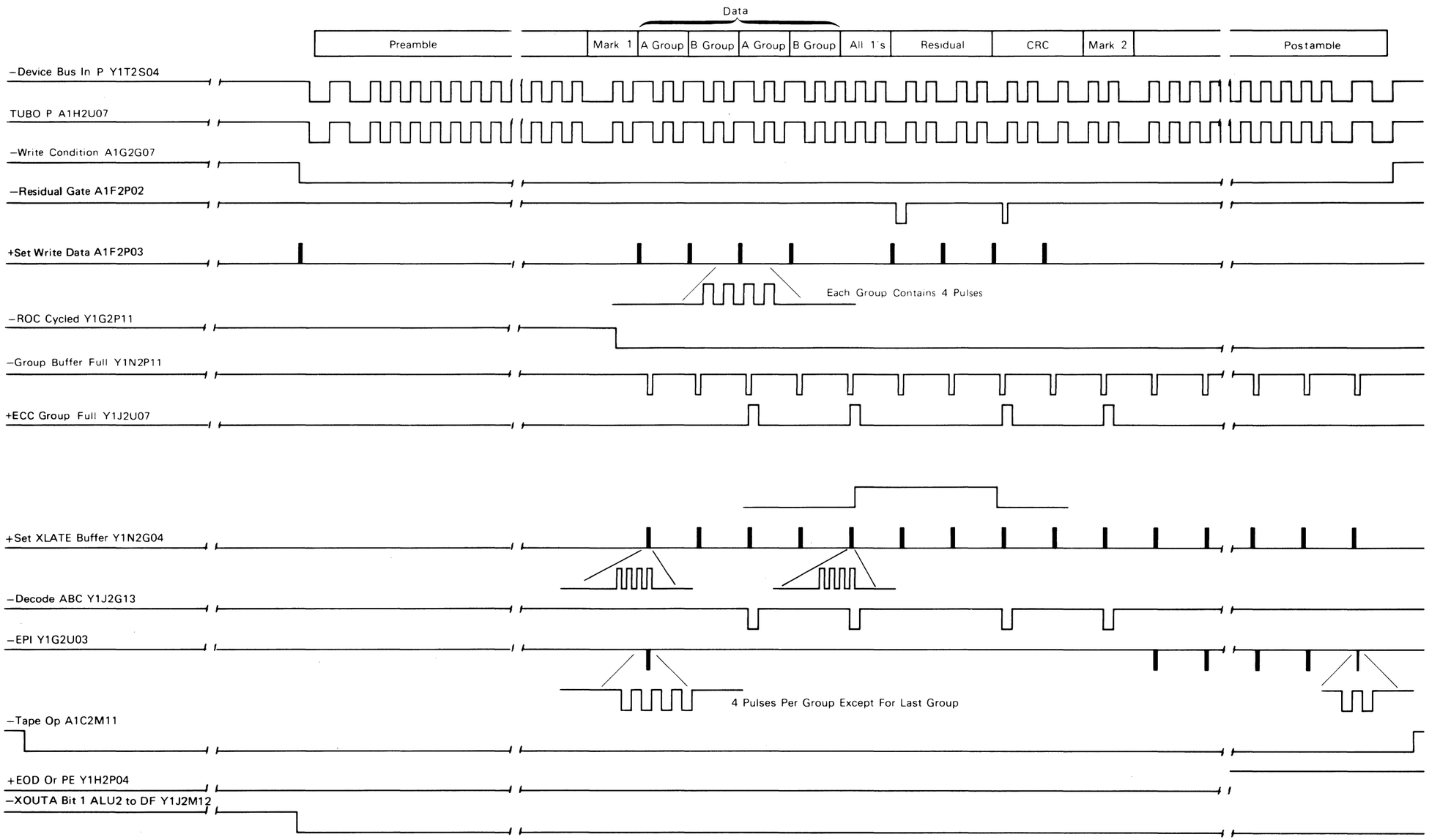
Seq	Condition/Instruction	Action
107	Is −Req CB Wrt Cycle (Y1J2S12) good? See timing chart on 17-545.	Change A1D2.
108	If not:	Change in order: 1. Y1J2 2. A1E2
109	Remove the Y1C2 and Y1D2 cards.	
110	Does the tape control run without errors now?	Change Y1D2.
111	If not:	Go to Seq 45.
112	Is +Residual 32 Compare (Y1H2U12) good? See timing chart on 17-545.	Go to Seq 131.
113	If not:	Go to Seq 140.
114	Is −CRC Data Trk 8 (Y1G2B04) pulsing?	Change Y1H2.
115	Is +NRZI CRC Bit P (Y1G2D04) ever plus? (If NRZI not installed, go to Seq 116.)	Change Y1D2.
116	If not:	Change Y1G2.
117	Do an Erase Gap (17) operation with the Stop On Data Flow Check switch on. Scope +EOD NRZI (Y1H2P11). Is it plus?	Change Y1C2.
118	If not:	Change Y1H2.
119	Does +Set Write Data Delayed (A1L2B04) compare with +Set Write Data A1G2B13? They should be the same.	Go to Seq 121.
120	If not:	Change A1L2.
121	Does +Set Write Data Feedback (A1L2G12) compare with +Set Write Data A1G2B13? They should be the same.	Go to Seq 123.
122	If not:	Change A1L2.
123	Is +CRC Shift (A1L2G07) pulsing?	Go to Seq 125.
124	If not:	Change in order: 1. A1F2 2. A1L2
125	Is −CRC Control (A1F2B03) good? See timing chart on 17-545.	Go to Seq 127.
126	If not:	Change A1F2.
127	Is −Residual Gate (A1F2P02) good? See timing chart on 17-544.	Go to Seq 129.
128	If not:	Change A1F2.
129	Is −CRC Gate (A1F2G10) good? See timing chart on 17-545.	Go to Seq 131.
130	If not:	Change A1F2.

Cyclic Redundancy Checks (Cont'd)

Seq	Condition/Instruction	Action
131	Is –Full Frame (A1F2J10) minus?	Change A1D2.
132	Is +Control (A1K2M07) minus?	Change A1K2.
133	Is –Stat Bit 2 Spare to DF (A1K2U09) minus?	Change A1K2.
134	If not:	Change A2T2.
135	Is –Read Cycle (A1F2B05) pulsing?	Change A1F2.
136	Is –Full Frame (A1F2J10) minus?	Change A1F2.
137	Is –Read and Tape Op (A1K2U12) minus?	Change A1F2.
138	If not:	Go to Seq 133.
139	Is +Set Residual Count (Y1J2J03) good? See timing chart on 17-545.	Change in order: 1. Y1H2 2. Y1C2
140	If not:	Change Y1J2.

17-543

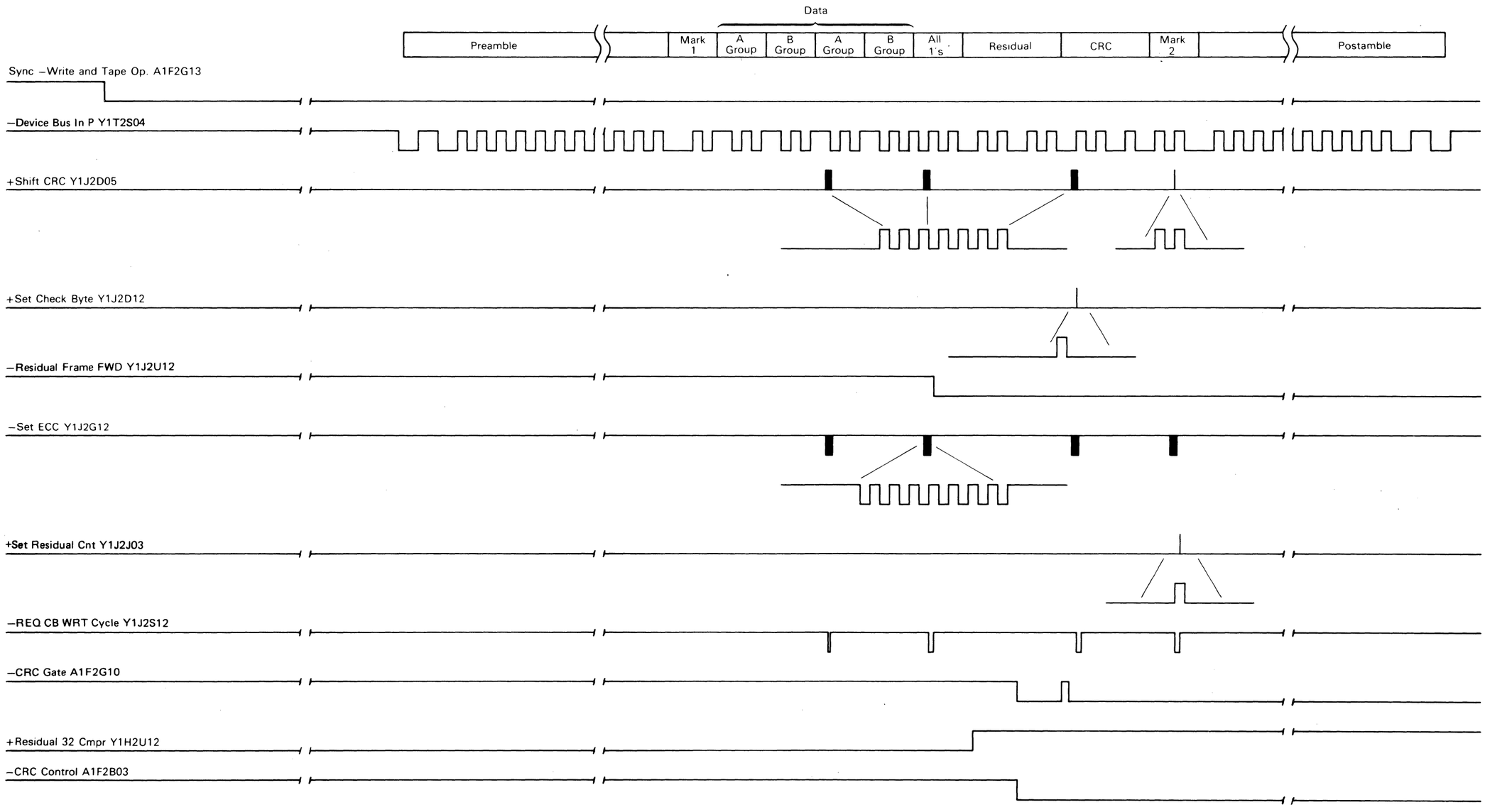
CYCLIC REDUNDANCY CHECK (CRC) TIMING CHART



3803-2/3420

XF4900 Seq 1 of 2	**2735945** Part Number	**See EC History**	**845958** 1 Sep 79					

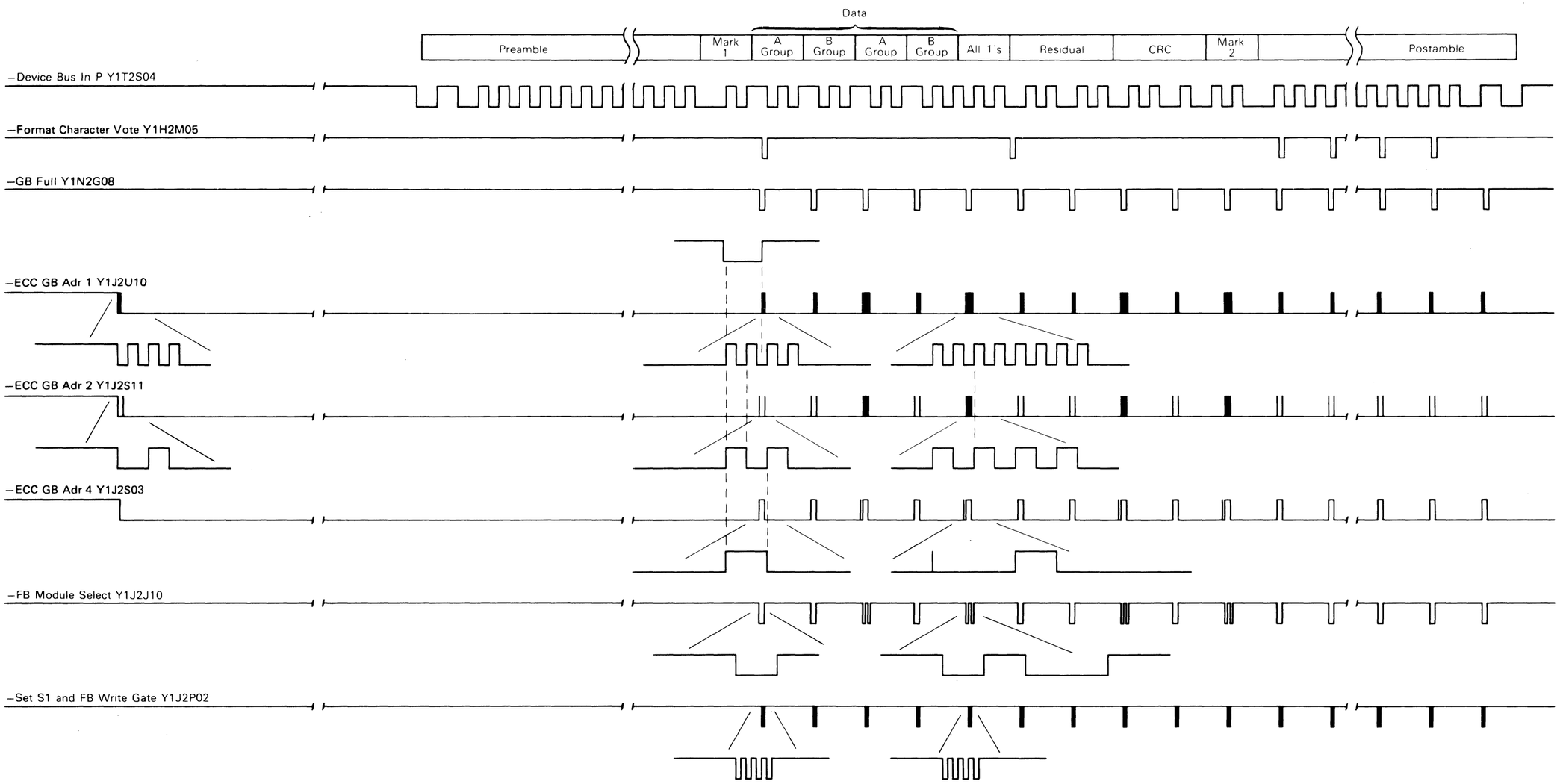
CRC TIMING CHART



3803-2/3420

XF4900 Seq 2 of 2	2735945 Part Number	See EC History	845958 1 Sep 79					

CRC TIMING CHART



3803-2/3420

XF5000 Seq 1 of 2	**2735946** Part Number	**See EC History**	**845958** 1 Sep 79					

NRZI CYCLIC REDUNDANCY CHECK (CRC)

From 14-001

ERROR DESCRIPTION:
Sense Byte 9, Bit 3 is set when a CRC is detected during a 9-track NRZI write operation. If there is no match between the bytes stored in the CRC-C register and the byte previously generated the CRC-B register during Write operation, Sense Byte 9, Bit 3 is set. A CRC is not performed during 7-track NRZI operations.

Most Probable Causes:
The cards are listed with the highest probability first. Lines with multiple cards have the same probability. Cards separated by slashes are interchangeable. The cards are listed with the highest probability first. Lines with multiple cards have the same probability.

A. Y1R2/Y1S2/Y1T2
B. Y1C2
C. Y1H2
D. Y1D2
E. A2R2

ADDITIONAL CARDS AFFECTED:

A. A1L2
B. A1D2
C. Y1J2
D. A1F2
E. A1G2

After replacing a FRU, run the diagnostics or the customer program.

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise.
Remember to END all problems or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Does the error occur on one tape only?	Go to 5B-000 for Models 4, 6, 8. Go to 5A-000 for Modesl 3, 5, 7.
2	Write a short block in the failing data pattern on a tape unit. Does the tape control fail with a P Compare error?	Go to 17-010.
3	Read the tape. Does the error occur when the tape is read?	Go to Seq 5
4	If not:	Change A1D2.
5	Do you have a Read/Write error with the CRC?	Go to 17-310.
6	Sync plus on +9-TRK CORRECTION (Y1D2J12). Is the sync present?	Change Y1D2.
7	Write a 10-byte record of all ones. Use the timing chart on 17-314. Does +NRZI HI CLIP VRC ERROR (Y1C2J03) occur with the CRC?	Go to 17-310 to Troubleshoot VRC Error.
8	Sync on +NRZI CHAR GATE (Y1C2J12). Does +SHIFT CRC NRZI (Y1C2U10) shift other than 11 times?	Change the Y1C2 card. If this doesn't fix the problem, change Y1J2.
9	Do any of the −NRZI RD DATA BIT x lines fail to go minus? See Chart on this page.	Change Y1D2.
10	Is the CRC Correct signal coming back on the −DEVICE BUS IN x lines as per the timing chart on 17-702.	Change Y1H2.
11	Sync on −END WRT SEQUENCE (A1F2G07). Does this line fail to go minus?	Go to ALD BR051 and follow it to the failing point.
12	Does −CRC CNTL (A1F2S07) fail to come up with −END WRT SEQUENCE?	Change A1F2.
13	Does −CH B CRC OR RESIDUAL BIT 7 (A1D2U13) fail to go minus when −CRC CNTL (A1D2S07) and −CROC REG 1 (A1D2S13) go minus?	Change A1D2.
14	If not:	Change A1G2.

BIT x	NRZI RD DATA BIT x test points	DEVICE BUS IN x test points
P	Y1D2B13	Y1D2U12
O	Y1D2G02	Y1D2U07
1	Y1D2B11	Y1D2U02
2	Y1D2M02	Y1D2P05
3	Y1D2G13	Y1D2P02
4	Y1D2J13	Y1D2J09
5	Y1D2J11	Y1D2D13
6	Y1D2G07	Y1D2D09
7	Y1D2G09	Y1D2D04

From 14-000, 21-000

ERROR DESCRIPTION:

Sense Byte 9, bit 0, (1 or 2 track error correction) can be set only on a 6250 bpi Read or Write operation.

1. **6250 bpi Write:**

   1 track error correction can only be performed on a 6250 bpi Write operation if the error occurs during the data portion of the record. No error correction can take place during the other portions of a 6250 bpi Write operation.

2. **6250 bpi Read Operation:**

   1 or 2 track error correction can be performed during any portion of the Read operation.

Most Probable Cause:

A. A1D2
B. Y1N2
C. Y1F2, Y1J2

Additional Cards Affected:

A. Y1K2
B. Y1L2
C. Y1M2
D. Y1G2
E. Y1R2
F. Y1S2
G. Y1T2
H. Y1P2

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problems or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Is the failure isolated to a single tape unit?	Go to 5B-000.
2	Is the failure occurring during OLT correction diagnostics?	Go to Seq 7.
3	Do a LWR from the tape control with FF data. Make sure the tape is away from load point (LWR at load point sets PE mode). Use a byte count of 14, 0B0 in the switches. **Note:** If you get no failures with FF data, try LWR with the Write Data switch in the Ripple position. Sync plus external on –IBG BRANCH (Y1P2M07). With one channel, display one of the DEVICE BUS IN lines. Observe the complete data portion of the record. –DEVICE BUS IN P Y1T2S04 –DEVICE BUS IN 0 Y1T2M04 –DEVICE BUS IN 1 Y1R2M04 –DEVICE BUS IN 2 Y1S2M04 –DEVICE BUS IN 3 Y1R2S04 –DEVICE BUS IN 4 Y1R2D13 –DEVICE BUS IN 5 Y1T2D13 –DEVICE BUS IN 6 Y1S2S04 –DEVICE BUS IN 7 Y1S2D13	
3	(continued) With channel 2, scope the +POINTER TRACK X lines. +POINTER TRACK P Y1J2M04 +POINTER TRACK 0 Y1F2P06 +POINTER TRACK 1 Y1F2M03 +POINTER TRACK 2 Y1F2P03 +POINTER TRACK 3 Y1F2M05 +POINTER TRACK 4 Y1F2P04 +POINTER TRACK 5 Y1F2M07 +POINTER TRACK 6 Y1F2P07 +POINTER TRACK 7 Y1F2M04 Are you getting a + pointer for any track during the data portion of the record?	Go to 17-700.
4	If + pointers are set, you are probably getting a false 1 or 2 track correction bit. Is +1 or 2 TRACK CORRECTION (Y1N2P06) minus?	Change A1D2.
5	Is –SET 1 CNT CMPR (Y1N2P09) plus?	Change Y1N2.
6	If not:	Change Y1F2, Y1J2.
7	Is the failure single track error correction?	Go to Seq 10.
8	Is the failure double track error correction?	Go to Seq 40.
9	If not:	Recheck symptoms.
10	Perform a LWR with gaps, tape away from load point, a 14 byte record (0B Byte Count), and ripple data from the CE panel. Jumper the +DEAD TRACK REG of the failing track, as indicated by the diagnostic printout, to ground. (Refer to Pointer Probe List on 17-701). Perform a sense after the LWR. Is the OLT failure duplicated in the offline mode?	Go to Seq 15.
11	Move the jumper in Seq 10 to –VFC DATA for the failing track. Repeat the procedure in Seq 10. Write Checking (LWR) will force a Skew Error. Is this a Skew Error?	Go to Seq 13.
12	If not:	Recheck your setup, then go to Seq 13.
13	Is the diagnostic failure duplicated with or without considering the Skew Error?	Go to Seq 33.
14	If not:	Recheck symptoms, and go to 00-030.
15	Display and sync on –GB FULL (Y1N2G08). Are there more than 12 negative pulses?	Go to Seq 18.
16	Display and sync on –ROC 25-75 (Y1N2D11). Are there 100 ns pulses?	Change Y1N2. If not fixed, go to ALD CB441 and check for bad input to GB FULL latch.
17	If not:	Change in order: 1. Y1N2 2. Y1K2/L2/M2 If not fixed, go to ALD CB421 and determine cause.
18	Display +ECC GROUP FULL (Y1J2U07). Are there four positive pulses during the first 12 –GB FULL pulses?	Go to Seq 20.
19	If not:	Change Y1J2. If not fixed, go to ALD CH011 and scope inputs to ECC GB FULL latch.
20	Sync on +ECC GROUP FULL (Y1J2U07) and display +GATE HDW PTRS (Y1J2J07). Are there four positive pulses?	Go to Seq 25.
21	Go to ALD CE001 and scope the outputs from the S1 Register. Are any bits negative during +ECC GROUP FULL time?	Go to Seq 23.
22	If not:	Change Y1F2. If not fixed, reference ALD CE001 and check for bad input (levels, etc.) to the S1 Register.
23	Scope the following lines for a bad level: –S2 EQUAL ZERO (Y1F2P09) –S1 EQUALS S2 bits 0-3 (Y1F2M08) –S1 EQUALS S2 bits 4-7 (Y1F2M11) Does any line have a bad level?	See ALD CE001 and determine the cause for the bad level.
24	If not:	Change Y1J2.
25	Display –SET I CNT CMPR (Y1J2G03). Are there four negative 100 ns pulses?	Go to Seq 27.
26	If not:	Change Y1J2. If not fixed, go to ALD CH041 and determine the cause.

Seq	Condition/Instruction	Action
27	Delay sync (B trigger after delay) on the second −SET I CNT CMPR (Y1J2G03) pulse using 5 usec/cm on sweep A and 0.2 usec/cm on sweep B. Display +SHIFT S2 (Y1J2J13) and observe the following waveform depending on the track that is dead tracked. **Track** **S2 Shifts** 0 = 0 5 = 1 6 = 2 2 = 3 7 = 4 4 = 5 1 = 6 3 = 7 p = −Corr trk 8 only (Y1J2M02) (S2 not used for P track correction). Do the correct number of shifts occur?	Go to Seq 29.
28	If not:	Change in order: 1. Y1J2 2. Y1F2
29	Display the following and observe the proper binary value for the S2 shifts. −I COUNT 1 (Y1F2M13), −I COUNT 2 (Y1F2P12), and −I COUNT 4 (Y1F2M10). Does the binary value of the I COUNT lines equal the number of shifts for S2?	Go to Seq 31.
30	If not:	Go to ALD CE001 and determine cause for bad line.
31	Display −SET ECC BUFFER (Y1J2G12) then display −EPI (Y1F2D12). Are there negative correction pulses −EPI at some time during the eight −SET ECC BUFFER pulses?	Change Y1G2.
32	If not:	Go to ALD CE001 and determine cause of the failure of −EPI.
33	Sync on and display −BOR 27 COMB OR DT BRANCH COND (Y1P2J13). Display +SOME TRK MARG (Y1P2M05). Is there a positive pulse on +SOME TRK MARG line?	Go to Seq 35.
34	If not:	Change the Skew Buffer card (Y1K2/L2/M2) for the offending track. If not fixed, go to ALD CC021 and trace the failing input line to the failure.

Seq	Condition/Instruction	Action
35	Sync on and display +SOME TRK MARG (Y1P2M05). Display +START RD CHECK (Y1P2D06). Is there a positive pulse during +SOME TRK MARG time?	Go to Seq 39.
36	Display the following. All should be positive at sync time (+SOME TRK MARG) except the track with the −VFC DATA grounded. +PE WRT SKEW TRK 0 Y1P2G02 +PE WRT SKEW TRK 1 Y1P2G10 +PE WRT SKEW TRK 2 Y1P2B09 +PE WRT SKEW TRK 3 Y1P2G05 +PE WRT SKEW TRK 4 Y1P2B04 +PE WRT SKEW TRK 5 Y1P2B12 +PE WRT SKEW TRK 6 Y1P2B11 +PE WRT SKEW TRK 7 Y1P2B13 +PE WRT SKEW TRK P Y1P2M11 Were the proper levels displayed?	Go to Seq 38.
37	If not:	Change in order: 1. Y1K2/L2/M2 2. Y1R2/S2/T2 If not fixed, go to ALD CC031 and trace failing level to source. (Track P, ALD CC111).
38	The LAG TRACK latch on ALD CC031 has not been set.	Change Y1P2. If not fixed, go to ALD CC031 and determine the cause.
39	The DEAD TRACK latch for the track with −VFC DATA grounded has not been set.	Change Y1P2. If not fixed, go to ALD CC031 through CC111 and determine why DEAD TRACK latch is not set.
40	Perform an LWR with gaps, tape away from load point, a 14-byte record (0B Byte Count), and ripple data from the CE panel. Jumper the +DEAD TRACK registers of the two failing tracks as indicated by the diagnostic print out to ground. (See the Pointer Probe List on 17-701). Perform a sense command after the LWR. Write checking will force MTE and read VRC errors. Is the OLT failure duplicated without considering the write checking errors?	Go to Seq 42.
41	If not:	Recheck set up and symptoms. If OK, go to Seq 7 and attempt using single error procedures.
42	Sync on and display −GB FULL (Y1N2G08). Are there more than 12 negative pulses?	Go to Seq 44.
43	If not:	Go to Seq 16.
44	Display +ECC GROUP FULL (Y1J2U07). Are there four positive pulses during the first 12 −GB FULL pulses?	Go to Seq 46.

Seq	Condition/Instruction	Action
45	If not:	Go to Seq 19.
46	Sync on and display +ECC GROUP FULL (Y1J2U07). Display −SET 1 CNT CMPR (Y1J2G03). Are there four negative 100 ns pulses?	Go to Seq 48.
47	If not:	Go to Seq 26.
48	Delay sync (B triggerable after delay) on the second −SET 1 CNT CMPR (Y1J2G03) pulse using 5 usec/cm on sweep A and 0.2 usec/cm on sweep B. Display −2 PTRS ON PWR (Y1J2G09). Is the pulse negative for approximately 1.6 usec after the sync pulse?	Go to Seq 51.
49	See the Pointer Probe List on 17-701. Probe the +POINTER TRACKS to determine which tracks have pointers. You should have pointers only in the tracks that are grounded (see Seq 41). Are pointers in the proper tracks only?	You have only two pointers active. Change in order: 1. Y1F2 2. Y1J2 If not fixed, reference ALD CH021 and check inputs in "Ptr Ct Dcd" circuit.
50	If not:	Change Y1G2, Y1K2/L2/M2. If not fixed, reference ALD CE001 or CH021 and trace improper or missing pointers to determine cause.
51	Display +SHIFT S2 (Y1J2J13). See Seq 28 to determine correct number of S2 shifts. Look down the track column and locate the first of the two tracks being corrected. The number in the S2 column will be the proper number of shifts. For example, if tracks 2 and 1 are grounded, there should be three shifts of S2. Were the proper number of shifts for S2 observed?	Go to Seq 54.
52	Display −COUNT EQUAL 1 (Y1F2S03). Does it go negative within 800 ns after the sync pulse?	Change Y1J2. If not fixed, go to ALD CH011 and determine cause for +Shift S2 failure.
53	If not:	Change Y1F2. If not fixed go to ALD CE001 and check the −COUNT EQUAL I output.
54	Display −SET ECC BUFFER (Y1J2612). Eight negative pulses starting 800 ns after the sync pulse should occur. Display −EPJ (Y1F2J02) remembering where the −SET ECC BUFFER pulses were displayed. Is there at least one 100 ns negative pulse during −SET ECC BUFFER time?	Change Y1G2. If not fixed, recheck symptoms and go to 00-030.
55	If not:	Change Y1F2. If not fixed, go to ALD CE001 and determine cause.

From 14-000, 17-220, 17-600, 21-000, 00-005

Pointers are indications of wrong data such as phase error, low amplitude, and invalid GCR Group. The pointer system determines which and how many tracks are in error or are corrected. There are three kinds of pointers: hardware, valid, and persistent.

Hardware pointers are set by PE phase error or phase error for 6250 mode (Group Buffer pointers and ECC Group Buffer pointers). Hardware error pointers in 6250 mode are reset after every ECC group in read, and after every resync burst in write. In PE, error pointers are reset every eight bytes.

During PE operation, Sense Byte 2 is set when the track(s) that are dead-tracked are due:

1. To an inactive time sensor during write.
2. To excessive skew in a given track or tracks.
3. To any error pointers that are present when End of Data (EOD) is detected on read or write ops.
4. To any dead tracks that are set during an operation.

During 6250 operation, Sense Byte 2 is set when the track(s) that are dead-track are due:

1. To excessive skew in a given track or tracks.
2. To any error pointers that are present at end data time.
3. To any dead track or tracks present at end of an operation.

CAUTION
Sense Byte 2 information may be invalid if a R/W VRC (Sense Byte 3, Bit 0) is indicated.

Valid pointers are set:

1. When an invalid character (one that does not comply with the translation table) is recognized.
2. When a format character is not recognized in track or tracks with an active format line.
3. When there is a Track In Error (TIE) indication or a multi-track correction.
4. When a format character void is recognized.

Persistent pointers are set during a 6250 bpi operation when eight ECC groups of data are corrected without resetting the valid pointer latch for that track. If eight ECC groups of data that require no correction occur, the valid pointer latch is reset. In PE Mode, persistent pointers are also set when eight bytes of data are corrected without losing the valid pointer. A byte is eight bits plus parity. Persistent pointers set the dead track register in PE mode.

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise.
Remember to END all problems or maintenance calls by going to MAP 00-030.
Refer to 17-701 through 17-705 for timing charts and to 17-701 for test points.

Seq	Condition/Instruction	Action
1	In the failing mode, write all ones. Use LWR if the unit fails in LWR. Write 14 bytes in 6250 bpi mode or eight bytes in PE mode.	
2	If the failure occurs during a Write operation, proceed to Seq 3. If the failure occurs during Read operation, read the tape you wrote in Seq 1 and proceed to Seq 3.	
3	Sync scope positive on −IBG BRANCH (Y1P2M07).	
4	Determine which pointer is ON before end of postamble by checking the +POINTER TRACK x test points. (See 17-701 for test points.)	
5	Does only one tape unit have a pointer on a specific track?	Go to 5A-000 for Models 3, 5, 7. Go to 5B-000 for Models 4, 6, 8.
6	Does more than one tape unit have a pointer on the same track?	Go to Seq 11.
7	Are the −DEVICE BUS IN TO DATA FLOW lines good? (See Pointer Probe list on 17-701.)	Change the VFC card for the bad track: Y1R2 for tracks 1, 3, and 4. Y1S2 for tracks 2, 6, and 7. Y1T2 for tracks P, 0, and 5.
8	Are the TUBI lines bad (see 17-312)?	Go to 18-010.
9	Is there a −6250 EPI CHECK during data tape control's secondary device interface?	Go to Seq 11.
10	If not:	Change A2D2.
11	Does −GB POINTER go minus during data time for all tracks with pointers? (See Pointer Probe List on 17-701.)	Go to Seq 44.
12	Does −POINTER BUS go minus during data time for the track that doesn't go minus in Seq 11? (See Pointer Probe List on 17-701.)	Go to Seq 16.
13	Is −ROC Cycled (Y1G2P11) bad? (See timing chart on 17-702.)	Go to ALD CC121BJ6 and follow line back to failing point.
14	Is −GATED PGM SYNC (Y1G2M11) good?	Change the Y1G2 card.
15	If not:	Go to ALD CC121BM6 and follow line back to failing point.
16	Is there a −6250 bpi CHECK during data time for the track used in Seq 12? (See 17-701.)	Go to Seq 31.
17	Is −XLATE BFR TK X good? (See the timing chart on 17-703.) Sync negative on −IBG BRANCH (Y1P2M07). (Y1P2J13) if you came here from Seq 42.	Go to Seq 38.
18	Is +SAMPLE HDB (Y1K2G11) bad? (See timing chart on 17-703.) **Note: This pulse is hard to see. Turn up the intensity on the scope.**	1. Go to ALD CB421ED6 and follow line back to failing point. 2. Change Y1N2.
19	Is −VFC DATA plus for failing track? (See Pointer Probe List on 17-701).	Go to Seq 7.
20	Does the failure occur during a Read Backward operation?	Go to Seq 56.
21	Is −WRT OR READ FORWARD (Y1H2U07) plus?	Go to ALD CH131BF6 and follow line back to failing point.
22	Is −GB ADR CNTR 1 (Y1K2J06) bad? (See timing chart on 17-705.)	Go to ALD CB441GD6 and follow line back to failing point.
23	Is −GB ADR CNTR 2 (Y1K2P02) bad? (See timing chart on 17-705.)	Go to ALD CB441GF6 and follow line back to failing point.
24	Is +STEP RIC TRACK X bad for failing tracks? (See timing chart on 17-704.)	Go to Seq 7.
25	Did −VFC DATA for the failing track have less than ten pulses while writing the preamble? (See Pointer Probe List on 17-701.)	Go to Seq 7.
26	Did less than ten of the pulses in Seq 25 occur before −VFC PRIME DATA became minus? (See Pointer Probe List on 17-701.)	Go to Seq 7.
27	Is +RESET FORMAT LTHS (Y1J2S09) a solid level?	Change Y1J2.
28	Does −VFC PRIME DATA TRACK become minus after −XOUTA BIT 6 ALU2 TO DF (Y1K2D06) is minus? (See timing chart on 17-705 and the Pointer Probe List on 17-701.)	Replace in order: Zone 1 — Y1M2 Zone 2 — Y1L2 Zone 3 — Y1K2
29	Does −XOUTA BIT 6 ALU2 TO DF (Y1K2D06) become minus at the correct time? (See timing chart on 17-705.)	Go to Seq 7.
30	If not:	Go to ALD AA141 and follow line back to failing point.
31	Is a pointer ON for the failing track while running in 6250 bpi mode?	Go to Seq 34.
32	Is +END OF DATA OR PE (Y1G2J04) minus while writing the record?	Go to ALD CH131GK6 and follow line back to failing point.
33	If not:	Go to Seq 17.
34	Is +INVALID CHARACTER minus for the failing track while writing data? (See timing chart on 17-704 and 17-705.)	Go to Seq 18.
35	Does −FORMAT CHARACTER X become minus on all other tracks at the same time it does on the failing track? (See timing chart on 17-004.)	Change Y1H2.
36	Does −FORMAT CHARACTER X become minus at the wrong time for the failing track? (See timing chart on 17-704.)	Go to Seq 18.
37	If not:	Change Y1H2.
38	Is −SET ECC BUFFER (Y1J2G12) good? (See timing chart on 17-703.) **Note:** This pulse is hard to see. Turn up the intensity on the scope.	Go to Seq 41.

Seq	Condition/Instruction	Action
39	Is –DECODE ABC (Y1J2G13) good? (See Timing Chart on 17-703.)	Change Y1J2.
40	If not:	Go to ALD CH011FB6 and follow line back to failing point.
41	Sync minus ON and display –SET ECC BUFFER (Y1J2G12).	
42	Does –EPI (Y1G2U03) go minus while –SET ECC BUFFER (Y1J2G12) is minus?	Replace in order: 1. Y1F2 2. Y1G2 Go to Seq 17.
43	If not:	Change Y1G2.
44	Does –PE PHASE ERROR ever go minus for the failing tracks while writing the record? (See Pointer Probe List on 17-701.)	Go to Seq 7.
45	Does –PHASE ERROR ever go minus for the failing tracks while writing the record? (See the Pointer Probe List on 17-701.)	Go to Seq 7.
46	Is +Dead Track Register plus for the failing tracks?	Go to Seq 58.
47	Is –SET GROUP BUFFER HWD PTRS (Y1N2D05) bad? **Note:** Short, hard to see pulses. Turn up scope intensity.	Change Y1N2.
48	If not:	Change: For Zone 1 — Y1M2 For Zone 2 — Y1L2 For Zone 3 — Y1K2
49	Is –TIME SENSE ever plus for the failing track while writing the record? (See Pointer Probe List on 17-701.)	Go to Seq 7.
50	Is +PE WRT SKEW plus for the failing track while writing the record? (See Pointer Probe List on 17-701.)	Go to 17-160.
51	Is –POINTER BUS always plus for the failing tracks during the record time? (See Pointer Probe List on 17-701.)	Change Y1P2.
52	Is –ROC CYCLED (Y1G2P11) bad? (See timing chart on 17-702.)	Go to ALD CC121BJ6 and follow line back to failing point.
53	Is –GATED PGM SYNC (Y1G2M11) bad? If in 6250 mode see timing chart on 17-702. If in PE mode, see timing chart on 17-705. (See Pointer Probe List on 17-701.)	Go to ALD CC121BM6 and follow line back to failing point.
54	Is –ALMOST SKEW minus during the record time? (See Pointer Probe List on 17-701.)	Go to 17-160.
55	If not:	Go to Seq 16.
56	Is –READ FORWARD (Y1K2P03) plus?	Go to ALD CH011EE2 and follow line back to failing point.
57	If not:	Go to Seq 22.
58	Ground pointer bus for bad track and recheck the dead track register for the failing track. Does the register still become plus?	Go to Seq 49.
59	If not:	Change card for bad zone: Zone 1—Y1M2 Zone 2—Y1L2 Zone 3—Y1K2

Pointer Probe List

ALL CARDS ARE IN THE Y1 PANEL UNLESS OTHERWISE NOTED	ZONE 1			ZONE 2			ZONE 3		
	TRK P	TRK 0	TRK 5	TRK 2	TRK 6	TRK 7	TRK 1	TRK 3	TRK 4
–DEVICE BUS IN TO DF (Card T2—CA100, Card S2—CA200, Card R2—CA300)	T2S04	T2M04	T2D13	S2M04	S2S04	S2D13	R2M04	R2S04	R2D13
–TIME SENSE (Card T2—CA100, Card S2—CA200, Card R2—CA300)	T2U05	T2M03	T2D10	S2M03	S2U05	S2D10	R2M03	R2U05	R2D10
–VFC DATA (Card T2—CA100, Card S2—CA200, Card R2—CA300)	T2U10	T2G09	T2D07	S2G09	S2U10	S2D07	R2G09	R2U10	R2D07
–VFC PRIME DATA (Card T2—CA100, Card S2—CA200, Card R2—CA300)	T2U13	T2G08	T2B05	S2G08	S2U13	S2B05	R2G08	R2U13	R2B05
–XLATE OUT (Zone 1—CD181, Zone 2—CD281, Zone 3—CD381)	M2G02	M2B13	M2D13	L2G02	L2B13	L2D13	K2G02	K2B13	K2D13
+STEP RIC (Card T2—CA100, Card S2—CA200, Card R2—CA300)	T2U12	T2M02	T2D12	S2M02	S2U12	S2D12	R2M02	R2U12	R2D12
+INVALID CHARACTER (Zone 1—CD181, Zone 2—CD281, Zone 3—CD381)	M2G04	M2M05	M2G13	L2G04	L2M05	L2G13	K2G04	K2M05	K2G13
–FORMAT CHARACTER (Zone 1—CD181, Zone 2—CD281, Zone 3—CD381)	M2G07	M2M07	M2M03	L2G07	L2M07	L2M03	K2G07	K2M07	K2M03
–6250 bpi CHECK (CH151 and CH161)	H2J02	H2J03	H2J11	H2M07	H2D12	H2D13	H2J04	H2M03	H2G10
–GB POINTERS (Zone 1—CD191, Zone 2—CD291, Zone 3—CD391)	M2G12	M2J12	M2J11	L2G12	L2J12	L2J11	K2G12	K2J12	K2J11
–PE PHASE ERROR (Card T2—CA100, Card S2—CA200, Card R2—CA300)	T2U09	T2G10	T2D02	S2G10	S2U09	S2D02	R2G10	R2U09	R2D02
–PHASE ERROR (Card T2—CA100, Card S2—CA200, Card R2—CA300)	T2S10	T2G07	T2B03	S2G07	S2S10	S2B03	R2G07	R2S10	R2B03
+DEAD TRACK REG (CC031 through CC111)	P2G03	P2B05	P2U03	P2U11	P2B02	P2D04	P2S09	P2S13	P2M09
–POINTER BUS (CJ081)	G2P10	G2B12	G2M08	G2D13	G2M05	G2M07	G2M02	G2P02	G2P05
–ALMOST SKEW (CJ081)	G2G09	G2J13	G2P07	G2G12	G2P03	G2P06	G2B13	G2G04	G2P04
DEVICE BUS IN SECONDARY (* A2 PANEL) (XC021)	* D2M03	* D2P05	* D2P04	* D2P10	* D2J12	* D2B04	* D2D10	* D2M12	* D2D04
DEVICE BUS IN PRIMARY (* A2 PANEL) (XC011)	* D2S07	* D2M05	* D2G10	* D2J06	* D2M10	* D2D06	* D2J09	* D2G13	* D2G08
–ALMOST SKEW (Zone 1—CD121-141, Zone 2—CD221-241, Zone 3—CD321-341)	M2M08	M2S09	M2P11	L2M08	L2S09	L2P11	K2M08	K2S09	K2P11
+PE WRT SKEW (Zone 1—CD121-141, Zone 2—CD221-241, Zone 3—CD321-341)	M2M09	M2P07	M2P04	L2M09	L2P07	L2P04	K2M09	K2P07	K2P04
+POINTER TRACK P—CH021, AK; TRACK 0-7—CE091, BB (Track 8 = P)	J2M04	F2P06	F2M07	F2P03	F2P07	F2M04	F2M03	F2M05	F2P04

Chart A

ALL CARDS ARE IN THE Y1 PANEL UNLESS OTHERWISE NOTED	LOCATION
–EPI	G2U03
–ROC CYCLED	G2P11
–GATED PGM SYNC	G2M11
–XOUTA BIT 6 ALU2 TO DF	K2D06
–DECODE ABC	J2G13
–SET ECC	J2G12
+SAMPLE HDB	K2G11
–GB ADR CNTR 1	K2J06
–GB ADR CNTR 2	K2P02
+READ FORWARD	K2P03
+END OF DATA OR PE	G2J04

Chart B

Track	A1G2 Channel or DC	A1H2 Write Bus	TUB0 (A1H2)
P	•	G11	U07
0	U10	D04	M10
1	S13	B04	S10
2	D12	M13	U05
3	G02	J04	P09
4	D07	B07	J03
5	B10	D07	J07
6	U11	D09	M04
7	M11	P07	J13

Chart C

Set Byte	A1H2
1	M07
2	G08
3	G03
4	D02

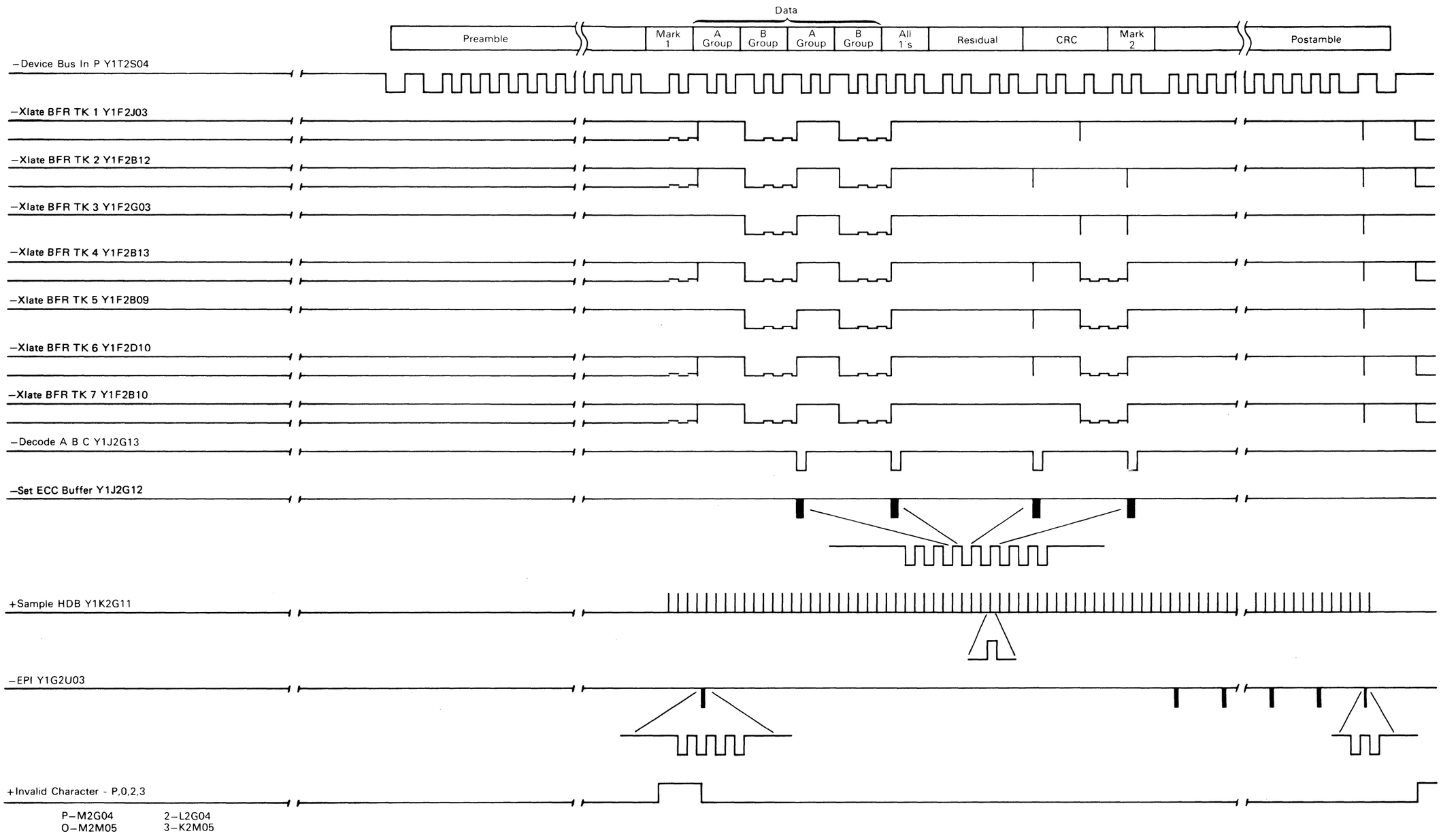
3803-2/3420

XF5200 Seq 1 of 2	2735948 Part Number	See EC History	845958 1 Sep 79					

3803-2/3420

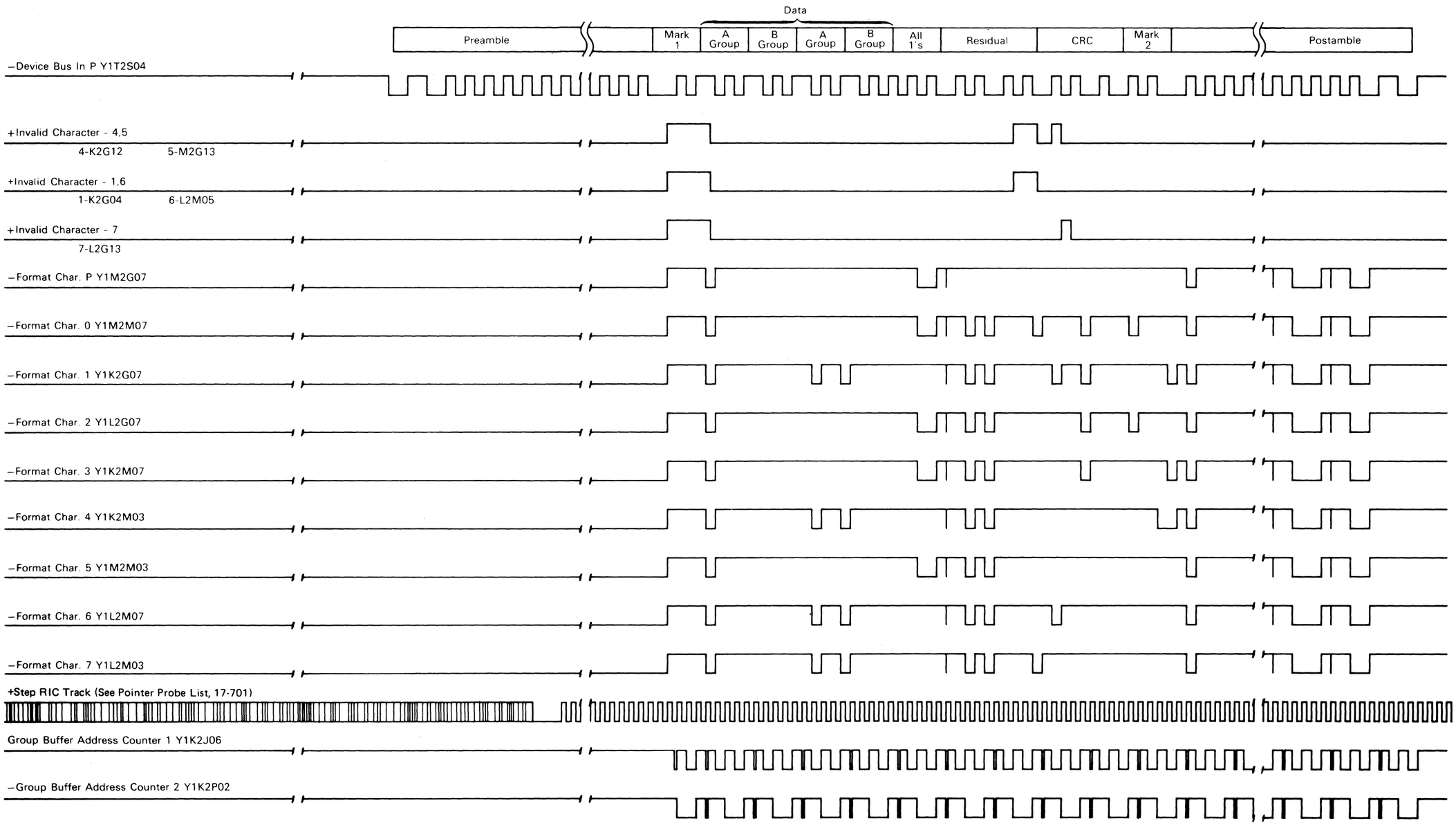
XF5200 Seq 2 of 2	**2735948** Part Number	**See EC History**	**845958** 1 Sep 79					

POINTER SYSTEM TIMING CHART - 6250



3803-2/3420

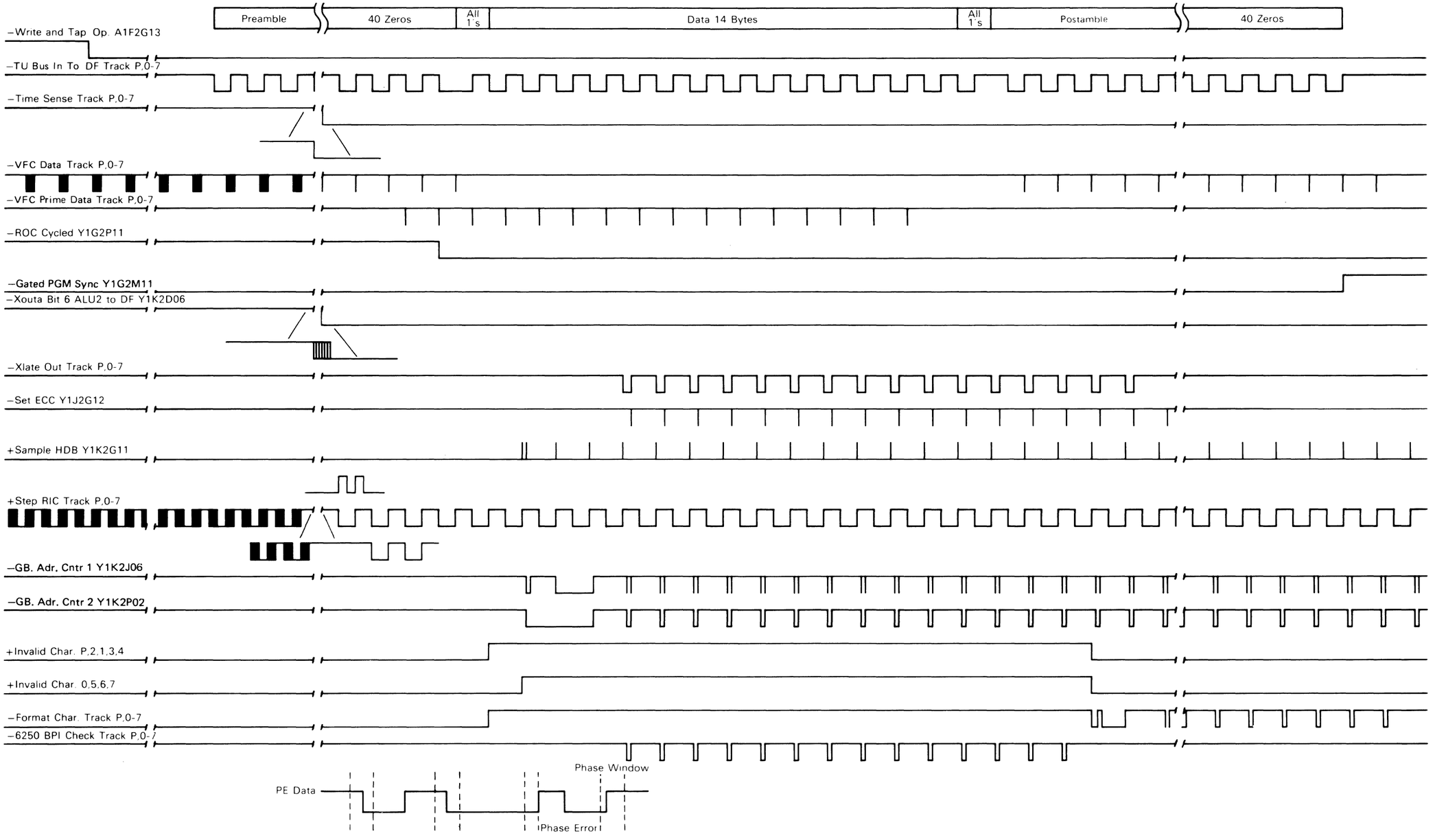
XF5300 Seq 1 of 2	2735949 Part Number	See EC History	845958 1 Sep 79					



3803-2/3420

XF5300 Seq 2 of 2	2735949 Part Number	See EC History	845958 1 Sep 79					

POINTER SYSTEM TIMING CHART - PE



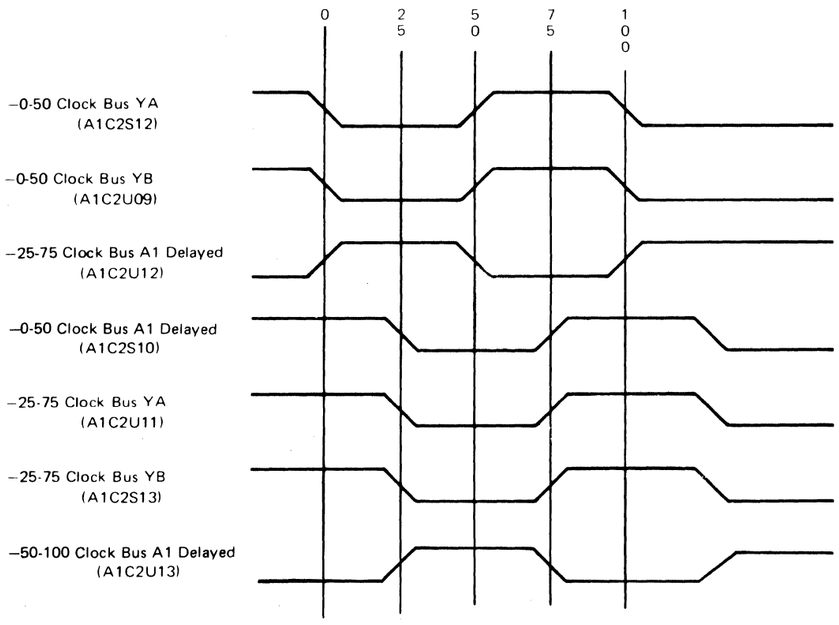
3803-2/3420

XF5400 Seq 1 of 2	2735950 Part Number	See EC History	845958 1 Sep 79	846927 20 Jun 80				

CLOCK CHECK

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problem or maintenance calls by going to MAP 00-030.		
Seq	**Condition/Instruction**	**Action**
1	Perform an LWR from the CE panel using any byte count and any density.	
2	Check all clock timings. If any are out of phase or fail to pulse, change card A1C2. Refer to Figure below. Sync on –0-50 CLOCK BUS YA (A1C2S12).	

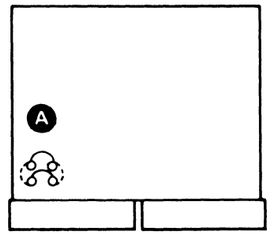
CLOCK TIMING CHART



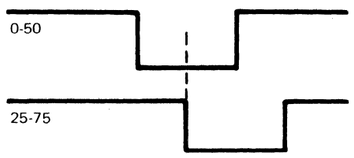
TYPE 2272 MST CARD ADJUSTMENT

Whenever a type 2272 MST card is replaced, the new card must be adjusted as follows:

1. Plug the jumpers horizontally as shown (A)



2. Sync oscilloscope on 0-50 CLOCK PULSE (A1C2S10) and scope 25-75 CLOCK PULSE (A1C2U12).
3. Compare the display obtained with the jumpers plugged horizontally, and the display obtained with the jumpers plugged vertically (as indicated by the broken lines on the above illustration). Determine which plugging arrangement gives the optimum centering of the two clock pulses and leave jumpers plugged that way.
4. The illustration shows the pulses ideally centered.



From: START 1, 15-010, 16-170, 16-171, 17-310

Note: If you have a 1x8 with address 8-F, change the address plugging to 0-7 before continuing (see 90-130). Return the address to 8-F before returning tape unit to the customer.

This procedure enables you to statically analyze solid access problems on a 1x8 (Selection) subsystem. Stopping ALU2 at FCHSNS in ALU2 microcode listing will allow static scoping of the first sense byte from the tape unit.

Setup:
Perform the following commands to the failing address:

Cmnd 1 = 8Bx
Cmnd 2 = 8Bx
Cmnd 3 = 8Bx
Cmnd 4 = 8Bx
Byte Count = FE0
Write Data = FF0

Jumper A1S2G08 to ground to write with gaps.
See 12-000 for CE panel operation.

Chart A on 18-001 provides the selection logic cards, outbound and inbound crosspoint (XPT) card, and device bus cables by tape unit address.

Notes:

1. Bit 7 requests tape unit sense byte 0. Bit 8 indicates DEV SELECT. TU SELECT lamp will not be on.
2. Bus In bit explanation.

   Bit 0 = Backward Bit 1 = Not File Protect Bit 2 = EOT Bit 3 = BOT Bit 4 = Write Status Bit 5 = Start (Ready) Bit 6 = Unit Check Bit 7 = Not Busy
3. A write command requires bits 1, 5, and 7 ON and bit 6 OFF. After the first Write, Backward is off and Write Status is on.

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise.
Remember to END all problem or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Set up ALU2 to stop on address 0F5. Set ROS Mode switch to STOP. Operate Set ROS Mode switch momentarily. Set COMPARE Register to 0F5. Set ALU1/ALU2 switch to ALU2. Set Display Select switch to IC.	
2	Operate START switch. Did ALU2 stop at 0F5?	Go to Seq 4.
3	If not:	Device is BUSY. Go to Seq 51.
4	Reset tape control and set COMPARE Register to 2E6 (FCHSNS). Set Display Select switch to IC.	
5	With ALU2 setup to stop at address 2E6 (FCHSNS), operate Start switch.	
6	With ALU2 at 2E6, turn Display Select switch to BUS OUT.	
7	Are data bits 0-7 OFF?	Go to Seq 9.
8		If not, any data bit ON at this time indicates an ALU2 problem. Recheck symptoms.
9	Do tag bits 8-11 = 1000?	Go to Seq 11.
10		If not, any other combination indicates an ALU2 problem. Recheck symptoms.
11	Set Display Select to BUS IN.	
12	Are data bits 0-7 all OFF?	Go to Seq 14.
13	Any data bits ON are 'hot' bits from the tape unit signal path. Scope failing lines using Charts D and E.	
14	Are tape unit address bits correct? Indicators 8-11.	Go to Seq 16.
15	If not:	Recheck setup.
16	Turn ROS Mode to STEP and operate Set ROS Mode switch momentarily. Operate Start or Step switch one time.	
17	You are now requesting tape unit sense byte 0. See Note 1.	
18	Set Display Select to BUS OUT.	
19	Do indicators 0-11 = 018 (Hex)?	Go to Seq 21.
20		If not, any other combination indicates an ALU2 problem. Recheck symptoms.
21	Set Display Select to BUS IN.	
22	Do bits 0-7 = D5 (hex)? (Sense byte 0.) See Notes 2 and 3.	Go to Seq 25.
23	Do bits 0-7 = 00?	Go to Seq 52.
24	Any other combination may indicate an XPT card or cable problem.	Go to Seq 53.
25	Are TU address bits 8-11 correct?	Go to Seq 27.
26	If not:	Recheck setup.
27	Turn ROS Mode rotary switch to Norm. Operate Set ROS Mode switch momentarily. Reset tape control and operate switch.	
28	Set Display Select switch to CE REG position. Set Data Entry to CMND1 position.	
29	Are lights flashing CB (hex)? **Note:** Lights seen are dependent on write data.	Go to Seq 43.
30	If the lights are not flashing, the command sequence set up is not running. Therefore, set ALU2 to stop on address 16C (MSKSTS). Turn ROS Mode rotary switch to Stop. Operate Set ROS Mode switch. Turn Display Select switch to IC.	
31	With ALU2 stopped at address 16C, set Display Select to BUS OUT.	
32	Do bits 0-11 = A0C?	Go to Seq 34.
33		If not, any other bit combination indicates an ALU2 problem. Recheck symptoms.
34	Set Display Select to BUS IN.	
35	Do data bits 0-7 = A0?	Go to Seq 37.
36	Any missing or extra bits may indicate an XPT card or cable failure. Be sure to check the Command tag.	Go to 16-160 for a status failure.
37	With ALU2 ROS still set to STOP, set COMPARE Reg to address 19B (LPNMOVE). Operate START switch.	
38	Turn ROS Mode to Step. Operate Set ROS Mode momentarily. Operate Start or Step one time.	
39	Set Display Select to BUS OUT.	
40	Do bits 0-11 = 009?	Go to Seq 42.
41		If not, any other combination indicates an ALU2 problem. Recheck symptoms.
42	Leave ALU2 IC at 19B and scope MOVE TAG (Indicator 11) at tape unit. Chart D provides scope point.	
43	Turn Display Select switch to Bus Out. Are data bits 0-7 flashing FF?	Go to Seq 45.
44		If not, should have set up data pattern of FF (all ones). Any missing bits may indicate a data flow problem. Recheck setup and symptoms.
45	Do tag bits 8-11 = 1101?	Go to Seq 47.
46	Any other combination indicates an ALU2 problem.	
47	Set Display Select to BUS IN.	
48	Are data bits 0-7 flashing FF?	Go to Seq 50.
49	Any missing bits would indicate a cable or XPT card problem. See 18-005, Charts D and E.	

X* SELECTION LOGIC

Seq	Condition/Instruction	Action
50	You are here because failure is intermittent or has disappeared. Scope inbound and outbound data lines for bad levels and slow responses. See charts on 18-001 and 18-005 for assistance.	
51	You are receiving a DEVICE BUSY from tape unit. Use Chart F to scope lines for your failing tape unit. Also refer to FT141 in tape unit logic.	Go to 00-030.
52	Ensure tape unit is online. Scope +INT DIS OR −OFFLINE (T-A1L6B03). Is it minus? (See FT910).	Possible FRUs: T-A1L6 TU to TC signal cable Go to Seq 54.
53	Use Charts D and E on 18-005 and scope failing BUS bit or bits.	
54	An incorrect SELECT XPT line can cause an offline identification. Use Chart C on 18-005 and scope for correct SELECT XPT, depending on TU address.	

Chart A: 1X8 Selection		
TU 0/8	Selection Logic	A2E2/A2D2
	Outbound XPT Card	B3S2 Type 5896
	Inbound XPT Card	B3D2 Type 5897
	Device Bus Out Cable	B3V2 to 01TA1C8
	Device Bus In Cable	B3A2 from 01TA1D8
TU 1/9	Selection Logic	A2E2/A2D2
	Outbound XPT Card	B3S2 Type 5896
	Inbound XPT Card	B3D2 Type 5897
	Device Bus Out Cable	B3V3 to 01TA1C7
	Device Bus In Cable	B3A3 from 01TA1D7
TU 2/A	Selection Logic	A2E2/A2D2
	Outbound XPT Card	B3S2 Type 5896
	Inbound XPT Card	B3D2 Type 5897
	Device Bus Out Cable	B3V4 to 01TA1C6
	Device Bus In Cable	B3A4 from 01TA1D6
TU 3/B	Selection Logic	A2E2/A2D2
	Outbound XPT Card	B3S2 Type 5896
	Inbound XPT Card	B3D2 Type 5897
	Device Bus Out Cable	B3V5 to 01TA1C5
	Device Bus In Cable	B3A5 from 01TA1D5
TU 4/C	Selection Logic	A2E2/A2D2
	Outbound XPT Card	B3Q2 Type 5896
	Inbound XPT Card	B3F2 Type 5897
	Device Bus Out Cable	B3U2 to 01TA1C4
	Device Bus In Cable	B3B2 from 01TA1D4
TU 5/D	Selection Logic	A2E2/A2D2
	Outbound XPT Card	B3Q2 Type 5896
	Inbound XPT Card	B3F2 Type 5897
	Device Bus Out Cable	B3U3 to 01TA1C3
	Device Bus In Cable	B3B3 from 01TA1D3
TU 6/E	Selection Logic	A2E2/A2D2
	Outbound XPT Card	B3Q2 Type 5896
	Inbound XPT Card	B3F2 Type 5897
	Device Bus Out Cable	B3U4 to 01TA1C2
	Device Bus In Cable	B3B4 from 01TA1D2
TU 7/F	Selection Logic	A2E2/A2D2
	Outbound XPT Card	B3Q2 Type 5896
	Inbound XPT Card	B3F2 Type 5897
	Device Bus Out Cable	B3U5 to 01TA1C1
	Device Bus In Cable	B3B5 from 01TA1D1

18-001

1X8 SELECTION LOGIC

Chart C: Select XPT 1x8			
Line Name (See Note 1)	Step 1	Step 2	Step 3
	Sel Logic Card A2D2 (XC511)	Cabling and Wiring	XPT Card
Select XPT 0	M05		B02
Select XPT 1	J09		G02
Select XPT 2	J06		M13
Select XPT 3	G13		S13
Select XPT 4	G08		B02
Select XPT 5	G10		G02
Select XPT 6	M10		M13
Select XPT 7	D06		S13

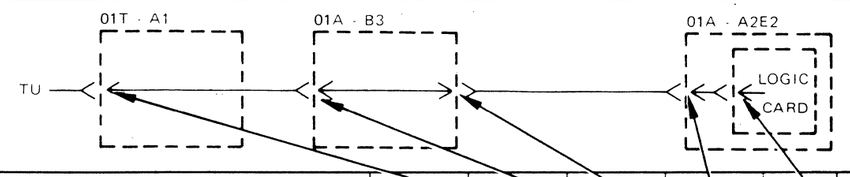
Chart E: Tape Control from Device					
	Step 1	Step 2	Step 3	Step 4	Step 5
Line Name		TC Device Bus In Cable	Output of Inbound XPT		TC Logic and Card Pin A2D2 Selection XC521
BUS IN 0		B02	P05		P05
BUS IN 1		D03	M07		D10
BUS IN 2		B04	P04		P10
BUS IN 3		D05	P06		M~~10~~ 12
BUS IN 4		B06	J13		D04
BUS IN 5		D07	G13		P04
BUS IN 6		D08	G12		J12
BUS IN 7		D09	J12		B04
BUS IN P		B10	D13		M03

Notes:

1. +0.2V Bit active to good line.
   +4.5V Bit inactive to good line.
   −0.1V Bit active to open line.
   +5.5V Bit inactive to open line.
2. +0.2V Active.
   +4.5V Inactive.

Chart D: Tape Control to Device						
	Step 1	Step 2	Step 3		Step 4	Step 5
Line Name	TC Logic and Card Pin A2E2 Selection XC601		Input to Outbound XPT		TC Device Bus Out Cable	
BUS OUT 0	G08		P05		B02	
BUS OUT 1	B03		M07		D03	
BUS OUT 2	B04		P04		B04	
BUS OUT 3	B12		P06		D05	
BUS OUT 4	D13		J13		B06	
BUS OUT 5	M07		G13		D07	
BUS OUT 6	M08		G12		B08	
BUS OUT 7	U11		J12		D09	
BUS OUT P	G07		D13		B10	
TAG A CNTRL	U12		B13		D11	
TAG B CMND	P10		D12		B12	
TAG C MOVE	S07		B12		D13	

Chart F: 1x8 Selection Logic



Dev	Line Name (See Note 2.) Device	SDI Switch	I/O 01T-A1	Board Cable Pin	Board Cable Pin	Board Cable Pin	Card Pin	Logic Page
0/8	Busy Tach In	Busy/Tach	C8G12	B3A2B12	B3B1C13	A2A3B06	U03	XC581
	Interrupt In	Dev End Intr	C8J11	B3A2D11	B3B1A13	A1A3B04	S12	XC581
	Meter Out	Run Meter	C8J13	B3A2D13	B3A1D13	A1A3B02	U09	XC601
1/9	Busy Tach In	Busy/Tach	C7G12	B3A3B12	B3C1D13	A2A3B12	J11	XC581
	Interrupt In	Dev End Intr	C7J11	B3A3D11	B3C1B13	A2A3B10	M03	XC581
	Meter Out	Run Meter	C7J13	B3A3D13	B3B1E13	A2A3B08	J12	XC601
2/A	Busy Tach In	Busy/Tach	C6G12	B3A4B12	B3B1D11	A2A3D07	U07	XC581
	Interrupt In	Dev End Intr	C6J11	B3A4D11	B3B1B11	A2A3D05	S05	XC581
	Meter Out	Run Meter	C6J13	B3A4D13	B3A1E11	A2A3D03	G12	XC601
3/B	Busy Tach In	Busy/Tach	C5G12	B3A5B12	B3C1E11	A2A3D13	D12	XC581
	Interrupt In	Dev End Intr	C5J11	B3A5D11	B3C1C11	A2A3D11	J13	XC581
	Meter Out	Run Meter	C5J13	B3A5D13	B3C1A11	A2A3D09	D06	XC601
4/C	Busy Tach In	Busy/Tach	C4G12	B3B2B12	B3E1D13	A2B3B06	M12	XC581
	Interrupt In	Dev End Intr	C4J11	B3B2D11	B3E1B13	A2B3B04	S02	XC581
	Meter Out	Run Meter	C4J13	B3B2D13	B3D1E13	A2B3B02	S03	XC601
5/D	Busy Tach In	Busy/Tach	C3G12	B3B3B12	B3F1E13	A2B3B12	J04	XC581
	Interrupt In	Dev End Intr	C3J11	B3B3D11	B3F1C13	A2B3B10	P03	XC581
	Meter Out	Run Meter	C3J13	B3B3D13	B3F1A13	A2B3B08	U02	XC601
6/E	Busy Tach In	Busy/Tach	C2G12	B3B4B12	B3F1E13	A2B3D07	U04	XC581
	Interrupt In	Dev End Intr	C2J11	B3B4D11	B3F1C13	A2B3D05	U06	XC581
	Meter Out	Run Meter	C2J13	B3B4D13	B3F1A13	A2B3D03	M02	XC601
7/F	Busy Tach In	Busy/Tach	C1G12	B3B5B12	B3G1A11	A2B3D13	B07	XC581
	Interrupt In	Dev End Intr	C1J11	B3B5D11	B3F1D11	A2B3D11	G04	XC581
	Meter Out	Run Meter	C1J13	B3B5D13	B3F1B11	A2B3D09	B05	XC601

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XF5550 Seq 1 of 2	8492609 Part Number	See EC History	845958 1 Sep 79	847298 15 Aug 83				

NOTES:

XF5550 Seq 2 of 2	8492609 Part Number	See EC History	845958 1 Sep 79	847298 15 Aug 83				

18-006

DEVICE SWITCH FEATURE

From: 16-180, 16-190, 16-212, 17-051,
17-080, 17-081, 17-160, 17-000

A device switching feature can be installed only in a "host" tape control; (a tape control with tape unit signal cables attached). A device switching feature allows the tape units attached to a host tape control to be accessed by one, two, or three additional tape controls, as well as by the host tape control.

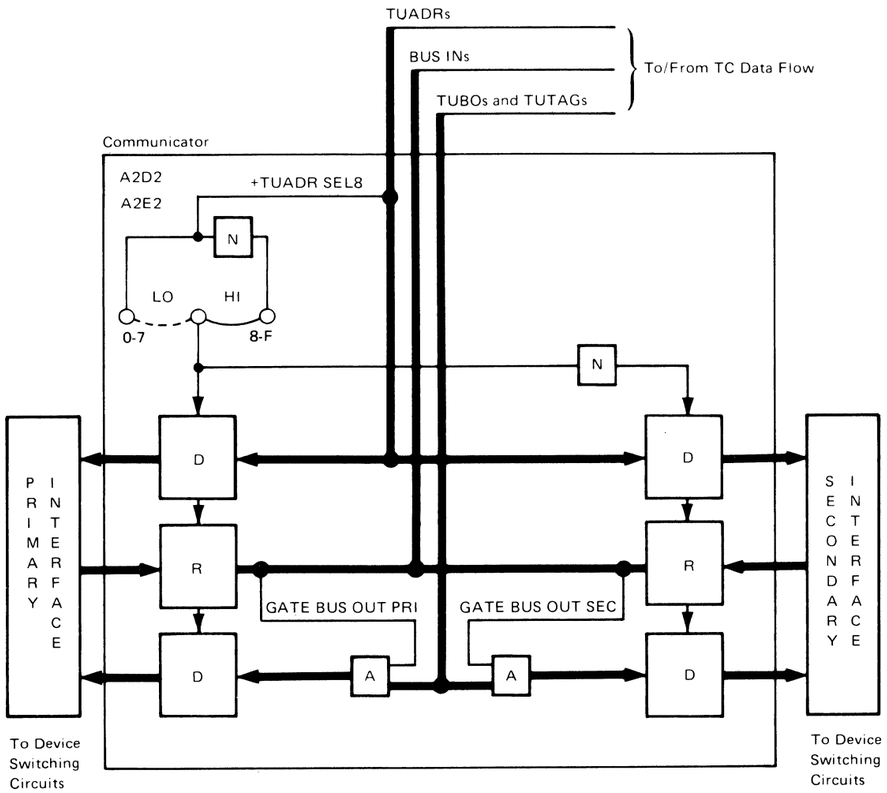
A communicator feature must be present in all tape controls, including the host tape control, to use a device switching feature. Each tape control with the communicator feature installed has two interfaces: a primary interface and a secondary interface. The primary interface is used to communicate with another tape control. The primary interface is always connected to tailgate positions 01TA1A7 (BUS) and 01TA1A8 (TAG).

The communicator feature includes a jumper that selects its primary interface to access tape unit addresses 0–7 ("Low") or 8–F ("High").

This jumper causes the TUADR SELECT 8 line to select the drivers and receivers of the correct interface, as shown. For example, if +TUADR SELECT 8 is active and the jumper is plugged for "High", the primary interface will access tape units 8–F, and the secondary interface will access tape units 0–7.

A host tape control always accesses attached tape units via its secondary interface. A tape control with a communicator feature installed but no tape units attached communicates with other tape controls via both its primary and secondary interfaces. After successful selection of a tape unit, the device switching circuits must return the GATE BUS OUT signal to the communicator before the operation can proceed.

Tape Subsystem Cabling Diagram



HOW TO USE SECTION 18-XXX

18-010 provides descriptions and basic ground rules for using sections 18-015 and 18-020.

18-015 is the Most Probable Cause. Analysis should be used first, to resolve a failure.

18-020 is a troubleshooting procedure to resolve a failure if Section 18-015 fails to do so.

FAILURE MODES

A. One tape control cannot access a certain tape unit or a certain combination of tape units.

B. Two or more tape controls cannot access a certain tape unit.

C. A control line or data line is failing from a certain tape control, to or from a certain tape unit.

1. Line is never active.
2. Line is always active.
3. Line has slow response.

D. Crosstalk or interference is occurring between two tape units operating concurrently from two tape controls.

E. Two tape units operate simultaneously from one tape control.

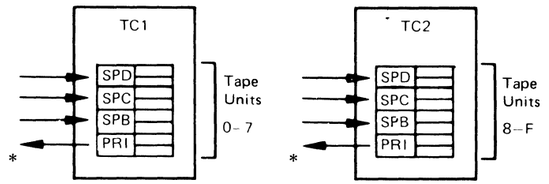
RULES AND DEFINITIONS

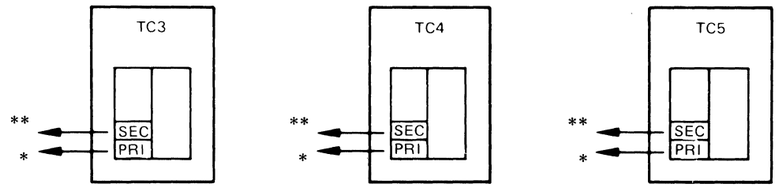
1. Because of the cabling and addressing flexibility provided by the device switching feature, the procedures reference switch paths with respect to the device switching capability of the host tape control. For example, a 4x8 configuration has four switch paths (SPs): SP-A (internal), SP-B, SP-C, and SP-D.
2. In this procedure:
   a. The tape control that hosts tape units 0-7 is called TC1.
   b. The tape control that hosts tape units 8-F is called TC2.
   c. A tape control that does not host tape units is called TC3, TC4, or TC5.
   d. The *operating* tape control is the tape control attempting to establish a switch path to perform an operation with a given tape unit.

TAPE SUBSYSTEM CABLING FOR THE DEVICE SWITCH FEATURE

1. A subsystem has a maximum of four tape controls cabled together using a device switch feature.
2. Cabling between tape controls must be known before the procedures on 18-015 or 18-020 can be used.
3. Tape control 1 (TC1) and tape units 0-7. The path to the device switch is internal via the SP-A circuits of tape control 1.
4. Tape control 2 (TC2) and tape units 8-F. The path to the device switch is internal via the SP-A circuits of tape control 2.
5. All other tape control to tape unit combinations (TC3, TC4 and TC5) have paths that include external cables from the tailgate of the operating tape control to the tailgate of the host tape control. To identify the switch path, check to see if the operating tape control is cabled to the SP-B, SP-C, or SP-D circuitry of the host tape control before using procedures 18-015 or 18-020.
6. An external switch path consists of two cables: a Bus cable and a Tag cable. Bus and Tag cables can be interchanged to isolate failures.
7. Make a drawing of the external switch path cabling for the subsystem at your location.
8. A subsystem cannot have more than four tape controls.

A maximum of four (4) tape controls can be cabled together using a device switch feature. See 90-050 through 90-080 (Installation section).





* These tailgate connectors (01TA1A7-BUS, 01TA1A6-TAG) are used by the primary interface of this tape control's communicator feature.

** These tailgate connectors (01TA1A5-BUS, 01TA1A6-TAG) are used by the secondary interface of this tape control's communicator feature.

CAUTION: After interchanging or replacing a card, always reset both the tape control and the tape unit before repeating the test procedure to verify a fix.

DEVICE SWITCH FEATURE (Cont'd)

DEVICE SWITCHING BLOCK DIAGRAM FOR 2x8 SWITCH

Tape control 1 (TC1) hosts tape units 0-7; Tape control 2 (TC2) hosts tape units 8-F.

Tape control Ⓑ operator panel switches must be ON to access these tape units.

A pair of cables Ⓒ connect the other tape control, via its communicator feature, to this device switch.

The indicated groups of tape units Ⓓ (0-2, 4-7; or 8-B, C-F) are associated with the card groups below them.

Each switch path (SP) Ⓔ through the device switch requires:

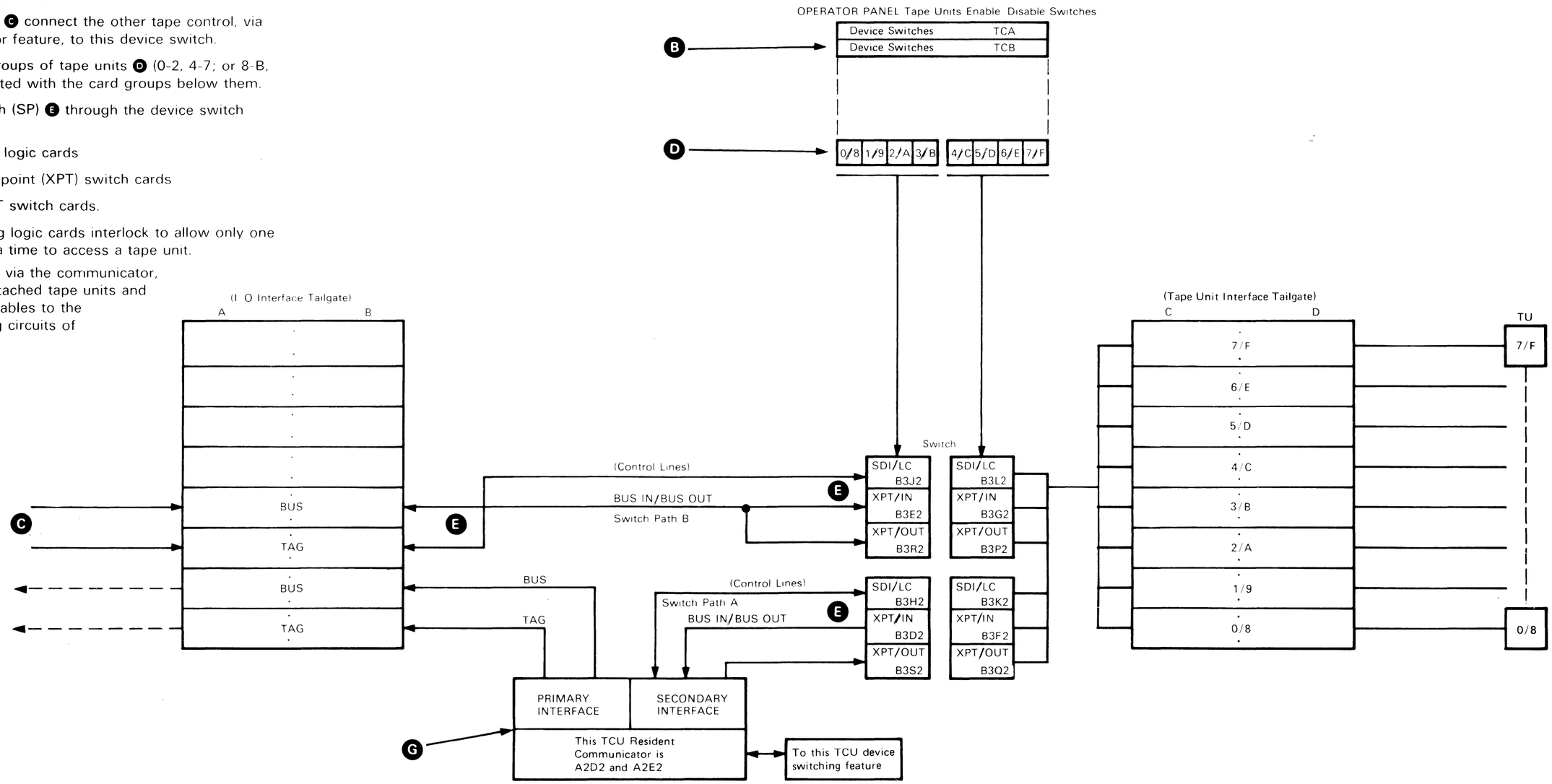
2-Device switch logic cards

2-Inbound crosspoint (XPT) switch cards

2-Outbound XPT switch cards.

Device switching logic cards interlock to allow only one tape control at a time to access a tape unit.

Tape control, Ⓖ via the communicator, accesses the attached tape units and the lower two cables to the device switching circuits of another 3803.



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XF5700 Seq 1 of 2	2735953 Part Number	See EC History	845958 1 Sep 79				

DEVICE SWITCH FEATURE (Cont'd)

DEVICE SWITCHING BLOCK DIAGRAM FOR 3x8 OR 4x8 SWITCH

Tape control 1 (TC1) hosts tape units 0-7; Tape control 2 (TC2) hosts tape units 8-F.

Tape control (B) operator panel switches must be ON to access these tape units.

Pairs of cables (C) connect other tape controls, via their resident communicators, to this device switch and the attached tape units.

The indicated groups of tape units (D) (0-3, 4-7; or 8-B, C-F) are associated with the card groups below them.

Each switch path (SP) (E) through the device switch requires:

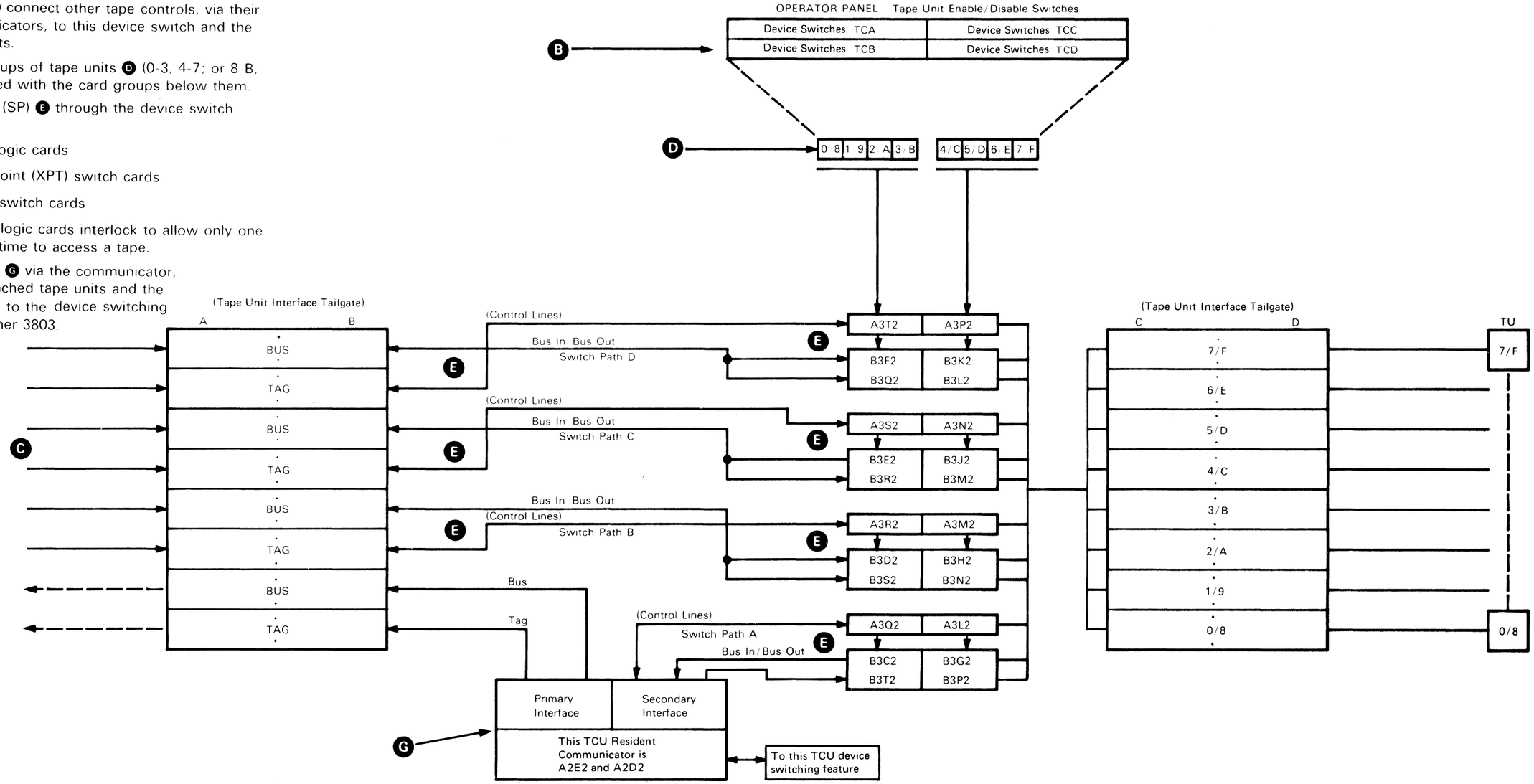
2-Device switch logic cards

2-Inbound crosspoint (XPT) switch cards

2-Outbound XPT switch cards

Device switching logic cards interlock to allow only one tape control at a time to access a tape.

This tape control, (G) via the communicator, accesses the attached tape units and the lower two cables to the device switching circuits of the other 3803.



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XF5700 Seq 2 of 2	2735953 Part Number	See EC History	845958 1 Sep 79					

From: START 1 15-010		
Note: If this MAP does not lead to fixing the problem, go to Map 18-019. If confused by tape path A, tape control 5, or host controller terminology, review 18-011, 18-012, 18-013.		
Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problem or maintenance calls by going to MAP 00-030.		
Seq	**Condition/Instruction**	**Action**
1	Does **only one** tape unit operate correctly and **all** others fail in the low order address group (0-7)?	Go to Seq 9.
2	Does **only one** tape unit operate correctly and **all** others fail in the high order address group (8-F)?	Go to Seq 9.
3	Is only **one** tape unit failing?	Go to Seq 13.
4	Are only **two** tape units failing?	Go to Seq 17.
5	Are only **four** tape units failing?	Go to Seq 24.
6	Are only **eight** tape units failing?	Go to Seq 31.
7	Are all **sixteen** tape units failing?	Go to Seq 36.
8	All other combinations of tape units failing.	Go to 18-020.
9	Is the tape unit failing from only one operating tape control?	Go to Seq 11.
10	Is the tape unit failing from more than one operating tape control?	Go to Seq 87.
11	Does the tape unit that is operating correctly have an address in groups 0-3 or 8-B?	If 2x8 device switch, go to Seq 78. If 3x8 or 4x8 device switch, go to Seq 37.
12	Does the tape unit that is operating correctly have an address in groups 4-7 or C-F?	If 2x8 device switch, go to Seq 83. If 3x8 or 4x8 device switch, go to Seq 41.
13	Is the tape unit failing from only one tape control?	Go to Seq 15.
14	Is the tape unit failing from two or more tape controls?	Go to Seq 57.
15	Does the failing tape unit have an address in groups 0-3 or 8-B?	If 2x8 device switch, go to Seq 77. If 3x8 or 4x8 device switch, go to Seq 37.
16	Does the failing tape unit have an address in groups 4-7 or C-F?	If 2x8 device switch, go to Seq 82. If 3x8 or 4x8 device switch, go to Seq 41.
17	Are the two tape units failing from only one tape control?	Go to Seq 19.
18	Are the two tape units failing from two or more tape controls?	Go to Seq 47.
19	Are the two failing tape units attached to one host tape control?	Go to Seq 21.
20	If not:	Go to Seq 45.

Seq	Condition/Instruction	Action
21	Do the two failing tape units have addresses in groups 0-3 or 8-B?	If 2x8 device switch, go to Seq 78. If 3x8 or 4x8 device switch, go to Seq 37.
22	Do the two failing tape units have addresses in groups 4-7 or C-F?	If 2x8 device switch, go to Seq 83. If 3x8 or 4x8 device switch, go to Seq 41.
23	If not:	Go to Seq 46.
24	Are the four tape units failing from only one tape control?	Go to Seq 26.
25	Are the four tape units failing from two or more tape controls?	Go to Seq 47.
26	Are all four failing tape units attached to one host tape control?	Go to Seq 28.
27	If not:	Go to Seq 45.
28	Do the four failing tape units have addresses in groups 0-3 or 8-B?	If 2x8 device switch, go to Seq 78. If 3x8 or 4x8 device switch, go to Seq 37.
29	Do the four failing tape units have addresses in groups 4-7 or C-F?	If 2x8 device switch, go to Seq 83. If 3x8 or 4x8 device switch, go to Seq 41.
30	If not:	Go to Seq 46.
31	Are the eight tape units failing from only one tape control?	Go to Seq 33.
32	Are the eight tape units failing from two or more tape controls?	Go to Seq 35.
33	Are the eight failing tape units attached to one host tape control?	Change: 1. A2E2 in operating tape control. 2. External cable from operating tape control. 3. A2P2, A2P3 4. A2D2 in operating tape control.
34	Are the eight failing tape units attached to two different host tape controls?	Change: 1. A2E2 in operating tape control. 2. A2D2 in operating tape control.
35	Are all eight failing tape units attached to one host tape control?	Check power on host tape control. Change: A2E2, A2D2
36	Are all sixteen tape units failing from only one tape control?	Change: 1. A2E2 in operating tape control. 2. A2P2, A2P3 3. A2D2 in operating tape control.
37	Is the operating tape control using switch path A of the host tape control?	Change: 1. A3Q3 of host tape control. 2. B3C2 of host tape control. 3. B3T2 of host tape control.
38	Is the operating tape control using switch path B of the host tape control?	Change: 1. A3R2 of host tape control. 2. B3D2 of host tape control. 3. B3S2 of host tape control.

Seq	Condition/Instruction	Action
39	Is the operating tape control using switch path C of the host tape control?	Change: 1. A3S2 of host tape control. 2. B3E2 of host tape control. 3. B3R2 of host tape control.
40	Is the operating tape control using switch path D of the host tape control?	Change: 1. A3T2 of host tape control. 2. B3F2 of host tape control. 3. B3Q2 of host tape control.
41	Is the operating tape control using switch path A of the host tape control?	Change: 1. A3L2 of host tape control. 2. B3G2 of host tape control. 3. B3P2 of host tape control.
42	Is the operating tape control using switch path B of the host tape control?	Change: 1. A3M2 of host tape control. 2. B3H2 of host tape control. 3. B3N2 of host tape control.
43	Is the operating tape control using switch path C of the host tape control?	Change: 1. A3N2 of host tape control. 2. B3J2 of host tape control. 3. B3M2 of host tape control.
44	Is the operating tape control using switch path D of the host tape control?	Change: 1. A3P2 of host tape control. 2. B3K2 of host tape control. 3. B3L2 of host tape control.
45	Go to ACTION column.	Change: A2E2 of operating tape control. A2D2 of operating tape control.
46	Go to ACTION column.	Change: 1. A2E2 of operating tape control. 2. External cable from operating tape control. 3. A2D2 of operating tape control.
47	Are the tape units failing from tape control 1? **Note:** If tape control 1 is not present, go to Seq 49.	Go to Seq 49.
48	If not:	Change: 1. A2E2 of tape control 1. 2. External cable from tape control 1. 3. A2D2 of tape control 1.
49	Are the tape units failing from tape control 2? **Note:** If tape control 2 is not present, go to Seq 51.	Go to Seq 51.
50	If not:	Change: 1. A2E2 of tape control 2. 2. External cable from tape control 2. 3. A2D2 of tape control 2.
51	Are the tape units failing from tape control 3? **Note:** If tape control 3 is not present, go to Seq 53.	Go to Seq 53.
52	If not:	Change: 1. A2E2 of tape control 3. 2. External cable from tape control 3. 3. A2D2 of tape control 3.

DEVICE SWITCHING FEATURE —MOST PROBABLE CAUSE ANALYSIS (Cont'd)

Seq	Condition/Instruction	Action
53	Are the tape units failing from tape control 4? **Note:** If tape control 4 is not present, go to Seq 55.	Go to Seq 55.
54	If not:	Change: 1. A2E2 of tape control 4. 2. External cable from tape control 4. 3. A2D2 of tape control 4.
55	Are the tape units failing from tape control 5? **Note:** If tape control 5 is not present, go to 18-020.	Go to 18-020.
56	If not:	Change: 1. A2E2 of tape control 5. 2. External cable from tape control 5. 3. A2D2 of tape control 5.
57	Is the tape unit failing from tape control 1? **Note:** If tape control 1 is not present, go to Seq 59.	Go to Seq 59.
58	If not:	Go to Seq 67.
59	Is the tape unit failing from tape control 2? **Note:** If tape control 2 is not present, go to Seq 61.	Go to Seq 61.
60	If not:	Go to Seq 67.
61	Is the tape unit failing from tape control 3? **Note:** If tape control 3 is not present, go to Seq 63.	Go to Seq 63.
62	If not:	Go to Seq 67.
63	Is the tape unit failing from tape control 4? **Note:** If tape control 4 is not present, go to Seq 65.	Go to Seq 65.
64	If not:	Go to Seq 67.
65	Is the tape unit failing from tape control 5? **Note:** If tape control 5 is not present, go to 18-020.	Go to 18-020.
66	If not:	Go to Seq 67.
67	Does the tape unit have an address in groups 0-3, or 8-B?	Go to Seq 69.
68	Does the tape unit have an address in groups 4-7 or C-F?	Go to Seq 73.
69	Is the operating tape control using switch path A of the host tape control?	Change A3Q2 of host tape control.
70	Is the operating tape control using switch path B of the host tape control?	Change A3R2 of host tape control.
71	Is the operating tape control using switch path C of the host tape control?	Change A3S2 of host tape control.
72	Is the operating tape control using switch path D of the host tape control?	Change A3T2 of host tape control.
73	Is the operating tape control using switch path A of the host tape control?	Change A3L2 of host tape control.
74	Is the operating tape control using switch path B of the host tape control?	Change A3M2 of host tape control.
75	Is the operating tape control using switch path C of the host tape control?	Change A3N2 of host tape control.
76	Is the operating tape control using switch path D of the host tape control?	Change A3P2 of host tape control.
77	Is the tape unit BUSY? (See Note.)	Go to Seq 80.
78	Is the operating tape control using switch path A of the host tape control?	Change: 1. B3H2 of host tape control. 2. B3D2 of host tape control. 3. B3S2 of host tape control.
79	Is the operating tape control using switch path B of the host tape control?	Change: 1. B3J2 of host tape control. 2. B3E2 of host tape control. 3. B3R2 of host tape control.
80	Is the operating tape control using switch path A of the host tape control?	Change: B3J2 of host tape control.
81	Is the operating tape control using switch path B of the host tape control?	Change: B3H2 of host tape control.
82	Is the tape unit BUSY? (See Note.)	Go to Seq 85.
83	Is the operating tape control using switch path A of the host tape control?	Change: 1. B3K2 of host tape control. 2. B3F2 of host tape control. 3. B3Q2 of host tape control.
84	Is the operating tape control using switch path B of the host tape control?	Change: 1. B3L2 of host tape control. 2. B3G2 of host tape control. 3. B3P2 of host tape control.
85	Is the operating tape control using switch path A of the host tape control?	Change: B3L2 of host tape control.
86	Is the operating tape control using switch path B of the host tape control?	Change: B3K2 of host tape control.
87	Suspect a short between two switch paths on the communicator side of the host tape control's device switch.	

Note: The Device Busy bit is bit 35 in the channel status word.

18-016

NOTES:

3803-2/3420

XF5850 Seq 1 of 2	8492856 Part Number	See EC History	845958 1 Sep 79				

From: 18-015

The type of device switch used determines the chart page reference. 1. Charts for 1x8 selection logic are located on 18-001. 2. Charts for 2x8, 3x8, and 4x8 selection logic start on 18-028.

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problem or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Are you entering this procedure with an interrupt problem?	Go to Seq 295.
2	Are you entering this procedure with a tach start problem?	Go to Seq 295.
3	Are you entering this procedure with a meter problem?	Go to Seq 295.
4	Are you entering this procedure with a control command problem?	Go to Seq 295.
5	Mount a CE work tape on one of the failing tape units. Load and Ready the tape unit.	
6	Take the tape control **offline**, and set up the CE panel to do multiple LWR (8B) commands at load point, using the failing tape unit. Use Byte Cnt = FE0 Write Data and Go Down = FF0 Reset the tape control. **Note**: Connect LWR jumper from A1S2G08 to ground.	
7	Set up an ALU2 COMPARE STOP on 0F5 (EXECSTSZ) (See 12-011) and operate the Start switch.	
8	Did it stop at 0F5?	Go to Seq 10.
9	If not:	TU BUSY response received. Go to Seq 62.
10	Turn the ROS Mode switch to Normal, then operate the Reset switch.	
11	Set up an ALU2 COMPARE STOP at 2E6 (FCHSNS) (See 12-011) and operate the Start switch.	
12	Set Display Select switch to Bus Out and the ALU1/ALU2 switch to ALU2.	
13	Are data bits 0-7 all Off?	Go to Seq 15.
14	Any data bit 0-7 On indicates an ALU2 problem.	
15	Do tag bits 8-11 = 1000?	Go to Seq 17.
16	Any other bit combination indicates an ALU2 problem.	
17	Set Display Select switch to Bus In and the ALU1/ALU2 switch to ALU2.	
18	Are tape unit data bits 0-7 all Off?	Go to Seq 20.
19	Any tape unit data bits that are On are "hot" bits from the tape unit signal path.	Go to Seq 89.
20	Are tape unit address bits 8-11 correct?	Go to Seq 22.
21	If not:	Go to Seq 6.
22	Turn ROS Mode switch to Step and step one time.	
23	This requests Sense Byte 0.	
24	Set Display Select switch to Bus Out and the ALU1/ALU2 switch to ALU2.	
25	Do bits 0-11 = hex 018?	Go to Seq 27.
26	Any other bit combination indicates an ALU2 problem.	
27	Set Display Select switch to Bus In and the ALU1/ALU2 switch to ALU2.	
28	Do bits 0-7 = D5 (Sense Byte 0)?	Go to Seq 31.
29	Are bits 0-7 all OFF?	Go to Seq 62.
30	Any other bit combination may indicate an XPT card or cable problem.	Go to Seq 109.
31	Are TU address bits 8-11 correct?	Go to Seq 33.
32	Has the setup been changed?	Go to Seq 6.
33	Turn ROS Mode switch to Normal, then operate Reset switch and operate Start switch.	
34	Set Display Select switch to CE Reg and Data Entry Select switch to Cmd1.	
35	Are lights flashing hex CB?	Go to Seq 37.
36	If lights are not flashing, command sequence you set up is not running. If lamps are flashing but not showing CB, tape control is not performing an LWR.	Go to Seq 46.
37	Set Display Select switch to Bus Out and the ALU1/ALU2 switch to ALU2.	
38	Do data bits 0-7 = hex FF?	Go to Seq 40.
39	In Seq 6, you should have set up an FF data pattern. This may be a data flow problem.	Go to Seq 6.
40	Do tag bits 8-11 = hex D (1101)?	Go to Seq 42.
41	If not, this is an ALU2 problem.	
42	Set Display Select switch to Bus In and the ALU1/ALU2 switch to ALU2.	
43	Do tape unit data bits 0-7 = hex FF?	Go to Seq 45.
44	Any missing bits may indicate an XPT card or cable problem.	Go to Seq 109.
45	Are there intermittent failures? Go to Seq 109 and scope the inbound and outbound data lines for slow	response, noise, and incorrect levels.
46	The command sequence set up is not running.	
47	Reset the tape control.	
48	Set up an ALU2 COMPARE STOP on 16C (MSKSTS) (See 12-011) and operate the Start switch.	
49	Set Display Select switch to Bus Out and the ALU1/ALU2 switch to ALU2.	
50	Do bits 0-11 = hex A0C?	Go to Seq 52.
51	Any other bit combination indicates an ALU2 problem.	
52	Set Display Select switch to Bus In and the ALU1/ALU2 switch to ALU2.	
53	Do tape unit data bits 0-7 = hex A0?	Go to Seq 55.
54	Any missing or extra bits may indicate an XPT card or cable failure. Be sure to check the command tag.	Go to Seq 109.
55	Turn ROS Mode switch to Normal mode and operate the Reset switch.	
56	Set up an ALU2 COMPARE STOP on 19B (LPNMOVE) (See 12-011) and operate the Start switch.	
57	Set ROS Mode switch to Step and step one time.	
58	Set Display Select switch to Bus Out and ALU1/ALU2 switch to ALU2.	
59	Do bits 0-11 = hex 009?	Go to Seq 61.
60	Any other bit combination indicates an ALU2 problem.	
61	Go to Seq 109 and check that the Move tag (bit 11) is going to the tape unit.	
62	Ensure the tape unit is online. T-A1L6B03 must be at −4V (FT910).	Go to Seq 63.
63	Is this a 2x8, 2x16, 3x8, 3x16, 4x8, or a 4x16 device switch?	Go to Seq 65
64	You don't have a device switch.	Go to 00-010

Seq	Condition/Instruction	Action
65	Use the following information to determine the location of the device switch logic and XPT cards that are being used: Tape Subsystem Cabling Diagram — 18-010 2x8 Device Switch Block Diagram — 18-012 3x8 or 4x8 Device Switch Block Diagram — 18-013. Examples: A. If TC1 is offline and is addressing TU address 2 through a 2x8 switch: Device switch logic card is B3H2 in TC1. XPT/IN is B3D2 in TC1. XPT/OUT is B3S2 in TC1. B. If TC3 is offline and is addressing TU address D via SP-C of TC2 through a 4x8 device switch: Device switch logic card is A3N2 in TC2 XPT/IN is B3J2 in TC2 XPT/OUT is B3M2 in TC2.	
66	Remember the device switch logic card and XPT cards determined in Seq 65.	
67	**Caution:** In the next sequences, you may be scoping in a tape control that is online.	
68	Was Seq 62 entered from Seq 9 (Busy)?	Go to Seq 209.
69	Was Seq 62 entered from Seq 308?	Go to Seq 309.
70	On the device switch logic card determined in step 65: (..... 3 .... in tape control .....), scope only the pins that correspond to the tape unit being tested for the level indicated. When a level is wrong, go to the step indicated at the bottom of that column. See charts D, E, F, and G at end of Map. Were all levels correct?	Go to Seq 71.
71	All line levels are correct to set the Committed latch for this tape unit, but it is not set On. A. Check the socket contacts carefully for this device switch logic card. B. Check the address jumpers carefully for correct plugging and good contact on this device switch logic card. See 90-1xx, and ALD AA004, Sheet 2. C. When interchanging device switch logic cards to isolate failures, check the address jumpers for correct plugging. D. A3Q2 and A3L2 are load cards for 3x8 and 4x8 device switches. E. B3H2 and B3K2 are load cards for 2x8 device switches.	
72	A tape unit address bit is not received at the correct level for the tape unit being tested by the device switch logic card.	
73	These address bit lines come from communicator card A2E2 in the operating tape control.	

Line Names for Reference to ALD XC70x Charts D, E, F, and G

	Tape Control Power Down	Committed	Enable Switches	Add Bit 1	Add Bit 2	Add Bit 4	Add Bit 8	Device Select	3x8 or 4x8 (pre) Committed	3x8 or 4x8 (pre) Committed	3x8 or 4x8 (pre) Committed	2x8 (pre) Committed
	+4.5 / 0	−.8 / −1.8	−.5 / −4.0	+4.5 / +.5	+4.5 / +.5	+4.5 / +.5	+4.5 / +.5	+4.5 / +.5	−.8 / −1.8	−.8 / −1.8	−.8 / −1.8	−.8 / −1.8
0	B02+	P04−	G08−	U11+	U12+	U07+	U06+	P03−	U02−	S02−	U04−	U02−
1	B02+	P05−	J09−	U11−	U12+	U07+	U06+	P03−	U05−	S04−	S05−	U05−
2	B02+	M02−	D13−	U11+	U12−	U07+	U06+	P03−	P11−	P13−	P12−	P11−
3	B02+	M03−	B13−	U11−	U12−	U07+	U06+	P03−	M08−	M12−	M10−	M08−
									3X-4X only			2X8
4	B02+	P04−	G08−	U11+	U12+	U07−	U06+	P03−	U02−	S02−	U04−	U02−
5	B02+	P05−	J09−	U11−	U12+	U07−	U06+	P03−	U05−	S04−	S05−	U05−
6	B02+	M02−	D13−	U11+	U12−	U07−	U06+	P03−	P11−	P13−	P12−	P11−
7	B02+	M03−	B13−	U11−	U12−	U07−	U06+	P03−	M08−	M12−	M10−	M08−
									3X-4X only			2X8
8	B02+	P04−	G08−	U11+	U12+	U07+	U06−	P03−	U02−	S02−	U04−	U02−
9	B02+	P05−	J09−	U11−	U12+	U07+	U06−	P03−	U05−	S04−	S05−	U05−
A	B02+	M02−	D13−	U11+	U12−	U07+	U06−	P03−	P11−	P13−	P12−	P11−
B	B02+	M03−	B13−	U11−	U12−	U07+	U06−	P03−	M08−	M12−	M10−	M08−
									3X-4X only			2X8
C	B02+	P04−	G08−	U11+	U12+	U07−	U06−	P03−	U02−	S02−	U04−	U02−
D	B02+	P95−	J09−	U11−	U12+	U07−	U06−	P03−	U05−	S04−	S05−	U05−
E	B02+	M02−	D13−	U11+	U12−	U07−	U06−	P03−	P11−	P13−	P12−	P11−
F	B02+	M03−	B13−	U11−	U12−	U07−	U06−	P03−	M08−	M12−	M10−	M08−
Go to Seq	80	81	79	72	72	72	72	75	78	78	78	78

Seq	Condition/Instruction	Action
74	Remember this sequence number.	Go to Seq 136.
75	DEVICE SELECT not received at the device switch logic card.	
76	DEVICE SELECT comes from communicator card A2E2 in the operating tape control.	
77	Remember this sequence number.	Go to Seq 136.
78	This tape unit is committed to another tape control.	Go to Seq 215.
79	A. Check the Operator Panel Enabled switch. B. Test switch operation. C. Go to ALD XC700 Sheet 1 Chart E for cabling on 2x8 device switches. D. Go to ALD XC701 Sheet 3 Chart E for cabling on 3x8 or 4x8 device switches.	
80	There is a POWER DOWN signal from the operating tape control.	Go to Seq 136.
81	The COMMITTED latch has been set correctly.	
82	The line that sets the COMMITTED latch leaves the device switch logic card as GATE BUS OUT and must be returned to communicator card A2E2 in the operating tape control to allow the gating of the TAGs and BUS OUT lines.	
83	Remember this sequence number.	Go to Seq 136.
84	On the device switch logic card you identified in Seq 65, scope GATE BUS OUT (pin B04).	
85	Is pin B04 at +0.2v?	Go to Seq 88.
86	Is pin B04 at ground level?	Go to Seq 163.
87	If pin B04 is at +4.5Vdc A. Check the socket connections on the device switch logic card identified in Seq 65. B. Replace the device switch logic card, making sure the address jumpers are plugged correctly.	
88	Determine if BUS OUT BIT 7 is present at the tape unit.	Go to Seq 109. line that is at ground level is shorted or open at both ends.
		Find and correct such a problem before proceeding.
89	Go to Chart A (see note) and record the cards and cables needed to use the following procedures. Return to Seq 90.	
90	Is there more that one "hot" bit?	Go to Seq 100.

Seq	Condition/Instruction	Action
91	Go to Chart E, Device to Tape Control, pick the BUS IN that was "hot" and go to Step 2 of the chart. Is the corresponding pin active? (See Note.)	Go to Seq 102.
92	Is the corresponding pin in Chart E, Step 3, active? (See Note.)	Go to Seq 95.
93	Is the corresponding pin in Chart E, Step 5, active? (See Note.)	Go to Seq 97.
94	This is not a switch problem. Go to Chart E Step 5 (see note) for the XC ALD page.	
95	Remove the inbound XPT card. Is the line in Seq 92 still active?	Go to Seq 97.
96	Change the inbound XPT card.	
97	Reinstall the inbound XPT card. Remove the A2D2 card. Is the line in Seq 92 still active?	Go to Seq 99.
98	Change the A2D2 card.	
99	Reinstall card A2D2 and check the cabling in Chart E, Step 4 (see Note), for shorts and opens.	
100	Go to Chart D, Tape Control to Device (see Note). Are any BUS OUT bits active that should not be active in Step 4?	Go to Seq 103.
101	If not:	Go to Seq 107.
102	1. Check Chart E, Step 1 for cabling (see Note). 2. Check the "device" and "external device" cabling. 3. Check Chart E, Steps 1 and 2 (see Note), for shorted cables and pins. 4. Pull the associated inbound XPT cards for that device.	
103	Is the corresponding pin in Chart D, Step 3 active? (See Note.)	Go to Seq 106.
104	Scope corresponding pin in Chart D, Step 4 (see note) Does pin go inactive when you a. Pull the associated outbound XPT card. b. Pull all the associated XPT cards for that device?	
105	Check the cabling in Chart G, Step 4, (see Note). Check for shorted cables and pins. Replace or repair as required.	
106	Is the corresponding pin in Chart D, Step 1, active? (See Note.)	Go to Seq 108.
107	Check the cabling in Chart D, Step 2 (see Note), for shorts and opens.	

Seq	Condition/Instruction	Action
108	Go to the corresponding XC ALD page referenced in Chart D, Step 1 (see Note).	
109	Go to Chart A (see Note) and record the cards and cables needed to use the following procedures. Return at Seq 110.	
110	Go to Chart C for 1x8 selection logic; or Chart B for 2X8, 3X8, or 4X8 device switches. Is the pin active in Step 3 of this chart for the device you are on? (See Note.)	Go to Seq 114.
111	Is the pin in Step 1 of Chart B active?	Go to Seq 113.
112	If not:	Go to Seq 290.
113	For a 3x8 or 4x8 device switch, you must have a cabling problem. See Chart B, Step 2. For a 2x8 device switch, problem must be a broken land. (See Note.)	
114	Go to Chart D, Tape Control to Device. Pick the BUS or TAG lines that should be active, and make sure all other BUS and TAG lines in Step 4 of this chart are Inactive. (See Note.)	
115	Are any BUS or TAG lines active that should not be?	Go to Seq 103.
116	Are all BUS or TAG lines active that should be?	Go to Seq 124.
117	Are all BUS or TAG lines active that should be? See Chart G, Step 3 (see Note).	Go to Seq 120.
118	Are all BUS or TAG lines active that should be? See Chart G, Step 1 (see Note).	Go to Seq 123.
119	See Chart D, Step 1 (see Note), for the XC ALD page to go to.	
120	Put another outbound XPT card in this position. Is the corresponding pin in Chart D, Step 4, still active? (See Note.)	Go to Seq 122.
121	Go to Chart D, Step 5, to check for possible broken land (see Note).	
122	Change the bad outbound XPT card.	
123	This must be a cabling problem. Go to Chart D, Step 2. (See Note.)	
124	Go to Chart E, Device to Tape Control (see Note). Are the correct BUS IN line(s) active?	Go to Seq 126.
125	This must be a cabling problem. Go to Chart E, Step 1 (see Note).	
126	Go to Chart E, Step 3 (see Note). Are the correct BUS IN line(s) active?	Go to Seq 132.

DEVICE SWITCHING FEATURE —TROUBLESHOOTING PROCEDURE (Cont'd)

Seq	Condition/Instruction	Action
127	See Chart B on 18–028 for 2x8, 3x8, 4x8 device switch. Is the pin active for the device you are on?	Go to Seq 129.
128	There is a broken land on this panel. Go to Step 2 of this chart (see Note).	
129	Put another inbound XPT card in this position. Is the corresponding pin in Chart E, Step 3, active now? (See Note.)	Go to Seq 131.
130	Go to Chart E, Step 4, to check for possible broken land. (See Note.)	
131	Change the bad inbound XPT card.	
132	Go to Chart E, Step 5 (see Note). Are the correct BUS IN line(s) active?	Go to Seq 134.
133	This must be a cabling problem. Go to Chart E, Step 4 (see Note).	
134	Go to the corresponding XC ALD page in Chart E, Step 5 (see Note).	
135	A. Entering this Seq indicates a possible cable problem. B. The card and pin number associated with this problem is known. C. Go to the proper chart on 18-010 to check the line through the cables to or from this pin.	
136	Before proceeding to scope communicator card, you must know if you are using its primary interface or its secondary interface. References: A. 18-010 – Tape Subsystem Cabling, and 18-012, and 18-013 for Device Switch Block Diagrams. B. ALD AA004, Sheet 2 – A2E2 card. C. 90-040.	

Note: Charts for 1x8 selection logic are located on 18-001. Charts for 2x8, 3x8 and 4x8 start on 18-028. 135

Seq	Condition/Instruction	Action
137	**Output line driver levels for communicator and device switch cards:** A. Inactive level; +4.5V.  B. Active level; +0.2V. C. If there is an open circuit between the line driver and the line receiver, the output pin will be at ground when the line driver is active. D. If the line driver is not active, the output pin may be at –1.5V with an open circuit to the line receiver. **Input levels at line receivers:** A. Inactive level; +4.5V.  B. Active level; +0.5V.	
138	Was Seq 136 entered from Seq 74?	Go to Seq 142.
139	Was Seq 136 entered from Seq 77?	Go to Seq 164.
140	Was Seq 136 entered from Seq 80?	Go to Seq 196.
141	Was Seq 136 entered from Seq 83?	Go to Seq 84.
142	Is the Secondary Interface of the communicator card in the operating tape control being used?	Go to Seq 150.
143	Scope the Primary Interface device address output lines at the communicator card in the operating tape control.	
144	Scope the line driver output corresponding to the incorrect address line found at the device switch logic card in Seq 70, for the same wrong level.	
145	Communicator card A2E2 pins: J12—Device Address 8 Primary U07—Device Address 4 Primary U03—Device Address 2 Primary S05—Device Address 1 Primary	
146	Is the corresponding pin still +4.5V?	Go to Seq 157.
147	Is the corresponding pin still approximately +0.2V?	Go to Seq 157.
148	Is the corresponding pin at ground?	Go to Seq 163.
149	If not:	Go back to Seq 72 and recheck the symptoms.
150	Scope the Secondary Interface Device Address Output lines at communicator card in the operating tape control.	

Seq	Condition/Instruction	Action
151	Scope the line driver output corresponding to the address line for the same incorrect level found at the device switch logic card in Seq 70.	
152	Communicator card A2E2 pins: U02 – Device Address 8 Secondary U04 – Device Address 4 Secondary M12 – Device Address 2 Secondary U06 – Device Address 1 Secondary	
153	Is the corresponding pin still +4.5V?	Go to Seq 157
154	Is the corresponding pin still approximately +0.2V?	Go to Seq 157
155	Is the corresponding pin at ground?	Go to Seq 163
156	If not:	Go to Seq 72 and recheck the symptoms.
157	One of the address lines from the communicator card is sending the wrong level for the operating tape unit.	
158	Scope the +TUADR SELECT lines which are inputs to communicator card. These lines are common to both the Primary and Secondary Interfaces.	
159	Scope the communicator card (A2E2) pins for the MST levels indicated on the line corresponding to the tape unit being tested.	

TU	Address lines (8)	(4)	(2)	(1)
	A2E2 Pins (XC111) G13	S09	M13	U05
0	–	–	–	–
1	–	–	–	+
2	–	–	+	–
3	–	–	+	+
4	–	+	–	–
5	–	+	–	+
6	–	+	+	–
7	–	+	+	+
8	+	–	–	–
9	+	–	–	+
A	+	–	+	–
B	+	–	+	+
C	+	+	–	–
D	+	+	–	+
E	+	+	+	–
F	+	+	+	+

Seq	Condition/Instruction	Action
160	Are all pins on the line that corresponds to to the tape unit you are using at the indicated levels (from Seq 159)?	Go to Seq 162.
161	The address expected from the operating tape control is missing. Set Display Select switch to Bus In. Do bits 8–11 contain an address other than the one previously verified?	Go to Seq 20.
162	The address input to communicator card is correct. A. Check communicator card socket connections. B. If cards are interchanged to isolate the failure, remember to check the jumper on communicator card.	
163	The problem appears to be an open circuit between the communicator card and the device switch logic card. The problem may involve external cabling or internal cables. A. An external cable is a very likely source of failure (address lines go through the Tag cable). B. Check connector contacts at both ends. C. For a 2x8 device switch, see ALD XC700 Sheet 1, Chart D, for cable routing and pin connections. D. For a 3x8 or 4x8 device switch, see ALD XC701, Sheet 3 Chart D for cable routing and pin connections. E. The receiving load card or card socket can be at fault.	
164	Does the DEVICE SELECT line come from the communicator card's Secondary Interface?	Go to Seq 181.
165	Scope –DEVICE SELECT PRIMARY (A2E2G12) in the operating tape control.	
166	Is A2E2G12 at +4.5V?	Go to Seq 169.
167	Is A2E2G12 at ground?	Go to Seq 163.
168	If not:	Go to Seq 62 and recheck the symptoms.
169	Scope +TUTAG BIT 4 DEVICE SELECT (A2E2P05).	
170	Is A2E2P05 –0.8V?	Go to Seq 172.
171	This is an ALU2 problem.	
172	Scope +TUADR SELECT 8 (A2E2G13).	
173	Is A2E2G13 at –.8V?	Go to Seq 176.
174	Is A2E2G13 at –.8V?	Go to Seq 177.
175	This is a tape control problem. Go to 00–010.	

Seq	Condition/Instruction	Action
176	Is the Primary/Secondary Interface Control jumper on card A2E2 plugged LO to use the Primary Interface? (See 90-130, Step D-5.) Check the jumper for plugging and good contact.	Go to Seq 178.
177	Is the Primary/Secondary Interface Control jumper on card A2E2 plugged HI to use the Primary Interface? (See 90-130, Step D-5.) Check the jumper for plugging and good contact.	Go to Seq 178.
178	Check A2E2 socket contacts.	
179	Is +DEVICE SELECT PRIMARY (A2E2G12) now +0.2V?	Rerun failing test to verify fix. Go to 00-030.
180	Change A2E2 card. Is jumper plugged correctly?	Rerun failing test to verify fix. Go to 00-030.
181	Scope –DEVICE SELECT SECONDARY (A2E2M02) in the operating tape control.	
182	Is A2E2M02 at +file?	Go to Seq 185.
183	Is A2E2M02 at ground?	Go to Seq 163.
184	If not:	Go to Seq 62 and recheck your work.
185	Scope +TUTAG BIT 4 DEVICE SELECT (A2E2P05).	
186	Is A2E2P05 at –0.8V?	Go to Seq 188.
187	This is an ALU2 problem.	
188	Scope +TUADR SELECT 8 (A2E2G13).	
189	Is A2E2G13 at –1.8V?	Go to Seq 192.
190	Is A2E2G13 at –0.8V?	Go to Seq 193.
191	This is a tape control problem.	
192	The Primary/Secondary Interface Control jumper on card A2E2 should be plugged HI to use the Secondary Interface. (See 90-130 Step D–5.) A. Check the jumper for plugging and good contact. B. Check the A2E2 socket contacts. C. After making these checks, go to Seq 194.	
193	The Primary/Secondary Interface Control jumper on card A2E2 should be plugged LO to use the Secondary Interface. (See 9-130 Step D–5.) A. Check the jumper for plugging and good contact. B. Check the A2E2 socket connections.	
194	Is +DEVICE SELECT SECONDARY (A2E2M02) now at +0.5V?	Rerun failing test to verify fix. Go to 00-030.

Seq	Condition/Instruction	Action
195	Change A2E2 card. Is the jumper plugged correctly?	Go to Seq 194 to verify fix.
196	Are you using the Secondary Interface?	Go to Seq 203.
197	Scope –CU PWR DOWN PRI TO TU SWITCH (A2P3B03) in the operating tape control.	
198	Is A2P3B03 at ground level?	Go to Seq 200.
199	If not:	Go to Seq 62.
200	Scope 0V POWER GOOD (A2P3D02). Is A2P3D02 at ground level?	Go to Seq 202.
201	Is the relay on A2P3 not picked?	This is a power problem. Go to 11-000.
202	There could be a shorted relay point between A2P3B07 and B03, or an accidental ground on the line from B03 to the device switch logic card. See FD051 and jumper list (2521041) on ALD AA005 for cable routing.	
203	Scope –CU POWER DOWN SECONDARY (A2P2B03) in the tape control you are working with offline.	
204	Is A2P2B03 at ground level?	Go to Seq 206.
205	If not:	Go to Seq 62 and recheck your work.
206	Is 0V POWER GOOD (A2P3D02) at ground level?	Go to Seq 208.
207	Is the relay on A2P3 not picked? Since the relay on A2P2 is picked in parallel, it probably is not picked either.	This is a power problem. Go to 11-000.
208	There could be a shorted relay point between A2P2B07 and B03, or an accidental ground on the line from B03 to the device switch logic card. A. See FD051 and jumper list (2521041) on ALD AA005 for cable routing. B. Relay A2P2 pick coil could be open.	
209	A BUSY condition tells you that the device switch logic card: A. Recognizes the tape unit address. B. Received a SELECT signal. C. The tape unit's ENABLED latch is ON. D. Is receiving a DEVICE BUSY from the tape unit; or E. Is receiving a SWITCH BUSY signal from another device switch logic card.	

Seq	Condition/Instruction	Action
210	On the device switch logic card identified in Seq 65, scope the BUSY/TACH IN line on the pin indicated in sequence 211. Reference: For 2x8 device switch configurations, see ALD XC700 Sheet 1 Chart H. For 3x8 and 4x8 device switches, see ALD XC701 Sheet 3 Chart H.	
211	Scope only the pin corresponding to the tape unit you are using on the device switch logic card identified in Seq 65.	

TU Addr	Logic Card Pin
0	J11
1	G10
2	J10
3	G09
4	J11
5	G10
6	J10
7	G09
8	J11
9	G10
A	J10
B	G09
C	J11
D	G10
E	J10
F	G09

212	Is the pin in Seq 211 at a +4.5V level?	Go to Seq 214.
213	The tape unit is sending a DEVICE BUSY signal. A. Go to the tape unit to determine why. B. Use Chart H on ALD XC700 or 701 for cable routing.	The problem is in TACH/BUSY circuits. Start at ALD FT141, T–A1L2B04.
214	You have determined that this is not a DEVICE BUSY condition. Is there a SWITCH BUSY?	Go to Seq 216.
215	You entered here from Seq 78 under abnormal circumstances. A. When Seq 5 through 8 were performed, if the tape unit had been committed to another tape control, you should not have stopped at 0F5. Therefore, there could be a failure of the BUSY TACH line. B. The other possibility could be that this tape unit was committed to the other tape control after sequences 5–8 were performed.	

Seq	Condition/Instruction	Action
216	Is this a 3x8 or 4x8 device switch?	Go to Seq 221
217	When using a 2x8 switch, the SWITCH BUSY indication can only be due to the COMMITTED latch being ON for the other tape control.	
218	Scope the pin indicated on both of the device switch logic cards, on the line corresponding to the tape unit being tested, for an active MST level (–0.8V). Only one pin should be active. Go to the Seq indicated at the bottom of this chart.	

TU Addr	Pin	Logic Card	
0 or 8	P04	B3H2	B3J2
1 or 9	P05	B3H2	B3J2
2 or A	M02	B3H2	B3J2
3 or B	M03	B3H2	B3J2
4 or C	P04	B3K2	B3L2
5 or D	P05	B3K2	B3L2
6 or E	M02	B3K2	B3L2
7 or F	M03	B3K2	B3L2
Go to Seq:		225	227

219	Were both pins inactive?	Go to Seq 285.
220	Were both pins active?	Go to Seq 218 and recheck the symptoms.
221	When using a 3x8 or 4x8 device switch, the SWITCH BUSY condition can be due to the COMMITTED Latch being On (active) in any of the other device switch logic cards.	
222	Scope the COMMITTED latch output at the pin indicated on all four device switch logic cards for the tape unit being tested for an active MST level (–0.8V). Only one pin should be active. Go to the appropriate Seq shown at the bottom of the chart in this sequence.	

TU Addr	Pin	Logic Cards			
0 or 8	P04	A3Q2	A3R2	A3S2	A3T2
1 or 9	P05	A3Q2	A3R2	A3S2	A3T2
2 or A	M02	A3Q2	A3R2	A3S2	A3T2
3 or B	M03	A3Q2	A3R2	A3S2	A3T2
4 or C	P04	A3L2	A3M2	A3N2	A3P2
5 or D	P05	A3L2	A3M2	A3N2	A3P2
6 or E	M02	A3L2	A3M2	A3N2	A3P2
7 or F	M03	A3L2	A3M2	A3N2	A3P2
Go to Seq:		225	227	229	231

223	Were all pins inactive?	Go to Seq 285.
224	Only one pin should have been active.	Go to Seq 222 and recheck the symptoms.

Seq	Condition/Instruction	Action
225	The operating tape unit is committed to SP–A (Switch Path A). Is the active pin found in Seqs 218 or 222 on the device switch logic card you identified in Seq 65?	Go to Seq 62 and recheck the symptoms.
226	SP–A is used by the tape control being scoped, and the active pin found in Seqs 218 or 222 is on the device switch logic card that the tape control would use to operate this tape unit.	Go to Seq 233.
227	The tape unit operating is committed to SP–B (Switch Path B). Is the active pin found in Seq 218 or 222 on the device switch logic card identified in Seq 65?	Go to Seq 235.
228	Determine which tape control is cabled into SP–B. This tape control will use the device switch logic card found with an active pin in Seqs 218 or 222.	Go to Seq 233.
229	The tape unit operating is committed to SP–C (Switch Path C). Is the active pin found in Seq 222 on the device switch logic card identified in Seq 65?	Go to Seq 235.
230	Determine which tape control is cabled into SP–C. This tape control will use the device switch logic card found with an active pin in Seq 222.	Go to Seq 233.
231	The tape unit operating is committed to SP–D (Switch Path–D). Is the active pin found in Seq 222 on the device switch logic card identified in Seq 65?	Go to Seq 235.
232	Determine which tape control is cabled into SP–D. This tape control will use the device switch logic card found with an active pin in Seq 222.	Go to Seq 233.
233	Did you reach this point from Seq 215?	Go to Seq 272.
234	To summarize the situation: The first tape control worked with **offline** cannot access the tape unit set up because the tape unit is committed to a second tape control which has been identified.	Go to Seq 236.
235	If not:	Go back to Seq 62 and recheck the symptoms.
236	Begin work from the second tape control to determine if the COMMITTED latch can be reset. Is it okay with the customer?	
237	Set the ROS Mode switch on the first tape control to Normal; then Reset the tape control.	
238	The tape unit you are using should still be Loaded, Ready, and at load point.	
239	Enable this tape unit to the second tape control from the operator panel of the host tape control.	

Seq	Condition/Instruction	Action
240	Switch the second tape control **offline** and set up the CE panel to perform multiple LWR (8B) commands with the above tape unit. Use Byte Cnt = FE0 Wrt Data and Go Down = FF0 Reset the tape control.	
241	The device switch logic card to be scoped is the one that had an active pin in Seq 218 or Seq 222.	
242	Is that pin still active?	Go to Seq 245.
243	The Reset performed in Seq 240 reset the COMMITTED latch.	
244	There could still be a bad Reset signal.	
245	Set up an ALU2 COMPARE on address "1BF" (see 12–011).	
246	Set ROS Mode switch to Norm. Then RESET and START.	
247	Set Display Select switch to CE Reg, and Data Entry Select switch to Cmd1.	
248	Are lights flashing a hex 8B?	Go to Seq 250.
249	If lights are not flashing, the command sequence is not running. If flashing but not showing "8B", the tape control is not performing an LWR.	Go to Seq 46 to resolve.
250	Sync minus on A1U2U07 of the second tape control. A long sync lead may be needed.	
251	Scope the device switch logic card identified in Seq 218 or 222 for a 50 ns SET/RESET pulse on pin P07. Minimum up level is +4.5V. Minimum down level is +0.5V. Minimum duration is 40 ns.	
252	Does the pulse meet specifications in Seq 251?	Go to Seq 271.
253	The SET/RESET pulse comes from communicator card A2E2 in the tape control being tested.	
254	Is the Secondary Interface of the communicator card being used?	Go to Seq 260.
255	Scope –SET/RESET PRIMARY (A2E2G13).	
256	Does the pulse meet specifications in Seq 251?	Go to Seq 271.
257	Is A2E2G13 a solid +4.5V?	Go to Seq 265.
258	Is A2E2G13 at a solid ground level?	Go to Seq 163.
259	Is there a bad pulse?	Go to Seq 268.
260	Scope –RESET RESERVE SECONDARY (A2E2G04).	
261	Does the pulse meet specifications in Seq 251?	Go to Seq 271.
262	Is A2E2G04 at a solid +4.5V level?	Go to Seq 265.
263	Is A2E2G04 at a solid ground level?	Go to Seq 163.
264	Is there just a bad pulse?	Go to Seq 268.
265	Scope +RESET COMMITTED LATCH PLS (A2E2G10) for a MST pulse of 50 ns duration.	
266	Is the pulse good?	Go to Seq 268.
267	If not:	This is a tape control problem. Go to 00-010.
268	Check A2E2 for good socket connections. Change A2E2. Be sure the jumper is plugged correctly.	
269	Cable contacts may cause a poor pulse. For a 2x8 device switch, see XC700 Sheet 3 Chart D for cable routing. For a 3x8 or 4x8 device switch, see XC701 Sheet 3 Chart D for cable routing.	
270	If not:	Go to Seq 250 and recheck your work.
271	Check the card socket contacts of the device switch logic card identified in Seqs 218 or 222 for good connections. A. Replace the device switch logic card identified in Seqs 218 or 222, making sure the jumpers are plugged correctly. B. A COMMITTED latch may be turned on erroneously by communicator card A2D2 of the tape control that normally uses it. This can happen even when the tape control is not working with this tape unit	
272	The BUSY/TACH line should be active back to the operating tape control.	
273	On the device switch logic card you identified in Seq 65, scope pin G03 (BUSY TACH).	
274	Is pin G03 at +0.2V level?	Go to Seq 277
275	Is pin G03 at a solid ground level?	Go to Seq 163.
276	The device switch logic card identified in Seq 65 is failing. A. Check the socket for good connections. B. Replace the device switch logic card, making sure the jumpers are plugged correctly.	
277	Are you using the Secondary Interface in the operating tape control?	Go to Seq 281.
278	In the operating tape control, scope –BUSY OR TACH PRIMARY (A2D2G09) at the communicator card.	
279	Is pin G09 at a +0.5V level?	Go to Seq 284.
280	If not:	Go to Seq 272 and recheck your work.
281	In the operating tape control, scope –BUSY OR TACH SECONDARY (A2D2D12) at the communicator card.	
282	Is pin D12 at +0.5V level?	Go to Seq 284.
283	If not:	Go to Seq 272 and recheck your work.
284	Check the A2D2 socket connections. Change A2D2. You should now determine why the COMMITTED latch was active in the other device switch logic card.	Go to Seq 5.
285	You are apparently branching on a false BUSY condition.	
286	On the device switch logic card identified in Seq 65, scope pin G03 (BUSY TACH).	
287	Is pin G03 at a +4.5V level?	Go to Seq 289.
288	If not:	Replace the device switch logic card. Make sure the jumpers are plugged correctly.
289	Change communicator card A2D2 in the operating tape control.	
290	You have determined that a line needed for a XPT card is not active.	
291	On the device switch logic card identified in Seq 65, scope pin B04 (GATE BUS OUT).	
292	Is pin B04 at +0.2V?	Go to Seq 294.
293	If not:	Go to Seq 1 and recheck your work.
294	Change the device switch logic card. A. Check the socket for good connections. B. Be sure the jumpers are plugged correctly.	
295	Mount a CE work tape on the failing tape unit you are working with. LOAD and READY the tape unit.	
296	Set up the CE panel of the operating tape control to do multiple commands of: WRT WRT WRT REW Use Byte Cnt = FE0 Wrt Data/Go Down = FF0 Operate the Reset switch.	

Seq	Condition/Instruction	Action
297	Set up an ALU2 Compare Stop on address 16D (MSKSTS). Start. Ensure that the tape positions behind load point.	
298	Set Display Select switch to ALU2 BUS OUT. Bits 0–11 should be 08C.	
299	Return Display Select switch to IC position and the Mple/Single switch to Single. Each time the Start/Step switch is operated, one of the commands in Seq 296 should execute. Observe the BUS OUT lights between Start/Step switch operations for the following: Start 1 — 08C Start 2 — 08C Start 3 — 08C Start 4 — 01A Start 5 — 08C	
300	If the tape control hangs on 08C:	Go to Seq 6.
301	If the tape control hangs on 01A:	Go to Seq 303.
302	Can you step through the commands in Seq 296?	Go to Seq 308.
303	This is a control command problem.	
304	Set Display Select switch to Bus In and ALU1/ALU2 switch to ALU2.	
305	Do tape unit Data bits 0–7 = hex 01?	Go to Seq 307.
306	Any missing or extra bits may be an XPT switch card or cable problem. Be sure to check the CTRL TAG.	Go to Seq 109.
307	This is the normal response, and the tape unit should rewind.	
308	Go to Seq 62 to identify the device switch logic card you are using.	
309	Is this an interrupt problem?	Go to Seq 336.
310	Is this a tach problem?	Go to Seq 351.
311	Is this a meter problem?	Go to Seq 313.
312	All other device switch problems are covered starting at Seq 5.	Go to Seq 5.
313	Set the ROS Mode switch to Norm. Then operate Reset and Start switch. When the tape moves away from load point, the meter should run. When tape returns to load point after rewinding, the meter should stop.	
314	Set up scope with a time base of 5 ms/div.	

Seq	Condition/Instruction	Action
315	On the device switch logic card you are using, scope the RUN METER line at the pin that corresponds to the tape unit you are using. TU Addr / Logic Card Pin 0 or 8 — B10 1 or 9 — D10 2 or A — D04 3 or B — D06 4 or C — B10 5 or D — D10 6 or E — D04 7 or F — D06	
316	Does the line in Seq 315 shift to +0.2V (active level) when tape is away from load point, and to a +4.5V (inactive level) when tape is at load point?	Go to Seq 319.
317	Does the line in Seq 315 stay at a solid +4.5V level?	Go to Seq 320.
318	Does the line in Seq 315 stay at a solid ground level? Read Seq 163.	Go to Seq 135.
319	The correct signals are being sent to the tape unit.	
320	On the device switch logic card you are using, scope pin D02 (RUN METER).	
321	Is pin D02 at a solid +4.5V level?	Go to Seq 325.
322	Does line D02 shift between +0.5V level and +4.5V level?	Go to Seq 324.
323	There are no other expected conditions.	
324	The device switch logic card being used must be failing. A. Check the socket for good connections. B. Replace the device switch logic card, be sure the jumpers are plugged correctly.	
325	Is the Secondary Interface in the tape control being used?	Go to Seq 329.
326	On communicator card A2E2 in the operating tape control, scope pin M03 (–RUN METER PRIMARY).	
327	Is pin M03 at a solid +4.5V level?	Go to Seq 332.
328	Is pin M03 at solid ground level? If so, read Seq 163.	Go to Seq 135.
329	On communicator card A2E2 in the operating tape control, scope pin P03.	
330	Is pin P03 at solid +4.5V level?	Go to Seq 332.

Seq	Condition/Instruction	Action
331	Is pin P03 at a solid ground level? If so, read Seq 163.	Go to Seq 135.
332	Scope pin A2E2P04 (+RUN METER).	
333	Is pin P04 shifting between active and inactive MST levels? Go to Seq 335.	
334	This is an ALU2 problem.	
335	The communicator card is failing. A. Check the socket for good connections. B. Replace this communicator card, be sure the jumper is plugged correctly.	
336	REWIND/UNLOAD the tape unit.	
337	Set the ROS mode switch to Norm. Then operate Reset and then Start.	
338	The INTERRUPT line should be pulsing.	
339	On the device switch logic card being tested, scope pin J03 (DEV END INTR).	
340	Are there pulses of 200 ns duration from a +4.5V level to +0.5V level occurring every 350 ns on pin J03?	Go to Seq 346.
341	Is pin J03 at a solid +4.5V level?	Go to Seq 343.
342	Is pin J03 at a solid ground level? If so, read Seq 163.	Go to Seq 135.
343	On the device switch logic card being used, scope the pin that corresponds to the tape unit being tested: TU Addr / Logic Card Pin 0 or 8 — D11 1 or 9 — J02 2 or A — D07 3 or B — B07 4 or C — D11 5 or D — J02 6 or E — D07 7 or F — B07	
344	Is the pin in Seq 343 pulsing as described in Seq 340?	Go to Seq 324.
345	Are there INTERRUPT pulses coming from the tape unit?	Go to Seq 135 and check cabling.
346	There are good INTERRUPT pulses going to communicator card A2D2 in the tape unit being used **offline**.	
347	Scope DEV END INTR (A2D2G12).	
348	Are there MST level pulses on G12?	Go to Seq 350.

DEVICE SWITCHING FEATURE —TROUBLESHOOTING PROCEDURE (Cont'd)

Seq	Condition/Instruction	Action
349	Card A2D2 is failing: A. Check the socket for good connection. B. Change A2D2.	
350	Good DEV END INTR pulses are going to the tape control.	
351	The tach problem will be scoped while the tape unit is in a runaway condition.	
352	Be ready to scope before starting program.	
353	Set up an ALU2 COMPARE STOP on address 219 (EXECVEL). See 12-011.	
354	RESET and START when ready to scope.	
355	On the device switch logic card being used, scope pin G03.	
356	Are pulses from a +4.5V level to a +0.5V level occurring at a uniform rate? **Model** / **Pulse Width** Model 4 — 126 usec Model 6 — 75 usec Model 8 — 47 usec	
357	Is pin G03 at a solid +4.5V level?	Go to Seq 359.
358	Is pin G03 at a solid ground level? If so, read Seq 163.	Go to Seq 135.
359	On the device switch logic card being used, scope the pin that corresponds to the tape unit being tested. **TU Addr** / **Logic Card Pin** 0 or 8 — J11 1 or 9 — G10 2 or A — J10 3 or B — G09 4 or C — J11 5 or D — G10 6 or E — J10 7 or F — G09	

Seq	Condition/Instruction	Action
360	Is the pin in Seq 359 pulsing as described in Seq 356?	Go to Seq 324.
361	If not:	Go to Seq 135 and check cabling.
362	There are good Tach pulses going to communicator card A2D2 in the tape control being used **offline**.	
363	Scope –TACH VELOCITY pulses (A2D2B02).	
364	Are there MST level pulses on B02?	Go to Seq 366.
365	Communicator card A2D2 is failing. A. Check the socket for good connections. B. Change A2D2.	
366	Good pulses are going to the tape control.	This is a tape control problem. Go to 00-010.

HOW TO USE CHART A

Follow these steps:

From Seq 89:	
Step 1	Find the failing tape unit address in the left-hand column.
Step 2	Find the subsystem configuration in the top row.
Step 3	Go to block where they intersect.
Step 4	Write down this information. Example: You have a 2x8 device switch, and TU5 is failing on TCB. The box where they intersect lists FRUs that could cause device switching problems with this tape unit: LOGIC CARD B3L2 OUTBOUND XPT CARD B3P2 INBOUND XPT CARD B3G2 DEVICE BUS OUT CABLE B3U3 DEVICE BUS IN CABLE B3B3
Step 5	Return to procedure at Seq 90.

CHART A

TU	Card/Cable	2x8 TCA	2x8 TCB	3x8 or 4x8 TCA	3x8 or 4x8 TCB	3x8 or 4x8 TCC	4x8 TCD
0/8	LOGIC CARD	B3H2 TYPE 6319	B3J2 TYPE 7867	A3Q2 TYPE 6319	A3R2 TYPE 7867	A3S2 TYPE 7867	A3T2 TYPE 7867
	OUTBOUND XPT CARD	B3S2 TYPE 5896	B3R2 TYPE 5896	B3T2 TYPE 5896	B3S2 TYPE 5896	B3R2 TYPE 5896	B3Q2 TYPE 5896
	INBOUND XPT CARD	B3D2 TYPE 5897	B3E2 TYPE 5897	B3C2 TYPE 5897	B3D2 TYPE 5897	B3E2 TYPE 5897	B3F2 TYPE 5897
	DEVICE BUS OUT CABLE	B3V2 TO 01TA1C8	B3V2 TO 01TA1C8	B3V2 TO 01TA1C8	B3U2 TO 01TA1C8	B3V2 TO 01TA1C8	B3V2 TO 01TA1C8
	DEVICE BUS IN CABLE	B3A2 FROM 01TA1D8	B3A2 FROM 01TA1D8	B3A2 FROM 01TA1D8	B3A2 FROM 01TA1D8	B3A2 FROM 01TA1D8	B3A2 FROM 01TA1D8
1/9	LOGIC CARD	B3H2 TYPE 6319	B3J2 TYPE 7867	A3Q2 TYPE 6319	A3R2 TYPE 7867	A3S2 TYPE 7867	A3T2 TYPE 7867
	OUTBOUND XPT CARD	B3S2 TYPE 5896	B3R2 TYPE 5896	B3T2 TYPE 5896	B3S2 TYPE 5896	B3R2 TYPE 5896	B3Q2 TYPE 5896
	INBOUND XPT CARD	B3D2 TYPE 5897	B3E2 TYPE 5897	B3C2 TYPE 5897	B3D2 TYPE 5897	B3E2 TYPE 5897	B3F2 TYPE 5897
	DEVICE BUS OUT CABLE	B3V3 TO 01TA1C7	B3V3 TO 01TA1C7	B3V3 TO 01TA1C7	B3V3 TO 01TA1C7	B3V3 TO 01TA1C7	B3V3 TO 01TA1C7
	DEVICE BUS IN CABLE	B3A3 FROM 01TA1D7	B3A3 FROM 01TA1D7	B3A3 FROM 01TA1D7	B3A3 FROM 01TA1D7	B3A3 FROM 01TA1D7	B3A3 FROM 01TA1D7
2/A	LOGIC CARD	B3H2 TYPE 7867	B3J2 TYPE 7867	A3Q2 TYPE 6319	A3R2 TYPE 7867	A3S2 TYPE 7867	A3T2 TYPE 7867
	OUTBOUND XPT CARD	B3S2 TYPE 6896	B3R2 TYPE 6896	B3T2 TYPE 6896	B3S2 TYPE 5896	B3R2 TYPE 5896	B3Q2 TYPE 5896
	INBOUND XPT CARD	B3D2 TYPE 5897	B3E2 TYPE 5897	B3C2 TYPE 5897	B3D2 TYPE 5897	B3E2 TYPE 5897	B3F2 TYPE 5897
	DEVICE BUS OUT CABLE	B3V4 TO 01TA1C6	B3V4 TO 01TA1C6	B3V4 TO 01TA1C6	B3V4 TO 01TA1C6	B3V4 TO 01TA1C6	B3V4 TO 01TA1C6
	DEVICE BUS IN CABLE	B3A4 FROM 01TA1D6	B3A4 FROM 01TA1D6	B3A4 FROM 01TA1D6	B3A4 FROM 01TA1D6	B3A4 FROM 01TA1D6	B3A4 FROM 01TA1D6
3/B	LOGIC CARD	B3H2 TYPE 7867	B3J2 TYPE 7867	A3Q2 TYPE 6319	A3R2 TYPE 7867	A3S2 TYPE 7867	A3T2 TYPE 7867
	OUTBOUND XPT CARD	B3S2 TYPE 5896	B3R2 TYPE 5896	B3T2 TYPE 5896	B3S2 TYPE 5896	B3R2 TYPE 5896	B3Q2 TYPE 5896
	INBOUND XPT CARD	B3D2 TYPE 5897	B3E2 TYPE 5897	B3C2 TYPE 5897	B3D2 TYPE 5897	B3E2 TYPE 5897	B3F2 TYPE 5897
	DEVICE BUS OUT CABLE	B3V5 TO 01TA1C5	B3V5 TO 01TA1C5	B3V5 TO 01TA1C5	B3V5 TO 01TA1C5	B3V5 TO 01TA1C5	B3V5 TO 01TA1C5
	DEVICE BUS IN CABLE	B3A5 FROM 01TA1D5	B3A5 FROM 02TA1D5	B3A5 FROM 01TA1D5	B3A5 FROM 01TA1D5	B3A5 FROM 01TA1D5	B3A5 FROM 01TA1D5
4/C	LOGIC CARD	B3K2 TYPE 7866	B3L2 TYPE 7868	A3L2 TYPE 7866	A3M2 TYPE 7868	A3N2 TYPE 7868	A3P2 TYPE 7868
	OUTBOUND XPT CARD	B3Q2 TYPE 5896	B3P2 TYPE 5896	B3P2 TYPE 5896	B3N2 TYPE 5896	B3M2 TYPE 5896	B3L2 TYPE 5896
	INBOUND XPT CARD	B3F2 TYPE 5897	B3G2 TYPE 5897	B3G2 TYPE 5897	B3H2 TYPE 5897	B3J2 TYPE 5897	B3K2 TYPE 5897
	DEVICE BUS OUT CABLE	B3U2 TO 01TA1C4	B3U2 TO 01TA1C4	B3U2 TO 01TA1C4	B3U2 TO 01TA1C4	B3U2 TO 01TA1C4	B3U2 TO 01TA1C4
	DEVICE BUS IN CABLE	B3B2 FROM 01TA1D4	B3B2 FROM 01TA1D4	B3B2 FROM 01TA1D4	B3B2 FROM 01TA1D4	B3B2 FROM 01TA1D4	B3B2 FROM 01TA1D4
5/D	LOGIC CARD	B3K2 TYPE 7866	B3L2 TYPE 7868	A3L2 TYPE 7866	A3M2 TYPE 7868	A3N2 TYPE 7868	A3P2 TYPE 7868
	OUTBOUND XPT CARD	B3Q2 TYPE 5896	B3P2 TYPE 5896	B3P2 TYPE 5896	B3N2 TYPE 5896	B3M2 TYPE 5896	B3L2 TYPE 5896
	INBOUND XPT CARD	B3F2 TYPE 5897	B3G2 TYPE 5897	B3G2 TYPE 5897	B3H2 TYPE 5897	B3J2 TYPE 5897	B3K2 TYPE 5897
	DEVICE BUS OUT CABLE	B3U3 TO 01TA1C3	B3U3 TO 01TA1C3	B3U3 TO 01TA1C3	B3U3 TO 01TA1C3	B3U3 TO 01TA1C3	B3U3 TO 01TA1C3
	DEVICE BUS IN CABLE	B3B3 FROM 01TA1D3	B3B3 FROM 01TA1D3	B3B3 FROM 01TA1D3	B3B3 FROM 01TA1D3	B3B3 FROM 01TA1D3	B3B3 FROM 01TA1D3
6/E	LOGIC CARD	B3K2 TYPE 7866	B3L2 TYPE 7868	A3L2 TYPE 7866	A3M2 TYPE 7868	A3N2 TYPE 7868	A3P2 TYPE 7868
	OUTBOUND XPT CARD	B3Q2 TYPE 5896	B3P2 TYPE 5896	B3P2 TYPE 5896	B3N2 TYPE 5896	B3M2 TYPE 5896	B3L2 TYPE 5896
	INBOUND XPT CARD	B3F2 TYPE 5897	B3G2 TYPE 5897	B3G2 TYPE 5897	B3H2 TYPE 5897	B3J2 TYPE 5897	B3K2 TYPE 5897
	DEVICE BUS OUT CABLE	B3U4 TO 01TA1C2	B3U4 TO 01TA1C2	B3U4 TO 01TA1C2	B3U4 TO 01Ta1C2	B3U4 TO 01TA1C2	B3U4 TO 01TA1C2
	DEVICE BUS IN CABLE	B3B4 FROM 01TA1D2	B3B4 FROM 01TA1D2	B3B4 FROM 01TA1D2	B3B4 FROM 01TA1D2	B3B4 FROM 01TA1D2	B3B4 FROM 01TA1D2
7/F	LOGIC CARD	B3K2 TYPE 7866	B3L2 TYPE 7868	A3L2 TYPE 7866	A3M2 TYPE 7868	A3N2 TYPE 7868	A3P2 TYPE 7868
	OUTBOUND XPT CARD	B3Q2 TYPE 5896	B3P2 TYPE 5896	B3P2 TYPE 5896	B3N2 TYPE 5896	B3M2 TYPE 5896	B3L2 TYPE 5896
	INBOUND XPT CARD	B3F2 TYPE 5897	B3G2 TYPE 5897	B3G2 TYPE 5897	B3H2 TYPE 5897	B3J2 TYPE 5897	B3K2 TYPE 5897
	DEVICE BUS OUT CABLE	B3U5 TO 01TA1C1	B3U5 TO 01TA1C1	B3U5 TO 01TA1C1	B3U5 TO 01TA1C1	B3U5 TO 01TA1C1	B3U5 TO 01TA1C1
	DEVICE BUS IN CABLE	B3B5 FROM 01TA1D1	B3B5 FROM 01TA1D1	B3B5 FROM 01TA1D1	B3B5 FROM 01TA1D1	B3B5 FROM 01TA1D1	B3B5 FROM 01TA1D1

Chart B: Sel XPT Drive 2x8, 3x8, 4x8

Line Name See Note	Step 1 SDI Logic Card	Step 2	Step 3 XPT Card
0 or 8 SEL XPT DRIVE	D12	Cabling and Wiring ALD XC701 Chart L	B02
1 or 4 SEL XPT DRIVE	B12		G02
2 or 10 SEL XPT DRIVE	B09		M13
3 or 11 SEL XPT DRIVE	D09		S13
4 or 12 SEL XPT DRIVE	D12		B02
5 or 13 SEL XPT DRIVE	B12	3x8 4x8 Only	G02
6 or 14 SEL XPT DRIVE	B09		M13
7 or 15 SEL XPT DRIVE	D09		S13

Chart D: Tape Control to Device

Line Name See Note	Step 1 Tape Unit Logic and Card Pin A2E2 Primary XC141	 Secondary XC151	Step 2 Cabling 3x8 ALD XC701 4x8 Chart K 2x8 ALD XC700 Chart K Sel ALD XC700 Chart P	Step 3 Input to Outbound XPT	XPT CARD OUTBOUND	Step 4 TC Device Bus Out Cable	Step 5 Cabling and Wiring 3x8 ALD XC701 4x8 Chart K 2x8 ALD XC700 Chart K Sel ALD XC700 Chart P
BUS OUT 0	G09	G08		P05		B02	
BUS OUT 1	D03	B03		M07		D03	
BUS OUT 2	D04	B04		P04		B04	
BUS OUT 3	B09	B12		P06		D05	
BUS OUT 4	D09	D13		J13		B06	
BUS OUT 5	P07	M07		G13		D07	
BUS OUT 6	M09	M08	→	G12		B08	→
BUS OUT 7	P02	U11	To Switch	J12		D09	To Drive
BUS OUT P	J07	G07		D13		B10	
TAG A CNTRL	P11	U12		B13		D11	
TAG B CMND	P12	P12		D12		B12	
TAG C MOVE	S04	S07		B12		D13	

Chart E: Device to Tape Control

Line Name See Note	Step 1 Cabling 3x8 ALD XC701 4x8 Chart K 2x8 ALD XC700 Chart K Sel ALD XC700 Chart P	Step 2 TC Device Bus In Cable	XPT CARD INBOUND	Step 3 Output of Inbound XPT	Step 4 Cabling and Wiring 3x8 ALD XC701 4x8 Chart K 2x8 ALD XC700 Chart K Sel ALD XC700 Chart P	Step 5 TC Logic and Card Pin A2D2 Primary XC011	 Secondary XC021
BUS IN 0		B02		P05		M05	P05
BUS IN 1		D03		M07		J09	D10
BUS IN 2		B04		P04		J06	P10
BUS IN 3		D05		P06		G13	M12
BUS IN 4		B06		J13		G08	D04
BUS IN 5		D07		G13		G10	P04
BUS IN 6	→	D05		G12	→	M10	J12
BUS IN 7	To Switch	D09		J12	To TCU	D06	B04
BUS IN P		B10		D13		S07	M03

+0.2 V Bit active to good line XPT Selected

+4.0 V Bit inactive to good line XPT Selected

+0.1 V Bit active to open line XPT Selected

+5.0 V Bit inactive to open line XPT Selected

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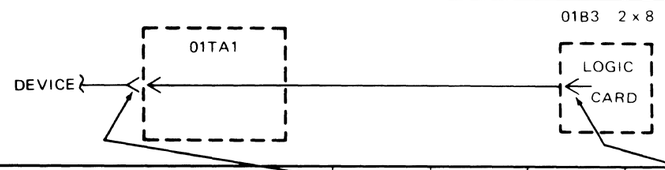
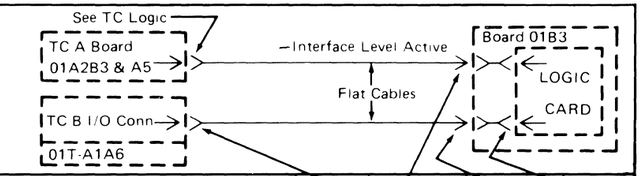
Device to SDI Logic Lines



Dev	Line Name: Device	Line Name: SDI Switch	I/O 01T-A1	Board Cable Pin			*Card Pin
0	Busy Tach In →	Busy/Tach	C8G12	B3A2B12			J11
	Interrupt In →	Dev End Intr	C8J11	B3A2D11			D11
	Meter Out ←	Run Meter	C8J13	B3A2D13			B10
1	Busy Tach In →	Busy/Tach	C7G12	B3A3B12			G10
	Interrupt In →	Dev End Intr	C7J11	B3A3D11			J02
	Meter Out ←	Run Meter	C7J13	B3A3D13			D10
2	Busy Tach In →	Busy/Tach	C6G12	B3A4B12			J10
	Interrupt In →	Dev End Intr	C6J11	B3A4D11			D07
	Meter Out ←	Run Meter	C6J13	B3A4D13			D04
3	Busy Tach In →	Busy/Tach	C5G12	B3A5B12			G09
	Interrupt In →	Dev End Intr	C5J11	B3A5D11			B07
	Meter Out ←	Run Meter	C5J13	B3A5D13			D06
4	Busy Tach In →	Busy/Tach	C4G12	B3B2B12			J11
	Interrupt In →	Dev End Intr	C4J11	B3B2D11			D11
	Meter Out ←	Run Meter	C4J13	B3B2D13			B10
5	Busy Tach In →	Busy/Tach	C3G12	B3B3B12			G10
	Interrupt In →	Dev End Intr	C3J11	B3B3D11			J02
	Meter Out ←	Run Meter	C3J13	B3B3D13			D10
6	Busy Tach In →	Busy/Tach	C2G12	B3B4B12			J10
	Interrupt In →	Dev End Intr	C2J11	B3B4D11			D07
	Meter Out ←	Run Meter	C2J13	B3B4D13			D04
7	Busy Tach In →	Busy/Tach	C1G12	B3B5B12			G09
	Interrupt In →	Dev End Intr	C1J11	B3B5D11			B07
	Meter Out ←	Run Meter	C1J13	B3B5D13			D06

*See Chart A on 18-028 for card location.

Tape Control to SDI Logic



TC ALD Pages: Primary	TC ALD Pages: Secondary	Line Names	T.C.B I/O Pin	T.C.A	T.C.B	*Card Pin
XC111	XC121	Add Bit 1 → Add Bit 1	B05	H6D02	M6B02	U11
XC111	XC121	Add Bit 2 → Add Bit 2	D06	H6E04	M6C04	U12
XC111	XC121	Add Bit 4 → Add Bit 4	B06	J6A02	M6C02	U07
XC111	XC121	Add Bit 8 → Add Bit 8	B08	J6B04	M6E04	U06
XC111	XC101	Device Sel → Device Sel	B03	H6B02	L6E02	P03
GND	GND	Switch Sel → Switch Sel	D02	H6A04	L6D04	P02
XC111	XC121	Set Reset → Set Reset	D11	J6E02	N6C02	P07
XC091	XC101	Enable/Disable → Test Cond.	D13	K6B02	N6E02	M07
FD051	FD051	TC Power Down → TC Power Down	D09	J6C02	N6A02	B02
		Not Used → Reserved	B12	K6A04	N6D04	D05
XC111	XC121	B Select → Int. B Sel	D04	H6C04	M6A04	B05
XC111	XC101	Run Meter → Run Meter	B10	J6D04	N6B04	D02
XC081	XC081	Dev Operating ← Dev Op. Int A	J09	R6B02	U6C02	G07
XC081	XC081	Dev Op. B ← Dev Op. Int B	G06	Q6E02	U6A02	J07
XC081	XC081	Busy Tach ← Busy Tach	G12	R6E04	V6A04	G03
XC081	XC081	Dev. End Intr ← Dev. End Intr	J11	R6D04	U6E04	J03
XC081	XC081	Gate Bus Out ← Gate Bus Out	G10	R6C04	U6D04	B04

*See Chart A on 18-028 for card location.

NOTES:

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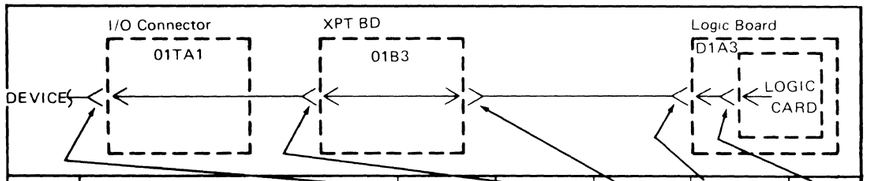
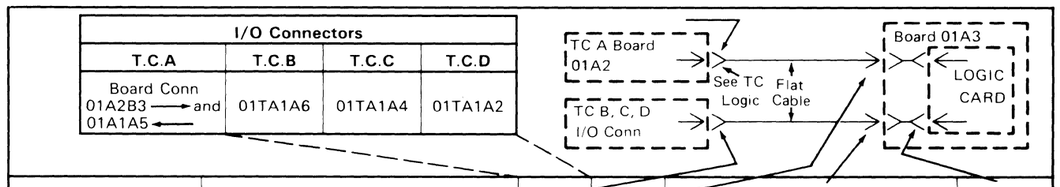
Device to SDI Logic Lines



Dev	Line Name	I/O Conn and Pin 01T-A1	XPT Board Cable Pin	XPT Board Cable Pin	Logic Board Cable Pin	*Card Pin
0, 8	Busy Tach In → Busy/Tach	C8G12	B3A2B12	B3B1D13	A3V3B06	J11
	Interrupt In → Dev End Intr	C8J11	B3A2D11	B3B1A13	A3V3B04	D11
	Meter Out ← Run Meter	C8J13	B3A2D13	B3A1D13	A3V3B02	B10
1, 9	Busy Tach In → Busy/Tach	C7G12	B3A3B12	B3C1D13	A3V3B12	G10
	Interrupt In → Dev End Intr	C7J11	B3A3D11	B3C1B13	A3V3B10	J02
	Meter Out ← Run Meter	C7J13	B3A3D13	B3B1E13	A3V3B08	D10
2, 10	Busy Tach In → Busy/Tach	C6G12	B3A4B12	B3B1D11	A3V3D07	J10
	Interrupt In → Dev End Intr	C6J11	B3A4D11	B3B1B11	A3V3D05	D07
	Meter Out ← Run Meter	C6J13	B3A4D13	B3A1E11	A3V3D03	D04
3, 11	Busy Tach In → Busy/Tach	C5G12	B3A5B12	B3C1E11	A3V3D13	G09
	Interrupt In → Dev End Intr	C5J11	B3A5D11	B3C1C11	A3V3D11	B07
	Meter Out ← Run Meter	C5J13	B3A5D13	B3C1A11	A3V3D09	D06
4, 12	Busy Tach In → Busy/Tach	C4G12	B3B2B12	B3B6C04	A3V2B06	J11
	Interrupt In → Dev End Intr	C4J11	B3B2D11	B3B6A04	A3V2B04	D11
	Meter Out ← Run Meter	C4J13	B3B2D13	B3A6D04	A3V2B02	B10
5, 13	Busy Tach In → Busy/Tach	C3G12	B3B3B12	B3C6D04	A3V2B12	G10
	Interrupt In → Dev End Intr	C3J11	B3B3D11	B3C6B04	A3V2B10	J02
	Meter Out ← Run Meter	C3J13	B3B3D13	B3B6E04	A3V2B08	D10
6, 14	Busy Tach In → Busy/Tach	C2G12	B3B4B12	B3B6D02	A3V2D07	J10
	Interrupt In → Dev End Intr	C2J11	B3B4D11	B3B6B02	A3V2D05	D07
	Meter Out ← Run Meter	C2J13	B3B4D13	B3A6E02	A3V2D03	D04
7, 15	Busy Tach In → Busy/Tach	C1G12	B3B5B12	B3C6E02	A3V2D13	G09
	Interrupt In → Dev End Intr	C1J11	B3B5D11	B3C6C02	A3V2D11	B07
	Meter Out ← Run Meter	C1J13	B3B5D13	B3C6A02	A3V2D09	D06

*See Chart A on 18-028 for card location.

Control Unit to SDI Logic



Tape Control Logic Pages		Line Names		TC B, C, D I/O Pin	Logic Board	Board I/O Flat Cable Locations				
Primary	Secondary	Control Unit	SDI Switch			T.C.A	T.C.B	T.C.C	T.C.D	Card Pin*
XC111	XC121	Add Bit 1 →	Add Bit 1	B05		A4D05	B4D05	A5D05	B5D05	U11
XC111	XC121	Add Bit 2 →	Add Bit 2	D06		A4B06	B4B06	A5B06	B5B06	U12
XC111	XC121	Add Bit 4 →	Add Bit 4	B06		A4D07	B4D07	A5D07	B5D07	U07
XC111	XC121	Add Bit 8 →	Add Bit 8	B08		A4B08	B4B08	A5B08	B5B08	U06
XC111	XC101	Device Sel →	Device Sel	B03		A4D03	B4D03	A5D03	B5D03	P03
GND	GND	Switch Sel →	Switch Sel	D02		A4B02	B4B02	A5B02	B5B02	P02
XC111	XC121	Set-Reset →	Set-Reset	D11		A4D11	B4D11	A5D11	B5D11	P07
XC091	XC101	Enable/Disable →	Test Cond	D13		A4D13	B4D13	A5D13	B5D13	M07
FD051	FD051	TC Power Down →	TC Pwr Down	D09	01A3	A4D09	B4D09	A5D09	B5D09	B02
		Not Used →	Reserved	B12		A4B12	B4B12	A5B12	B5B12	D05
XC111	XC121	B Select →	Int B Sel	D04		A4B04	B4B04	A5B04	B5B04	B05
XC111	XC101	Run Meter →	Run Meter	B10		A4B10	B4B10	A5B10	B5B10	D02
XC081	XC081	Dev Operating A ←	Dev-Op Int A	J09		V5D09	U5D09	V4D09	U4D09	G07
XC081	XC081	Dev Operating B ←	Dev-Op Int B	G06		V5D07	U5D07	V4D07	U4D07	J07
XC081	XC081	Busy Tach ←	Busy Tach	G12		V5B12	U5B12	V4B12	U4B12	G03
XC081	XC081	Dev End Intr ←	Dev End Intr	J11		V5B11	U5D11	V4D11	U4D11	J03
XC081	XC081	Gate Bus Out ←	Gate Bus Out	G10		V5B10	U5B10	V4B10	U4B10	B04

*See Chart A on 18-028 for card location

NOTES:

TAPE CONTROL CHANNEL INTERFACE PROBLEMS

Interface Control checks caused by the 3803 are primarily due to errors in ALU1 or ALU2. To check for this condition, run with the Control Check Stop switch ON and ALU1 in STOP mode. If an ALU1 Control Check occurs, refer to 13-000 for failure analysis: If the failure is not of this type and can be duplicated offline, refer to 12-000. **(CAUTION, see Note 2.)** To aid in online failure analysis, use program FRIEND. If possible, use the failing command sequence with timeout to restart on error.

Use the chart to locate the logic and cards associated with the failure type.

Most Probable Cause:

1. Interface Control Checks.
   - a. INTERFACE LOGIC
   - b. OUT TAG RECEIVERS
   - c. IN TAG DRIVERS
   - d. INITIAL SELECTION LOGIC
   - e. TIE-BREAKER LOGIC (Two-Channel Switch feature only)
   - f. TAG CABLES
2. Channel Data Checks.
   - a. BUS IN DRIVERS
   - b. BUS CABLES
3. Condition Code 3 — (or unit not available).
   - a. BUS OUT RECEIVERS
   - b. ADDRESS GENERATION AND COMPARE
   - c. BUS CABLES
   - d. TIE BREAKER LOGIC (only if Two-Channel Switch feature is installed)

Numbers in () are card types which can be interchanged between interfaces to aid in isolating a failure, if Two-Channel Switch feature is installed.

Chart 1: Channel Interface Cables and MST Cards by Function

Card/Cable Function	Logic		Channel A		Channel B	
	Chan A	Chan B	With EC733814	Without EC733814	With EC733814	Without EC733814
OUT TAG RECEIVERS	FC011	XM011	01A-B2Q2 (9147) or (W031)	01A-B2Q2 (9147) or (W031)	01A-B2P2 (9147) or (W031)	01A-B2P2 (9147) or (W031)
SELECT OUT BYPASS LOGIC	FC031	XM031				
INTERFACE LOGIC	FC021 FC041 FC051	XM021 XM041 XM051	(CAUTION: See Note 1.)			
IN TAG DRIVERS	FC221 FC251 FC261	XM121 XM151 XM161	01A-B2S2 (5840)	01A-B2R2 (5840)	01A-B2R2 (5840)	01A-B2S2 (5840)
BUS IN DRIVERS	FC231 FC241 FC251	XM131 XM141 XM151				
SELECT BYPASS RELAYS	FC271	XM171	(CAUTION: See Note 1.)			
BUS OUT RECEIVERS GATING AND PARITY	FC071 FC081 FC091	XM061 XM071 XM081	01A-B2M2	01A-B2L2	01A-B2N2	01A-B2N2
ADDRESS GENERATION AND COMPARE	FC101 FC121	XM091 XM111				
SERVICE LOGIC	FC111					
TIE BREAKER LOGIC		XM101				
INITIAL SELECTION LOGIC	FC141 FC151	FC141 FC151				
INTERFACE BRANCH CONDITIONS TO ALU1	AB161 AB171	AB161 AB171	01A-B2L2	01A-B2M2	01A-B2L2	01A-B2M2
BUS IN ASSEMBLY AND GATING	FC171 FC211	FC171 FC211	01A-A2R2	01A-A2R2	01A-A2R2	01A-A2R2
TAG CABLES	FC291 FC061	XM191 XM055	01A-B2T4 & 01A-B2V4 01A-B2U5 & 01A-B2V5	01A-B2V4 & 01A-B2V5 01A-B2U4 & 01A-B2U5	01A-B2U4 & 01A-B2T5 01A-B2Z5 & 01A B2Z6	01A-B2V2 & 01A-B2V3 01A-B2U2 & 01A-B2U3
BUS CABLES	FC291 FC061	XM191 XM055	01A-B2U2 & 01A-B2V2 01A-B2T3 & 01A-B2V3	01A-B2T4 & 01A-B2T5 01A-B2T2 & 01A-B2T3	01A-B2Y5 & 01A-B2Y6 01A-B2T2 & 01A-B2U3	01A-B2Y5 & 01A-B2Z5 01A-B2Y6 & 01A-B2Z6

Note 1: Removing this card may cause channel errors, even with power off. Put processing unit in single cycle mode before removing card.

Note 2: Trapping ALU errors online with the Control Check Switch ON may cause severe impact on customer operations. Make use of the channel retry feature on System 370 CPUs. Place the CPU in hard-stop mode before activating the Control Check switch. Use the hard-stop mode that ignores recoverable storage errors. When the ALU stops (1) obtain the required information from the CE panel, (2) turn OFF the Control Check switch, (3) switch the CPU to Process, and (4) start the CPU. This allows the channel retry hardware and software to recover. Recovery is only possible on intermittent ALU errors.

EXTRA OR MISSING INTERRUPTS

There are six cards that usually fix all interrupt problems. The symptoms (and normal fix) are listed below.

Example: If there are extra interrupts, the cards that are affected are A2D2, A2R2.

Symptom/Most Probable Cause:

1. Missing Interrupts:

   A2D2, A2N2, A2R2, A2Q2

2. Extra Interrupts:

   A2D2, A2R2

3. Interrupts from the wrong device:

   A2T2

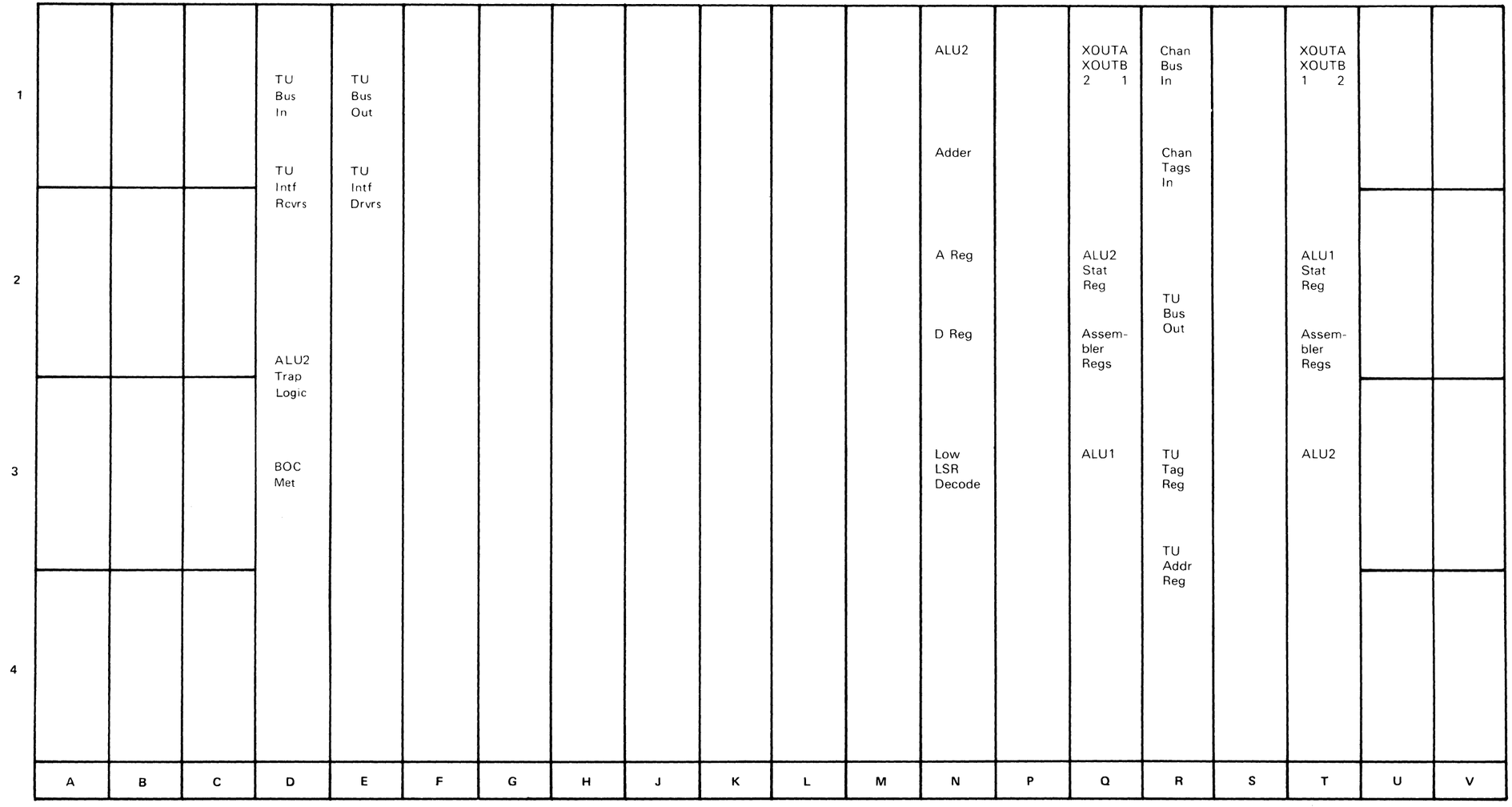
4. Lost Device End or a solid Device Busy:

   A2D2 or the switch logic card (go to 18-010 for the switch).

5. Random device failures:

   A2E2

A2 Panel



TAPE CONTROL METERING PROBLEMS

From: START 1, 00-010, 00-040

DESCRIPTION OF METERING:
The tape control usage meter should run when METERING OUT is active from either channel interface and that interface is Enabled. The tape unit usage meter should run whenever the tape control usage meter is running and the tape unit is away from load point.

Most Probable Cause:

1. Only tape control usage meter failing: With EC733814—B2S2 (See CAUTION) Without EC733814—B2R2 (See CAUTION)
2. Only tape unit usage meter or meters failing: A2E2.
3. Tape control and tape unit usage meters failing: CHAN A — B2Q2(See CAUTION) CHAN B — B2P2 (See CAUTION) Both CHAN A and CHAN B — B2Q2 (see CAUTION)
4. One tape unit failing:
   A. T-A1L2
   B. T-A1F2
   C. T-A1K4
   D. T-A1J2

CAUTION: Removing this card may cause channel errors, even with power off. Put processing unit in single cycle mode before removing card.

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise. **Remember** to END all problem or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Is the failing meter running all the time?	Go to Seq 21.
2	Does the meter fail to run when only interface B is active?	Go to Seq 29.
3	Are the tape unit meters running and the tape control meter not running?	Go to Seq 14.
4	Is the tape control meter running and the tape unit meters not running?	Go to Seq 7.
5	Ensure that Channel A is enabled and METERING OUT is active at the channel. Scope +IF METERING OUT CHAN A (B2Q2J13) (channel interface level). Is this line active? (+3 vdc)	Change B2Q2. (See CAUTION)
6	If not:	Go to ALD FC011 and follow line back to failing point.
7	Does the tape control have Selection Logic? (1x8)	Go to Seq 12.
8	Scope the following points (device interface levels): A2E2P03 — RUN METER SECONDARY A2E2M03 — RUN METER PRIMARY Is either line inactive? (+4.4 vdc)	Go to Seq 10.
8A	Scope T-A1L2P05 in the failing tape unit (-METER OUT I/O). Is this line active? (Ground level) ailure is in tape unit. Go to Seq 32.	
9	If not:	Go to 18-010.
10	Scope +RUN METER (A2E2P04). Is this line active? (-0.85 vdc)	Change A2E2.
11	If not:	Go to XC101 and follow line back to failing point.
12	Scope the following points (device interface levels): A2E2U09 — RUN METER DRIVE 0 A2E2J12 — RUN METER DRIVE 1 A2E2G12 — RUN METER DRIVE 2 A2E2D06 — RUN METER DRIVE 3 A2E2S03 — RUN METER DRIVE 4 A2E2U02 — RUN METER DRIVE 5 A2E2M02 — RUN METER DRIVE 6 A2E2B05 — RUN METER DRIVE 7 Are any of the lines inactive? +4.4 vdc	Go to Seq 10.
12A	Scope T-A1L2P05 in the failing tape unit (-METER OUT I/O). Is this line active? (Ground level) ailure is in tape unit. Go to Seq 32.	
13	If not:	Go to 18-010, Chart F.
14	Scope –PICK METER RLY (device interface level): With EC733814—B2S2M05 Without EC733814—B2R2M05 Is this line active? (Ground)	Go to Seq 17.
15	Scope +RUN METER: With EC733814—B2S2J06 Without EC733814—B2R2J06 Is this line active? (-0.85 vdc)	With EC733814—change B2S2 Without EC733814—change B2R2 (See **CAUTION**)
16	If not:	Go to ALD FC261 and follow line back to failing point.
17	Check meter card voltages as follows: Remove the four mounting screws holding the black panel over the back of the meter. Break the top off the plastic tamper-proof plug. Turn off tape unit power and remove the two screws holding the cover over the meter card. Check between the following points on the meter card: 3-4 should be approximately 41 V ac 5-9 should be approximately 6 V dc Are these voltages present?	Go to Seq 19.
18	If not:	Go to ALD YF033 and follow incorrect or missing voltage back to locate failure.
19	Short terminal 4 to terminal 5. Does the meter run?	Change meter card.
20	If not:	Change meter.
21	Is the failing meter in a tape unit?	Go to Seq 24.
22	Disable interface. Scope –PICK METER RLY: With EC733814—B2S2M05 Without EC733814—B2R2M05 Is this line active? (Ground)	Go to ALD FC261 and follow –PICK METER RLY line back to failing point.
23	If not:	Change meter card. See Seq 17 to gain access to meter card.
24	Does the tape control have Selection Logic? (1x8)	Go to Seq 27.
25	Disable interfaces. Scope the following points (device interface levels): A2E2P03 — RUN METER SECONDARY A2E2M03 — RUN METER PRIMARY Is either line active? (Ground)	Change A2E2.
25A	Scope T-A1L2P05 in the failing tape unit (-METER OUT I/O). Is this line inactive? (+4.4 vdc) Failure is in tape unit. Go to Seq 32.	
26	If not:	Go to 18-020.
27	Disable interfaces. Scope the following points (device interface levels): A2E2U09 — RUN METER DRIVE 0 A2E2J12 — RUN METER DRIVE 1 A2E2G12 — RUN METER DRIVE 2 A2E2D06 — RUN METER DRIVE 3 A2E2S03 — RUN METER DRIVE 4 A2E2U02 — RUN METER DRIVE 5 A2E2M02 — RUN METER DRIVE 6 A2E2B05 — RUN METER DRIVE 7 Are any of these lines active? (Ground)	Change A2E2.
27A	Scope T-A1L2P05 in the failing tape unit (-METER OUT I/O). Is this line inactive? (+4.4 vdc) Failure is in tape unit. Go to Seq 32.	

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TAPE CONTROL METERING PROBLEMS (Cont'd)

Seq	Condition/Instruction	Action
28	If not:	Go to 18-001, Chart F.
29	Ensure that interface B is enabled, interface A is disabled, and METERING OUT is active at the channel which is connected to interface B. Scope +RUN METER CHAN B (B2Q2J05). Is this line active? (-0.85 vdc)	Change B2Q2. (See CAUTION)
30	Scope +IF METERING OUT CHAN B (B2P2J13). (Channel interface level.) Is this line active? (+3 vdc)	Change B2P2. (See CAUTION)
31	If not:	Go to ALD XM011 and follow line back to failing point.
32	Scope T-A1L2M08. (-RUN METER) Is this line level correct? Ground - Run +12 vdc - Stop Go to ALD ZT001. Check usage meter card inputs.	
33	If not: Go to ALD FT141 and follow line back to failing point.	

18-061

CARD/BOARD FUNCTION LAYOUT

3803-2 A1 Board

Note: Refer to ALD AA005, feature list, if installing new logic board.

	Y1 To Y1Y6			Y2 To Y1Z6				Y3 To B2Y1			Y4 To B2Y3			Y5 To B2Y2		Y6 To A2Y6				
	To Y1V2	16 IND Drivers	Service Logic	Over All CRC	7 Trk	Chnl BFR Checking	Write Gating	A & B BFR		Write OSC	7 Trk 7 Trk OSC					CE Panels Ctrls	CE Panel Ctrls	CE Panel Ctrls	CE Panel Ctrls	To Y1V3 AMP Sense Control To Drive Dead Trk
2	ECC Reg		CE Ripple Gen	Over All Checking	DC and Xlate	Write Format	Write CRC	Encode and Seq		Mode Powering	Misc 7 Trk Ctrls					Comp Gen	CE LSR's	CB1	ALU Hard-ware Error IND Drivers	
	To A2C2	16 IND Drivers	Over All CRC				Write ORC	WR TGRS		Error Latches						In Tags	Master Clock and Controls	CE Entry Drivers		CE Panel
3			RD Reg				Write Clock									Out Tags	Word Select	CE Switch Circuit	Comp Reg	
	To A2A2	To Y1V4	Bus In Assembly				Write Controls									Go Down	Data Entry Select	Sel Reg Decode	Sel Reg IND Drivers	CE Panel
4		Clocks ALU2 XOUTA To DF Controls	Channel BFR Checking													Compare	Sense Byte Gating	ROS Mode Ctrl	ROS Stop Pulses	
	A2B2	To Y1V5 Device	Master Clk and OSC				WR TGR URC				W/O 7 Trk					Multiplier		Stop Circuit		CE Panel
5		Bus In ALU1 XOUTA To DF Controls									TLD Load Card									
	Z1 TO A2Y1			Z2 To A2Y3				Z3 To A2Y3			Z4 To A2Y4			Z5 To A2Y5		Z6 To B2Y4				
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V

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CARD/BOARD FUNCTION LAYOUT

3803-2 Y1 Board

Notes:

1. Refer to ALD AA005, feature jumper list, if installing new logic board.
2. Panel Y1 is located in position 01A-A3, unless the 3803-2 has optional features installed. On feature machines, Panel Y1 is located in position 01B-A1.

S = Interchangeable Cards

	Y1					Y2					Y3					Y4					Y5					Y6 to A1Y1					
1			9 TRK	9 TRK		S1 and S2 Logic	Correction ECC REG	Format Voting	FB Count and Controls	SKB Start Logic ZN 3 1,3,4	SKB Start Logic ZN 2 2,6,7	SKB Start Logic ZN1 P,0,5	ROC Counter	IBG BOR TM, etc.	RD Detection Controls	VFC and Det ZN3 1,3,4	VFC and Det ZN2 2,6,7	VFC and Det ZN1 P,0,5		To A1A2 ECC REG
2			Delay Counter	Single Shots		Error Matrix	Valid Pointers	PE Format Controls	Find I and Pointer	SKB RIC	SKB RIC	SKB RIC	READ READY	DT Latches	PE Sync Correction					
3		TLD Load Card	Char Gate	URC EPR LRC		J and I Logic	Resist Pointers	6250 START STOP Data	ABC Counter	GB,FB XLATE	GB,FB XLATE	GB,FB XLATE	GB Counter	Resync Dead Track Control	Amp SMS Control					To A1V2 Amp Sense Control to Drive
			TM, RDD Restart	Correction		Error Pointers		PE Controls		Skew CK	Skew CK	Skew CK		Start RD Check						Dead Track
4		TLD Load Card		7 TRK Read Amp Control		Pointer Counter		Residual Controls												To A1B4 Clocks XOUTA from ALU2 Controls
						Bus Assembly														
5										S	S	S				S	S	S		To A1B5 Device Bus In ALU1 XOUTA to DF Controls
	Z1					Z2					Z3					Z4					Z5					Z6 to A1Y2					
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V

CARD/BOARD FUNCTION LAYOUT

3803-2 B2 Board

Caution:
Removing the cards may cause channel errors, even with power off. Put CPU in single cycle mode before removing either of these cards

Notes:

1. *Refer to ALD AA005, feature jumper lists, if installing new logic board.*
2. *For machines with EC 733814 installed, reverse B2R2 and B2S2, and also reverse B2L2 and B2M2. The I/O cable socket assigned is also changed. Refer to ALDs.*

S = Interchangeable cards (care must be taken when swapping cards with feature or functional jumpers on them)

B2C2 = A2N2 — B2F2 = A2K2
B2D2 = A2M2 — B2Q2 = B2P2 with 2CS } See CAUTION.
B2E2 = A2L2 — B2R2 = B2S2 with 2CS }
B2J2 = A2G2

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V
1	Y1 To A1Y3			Y2 To A1Y5				Y3 To A1Y4			Y4 To A1Z6			Y5 To 01S-A1A5				Y6 To 01S-A1A6		
2	To A2V2	To A2U2	ALU1 Adder	ALU1 ROS Reg. P, 0-7	ALU1 ROS Reg. P, 8-15	ALU1 Clock	ALU1 CE Sel. Reg.	ALU1 ROS	ALU1 Array Patch Card	Chan A Chan B Select Out Bypass Relay	Chan. A Addr. Comp. and Emit	Basic Intf. Branch Conds.	Chan. B Addr. Comp. and Emit	Chan. B In Tags	Chan. A In Tags	Chan. A Bus. In	Chan. B Bus. In	To 01S A1B5	To 01S A1B6	To 01S A1B2
3	To A2V3	R P Q	A Reg. D Reg.	Inst. Decode Branch Ctrl. Page	Inst. Ctr. Xfer. Decode						Bus. Out Check and Gating		Bus. Out Check and Gating	Out Tags Meter Sel. Out Bypass Logic	Out Tags Meter Sel. Out Bypass Logic	Sel. Out Bypass Relay	Sel. Out Bypass Relay	To 01S A1A1	To 01S A1B6	To 01S A1B1
4	To A2V4		Low LSR Decode	BOC Met High LSR Decode	Low IC Parity					Power On Reset Degate Chan. Intf. S	Serv. In Serv. Out See Note 2.	See Note 2.	Tie Breaker Logic	See CAUTION, and Note 1.	See CAUTION, and Note 1.	See CAUTION, and Note 1.	See CAUTION, and Note 1.	To 01S A1B3	To 01S A1B7	To 01S A1A3
5	To A2V5	To A2U5	S	S	S	S			S	Term Rstrs. S				S ◄► S		S ◄► S		To 01S A1B8	To 01S A1B4	To 01S A1A4
6	Z1			Z2				Z3			Z4			Z5 To 01S-A1A8				Z6 To 01S-A1A7		

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CARD/BOARD FUNCTION LAYOUT

3803-2 A2 Board – 1x8 Machines

Note: *Refer to ALD AA005 feature jumper lists, if installing new board.*

S = Interchangeable cards (care must be taken when swapping cards with feature or functional jumpers on them)

A2C3 = B2K5 A2M2 = B2D2
A2K2 = B2F2 A2N2 = B2C2
A2L2 = B2E2 A2P2 = A2P3 = B2K4
A2G2 = B2J2

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V
1	Y1 To A1Z1			Y2 To A1Z2			Y3 To A1Z3				Y4 To A1Z4			Y5 To A1Z5				Y6 To A1Y6		
2	To A1A4	To A1A5	To A1A3	TU Bus In	TU Bus Out		ALU2 Array Patch Card				ALU2 ROS Reg P, 8-15	ALU2 ROS Reg P, 0-7		Com. 2 Feature CU Power Down Sec. S	XOUTA XOUTB 2 → 1	Chan. Bus In		XOUTA XOUTB 1 → 2	To B2B2	To B2A2
3	To B3Y1 Add 0-3 Run Meter Busy/Tach. DE Interrupt	To B3Y2 Add 4-7	Term. Rstrs. S	TU Intf. Rcvrs.	TU Intf. Drvrs.			ALU2 ROS	ALU2 CE Select Reg. P-11	ALU2 Clock	Inst. Ctr. Xfer. Decode	Inst. Decode Branch Ctrl.	ALU2 Adder A Reg.	Power On Reset CU Power Down Pri. S	ALU2 Stat. Reg.	Chan. Tags In TU Bus Out		ALU1 Stat. Reg.	R P Q	To B2A3
4		To B3Y3 Select Xpt. 0-7		ALU2 Trap Logic							Low IC Parity	Page Reg. BOC Met	D Reg. Low LSR Decode	Hrdwr. Error Latches	Assem-bler Regs. ALU1	TU Tags Reg. TU Addr. Reg.		Assem-bler Regs. ALU2		To B2A4
5		To B3Z1 Device Bus In P-7	To B3Y5 Bus Out P-7 Cmd. Ctrl. Move Tags	BOC Met			S			S	S	S	S	Trap Logic ALU1 and ALU2					To B2B5	To B2A5
6	Z1			Z2			Z3				Z4			Z5				Z6 RPQ		

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3803-2 B3 Board – 1x8 Machine

S = Interchangable cards

B3D2 = B3F2
B3Q2 = B3S2

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V
1	Y1 To A2A3 Add 0-3 Run Meter - Busy			Y2 To A2B3 Add 4-7 Tach. - DE Interrupt				Y3 To A2B4 Sel. Xpt. 0-7			Y4			Y5 To A2C5 Bus Out Cmd. Ctrl. Move Tags				Y6		
2	To I/O Gate Bus In 0	To I/O Gate Bus In 4		CU A Bus In 0-3		CU A Bus In 4-7								CU A Bus Out and Tags 4-7		CU A Bus Out and Tags 0-3		To I/O Gate Bus Out and Tags 4	To I/O Gate Bus Out and Tags 0	
3	To I/O Gate Bus In 1	To I/O Gate Bus In 5																To I/O Gate Bus Out and Tags 5	To I/O Gate Bus Out and Tags 1	
4	To I/O Gate Bus In 2	To I/O Gate Bus In 6																To I/O Gate Bus Out and Tags 6	To I/O Gate Bus Out and Tags 2	
5	To I/O Gate Bus In 3	To I/O Gate Bus In 7		S	←	S								S		←	S	To I/O Gate Bus Out and Tags 7	To I/O Gate Bus Out and Tags 3	
6	Bus In P-7 Z1 To A2B5			Z2				Z3			Z4			Z5				Z6		

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CARD/BOARD FUNCTION LAYOUT

A2 Board – 2x8 Machines

S = Interchangable cards (care must be taken when swapping cards with feature or functional jumpers on them)

A2G2	=	**B2J2**					
A2C3	=	B2K5	A2M2	=	B2D2		
A2K2	=	B2F2	A2N2	=	B2C2		
A2L2	=	B2E2	A2P4	=	A2P3	=	B2K4

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V
1	Y1 To A1Z1			Y2 To A1Z2			Y3 To A1Z3				Y4 To A1Z4			Y5 To A1Z5				Y6 To A1Y6		
2	To A1A4	To A1A5	To A1A3	TU Bus In	TU Bus Out		ALU2 Array Patch Card	ALU2 ROS	ALU2 Select Reg. P-11	ALU2 Clock	ALU2 ROS Reg P.8-15	ALU2 ROS Reg. P.0-7	ALU2	Com. 2 Feature CU Power Down Sec. S	XOUTA XOUTB 2 → 1	Chan. Bus In		XOUTA XOUTB 1 → 2	To B2B2	To B2A2
3	To I/O Tail Gate	To B3Z3 Addr. and Sel	Term. Rstr. S	TU Intf. Rcvrs.	TU Intf. Drvrs.						Inst. Ctr Xfer Decode	Inst. Decode Branch Ctrl.	Adder A Reg.	Power On Reset Cu Power Down Pri S	ALU2 Stat. Reg.	Chan. Tags In TU Bus Out		ALU1 Stat. Reg.	R P Q	To B2A3
4	To I/O Tail Gate	To I/O Tail Gate	To I/O Tail Gate	ALU2 Trap Logic							Low IC Parity	Page Reg. BOC Met	D Reg.	Hrdwr. Error Latches	Assem-bler Regs. ALU1	TU Tags Reg.		Assem-bler Regs. ALU2		To B2A4
5	To B3Z5 Busy Tach. Dev. Intrpt. Gate Bus Out	To B3Z1 Dev. Bus In P-7	To B3Y5 Dev. Bus Out P-7 Cmd. Ctrl. Move Tags	BOC Met			S			S	S	S High LSR Decode	S Low LSR Decode	Trap Logic ALU1 and ALU2		TU Addr. Reg			To B2B5	To B2A5
6	Z1			Z2			Z3				Z4			Z5				Z6 RPQ		

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CARD/BOARD FUNCTION LAYOUT

3803-2 B3 Board – 2x8 Machines

S=Interchangeable Cards

B3D2 · B3E2 = B3F2 = B3G2
B3P2 · B3Q2 · B3R2 = B3F2

Address Notation Equates 0-3 = 8-B
A-7 = C-F

	Y1			Y2				Y3			Y4			From Host: Y5 To A2C5 Bus Out Cmd ,Ctrl ,Move Tags				From Communicator: Y6 To I/O Gate-Bus Out Cmd ,Ctrl ,Move Tags		
1	To I/O Gate	To I/O Gate		CU A	CU B	CU A	CU B	CU A	CU B	CU A	CU B			CU B	CU A	CU B	CU A		To I/O Gate	To I/O Gate
2	Bus In 0	Bus In 4		Bus In 0-3	Bus In 0-3	Bus In 4-7	Bus In 4-7	Logic 0-3	Logic 0-3	Logic 4-7	Logic 4-7			Bus Out and Tags 4-7	Bus Out and Tags 4-7	Bus Out and Tags 0-3	Bus Out and Tags 0-3		Bus Out and Tags 4	Bus Out and Tags 0
3	To I/O Gate Bus In 1	To I/O Gate Bus In 5	Enable Switches CU A and B					Load Card For Logic "A"	Load Card For Logic "B"										To I/O Gate Bus Out and Tags 5	To I/O Gate Bus Out and Tags 1
4	To I/O Gate Bus In 2	To I/O Gate Bus In 6		Selects Xpts				Logic						Selects Xpts					To I/O Gate Bus Out and Tags 6	To I/O Gate Bus Out and Tags 2
5	To I/O Gate Bus In 3	To I/O Gate Bus In 7		S ↔ S	S ↔ S	S ↔ S	S ↔ S							S ↔ S	S ↔ S	S ↔ S	S ↔ S		To I/O Gate Bus Out and Tags 7	To I/O Gate Bus Out and Tags 3
	Z1 To A2B5 Bus In P-7			Z2 To I/O Gate Bus In P-7				Z3 To A2B3 Addr. and Select			Z4 To I/O Gate Addr. and Select			Dev OP-Busy Tach.,DE Intf. Z5 To A2A5 Gate Bus Out					Dev. P-Busy Tach.,DE Intf. Z6 To I/O Gate Bus Out	
6	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V
	To Host			To Communicator				From Host			From Communicator			To Host				To Communicator		

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CARD/BOARD FUNCTION LAYOUT

3803-2 A2 Board – 3x8 or 4x8 Machines

S=Interchangeable Cards (care must be taken when swapping cards with feature or functional jumpers on them)

A2G2	=	B2J2				
A2C3	=	B2K5	A2M2	=	B2D2	
A2K2	=	B2F2	A2N2	=	B2C2	
A2L2	=	B2E2	A2P2	=	A2P3	= B2K4

	Y1 To A1Z1			Y2 To A1Z2			Y3 To A1Z3				Y4 To A1Z4			Y5 To A1Z5				Y6 To A1Y6		
1																				
2	To A1A4	To A1A5	To A1A3	TU Bus In	TU Bus Out		ALU2 Array Patch Card	ALU2 ROS	ALU2 CE Sel Reg P-11	ALU2 Clock	ALU2 ROS Reg P.8-15	ALU2 ROS Reg P.0-7	ALU2 Adder	Com 2 CU Power Down Sec	XOUTA XOUTB 2 → 1	Chan Bus In		XOUTA XOUTB 1 → 2	To B2B2	To B2A2
3	To I O Tail Gate	To A3A4 CU A Out Bound Logic	Term Rstrs S	TU Intf Rcvrs	TU Intf Drvrs						Inst Ctr Xfer Decode	Inst Decode Branch Ctrl	A Reg D Reg	Power On Reset CU Power Down Pri S	ALU2 Stat Reg	Chan Tags In TU Bus Out		ALU1 Stat Reg	R P Q	To B2A3
4	To I O Tail Gate	To I O Tail Gate		ALU2 Trap Logic							Low IC Parity	Page Reg BOC Met	Low LSR Decode	Hrdwr Error Latches	Assem-bler Regs ALU1	TU Tags Reg TU Addr Reg		Assem-bler Regs ALU2		To B2A4
5	To A3Y5 CU A In Bound Logic	To B3Y3 CU A Bus In	To B3Y4 CU A Bus Out and Tags	BOC Met			S			S	S	S	S	Trap Logic ALU1 and ALU2					To B2B5	To B2A5
6	Z1			Z2			Z3				Z4			Z5				Z6 RPQ		
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V

3803-2/3420

XF7100 Seq 2 of 2	2735967 Part Number	See EC History	845958 1 Sep 79	846627A 3 Dec 80				

CARD/BOARD FUNCTION LAYOUT

3803-2 B3 Board – 3x8 or 4x8 Machines

S = Interchangeable Cards

B3C2 = B3D2 = B3E2 = B3F2 = B3G2 = B3H2 = B3J2 = B3K2
B3L2 = B3M2 = B3N2 = B3P2 = B3Q2 = B3R2 = B3S2 = B3T2

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V
1	Y1 To A3V3 0-3,8-B Busy,Interrupt,Meter			Y2 To I/O Gate CU B Bus In				Y3 To A2B5 CU A Bus In			Y4 To A2C5 CU A Bus Out			Y5 To I/O Gate CU B Bus Out				Y6 To A3Y4 CU A,B Sel. Xpt.		
2	To I/O Gate Bus In 0,8	To I/O Gate Bus In 4,C	CU A 0-3 or 8-B	CU B 0-3 or 8-B	CU C 0-3 or 8-B	CU D 0-3 or 8-B	CU A 4-7 or C-F	CU B 4-7 or C-F	CU C 4-7 or C-F	CU D 4-7 or C-F	CU D 4-7 or C-F	CU C 4-7 or C-F	CU B 4-7 or C-F	CU A 4-7 or C-F	CU D 0-3 or 8-B	CU C 0-3 or 8-B	CU B 0-3 or 8-B	CU A 0-3 or 8-B	To I/O Gate Bus Out 4,C	To I/O Gate Bus Out 0,8
3	To I/O Gate Bus In 1,9	To I/O Gate Bus In 5,D					Bus In							Bus Out and Tags					To I/O Gate Bus Out 5,D	To I/O Gate Bus Out 1,9
4	To I/O Gate Bus In 2,A	To I/O Gate Bus In 6,E																	To I/O Gate Bus Out 6,E	To I/O Gate Bus Out 2,A
5	To I/O Gate Bus In 3,B	To I/O Gate Bus In 7,F	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	To I/O Gate Bus Out 7,F	To I/O Gate Bus Out 3,B
6	Busy, Interrupt, Meter Z1 To A3V2 4-7,C-F			CU D Bus In Z2 To I/O Gate				CU C Bus In Z3 To I/O Gate			CU C Bus Out Z4 To I/O Gate			CU D Bus Out Z5 To I/O Gate				CU C, D Sel. Xpt. Z6 To A3Y5		

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XF7200 Seq 1 of 2	2735968 Part Number	See EC History	845958 1 Sep 79					

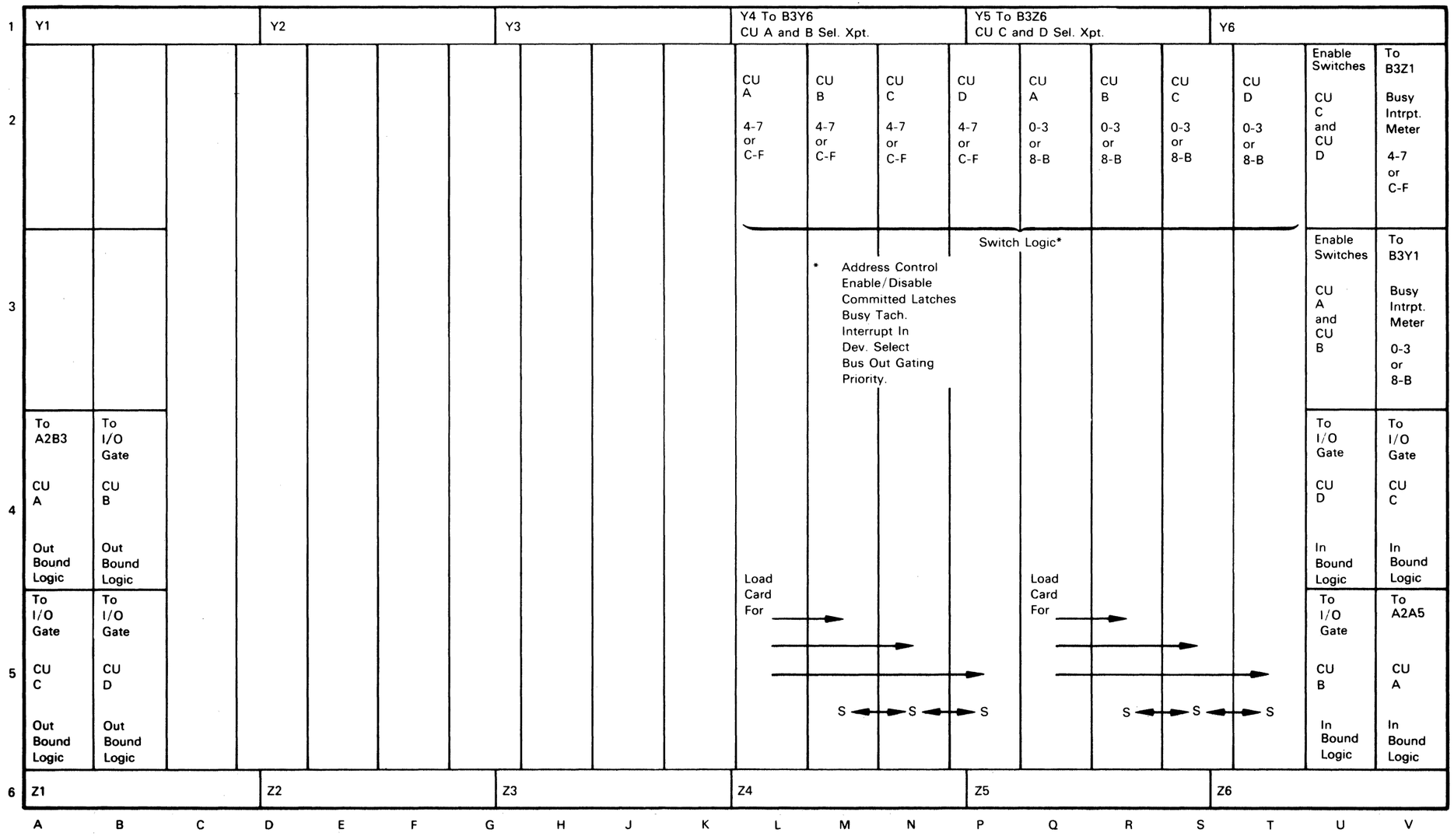
CARD/BOARD FUNCTION LAYOUT

3803-2 A3 Board – 3x8 or 4x8 Machines

Notes: Care must be taken when swapping these cards with another machine. Address jumpering may be different, whereas the addresses are plugged the same within one machine. Priority jumpers with not affect operation unless cards are swapped between machines.

S = Interchangeable Cards

A3M2 = A3N2 = A3P2
A3R2 = A3S2 = A3T2



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XF7200 Seq 2 of 2	2735968 Part Number	See EC History	845958 1 Sep 79					

CARD/BOARD FUNCTION LAYOUT

3420 Models 3, 5, 7 A1 Board

	A	B	C	D	E	F	G	H	J	K	L	M	N
1					Connector		Connector				Terminator		
2	Connector	Reel Control	Rewind Gated Ready Load Complete Push Buttons Cartridge and Door Interlock	Photo Detection	Load OP Thread Status Load Check Tape Present Load Rewind Reels Loaded	Load Point Status Backward	Capstan Control	Status Multi-Plexing 0-7 Write Status Drive Write Fail Detect Erase Power On and Sense Resets Sense Decode Interrupt Generation Unit Check Mech. Ready	TCU Interface Interface Decode Write Select Write Current Control Write Data Gating Sense Level Control Degauss EOT	NZRI 7–9 TRK Write Deskew P,0-7 Bus Out Tag Out	Interface Bus In ID Gating Read Select Sense Byte 3,4,5 Decode Tach/ Busy Metering Loop Gating	NRZI 7–9 TRK Read Deskew P,0-7	Connector
3	Connector			Unused									Connector
4	Connector		Columns Loaded and Unloaded		Window Up/Down Pneumatic Drive Cartridge	Capstan Drive IBG Control							Connector
5	Connector		Unload Complete Manual Status Control		Air Pressure Detection								Unused
6	Unused	Unused	Unused		Unused	Unused	Unused	Unused	Unused	Unused	Off Line Relay	Unused	
7											Unused		

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XF7300 Seq 1 of 2	**2735969** Part Number	**See EC History**	**845958** 1 Sep 79	**847298** 15 Agu 83				

CARD/BOARD FUNCTION LAYOUT

3420 Model 4, 6, 8 A1 Board

CAUTION: Refer to ALD A6106, feature jumper list, if installing new logic board.

1				Connector		Connector			Terminator			
2	Cartridge Switches Connector Air Bearing Pressure Switch	Capstan Control (Rewind)	Rewind Gated Ready Load Complete	Photo Detection	Capstan Control Proportional Drive Counter	Capstan Control Go	Auto Cleaner Control	Capstan Control	Interface Decode	Zero Threshold	Interface Bus–In ID Gating	Status Multi Plexing 0-7 Write Status Drive	Interrupt In Bus In Connector Tach/Busy
3	EOT/BOT Connector	Reel Control	Push Buttons Cartridge and Door Interlock	Cartridge Controls Window Up/Down	Polarity Hold Drive Register	IBG Counter	Capstan Control	Reel Control (Rewind)	Write Select Write Current Control	Erase Status	Read Select Sense Byte 3,4,5 Decode	Sense Decode Power On & Sense Resets Erase	Read Data Connector SAGC Check
4	Reel Control Connector	Vacuum Switches	Columns Loaded and Unloaded	Thread Status Air Pressure Detection		Forward Hitch	Load Point Status	Crease Tape Control	Write Data Gating Sense Level Control	Density Select Status Bus	Tach/Busy Metering Feature Jumpers	Mech. Ready Unit Check Interrupt Generation	Bus Out Connector
5	Connector Vacuum Switches		Unload Complete Manual Status Control	Load Rewind					Degauss EOT		Loop Gating		Unused Tape Unit Tester (Pin Side)
6	Unused	Unused	Unused	Load Check Reels Loaded	Unused	Unused	Capstan Control Tach Pulse Counter	Unused	Unused	Tape Unit Bus & Tags From T.C.U.	Off Line Relay	Unused	Unused
7	Unused						ROS				Unused		Connector (Auto Cleaner)
	A	B	C	D	E	F	G	H	J	K	L	M	N

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XF7300 Seq 2 of 2	2735969 Part Number	See EC History	845958 1 Sep 79	847298 15 Aug 83				

3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
A1B2D07	–END DATA CHECK	BW241FG6	PP061	17-540	
A1C2B02	+0 PCT AMP CTRL TRK2	CB13FC6	BS071	15-040	
A1C2B03	+5.12 MHZ	BS011EH6	BS011	13-010	
A1C2B07	–CROC REG 8	BR001GN2	BS061	17-010	
A1C2B09	–CROC REG 4	BR001EL2	BS061	17-010	
A1C2B12	–GATE TIE	PR161GM6	BS071	13-480	
A1C2D04	+BUS IN BIT 2	BS071GD2	BS071	15-080	
			BS071	15-100	
A1C2D06	+BUS IN BIT 3	BS071GD7	BS071	15-080	
			BS071	15-100	
A1C2D07	–CROC REG 16 OR NOT RD CYC	BR001EN2	BS061	17-010	
A1C2D09	–CROC REG 2	BR001GL2	BS061	17-010	
A1C2D10	–CROC REG 1	BR001CL2	BS061	17-010	
A1C2D13	+BUS IN BIT 6	BS071GK2	BS071	15-080	
			BS071	15-100	
A1C2G02	+BUS IN BIT 7	BS071GK7	BS071	15-080	
			BS071	15-100	
A1C2G05	–SET WRT REGISTER	BS031ED6	BS031	17-010	
A1C2G07	+BUS IN BIT 5	BS071EG7	BS071	15-080	
			BS071	15-100	
A1C2G09	+BUS IN BIT 0	BS071EA2	BS071	15-080	
			BS071	15-100	
A1C2G12	+BUS IN BIT 1	BS071EA7	BS071	15-080	
			BS071	15-100	
A1C2G13	+DATA IN	BS041GJ6	BS041	13-100	
A1C2J03	–5.12 MHZ	BS011EH2	BS011	13-450	
A1C2J04	+BUS IN BIT 4	BS071EG2	BS071	15-080	
			BS071	15-100	
A1C2J06	–20.48 MHZ	BS011GJ6	BS011	13-010	
A1C2J07	+CRIC REG 1 POWERED	BR041EB0	BS061	17-010	
A1C2J09	+CE MODE	PK011FH2	BS071	13-480	
A1C2J10	–READ AND TAPE OP	BW231GL6	BS091	15-040	
			BS091	17-010	
A1C2J11	–SPARE XFER 18	AA171EK6	BS061	17-010	
A1C2J13	–DATA IN	BS041GJ2	BS041	13-480	
A1C2M07	–SERVICE RESPONSE	FC111GM2	BS031	13-480	
			BS031	15-040	
			BS031	17-010	
A1C2M08	–SERVICE OUT	FC111FE2	BS041	17-370	
A1C2M11	–TAPE OP A	BW231EK6	BS031	17-010	
A1C2P03	–WRT BUFFER OVERRUN	BW151FM6	BS061	17-010	
A1C2P04	+WRT ADDRESS ERROR TP	BS061EA2	BS061	17-010	
A1C2P05	+RESET SENSE DATA	AB181CK2	BS041	13-480	
			BS061	13-480	
A1C2P06	+WRITE SERVICE IN	BS031GD2	BS031	15-040	
A1C2P06	+SERVICE IN FOR DATA	BS041GG4	BS041	13-100	
			BS041	13-480	
A1C2P07	+BUFFER WRITE CYCLE	BR011EL6	BS031	15-040	
A1C2P12	–WR AND TAPE OP NOT CTL	BW231GA6	BS031	13-480	
			BS031	15-040	
			BS031	17-010	
A1C2S04	–WRT DATA READY	BS031FB6	BS031	15-040	
			BS031	17-010	
A1C2S05	–BFR ERROR TP	BS061GK6	BS061	17-010	
A1C2S07	–READ BYTE BUFFER EMPTY	BS041AC2	BS041	17-010	
A1C2S10	–0-50 CLOCK BUS A1 DELAYED	BS021FG8	BS021	17-010	
			BS021	17-160	
			BS021	17-800	
A1C2S12	–0-50 CLOCK BUS YA	BS021FD9	BS021	17-160	
			BS021	17-800	
A1C2S13	–25-75 CLOCK BUS YB	BS021FG0	BS021	17-160	
			BS021	17-800	
A1C2U04	–20.48 MHZ		BS011	13-010	
A1C2U05	+DATA OUT	FC021GA4	BS041	13-480	
A1C2U06	–CHANNEL BUFFER OUT P	BR031GC6	BN321	17-010	
A1C2U09	–0-50 CLOCK BUS YB	BS021FD0	BS021	17-160	
			BS021	17-800	
A1C2U11	–25-75 CLOCK BUS YA	BS021FG9	BS021	17-160	
			BS021	17-800	
A1C2U12	–25-75 CLOCK BUS A1 DLYD	BS021FD1	BS021	17-010	
			BS020	17-800	
A1C2U13	–50-100 CLOCK BUS	BS021FG2	BS021	17-800	
A1D2D10	–SERVICE RESPONSE	FC111GM2	BK001	13-480	
A1D2J04	–BUFFER CRC ERR	BK041EN6	BK001	17-530	
A1D2J05	–BUFFER CRC P COMP TP	BK041FN6	BK001	17-010	
A1D2J10	–B EQUAL A TP	BK031FF4	BK041	17-010	
A1D2M05	–BYTE REG 1 NOT 1-2-4	BR001FA6	BK001	17-540	
A1D2M07	–CROC REG 16 OR NOT RD CYC	BR001EN2	BK001	17-540	
A1D2M10	–CROC REG 8	BR001GN2	BK001	17-540	
A1D2M11	–CHB CRC OR RES BIT 5	BK001ED6	BK001	17-540	
A1D2M12	–CROC REG 4	BR001EL2	BK001	17-540	
A1D2M13	–CHB CRC OR RES BIT 0	BK001AB6	BK001	17-540	
A1D2P03	–ALLOW CRIC	CH141FG2	BK041	17-010	
A1D2P04	–CHB CRC OR RES BIT 2	BK001CB6	BK001	17-540	
A1D2P05	–SPARE XFER 18	AA171EK6	BK041	17-530	
A1D2P06	+1 OR 2 TRK CORR TP	CB431EE6	BK001	15-140	
A1D2P07	–CHB CRC OR RES BIT 3	BK001CD6	BK001	17-540	
A1D2P09	–CHB CRC OR RES BIT 4	BK001EB6	BK001	17-540	
A1D2P12	+SET WRITE REGS	BK031CL2	BK031	17-010	
A1D2S02	–BYTE REG 4 NOT 1-2-4	BR001FE6	BK001	17-540	
A1D2S03	–BYTE REG 2 NOT 1-2-4	BR001FC6	BK001	17-540	
A1D2S07	–CRC CONTROL	BR051FL6	BK001	17-540	
A1D2S10	–CHB CRC OR RES BIT 6	BK001GB6	BK001	17-540	
A1D2S11	–CROC REG 2	BR001GL2	BK001	17-540	
A1D2S13	–CROC REG 1	BR001CL2	BK001	17-540	
			BK001	17-590	
A1D2U03	–CHB CRC OR RES BIT 1	BK001AD6	BK001	17-540	
A1D2U13	–CHB CRC OR RES BIT 7	BK001GD6	BK001	17-540	
			BK001	17-590	
A1E2G02	+SET BYTE 2 FROM DC A	BN011EK2	BN011	17-010	
A1E2G07	–BUFFER EMPTY TO CHANNEL	BN011GA6	BN011	17-010	
A1E2J07	–WRITE GROUP BUFFER EMPTY	BW151GG6	BN091	13-480	
A1E2J10	–PARTIAL OR LAST FRAME	BR001DF6	BN031	13-480	
A1E2J13	–EOD NRZI	CN281FL6	BN071	15-070	
A1E2M12	–DATA CONVERTER ON	BN311DK6	BN051	13-480	
			BN051	17-010	
A1E2P02	–REQ CB WRT CYCLE	CH021GE2	BN071	17-370	
A1E2P09	–STATE BIT 3 7-TRACK	AA141EG6	BN051	13-480	
			BN051	17-010	
A1E2S10	+FOURTH BYTE	BN011ED6	BN011	17-010	
A1F2B02	–STEP BYTE COUNTER	BR051GK6	BR051	13-480	
A1F2B03	–CRC CONTROL	BR051FL6	BR051	17-540	

3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
A1F2B04	–ALLOW CRIC	CH141FG2	BR061	13-480	
			BR011	17-010	
			BR011	17-370	
A1F2B05	–READ CYCLE	BR011GE6	BR011	13-480	
			BW141	17-010	
			BR011	17-170	
			BR011	17-540	
A1F2B07	–CHANNEL BUFFER OUT 5	BR031GJ6	BR031	17-010	
A1F2B10	–CHANNEL BUFFER OUT 6	BR031GK6	BR031	17-010	
A1F2B13	+SET BYTE 2	BR041GL4	BR041	17-010	
A1F2D02	+COMBINED RESID 32 CMPR	CK001CK4	BR061	15-040	
A1F2D03	–REQ CB WRITE CYC DOT	BR111BK4	BR061	15-040	
			BR071	17-370	
A1F2D04	–OVERRUN	BR021GG6	BR021	15-040	
A1F2D05	–CB WRITE PULSE	BR011GL6	BR011	17-010	
A1F2D07	–CHANNEL BUFFER OUT 4	BR031GH6	BR031	17-010	
A1F2D09	–CHANNEL BUFFER OUT 3	BR031GG6	BR031	17-010	
A1F2D10	+READ CYCLE RESET	BR071FJ2	BR011	17-010	
			BR071	17-370	
A1F2D12	–CHANNEL BUFFER OUT 7	BR031GL6	BR031	17-010	
A1F2D13	+SET BYTE 4	BR041GN2	BR041	17-010	
A1F2G02	+BUFFER WRITE CYCLE	BR011EL6	BR011	13-480	
			BR011	15-040	
A1F2G03	+CRIC REG 1 POWERED	BR041EB0	BR041	17-010	
A1F2G04	–50-100 CLOCK BUS A1 DELAYED	BS021FG2	BR061	13-480	
			BR061	15-040	
A1F2G05	–WRITE GROUP BUFFER EMPTY	BW151GG6	BR071	17-010	
A1F2G07	–END WRITE SEQUENCE	BR041GF6	BR041	17-010	
			BR001	17-590	
A1F2G08	+SET BYTE 3	BR041GK2	BR041	17-010	
A1F2G09	–6250 MODE	BW231GH6	BR001	17-020	
A1F2G11	+STOP TO DATA FLOW	FC111AM6	BR061	13-480	
			BR001	15-040	
A1F2G13	–WRT AND TAPE OP NOT CTL	BW231GA6	BR061	17-540	
			BR071	15-040	
			BR071	17-020	
			BR071	17-160	
			BR071	17-170	
			BR071	17-700	
A1F2J02	+SET WRITE DATA B	BR101BL4	BR041	13-480	
A1F2J07	+SET BYTE 1	BR041GJ2	BR041	17-010	
A1F2J09	+WRITE CYCLE DELAYED	BR011BD2	BR011	17-010	
A1F2J10	–FULL FRAME	BR001AF6	BR001	13-480	
			BR001	17-010	
			BR001	17-540	
A1F2J13	–READ AND TAPE OP	BW231GL6	BR071	17-170	
			BR071	17-370	
A1F2M05	–ORC GATE	BR051GH6	BR051	13-480	
A1F2M10	–READ BYTE BUFFER EMPTY	BS041AC2	BR061	15-040	
A1F2M11	P TEST POINT	BR051ED2	BR051	17-010	
A1F2M13	–CHANNEL BUFFER OUT 1	BR031GE6	BR031	17-010	
A1F2P02	–RESIDUAL GATE	BR051GD6	BR051	17-540	
A1F2P03	+SET WRITE DATA	BR041GM2	BR041	13-480	
			BR041	17-010	
			BR041	17-020	
			BR041	17-540	
A1F2P09	–WRT BUFFER EMPTY DOT	BR111DK4	BR061	13-480	
A1F2P10	–WRITE DATA READY	BS031FB6	BR061	13-480	
			BR061	17-010	
A1F2P11	+RD CHAN BFR	BR011CL2	BR011	17-010	
A1F2P13	–CHANNEL BUFFER OUT 0	BR031GD6	BR031	17-010	
A1F2S02	–TAPE OP A	BW231EK6	BR061	13-480	
A1F2S03	–25-75 CLOCK BUS A1 DELAYED	BS021FD1	BR071	13-480	
			BR061	15-040	
A1F2S04	–0-50 CLOCK BUS A1 DELAYED	BS021FG8	BR071	13-480	
			BR061	15-040	

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
A1F2S07	–BUS OUT BIT 4	FC081FH2	BR031	17-590	
A1F2U02	–CHANNEL BUFFER OUT P	BR031GC6	BR031	17-010	
A1F2U03	–CHANNEL BUFFER OUT 2	BR031GF6	BR031	17-010	
A1G2B03	–XOUTA BIT 3 ALU1 TO DF	AB141EC2	BW151	16-190	
			AB141	17-080	
			BW181	17-180	
A1G2B04	+FORMAT	BW151EA6	BW151	17-020	
A1G2B10	–CHB OR DC OUT 5	BR101BG4	BW121	17-020	
			BW121	17-700	
A1G2B11	–WRITE BUS BIT P	BW121GF2	BW121	17-010	
A1G2B13	+SET WRITE DATA A	BR101BK4	BW121	17-010	
			BW141	17-020	
			BW121	17-540	
A1G2D03	–WRITE AND TAPE OP	BW231GF6	BW141	13-480	
			BW141	17-180	
A1G2D07	–CHB OR DC OUT 4	BR101FF4	BW121	17-020	
			BW121	17-700	
A1G2D09	–WC 11	BW111GF6	BW111	17-020	
A1G2D10	+WRT TRG VRC ODD	BW061GK6	BW161	17-020	
			BW161	17-170	
A1G2D12	–CHB OR DC OUT 2	BR101BD4	BW121	17-020	
			BW121	17-700	
A1G2D13	–TAPE OP A	BW231EK6	BW161	13-480	
A1G2G02	–CHB OR DC OUT 3	BR101DE4	BW121	17-020	
			BW121	17-700	
A1G2G03	+WRITE TIME GATE	BW161GJ2	BW161	16-190	
			BW161	17-080	
A1G2G05	–STAT BIT 1 START WR RD	AA141GF6	BW151	13-480	
			BW151	17-050	
			BW151	17-180	
A1G2G07	–WRITE CONDITION	BW151GN6	BW151	13-480	
			BW151	16-170	
			BW151	17-010	
			BW151	17-020	
			BW151	17-160	
			BW151	17-170	
			BW151	17-310	
			BW151	17-540	
A1G2G08	–WRITE CNTR 4	BW091GL2	BW181	17-020	
A1G2G09	–WRITE CNTR 0	BW091GJ2	BW151	13-480	
			BW181	17-020	
A1G2G10	–XOUTA BIT 1 ALU1 TO DF	AB141GB2	BW151	13-480	
A1G2G11	+SET 2ND BUFFER	BW151EH2	BW151	13-480	
A1G2G13	–STOP STAT TO DF	FC111GF2	BW151	13-480	
A1G2J04	–RESIDUAL GATE	BR051GD6	BW121	17-010	
			BW121	17-020	
			BW121	17-540	
A1G2J06	–WRITE GROUP B BRANCH	BW151GH2	BW151	17-020	
			BW151	17-170	
A1G2J07	–ORC GATE	BR051GH6	BW121	17-010	
			BW121	17-020	
			BW121	17-170	
A1G2J09	–WR BUFFER OVERRUN	BW151FM6	BW151	17-010	
A1G2J10	–PARTIAL OR LAST FRAME	BR101FK4	BW151	13-480	
			BW151	17-020	
A1G2J11	+SET BYTE 4	BR041GN2	BW151	13-480	
A1G2M02	–CHANNEL BUFFER OUT P	BR031GC6	BW141	17-010	
A1G2M04	+PARITY EVEN	BN311DM2	BW141	17-010	
			BW141	17-020	
A1G2M05	–WC 0	BW101GA6	BW101	13-480	
			BW101	17-020	
A1G2M07	–6250 MODE	BW231GH6	BW141	13-480	
			BW141	13-480	
			BW141	16-190	
			BW141	17-020	

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3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
A1G2M10	–GATE WRITE	BW151DN6	BW151	16-170	
			BW151	17-180	
A1G2M11	–CHB OR DC OUT 7	BR101FJ4	BW121	17-020	
			BW121	17-700	
A1G2M12	+MARK 1	BW151FC6	BW151	17-020	
			BW151	17-170	
A1G2M13	USEC FREQ	BW221GK2	BW101	13-480	
A1G2P03	–CRC GATE	BR051GF6	BW121	17-010	
			BW121	17-020	
			BW121	17-540	
A1G2P04	–WC 9	BW111GD6	BW111	16-170	
A1G2P06	–NRZI MODE	BW231GK6	BW141	17-020	
A1G2P07	–STAT BIT 3 7 TRK	AA141EG6	BW141	17-020	
A1G2P10	–WR TRIGGER GATE	BW161GL6	BW161	16-170	
			BW161	16-190	
			BW161	17-080	
A1G2P13	–WRT TRG VRC ERROR	BW161GG6	BW161	17-020	
A1G2S04	–XOUT BIT 4 ALU1 TO DF	AB141CC2	BW151	17-020	
A1G2S05	–XOUTA BIT 0 ALU1 TO DF	AB141GA2	BW151	13-480	
			BW151	17-020	
A1G2S07	–XOUTA BIT 5 ALU1 TO DF	AB141CD2	BW151	17-020	
A1G2S10	–WRITE GROUP BUFFER EMPTY	BW151GG6	BW151	15-040	
A1G2S12	+INHIBIT WRITE	BW231DG6	BW151	16-190	
			BW231	17-080	
			BW151	17-180	
A1G2S13	–CHB OR DC OUT 1	BR101FC4	BW121	17-020	
			BW121	17-700	
A1G2U02	+END ONES LATCH	BW151BF2	BW151	17-020	
A1G2U03	–SET ANY BYTE	BW091GA2	BW181	17-010	
A1G2U06	–XOUT BIT 6 ALU1 TO DF	AB141AD6	BW151	17-020	
A1G2U07	–XOUTA BIT 7 ALU TO DF	AB141AE2	BW151	17-020	
A1G2U10	–CHB OR DC OUT 0	BR101DB4	BW121	17-020	
			BW121	17-700	
A1G2U11	–CHB OR DC OUT 6	BR101DH4	BW121	17-020	
			BW121	17-700	
A1G2U12	+MARK 2	BW151GC6	BW151	17-170	
A1H2B02	–WRITE CONDITION	BW151GN6	BW191	16-220	
			BW191	17-050	
			BW071	17-310	
A1H2B04	–WRITE BUS BIT 1	BW121BA7	BW001	17-020	
			BW001	17-700	
A1H2B07	–WRITE BUS BIT 4	BW121BG2	BW001	17-020	
			BW001	17-700	
A1H2B12	+WRITE TIME GATE	BW161GJ2	BW191	17-020	
A1H2B13	+A1	BW151GA6	BW191	17-020	
			BW011	17-170	
A1H2D02	+SET BYTE 4	BR041GN2	BW091	17-010	
			BW091	17-020	
			BR041	17-700	
A1H2D03	–GATE WRITE	BW151DN6	BW071	13-480	
			BW071	16-220	
			BW071	17-080	
			BW071	17-180	
A1H2D04	–WRITE BUS BIT 0	BW121BA2	BW001	17-020	
			BW001	17-700	
A1H2D05	+PE MODE	BW231GJ2	BW091	17-050	
A1H2D07	–WRITE BUS BIT 5	BW121BG7	BW001	17-020	
			BW001	17-700	
A1H2D09	–WRITE BUS BIT 6	BW121BK2	BW001	17-020	
			BW001	17-700	
A1H2D10	–STAT BIT 3 DIAGNOSTIC MODE	AB141EG6	BW091	17-020	
A1H2D13	+MARK 1	BW151FC6	BW191	16-220	
			BW191	17-020	
A1H2G02	–WR TRIGGER GATE	BW161GL6	BW071	17-020	
A1H2G03	+SET BYTE 3	BR041GK2	BW091	17-010	
			BW001	17-020	
			BW001	17-700	

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
A1H2G04	–XOUTA BIT 2 ALU1 TO DF	AB141EB6	BW071	16-220	
			BW071	17-180	
A1H2G05	+PE P BURST	BW221GK6	BW191	17-050	
A1H2G08	+SET BYTE 2	BR101DL4	BW091	17-010	
			BW001	17-020	
			BW001	17-700	
A1H2G10	+SET 2ND BUFFER	BW151EH2	BW191	17-020	
A1H2G11	–WRITE BUS BIT P	BW121GF2	BW091	17-020	
			BW091	17-700	
A1H2J03	+TUBO BIT 4	BW071GM6	BW071	16-220	
			BW071	17-020	
			BW071	17-310	
			BW071	17-700	
A1H2J04	–WRITE BUS BIT 3	BW121BD7	BW001	17-020	
			BW001	17-700	
A1H2J05	+0 PCT AMPL CTRL TRK 4	CB131CF2	BW071	16-210	
			BW071	16-220	
A1H2J06	–GATE WRITE NOT TM	BW151EN6	BW071	16-190	
			BW191	16-220	
			BW151	17-080	
			BW071	17-180	
A1H2J07	+TUBO BIT 5	BW081GD6	BW081	16-220	
			BW081	17-020	
			BW081	17-310	
			BW081	17-700	
A1H2J10	+0 PCT AMPL CTRL TRK 5	CB131DG2	BW081	16-220	
A1H2J11	+FORMAT	BW151EA6	BW191	16-220	
			BW021	17-020	
			BW151	17-170	
			BW021	17-190	
A1H2J13	+TUBO BIT 7	BW081GM6	BW081	16-220	
			BW081	17-020	
			BW081	17-310	
			BW081	17-700	
A1H2M04	+TUBO BIT 6	BW081GH6	BW081	16-220	
			BW081	17-020	
			BW081	17-310	
			BW081	17-700	
A1H2M07	+SET BYTE 1	BR041GJ2	BW091	17-010	
			BW091	17-020	
			BW001	17-700	
A1H2M09	+WRT TGR VRC ODD	BW061GK6	BW061	17-020	
			BW061	17-310	
A1H2M10	+TUBO BIT 0	BW061GH6	BW061	16-220	
			BW061	17-020	
			BW061	17-310	
			BW061	17-700	
A1H2M11	+0 PCT AMPL CTRL TRK 3	CB131FE6	BW071	16-160	
			BW071	16-220	
A1H2M13	–WRITE BUS BIT 2	BW121BD2	BW001	17-020	
			BW001	17-700	
A1H2P02	+0 PCT AMPL CTRL TRK 7	CB131DJ2	BW081	16-160	
			BW191	16-220	
A1H2P06	+0 PCT AMPL CNTRL TRK 6	CB131CH2	BW081	16-160	
			BW191	16-220	
A1H2P07	–WRITE BUS BIT 7	BW121BK7	BW001	17-020	
			BW001	17-700	
A1H2P09	+TUBO BIT 3	BW071GH6	BW071	16-220	
			BW071	17-020	
			BW071	17-310	
			BW071	17-700	
A1H2P11	+0 PCT AMPL CTRL TRK 0	CB131FA6	BW061	16-160	
			BW191	16-220	
A1H2S02	+A2	BW151FA6	BW191	17-020	
			BW011	17-020	
			BW011	17-170	

3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
A1H2S05	–WRITE CNTR 0	BW091GJ2	BW091	16-170	
			BW091	17-020	
A1H2S07	–WRITE CNTR 4	BW091GL2	BW091	13-470	
			BW091	17-020	
A1H2S09	+0 PCT AMPL CTRL TRK P	CB131CK2	BW061	16-220	
			BW061	17-050	
A1H2S10	+TUBO BIT 1	BW061GM6	BW061	16-220	
			BW061	17-020	
			BW061	17-050	
			BW061	17-310	
			BW061	17-700	
A1H2S12	–XOUTA BIT 4 ALU2 TO DF	AA141CC2	BW091	13-480	
			BW091	17-020	
A1H2S13	–ST BIT 2 WR P BURST	AA141EF6	BW061	17-050	
	UNUSED				
A1H2U03	+MARK2	BW151GC6	BW191	16-220	
			BW191	17-020	
A1H2U05	+TUBO BIT 2	BW071GD6	BW071	16-220	
			BW071	17-020	
			BW071	17-310	
			BW071	17-700	
A1H2U06	+0 PCT AMPL CTRL TRK 2	CB131FC6	BW071	16-210	
			BW191	16-220	
A1H2U07	–TUBO BIT P	BW061GD2	BW061	16-190	
			BW061	16-220	
			BW061	17-020	
			BW061	17-050	
			BW061	17-170	
			BW061	17-180	
			BW061	17-310	
			BW061	17-540	
			BW061	17-700	
A1H2U09	–WC 11	BW111GF6	BW091	13-480	
			BW091	17-020	
A1H2U10	–WC 9	BW111GD6	BW091	13-480	
			BW191	17-020	
A1H2U11	+0 PCT AMPL CTRL TRK 1	CB131FG6	BW061	16-220	
			BW061	17-050	
A1H2U12	–WRITE OSCILLATOR	BW221GK4	BW061	17-050	
A1K2B07	–XOUTA BIT 5 ALU2 TO DF	AA141CD2	BW241	17-050	
A1K2B09	–STAT BIT 1 START WR RD	AA141GF6	BW231	17-180	
A1K2B10	–TAPE OP A	BW231EK6	BW231	13-380	
			BW231	16-190	
			BW231	17-100	
			BW231	17-180	
			BW231	17-540	
A1K2B11	+INHIBIT WRITE	BW231DG6	BW231	16-170	
A1K2B13	–P OR C COMPARE	BW241FF6	BW241	15-040	
			BW241	17-010	
A1K2D04	10.85 MHZ	BW201FB2	BW201	13-450	
A1K2D09	–XOUTA BIT 4 ALU2 TO DF	AA141CC2	BW231	15-060	
			BW211	16-170	
			BW211	16-190	
			BW231	16-220	
			BW231	17-020	
			BW231	17-050	
			BW211	17-180	
			BW211	17-530	
A1K2D10	–NRZI MODE	BW231GK6	BW221	17-010	
			BW231	17-020	
			BW231	17-050	
			BW231	17-180	
A1K2D11	–XOUTA BIT 7 ALU2 TO DF	AA141AE6	BW241	17-050	
A1K2D12	+SENSE RST A	BW231FK6	BW231	17-010	
A1K2D13	–XOUTA BIT 2 ALU2 TO DF	AA141EB6	BW231	17-180	
A1K2G02	–5.12 MHZ	BS011EH2	BW221	17-050	
A1K2G08	–STAT BIT 3 DIAGNOSTIC MODE	AB141EG6	BW211	16-190	
			AB141	17-080	
A1K2G13	–PE MODE	BW231GJ6	BW231	17-050	
A1K2J04	–6.781 MHZ	BW201FF2	BW201	13-450	
A1K2J07	USEC FREQ	BW221GK2	BW221	16-170	
A1K2J10	+556 OR 200 BPI 7 TK	BN311EH6	BW221	17-050	
A1K2M02	4.069 MHZ	BW201FK2	BW201	13-450	
A1K2M07	+CONTROL	BW231GE2	BW231	17-540	
A1K2M10	–6250 MODE	BW231GH6	BW231	17-080	
A1K2M11	–END DATA CHECK	BW241FG6	BW241	15-100	
			BW241	17-540	
A1K2M12	–READ TIME	BW221GK6	BW221	13-450	
A1K2M13	+C COMPARE ERROR	BN231GD2	BW241	17-010	
A1K2P02	–R/W VRC ERROR	BW241BC6	BW241	17-410	
A1K2P03	+TAPE OP DELAYED	CB411BL2	BW241	16-220	
			BW241	17-370	
A1K2P06	–OVERRUN	BR021GG6	BW211	15-040	
A1K2P09	–WRT AND TAPE OP NOT CTRL	BW231GA6	BW231	13-380	
			BN321	17-010	
A1K2P10	–EOD OR CRC OK	BK041FL6	BW241	17-370	
			BW241	17-530	
			BW241	17-540	
A1K2P11	–SKEW ERROR	BW241FK6	BW241	17-160	
A1K2P12	1.92 MHZ	BW211FB2	BW211	13-450	
A1K2P13	+1 TRACK ENV BRANCH	BW231GC2	BW231	15-060	
			BW231	15-060	
			BW231	16-220	
			BW231	17-050	
A1K2S02	+MTE OR LRCR ERROR	CC300DD4	BW241	17-110	
A1K2S07	–DATA CHECK BRANCH	BW241FC2	BW241	17-370	
A1K2S11	–TIME SENSE P	CA100DC1	BW231	15-060	
A1K2S12	+SKEW CHK	CB431FC6	BW241	17-160	
			BW241	17-540	
A1K2S13	–XOUTA BIT 0 ALU2 TO DF	AA141GA2	BW231	13-480	
			BW231	16-190	
			BW231	17-050	
			AA141	17-080	
			BW231	17-180	
			BW231	17-220	
A1K2U02	+P TRACK ENV BRANCH	BW231GB2	BW231	15-060	
			BW231	16-220	
			BW231	17-050	
A1K2U04	3.2 MHZ	BW211FF2	BW211	13-450	
A1K2U05	–6250 BRANCH	BW231DK2	BW231	16-170	
A1K2U06	–STAT BIT 0 TAPE OP TO DF	AA141GE6	BW231	13-480	
			BW231	15-040	
			BW231	15-060	
			BW231	17-020	
			BW231	17-050	
			AA141	17-080	
			BW231	17-530	
A1K2U07	–XOUTA BIT 5 ALU1 TO DF	AB141CD2	BW231	13-480	
			BW231	16-190	
			AB141	17-080	
			BW231	17-180	
A1K2U09	–STAT BIT 2 SPARE TO DF	AB141EF6	BW231	13-480	
			BW231	15-040	
			BW231	16-190	
			BW231	17-080	
			BW231	17-170	
			BW231	17-180	
			BW231	17-540	
A1K2U10	+BLOCK OR ENV LOSS BRANCH	CC011GC6	BW231	15-060	
			BW231	17-050	
A1K2U11	+PE MODE	BW231GJ2	BW231	17-170	
A1K2U12	–READ AND TAPE OP	BW231GL6	BW211	16-200	
			BW211	17-010	
			BW23†	17-540	

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3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
A1K2U13	–TIME SENSE 1	CA300DE4	BW231	15-060	
			BW231	16-220	
A1L2B04	+SET WRITE DATA DELAYED	BN311GN6	BN311	17-540	
A1L2B12	–WR OR RD FORWARD	CH131BF6	BN311	15-070	
A1L2B13	–DATA CONVERTER ON	BN311DK6	BN311	15-070	
			BN311	17-310	
A1L2D09	–XLATE ON	BN311EL6	BN311	17-310	
A1L2D12	–STAT BIT 3 7-TRACK	AA141EG6	BN311	13-480	
A1L2D13	–PARITY EVEN	BN311DM6	BN311	17-310	
A1L2G04	+PARITY EVEN	BN311DM2	BN311	17-310	
A1L2G07	+CRC SHIFT	BR051FG2	BN311	17-540	
A1L2G12	+SET WR DATA FEEDBACK	BN311GM6	BN311	17-010	
			BN311	17-540	
A1L2M04	–CB WRITE PULSE	BR011GL6	BN321	17-010	
A1L2S02	–COMBINED ECC DATA P	CK001AA4	BN321	17-010	
A1L2S04	–READ AND TAPE OP	BW231GL6	BN321	17-010	
A1L2S05	–RD DATA TRK P	BR111BA4	BN321	17-010	
A1L2S07	+SET BYTE 2	BR101DL4	BN321	17-010	
A1L2S08	+SET BYTE 2	BR041GL4	BN321	17-010	
A1L2S13	+C COMPARE ERROR	BN321GD2	BN321	17-010	
A1L2U03	+FOURTH BYTE	BN011ED2	BN321	17-010	
A1L2U05	–WRITE BUS BIT P	BW121GF2	BN321	17-010	
A1L2U06	–CHANNEL BUFFER OUT P	BR031GC6	BN321	17-010	
A1L2U07	–REQ CB WR CYCLE	CH021GE2	BN321	17-010	
A1R2B13	+CBI BITS 3-6 ORED	PK021GN6	PK101	13-480	
A1R2D04	–ANY COMMAND TEST BRK	PK101EG6	PK091	12-020	
A1R2D05	–ANY COMMAND TEST BRK	PK101EG6	PK101	13-050	
			PK101	13-300	
A1R2D06	+CE STROBE TEST BRK	PK101DA2	PK101	12-020	
			PK101	13-050	
A1R2D12	–CE OP IN	PR181EC6	PK091	12-020	
			PK081	13-050	
A1R2D13	–CE STATUS IN	PR181EF6	PK081	13-170	
			PR181	13-050	
A1R2G12	–CNTR COMPARE EQ TEST BRK	PK091GG6	PK101	13-110	
			PK081	13-480	
A1R2G13	+CE COMMAND OUT	PK081CJ2	PK091	12-020	
			PK091	13-050	
A1R2J03	–OPERATIONAL IN	FC141GK6	PK081	13-050	
A1R2J04	+CE MASTER RESET	PR181DG2	PK081	13-140	
A1R2J06	+START OR STATUS IN	PK101FE2	PK081	13-330	
A1R2J11	+CE STROBE TEST BRK	PK101DA2	PR181	13-050	
A1R2J12	–COMPARE EQUAL SERV	BB001GG4	PK081	13-050	
			PK101	13-050	
A1R2J13	–CE SERVICE IN	PR181FD6	PK091	12-020	
			PK091	12-020	
A1R2M02	+CTI BIT 6 TO CE	FC161GL2	PK091	13-480	
A1R2M03	+ANY CE OUT TAG	PK081FE6	PK091	12-020	
A1R2M09	–4 BIT BUS 0,4,OR 8	PK035GB2	PR181	13-170	
A1R2M11	–4 BIT BUS 1,5,OR 9	PK035GD2	PR181	13-050	
A1R2M12	+CE MODE	PK011FH2	PR151	13-050	
A1R2M13	+CTI BIT 5 TO CE	FC161GJ2	PK091	12-020	
			PK091	12-020	
A1R2P02	+CE ADDRESS OUT	PK081CG2	PR181	13-050	
A1R2P11	–4 BIT BUS 2,6,OR 10	PK035GF2	PR181	13-050	
A1R2P12	–4 BIT BUS 3,7,OR 11	PK035GH2	PR181	13-110	
A1R2P13	–WR RIPPLE DATA SW NO	PS041AL4	PK081	13-050	
A1R2S04	+ROS CYCLE MODE	PR181AM2	PK091	12-020	
A1R2S05	+CE COMMAND OUT TAG	PK081FJ6	PK091	12-020	
			PR181	12-020	
A1R2S07	–GATE CBI TO CE ENTRY	PR181EK6	PR181	12-020	
			PK081	13-100	
			PK081	13-290	
			PK081	13-330	
			PR181	12-020	
			PR181	13-380	

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
A1R2S09	–REGISTER TEST	FC161GN4	PR181	12-020	
A1R2S11	+CE SERVICE OUT TAG	PK081FL6	PK081	13-100	
			PK081	13-280	
			PK081	13-350	
A1R2S12	–STOP ON CTRL ERROR SW NO	PS041AC4	PR181	12-020	
A1R2S13	–ROS CYCLE MODE	PK011EN9	PR181	12-020	
A1R2U04	+CE INITIAL SEL TAG	PK081GB6	PK081	13-320	
A1R2U05	+CE ADDR OUT TAG	PK081FG6	PK081	13-300	
			PK081	13-360	
A1R2U07	–GATE CE REGS TO CE ENTRY	PR181DJ6	PR181	12-020	
A1R2U09	–STOP ON HDW ERROR	PR181EN6	PR181	12-020	
A1R2U11	+REGISTER TEST	PK081BN2	PK081	13-280	
			PK081	13-310	
			PK081	13-340	
A1R2U12	+STOP ON HDW ERROR	PR181CN2	PR181	12-020	
A1R2U13	–PANEL ENABLE	PK011EK6	PR181	12-020	
A1S2B02	–DATA ENTRY BIT 0	PS021AM4	PP051	12-020	
A1S2B03	–DATA ENTRY BIT 2	PS021AK4	PP051	12-020	
A1S2B04	–DATA ENTRY BIT 4	PS021AG4	PP051	12-020	
A1S2B05	–DATA ENTRY BIT 6	PS021AF4	PP051	12-020	
A1S2B07	–DATA ENTRY BIT 9	PS021AC4	PP051	12-020	
A1S2B09	–DATA ENTRY BIT 11	PS021AA4	PP051	12-020	
A1S2B10	–DATA ENTRY SELECT BIT 2	PS021AP4	PP051	12-020	
A1S2D02	–DATA ENTRY BIT 1	PS021AL4	PP051	12-020	
A1S2D03	–DATA ENTRY BIT 3	PS021AJ4	PP051	12-020	
A1S2D04	–DATA ENTRY BIT 5	PS021AH4	PP051	12-020	
A1S2D05	–DATA ENTRY BIT 7	PS021AE4	PP051	12-020	
A1S2D06	–DATA ENTRY BIT 8	PS021AD4	PP051	12-020	
A1S2D07	–DATA ENTRY BIT 10	PS021AB4	PP051	12-020	
A1S2D09	–DATA ENTRY SELECT BIT 1	PS021AN4	PP051	12-020	
A1S2D10	–DATA ENTRY SELECT BIT 4	PS021AQ4	PP051	12-020	
A1S2G08	+WRITE CMND	PP041GK6	PK041	12-000	
			PP041	13-050	
			PP041	13-480	
			PP041	15-100	
			PP041	16-170	
			PP041	17-020	
			PP041	17-170	
			PP041	17-220	
A1S2J02	+CE MASTER RESET	PR181DG2	PP051	12-020	
A1S2J06	–GATE TAGS	PP041GH6	PP041	13-050	
			PP041	13-330	
A1S2J13	–NOT RUN CLOCK	PP041AD6	PP041	13-050	
A1S2M03	+ANY CE OUT TAG	PK081FE6	PR151	13-050	
A1S2M09	–C3 AND STEP3	PR151CM6	PR151	13-240	
A1S2M13	–P OR C COMP	BW241FF6	PR161	15-140	
A1S2S02	+6250 1 OR 2 TRK CORR	BK001BF2	PR161	13-480	
			PR161	15-140	
A1S2S03	+CRC A NOT EQUAL B	BK001BH2	PR161	13-480	
A1S2S09	–SKEW ERROR	BW241FK6	PR161	15-140	
A1S2U03	+NEW CRC ERR	BK001BK2	PR161	13-480	
A1S2U05	–R/W VRC ERROR	BW241BC6	PR161	15-140	
A1S2U06	–MTE	BW241BE6	PR161	15-140	
A1S2U07	–END DATA CHECK	BW241FG6	PR161	15-100	
			PR161	15-140	
A1S2U09	–STAT BIT 1 SENSE	AB141GF6	PR161	13-480	
			PR161	17-050	
A1T2B02	–DISPLAY SELECT BIT 1	PS031AD4	PK011	12-020	
A1T2B03	–DISPLAY SELECT BIT 2	PS031AE4	PK011	12-020	
A1T2B04	–DISPLAY SELECT BIT 4	PS031AF4	PK011	12-020	
A1T2B05	–ROS MODE SELECT BIT 1	PS041AD4	PK011	12-020	
A1T2B07	–ROS MODE SELECT BIT 2	PS041AE4	PK011	12-020	
A1T2B09	–ROS MODE SELECT BIT 4	PS041AF4	PK011	12-020	
A1T2B10	+SELECT WRITE OR OUT BUS	PK011ED2	PK011	12-020	
A1T2B11	+SELECT ROS DATA LOW	PK011EF2	PK011	12-020	

3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
A1T2B12	+CE MODE	PK011FH2	PK011	12-020	
A1T2D03	–PANEL ENABLE SW NO	PS041AA4	PK011	12-020	
			PK011	13-050	
A1T2D06	–DISPLAY CE REG	PK011AC3	PK011	12-020	
A1T2D07	+DISPLAY COMPARE REG	PK011GD2	PK011	12-020	
A1T2D09	+SELECT ROS ADR	PK011CB2	PK011	12-020	
A1T2D11	+SELECT READ OR IN BUS	PK011CD2	PK011	12-020	
A1T2D13	+SELECT ROS DATA HIGH	PK011CF2	PK011	12-020	
A1T2G03	–PANEL ENABLE	PK011EK6	PK011	12-020	
A1T2G04	–CMPR EQUAL IND	PS011EC6	PS011	12-020	
A1T2G05	+START NB LTH	PK035DN2	PK035	13-050	
			PK035	16-000	
A1T2G07	+RESET OR START/STEP SW NC	PS031AC4	PS011	12-020	
A1T2G08	–SELECTED ALU STEP PULSE	PP021FL6	PS011	12-020	
A1T2G11	–CE SELECT REG PULSE	PP021FG6	PS011	12-020	
A1T2J02	–ROS CYCLE MODE	PK011EN9	PK011	12-020	
A1T2J04	+ROS STOP MODE	PK011CK2	PK011	12-020	
A1T2J05	+ROS STEP MODE	PK011FK2	PK011	12-020	
A1T2J06	+STOP CONDITIONS	PK035GK6	PK035	13-240	
A1T2J10	+ANY ALU HDW ERROR	PP031GM6	PS011	12-020	
A1T2J11	–START/STEP SW NO	PS031AB4	PS011	12-020	
A1T2M02	–LS OR DE 0 OR 2	PP051BB2	PK031	12-020	
A1T2M03	–LS OR DE 4 OR 8	PP051DB2	PK031	12-020	
A1T2M04	–LS OR DE 6 OR 10	PP051FB2	PK031	12-020	
A1T2M05	–GATE CBI TO CE ENTRY	PR181EK6	PK031	12-020	
A1T2M07	+REGISTER TEST	PK081BN2	PK031	12-020	
A1T2M08	+CE RESET SWITCH	PS011DM6	PS011	12-020	
			PS011	13-010	
A1T2M11	+SINGLE STEP OR START ALU	PS011EA2	PS011	12-020	
A1T2P03	–LS OR DE 5 OR 9	PP051DD2	PK031	12-020	
A1T2P04	–LS OR DE 7 OR 11	PP051FD2	PK031	12-020	
A1T2P05	–GATE CE REGS TO CE ENTRY	PR181DJ6	PK031	12-020	
A1T2P11	+SET IC	PS011GM2	PS011	12-020	
A1T2S07	–COMPARE EQUAL	PK021GG6	PK021	12-020	
A1T2S09	–CE STATUS ADVANCE CMND	PK021GL6	PK021	12-020	
			PK021	13-050	
A1T2S10	–4 BIT BUS 0,4,OR 8	PK035GB2	PK021	12-020	
A1T2S11	–4 BIT BUS 2,6,OR 10	PK035GF2	PK021	12-020	
A1T2S13	+CE BUS OUT PARITY GOOD	PK031AK6	PK031	12-020	
A1T2U06	+CE ENTRY BIT P	PK031GK2	PK031	12-020	
A1T2U10	–4 BIT BUS 1,5,OR 9	PK035GD2	PK021	12-020	
A1T2U11	–4 BIT BUS 3,7,OR 11	PK035GH2	PK021	12-020	
A1T2U13	–CE STATUS IN	PR181EF6	PK021	12-020	
A1U2G10	–50 NS TAP POWERED ALU1	AB041CD6	PP021	12-020	
A1U2G11	–50 NS TAP POWERED	AA041CD6	PP021	12-020	
A1U2G13	–4 BIT BUS 3,7,OR 11	PK035GH2	PR141	12-020	
A1U2M02	–4 BIT BUS 1,5,OR 9	PK035GD2	PR141	12-020	
A1U2M10	+ROS STEP MODE	PK011PK2	PP021	12-020	
A1U2P02	–4 BIT BUS 0,4,OR 8	PK035GB2	PR141	12-020	
A1U2P03	–4 BIT BUS 2,6,OR 10	PK035GF2	PR141	12-020	
A1U2P10	+ROS STOP MODE	PK011CK2	PR141	12-020	
A1U2S02	–SELECT ROS ADR	PK011CB6	PP021	12-020	
A1U2S09	+SET IC	PS011GM2	PR141	12-020	
A1U2S10	–CE COMPARE SAMPLE ALU2	A021FH2	PP021	12-020	
A1U2S12	–PANEL ENABLE	PK011EK6	PP021	12-020	
A1U2S13	–CE COMPARE SAMPLE ALU1	AB021FH2	PP021	12-020	
A1U2U05	–STOP ON HDW ERROR	PR181EN6	PP021	12-020	
A1U2U07	–CE SELECT REG PULSE	PP021FG6	PP021	12-020	
			PP021	16-000	
			PP021	16-220	
			PP021	17-370	
A1U2U10	–COMPARE STOP OR STEP ALU1	PP021EG6	PP021	12-020	
			PP021	13-090	
A1U2U12	–SELECTED ALU STEP PULSE	PP021FL6	PP021	12-020	
A1U2U13	+ANY ALU HDW ERROR	PP031GM6	PP031	12-020	

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
A2D2B02	–TACH VELOCITY	XC031EC6	XC031	13-460	
			XC031	13-510	
			XC031	16-170	
A2D2B03	+TRAP ALU2 LATCH 2	XC032CH4	XC061	13-420	
A2D2B04	–DEVICE BUS IN 7 SECONDARY	XC081DD8	XC021	17-160	
			XC081	17-310	
			XC021	17-700	
A2D2B07	–DEVICE BUS IN 6 TO DF	XC031BL2	XC031	16-220	
A2D2B09	–DEVICE BUS IN 7 TO DF	XC031CM2	XC031	16-220	
A2D2B10	–DEVICE BUS IN 4 TO DF	XC031CJ2	XC031	16-220	
A2D2D03	–GATE TRAP PULSE	AA031GA6	XC061	13-190	
A2D2D04	–DEVICE BUS IN 4 SECONDARY	XC081DD5	XC021	15-060	
			XC021	17-160	
			XC081	17-310	
			XC081	17-700	
A2D2D05	–25 NS TAP	AA021CA4	XC061	13-190	
			XC061	13-260	
A2D2D06	–DEVICE BUS IN 7 PRIMARY	XC081DA8	XC011	17-160	
			XC081	17-310	
			XC011	17-700	
A2D2D07	–DEVICE BUS IN 5 TO DF	XC031BK2	XC031	16-220	
A2D2D10	–DEVICE BUS IN 1 SECONDARY	XC081DD2	XC021	15-060	
			XC081	17-050	
			XC021	17-160	
			XC081	17-310	
			XC081	17-700	
A2D2D11	–GATE PRIMARY RECEIVERS	XC131GE6	XC011	16-200	
			XC011	17-310	
A2D2D13	–GATE SECONDARY RECEIVERS	XC131GA6	XC021	16-200	
			XC021	17-310	
A2D2G04	+RESET ALU2 IC	XC032CG4	XC061	13-190	
			XC061	13-420	
A2D2G08	–DEVICE BUS IN 4 PRIMARY	XC081DA5	XC011	15-060	
			XC011	17-160	
			XC081	17-310	
			XC001	17-700	
A2D2G10	–DEVICE BUS IN 5 PRIMARY	XC081DA6	XC011	17-160	
			XC081	17-310	
			XC011	17-700	
A2D2G12	–INTERRUPT	XC031BB2	XC031	13-050	
			XC031	16-200	
			XC031	16-220	
A2D2G13	–DEVICE BUS IN 3 PRIMARY	XC081DA4	XC011	15-060	
			XC011	17-160	
			XC081	17-310	
			XC011	17-700	
A2D2J02	–DEVICE BUS IN 1 TO DF	XC031CF2	XC031	15-020	
			XC031	16-220	
A2D2J03	–DEVICE BUS IN 2 TO DF	XC031BG2	XC031	16-220	
A2D2J04	–DEVICE BUS IN 3 TO DF	XC031BH2	XC031	16-220	
A2D2J05	–DEVICE BUS IN 0 TO DF	XC031BE2	XC031	16-220	
A2D2J06	–DEVICE BUS IN 2 PRIMARY	XC081DA3	XC011	15-060	
			XC011	17-160	
			XC081	17-310	
			XC011	17-700	
A2D2J07	+METER FREE RUN CHAN B	XC031BC6	XC031	17-160	
A2D2J09	–DEVICE BUS IN 1 PRIMARY	XC081DA2	XC011	15-060	
			XC011	17-050	
			XC081	17-310	
			XC011	17-700	
A2D2J12	–DEVICE BUS IN 6 SECONDARY	XC081DD7	XC021	17-160	
			XC081	17-310	
			XC021	17-700	

3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
A2D2M03	–DEVICE BUS IN P SECONDARY	XC081DD9	XC021	15-060	
			XC021	17-050	
			XC021	17-160	
			XC081	17-310	
			XC081	17-700	
A2D2M05	–DEVICE BUS IN 0 PRIMARY	XC081DA1	XC011	15-060	
			XC011	17-160	
			XC081	17-310	
			XC011	17-700	
A2D2M08	+BLOCK OR ENV LOSS BRANCH	CC011GC6	CC051	17-100	
A2D2M09	+DCC ERROR OR SAGC BRANCH	BN321GK4	XC041	16-220	
			BN321	17-080	
A2D2M10	–DEVICE BUS IN 6 PRIMARY	XC081DA7	XC011	17-160	
			XC081	17-310	
			XC011	17-700	
A2D2M12	–DEVICE BUS IN 3 SECONDARY	XC081DD4	XC021	15-060	
			XC021	17-160	
			XC081	17-310	
			XC081	17-700	
A2D2P02	–CLK 17	AA041EB6	XC041	16-120	
A2D2P03	–DEVICE END IRPT PRIMARY	XC081DG3	XC011	16-200	
			XC011	16-220	
A2D2P04	–DEVICE BUS IN 5 SECONDARY	XC081DD6	XC021	17-160	
			XC081	17-310	
			XC021	17-700	
A2D2P05	–DEVICE BUS IN 0 SECONDARY	XC081DD1	XC021	15-060	
			XC021	17-160	
			XC081	17-310	
			XC081	17-700	
A2D2P06	–DEVICE BUS IN P TO DF	XC031BN2	XC031	16-220	
A2D2P07	–ROS REG 5 ALU2	AA071CJ6	XC051	16-120	
A2D2P10	–DEVICE BUS IN 2 SECONDARY	XC081DD3	XC021	15-060	
			XC021	17-160	
			XC081	17-310	
			XC081	17-700	
A2D2P11	+ROS REG 5 ALU2	AA071CJ2	XC041	16-120	
A2D2S07	–DEVICE BUS IN P PRIMARY	XC081DA9	XC011	15-060	
			XC011	17-050	
			XC011	17-160	
			XC081	17-310	
			XC011	17-700	
A2D2S10	+TM CONFIGURATION	CC001GE4	XC051	17-180	
A2D2S11	–DEVICE OPERATING SECONDARY B	XC081BH2	XC021	16-200	
			XC551	16-220	
A2D2S12	–EOD OR CRC OK DOT	BK041FL6	XC041	17-150	
A2D2U04	–FB DATA OR ALL ONES	CB121FK4	XC051	17-100	
A2D2U06	–ROS REG 6 ALU2	AA071CL6	XC041	16-120	
A2D2U07	–DEVICE END IRPT SECONDARY	XC081DG6	XC021	16-200	
			XC021	16-220	
A2D2U11	+ROS REG 6 ALU2	AA071CL2	XC051	16-120	
A2D2U13	–IBG BRANCH	CC001FC2	XC051	16-190	
			CC001	17-150	
A2E2B03	–BUS OUT 1 SECONDARY	XC151FC6	XC151	16-190	
			XC151	17-050	
			XC141	17-080	
			XC151	17-180	
A2E2B04	–BUS OUT 2 SECONDARY	XC151FD6	XC151	16-190	
			XC141	17-080	
			XC151	17-180	
A2E2B09	–BUS OUT 3 PRIMARY	XC141CF6	XC141	15-090	
			XC141	16-190	
			XC141	17-180	
A2E2B12	–BUS OUT 3 SECONDARY	XC151CF6	XC151	15-090	
			XC151	16-190	
			XC141	17-080	
			XC151	17-180	

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
A2E2B12	–BUS OUT 3	XC601DG6	XC601	15-090	
A2E2D02	–TUBO BIT 1	FD021GB2	XC091	16-220	
A2E2D03	–BUS OUT 1 PRIMARY	XC141FC6	XC141	16-190	
			XC141	17-050	
			XC141	17-180	
A2E2D04	–BUS OUT 2 PRIMARY	XC141FD6	XC141	16-190	
			XC141	17-180	
A2E2D05	–TUBO BIT 2	FD021GD2	XC091	16-220	
A2E2D07	–TUBO BIT 3	FD021GE2	XC091	16-220	
A2E2D09	–BUS OUT 4 PRIMARY	XC141CG6	XC141	15-090	
			XC141	16-190	
			XC141	17-180	
A2E2D10	–TUBO BIT 4	FD021GG2	XC091	16-220	
A2E2D13	–BUS OUT 4 SECONDARY	XC151CG6	XC151	15-090	
			XC151	16-190	
			XC141	17-080	
			XC151	17-180	
A2E2D13	–BUS OUT 4	XC601DJ6	XC601	15-090	
A2E2G04	–DE INTERRUPT 7 (OR F)	XC581DE8	XC621	16-200	
			XC621	16-220	
A2E2G07	–BUS OUT P SECONDARY	XC151CA6	XC151	16-190	
			XC151	17-050	
			XC141	17-080	
			XC151	17-180	
A2E2G08	–BUS OUT 0 SECONDARY	XC151CB6	XC151	15-090	
			XC151	16-190	
			XC141	17-080	
			XC151	17-180	
A2E2G08	–BUS OUT 0	XC601DC6	XC601	15-090	
A2E2G09	–BUS OUT 0 PRIMARY	XC141CB6	XC141	15-090	
			XC141	16-190	
			XC141	17-180	
A2E2J06	–TUBO BIT P	BW061GD2	XC091	16-220	
A2E2J07	–BUS OUT P PRIMARY	XC141CA6	XC141	16-190	
			XC141	17-050	
			XC141	17-180	
A2E2J09	–TUBO BIT 0	FD021GA2	XC091	16-220	
A2E2J13	–DE INTERRUPT 3 (OR B)	XC581DE4	XC621	16-200	
			XC621	16-220	
A2E2M03	–DE INTERRUPT 1 (OR 9)	XC581DE2	XC621	16-200	
			XC621	16-220	
A2E2M07	–BUS OUT 5 SECONDARY	XC151FH6	XC151	16-190	
			XC141	17-080	
			XC151	17-180	
A2E2M08	–BUS OUT 6 SECONDARY	XC151FJ6	XC141	15-090	
			XC151	16-190	
			XC141	17-080	
			XC151	17-180	
A2E2M08	–BUS OUT 6	XC601DM6	XC601	15-090	
A2E2M09	–BUS OUT 6 PRIMARY	XC141FJ6	XC141	15-090	
			XC141	16-190	
			XC141	17-180	
A2E2P02	–BUS OUT 7 PRIMARY	XC141CK6	XC141	15-090	
			XC141	16-190	
			XC141	17-180	
A2E2P03	–DE INTERRUPT 5 (OR D)	XC581DE6	XC621	16-200	
			XC621	16-220	
A2E2P06	–TUBO BIT 5	D021GH2	XC091	16-220	
A2E2P07	–BUS OUT 5 PRIMARY	XC141FH6	XC141	16-190	
			XC141	17-180	
A2E2P09	–TUBO BIT 6	FD021GK2	XC091	16-220	
A2E2P13	–TUTAG BIT 7 MOVE	FD041GG6	XC121	16-170	
A2E2S02	–DE INTERRUPT 4 (OR C)	XC581DE5	XC621	16-200	
			XC621	16-220	
A2E2S05	–DE INTERRUPT 2 (OR A)	XC581DE3	XC621	16-200	
			XC621	16-220	

3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
A2E2S10	–TUBO BIT 7	FD021GL2	XC091	16-220	
A2E2S12	–DE INTERRUPT O (OR 8)	XC581DE1	XC621	16-200	
			XC621	16-220	
A2E2U06	–DE INTERRUPT 6 (OR E)	XC581DE7	XC621	16-200	
			XC621	16-220	
A2E2U11	–BUS OUT 7 SECONDARY	XC151CK6	XC151	15-090	
			XC151	16-190	
			XC141	17-080	
			XC151	17-180	
A2E2U11	–BUS OUT 7	XC601DN6	XC601	15-090	
A2H2M02	+ROS BIT P1 ROS X	QA091AA6	QA091	13-190	
A2H2M03	+ROS BIT 15 ROS X	QA091EJ6	QA091	13-190	
A2H2P02	+ROS BIT P2 ROS X	QA091EL6	QA091	13-190	
A2H2P04	+ROS BIT 14 ROS X	QA091EG6	QA091	13-190	
A2H2P05	+ROS BIT 13 ROS X	QA091EE6	QA091	13-190	
A2H2P06	+ROS BIT 12 ROS X	QA091EC6	QA091	13-190	
A2H2P07	+ROS BIT 11 ROS X	QA091EA6	QA091	13-190	
A2H2P09	+ROS BIT 10 ROS X	QA091CL6	QA091	13-190	
A2H2P10	+ROS BIT 9 ROS X	QA091CJ6	QA091	13-190	
A2H2P11	+ROS BIT 8 ROS X	QA091CG6	QA091	13-190	
A2H2U02	+ROS BIT 7 ROS X	QA091CE6	QA091	13-190	
A2H2U03	+ROS BIT 6 ROS X	QA091CC6	QA091	13-190	
A2H2U04	+ROS BIT 5 ROS X	QA091CA6	QA091	13-190	
A2H2U05	+ROS BIT 4 ROS X	QA091AL6	QA091	13-190	
A2H2U10	+ROS BIT 3 ROS X	QA091AJ6	QA091	13-190	
A2H2U11	+ROS BIT 2 ROS X	QA091AG6	QA091	13-190	
A2H2U12	+ROS BIT 1 ROS X	QA091AE6	QA091	13-190	
A2H2U13	+ROS BIT 0 ROS X	QA091AC6	QA091	13-190	
A2K2B09	+20.48 MHZ	BS011GJ2	AA011	13-190	
A2K2D10	–RESET OR TRAP ALU2	AA011BL2	AA031	13-190	
			AA011	16-000	
A2K2D12	+SYSTEM RESET	AA011BL6	AA021	13-190	
A2K2G03	+CLK 1 NOT CE CYC L2 ALU2	AA041BJ2	AA041	13-190	
A2K2G09	+CLK 4 ALU2 L1	AA041GF2	AA041	13-420	
A2K2G12	–0 NS TAP	AA021AC6	AA021	13-000	
			AA021	13-190	
			AA021	16-000	
A2K2J02	–CE COMPARE SAMPLE ALU2	AA021FH2	AA021	12-020	
A2K2J05	+CLK 1 NOT CE CYC L1 ALU2	AA041BG2	AA041	13-190	
A2K2J10	+5.12 MHZ	BS011EH6	AA031	13-190	
A2K2M08	+CLK 6 ALU2	AA041GD6	AA041	13-190	
			AA041	13-420	
			AA011	13-190	
			AA011	13-420	
A2K2P04	–150 NS TAP	AA021AJ6	AA021	12-020	
			AA041	13-190	
A2K2P12	–100 NS TAP	AA021AG6	AA021	12-020	
A2K2U07	–75 NS TAP	AA021AF6	AA041	13-190	
A2K2U11	+RESET HI ORDER ROS L2	AA021EM6	AA021	13-190	
A2L2B02	+ROS REG 14 MASK ALU2	AA051FL6	AA181	13-190	
A2L2B03	+ROS REG 15 MASK ALU2	AA051FN6	AA181	13-190	
A2L2B04	+ROS BIT 14	QA011FF4	AA051	16-080	
A2L2B05	+ROS BIT 12	QA011FB4	AA051	16-080	
A2L2B07	+ROS REG 12 MASK ALU2	AA051FG6	AA181	13-190	
A2L2B09	–150 NS TAP	AA021AJ6	AA101	16-080	
A2L2B10	+ROS REG 13 MASK ALU2	AA051FJ6	AA181	13-190	
A2L2B12	+XFR LSR2 TO XOUTA	AA171GC2	AA171	13-430	
A2L2B13	+XFR LSR2 TO STAT	AA171EJ2	AA171	13-190	
			AA171	13-420	
A2L2D02	+ROS BIT 15	QA011FH4	AA051	16-080	
A2L2D05	+ROS BIT P2	QA011FM4	AA101	16-080	
A2L2D11	+XFR LSR2 TO XOUTB	AA171GF2	AA171	13-430	

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
A2L2G02	+XFR LSR2 TO TU TAGS	AA171EM2	AA171	13-240	
A2L2G03	+ROS REG 10 MASK ALU2	AA051CE6	AA181	13-190	
A2L2G04	+ROS REG 9 MASK ALU2	AA051CC6	AA181	13-190	
A2L2G05	+ROS BIT 10	QA011DK4	AA051	16-080	
A2L2G11	–SPARE XFR 18	AA171EK6	AA171	17-010	
A2L2G12	+INST COUNT 10 ALU2	AA185CH4	AA185	13-190	
A2L2G13	+INST COUNT 9 ALU2	AA185CE4	AA185	13-190	
A2L2J03	+ROS BIT 11	QA011DM4	AA051	16-080	
A2L2J04	+ROS REG 11 MASK ALU2	AA051CG6	AA181	13-190	
A2L2J05	+ROS BIT 9	QA011DH4	AA051	16-080	
A2L2J06	+ROS BIT 8	QA011DF4	AA051	16-080	
A2L2J13	+INST COUNT 11 ALU2	AA185CL4	AA185	13-190	
A2L2M02	+INST COUNT 12 ALU2	AA185FB4	AA185	13-190	
A2L2M03	+INST COUNT 13 ALU2	AA185FE4	AA185	13-190	
A2L2M04	+XFR OPER	AA101AM4	AA171	13-190	
A2L2M05	+ROS REG 8 MASK ALU2	AA051CA6	AA181	13-190	
A2L2M12	+CLK NOT CE CYCLE L2 ALU2	AA041BJ2	AA051	16-080	
A2L2P02	+INST COUNT 15 ALU2	AA185FL4	AA185	13-190	
A2L2P03	+INST COUNT 14 ALU2	AA185FH4	AA185	13-190	
A2L2P11	+INST COUNT 8 ALU2	AA185CB4	AA185	13-190	
A2L2S04	–ROS REG 8 ALU2	AA051CA2	AA185	16-100	
			AA185	16-110	
A2L2U04	–BOC MET ALU2	AA271CM2	AA101	16-080	
A2M2B02	–PAGE BIT 6 ALU2	AA111EC6	AA111	13-190	
A2M2B04	–PAGE BIT 4 ALU2	AA111EA6	AA111	13-190	
A2M2B05	–PAGE BIT 5 ALU2	AA111EB2	AA111	13-190	
A2M2B10	+ROS REG 0 ALU2	AA071CA2	AA071	13-190	
A2M2B11	–LSR DECODE 5 ALU2	AA071CL6	AA071	13-190	w/o EC733838
A2M2B12	–LSR DECODE 6 ALU2	AA071EL6	AA071	13-190	w/o EC733838
A2M2B13	–ROS REG 4 ALU2	AA071CH6	AA071	13-190	
			AA071	16-090	
			AA071	16-120	
A2M2D05	–ROS REG 5 ALU2	AA071CJ6	AA071	13-190	
			AA071	16-120	
A2M2D07	–ROS REG 7 ALU2	AA071CN6	AA071	13-190	
			AA071	16-120	
A2M2D09	–ROS REG 6 ALU2	AA071CL6	AA071	13-190	
			AA071	16-120	
A2M2D10	–ROS REG 3 ALU2	AA071DD2	AA071	13-190	
			AA071	16-120	
A2M2D11	+BRANCH MET ALU2	XC032CD4	AA271	16-090	
A2M2D13	–LSR DECODE 4 ALU2	AA071AL6	AA071	13-190	w/o EC733838
A2M2G02	–LSR DECODE 7 ALU2	AA071GL6	AA071	13-191	w/o EC733838
A2M2G04	–BU OPERATION ALU2	AA111BF6	AA111	13-190	
A2M2G05	+ROS BIT 1	QA011BD4	AA061	16-090	
A2M2G07	+ROS BIT 0	QA011BB4	AA061	16-090	
A2M2G10	+ROS BIT P1	QA011FK4	AA071	16-090	
A2M2G12	–XFR OPERATION ALU2	AA111BM6	AA111	13-190	
A2M2J02	+ROS BIT 3	QA011BH4	AA061	16-090	
A2M2J04	–BU OR BOC ALU2	AA111CG2	AA111	13-190	
A2M2J06	+ROS BIT 2	QA011BF4	AA061	16-090	
A2M2J11	+CLK 1 NOT CE CYC L1 ALU2	AA041BG2	AA071	16-090	
A2M2J12	–ADD OPERATION ALU2	AA111EL6	AA111	13-190	
A2M2J13	–STORE OPERATION ALU2	AA111BK6	AA111	13-190	
A2M2M09	–BOC OPERATION ALU2	AA111BH6	AA111	13-190	
A2M2M13	+LSR ADDRESS BIT 2 ALU2	AA071CM2	AA071	13-190	with EC733838
A2M2M13	–LSR DECODE 2 ALU2	AA071EJ6	AA071	13-190	w/o EC733838
A2M2P02	–LOGIC OPERATION ALU2	AA111FN6	AA111	13-190	
A2M2P03	+7 TRK JMPR - SEE REF PAGE	AA005001	AA131	15-060	
A2M2P04	+ROS REG 5 ALU2	AA071CJ2	AA071	13-420	
A2M2P06	–PAGE BIT 7 ALU2	AA111ED6	AA111	13-190	
A2M2P09	–ROS REG 0 AND 1 ALU2	AA111EJ6	AA111	13-190	
A2M2P12	–ROS REG 0 AND 2 ALU2	AA111EG6	AA111	13-190	
A2M2P13	–LSR DECODE 1 ALU2	AA071CJ6	AA071	13-190	w/o EC733838
A2M2P13	+LSR ADDRESS BIT 4 ALU2	AA071CK2	AA071	13-190	with EC733838
A2M2S05	–LSR DECODE 2 ALU2	AA191CE6	AA191	13-190	w/o EC733838

3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
A2M2S07	–LSR DECODE 3 ALU2	AA191CF6	AA191	13-190	w/o EC733838
A2M2S09	–LSR DECODE 5 ALU2	AA191CJ6	AA191	13-190	w/o EC733838
A2M2S12	+ROS BIT 6	QA011DB4	AA061	16-090	
A2M2U02	–LSR DECODE 0 ALU2	AA071AJ6	AA071	13-190	w/o EC733838
A2M2U02	+LSR ADDRESS BIT 8 ALU2	AA071CH2	AA071	13-190	with EC733838
A2M2U03	+LSR ADDRESS BIT 1 ALU2	AA071CN2	AA071	13-190	with EC733838
A2M2U03	–LSR DECODE 3 ALU2	AA071GJ6	AA071	13-190	w/o EC733838
			AA071	13-220	w/o EC733838
A2M2U04	+ROS BIT 4	QA011BK4	AA061	16-090	
A2M2U05	–LSR DECODE 1 ALU2	AA191CC6	AA191	13-190	w/o EC733838
A2M2U06	–LSR DECODE 7 ALU2	AA191CM6	AA191	13-190	w/o EC733838
A2M2U07	–LSR DECODE 0 ALU2	AA191CB6	AA191	13-190	w/o EC733838
A2M2U09	+ROS BIT 7	QA011DD4	AA061	16-090	
A2M2U10	–LSR DECODE 6 ALU2	AA191CL6	AA191	13-190	w/o EC733838
A2M2U11	+ROS BIT 5	QA011BM4	AA061	16-090	
A2M2U12	–LSR DECODE 4 ALU2	AA191CH6	AA191	13-190	w/o EC733838
A2N2B11	–B BUS PARITY ERROR ALU2	AA261DK6	AA261	16-100	
A2N2B12	+REGISTER IN BIT 7 ALU2	AA431GN6	AA211	16-110	
A2N2D06	+CLK 16 ALU2	AA041AH2	AA261	16-110	
A2N2D09	+REGISTER IN BIT P ALU2	AA431GA6	AA261	16-110	
A2N2G02	–B BUS 7 ALU 2	AA231FK6	AA261	13-420	
			AA261	16-100	
A2N2G03	–B BUS 2 ALU2	AA221FG6	AA261	16-100	
A2N2G04	–B BUS 1 ALU2	AA221FD6	AA261	16-100	
A2N2G07	–B BUS 0 ALU2	AA221FA6	AA261	16-100	
A2N2G08	+REGISTER IN BIT 5 ALU2	AA431GK6	AA211	16-110	
A2N2G09	–D BUS 0 ALU2	AA201FB6	AA261	16-110	
A2N2G11	–D BUS 6 ALU2	AA211FJ6	AA261	16-110	
A2N2G12	–CHK B BUS ON EXT XFR	AA171AD6	AA261	16-100	
A2N2G13	+REGISTER IN BIT 4 ALU2	AA431GH6	AA211	16-110	
A2N2J03	+REGISTER IN BIT 6 ALU2	AA431GL6	AA211	16-110	
A2N2J04	–B BUS 5 ALU2	AA231FD6	AA261	16-100	
A2N2J05	–B BUS 6 ALU2	AA231FG6	AA261	16-100	
A2N2J06	–B BUS 4 ALU2	AA231FA6	AA261	16-100	
A2N2J07	–B BUS 3 ALU2	AA221FK6	AA261	16-100	
A2N2J09	–D BUS 7 ALU2	AA211FM6	AA261	16-110	
A2N2J11	+CLK 22 L1 ALU2	AA041EJ6	AA211	16-110	
A2N2J13	–CLK 15 ALU2	AA041GG4	AA191	16-100	
A2N2M02	–D BUS 5 ALU2	AA211FE6	AA261	16-110	
A2N2M05	–D BUS 4 ALU2	AA211FB6	AA261	16-110	
A2N2M09	+REGISTER IN BIT 2 ALU2	AA431GE6	AA201	16-110	
A2N2M13	+REGISTER IN BIT 1 ALU2	AA431GD6	AA201	16-110	
A2N2P04	+REGISTER IN BIT 3 ALU2	AA431GG6	AA201	16-110	
A2N2P05	+CLK 21 ALU2	AA041BD2	AA201	16-110	
A2N2P12	–D BUS 3 ALU2	AA201FM6	AA261	16-110	
A2N2P13	–D BUS 2 ALU2	AA201FJ6	AA261	16-110	
A2N2S05	+REGISTER IN BIT 0 ALU2	AA431GB6	AA201	16-110	
A2N2U04	–D BUS 1 ALU2	AA201FE6	AA261	16-110	
A2P4B04	–INSTRUCTION CARD ERROR ALU2	AA271GE6	AA461	16-090	
A2P4B13	–INSTRUCTION CARD ERROR ALU1	AB281GE6	AA471	16-020	
A2P4D02	–IC ROS REG PARITY ERROR	AA181GF6	AA461	16-080	
A2P4D04	–D BUS PARITY ERROR ALU2	AA261GC6	AA461	16-110	
A2P4D06	+TRAP ALU2 LATCH 2	XC032CH4	AA451	13-190	
A2P4D13	–ALU2 LOCKED STATUS	AA451GF2	AA451	13-190	
A2P4G02	+SYSTEM RESET	AB011BL6	AA451	13-010	
A2P4G03	+BLOCK ALU1 IC	AA451GA2	AA451	13-050	
A2P4G09	+LOCK ALU2 IC	AA451GF6	AA451	13-190	
A2P4G11	+XFR SET CHECKOUT ERROR	AB181CN2	AB471	16-060	
A2P4G12	–D BUS PARITY ERROR ALU1	AB271GF4	AA471	16-040	
A2P4J02	+XFR SET CHECKOUT ERROR	AA171EF2	AA461	16-130	
A2P4J03	–HARDWARE ERROR ALU1	AA451GA6	AA451	13-010	
			AA451	13-400	
A2P4J04	+BRANCH ERROR ALU2	XC032CE4	AA461	16-120	
A2P4J05	–TRAP ALU2	AA451BK2	AA451	13-190	
			AA451	13-420	
A2P4J10	–IC ROS REG PARITY ERROR	AB191GF6	AB471	16-010	
A2P4J11	–BRANCH ERROR ALU1	AB151GJ6	AB471	16-050	
A2Q2B02	+REGISTER IN BIT 1 ALU1	AB441GD6	AB441	16-040	
A2Q2B03	–STAT BIT 1 START WR/RD	AA141GF6	AA141	16-170	
			AA141	17-170	
A2Q2B05	+REGISTER IN BIT 0 ALU1	AB441GB6	AB441	16-040	
A2Q2D02	+STAT D ALU2 TO ALU1	AA141EL2	AA141	13-190	
A2Q2D03	+REGISTER IN BIT 2 ALU1	AB441GE6	AB441	16-040	
A2Q2D04	–STAT BIT 0 TAPE OP TO AIU1	AA141GD6	AA141	13-380	
A2Q2D06	+REGISTER IN BIT 3 ALU1	AB441GG6	AB441	16-040	
A2Q2D11	–B BUS 7 ALU2	AA411FM4	AA411	13-420	
A2Q2G09	–XOUTA BIT 1 ALU2 TO DF	AA141GB2	AA141	17-170	
A2Q2G11	+REGISTER IN BIT 6 ALU1	AB441GL6	AB441	16-040	
A2Q2G12	+REGISTER IN BIT 4 ALU1	AB441GH6	AB441	16-040	
A2Q2G13	+REGISTER IN BIT 7 ALU1	AB441GN6	AB441	16-040	
A2Q2J04	–XOUTA BIT 5 ALU2 TO DF	AA141CD2	AA141	16-170	
A2Q2J07	–STAT BIT 0 TAPE OP TO DF	AA141GE6	AA141	13-380	
A2Q2J11	+REGISTER IN BIT 5 ALU1	AB441GK6	AB441	16-040	
A2Q2M05	–STAT B ALU2 TO ALU1	AA141GK6	AA141	13-420	
A2Q2M09	–STAT D ALU2 TO ALU1	AA141GM6	AA141	13-190	
			AA141	13-420	
A2Q2S11	–XOUTA BIT 2 ALU2 TO DF	AA141EB6	AA141	16-170	
A2Q2S12	+REGISTER IN BIT P ALU1	AB441GA6	AB441	16-040	
A2R2B04	–CTI BIT 7 OP IN	FC161GM2	FC161	13-210	
			FC161	13-250	
A2R2B05	+TUBO BIT 2	BW071GD6	FD021	16-160	
			FD021	16-180	
			FD021	16-210	
A2R2B07	–TUBO BIT 4	FD021GG2	FD021	16-160	
			FD021	16-180	
			FD021	16-190	
			FD021	16-210	
			FD021	17-180	
A2R2B09	+TUBO BIT 5	BW081GD6	FD021	16-160	
			FD021	16-180	
			FD021	16-210	
A2R2B10	–TUBO BIT 5	FD021GH2	FD021	16-160	
			FD021	16-180	
			FD021	16-190	
			FD021	16-210	
			FD021	17-180	
A2R2B11	+CTI BIT 4 SERVICE IN	FC161GH2	FC161	13-170	
			FC161	15-050	
A2R2B12	–TUBO BIT 1	FD021GB2	FD021	16-160	
			FD021	16-180	
			FD021	16-190	
			FD021	16-210	
			FD021	17-180	
A2R2B13	+TUBO BIT 1	BW061GM6	FD021	16-160	
			FD021	16-180	
			FD021	16-210	
A2R2D03	–TUTAG BIT 7 MOVE	FD041GG6	FD041	13-050	
			FD041	16-170	
A2R2D05	–TUBO BIT 2	FD021GD2	FD021	16-160	
			FD021	16-180	
			FD021	16-190	
			FD021	16-210	
			FD021	17-180	
A2R2D09	+TUBO BIT 4	BW071GM6	FD021	16-160	
			FD021	16-180	
			FD021	16-210	
A2R2D10	+CTI BIT 6 TO CE	FC161GL2	FC161	13-140	
			FC161	13-290	
A2R2D12	+TUBO BIT 0	BW061GH6	FD021	16-160	
			FD021	16-180	
			FD021	16-210	

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3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
A2R2D13	+TUBO BIT 3	BW071GH6	FD021	16-160	
			FD021	16-180	
			FD021	16-210	
A2R2G02	–TUBO BIT 3	FD021GE2	FD021	16-160	
			FD021	16-180	
			FD021	16-190	
			FD021	16-210	
			FD021	17-180	
A2R2G05	–B BUS 1 ALU2	AA411DC6	FD021	16-160	
			FD021	16-210	
A2R2G09	–CBI BIT 2	FC171GD2	FC171	15-080	
			FC171	15-140	
A2R2G10	–CBI BIT 6	FC171GJ2	FC171	15-080	
			FC171	15-140	
A2R2G11	–CBI BIT 5	FC171GH2	FC171	15-080	
			FC171	15-140	
A2R2G12	+TUBO BIT 6	BW081GH6	FD021	16-160	
			FD021	16-180	
			FD021	16-210	
A2R2G13	–TUBO BIT 6	FD021GK2	FD021	16-160	
			FD021	16-180	
			FD021	16-190	
			FD021	16-210	
			FD021	17-180	
A2R2J02	+CTI BIT 5 TO CE	FC161GJ2	FC161	13-280	
A2R2J03	–B BUS 3 ALU2	AA411DK4	FD021	16-160	
			FD021	16-210	
A2R2J05	–B BUS 2 ALU2	AA411BN4	FD021	16-160	
			FD021	16-210	
A2R2J06	–TU TAG BIT 6 COMMAND	FD041GE2	FD041	15-090	
			FD041	16-160	
A2R2J07	–B BUS 0 ALU2	AA411BK4	FD021	16-160	
			FD021	16-210	
A2R2J10	–CBI BIT 7	FC171GK2	FC171	15-080	
			FC171	15-140	
A2R2J11	+DATA BUS IN 7	BB001FF4	FC211	15-140	
A2R2J12	+DATA BUS IN 3	BB001DD4	FC211	15-140	
A2R2M03	+TUBO BIT 7	BW081GM6	FD021	16-160	
			FD021	16-180	
A2R2M04	+DATA BUS IN 2	BB001CC4	FC211	15-140	
A2R2M09	–B BUS 5 ALU2	AA411DN4	FD021	16-160	
			FD021	16-210	
A2R2M12	–B BUS 4 ALU2	AA411DM4	FD021	16-160	
			FD021	16-210	
A2R2P02	+BUS IN 5	BS071EG7	FC211	15-140	
A2R2P03	+DATA BUS IN 1	BB001BB4	FC211	15-140	
A2R2P04	+BUS IN 6	BS071GK2	FC211	15-140	
A2R2P06	+DATA BUS IN 4	BB001EE4	FC211	15-140	
A2R2P07	+DATA BUS IN 0	BB001AA4	FC211	15-140	
A2R2P13	–B BUS 7 ALU2	AA411FM4	FD021	16-160	
			FD021	16-210	
A2R2S02	–TUBO BIT 7	FD021GL2	FD021	16-160	
			FD021	16-180	
			FD021	16-190	
			FD021	16-210	
			FD021	17-180	
A2R2S03	–TUBO BIT 0	FD021GA2	FD021	16-160	
			FD021	16-180	
			FD021	16-190	
			FD021	16-210	
			FD021	17-180	
A2R2S04	–CBI BIT 4	FC171GG2	FC171	15-080	
			FC171	15-140	
A2R2S05	–CBI BIT 3	FC171GE2	FC171	15-080	
			FC171	15-140	
A2R2S07	–CBI BIT 1	FC171GB2	FC171	15-080	
			FC171	15-140	
A2R2S09	–CBI BIT 0	FC171GA2	FC171	15-080	
			FC171	15-140	
A2R2S11	–REGISTER TEST	FC161GN4	FC161	13-320	
			FC161	13-340	
A2R2U03	–B BUS 6 ALU2	AA411FK4	FD021	16-160	
			FD021	16-210	
A2R2U11	–CTI BIT 5 STATUS IN	FC161GJ6	FC161	15-080	
A2T2B03	–STAT BIT 1 SENSE	AB141GF6	AB141	15-100	
			AB141	15-140	
A2T2B04	+STAT BIT 0 ALU1 UNUSED	AB141GD2	AB141	13-440	
A2T2D04	–STAT BIT 0 ALU1 TO ALU2	AB141FD2	AB141	13-440	
A2T2D05	+STAT BIT 1 SENSE	AB141GF2	AB141	13-380	
			AB141	15-140	
A2T2D11	–B BUS 7 ALU1	AB421FM6	AB421	13-320	
A2T2G10	+STAT BIT 0 ALU1 STOP SERV	AB141GE2	AB141	13-470	
A2T2J10	–DEVICE BUS IN 3 TO DF	XC032AH4	FD011	16-160	
			FD011	16-210	
A2T2M02	–DEVICE BUS IN 2 TO DF	XC032AF4	FD011	16-160	
			FD011	16-210	
A2T2M04	–DEVICE BUS IN 0 TO DF	XC032AD4	FD011	16-160	
			FD011	16-210	
A2T2M10	–DEVICE BUS IN 5 TO DF	XC032AK4	FD011	16-160	
			FD011	16-210	
A2T2P03	–DEVICE BUS IN 1 TO DF	XC032AE4	FD011	16-160	
			FD011	16-210	
A2T2P07	–DEVICE BUS IN 6 TO DF	XC032AL4	FD011	16-160	
			FD011	16-210	
A2T2P09	–DEVICE BUS IN 7 TO DF	XC032AM4	FD011	16-160	
			FD011	16-210	
A2T2P11	–DEVICE BUS IN 4 TO DF	XC032AJ4	FD011	16-160	
			FD011	16-210	
B2C2B09	–ALU 0 ALU1	AB271FE6	AB271	13-220	
			AB271	13-380	
B2C2B11	–B BUS PARITY ERROR ALU1	AB271DK6	AB271	16-030	
B2C2B12	+BUS OUT BIT 7 TO ALU1	AB451FM6	AB221	16-040	
B2C2D06	+CLK 16 ALU1	AB041AH2	AB271	16-040	
B2C2D09	+BUS OUT BIT P TO ALU1	AB451FN4	AB271	16-040	
B2C2G02	–B BUS 7 ALU1	AB241FK6	AB241	13-320	
			AB271	16-030	
B2C2G03	–B BUS 2 ALU1	AB231FG6	AB271	16-030	
B2C2G04	–B BUS 1 ALU1	AB231FD6	AB271	16-030	
B2C2G07	–B BUS 0 ALU1	AB231FA6	AB271	16-030	
B2C2G08	+BUS OUT BIT 5 TO ALU1	AB451FK6	AB221	16-040	
B2C2G09	–D BUS 0 ALU1	AB211FB6	AB211	13-320	
			AB271	16-040	
B2C2G11	–D BUS 6 ALU1	AB221FJ6	AB201	13-320	
			AB271	16-040	
B2C2G12	–CHK B BUS ON EXT XFR	AB181AD6	AB271	16-030	
B2C2G13	+BUS OUT BIT 4 TO ALU1	AB451FJ6	AB221	16-040	
B2C2J03	+BUS OUT BIT 6 TO ALU1	AB451FL6	AB221	16-040	
B2C2J04	–B BUS 5 ALU1	AB241FD6	AB271	16-030	
B2C2J05	–B BUS 6 ALU1	AB241FG6	AB271	16-030	
B2C2J06	–B BUS 4 ALU1	AB241FA6	AB271	16-030	
B2C2J07	–B BUS 3 ALU1	AB231FK6	AB271	16-030	
B2C2J09	–D BUS 7 ALU1	AB221FM6	AB201	13-320	
			AB221	16-040	
B2C2J11	+CLK 22 L1 ALU1	AB041EJ6	AB221	16-040	
B2C2J13	–CLK 15	AB041GG6	AB201	16-030	
B2C2M02	–D BUS 5 ALU1	AB221FE6	AB201	13-320	
			AB271	16-040	
B2C2M05	–D BUS 4 ALU1	AB221FB6	AB201	13-320	
			AB271	16-040	
B2C2M09	+BUS OUT BIT 2 TO ALU1	AB451FG6	AB211	16-040	
B2C2M13	+BUS OUT BIT 1 TO ALU1	AB451FF6	AB211	16-040	

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3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
B2C2P04	+BUS OUT BIT 3 TO ALU1	AB451FH6	AB211	16-040	
B2C2P05	+CLK 21 ALU1	AB041BD2	AB221	16-040	
B2C2P12	−D BUS 3 ALU1	AB211FM6	AB201	13-320	
			AB271	16-040	
B2C2P13	−D BUS 2 ALU1	AB211FJ6	AB201	13-320	
			AB271	16-040	
B2C2S05	+BUS OUT BIT 0 TO ALU1	AB451FE6	AB211	16-040	
B2C2U04	−D BUS 1 ALU1	AB211FE6	AB201	13-320	
			AB271	16-040	
B2D2B02	−PAGE BIT 6 ALU1	AB111EC6	AB111	13-090	
B2D2B04	−PAGE BIT 4 ALU1	AB111EA6	AB111	13-090	
B2D2B05	−PAGE BIT 5 ALU1	AB111EB2	AB111	13-090	
B2D2B09	+ROS REG 3 ALU1	AB071DD6	AB071	13-370	
B2D2B10	+ROS REG 0 ALU1	AB071CA2	AB071	13-090	
			AB071	13-190	
B2D2B11	−LSR DECODE 5 ALU1	AB071CL6	AB071	13-090	w/o EC733838
			AB071	13-320	w/o EC733838
B2D2B12	−LSR DECODE 6 ALU1	AB071EL6	AB071	13-090	w/o EC733838
B2D2B13	−ROS REG 4 ALU1	AB071CH6	AB071	13-090	
			AB071	16-020	
			AB071	16-050	
B2D2D05	−ROS REG 5 ALU1	AB071CJ6	AB071	13-090	
			AB071	16-050	
B2D2D07	−ROS REG 7 ALU1	AB071CN6	AB071	13-090	
			AB071	16-050	
B2D2D09	−ROS REG 6 ALU1	AB071CL6	AB071	13-090	
			AB071	13-280	
			AB071	16-050	
B2D2D10	−ROS REG 3 ALU1	AB071DD2	AB071	13-090	
			AB071	13-190	
			AB071	13-220	
			AB071	16-050	
B2D2D11	+BRANCH COND MET ALU1	AB151GG6	AB281	16-020	
B2D2D13	−LSR DECODE 4	AB071AL6	AB071	13-090	w/o EC733838
B2D2G02	−LSR DECODE 7	AB071GL6	AB071	13-090	w/o EC733838
B2D2G04	−BU OPERATION ALU1	AB111BF6	AB111	13-090	
B2D2G05	+ROS BIT 1	QB011BD4	AB051	16-020	
B2D2G07	+ROS BIT 0	QB011BB4	AB051	16-020	
B2D2G10	+ROS BIT P1	QB011FK4	AB071	16-020	
B2D2G12	−XFR OPERATION ALU1	AB111BM6	AB111	13-090	
			AB111	13-320	
B2D2J02	+ROS BIT 3	QB011BH4	AB051	16-020	
B2D2J04	−BU OR BOC ALU1	AB111CG2	AB111	13-090	
B2D2J06	+ROS BIT 2	QB011BF4	AB051	16-020	
B2D2J12	−ADD OPERATION ALU1	AB111EL6	AB111	13-090	
			AB111	13-370	
B2D2J13	−STORE OPERATION ALU1	AB111BK6	AB111	13-090	
			AB111	13-320	
B2D2M02	+BUS PARITY OK	FC011GB6	AB131	15-030	
B2D2M09	−BOC OPERATION ALU1	AB111BH6	AB111	13-090	
B2D2M13	+LSR ADDRESS BIT 2 ALU1	AB071CM2	AB071	13-090	with EC733838
B2D2M13	−LSR DECODE 2	AB071EJ6	AB071	13-090	w/o EC733838
B2D2P02	−LOGIC OPERATION ALU1	AB111FN6	AB111	13-090	
B2D2P04	+ROS REG 5 ALU1	AB071CJ2	AB071	16-050	
B2D2P06	−PAGE BIT 7 ALU1	AB111ED6	AB111	13-090	
B2D2P09	−ROS REG 0 AND 1 ALU1	AB111EJ6	AB111	13-090	
			AB111	13-320	
			AB111	13-380	
B2D2P11	−GROUP OR DFLER BRANCH	FC091GM4	AB131	13-480	
B2D2P12	−ROS REG 0 AND 2 ALU1	AB111EG6	AB111	13-090	
			AB111	13-380	
B2D2P13	−LSR DECODE 1 ALU1	AB071CJ6	AB071	13-090	w/o EC733838
			AB071	13-320	
B2D2P13	+LSR ADDRESS BIT 4 ALU1	AB071CK2	AB071	13-090	with EC733838
			AB071	13-320	
B2D2S05	−LSR DECODE 2B ALU1	AB201CE6	AB201	13-090	w/o EC733838

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
B2D2S07	−LSR DECODE 3B ALU1	AB201CF6	AB201	13-090	w/o EC733838
B2D2S09	−LSR DECODE 5B ALU1	AB201CJ6	AB201	13-090	w/o EC733838
B2D2S12	+ROS BIT 6	QB011DB4	AB051	16-020	
B2D2U02	−LSR DECODE 0 ALU1	AB071AJ6	AB071	13-090	w/o EC733838
B2D2U02	+LSR ADDRESS BIT 8 ALU1	AB071CH2	AB071	13-090	with EC733838
B2D2U03	+LSR ADDRESS BIT 1 ALU1	AB071CN2	AB071	13-090	with EC733838
B2D2U03	−LSR DECODE 3 ALU1	AB071GJ6	AB071	13-090	w/o EC733838
			AB071	13-240	w/o EC733838
B2D2U04	+ROS BIT 4	QB011BK4	AB051	16-020	
B2D2U05	−LSR DECODE 1B ALU1	AB201CC6	AB201	13-090	w/o EC733838
B2D2U06	−LSR DECODE 7B ALU1	AB071AK6	AB071	16-170	with EC733838
B2D2U06	−LSR DECODE 7B ALU1	AB201CM6	AB201	13-090	w/o EC733838
B2D2U07	−LSR DECODE 0B ALU1	AB201CB6	AB201	13-090	w/o EC733838
			AB201	13-190	w/o EC733838
B2D2U09	+ROS BIT 7	QB011DD4	AB051	16-020	
B2D2U10	−LSR DECODE 6B ALU1	AB201CL6	AB201	13-090	w/o EC733838
B2D2U11	+ROS BIT 5	QB011BM4	AB051	16-020	
B2D2U12	−LSR DECODE 4B ALU1	AB201CH6	AB201	13-090	w/o EC733838
			AB201	13-250	w/o EC733838
B2E2B02	+ROS REG 14 MASK ALU1	AB061FL6	AB061	13-090	
B2E2B03	+ROS REG 15 MASK ALU1	AB061FN6	AB061	13-090	
B2E2B04	+ROS BIT 14	QB011FF4	AB061	16-010	
B2E2B05	+ROS BIT 12	QB011FB4	AB061	16-010	
B2E2B07	+ROS REG 12 MASK ALU1	AB061FG6	AB061	13-090	
B2E2B09	−150 NS TAP ALU1	AB021AJ6	AB101	16-010	
B2E2B10	+ROS REG 13 MASK ALU1	AB061FJ6	AB061	13-090	
B2E2B11	+XFR LSR 1 TO CHNL BUS IN	AB181CC2	AB181	13-380	
B2E2D02	+ROS BIT 15	QB011FH4	AB061	16-010	
B2E2D05	+ROS BIT P2	QB011FM4	AB101	16-010	
B2E2D09	+ROS BIT 13	QB011FD4	AB061	16-010	
B2E2D11	+XFR XOUTB TO TRAP ALU2	AB181GF2	AB181	13-190	
B2E2D12	+XFR LSR 1 TO CHANNEL TAGS	AB181CF2	AB181	13-320	
B2E2G03	+ROS REG 10 MASK ALU1	AB061CE6	AB061	13-090	
B2E2G04	+ROS REG 9 MASK ALU1	AB061CC6	AB061	13-090	
B2E2G05	+ROS BIT 10	QB011DK4	AB061	16-010	
B2E2G07	+RESET CUE CHAN A	AB181GM2	AB181	13-050	
B2E2G12	+INST COUNT 10 ALU1	AB195CH4	AB195	13-090	
			AB195	13-140	
B2E2G13	+INST COUNT 9 ALU1	AB195CE4	AB195	13-090	
B2E2J03	+ROS BIT 11	QB011DM4	AB061	16-010	
B2E2J04	+ROS REG 11 MASK ALU1	AB061CG6	AB061	13-090	
B2E2J05	+ROS BIT 9	QB011DH4	AB061	16-010	
B2E2J06	+ROS BIT 8	QB011DF4	AB061	16-010	
B2E2J11	+RESET CUE CHAN B	AB181GJ2	AB181	13-200	
			AB181	13-500	
B2E2J12	+XFR B BUS TO IC	AB181CJ2	AB181	13-130	
B2E2J13	+INST COUNT 11 ALU1	AB195CL4	AB195	13-090	
B2E2M02	+INST COUNT 12 ALU1	AB195FB4	AB195	13-090	
B2E2M03	+INST COUNT 13 ALU1	AB195FE4	AB195	13-090	
			AB195	13-220	
B2E2M05	+ROS REG 8 MASK ALU1	AB061CA6	AB061	13-090	
			AB061	16-030	
B2E2M07	−XFR LSR TO A REGISTER	AB181CM2	AB181	13-380	
B2E2M08	−GATE CHAN BUS OUT TO ALU	AB181CB6	AB181	16-040	
B2E2M10	−XFR XINB TO LSR1	AB181EB6	AB181	13-320	
B2E2M12	+CLK 1 NOT CE CYC L2 ALU1	AB041BJ2	AB101	16-010	
B2E2M13	+INHIBIT RIPPLE BUS CHAN A	FC021BB2	AB101	13-380	
B2E2P02	+INST COUNT 15 ALU1	AB195FL4	AB195	13-090	
B2E2P03	+INST COUNT 14 ALU1	AB195FH4	AB195	13-090	
B2E2P11	+INST COUNT 8 ALU1	AB195CB4	AB195	13-090	
			AB195	13-140	
B2E2P12	−XFR XINA TO LSR1	AB181CE6	AB181	13-320	
B2E2P13	+INHIBIT RIPPLE BUS CHAN B	XM021BB2	AB101	13-380	
B2E2S04	−ROS REG 8 ALU1	AB061CA2	AB181	16-040	
B2E2U04	−BOC MET ALU1	AB281CM2	AB195	16-010	

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
B2F2B02	–50 NS TAP POWERED ALU1	AB041CD6	AB041	13-050	
B2F2B04	+CLK4 ALU1	AB041EC6	AB041	13-220	
			AB041	13-320	
B2F2B09	–20.48 MHZ	BS011GJ6	AB011	13-010	
B2F2D05	+RESET HI ORDER ROS ALU1	AB031CM6	AB031	13-090	
B2F2D06	+CLK 22 L1 ALU1	AB041EJ6	AB041	13-320	
B2F2D10	–SYSTEM RESET	AB011BL2	AB011	13-010	
B2F2D12	+SYSTEM RESET	AB011BL6	AB011	13-010	
B2F2G02	+CLK 21 ALU1	AB041BD2	AB041	13-320	
			AB041	13-380	
B2F2G03	+CLK 1 NOT CE CYC L2 ALU1	AB041BJ2	AB041	13-090	
B2F2G05	+CLK 1 L3 ALU1	AB041AL6	AB041	13-090	
B2F2G07	–GATE TRAP PULSE	AB031GA6	AB031	13-010	
B2F2G08	+CLK 16 ALU1	AB041AH2	AB041	13-380	
B2F2G12	–0 NS TAP ALU1	AB021AC6	AB021	13-000	
			AB021	16-000	
B2F2J02	–CE COMPARE SAMPLE ALU1	AB021FH2	AB021	12-020	
B2F2J05	+CLK 1 NOT CE CYC L1 ALU1	AB041BG2	AB041	13-090	
			AB041	16-020	
B2F2J10	+5.12 MHZ	BS011EH6	AB031	13-010	
B2F2J12	+125 NS TAP ALU1	AB021AH2	AB021	13-320	
B2F2M02	–CLK 17 DLYD ALU1 TP	AB041EB6	AB041	16-050	
B2F2M03	+CLK 19 ALU1	AB041BB2	AB041	13-370	
B2F2M08	+CLK 6 ALU1	AB041GD6	AB041	13-090	
B2F2M13	+CLK 8 ALU1	AB041GM4	AB041	13-090	
B2F2P02	+CLK 22 ALU1	AB041EG6	AB041	13-320	
			AB041	13-380	
B2F2P04	–150 NS TAP ALU1	AB021AJ6	AB021	12-020	
			AB021	13-370	
B2F2P09	–CLK 15 ALU1	AB041GG4	AB041	13-320	
B2F2P12	–100 NS TAP ALU1	AB021AG6	AB021	12-020	
			AB021	13-090	
B2F2S04	–100-175 NS	AB021ED2	AB021	13-320	
B2F2S09	–CLK 11 ALU1	AB041BF6	AB041	13-090	
B2F2S10	–25 NS TAP ALU1	AB021CA4	AB021	13-050	
B2F2U07	–75 NS TAP ALU1	AB021AF6	AB041	13-090	
			AB021	13-320	
B2H2M02	+ROS BIT P1 ROS X	QB091AA6	QB091	13-090	
B2H2M03	+ROS BIT 15 ROS X	QB091EJ6	QB091	13-090	
B2H2P02	+ROS BIT P2 ROS X	QB091EL6	QB091	13-090	
B2H2P04	+ROS BIT 14 ROS X	QB091EG6	QB091	13-090	
B2H2P05	+ROS BIT 13 ROS X	QB091EE6	QB091	13-090	
B2H2P06	+ROS BIT 12 ROS X	QB091EC6	QB091	13-090	
B2H2P07	+ROS BIT 11 ROS X	QB091EA6	QB091	13-090	
B2H2P09	+ROS BIT 10 ROS X	QB091CL6	QB091	13-090	
B2H2P10	+ROS BIT 9 ROS X	QB091CJ6	QB091	13-090	
B2H2P11	+ROS BIT 8 ROS X	QB091CG6	QB091	13-090	
B2H2U02	+ROS BIT 7 ROS X	QB091CE6	QB091	13-090	
B2H2U03	+ROS BIT 6 ROS X	QB091CC6	QB091	13-090	
B2H2U04	+ROS BIT 5 ROS X	QB091CA6	QB091	13-090	
B2H2U05	+ROS BIT 4 ROS X	QB091AL6	QB091	13-090	
B2H2U10	+ROS BIT 3 ROS X	QB091AJ6	QB091	13-090	
B2H2U11	+ROS BIT 2 ROS X	QB091AG6	QB091	13-090	
B2H2U12	+ROS BIT 1 ROS X	QB091AE6	QB091	13-090	
B2H2U13	+ROS BIT 0 ROS X	QB091AC6	QB091	13-090	
B2L2B05	–BUS OUT BIT 0	FC081GC2	FC081	16-040	w/o EC733814
			FC081	17-010	w/o EC733814
B2L2B07	–BUS OUT BIT 2	FC081GE2	FC081	16-040	w/o EC733814
			FC081	17-010	w/o EC733814
B2L2B07	+MACH RESET	FC141GF2	FC141	13-010	with EC733814
B2L2B09	–BUS OUT BIT 3	FC081GG2	FC081	16-040	w/o EC733814
			FC081	17-010	w/o EC733814
B2L2B09	+MACH RESET	FC141GH2	FC141	13-320	with EC733814

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
B2L2D06	–BUS OUT BIT 1	FC081FD2	FC081	16-040	w/o EC733814
			FC081	17-010	w/o EC733814
B2L2D07	+COMMAND OUT CHAN A GATED	FC021FE2	FC151	15-040	with EC733814
B2L2D09	+CE SERVICE OUT TAG	PK081FL6	FC151	13-110	with EC733814
B2L2D10	+CE COMMAND OUT TAG	PK081FJ6	FC151	13-100	with EC733814
			FC151	15-040	with EC733814
B2L2D12	+IF BUS OUT 4 CHAN A	FC061DD6	FC071	15-030	w/o EC733814
B2L2D13	+DATA SERVICE ACTIVE	FC111CH2	FC151	13-100	with EC733814
			FC151	17-370	with EC733814
B2L2G03	+IF BUS OUT 6 CHAN A	FC061DD8	FC071	15-030	w/o EC733814
B2L2G03	+SERVICE OUT CHAN A B CE	FC151CF6	FC151	13-100	with EC733814
			FC151	13-280	with EC733814
			FC151	13-350	with EC733814
			FC151	17-370	with EC733814
B2L2G04	–BUS OUT BIT 6	FC081GL2	FC081	16-040	w/o EC733814
			FC081	17-010	w/o EC733814
B2L2G04	–OPERATIONAL IN	FC141GK6	FC141	13-210	with EC733814
			FC141	13-250	with EC733814
B2L2G05	–BUS OUT BIT 7	FC081GN2	FC081	16-040	w/o EC733814
			FC081	17-010	w/o EC733814
B2L2G05	+POWER ON RESET	FC141FF2	FC141	13-010	with EC733814
B2L2G08	+BUS OUT 7 CHANNEL B	XM071GN2	FC081	17-010	w/o EC733814
B2L2G09	+COMMAND OUT OR HIO	FC151EN4	FC111	15-040	w/o EC733814
B2L2G10	–BUS OUT BIT 4	FC081FH2	FC081	16-040	w/o EC733814
			FC081	17-010	w/o EC733814
B2L2G11	–GATE TRAP PULSE	AB031GA6	FC141	13-010	with EC733814
B2L2G12	+BUS OUT PARITY ODD CHAN A	FC091GC2	FC151	15-030	with EC733814
B2L2G13	+BUS OUT BIT 3 CHANNEL B	XM071GG2	FC081	17-010	w/o EC733814
B2L2J02	–BUS OUT BIT 5	FC081GJ2	FC081	16-040	w/o EC733814
			FC081	17-010	w/o EC733814
B2L2J03	–POWER RESET	FC271FF4	FC141	13-010	with EC733814
B2L2J03	+BUS OUT BIT 1 CHANNEL B	XM071FD2	FC081	17-010	w/o EC733814
B2L2J04	+BUS OUT BIT 0 CHANNEL B	XM071GC2	FC081	17-010	w/o EC733814
			FC081	17-010	w/o EC733814
B2L2J06	+BUS OUT 6 CHANNEL B	XM071GL2	FC081	17-010	w/o EC733814
B2L2J10	+COMMAND OUT CH B GATED	XM021FE2	FC151	15-040	with EC733814
B2L2J11	+BUS OUT BIT P CHANNEL B	XM071GA2	FC081	17-010	w/o EC733814
B2L2J12	+BUS OUT BIT 4 CHANNEL B	XM071FH2	FC081	17-010	w/o EC733814
B2L2J12	+BUS OUT PARITY ODD CHAN B	XM081GC2	FC151	15-030	with EC733814
B2L2M03	+BUS OUT 5 CHANNEL B	XM071GJ2	FC081	17-010	w/o EC733814
B2L2M04	–BUS OUT BIT P	FC081GA2	FC081	16-040	w/o EC733814
			FC081	17-010	w/o EC733814
B2L2M05	+IF BUS OUT 1 CHAN A	FC061DD3	FC071	15-030	w/o EC733814
B2L2M08	–HARDWARE ERROR ALU1	AA451GA6	FC141	13-010	with EC733814
B2L2M08	+STAT BIT 0 ALU1 STOP SERV	AB141GE2	FC111	13-480	w/o EC733814
B2L2M09	+IF BUS OUT 3 CHAN A	FC061DD5	FC071	15-030	w/o EC733814
B2L2M10	+BUS OUT PARITY ODD	FC151DD6	FC111	15-030	w/o EC733814
B2L2M11	+BRANCH COND MET ALU1	AB151GG6	AB151	13-090	with EC733814
			AB151	13-280	with EC733814
			AB151	17-370	with EC733814
B2L2M12	+BUS PARITY OK	FC111GB6	FC111	15-030	w/o EC733814
B2L2M13	+IF BUS OUT 0 CHAN A	FC061DD2	FC071	15-030	w/o EC733814
B2L2P05	+BUS OUT BIT 2 CHANNEL B	XM071GE2	FC081	17-010	w/o EC733814
B2L2P09	–RESET ALU1 1C	FC141GB6	FC141	13-380	with EC733814
B2L2P12	+RESET ALU1 IC	FC141GB2	FC141	13-010	with EC733814
			FC141	13-380	with EC733814
B2L2S02	+DATA SERVICE ACTIVE	FC111CH2	FC111	13-280	w/o EC733814
B2L2S02	–SUPPRESS OUT A B	FC151AD2	FC151	13-310	with EC733814
			FC151	13-340	with EC733814
B2L2S03	+ROS REG 6 ALU1	AB071CL2	AB171	16-050	with EC733814
B2L2S04	+IF BUS OUT 2 CHAN A	FC061DD4	FC071	15-030	w/o EC733814
B2L2S05	–ADDRESS OUT A B CE	AB171CB2	FC141	13-300	with EC733814
			FC151	13-360	with EC733814
B2L2S07	–STAT BIT 0 TP OP TO ALU1	AA141GD6	FC111	13-100	w/o EC733814
			FC111	13-480	w/o EC733814
			FC111	15-030	w/o EC733814

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3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
B2L2S07	–ROS REG 6 ALU1	AB071CL6	AB161	16-050	with EC733814
B2L2S08	–SERVICE IN	C111FG2	FC111	13-240	w/o EC733814
			FC111	13-480	w/o EC733814
B2L2S09	+CTI BIT 4 SERVICE IN	FC161GH2	FC131	13-480	
B2L2S10	+IF BUS OUT 7 CHAN A	FC061DD9	FC071	15-030	w/o EC733814
B2L2S12	+IF BUS OUT P CHAN A	FC061DD1	FC071	15-030	w/o EC733814
B2L2U02	–COMMAND OUT A B CE	FC151AM2	AB171	13-100	with EC733814
			FC151	13-290	with EC733814
			FC151	13-330	with EC733814
			FC151	15-030	with EC733814
B2L2U04	+IF BUS OUT 5 CHAN A	FC061DD7	FC071	15-030	w/o EC733814
B2L2U05	–SERVICE RESPONSE	FC111GM2	FC111	15-030	w/o EC733814
B2L2U06	–OVRUN OR ONES OR RD BFR BRCH	FC091GK4	AB161	13-480	with EC733814
B2L2U06	+SERVICE IN	FC111FG6	FC111	13-170	w/o EC733814
			FC111	15-030	w/o EC733814
B2L2U07	+DATA IN	BS041GJ6	FC111	13-480	w/o EC733814
			FC111	15-030	w/o EC733814
B2L2U09	–STOP STAT TO DF	FC111GF2	FC111	13-470	w/o EC733814
			FC111	16-170	w/o EC733814
B2L2U11	–CTI BIT 7 OP IN	FC161GM2	FC111	15-030	w/o EC733814
			FC101	15-040	w/o EC733814
B2L2U12	+SERVICE IN FOR DATA	BS041GG4	FC111	13-480	w/o EC733814
			FC111	15-040	w/o EC733814
			FC111	17-370	w/o EC733814
B2L2U13	–DATA OUT OR SVC RESP	BS091CF2	FC111	15-030	w/o EC733814
B2M2B05	–BUS OUT BIT 0	FC081GC2	FC081	16-040	with EC733814
			FC081	17-010	with EC733814
B2M2B07	–BUS OUT BIT 2	FC081GE2	FC081	16-040	with EC733814
			FC081	17-010	with EC733814
B2M2B07	+MACH RESET	FC141GF2	FC141	13-010	w/o EC733814
B2M2B09	–BUS OUT BIT 3	FC081GG2	FC081	17-010	with EC733814
B2M2B12	+SERVICE OUT CH A B CE	FC151CF6	FC141	13-320	w/o EC733814
			FC111	15-030	with EC733814
B2M2B13	+BUS OUT BIT 7 TO ALU1	AB451FM6	FC101	15-040	with EC733814
B2M2D06	–BUS OUT BIT 1	FC081FD2	AB451	13-320	with EC733814
			FC081	16-040	with EC733814
B2M2D07	+COMMAND OUT CH A GATED	FC021FE2	FC081	17-010	with EC733814
B2M2D09	+CE SERVICE OUT TAG	PK081FL6	FC151	15-040	w/o EC733814
B2M2D10	+CE COMMAND OUT TAG	PK081FJ6	FC151	13-110	w/o EC733814
			FC151	13-100	w/o EC733814
B2M2D12	+IF BUS OUT 4 CHAN A	FC061DD6	FC151	15-040	w/o EC733814
B2M2D13	+DATA SERVICE ACTIVE	FC111CH2	FC071	15-030	with EC733814
			FC151	13-100	w/o EC733814
B2M2G03	+IF BUS OUT 6 CHAN A	FC061DD8	FC151	17-370	w/o EC733814
B2M2G03	+SERVICE OUT CHAN A B CE	FC151CF6	FC071	15-030	with EC733814
			FC151	13-100	w/o EC733814
			FC151	13-280	w/o EC733814
			FC151	13-350	w/o EC733814
			FC151	17-370	w/o EC733814
B2M2G04	–BUS OUT BIT 6	FC081GL2	FC081	16-040	with EC733814
			FC081	17-010	with EC733814
B2M2G04	–OPERATIONAL IN	FC141GK6	FC141	13-210	w/o EC733814
			FC141	13-250	w/o EC733814
B2M2G05	–BUS OUT BIT 7	FC081GN2	FC081	16-040	with EC733814
			FC081	17-010	with EC733814
B2M2G05	+POWER ON RESET	FC141FF2	FC141	13-010	w/o EC733814
B2M2G08	+BUS OUT BIT 7 CHAN B	XM071GN2	FC081	17-010	with EC733814
B2M2G09	+COMMAND OUT OR HIO	FC151EN4	FC111	15-040	with EC733814
B2M2G10	–BUS OUT BIT 4	FC081FH2	FC081	16-040	with EC733814
			FC081	17-010	with EC733814
B2M2G11	–GATE TRAP PULSE	AB031GA6	FC141	13-010	w/o EC733814
B2M2G12	+BUS OUT PARITY ODD CHAN A	FC091GC2	FC151	15-030	w/o EC733814
B2M2G13	+BUS OUT BIT 3 CHAN B	XM071GG2	FC081	17-010	with EC733814
B2M2J02	–BUS OUT BIT 5	FC081GJ2	FC081	16-040	with EC733814
			FC081	17-010	with EC733814

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
B2M2J03	–POWER RESET	FC271FF4	FC141	13-010	w/o EC733814
B2M2J03	+BUS OUT 1 CHAN B	XM071FD2	FC081	17-010	with EC733814
B2M2J04	+BUS OUT 0 CHAN B	XM071GC2	FC081	17-010	with EC733814
B2M2J06	+BUS OUT 6 CHAN B	XM071GL2	FC081	17-010	with EC733814
B2M2J10	+COMMAND OUT CH B GATED	XM021FE2	FC151	15-040	w/o EC733814
B2M2J11	+BUS OUT P CHAN B	XM071GA2	FC081	17-010	with EC733814
B2M2J12	+BUS OUT 4 CHAN B	XM071FH2	FC081	17-010	with EC733814
B2M2J12	+BUS OUT PARITY ODD CHAN B	XM081GC2	FC151	15-030	w/o EC733814
B2M2M03	+BUS OUT BIT 5 CHANNEL B	XM071GJ2	FC081	17-010	with EC733814
B2M2M04	–BUS OUT BIT P	FC081GA2	FC081	16-040	with EC733814
			FC081	17-010	with EC733814
B2M2M05	+IF BUS OUT 1 CHAN A	FC061DD3	FC071	15-030	with EC733814
B2M2M08	–HARDWARE ERROR ALU1	AA451GA6	FC141	13-010	w/o EC733814
B2M2M08	+ST BIT 0 ALU1 STOP SERV	AB141GE2	FC111	13-480	with EC733814
B2M2M09	+IF BUS OUT 3 CHAN A	FC061DD5	FC071	15-030	with EC733814
B2M2M10	+BUS OUT PARITY ODD	FC151DD6	FC111	15-030	with EC733814
B2M2M11	+BRANCH CONDITION MET ALU1	AB151GG6	AB151	13-090	w/o EC733814
			AB151	13-280	w/o EC733814
			AB151	17-370	w/o EC733814
B2M2M12	+BUS PARITY OK	FC111GB6	FC111	15-030	with EC733814
B2M2M13	+IF BUS OUT 0 CHAN A	FC061DD2	FC071	15-030	with EC733814
B2M2P05	+BUS OUT 2 CHAN B	XM071GE2	FC081	17-010	with EC733814
B2M2P09	–RESET ALU1 IC	FC141GB6	FC141	13-380	w/o EC733814
B2M2P12	+RESET ALU1 IC	FC141GB2	FC141	13-010	w/o EC733814
			FC141	13-380	w/o EC733814
B2M2S02	+DATA SERVICE ACTIVE	FC111CH2	FC111	13-280	with EC733814
B2M2S02	–SUPPRESS OUT A B	FC151AD2	FC151	13-310	w/o EC733814
			FC151	13-340	w/o EC733814
B2M2S03	+ROS REG 6 ALU1	AB071CL2	AB171	16-050	w/o EC733814
B2M2S04	+IF BUS OUT 2 CHAN A	FC061DD4	FC071	15-030	with EC733814
B2M2S05	–ADDRESS OUT A B CE	AB171CB2	FC141	13-300	w/o EC733814
			FC151	13-360	w/o EC733814
B2M2S07	–STAT BIT 0 TAPE OP TO ALU1	AA141GD6	FC111	13-100	with EC733814
			FC111	13-480	with EC733814
			FC111	15-030	with EC733814
B2M2S07	–ROS REG 6 ALU1	AB071CL6	AB161	16-050	w/o EC733814
B2M2S08	–SERVICE IN	FC111FG2	FC111	13-240	with EC733814
			FC111	13-480	with EC733814
B2M2S09	+CTI BIT 4 SERVICE IN	FC161GH2	FC131	13-480	w/o EC733814
B2M2S10	+IF BUS OUT 7 CHAN A	FC061DD9	FC071	15-030	with EC733814
B2M2S12	+IF BUS OUT P CHAN A	FC061DD1	FC071	15-030	with EC733814
B2M2U02	–COMMAND OUT A B CE	FC151AM2	AB171	13-100	w/o EC733814
			FC151	13-290	w/o EC733814
			FC151	13-330	w/o EC733814
			FC151	15-030	w/o EC733814
B2M2U04	+IF BUS OUT 5 CHAN A	FC061DD7	FC071	15-030	with EC733814
B2M2U05	–SERVICE RESPONSE	FC111GM2	FC111	15-030	with EC733814
B2M2U06	–OVRUN OR ONES OR RD BFR BRCH	FC091GK4	AB161	13-480	w/o EC733814
B2M2U06	+SERVICE IN	FC111FG6	FC111	13-170	with EC733814
			FC111	15-030	with EC733814
B2M2U07	+DATA IN	BS041GJ6	FC111	13-480	with EC733814
			FC111	15-030	with EC733814
B2M2U09	–STOP STAT TO DF	FC111GF2	FC111	13-470	with EC733814
			FC111	16-170	with EC733814
B2M2U11	–CTI BIT 7 OP IN	FC161GM2	FC111	15-030	with EC733814
			FC101	15-040	with EC733814
B2M2U12	–SERVICE IN FOR DATA	BS041GG4	FC111	13-480	with EC733814
			FC111	15-040	with EC733814
B2M2U13	–DATA OUT OR SVC RESP	BS091CF2	FC111	15-030	with EC733814
B2N2B13	+IF BUS OUT 3 CHAN B	XM055BK5	XM061	15-030	
B2N2D04	+IF BUS OUT 4 CHAN B	XM055BK6	XM061	15-030	
B2N2G12	+IF BUS OUT 2 CHAN B	XM055BK4	XM061	15-030	
B2N2J09	+IF BUS OUT 0 CHAN B	XM055BK2	XM061	15-030	
B2N2P11	+IF BUS OUT 7 CHAN B	XM055BK9	XM061	15-030	
B2N2S07	+IF BUS OUT 1 CHAN B	XM055BK3	XM061	15-030	

3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
B2N2S08	+IF BUS OUT 6 CHAN B	XM055BK8	XM061	15-030	
B2N2U06	+IF BUS OUT P CHAN B	XM055BK1	XM061	15-030	
B2N2U07	+IF BUS OUT 5 CHAN B	XM055BK7	XM061	15-030	
B2N2U12	+SERVICE IN FOR DATA	BS041GG4	FC111	17-370	with EC733814
B2P2D03	+SUPPRESS OUT CHAN B GATED	XM011GE2	XM011	13-310	
B2P2D04	+IF SUP OUT CHAN B	XM055BG3	XM011	13-220	
B2P2D11	+SERVICE OUT CHAN B GATED	XM021GF2	XM021	13-100	
			XM021	13-280	
B2P2D12	+COMMAND OUT CHAN B GATED	XM021FE2	XM021	13-100	
			XM021	13-290	
B2P2D13	+ADDR OUT CHAN B GATED	XM011GC2	XM011	13-300	
B2P2G02	–REQUEST IN CHAN B	XM051FN6	XM051	13-220	
B2P2G03	–SELECT SIGNAL CHAN	XM011GH6	XM011	13-210	
			XM011	13-250	
B2P2J03	+IF ADR OUT CHAN B	XM055BG2	XM011	15-050	
B2P2S08	+IF SELECT SIG CHAN B	XM171BJ2	XM171	13-250	w/o EC733814
B2P2S08	+5.12 MHZ	BS011EH6	XM021	13-250	with EC733814
B2P2S10	+GENERAL RESET CHAN B	XM041FF6	XM041	13-050	
B2P2U13	+CUE PENDING CHAN B	XM031GK2	XM031	13-500	
B2Q2D03	+SUPPRESS OUT CHAN X GATED	FC011GE2	FC011	13-310	
B2Q2D04	+IF SUP OUT CHAN A	FC061DA3	FC011	13-220	
B2Q2D09	+IF CMND CHAN A	FC061DA4	FC011	15-050	
B2Q2D11	+SERVICE OUT CHAN A GATED	FC021GF2	FC021	13-100	
			FC021	13-280	
B2Q2D12	+COMMAND OUT CHAN A GATED	FC021FE2	FC021	13-100	
			FC021	13-290	
B2Q2D13	+ADDR OUT CHAN X GATED	FC011GC2	FC011	13-300	
B2Q2G02	–REQUEST IN CHAN A	FC051FN6	FC051	13-220	
B2Q2G03	–SELECT SIG CHAN	FC011GH6	FC021	13-210	
			FC011	13-250	
B2Q2S10	+GENERAL RESET CHAN A-B	FC041FF6	FC041	13-050	
			FC041	16-000	
B2Q2U13	+CUE PENDING CHAN A	FC031GK2	FC031	13-200	
B2R2B03	+INTF REQUEST IN CHAN	FC221EH6	FC221	13-220	w/o EC733814
B2R2P09	+SELECT TO RCVRS OR BYPASS	FC281EC4	FC281	13-250	w/o EC733814
B2R2P09	+SELECT TO RCVRS OR BYPASS	XM181EC4	XM171	13-210	with EC733814
			XM171	13-250	with EC733814
B2R2S08	+SELECT OUT TO LINE RCVR	FC271BJ2	FC271	13-210	w/o EC733814
			FC271	13-250	w/o EC733814
B2R2S08	+IF SELECT SIG CHAN B	XM171BJ2	XM171	13-210	with EC733814
			XM171	13-250	with EC733814
B2S2B03	+INTF REQUEST IN CHAN	FC221EH6	FC221	13-220	with EC733814
B2S2B03	+INTF REQUEST IN CHAN	XM121EH6	XM121	13-220	w/o EC733814
B2S2P09	+SELECT TO RCVRS OR BYPASS	FC281EC4	FC281	13-250	with EC733814
B2S2P09	+SELECT TO RCVRS OR BYPASS	XM181EC4	XM171	13-210	w/o EC733814
			XM171	13-250	w/o EC733814
B2S2S08	+SELECT OUT TO LINE RCVR	FC271BJ2	FC271	13-210	with EC733814
			FC271	13-250	with EC733814
B2S2S08	+IF SELECT SIG CHAN B	XM171BJ2	XM171	13-210	w/o EC733814
			XM171	13-250	w/o EC733814
T-A1B2B03	–REEL STAB	FT311FC6	FT454	3B-110	
			FT454	3B-160	
			FT454	3B-180	
T-A1B2B04	+TAPE BREAK	FT284EB2	FT454	2A-110	
			FT454	2A-160	
			FT454	2B-110	
			FT454	2B-160	
T-A1B2B05	+REEL STAB OR RST REEL FST	FT311FG6	FT452	2A-170	
			FT452	2B-170	
			FT453	3A-170	
			FT453	3B-110	
			FT452	3B-110	
			FT452	3B-170	
T-A1B2D04	+LEFT REEL LOAD OR UNLOAD	FT285FA4	FT452	2B-110	
			FT452	2B-180	
			FT452	3B-110	
T-A1B2D06	+RIGHT REEL UNLOAD	FT265GF2	FT453	2A-120	
			FT453	2A-170	
			FT453	2B-120	
			FT453	3A-110	
			FT453	3B-110	
			FT453	4A-110	
			FT453	4A-120	
			FT453	4A-130	
			FT453	4B-110	
			FT453	4B-120	
			FT453	4B-130	
T-A1B2D10	–GO BACKWARD	FT331EH6	FT453	2B-110	
			FT453	2B-120	
T-A1B2D10	–GO BACKWARD	FT391DH6	FT452	2A-110	
			FT452	2A-120	
			FT452	2A-170	
T-A1B2G04	+UNOPENED CART	FT281BK2	FT453	2A-120	
			FT453	2B-120	
T-A1B2G05	+UNLOAD OP	FT265FL2	FT452	2A-110	
			FT452	2A-120	
			FT452	2B-110	
			FT452	4A-110	
			FT452	4A-120	
			FT452	4A-130	
			FT452	4B-110	
			FT452	4B-120	
			FT452	4B-130	
T-A1B2G08	+EARLY MANUAL STA	FT264FG6	FT452	2A-110	
			FT452	2A-120	
			FT452	2A-160	
			FT452	2A-170	
			FT452	2B-110	
			FT452	2B-120	
			FT453	2B-160	
			FT452	2B-170	
			FT452	3A-110	
			FT452	3B-110	
T-A1B2J02	+LEFT REEL UNLOAD STOP	FT265FH2	FT452	2A-110	
			FT452	2A-170	
			FT452	2B-110	
			FT452	3A-110	
			FT452	3B-110	
T-A1B2J06	+RIGHT REEL THREAD LOAD	FT285CJ2	FT453	2A-120	
			FT453	2A-170	
			FT453	2B-120	
			FT453	3A-110	
			FT453	3B-110	
T-A1B2J09	–16 CNT PULSE	FT302EH2	FT452	2B-170	
			FT452	3B-110	
			FT452	3B-170	
T-A1B2J09	–16 COUNT PULSE	FT354FJ2	FT452	2A-170	
			FT452	3A-110	
T-A1B2J10	+LEFT REEL LOAD OR UNLOAD	FT285FA4	FT452	2A-110	
			FT452	2A-170	
			FT452	3A-110	
T-A1B2J13	+INHIBIT REEL STOP	FT331EF2	FT454	3B-110	
T-A1B2J13	+INHIBIT REEL STOP	FT391GM2	FT454	3A-110	
T-A1B2M02	–RIGHT REEL DRIVE A	FT454GM4	FT454	2A-120	
T-A1B2M02	–RIGHT REEL DRIVE A	FT454GM4	FT454	2B-120	
T-A1B2M03	+RIGHT REEL DRIVE C	FT454GK4	FT454	2A-120	
T-A1B2M04	+LEFT REEL THRD OR TAKE UP	FT285EA4	FT452	2A-110	
			FT452	2A-160	
			FT452	2A-170	
			FT452	2B-110	
			FT452	2B-160	
			FT452	2B-180	
			FT452	3B-110	
			FT452	3B-110	

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3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
T-A1B2M05	–RIGHT REEL DRIVE B	FT454GJ4	FT454	2A-120	
T-A1B2M05	–RIGHT REEL DRIVE B	FT454GJ4	FT454	2B-120	
T-A1B2M08	–LEFT REEL DRIVE A	FT454GD4	FT454	2A-110	
			FT454	2B-110	
T-A1B2M09	+LEFT REEL DRIVE C	FT454GB4	FT454	2A-110	
			FT454	2B-110	
T-A1B2M12	–LEFT REEL DRIVE B	FT454GA4	FT454	2A-110	
			FT454	2B-110	
T-A1B2M13	+LEFT REEL DRIVE D	FT454GC4	FT454	2A-110	
			FT454	2B-110	
T-A1B2P02	–GO FORWARD	FT331EG6	FT453	2B-120	
T-A1B2P07	+RIGHT REEL DRIVE D	FT454GL4	FT454	2A-120	
			FT454	2B-120	
T-A1B2P09	+STOP RIGHT REEL UNLOAD	FT283FJ2	FT453	2A-170	
			FT453	2B-120	
			FT453	3A-110	
			FT453	3B-110	
T-A1B2S02	+SWITCH L-1	WB021AG1	FT451	2A-170	
			FT451	3A-110	
			FT451	3A-160	
			FT451	3A-170	
			FT451	3B-110	
			FT451	3B-160	
			FT451	3B-170	
			FT451	4A-120	
			FT451	4B-120	
T-A1B2S03	+SWITCH L-2	WB021AG2	FT451	2A-170	
			FT451	2B-170	
			FT451	2B-175	
			FT451	2B-180	
			FT451	3A-110	
			FT451	3B-110	
T-A1B2S08	+SWITCH R-1	WB021AG5	FT451	2A-170	
			FT451	2B-170	
			FT451	2B-175	
			FT451	3A-110	
			FT451	3B-110	
T-A1B2S09	+SWITCH R-3	WB021AG7	FT451	2A-170	
			FT451	3A-110	
			FT451	3A-160	
			FT451	3A-170	
			FT451	3B-110	
			FT451	3B-160	
			FT451	3B-170	
T-A1B2U04	+SWITCH L-3	WB021AG3	FT451	2A-110	
			FT451	2A-170	
			FT451	2B-110	
			FT451	2B-170	
			FT451	3A-110	
			FT451	3B-110	
T-A1B2U06	+RIGHT REEL SQUARING CKT	FT231GB6	FT453	3A-170	
			FT453	3B-110	
			FT453	3B-170	
T-A1B2U07	+LEFT REEL SQUARING CKT	FT231GA6	FT452	3A-170	
			FT452	3B-110	
			FT452	3B-170	
T-A1B2U09	+SWITCH R-2	WB021AG6	FT451	2A-120	
			FT451	2A-170	
			FT451	2B-120	
			FT451	2B-170	
			FT451	3A-110	
			FT451	3B-110	
T-A1B2U12	+HSFL	FT262GB4	FT455	2A-110	
			FT455	2A-170	
			FT455	2B-110	
			FT455	3A-110	
			FT455	3B-110	

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
T-A1B2U13	+STEP DOWN	FT261EC6	FT455	2A-110	
			FT455	2A-170	
			FT455	2B-110	
			FT455	3A-110	
			FT455	3A-160	
			FT455	3A-170	
			FT455	3B-110	
			FT455	3B-160	
			FT455	3B-170	
			FT455	3B-180	
T-A1C2B02	+GATED OVERFLOW	FT322GC2	FT261	3B-180	
T-A1C2B05	–SET REWIND COMMAND	FT134CK2	FT261	16-160	
			FT261	16-210	
			FT261	3B-100	
			FT261	3B-100	
			FT261	3B-170	
T-A1C2B07	+SAFETY BAIL RESET	FT283BA2	FT266	2A-100	
T-A1C2B07	+RESET SAFETY BL/ERASE UK	FT182CM6			
			FT266	2A-110	
			FT266	2B-100	
			FT266	2B-110	
			FT266	2B-210	
			FT266	3B-100	
T-A1C2B09	+POWER ON RESET	FT112BF6	FT266	2A-100	
			FT266	2A-110	
			FT266	2B-100	
			FT266	2B-110	
T-A1C2B3	+REEL REVOLUTION PULSES	FT23IGD4	FT261	3A-170	
T-A1C2B13	+REEL REV PULSE OR LP STAT	FT323FK2	FT261	3B-170	
			FT261	3B-180	
T-A1C2D04	–MECH READY	FT114GB4	FT262	2A-100	
			FT262	2A-110	
			FT262	2B-100	
			FT262	2B-110	
			FT262	3B-170	
T-A1C2D05	–GATED LOAD PB	FT262DM6	FT261	16-160	
T-A1C2D06	+SET REWIND UNLOAD COMMAND	FT134BJ2	FT261	16-210	
			FT261	3A-100	
T-A1C2D13	–LOAD POINT STATUS	FT391CC6	FT265	2A-210	
			FT265	3A-170	
			FT265	4A-110	
			FT265	4A-120	
T-A1C2D13	+LP STATUS DELAYED	FT323FE6	FT265	2B-175	
			FT265	2B-210	
			FT265	3B-170	
			FT265	4B-110	
			FT265	4B-120	
T-A1C2G02	+LEFT REEL FAST	FT452DD2	FT262	3A-170	
			FT262	3B-170	
T-A1C2G05	+RIGHT REEL FAST	FT453DD2	FT262	3A-170	
			FT262	3B-170	
T-A1C2G08	–MANUAL STATUS CONT	WB022AK4	FT265	2A-170	
			FT265	2B-175	
			FT265	3A-110	
			FT265	3B-110	
			FT265	4A-110	
			FT265	4A-120	
			FT265	4B-110	
			FT265	4B-120	
T-A1C2G10	–READY LAMP	FT261GK4	FT261	2A-210	
			FT261	2B-210	
			FT261	4A-100	
			FT261	4B-100	

3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
T-A1C2G13	–PICK REEL CONT.	FT265FA4	FT265	2A-111	
			FT265	2A-170	
			FT265	2B-110	
			FT265	2B-175	
			FT265	3A-110	
			FT231	3B-110	
			FT265	3B-110	
			FT265	4A-110	
			FT265	4A-120	
			FT265	4B-110	
			FT265	4B-120	
T-A1C2J02	–UNLOAD DELAY	FT302BD6	FT265	2B-110	
			FT265	4A-110	
			FT265	4B-110	
T-A1C2J04	+SET UNLOAD LATCH	FT284BL2	FT265	2A-110	
			FT265	2B-110	
T-A1C2J05	+LOAD REWIND	FT282AL2	FT261	16-160	
			FT261	2A-170	
			FT261	2A-190	
			FT261	2A-210	
			FT261	2B-175	
			FT261	2B-210	
T-A1C2J06	–WINDOW CLOSED	FT283AB6	FT261	2A-210	
			FT261	2B-210	
T-A1C2J13	–GATED READY	FT261CN6	FT261	2B-210	
T-A1C2M02	–HI SPEED FIELD	FT262GJ4	FT262	2A-110	
			FT262	2A-140	
			FT262	2B-110	
			FT262	2B-140	
			FT262	3B-170	
			FT262	3B-170	
T-A1C2M03	+RESET PB	WB021AF4	FT263	2A-100	
			FT263	2A-110	
			FT263	2B-100	
			FT263	2B-110	
			FT263	4A-100	
			FT263	4B-100	
T-A1C2M04	+START PB	WB021AF1	FT263	2A-210	
			FT263	2B-210	
			FT263	4A-100	
			FT263	4B-100	
T-A1C2M05	+HSFL	FT262GB4	FT261	6B-140	
T-A1C2M09	+SWITCH R-4	WB021AG8	FT263	2A-100	
			FT263	2A-110	
			FT263	2A-170	
			FT263	2B-100	
			FT263	2B-110	
			FT263	2B-175	
			FT263	2B-210	
			FT263	3B-170	
			FT263	4A-120	
T-A1C2M12	+LOAD OP	FT284BE2	FT265	2A-170	
			FT265	2B-110	
			FT265	2B-175	
			FT265	4A-110	
			FT265	4B-110	
T-A1C2M13	–OPERATOR INTERVENTION	FT263EK2	FT263	15-090	
T-A1C2P04	+STEP DOWN	FT261EC6	FT261	6B-140	
T-A1C2P05	+UNLOAD PB	WB021AF3	FT263	2A-210	
			FT263	2B-210	
			FT263	4A-110	
			FT263	4B-110	
T-A1C2P06	+DOOR INTERLOCK	WB021AF5	FT263	2A-100	
			FT263	2A-110	
			FT263	2B-100	
			FT263	2B-110	
T-A1C2P07	+LOAD PB	WB021AF2	FT263	2A-100	
			FT263	2A-110	
			FT263	2A-120	
			FT263	2B-100	
			FT263	2B-110	
			FT263	2B-120	
T-A1C2P09	+SWITCH L-4	WB021AG4	FT263	2A-100	
			FT263	2A-110	
			FT263	2A-170	
			FT263	2A-190	
			FT263	2B-100	
			FT263	2B-110	
			FT263	2B-175	
			FT263	2B-210	
			FT263	3B-170	
			FT263	4A-120	
T-A1C2P11	–BELOW L-2	FT451CE2	FT264	2A-170	
			FT264	2B-175	
T-A1C2P13	+CART INTERLOCK	FT266CC2	FT266	4B-110	
T-A1C2S07	+MANUAL STATUS	FT265DE2	FT265	2B-210	
T-A1C2S08	+TAPE PRESENT	FT281BE2	FT266	16-160	
			FT266	4A-130	
			FT266	4A-140	
			FT266	4B-130	
T-A1C2U12	–BELOW R-1	FT451GB2	FT264	2A-170	
			FT264	2B-175	
T-A1D2B02	F/O LAMP SENSE A	WB022AC2	FT231	2A-100	
			FT231	2A-110	
			FT231	2B-100	
			FT231	2B-110	
T-A1D2B07	–EOT SS	FT231GK2	FT231	3A-100	
			FT231	3B-100	
T-A1D2B12	EOT PHOTO TX	WB022AD6	FT231	2A-110	
			FT231	2A-150	
			FT231	2B-110	
			FT231	2B-150	
			FT231	3A-150	
			FT231	3B-150	
			FT231	4A-130	
			FT231	4B-130	
T-A1D2D02	F/O LAMP SENSE B	WB022AC4	FT231	2A-100	
			FT321	2A-110	
			FT231	2B-100	
			FT231	2B-110	
T-A1D2D12	BOT PHOTO TX	WB022AD2	FT231	2A-110	
			FT231	2A-150	
			FT231	2A-160	
			FT231	2A-170	
			FT231	2A-190	
			FT231	2B-110	
			FT231	2B-150	
			FT231	2B-160	
			FT231	4A-130	
			FT231	4B-130	
T-A1D2G10	RADIUS SENSE PHOTO TX	WB022AC6	FT231	2A-120	
			FT231	2B-120	
T-A1D2G12	RIGHT REEL PHOTO TX	WB022AE6	FT231	3B-110	
			FT231	3B-170	
T-A1D2G13	LEFT REEL PHOTO TX	WB022AE2	FT231	3B-110	
			FT231	3B-170	
T-A1D4B02	–WINDOW CLOSED SW	WB022AH2	FT283	2B-210	
T-A1D4B04	+WINDOW DOWN	FT283GB4	FT283	4B-140	
T-A1D4B05	–SAFETY BAIL ACTUATED	WB022AH6	FT283	2B-100	
			FT283	2B-110	
			FT283	2B-210	

3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
T-A1D4B07	+REELS LOADED SWITCH	WB021AJ2	FT284	2B-140	
			FT284	2B-150	
			FT284	4B-130	
			FT284	4B-130	
T-A1D4D04	+CART ON SWITCH	WB021AL1	FT281	2B-100	
T-A1D4D05	+CART OPEN SWITCH	WB021AL2	FT281	2B-100	
			FT281	4B-150	
T-A1D4D06	–PICK CHAN AIR SOL	FT283FN4	FT283	2B-130	
			FT283	2B-160	
			FT283	4B-120	
T-A1D4D13	–COLUMNS LOADED	FT264DD2	FT285	2B-100	
			FT285	2B-110	
			FT285	2B-120	
T-A1D4G05	–IBG 18 CNT NO CTG OR 24 OR 56	FT332GG2	FT284	2B-100	
			FT284	2B-110	
T-A1D4G07	+STOP RIGHT REEL UNLOADED	FT283FJ2	FT282	2B-210	
			FT282	4B-160	
T-A1D4G08	+MANUAL STATUS	FT265DE2	FT281	2B-120	
T-A1D4G09	–TAPE PRESENT A	FT231DL1	FT281	2B-110	
			FT281	2B-160	
			FT281	4B-130	
T-A1D4G12	+LOAD COMPLETE	FT262DH2	FT282	4B-160	
T-A1D4G13	–BOT SS	FT231DJ6	FT284	2B-160	
T-A1D4J02	+REEL HUB AIR PRESSURE SW	WB021AG9	FT285	2B-110	
			FT285	2B-120	
			FT285	4B-140	
T-A1D4J04	–TAPE PRESENT B	FT231EN2	FT281	2B-110	
			FT281	2B-150	
			FT281	2B-160	
			FT281	4B-130	
T-A1D4J05	–IBG 8 BIT	FT332AD5	FT285	2B-120	
T-A1D4J07	+WINDOW UP	FT281FC2	FT281	2B-210	
T-A1D4J09	–PICK AIR SUPPLY CONT	FT282DB4	FT282	2B-130	
			FT282	2B-210	
			FT282	4B-160	
			FT282	08-450	
T-A1D4J10	+MACHINE RESET	FT266AB6	FT281	2B-100	
T-A1D4J11	–BELOW L-1	FT451CA2	FT283	4B-120	
T-A1D4J12	+IBG 72 COUNT	FT332FH2	FT284	2B-110	
			FT284	2B-110	
			FT284	2B-150	
T-A1D4J13	+COLS LOADED	FT264AE2	FT283	2B-100	
			FT283	2B-210	
T-A1D4M03	+AIR BEARING PRESSURE SW	WB021AJ1	FT285	2B-160	
T-A1D4M05	+LOAD COMPLETE	FT262DH2	FT284	2B-100	
T-A1D4M08	+RESET CTG HOLD LATCH	FT311CH2	FT284	2B-100	
			FT284	2B-110	
			FT284	4B-150	
T-A1D4M09	+HALT RIGHT REEL LOAD	FT264AC2	FT285	2B-120	
T-A1D4M10	+HALT LEFT REEL LOAD	FT264BA2	FT285	2B-180	
T-A1D4P06	–LOAD CHECK LAMP	FT285FF4	FT285	2B-150	
T-A1D4P10	+HSRS	FT261DJ2	FT282	2B-160	
T-A1D4P11	–IBG 4 BIT	FT332AD4	FT284	2B-160	
T-A1D4P13	+LP STATUS DELAYED	FT323FE2	FT282	2B-160	
			FT282	2B-175	
			FT282	2B-210	
T-A1D4U06	–GATED LOAD PB	FT262DM6	FT284	2B-100	
			FT284	2B-110	
			FT284	2B-120	
T-A1D4U07	+CART INTERLOCK	FT266CC2	FT282	4B-150	
T-A1D4U13	–DR CTG MOTOR	FT281FH4	FT281	2B-100	
			FT281	4B-150	
T-A1E2B02	–SIGN BIT DAC	FT345GJ2	FT345	6B-000	
			FT345	6B-140	
T-A1E2B02	–WINDOW CLOSED SW	WB022AH2	FT283	2A-210	
T-A1E2B03	+REWIND CURRENT	FT321CH6	FT345	6B-140	

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
T-A1E2B04	+WINDOW DOWN	FT283GB4	FT283	4A-140	
T-A1E2B04	–32 BIT DAC	FT345GG2	FT345	6B-000	
T-A1E2B05	–16 BIT DAC	FT345GE2	FT345	6B-000	
			FT345	6B-140	
T-A1E2B05	–SAFETY BAIL ACTUATED	WB022AH6	FT283	2A-100	
			FT283	2A-110	
T-A1E2B07	+REELS LOADED SWITCH	WB021AJ2	FT284	2A-140	
			FT284	2A-150	
			FT284	2A-160	
			FT284	4A-130	
T-A1E2B12	–4 BIT DAC	FT345GC2	FT345	6B-000	
			FT345	6B-140	
T-A1E2D02	–1 BIT DAC	FT345GA2	FT345	6B-000	
			FT345	6B-100	
T-A1E2D04	+CART ON SWITCH	WB021AL1	FT281	2A-100	
T-A1E2D05	–2 BIT DAC	FT345GB2	FT345	6B-000	
			FT345	6B-100	
			FT345	6B-110	
T-A1E2D05	+CART OPEN SWITCH	WB021AL2	FT281	2A-100	
			FT281	4A-150	
T-A1E2D06	–PICK CHAN AIR SOL	FT283FN4	FT283	2A-130	
			FT283	2A-160	
T-A1E2D06	–16 BIT DAC	FT345GE2	FT345	6B-110	
T-A1E2D11	–8 BIT DAC	FT345GD2	FT345	6B-000	
			FT345	6B-140	
T-A1E2D12	+BLOCK PDC COUNTING	FT343GE6	FT343	6B-100	
			FT343	6B-110	
T-A1E2D13	–COLUMNS LOADED	FT264DD2	FT285	2A-100	
			FT285	2A-110	
			FT285	2A-120	
T-A1E2G05	–9 CNT NO CART 12 OR 28	FT393CN2	FT285	2A-100	
			FT285	2A-110	
T-A1E2G07	+STOP RT REEL UNLOADED	FT283FJ2	FT282	2A-190	
			FT282	2A-210	
			FT282	4A-160	
T-A1E2G09	–TAPE PRESENT A	FT231DL1	FT281	2A-110	
			FT281	2A-160	
			FT281	4A-130	
T-A1E2G12	+LOAD COMPLETE	FT262DH2	FT282	4A-160	
T-A1E2G13	–BOT S.S.	FT231DJ6	FT284	2A-160	
T-A1E2J02	+REEL HUB AIR PRESSURE SW	WB021AG9	FT285	2A-110	
			FT285	2A-120	
			FT285	2A-160	
			FT285	4A-140	
T-A1E2J04	–TAPE PRESENT B	FT231EN2	FT281	2A-110	
			FT281	2A-150	
			FT281	2A-160	
			FT281	4A-130	
T-A1E2J05	–BIT 4A	FT395FH2	FT285	2A-120	
T-A1E2J07	+WINDOW UP	FT281FC2	FT281	2A-210	
T-A1E2J09	–PICK AIR SUPPLY CONT.	FT282DB4	FT282	2A-130	
			FT282	2A-210	
			FT282	4A-120	
			FT282	4A-160	
T-A1E2J10	+MACHINE RESET	FT266AB6	FT281	2A-100	
T-A1E2J11	–BELOW L-1	FT451CA2	FT283	4A-120	
T-A1E2J12	+36 COUNT	FT393AD2	FT284	2A-100	
			FT284	2A-110	
			FT284	2A-150	
T-A1E2J13	+COLS UNLOADED	FT264AE2	FT283	2A-100	
T-A1E2M03	+AIR BEARING PRESSURE SW	WB021AJ1	FT285	2A-160	
			FT285	4A-140	
T-A1E2M05	+LOAD COMPLETE	FT262DH2	FT281	2A-100	
T-A1E2M08	+UNLOAD COMPLETE	FT266BJ2	FT284	2A-100	
			FT284	2A-110	
			FT284	4A-140	

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3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
T-A1E2M09	+HALT RIGHT REEL LOAD	FT264AC2	FT285	2A-110	
			FT285	2A-120	
T-A1E2M10	+HALT LEFT REEL LOAD	FT264BA2	FT285	2A-170	
			FT285	3A-110	
T-A1E2P05	+TAPE BREAK	FT284EB2	FT284	2A-120	
T-A1E2P05	+COMPLEMENT TP	FT341EL2	FT341	6B-110	
T-A1E2P06	-LOAD CHECK LAMP	FT285FF4	FT285	2A-150	
T-A1E2P10	+HSRS	FT261DJ2	FT282	2A-160	
T-A1E2P11	-BIT 2A	FT395CH2	FT284	2A-160	
T-A1E2P13	+LOAD POINT STATUS	FT391CC2	FT282	2A-160	
T-A1E2S09	-PDC 1 BIT	FT342CA4	FT342	6B-100	
T-A1E2S10	-PDC 16 BIT	FT342CH4	FT342	6B-110	
T-A1E2S13	-PDC 32 BIT	FT342CH5	FT344	6B-110	
T-A1E2U06	-GATED LOAD PB	FT262DM6	FT284	2A-100	
			FT284	2A-110	
			FT284	2A-120	
T-A1E2U07	+CART INTERLOCK	FT266CC2	FT282	4A-150	
T-A1E2U10	-PDC 4 BIT	FT342DC4	FT342	6B-100	
T-A1E2U12	-PDC SIGN BIT	FT342DK4	FT342	6B-100	
T-A1E2U13	-DR CTG MOTOR	FT281FH4	FT281	2A-100	
			FT281	4A-150	
T-A1E2U13	-PDC 8 BIT	FT342DC5	FT342	6B-100	
T-A1F2B04	+REEL REVOLUTION PULSES	FT231GD4	FT334	2B-120	
T-A1F2B09	-BOT S.S.	FT231DJ6	FT391	2A-170	
			FT391	2A-190	
			FT391	3A-130	
T-A1F2B13	-GATED REWIND	FT134FG6	FT391	2A-170	
			FT391	2A-190	
			FT391	3A-100	
			FT391	3A-170	
T-A1F2D02	+IBG 68 COUNT	FT332FF2	FT332	6B-100	
T-A1F2D06	+CAPSTAN FAST	FT351GE2	FT392	2A-190	
			FT392	3A-100	
T-A1F2D11	-CAPSTAN GO HI SPEED	FT455GA6	FT392	3A-160	
T-A1F2D12	-GATED READY	FT261CN6	FT392	3A-170	
T-A1F2D13	-MOVE COMMAND	FT134DB2	FT391	3A-100	
			FT391	3A-100	
			FT391	3A-110	
			FT391	3A-140	
			FT391	6A-000	
T-A1F2G04	+THREAD STATUS	FT284EH2	FT391	2A-110	
			FT391	3A-130	
T-A1F2G04	-TO	FT301EE2	FT333	16-160	
T-A1F2G07	+T1	FT301GB2	FT334	3B-100	
T-A1F2G09	-IBG 1 OR 2 BIT	FT332GB2	FT332	6B-110	
T-A1F2G12	+BACKWARD STATUS	FT134EL6	FT391	2A-170	
			FT394	2A-190	
			FT391	2A-200	
			FT391	3A-100	
			FT394	3A-130	
			FT394	3A-170	
T-A1F2J02	-FORWARD DRIVE	FT334FD2	FT334	6B-100	
T-A1F2J04	+MANUAL STATUS	FT265DE2	FT391	2A-170	
			FT391	3A-110	
T-A1F2J05	-COLS LOADED	FT264CB2	FT391	4A-110	
			FT391	4A-120	
T-A1F2J05	-START CURRENT	FT334FB2	FT334	6B-100	
			FT334	6B-100	
T-A1F2J06	+4 CNT HITCH	FT394CC2	FT394	2A-200	
T-A1F2J09	+CAPSTAN COAST	FT455GG4	FT392	3A-160	
T-A1F2J10	+READ WRITE INHIBIT	FT394BL6	FT394	6A-000	
T-A1F2J11	+LO COMP OR STEP DOWN	FT262FG6	FT391	2A-160	
			FT391	2A-170	

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
T-A1F2J11	+EXTENDED GO	FT331GB6	FT331	6B-020	
			FT331	6B-100	
			FT331	6B-100	
T-A1F2J12	-GATE NORMAL RUN	FT331EM6	FT331	6B-110	
T-A1F2J12	+GO INTERNAL	FT391DE6	FT391	5A-000	
			FT391	6A-000	
T-A1F2M02	+SET FWD HITCH REQ	FT311BE2	FT334	2B-200	
T-A1F2M04	+RESET INHIB HITCH	FT354CJ2	FT394	3A-160	
T-A1F2M05	+REEL REVOLUTION PULSES	FT231GD4	FT395	2A-120	
T-A1F2M05	-52 COUNT LATCH	FT333FB2	FT333	6B-110	
T-A1F2M07	+MANUAL STATUS	FT265DE2	FT333	2B-175	
			FT333	3B-110	
			FT334	3B-110	
T-A1F2M08	+COUNTER RESET	FT282AM6	FT334	2B-110	
			FT334	2B-120	
			FT334	2B-160	
T-A1F2M10	+SET IBG COUNTER	FT304EE2	FT334	2B-110	
			FT334	2B-120	
			FT334	2B-160	
T-A1F2M13	-GATED READY	FT261CN6	FT331	3B-100	
T-A1F2P02	-IBG 28 COUNT	FT332DJ6	FT332	6B-100	
T-A1F2P06	+COUNTER RESET	FT282AM6	FT394	2A-120	
T-A1F2P07	+GATED OPP DIRECTION	FT334EH2	FT334	6B-100	
			FT334	6B-100	
T-A1F2P12	-MOVE COMMAND B	FT183GK6	FT331	16-160	
			FT331	3B-100	
			FT331	3B-110	
			FT331	3B-130	
			FT331	3B-140	
			FT331	5B-000	
			FT331	6B-020	
T-A1F2P13	-GO BACKWARD	FT331EH6	FT331	6B-100	
T-A1F2S02	-EXTENDED GO	FT331GB2	FT331	6B-100	
			FT333	6B-100	
T-A1F2S03	-LOAD POINT STATUS	FT342DH6	FT331	3B-130	
T-A1F2S04	+BACKWARD STATUS	FT134EL6	FT334	2B-200	
			FT331	3B-100	
			FT331	3B-100	
			FT331	3B-130	
			FT331	6B-100	
T-A1F2S07	+GO INTERNAL	FT331BB6	FT331	16-160	
			FT331	6B-100	
T-A1F2U02	-GATED REWIND	FT134FG6	FT331	16-160	
			FT331	2B-175	
			FT331	3B-100	
T-A1F2U05	-GO INTERNAL	FT331BB2	FT333	3B-130	
			FT331	3B-140	
			FT331	6B-100	
			FT334	6B-100	
T-A1F2U06	+LD COMP OR STEP DOWN	FT262FG6	FT331	2B-175	
			FT331	2B-190	
T-A1G1E09	+12V	WB021AN1	WB021	5B-100	
T-A1G2B05	-LOAD POINT STATUS	FT324DH6	FT323	2B-160	
T-A1G2B07	+STEP DOWN	FT261EC6	FT321	6B-140	
T-A1G2B11	+6V TEST POINT	FT910	FT910	1B-000	
T-A1G2B13	+GATE NOM STOP DLY TP	FT322BC2	FT322	6B-100	
T-A1G2D02	+MANUAL STATUS	FT265DE2	FT324	3B-130	
T-A1G2D07	+HSFL	FT262GB4	FT321	6B-140	
T-A1G2D09	-OVERFLOW	FT314EM6	FT322	3B-180	
T-A1G2D10	+GATE PHD	FT321GJ2	FT321	3B-170	
			FT321	6B-100	
T-A1G2D11	-ERASE HEAD ON	WB011AF2	FT323	15-090	
			FT323	5B-000	
			FT323	5B-100	

3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
T-A1G2D12	+SAMPLED TPC EQUAL GATED	FT322AF2	FT322	6B-100	
			FT322	6B-110	
T-A1G2G02	–SET NOMINAL STOP CURRENT	FT322EG2	FT322	6B-100	
			FT322	6B-110	
T-A1G2G02	+SQUARING CKT PULSES	FT352AN6	FT352	6A-000	
T-A1G2G03	+SET PHD REG	FT321GL6	FT321	3B-170	
			FT321	6B-100	
T-A1G2G04	+NOT STOP COMPLEMENT	FT322EM2	FT322	6B-110	
T-A1G2G07	+LOW REWIND CURRENT	FT321GE2	FT321	3B-160	
			FT321	3B-170	
T-A1G2G10	–CAPSTAN GO HI SPEED	FT455GA6	FT321	3B-160	
			FT321	3B-170	
			FT321	3B-180	
T-A1G2G12	–GATE STOPLOCK CTR	FT321BG2	FT321	6B-110	
T-A1G2G13	+INCR PDC	FT324AD2	FT324	6B-100	
			FT324	6B-110	
T-A1G2J02	–PDC INPUT	FT324FF6	FT324	6B-100	
T-A1G2J04	+CAPSTAN COAST	FT455GG4	FT321	3B-160	
			FT321	3B-170	
T-A1G2J05	–SET PDC	FT324GK2	FT324	6B-100	
T-A1G2J10	–STOP	FT321DA2	FT321	2B-190	
			FT321	6B-100	
T-A1G2M02	+REWIND CURRENT	FT321CH6	FT321	3B-160	
			FT321	6B-140	
T-A1G2M02	+HI POWER DRIVE	FT391EL2	FT351	4A-110	
T-A1G2M04	+1/4 TACH STOP SYNC	FT322BH2	FT322	6B-100	
			FT322	6B-110	
T-A1G2M05	–GATE PDC	FT324DL2	FT324	6B-100	
			FT324	6B-110	
T-A1G2M07	+EXTENDED GO	FT331GB6	FT322	2B-190	
T-A1G2M13	–BACKWARD STATUS	FT334BD2	FT324	3B-130	
T-A1G2P04	+STOPLOCK	FT321BE2	FT321	6B-100	
T-A1G2P05	+CAPSTAN FAST	FT352GE2	FT351	6A-000	
T-A1G2P09	+768 MS	FT311BD2	FT323	2B-210	
			FT323	4B-110	
T-A1G2P10	–PICK SOLENOID	FT323GD4	FT323	5B-000	
T-A1G2P13	+IBG 28 AND STOP	FT322BA2	FT322	6B-110	
T-A1G2S02	–BOT S-S	FT231DJ6	FT324	2B-190	
			FT324	3B-130	
T-A1G2S03	+LD COMP OR STEP DOWN	FT262FG6	FT324	2B-160	
			FT324	4B-110	
T-A1G2S04	–GATED ERASE CURRENT	FT323FH2	FT323	15-090	
T-A1G2S07	+GO INTERNAL	FT391DE6	FT351	4A-110	
T-A1G2S08	+STOP 1 DELAY	FT322CB2	FT321	6B-110	
T-A1G2S13	+CTRL CTR RESET 64-256	FT352DE6	FT351	4A-110	
T-A1G2U05	+REEL REVOLUTION PULSES	FT231GD4	FT323	3B-180	
T-A1G2U13	+RESET TPC	FT322FF6	FT322	6B-100	
			FT322	6B-110	
T-A1G6B09	+STOP LOCK	FT321BE2	FT311	2B-170	
T-A1G6B13	–SAMPLED TPC EQUAL	FT314FH6	FT314	6B-100	
T-A1G6D02	+2 KHZ OSC	FT302EL2	FT311	2B-170	
T-A1G6J05	+UNLOAD COMPLETE	FT266BJ2	FT311	2B-100	
			FT311	2B-110	
T-A1G6J13	+SET FWD HITCH REQ	FT311BE2	FT311	6B-100	
T-A1H1B09	GROUND	FT910AE4	FT910	5B-100	
T-A1H1C09	–4V TEST POINT	FT910AA4	FT910	1B-000	
			FT910	5B-100	
T-A1H2B02	–OPPOSITE DIRECTION	FT303FJ2	FT303	6B-100	
			FT303	6B-110	
T-A1H2B05	+STATUS BUS 0	FT113DA2	FT113	15-090	Mod 3,5,7
T-A1H2B13	+STOPLOCK NOT HITCH ACTIVE	FT304DL2	FT304	6B-100	
T-A1H2D02	+AT5	FT303EA2	FT302	6B-100	
T-A1H2D04	+2 KHZ OSC	FT302EL2	FT302	6B-100	
T-A1H2D13	+PHASE B GATED	FT303DK6	FT303	16-170	
			FT303	6B-020	
T-A1H2G05	–WRITE CURRENT ON	WB011AD6	FT111	15-090	Mod 3,5,7
			FT111	2A-100	
			FT111	2A-110	
T-A1H2G09	–PHASE A TP	FT303BK2	FT303	6B-020	
			FT303	6B-100	
			FT303	6B-100	
T-A1H2J04	–TRANSITION T1 - T4	FT303GD2	FT303	6B-100	
T-A1H2J06	+TAPE BOTTOMED	FT264GL2	FT114	2A-100	
			FT114	2A-110	
T-A1H2J06	–GATE NORMAL RUN	FT331EM6	FT303	2B-170	
			FT303	3B-110	
			FT303	3B-110	
T-A1H2J09	+NORMAL RUN PULSE	FT303FB2	FT303	6B-100	
T-A1H2M05	+SET STOP LOCK	FT304GG2	FT304	6B-100	
T-A1H2M09	–WRITE STATUS DRIVE	FT111DA6	FT111	15-090	Mod 3,5,7
			FT111	5A-000	
			FT111	5A-100	
T-A1H2M09	+SET ERROR HITCH	FT304FG2	FT304	6B-100	
T-A1H2M10	+LONG STOP RESPONSE	FT304DF6	FT304	16-160	
			FT304	16-210	
T-A1H2M10	+NFP-1 PICKED	WB021AN1	FT111	5A-000	Mod 3,5,7
			FT111	5A-100	
T-A1H2M12	–BKWD CAPS MOTION	FT303BB6	FT303	6B-100	
T-A1H2M13	+POWER ON RESET	FT182BF6	FT301	3B-100	
T-A1H2P04	+POWER ON RESET	WB022BK4	FT112	2A-100	
			FT112	2A-110	
T-A1H2P05	+AIR PRESSURE FAIL	FT285CL2	FT114	2A-110	
T-A1H2P05	–16 CNT PULSE	FT302EH2	FT302	6B-100	
T-A1H2P10	+WRITE CURRENT U.K.	FT111FJ2	FT111	15-090	Mod 3,5,7
T-A1H2P12	–BUS OUT 5	FT102GA2	FT112	15-090	Mod 3,5,7
T-A1H2P12	–NORMAL RUN PULSE	FT303FB6	FT303	6B-100	
T-A1H2P13	–ERASE HEAD ON	WB011AD2	FT111	15-090	Mod 3,5,7
			FT111	2A-100	
			FT111	2A-110	
T-A1H2S07	+LAMP OFF	FT231CF6	FT114	15-090	Mod 3,5,7
			FT114	2A-100	
			FT114	2A-110	
T-A1H2S07	–T0	FT301EE2	FT301	6B-100	
T-A1H2S09	–FILE PROTECT LAMP	FT111DK4	FT111	5A-100	
T-A1H2S09	–T2	FT301EE4	FT301	6B-100	
T-A1H2S10	–T3	FT301EE5	FT301	6B-100	
			FT301	6B-110	
T-A1H2S12	–T4	FT301EE6	FT301	6B-100	
			FT301	6B-100	
T-A1H2U02	–MOD 8	FT145FK4	FT301	3B-100	
T-A1H2U05	+T1	FT301GB2	FT301	6B-100	
			FT301	6B-110	
T-A1H2U06	+LOAD CHECK	FT285EC2	FT114	15-090	Mod 3,5,7
T-A1H2U13	+T5	FT301GG2	FT301	6B-100	
			FT301	6B-100	
			FT301	6B-110	
T-A1J1B09	–12 V	ZT051TB1	ZT051	5B-100	
T-A1J2B02	–EOT STATUS	FT135FE6	FT135	3A-100	
			FT135	3B-100	
			FT135	5A-100	
T-A1J2B03	–EOT LAMP	FT135GB4	FT135	3A-150	
			FT135	3B-150	
T-A1J2B07	–SELECT PE	FT133GM2	FT133	5A-100	
T-A1J2B09	–MOVE TAG	FT102GL2	FT131	16-170	
			FT134	3A-100	
			FT131	3A-110	
			FT134	3A-140	
			FT134	3B-100	
			FT131	3B-110	
			FT131	3B-140	

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CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
T-A1J2B10	+CONTROL TAG	FT102GG6	FT134	2A-190	
			FT131	2B-175	
			FT131	3A-100	
			FT134	3B-100	
			FT134	3B-170	
T-A1J2D02	–HI CURRENT	FT132FM2	FT132	5A-100	
T-A1J2D06	–EOT S.S.	FT231GK2	FT135	3A-150	
			FT135	3B-150	
T-A1J2D09	+REWIND OP	FT261FF2	FT134	16-160	
			FT134	2A-170	
			FT134	2A-190	
			FT134	2B-175	
			FT134	3A-100	
			FT134	3A-170	
			FT134	3B-100	
T-A1J2D11	–BUS OUT 0	FT101GC2	FT133	16-160	
			FT133	16-210	
			FT134	3A-100	
			FT133	3B-100	
			FT133	3B-130	
			FT131	5A-100	
			FT131	5B-100	
T-A1J2G02	–NRZI DATA TRACK P	FT603EE0	FT133	5A-100	
T-A1J2G03	+WRITE SELECT	FT132CG2	FT132	5A-100	
T-A1J2G04	–BUS OUT 1	FT101GE2	FT133	16-160	
			FT134	16-210	
			FT131	3B-130	
			FT133	5A-100	Mod 3,5,7
			FT131	5B-100	
T-A1J2G05	–BUS OUT P	FT101GA2	FT133	5A-100	
			FT131	5B-100	
T-A1J2G07	+READ GATE	FT134CB6	FT134	5A-100	
T-A1J2G12	–WRITE DATA 3	FT132EE2	FT133	5B-100	
				5A-100	
T-A1J2G13	–WRITE DATA 0	FT132GB2	FT133	5B-100	
				5A-100	
T-A1J2J02	–NRZI DATA TRACK 1	FT601EA0	FT133	5A-100	
T-A1J2J04	–TIE DOWN MOD LINE	FT182CF4	FT132	5B-100	
T-A1J2J04	+NRZI L1	FT604DC6	FT132	5A-100	
T-A1J2J05	–NRZI DATA TRACK 0	FT603EJ0	FT133	5A-100	
T-A1J2J10	–COMMAND TAG	FT102GJ2	FT134	3A-100	
			FT134	3A-130	
			FT131	3B-100	
			FT131	3B-130	
T-A1J2J11	–WRITE DATA 1	FT132EC2	FT133	5B-100	
				5A-100	
T-A1J2J12	–WRITE DATA 2	FT132GD2	FT133	5B-100	
				5A-100	
T-A1J2M04	–BUS OUT 2	FT101GG2	FT133	16-160	
			FT134	16-210	
			FT133	5A-100	
			FT131	5B-100	
T-A1J2M05	–NRZI DATA TRACK 5	FT602EE0	FT133	5A-100	
T-A1J2M07	–BUS OUT 7	FT101GE2	FT133	5A-100	
T-A1J2M07	–BUS OUT 7	FT102GE2	FT134	16-210	
			FT131	3B-170	
			FT131	5B-100	
T-A1J2M08	–BUS OUT 5	FT102GA2	FT133	16-210	
			FT133	5A-100	
			FT131	5B-100	
T-A1J2M09	–NRZI DATA TRACK 6	FT602EJ0	FT133	5A-100	
T-A1J2M10	–BUS OUT 6	FT101GC2	FT133	5A-100	
T-A1J2M10	–BUS OUT 6	FT102GC2	FT133	16-210	
			FT131	5B-100	
T-A1J2M12	–WRITE STATUS	FT134BF2	FT134	16-160	
			FT134	5A-000	
			FT134	5A-100	
			FT134	5B-000	
			FT134	5B-100	
T-A1J2M13	–WRITE DATA 4	FT132GF2	FT133	5B-100	
				5A-100	
T-A1J2P05	+SENSE RESET	FT112FJ2	FT134	16-160	
T-A1J2P06	–NRZI DATA TRACK 7	FT602EA0	FT133	5A-100	
T-A1J2P10	–WRITE DATA 5	FT133EG2	FT133	5A-100	
			FT133	5B-100	
T-A1J2P11	+BKWD STATUS	FT134EL6	FT134	16-160	
T-A1J2P12	–WRITE DATA 6	FT132GH2	FT132	5B-100	
				5A-100	
T-A1J2P13	–WRITE DATA 7	FT132EJ2	FT132	5B-100	
				5A-100	
T-A1J2S03	–WRITE DATA P	FT132EA2	FT132	5B-100	
				5A-100	
T-A1J2S05	–NRZI DATA TRACK 4	FT602EA0	FT133	5A-100	
T-A1J2S07	–BUS OUT 4	FT101GL2	FT133	16-160	
			FT134	16-210	
			FT134	3A-100	
			FT134	3B-100	
			FT131	3B-130	
			FT133	5A-100	
			FT131	5B-100	
T-A1J2S09	–BUS OUT 3	FT101GJ2	FT131	16-160	
			FT133	16-210	
			FT133	5A-100	
			FT131	5B-100	
T-A1J2S10	–INTERRUPT 1	FT116CE6	FT131	16-160	
T-A1J2U05	–NRZI DATA TRACK 2	FT601EE0	FT133	5A-100	
T-A1J2U09	–NRZI DATA TRACK 3	FT601EJ0	FT133	5A-100	
T-A1J2U10	–INTERRUPT 2	FT131GD6	FT131	16-160	
T-A1K2B03	–NRZI DATA TRK P	FT603EE0	FT603	5A-100	
T-A1K2B05	+SUM OF TAGS	FT134ED2	FT181	16-210	
T-A1K2B05	–NRZI DATA TRK 0	FT603EJ0	FT603	5A-100	
T-A1K2B07	–ZERO THRESH 6	FT183EG6	FT183	5B-100	
T-A1K2B09	–BUS OUT 2	FT101GG2	FT601	5A-100	
T-A1K2B10	+PE MODE UNUSED	FT182GE2	FT182	5B-000	
			FT182	5B-100	
T-A1K2B12	–NRZI DATA TRK 1	FT601EA0	FT601	5A-100	
T-A1K2B13	–NRZI DATA TRK 2	FT601EE0	FT601	5A-100	
T-A1K2D04	–BUS OUT 6	FT102GC2	FT184	16-210	
T-A1K2D05	+STATUS BUS 2	FT113DG2	FT181	16-160	
T-A1K2D06	–BUS OUT 0	FT101GC2	FT603	5A-100	
T-A1K2D06	+STATUS BUS 2A	FT181DG6	FT181	16-160	
			FT181	16-210	
T-A1K2D07	–BUS OUT P	FT101GA2	FT603	5A-100	
T-A1K2D07	–MOVE COMMAND	FT183GD6	FT183	5B-000	
			FT183	5B-100	
T-A1K2D09	–BUS OUT 1	FT101GE2	FT601	5A-100	Mod 3,5,7
T-A1K2D09	–ZERO THRESH P	FT183DB6	FT183	5B-100	
T-A1K2D11	+NRZI L2	FT604DE6	FT604	5A-100	Mod 3,5,7
T-A1K2D12	+WRITE SELECT	FT132CG2	FT604	5A-100	Mod 3,5,7
T-A1K2D12	+SAFETY BAIL RESET	FT283BA2	FT182	2B-100	
			FT182	2B-210	
T-A1K2D13	–MOVE COMMAND	FT134DB2	FT183	16-160	
			FT183	3B-100	
			FT183	3B-110	
			FT133	3B-110	
			FT133	3B-130	
			FT183	3B-140	
T-A1K2D13	+NRZI L1	FT604DC6	FT604	5A-100	Mod 3,5,7
T-A1K2G02	+ERASE U K	FT111FG2	FT182	2B-210	
			FT182	3B-100	

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CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
T-A1K2G02	–NRZI DATA TRACK 3	FT601EJ0	FT601	5A-100	Mod 3,5,7
T-A1K2G04	–BUS OUT 4	FT101GL2	FT184	16-210	
T-A1K2G04	–NRZI DATA TRACK 4	FT602EA0	FT602	5A-100	Mod 3,5,7
T-A1K2G07	+120 PER CENT THRESHOLD	FT181GE2	FT181	5B-100	
T-A1K2G07	–NRZI DATA TRACK 5	FT602EE0	FT602	5A-100	Mod 3,5,7
T-A1K2G08	+ARA CHECK	WB011AC2	FT181	16-160	
			FT181	5B-000	
			FT181	5B-100	
T-A1K2G09	–INTERRUPT 2A	FT181FM2	FT181	16-160	
			FT181	5B-000	
T-A1K2G09	–NRZI DATA TRACK 6	FT602EJ0	FT602	5A-100	Mod 3,5,7
T-A1K2G10	–BUS OUT 2	FT101GG2	FT183	16-210	
T-A1K2G12	+STATUS BUS 6A	FT181EB6	FT181	16-160	
			FT181	16-210	
T-A1K2G13	+STATUS BUS 7A	FT181FG6	FT181	15-010	
			FT181	16-160	
			FT181	16-210	
T-A1K2J02	+FORCE NRZI	FT113FB2	FT604	5A-100	Mod 3,5,7
T-A1K2J04	–BUS OUT 4	FT101GL2	FT602	5A-100	Mod 3,5,7
T-A1K2J04	+ERASE STATUS	FT181EA6	FT181	5B-100	
T-A1K2J06	–BUS OUT 3	FT101GJ2	FT601	5A-100	Mod 3,5,7
T-A1K2J06	–ZERO THRESH 4	FT183EE6	FT183	5B-100	
T-A1K2J07	+STATUS BUS 3A	FT181GH6	FT181	16-160	
			FT181	16-210	
T-A1K2J07	–NRZI DATA TRACK 7	FT603EA0	FT603	5A-100	Mod 3,5,7
T-A1K2J09	–WRITE STATUS	FT134BF2	FT183	5B-100	
T-A1K2J10	–BUS OUT 7	FT102GE2	FT603	5A-100	Mod 3,5,7
T-A1K2J11	–BUS OUT 5	FT102GA2	FT602	5A-100	Mod 3,5,7
T-A1K2J11	+GATED OPP DIRECTION	FT334EH2	FT181	16-160	
T-A1K2J13	–BUS OUT 6	FT102GC2	FT602	5A-100	Mod 3,5,7
T-A1K2J13	+PE SELECT	FT182GD2	FT182	5B-100	
T-A1K2M04	–ZERO THRESH 7	FT183FH6	FT183	5B-100	
T-A1K2M05	+WRITE STATUS A	FT183GG6	FT183	5B-000	
			FT183	5B-100	
T-A1K2M07	–WRITE STATUS	FT183FG2	FT183	5B-100	
T-A1K2P02	+GAP CONTROL TP	FT182002	FT182	5B-000	
			FT182	5B-120	
			FT182	6B-020	
T-A1K2P04	–ZERO THRESH 2	FT183FB6	FT183	5B-100	
T-A1K2P07	–ZERO THRESH 1	FT183EC6	FT183	5B-100	
T-A1K2P09	+SENSE RESET	FT112FJ2	FT181	16-210	
T-A1K2P11	+BACKWARD STATUS	FT134EL6	FT181	15-090	Mod 4,6,8
T-A1K2P12	+INITIATE ARA	FT182GC6	FT182	5B-000	
			FT182	5B-100	
T-A1K2P13	–ZERO THRESH 5	FT183CH6	FT183	5B-100	
T-A1K2S03	–ZERO THRESH 0	FT183DD6	FT183	5B-100	
T-A1K2S04	+80 PER CENT THRESHOLD	FT181GD2	FT181	5B-100	
T-A1K2S12	+STATUS BUS 4A	FT181ED6	FT181	16-160	
			FT181	16-210	
T-A1K2U02	–ZERO THRESH 3	FT183CF6	FT183	5B-100	
T-A1K2U04	+ERASE STATUS	FT181EA6	FT181	15-090	Mod 4,6,8
			FT181	5B-000	
T-A1K2U05	+WRITE CURRENT U K	FT111FJ2	FT182	2B-210	
T-A1K2U06	–6250 SELECT	FT182FB6	FT182	5B-000	
T-A1K2U11	+ARA ON	WB011AC6	FT182	16-210	
			FT182	5B-100	
T-A1K2U13	+PE SELECT	FT182GD2	FT182	5B-000	
T-A1K4B12	–MOVE TAG	FT102GL2	FT102	15-090	Mod 3,5,7
T-A1K4D04	+CONTROL TAG UNUSED	FT102001	FT102	3A-100	
T-A1K4D13	–MOVE TAG I/O	WK001AE5	FT102	3A-140	
T-A1K4G03	+TSTR BUS OUT 0	WK001AC2	FT101	3A-100	
T-A1K4G08	+TSTR BUS OUT 4	WK001AC6	FT101	3A-100	
T-A1K4J09	+TSTR MOVE TAG	WK001AF5	FT102	3A-100	
			FT102	3A-140	
T-A1K4J12	+TSTR COMMAND TAG	WK001AF3	FT102	3A-100	
			FT102	3A-130	

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
T-A1K6B02	–BUS OUT 0 I/O	WK001AA2	FT101	16-160	
			FT101	16-210	
T-A1K6B03	–BUS OUT 1 I/O	WK001AA3	FT101	16-210	
			FT101	16-160	
T-A1K6B04	–BUS OUT 2 I/O	WK001AA4	FT101	16-210	
T-A1K6B05	–BUS OUT 3 I/O	WK001AA5	FT101	16-160	
			FT101	16-210	
T-A1K6B07	–BUS OUT 5 I/O	WK001AA7	FT102	16-210	
T-A1K6B09	–BUS OUT 7 I/O	WK001AA9	FT102	16-160	
			FT101	16-210	
T-A1K6B12	–MOVE TAG	FT102GL2	FT102	15-090	Mod 4,6,8
			FT102	16-160	
			FT102	16-210	
T-A1K6D06	–BUS OUT 4 I/O	WK001AA6	FT101	16-160	
			FT101	16-210	
T-A1K6D07	–BUS OUT 6 I/O	WK001AA8	FT102	16-160	
			FT101	16-210	
T-A1K6D09	–COMMAND TAG	FT102GJ2	FT102	16-160	
			FT102	16-210	
T-A1K6D10	+CONTROL TAG	FT102GG6	FT102	16-160	
			FT102	16-210	
T-A1K6D11	–CNTRL TAG I/O	WK001AE2	FT102	16-160	
			FT102	16-210	
T-A1K6D12	–COMMAND TAG I/O	WK001AE3	FT102	16-160	
T-A1K6D13	–MOVE TAG I/O	WK001AE5	FT102	15-060	
			FT102	16-160	
			FT102	3B-140	
T-A1K6G03	+TSTR BUS OUT 0	WK001AC2	FT101	3B-100	
T-A1K6G08	+TSTR BUS OUT 4	WK001AC6	FT101	3B-100	
T-A1K6J06	+GAP CONTROL	FT102EN2	FT102	6B-020	
T-A1K6J09	+TSTR MOVE TAG	WK001AF5	FT102	3B-100	
			FT102	3B-140	
T-A1K6J11	+TSTR BUS OUT 7	WK001AC9	FT102	3B-170	
T-A1K6J12	+TSTR COMMAND TAG	WK001AF3	FT102	3B-100	
			FT102	3B-130	
T-A1L2B02	–INTERFACE DISABLE	FT910BL4	FT141	16-170	
T-A1L2B04	–TACH/BUSY IN	FT141GG4	FT141	16-160	
T-A1L2B05	–INTERRUPT IN	FT141GJ4	FT141	16-160	
			FT141	5B-000	
			FT141	5B-100	
T-A1L2B09	+LP STATUS DELAYED	FT323FE2	FT141	16-160	
T-A1L2B10	+NRZI READ DATA TRACK 0	FT701GB6	FT146	5A-100	
T-A1L2B12	+NRZI READ DATA TRACK 2	FT701GM6	FT146	5A-100	
T-A1L2B13	–TRACK 0 READ DATA	WB011AA2	FT146	5A-100	
			FT146	5B-100	
T-A1L2D02	–BUS IN 0	FT146FA4	FT146	3A-100	Mod 3,5,7
			FT146	5A-100	
T-A1L2D02	–BUS IN 0	FT148BB6	FT148	15-060	
			FT148	16-160	
			FT148	16-210	
			FT148	3B-100	
			FT148	5B-100	
T-A1L2D04	–BUS IN 1	FT146FB4	FT146	5A-100	Mod 3,5,7
T-A1L2D04	–BUS IN 1	FT148FC6	FT148	15-060	
			FT148	16-160	
			FT148	16-210	
			FT148	5B-100	
T-A1L2D05	–BUS IN 2	FT146FD4	FT146	5A-100	Mod 3,5,7
T-A1L2D05	–BUS IN 2	FT148BC6	FT148	15-060	
			FT148	16-160	
			FT148	16-210	
			FT148	5B-100	
T-A1L2D06	–BUS IN 3	FT146FE4	FT146	5A-100	Mod 3,5,7
T-A1L2D06	–BUS IN 3	FT148FD6	FT148	15-060	
			FT148	16-160	
			FT148	16-210	
			FT148	5B-100	

3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
T-A1L2D07	–BUS IN 4	FT146FG4	FT146	5A-100	Mod 3,5,7
T-A1L2D07	–BUS IN 4	FT148BF6	FT148	15-060	
			FT148	16-160	
			FT148	16-210	
			FT148	5B-100	
T-A1L2D09	–BUS IN 5	FT146FH4	FT146	5A-100	Mod 3,5,7
T-A1L2D09	–BUS IN 5	FT148FG6	FT148	15-010	
			FT148	16-160	
			FT148	16-210	
			FT148	5B-100	
T-A1L2D10	–BUS IN 6	FT146FK4	FT146	5A-100	Mod 3,5,7
T-A1L2D10	–BUS IN 6	FT148BG6	FT148	16-160	
			FT148	16-210	
			FT148	5B-100	
T-A1L2D11	–BUS IN 7	FT146FL4	FT146	5A-100	Mod 3,5,7
T-A1L2D11	–BUS IN 7	FT148FH6	FT148	16-160	
			FT148	16-210	
				5B-100	
T-A1L2D12	–BUS IN P	FT146FN4	FT146	5A-100	Mod 3,5,7
T-A1L2D12	–BUS IN P	FT148BK6	FT148	15-060	
			FT148	5B-100	
T-A1L2D13	–TRACK 2 READ DATA	WB011AA4	FT146	5A-100	
			FT146	5B-100	
T-A1L2G02	+NRZI READ DATA TRACK 1	FT701GG6	FT146	5A-100	
T-A1L2G03	+NRZI READ DATA TRACK 5	FT702GM6	FT146	5A-100	
T-A1L2G04	+NRZI READ DATA TRACK 3	FT702GB6	FT146	5A-100	
T-A1L2G05	–TRACK 5 READ DATA	WB011AA7	FT146	5A-100	
			FT146	5B-100	
T-A1L2G07	+NRZI READ DATA TRACK P	FT703GM6	FT146	5A-100	
T-A1L2G08	+NRZI READ DATA TRACK 6	FT703GB6	FT146	5A-100	
T-A1L2G09	–TIE UP	FT910GD4	FT141	5B-100	
T-A1L2G10	–TRACK 6 READ DATA	WB011AA8	FT146	5A-100	
			FT146	5B-100	
T-A1L2G12	–TRACK 7 READ DATA	WB011AA9	FT146	5A-100	
			FT146	5B-100	
T-A1L2G13	+NRZI L2	FT604DE6	FT141	5A-100	
T-A1L2J02	–TRACK 1 READ DATA	WB011AA3	FT146	5A-100	
			FT146	5B-100	
T-A1L2J04	–TRACK 3 READ DATA	WB011AA5	FT146	5A-100	
			FT146	5B-100	
T-A1L2J05	+NRZI READ DATA TRACK 4	FT702GG6	FT146	5A-100	
T-A1L2J06	–TRACK 4 READ DATA	WB011AA6	FT146	5A-100	
			FT146	5B-100	
T-A1L2J07	–SET METER ENABLE	FT134FC2	FT141	16-160	
T-A1L2J10	–TRACK P READ DATA	WB011AA1	FT146	5A-100	
			FT146	5B-000	
			FT146	5B-100	
			FT146	6A-100	
T-A1L2J11	–BUSY STATUS	FT134FA2	FT141	16-160	
			FT141	16-170	
T-A1L2J12	–PHASE B GATED	FT303DK6	FT141	16-160	
			FT141	16-170	
T-A1L2J13	+SUM OF TAGS	FT134ED2	FT141	16-160	
			FT141	16-170	
T-A1L2M04	+STATUS BUS 2A	FT181DG6	FT147	16-160	
T-A1L2M05	+STATUS BUS 0	FT113DA2	FT147	3A-100	
			FT147	3B-100	
T-A1L2M08	–RUN METER	FT141GH4	FT141	16-160	
T-A1L2P04	+READ GATE	FT134CB6	FT141	16-170	
			FT141	5A-000	
			FT141	5A-100	
T-A1L2P05	–METER OUT I/O	WK001AE6	FT141	16-160	
T-A1L2P09	+NRZI READ DATA TRACK 7	FT703GG6	FT146	5A-100	
T-A1L2P12	+STATUS BUS 4A	FT181ED6	FT147	16-160	
T-A1L6B03	+INT DIS OR - OFF LINE	FT910BM4	FT910	15-010	
			FT910	18-000	

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
T-A1L6B10	–PICK ON LINE RELAY	BW021AB4	FT910	15-010	
			FT910	16-170	
T-A1L6D04	–INTERFACE DISABLE	FT910BL4	FT910	15-010	
T-A1M1E11	+6V	FT910DH4	FT910	5B-100	
T-A1M2B04	+STATUS BUS 3	FT113DK2	FT113	16-160	
			FT113	16-210	
T-A1M2B05	+STATUS BUS 0	FT113DA2	FT113	15-090	Mod 4,6,8
			FT113	16-160	
			FT113	16-210	
T-A1M2B07	+STATUS BUS 1	FT113DD2	FT113	16-160	
			FT113	16-210	
T-A1M2B12	+STATUS BUS 6	FT115CH2	FT115	16-160	
			FT115	16-210	
T-A1M2D06	–GAP CONTROL	FT333EH6	FT113	16-160	
			FT113	5B-000	
			FT113	5B-120	
			FT113	6B-020	
T-A1M2D06	–TRACK 0 READ DATA	WB011AA2	FT701	5A-100	
T-A1M2D10	–DIAGNOSTIC MODE	FT134CF6	FT113	16-160	
T-A1M2D12	+GATED 6250	FT182CG2	FT113	16-210	
T-A1M2D13	+REWIND UNLOAD	FT261BK2	FT113	16-210	
T-A1M2G02	+BACKWARD STATUS LATCH	FT134EN2	FT701	5A-100	
T-A1M2G04	+BKWD STATUS	FT134EL6	FT113	16-160	
T-A1M2G04	+NRZI READ DATA TRACK 0	FT701GB6	FT701	5A-100	Mod 3,5,7
T-A1M2G05	–WRITE CURRENT ON	WB011AF6	FT111	15-090	Mod 4,6,8
			FT111	5B-000	
			FT111	5B-100	
T-A1M2G10	+STATUS BUS IN 2	FT113DG2	FT113	16-160	
			FT113	16-210	
T-A1M2J02	+STATUS BUS 7	FT115EK2	FT115	16-160	
			FT115	16-210	
T-A1M2J02	–TRACK 1 READ DATA	WB011AA3	FT701	5A-100	
T-A1M2J04	+NRZI READ DATA TRACK 1	FT701GG6	FT701	5A-100	
T-A1M2J05	–DATA SECURITY ERASE LATCH	FT134DK6	FT115	16-210	
T-A1M2J06	+TAPE BOTTOMED	FT264GL2	FT114	2B-100	
			FT114	2B-110	
			FT114	3B-170	
T-A1M2J06	–TRACK 2 READ DATA	WB011AA4	FT701	5A-100	Mod 3,5,7
T-A1M2J09	+STATUS BUS 4	FT115CA2	FT115	16-160	
			FT115	16-210	
T-A1M2J09	+NRZI READ DATA TRACK 2	FT701GM6	FT701	5A-100	Mod 3,5,7
T-A1M2J10	–TRACK 3 READ DATA	WB011AA5	FT702	5A-100	Mod 3,5,7
T-A1M2J13	+NRZI READ DATA TRACK 3	FT702GB6	FT702	5A-100	Mod 3,5,7
T-A1M2M02	–BUS OUT 7	FT102GE2	FT112	15-010	
T-A1M2M04	+REWIND OP	FT261FF2	FT111	16-210	
			FT111	5B-100	
T-A1M2M10	+NFP-1A PICKED	FT182CJ4	FT111	5B-100	
T-A1M2M12	–GATED READY	FT261CN6	FT116	15-010	
T-A1M2P02	–BUS OUT 6	FT102GC2	FT112	16-160	
T-A1M2P02	–TRACK 4 READ DATA	WB011AA6	FT702	5A-100	Mod 3,5,7
T-A1M2P04	+NRZI READ DATA TRACK 4	FT702GG6	FT702	5A-100	Mod 3,5,7
T-A1M2P04	+POWER ON RESET	WB022BK4	FT112	2B-100	
			FT112	2B-110	
T-A1M2P05	+AIR PRESSURE FAIL	FT285CL2	FT114	2B-110	
T-A1M2P06	+STATUS BUS 5	FT115EE6	FT115	15-010	
			FT115	16-160	
			FT115	16-210	
T-A1M2P06	–TRACK 5 READ DATA	WB011AA7	FT702	5A-100	Mod 3,5,7
T-A1M2P07	+SUM OF TAGS	FT134ED2	FT112	15-010	
T-A1M2P10	+WRITE CURRENT U.K.	FT111FJ2	FT111	15-090	Mod 4,6,8
			FT111	16-160	
T-A1M2P11	+SENSE RESET	FT112FJ2	FT112	16-160	
			FT112	16-170	
T-A1M2P12	–BUS OUT 5	FT102GA2	FT112	15-090	Mod 4,6,8

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3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
T-A1M2P13	–GATED ERASE CURRENT ON	FT323FH2	FT111	2B-210	
			FT111	3B-100	
T-A1M2S02	-LOSS OF AIR OR OVUV LT	FT114CB6	FT114	16-160	
T-A1M2S04	+NRZI READ DATA TRACK 5	FT702GM6	FT702	5A-100	
T-A1M2S05	+ERASE U.K.	FT111FG2	FT111	16-160	
T-A1M2S07	+LAMP OFF	FT231CF6	FT114	15-090	Mod 4,6,8
			FT114	16-160	
			FT114	2B-100	
			FT114	2B-110	
T-A1M2S09	–FILE PROTECT LAMP	FT111DK4	FT111	5B-100	
T-A1M2U02	+TAPE BOTTOM LEFT	FT264CH4	FT114	16-160	
T-A1M2U02	–TRACK 6 READ DATA	WB011AA8	FT703	5A-100	
T-A1M2U04	–WRITE STATUS	FT134BF2	FT111	16-160	
T-A1M2U04	+NRZI READ DATA TRACK 6	FT703GB6	FT703	5A-100	
T-A1M2U05	+TAPE BOTTOM RIGHT	FT264EH4	FT114	16-160	
T-A1M2U06	+LOAD CHECK	FT285EC2	FT114	15-090	Mod 4,6,8
T-A1M2U06	–TRACK 7 READ DATA	WB011AA9	FT703	5A-100	
T-A1M2U09	+NRZI READ DATA TRACK 7	FT703GG6	FT703	5A-100	
T-A1M2U10	+TIE UP	FT115GB4	FT115	16-160	
			FT114	16-210	
T-A1M2U10	–TRACK P READ DATA	WB011AA1	FT703	5A-100	
T-A1M2U13	+NRZI READ DATA TRACK P	FT703GM6	FT703	5A-100	
T-A1N3D02	–4V	FT910CA4	FT910	5B-100	
T-A1N3D08	GROUND	FT910CB4	FT910	5B-100	
T-A1TB1-9	–48V TEST POINT	ZT051TB1	ZT051	1B-000	
T-A1TB2-1	+12V TEST POINT	ZT051TB1	ZT051	1B-000	
T-A1TB2-5	–12V TEST POINT	ZT051TB2	ZT051	1B-000	
T-A1TB3-12	+11V TEST POINT	ZT051TB3	ZT051	1B-000	
Y1C2B07	–READ AND TAPE OP	BW231EL6	CN281	17-310	
Y1C2D04	+NRZI CHAR GATE FREQ	BW221GK5	CN231	17-160	
			CN231	17-310	
Y1C2D13	–NRZI TM	CN071GE2	CN241	17-180	
Y1C2G03	–SET NRZI FIRST BIT	CN061EM2	CN251	16-190	
			CN061	17-100	
			CN251	17-180	
			CN251	17-310	
Y1C2G13	+RESET FIRST BIT	CN251BH6	CN251	13-410	
			CN251	17-310	
Y1C2J03	+NRZI HI CLIP VRC	CN281FD2	CN281	17-590	
Y1C2J04	+NRZI WRT SKEW CHK	CN251CN2	CN251	17-160	
Y1C2J09	+PARITY EVEN	BN311DM2	CN241	17-310	
Y1C2J11	–TAPE OP B	BW231DL6	CN261	17-180	
			CN261	17-540	with EC733814
Y1C2J12	+NRZI CHAR GATE	CN231GG2	CN231	13-410	
			CN231	17-100	
			CN231	17-180	
			CN231	17-310	
			CN231	17-590	
Y1C2M02	+NRZI DEGATE ECC PH	CN261AE2	CN261	17-540	
Y1C2M03	–NRZI MODE	BW231GK6	CN261	16-190	
			CN261	17-070	
			CN261	17-180	
			CN261	17-220	
			CN261	17-530	
Y1C2M05	–STAT BIT 3 7 TRK	BW231EA6	CN271	17-310	
Y1C2M12	–R/W VRC	CN281EF6	CN281	17-310	
Y1C2P10	+EOD NRZI	CN281FL2	CN281	13-410	
			CN281	17-150	
Y1C2S05	+RESET RD REG 1	CN251FH6	CN251	17-310	
Y1C2S07	+NRZI R/W VRC	GK001GF2	CN281	17-310	
Y1C2S09	+SHIFT EPR	CN291DA6	CN291	17-540	w/o EC733814
Y1C2S10	+SPARE XFR OA	AA171GJ2	CN291	17-540	
Y1C2S11	–STAT BIT 1 START WR RD	AA141GF6	CN251	16-190	
			AA141	17-100	
Y1C2U02	+DEGATE NRZI SELECT	FD041DK6	CN251	16-190	

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
Y1C2U06	–WRT AND TAPE OP	BW231GF6	CN291	17-160	
			CN291	17-310	
Y1C2U09	+BLOCK NRZI ONES	CN231GL6	CN231	13-410	
Y1C2U10	+SHIFT CRC NRZI	CN291EA6	CN291	17-590	
Y1D2B11	–NRZI RD DATA BIT 1	CN061CF2	CN061	17-010	
			CN061	17-590	
Y1D2B13	–NRZI RD DATA BIT P	CN061DB2	CN061	17-010	
			CN061	17-590	
Y1D2D04	–DEVICE BUS IN 7 TO DF	XC032AM4	CN051	16-190	
			XC031	17-310	
			XC031	17-590	
Y1D2D09	–DEVICE BUS IN 6 TO DF	XC032AL4	CN051	16-190	
			CN051	17-310	
			CN051	17-590	
Y1D2D13	–DEVICE BUS IN 5 TO DF	XC032AK4	CN051	16-190	
			CN051	17-310	
			CN051	17-590	
Y1D2G02	–NRZI RD DATA BIT 0	CN061CD2	CN061	17-010	
			CN061	17-590	
Y1D2G07	–NRZI RD DATA BIT 6	CN061GF2	CN061	17-010	
			CN061	17-590	
Y1D2G09	–NRZI RD DATA BIT 7	CN061GH2	CN061	17-010	
			CN061	17-590	
Y1D2G13	–NRZI RD DATA BIT 3	CN061CK2	CN061	17-010	
			CN061	17-590	
Y1D2J02	–STAT BIT 3 7 TRK	BW231EA6	CN051	17-180	
Y1D2J04	+NRZI CRC BIT P	CN061DH6	CN061	17-010	
Y1D2J07	–RDD 169	CN221CG6	CN021	17-110	
Y1D2J09	–DEVICE BUS IN 4 TO DF	XC032AJ4	CN041	16-190	
			CN041	17-310	
			CN041	17-590	
Y1D2J11	–NRZI RD DATA BIT 5	CN061GD2	CN061	17-010	
			CN061	17-590	
Y1D2J12	+9 TRK CORRECTION	CN071ED2	CN071	17-590	
Y1D2J13	–NRZI RD DATA BIT 4	CN061GB2	CN061	17-010	
			CN061	17-590	
Y1D2M02	–NRZI RD DATA BIT 2	CN061CH2	CN061	17-010	
			CN061	17-590	
Y1D2P02	–DEVICE BUS IN 3 TO DF	XC032AH4	CN041	16-190	
			XC031	17-310	
			XC031	17-590	
Y1D2P05	–DEVICE BUS IN 2 TO DF	XC032AF4	CN041	16-190	
			XC031	17-310	
			XC031	17-590	
Y1D2P11	–SET NRZI FIRST BIT	CN061EM2	CN061	13-410	
Y1D2S05	–NRZI MODE	BW231GK6	CN061	17-540	
Y1D2U02	–DEVICE BUS IN 1 TO DF	XC032AE4	CN031	16-190	
			CN031	17-310	
			CN031	17-590	
Y1D2U04	+6250 BPI MODE	BW231GH2	CN061	16-190	
Y1D2U05	+PE MODE	BW231GJ2	CN061	16-190	
Y1D2U07	–DEVICE BUS IN 0 TO DF	XC032AD4	CN031	16-190	
			CN031	17-310	
			CN031	17-590	
Y1D2U09	–R/W VRC BAD A	CN011GD6	CN011	17-310	
Y1D2U12	–DEVICE BUS IN P TO DF	XC032CB4	CN031	16-190	
			CN031	17-310	
			CN031	17-590	
Y1F2B09	–XLATE BFR TK 5	CD111GH7	CE001	17-700	
Y1F2B10	–XLATE BFR TK 7	CD211GH7	CE001	17-700	
Y1F2B12	–XLATE BFR TK 2	CD211GH1	CE001	17-700	
Y1F2B13	–XLATE BFR TK 4	CD311GH7	CE001	17-700	
Y1F2D10	–XLATE BFR TK 6	CD211GH4	CE001	17-700	
Y1F2D12	–EPI	CE001DM2	CE001	17-600	
Y1F2G02	–SR2 BIT 0 TP	CE001CF2	CE001	17-170	
Y1F2G03	–XLATE BFR TK 3	CD311GH4	CE001	17-700	

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3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
Y1F2G05	–SR2 BIT 1 TP	CE001CF3	CE001	17-170	
Y1F2G07	–SR2 BIT 4 TP	CE001CF6	CE001	17-170	
Y1F2G08	–SR2 BIT 2 TP	CE001CF4	CE001	17-170	
Y1F2G09	–SR2 BIT 5 TP	CE001CF7	CE001	17-170	
Y1F2G10	–SR2 BIT 6 TP	CE001CF8	CE001	17-170	
Y1F2G11	–SR2 BIT 3 TP	CE001CF5	CE001	17-170	
Y1F2G12	–SR2 BIT 7 TP	CE001CF9	CE001	17-170	
Y1F2J03	–XLATE BFR TK 1	CD311GH1	CE001	17-700	
Y1F2M03	+POINTER TRK 1	CJ031CB2	CE001	17-220	
			CE001	17-600	
Y1F2M04	+POINTER TRK 7	CJ031CB8	CE001	17-220	
			CE001	17-600	
Y1F2M05	+POINTER TRK 3	CJ031CB4	CE001	17-220	
			CE001	17-600	
Y1F2M07	+POINTER TRK 5	CJ031CB6	CE001	17-220	
			CE001	17-600	
Y1F2M08	–S1 EQUALS S2 BITS 0-3	CE001DG2	CE001	17-600	
Y1F2M10	–I COUNT 4	CE001DD4	CE001	17-600	
Y1F2M11	–S1 EQUALS S2 BITS 4-7	CE001DG4	CE001	17-600	
Y1F2M13	–I COUNT 1	CE001DD2	CE001	17-600	
Y1F2P02	–1 OR 0 PNTRS ON	CE001BA2	CE001	17-110	
Y1F2P03	+POINTER TRK 2	CJ031CB3	CE001	17-220	
			CE001	17-600	
Y1F2P04	+POINTER TRK 4	CJ031CB5	CE001	17-220	
			CE001	17-600	
Y1F2P05	–2 OR 0 PNTRS ON	CE001BA4	CE001	17-110	
Y1F2P06	+POINTER TRK 0	CJ031CB1	CE001	17-220	
			CE001	17-600	
Y1F2P07	+POINTER TRK 6	CJ031CB7	CE001	17-220	
			CE001	17-600	
Y1F2P09	–S2 EQUAL ZERO	CE001CF1	CE001	17-600	
Y1F2P11	–XLATE BFR TKP	CD111GH1	CE001	17-700	
Y1F2P12	–I COUNT 2	CE001DD3	CE001	17-600	
Y1F2S03	–COUNT EQUAL I	CE001EB2	CE001	17-170	
Y1F2S09	–ECC GB ADR 2	CH011FH6	CE001	17-170	
Y1F2U02	+SET I CNT	CH041DJ4	CE001	17-170	
Y1F2U06	–ECC GB ADR 1	CH011FF6	CE001	17-170	
Y1F2U07	–2 PTRS ON PWR	CH021GD6	CE001	15-100	
Y1G2B04	–CRC DATA TRK 8	CJ031EK2	CJ031	17-540	
Y1G2B12	–POINTER BUS BIT 0	CJ011GB2	CJ011	15-100	
			CJ011	17-160	
Y1G2B13	–ALMOST SKEW TRK 1	CD391DC2	CJ011	17-160	
			CJ011	17-700	
Y1G2D13	–POINTER BUS BIT 2	CJ011GB6	CJ011	15-100	
			CJ011	17-160	
Y1G2G04	–ALMOST SKEW TK 3	CD391DC5	CJ011	17-160	
			CJ011	17-700	
Y1G2G09	–RD ECC DATA TRK 7	CJ031DH8	CJ031	17-540	
Y1G2G11	+NRZI DEGATE ECC PH	CN261AE2	CJ031	17-070	
Y1G2G12	–ALMOST SKEW TK 2	CD291DC2	CJ011	17-160	
			CJ011	17-700	
Y1G2J04	+END OF DATA OR PE	CH131GK6	CJ011	17-700	
Y1G2J09	–RD ECC DATA TRK 8	CJ031DH9	CJ031	17-540	
Y1G2J13	–ALMOST SKEW TK 0	CD191DC5	CJ011	17-160	
			CJ011	17-700	
Y1G2M02	–POINTER BUS BIT 1	CJ011GB4	CJ011	15-100	
			CJ011	17-160	
Y1G2M05	–POINTER BUS BIT 6	CJ021GB4	CJ021	15-100	
			CJ021	17-160	
Y1G2M07	–POINTER BUS BIT 7	CJ021GB6	CJ021	15-100	
			CJ021	17-160	
Y1G2M08	–POINTER BUS BIT 5	CJ021GB2	CJ021	15-100	
			CJ021	17-160	
Y1G2M11	–GATED PGM SYNC	CC121BM6	CJ011	17-160	
			CJ011	17-700	
Y1G2P02	–POINTER BUS BIT 3	CJ011GB8	CJ011	15-100	
			CJ011	17-160	
Y1G2P03	–ALMOST SKEW TK 6	CD291DC5	CJ021	17-160	
			CJ021	17-700	
Y1G2P04	–ALMOST SKEW TK 4	CD391DC9	CJ011	17-160	
			CJ011	17-700	
Y1G2P05	–POINTER BUS BIT 4	CJ011GB0	CJ011	15-100	
			CJ011	17-160	
Y1G2P06	–ALMOST SKEW TK 7	CD291DC9	CJ021	17-160	
			CJ021	17-700	
Y1G2P07	–ALMOST SKEW TK 5	CD191DC9	CJ021	17-160	
			CJ021	17-700	
Y1G2P09	–ALMOST SKEW TK P	CD191DC2	CJ021	17-160	
			CJ021	17-700	
Y1G2P10	–POINTER BUS BIT P	CJ021GB8	CJ021	17-160	
Y1G2P11	–ROC CYCLED	CC121BJ6	CJ011	17-160	
			CJ011	17-540	
			CJ011	17-700	
Y1G2P12	–ECC GB TK P	CD111GH2	CJ031	17-540	
Y1G2S03	–EP J	CE001DH4	CJ031	17-540	
Y1G2U03	–EP I	CE001DH2	CJ031	17-540	
			CJ031	17-700	
Y1H2B02	+RESET FORMAT LTHS	CH031DB6	CH151	17-150	
			CH151	17-410	
Y1H2B03	–FORMAT CHAR TK 7	CD211FG9	CH151	17-070	
Y1H2B04	–FORMAT CHAR TK P	CD111FG3	CH151	17-070	
Y1H2D02	–FORMAT CHAR TK 6	CD211FG6	CH151	17-070	
Y1H2D03	–FORMAT CHAR TK 4	CD311FG9	CH161	17-070	
Y1H2D04	+SET FORMAT CHARACTER	CH061DC2	CH151	17-150	
			CH151	17-410	
Y1H2D05	–FORMAT CHAR TK 5	CD111FG9	CH161	17-070	
Y1H2D10	–TAPE OP B	BW231DL6	CH131	16-190	
			BW231	17-150	
			BW231	17-410	
Y1H2D12	–6250 CHK TRK 6	CH151FA2	CH151	17-170	
			CH151	17-700	
Y1H2D13	–6250 CHK TRK 7	CH151FA5	CH151	17-170	
			CH151	17-700	
Y1H2G08	+RESET VOTE LTHS	CH031DE4	CH151	17-150	
Y1H2G09	+A3 OR B1	CH061DG2	CH151	17-070	
			CH151	17-150	
			CH151	17-410	
Y1H2G10	–6250 CHK TRK 4	CH161FK5	CH161	17-170	
			CH161	17-700	
Y1H2G11	–FORMAT CHAR TK 2	CD211FG3	CH161	17-070	
Y1H2G12	+A1 OR B1	CH061DE2	CH151	17-070	
			CH151	17-150	
			CH151	17-410	
Y1H2J02	–6250 CHK TRK P	CH151FA8	CH151	17-170	
			CH151	17-700	
Y1H2J03	–6250 CHK TRK 0	CH161FD2	CH161	17-170	
			CH161	17-700	
Y1H2J04	–6250 CHK TRK 1	CH161FD5	CH161	17-170	
			CH161	17-700	
Y1H2J05	–PE MODE	BW231GJ6	CH121	13-480	
			CH121	17-540	
Y1H2J09	–FORMAT CHAR TK 0	CD111FG6	CH161	17-070	
Y1H2J10	–FORMAT CHAR TK 1	CD311FG3	CH161	17-070	
Y1H2J11	–6250 CHK TRK 5	CH161FK8	CH161	17-170	
			CH161	17-700	
Y1H2J12	–FORMAT CHAR TK 3	CD311FG6	CH161	17-070	
Y1H2J13	–EOD OR CRC OK	CH111FG6	CH111	17-410	
Y1H2M03	–6250 CHK TRK 3	CH161FK2	CH161	17-170	
			CH161	17-700	
Y1H2M05	–FORMAT CHARACTER VOTE	CH151GJ2	CH151	17-540	

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3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
Y1H2M07	–6250 CHK TRK 2	CH161FD8	CH161	17-170	
			CH161	17-700	
Y1H2M09	+END OF DATA PWR	CH131GL6	CH131	17-080	
			CH131	17-170	
Y1H2M11	+9 TRACK CHECK CRC	CN281FJ2	CH111	17-530	
Y1H2M12	–XOUTA BIT 1 ALU2 TO DF	AA141GB2	CH131	13-480	
			CH131	17-170	
			CH131	17-540	
Y1H2M13	–COMBINED ECC DATA 1	CK001CC4	CH111	17-070	
Y1H2P04	+END OF DATA OR PE	CH131GK6	CH131	17-170	
			CH131	17-540	
Y1H2P06	–DETECTED ALL ONES DATA	CH121EF6	CH121	17-410	
Y1H2P11	+EOD NRZI	CN281FL2	CH131	17-540	
Y1H2P12	–STAT BIT 1 START WR RD	AA141GF6	CH131	17-170	
Y1H2P13	–COMBINED ECC DATA 0	CK001BB4	CH111	17-070	
Y1H2S02	–COMBINED ECC DATA 2	CK001DD4	CH111	17-070	
Y1H2S03	–COMBINED ECC DATA 3	CK001EE4	CH141	17-070	
Y1H2S05	–COMBINED ECC DATA 5	CK001GG4	CH121	17-070	
Y1H2S07	–COMBINED ECC DATA 6	CK001AH4	CH121	17-070	
Y1H2S09	–6250 MODE	BW231GH6	CH141	17-530	
Y1H2S10	–CROC REG 16 OR NOT RD CYC	BR001EN2	CH141	16-190	
Y1H2S12	+NRZI CHAR GATE	CN231GG2	CH131	17-370	
Y1H2U02	–COMBINED ECC DATA 4	CK001FF4	CH141	17-070	
Y1H2U04	–PE DECODE A7	CH071ED6	CH121	17-070	
			CH121	17-410	
Y1H2U05	–COMBINED ECC DATA 7	CK001BJ4	CH111	17-070	
Y1H2U06	–RESIDUAL FRAME BKWD	CH131CC6	CH131	17-540	
Y1H2U07	–WR OR RD FORWARD	CH131BF6	CH131	17-170	
			CH111	17-700	
Y1H2U09	–FB DATA OR ALL ONES	CH131GC2	CH131	16-190	
			CH131	17-070	
			CH131	17-170	
			CH131	17-370	
Y1H2U11	–RESIDUAL FRAME FWD	CH131CE6	CH131	17-540	
Y1H2U12	+RESIDUAL 32 COMPARE	CH141FK2	CH141	17-540	
Y1J2B07	+A1 OR B1	CH061DE2	CH061	17-170	
Y1J2B10	+A3 OR B3	CH061DG2	CH061	17-170	
Y1J2D02	–ABC2-C7	CH021CD6	CH081	17-540	
Y1J2D03	+READ FORWARD	CH011EE2	CH011	17-170	
Y1J2D05	+SHIFT CRC	CH081GH4	CH081	17-540	
Y1J2D09	–25 - 75 CLOCK BUS YA	BS021FG9	BS061	17-150	
			CH021	17-410	
Y1J2D12	+SET CHECK BYTE	CH081EB4	CH021	17-540	
Y1J2G03	–SET I CNT CMPR	CH041EL6	CH041	17-170	
			CH041	17-600	
Y1J2G09	–2 PTRS ON PWR	CH021GD6	CH021	15-100	
			CH021	17-600	
Y1J2G12	–SET ECC BUFFER	CH011DD6	CH011	17-600	
			CH081	17-700	
Y1J2G13	–ABC+PE-A6	CH011BF6	CH011	17-700	
Y1J2J03	+SET RESIDUAL CNT	CH081DD4	CH081	17-540	
Y1J2J04	–GB FULL	CB441GK6	CH031	17-070	
Y1J2J05	–PE MODE	BW231GJ6	CH071	17-110	
			CH071	17-220	
Y1J2J07	+GATE HDW PTRS	CH021GM6	CH021	17-600	
Y1J2J10	–FB MODULE SELECT	CH011CB2	CH011	17-170	
			CH011	17-540	
Y1J2J11	–0 - 50 CLOCK BUS YA	BS021FD9	CH081	17-150	
			BS021	17-410	
Y1J2J13	+SHIFT S2	CH011EC4	CH011	17-170	
			CH011	17-600	
Y1J2M02	–CORR TRK 8 ONLY	CH021FB6	CH021	17-170	
Y1J2M04	+POINTER TRK 8	CJ031CB9	CH021	17-110	
			CH021	17-220	
			CH021	17-600	
			CJ031	17-700	

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
Y1J2M11	+WRITE AND TAPE OP	BW231GF2	CH071	17-110	
Y1J2M12	–WR OR RD FORWARD	CH131BF6	CH011	17-170	
Y1J2M13	–1 OR 0 PNTRS ON	CE001BA2	CH021	17-110	
			CH021	17-220	
Y1J2P02	–SET S1 AND FB WRITE GATE	CH011DE6	CH011	17-170	
			CH011	17-540	
Y1J2P03	–MTE WRT SAMPLE	CH131GM6	CH071	17-110	
Y1J2P04	+SET FORMAT CHARACTER	CH061DC2	CH061	17-070	
Y1J2P10	+RESET I CNT	CH031BJ2	CH031	17-160	
Y1J2P12	–STEP CTR LTH	CH031GJ6	CH031	17-160	
Y1J2P13	–2 OR 0 PNTRS ON	CE001BA4	CH021	17-110	
			CH021	17-220	
Y1J2S02	+DEGATE SERIALIZE S1	CH071DF2	CH071	15-100	
Y1J2S03	–ECC GB ADR 4	CH011EK2	CH011	17-170	
			CH011	17-540	
Y1J2S07	–RESET S1 AND S2	CH031GB2	CH031	17-170	
Y1J2S09	+RESET FORMAT LTHS	CH031DB6	CH031	17-160	
			CH031	17-700	
Y1J2S10	+NRZI WRT REQ	CN291ED4	CH021	15-040	
			CH021	17-110	
			CH021	17-370	
Y1J2S11	–ECC GB ADR 2	CH011FH6	CH011	17-170	
			CH011	17-540	
Y1J2S12	–REQ CB WRT CYCLE	CH021GE2	CH021	17-110	
			CH021	17-370	
			CH021	17-540	
			CH021	17-540	
Y1J2U02	+SET PE WRT ENV CHECK	CH071GL2	CH071	17-220	
Y1J2U07	+ECC GROUP FULL	CH011CJ2	CH011	17-160	
			CH011	17-170	
			CH011	17-540	
			CH011	17-600	
Y1J2U09	+SET R/W VRC ERROR	CH071GC2	CH071	17-170	
Y1J2U10	–ECC GB ADR 1	CH011FF6	CH011	17-170	
			CH011	17-540	
Y1J2U12	–RESIDUAL FRAME FWD	CH131CE6	CH081	17-540	
Y1J2U13	+RESET VOTE LTHS	CH031DE4	CH031	17-170	
Y1K2B13	–XLATE BFR TK 1	CD311GH4	CD311	17-170	
Y1K2D03	–NO CMPR TKS 1-3-4	CD391DC7	CD391	17-160	
Y1K2D06	–XOUTA BIT 6 ALU2 TO DF	AA141AD6	CD311	17-170	
			CD311	17-700	
Y1K2D13	–XLATE BFR TK 4	CD311GH7	CD311	17-170	
Y1K2G02	–XLATE BFR TK 1	CD311GH1	CD311	17-170	
Y1K2G04	+INVALID CHAR TK 1	CD311FG1	CD311	17-700	
Y1K2G07	–FORMAT AT CHAR TK 1	CD311FG3	CD311	17-170	
			CD311	17-700	
Y1K2G11	+SAMPLE HDB	CB421ED6	CD311	17-160	
			CD311	17-170	
			CD311	17-700	
Y1K2G12	–GB PTR 1	CD391BK6	CD391	17-170	
			CD391	17-700	
Y1K2G13	+INVALID CHAR TK 4	CD311FG7	CD311	17-700	
Y1K2J06	–GB ADR CNTR 1	CB441GD6	CD311	17-700	
Y1K2J11	–GB PTR 4	CD391FK6	CD391	17-170	
			CD391	17-700	
Y1K2J12	–GB PTR 3	CD391DK6	CD391	17-170	
			CD391	17-700	
Y1K2M03	–FORMAT CHAR TK 4	CD311FG9	CD311	17-170	
			CD311	17-700	
Y1K2M05	+INVALID CHAR TK 3	CD311FG4	CD311	17-700	
Y1K2M07	–FORMAT CHAR TK 3	CD311FG6	CD311	17-170	
			CD311	17-700	
Y1K2M08	–ALMOST SKEW TK 1	CD391DC2	CD391	17-700	

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3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
Y1K2M09	+PE WRITE SKEW TR 1	CD391DC3	CD391	17-160	
			CD391	17-700	
Y1K2P02	−GB ADR CTR 2	CB441GF6	CD311	17-700	
Y1K2P03	+READ FORWARD	CH011EE2	CD311	17-700	
Y1K2P04	+PE WRT SKEW TR 4	CD391DC0	CD391	17-160	
			CD391	17-700	
Y1K2P07	+PE WRT SKEW TR 3	CD391DC6	CD391	17-160	
			CD391	17-700	
Y1K2P11	−ALMOST SKEW TK 4	CD391DC9	CD391	17-700	
Y1K2S09	−ALMOST SKEW TK 3	CD391DC5	CD391	17-700	
Y1K2U07	+RIC RESET TRK 4	CD311BE6	CD311	17-160	
Y1L2B13	−XLATE BFR TK 6	CD211GH4	CD211	17-170	
Y1L2D03	−NO CMPR TKS 2-6-7	CD291DC7	CD291	17-160	
Y1L2D13	−XLATE BFR TK 7	CD211GH7	CD211	17-170	
Y1L2G02	−XLATE BFR TK 2	CD211GH1	CD211	17-170	
Y1L2G04	+INVALID CHAR TK 2	CD211FG1	CD211	17-700	
Y1L2G07	−FORMAT CHAR TK 2	CD211FG3	CD211	17-170	
			CD211	17-700	
Y1L2G12	−GB PTR 2	CD291BK6	CD291	17-170	
			CD291	17-700	
Y1L2G13	+INVALID CHAR TK 7	CD211FG7	CD211	17-700	
Y1L2J11	−GB PTR 7	CD291FK6	CD291	17-170	
			CD291	17-700	
Y1L2J12	−GB PTR 6	CD291DK6	CD291	17-170	
			CD291	17-700	
Y1L2M03	−FORMAT CHAR TK 7	CD211FG9	CD211	17-170	
			CD211	17-700	
Y1L2M05	+INVALID CHAR TK 6	CD211FG4	CD211	17-700	
Y1L2M07	−FORMAT CHAR TK 6	CD211FG6	CD211	17-170	
			CD211	17-700	
Y1L2M08	−ALMOST SKEW TK 2	CD291DC2	CD291	17-700	
Y1L2M09	+PE WRT SKEW TR 2	CD291DC3	CD291	17-160	
			CD291	17-700	
Y1L2P04	+PE WRT SKEW TR 7	CD291DC0	CD291	17-160	
Y1L2P07	+PE WRT SKEW TR 6	CD291DC6	CD291	17-160	
			CD291	17-700	
Y1L2P11	−ALMOST SKEW TK 7	CD291DC9	CD291	17-700	
Y1L2S09	−ALMOST SKEW TK 6	CD291DC5	CD291	17-700	
Y1M2B13	−XLATE BFR TK 0	CD111GH4	CD111	17-170	
Y1M2D03	−NO CMP TKS P-0-5	CD191DC7	CD191	17-160	
Y1M2D13	−XLATE BFR TK 5	CD111GH7	CD111	17-170	
Y1M2G02	−XLATE BFR TK P	CD111GH1	CD111	17-170	
Y1M2G07	−FORMAT CHAR TK P	CD111FG3	CD111	17-170	
Y1M2G12	−GB PTR P	CD191BK6	CD191	17-170	
			CD191	17-700	
Y1M2G13	+INVALID CHAR TK 5	CD111FG7	CD111	17-700	
Y1M2J11	−GB PTR 5	CD191FK6	CD191	17-170	
			CD191	17-700	
Y1M2J12	−GB PTR 0	CD191DK6	CD191	17-170	
			CD191	17-700	
Y1M2M03	−FORMAT CHAR TRK 5	CD111FG9	CD111	17-170	
			CD111	17-700	
Y1M2M04	+6250 BPI WRT SKEW ZN 1	CD191FB3	CD191	17-160	
Y1M2M05	+INVALID CHAR TK 0	CD111FG4	CD111	17-700	
Y1M2M07	−FORMAT CHAR TK 0	CD111FG6	CD111	17-170	
			CD111	17-700	
Y1M2M08	−ALMOST SKEW TK P	CD191DC2	CD191	17-700	
Y1M2M09	+PE WRT SKEW TK P	CD191DC3	CD191	17-160	
			CD191	17-700	
Y1M2P04	+PE WRT SKEW TR 5	CD191DC0	CD191	17-700	
Y1M2P06	+PE WRT SKEW ZN 1	CD191FB4	CD191	17-160	
Y1M2P07	+PE WRT SKEW TR 0	CD191DC6	CD191	17-160	
			CD191	17-700	
Y1M2P09	−ROC IMAGE SA	CB421GM6	CD191	17-160	
Y1M2P11	−ALMOST SKEW TK 5	CD191DC9	CD191	17-700	
Y1M2P13	+EXCESSIVE SKEW ZN 1	CD191FB1	CD191	17-160	
Y1M2S02	+SOME TRK MARG ZN 1	CD191FB2	CD191	17-160	
Y1M2S09	−ALMOST SKEW TK 0	CD191DC5	CD191	17-700	
Y1N2B12	+WRITE SKEW ERROR	CB431CC6	CB431	17-160	
Y1N2D02	−ROC ROTATION BRANCH	CC300DL2	CB411	17-070	
Y1N2D05	−SET GROUP BFR HDR PTRS	CB421DK6	CB421	17-700	
Y1N2D06	−SAMPLE HDB	CB421ED6	CB421	17-160	
Y1N2D09	+GT ROC ADDR TO HDB	CB421EF6	CB421	17-170	
Y1N2D11	−ROC 25 75	CB421EK6	CB421	17-600	
Y1N2G02	−TAPE OP POWERED 2	CB411BL6	CB441	17-070	
Y1N2G04	+SET XLT BUFFER	CB441BD2	CB441	17-170	
			CB441	17-540	
Y1N2G05	−GB ADR CTR 1	CB441GD6	CB441	17-170	
Y1N2G07	−GB ADR CTR 2	CB441GF6	CB441	17-170	
Y1N2G08	−GB FULL	CB441GK6	CB441	17-070	
			CB441	17-160	
			CB441	17-170	
			CB441	17-540	
			CB441	17-600	
Y1N2J04	+A+B 3 25-75	CH061EE2	CB441	17-160	
Y1N2J09	−WRT AND TAPE OP	CB431AL6	CB441	17-160	
Y1N2J12	−0 - 50 CLOCK BUS YB	BS021GD0	CB411	17-070	
Y1N2J13	−25 TO 75 CLOCK BUS YB	BS021FG0	CB411	17-070	
Y1N2M05	+TAPE OP DELAYED	CB411BL2	CB411	15-100	
			CB411	17-540	
Y1N2P06	+1 OR 2 TRK CORR TP	CB431EE6	CB431	17-540	
			CB431	17-600	
Y1N2P09	−SET I CNT CMPR	CH041EL6	CB431	15-140	
			CB431	17-600	
Y1N2P13	+COMBINED R/W VRC ERROR	CB431BK6	CB431	17-170	
Y1P2B02	+DEAD TRACK 6	CC091DK2	CC091	17-160	
			CC091	17-700	
Y1P2B04	+PE WRT SKEW TRK 4	CD391DC0	CC031	17-600	
Y1P2B05	+DEAD TRACK 0	CC031DK2	CC031	17-160	
			CC031	17-700	
Y1P2B09	+PE WRT SKEW TK 2	CD291CD3	CC031	17-600	
Y1P2B11	+PE WRT SKEW TK 6	CD291DC6	CC031	17-600	
Y1P2B12	+PE WRT SKEW TK 5	CD191DC0	CC031	17-600	
Y1P2B13	+PE WRT SKEW TK 7	CD291DC0	CC031	17-600	
Y1P2D02	−SYNC TRACK 0	CC031GG6	CC031	17-160	
Y1P2D04	+DEAD TRACK 7	CC101DK2	CC101	17-160	
			CC101	17-700	
Y1P2D05	−SYNC TRACK 6	CC091GG6	CC091	17-160	
Y1P2D06	+START READ CHECK TP	CC031EC2	CC031	17-600	
Y1P2D07	−RECORD TRACK 6	CC091GK6	CC091	17-160	
Y1P2D10	−TIME SENSE TK 5	CA100DH1	CC001	15-060	
			CC001	16-190	
			CC001	16-220	
			CC001	17-100	
			CC001	17-150	
			CC001	17-180	
Y1P2D11	−RECORD TRACK 7	CC101GK6	CC101	17-160	
Y1P2G02	+PE WRT SKEW TK 0	CD191DC6	CC031	17-600	
Y1P2G03	+DEAD TRACK REG P	CC111DK2	CC111	17-160	
			CC111	17-700	
Y1P2G05	+PE WRT SKEW TK 3	CD391DC6	CC031	17-600	
Y1P2G10	+PE WRT SKEW TK 1	CD391DC3	CC031	17-600	

3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
Y1P2G11	–RECORD TRACK 3	CC061GK6	CC061	17-160	
Y1P2G12	–TIME SENSE TK 7	CA200DH1	CC001	15-060	
			CC001	16-190	
			CC001	16-220	
			CC001	17-100	
			CC001	17-150	
			CC001	17-180	
Y1P2G13	–TIME SENSE 2	CA200DE4	CC001	15-060	
			CC001	16-190	
			CC001	16-220	
			CC001	17-100	
			CC001	17-150	
			CC001	17-180	
Y1P2J03	–SYNC TRACK 7	CC101GG6	CC101	17-160	
Y1P2J06	–SYNC TRACK P	CC111GG6	CC111	17-160	
Y1P2J12	–GATED PGM SYNC	CC121BM6	CC121	17-700	
Y1P2J13	–BOR 27 COMB OR DT BRANCH COND	CC001GM6	CC001	15-060	
			CC001	15-100	
			CC001	16-190	
			CC001	16-220	
			CC001	17-070	
			CC001	17-080	
			CC001	17-600	
Y1P2M02	+TM CONFIGURATION	CC001GE4	CC001	15-080	
			CC001	16-190	
Y1P2M03	–TAPE OP B	BW231DL6	CC001	17-160	
Y1P2M05	+SOME TRK MARG	CD401CF4	CC021	17-600	
Y1P2M07	–IBG BRANCH	CC001FC2	CC001	13-240	
			CC001	16-190	
			CC001	17-010	
			CC001	17-070	
			CC001	17-080	
			CC001	17-110	
			CC001	17-160	
			CC001	17-170	
			CC001	17-220	
			CC001	17-410	
			CC001	17-540	
			CC001	17-600	
			CC001	17-700	
Y1P2M08	–SYNC TRACK 3	CC061GG6	CC061	17-160	
Y1P2M09	+DEAD TRACK 4	CC071DK2	CC071	17-160	
			CC071	17-700	
Y1P2M11	+PE WRT SKEW TRK P	CD191DC3	CC111	17-600	
Y1P2M12	–TIME SENSE 6	CA200DC1	CC001	15-060	
			CC001	16-190	
			CC001	16-220	
			CC001	17-100	
			CC001	17-150	
			CC001	17-180	
Y1P2P02	–TIME SENSE 1	CA300DE4	CC001	15-060	
			CC001	16-190	
			CC001	16-220	
			CC001	17-100	
			CC001	17-150	
			CC001	17-180	
Y1P2P03	–TIME SENSE P	CA100DC1	CC001	15-060	
			CC001	16-190	
			CC001	16-220	
			CC001	17-100	
			CC111	17-150	
			CC001	17-180	
Y1P2P04	–RECORD TRACK P	CC111GK6	CC111	17-160	
Y1P2P06	+WRITE AND TAPE OP	BW231GF2	CC021	17-050	
Y1P2P09	–TIME SENSE 0	CA100DE4	CC001	15-060	
			CC001	16-190	
			CC001	16-220	
			CC001	17-100	
			CC121	17-150	
			CC001	17-180	
Y1P2P10	–TIME SENSE 3	CA300DC1	CC001	15-060	
			CC001	16-190	
			CC001	16-220	
			CC001	17-100	
			CC001	17-150	
			CC001	17-180	
Y1P2P11	–RECORD TRACK 0	CC031GK6	CC031	17-160	
Y1P2P12	–SYNC TRACK 4	CC071GG6	CC071	17-160	
Y1P2S04	–SYNC TRACK 1	CC041GG6	CC041	17-160	
Y1P2S05	–RECORD TRACK 1	CC041GK6	CC041	17-160	
Y1P2S09	+DEAD TRACK 1	CC041DK2	CC041	17-160	
			CC041	17-700	
Y1P2S10	+BLOCK OR ENV LOSS BRANCH	CC011GC6	CC011	16-190	
			CC011	17-080	
			CC011	17-370	
			CC011	17-410	
Y1P2S11	+SAGC 6 COMBINATION	CC001EA2	CC001	15-060	
			CC001	16-200	
			CC001	16-220	
Y1P2S12	–TIME SENSE TK 4	CA300DH1	CC001	15-060	
			CC001	16-190	
			CC001	16-220	
			CC001	17-100	
			CC001	17-150	
			CC001	17-180	
Y1P2S13	+DEAD TRACK 3	CC061DK2	CC061	17-160	
			CC061	17-700	
Y1P2U02	–SYNC TRACK 5	CC081GG6	CC081	17-160	
Y1P2U03	+DEAD TRACK 5	CC081DK2	CC081	17-160	
			CC081	17-700	
Y1P2U04	–ROC CYCLED	CC121BJ6	CC121	15-100	
Y1P2U05	–RECORD TRACK 5	CC081GK6	CC081	17-160	
Y1P2U07	–CLOCK SYNC FREQ OSC	BW221GN2	CC041	17-160	
Y1P2U09	–RECORD TRACK 4	CC071GK6	CC061	17-160	
Y1P2U10	–RECORD TRACK 2	CC051GK6	CC051	17-160	
Y1P2U11	+DEAD TRACK 2	CC051DK2	CC051	17-160	
			CC051	17-700	
Y1P2U12	–WRITE OSC	CC041FC6	CC041	17-160	
Y1P2U13	–SYNC TRACK 2	CC051GG6	CC051	17-160	
Y1Q2B02	+LOW GAIN	CB111EL6	CB111	16-190	
			CB111	17-080	
			CB111	17-160	
Y1Q2B03	–B	CB111CJ6	CB111	16-190	
			CB111	17-080	
Y1Q2B05	–A	CB111CL6	CB111	16-190	
			CB111	17-080	
Y1Q2B07	–XOUTA BIT 7 ALU2	BW211EH6	CB111	16-190	
			CB111	17-080	
Y1Q2B10	–XOUTA BIT 5 ALU2	BW211BC6	CB111	16-190	
			CB111	17-080	
Y1Q2B12	+P.E. WRITE AND TAPE OP	CB471FD2	CB111	16-190	
			CB111	17-050	
			CB111	17-080	
Y1Q2B13	–GATE TIE	PR161GM6	CB131	17-050	
Y1Q2D02	+PE MODE	BW231GJ2	CB111	16-190	
			CB111	17-050	
			BW231	17-080	

3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
Y1Q2D03	–PE SLD LEVEL	CB111EB2	CB111	16-190	
			CB111	17-080	
Y1Q2D05	–6250 SLD LEVEL	CB111BD6	CB111	16-190	
			CB111	17-080	
Y1Q2D06	+STAT BIT 2 ALU WR P BURST	AA141EF2	CB121	16-190	
			AA141	17-080	
Y1Q2D07	–6250 2 SLD	CB111FJ2	CB111	16-190	
			CB111	17-080	
Y1Q2D10	–6250 POINTER MODE	CC121GM6	CB131	17-050	
Y1Q2D11	–6250 1 SLD	CB111DH6	CB111	16-190	
			CB111	17-080	
Y1Q2D12	–WRITE SLD LEVEL	CB111FB2	CB111	16-190	
			CB111	17-080	
Y1Q2G03	–PE2 SLD	CB111FF2	CB111	16-190	
			CB111	17-080	
			CB111	17-170	
Y1Q2G05	–PE1 SLD	CB111DE6	CB111	16-190	
			CB111	17-080	
Y1Q2G08	+0 PCT AMPL CTRL TRK 5	CB131DG2	CB131	15-060	
Y1Q2J02	–6250 DENSITY SLD	CB111DC6	CB111	16-190	
			CB111	17-080	
Y1Q2M04	–PE	CB111BH6	CB111	16-190	
			CB111	17-080	
			CB111	17-160	
Y1Q2M05	–PE	CB111BG6	CB111	16-190	
			CB111	17-080	
			CB111	17-160	
Y1Q2M07	–6250	CB111BF2	CB111	16-190	
			CB111	17-080	
			CB111	17-160	
Y1Q2P03	+0 PCT AMPL CTRL TRK O	CB131FA6	CB131	15-060	
Y1Q2P04	–6250	CB111BH2	CB111	16-190	
			CB111	17-080	
			CB111	17-160	
Y1Q2P05	–PE	CB111BF6	CB111	16-190	
			CB111	17-080	
			CB111	17-160	
Y1Q2P06	–6250	CB111BG2	CB111	16-190	
			CB111	17-080	
			CB111	17-160	
Y1Q2P13	+0 PCT AMPL CTRL TRK P	CB131CK2	CB131	15-060	
Y1Q2S13	–NRZI MODE	BW231GK6	CB111	16-190	
Y1Q2U13	+NRZI	CB111DL2	CB111	16-190	
			CB111	17-050	
			CB111	17-080	
Y1R2B03	–PHASE ERROR TK 4	CA300DJ5	CA300	17-700	
Y1R2B05	–VFC PRIME DATA TK 4	CA300DJ4	CA300	17-160	
			CA300	17-700	
Y1R2D02	–PE PHASE ERROR TK 4	CA300DJ3	CA300	17-700	
Y1R2D07	–VFC DATA TK 4	CA300DJ6	CA300	17-160	
			CA300	17-170	
			CA300	17-700	
Y1R2D10	–TIME SENSE TK 4	CA300DH1	CA300	13-470	
			CA300	17-160	
			CA300	17-700	
Y1R2D12	+STEP RIC TK 4	CA300DK1	CA300	17-160	
			CA300	17-700	
Y1R2D13	–DEVICE BUS IN 4 TO DF	XC032AJ4	CA300	15-060	
			CA300	16-190	
			XC031	17-100	
			XC031	17-150	
			CA300	17-160	
			CA300	17-170	
			XC031	17-180	
			CA300	17-600	
			CA300	17-700	

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
Y1R2G07	–PHASE ERROR TK 1	CA300DG1	CA300	17-700	
Y1R2G08	–VFC PRIME DATA TK 1	CA300DF6	CA300	17-160	
			CA300	17-700	
Y1R2G09	–VFC DATA TK 1	CA300DG2	CA300	17-160	
			CA300	17-170	
			CA300	17-700	
Y1R2G10	–PE PHASE ERROR TK 1	CA300DF5	CA300	17-700	
Y1R2M02	+STEP RIC TK 1	CA300DG4	CA300	17-160	
			CA300	17-700	
Y1R2M03	–TIME SENSE 1	CA300DE4	CA300	13-470	
			CA300	17-050	
			CA300	17-160	
			CA300	17-700	
Y1R2M04	–DEVICE BUS IN 1 TO DF	XC032AE4	CA300	15-060	
			CA300	16-190	
			CA321	17-050	
			XC031	17-100	
			XC031	17-150	
			CA300	17-160	
			CA300	17-170	
			XC031	17-180	
			CA300	17-600	
			CA300	17-700	
Y1R2S04	–DEVICE BUS IN 3 TO DF	XC032AH4	CA300	15-060	
			CA300	16-190	
			XC031	17-100	
			XC031	17-150	
			CA300	17-160	
			CA300	17-170	
			XC031	17-180	
			CA300	17-600	
			CA300	17-700	
Y1R2S10	–PHASE ERROR TK 3	CA300DD5	CA300	17-700	
Y1R2U05	–TIME SENSE 3	CA300DC1	CA300	13-470	
			CA300	17-160	
			CA300	17-700	
Y1R2U09	–PE PHASE ERROR TK 3	CA300DD3	CA300	17-700	
Y1R2U10	–VFC DATA TK 3	CA300DD6	CA300	17-160	
			CA300	17-170	
			CA300	17-700	
Y1R2U12	+STEP RIC TK 3	CA300DE1	CA300	17-160	
			CA300	17-700	
Y1R2U13	–VFC PRIME DATA TK 3	CA300DD4	CA300	17-160	
			CA300	17-700	
Y1S2B03	–PHASE ERROR TK 7	CA200DJ5	CA200	17-700	
Y1S2B05	–VFC PRIME DATA TK 7	CA200DJ4	CA200	17-160	
			CA200	17-700	
Y1S2D02	–PE PHASE ERROR TK 7	CA200DJ3	CA200	17-700	
Y1S2D07	–VFC DATA TK 7	CA200DJ6	CA200	17-160	
			CA200	17-170	
			CA200	17-700	
Y1S2D10	–TIME SENSE TRK 7	CA200DH1	CA200	17-160	
			CA200	17-700	
Y1S2D12	+STEP RIC TK 7	CA200DK1	CA200	17-160	
			CA200	17-700	
Y1S2D13	–DEVICE BUS IN 7 TO DF	XC032AM4	CA200	15-060	
			CA200	16-190	
			XC031	17-100	
			XC031	17-150	
			CA200	17-160	
			CA200	17-170	
			XC031	17-180	
			CA200	17-600	
			CA200	17-700	
Y1S2G07	–PHASE ERROR TK 2	CA200DG1	CA200	17-700	
Y1S2G08	–VFC PRIME DATA TK 2	CA200DF6	CA200	17-700	

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XF7375 Seq 2 of 2	2736058 Part Number	See EC History	845958 1 Sep 79	847298 15 Aug 83				

3803-2 CROSS-REFERENCE, PINS TO LOGICS

CARD PIN	LINE NAME	NET NUMBER	LOGIC PAGE	MAP	COMMENTS
Y1S2G09	–VFC DATA TK 2	CA200DG2	CA200	17-160	
			CA200	17-170	
			CA200	17-700	
Y1S2G10	–PE PHASE ERROR TK 2	CA200DF5	CA200	17-700	
Y1S2M02	+STEP RIC TK 2	CA200DG4	CA200	17-160	
			CA200	17-700	
Y1S2M03	–TIME SENSE 2	CA200DE4	CA200	17-160	
			CA200	17-700	
Y1S2M04	–DEVICE BUS IN 2 TO DF	XC032AF4	CA200	15-060	
			CA200	16-190	
			XC031	17-100	
			XC031	17-150	
			CA200	17-160	
			CA200	17-170	
			XC031	17-180	
			CA200	17-600	
			CA200	17-700	
Y1S2S04	–DEVICE BUS IN 6 TO DF	XC032AL4	CA200	15-060	
			CA200	16-190	
			XC031	17-100	
			XC031	17-150	
			CA200	17-160	
			CA200	17-170	
			XC031	17-180	
			CA200	17-600	
			CA200	17-700	
Y1S2S10	–PHASE ERROR TK 6	CA200DD5	CA200	17-700	
Y1S2U05	–TIME SENSE 6	CA200DC1	CA200	17-160	
			CA200	17-700	
Y1S2U09	–PE PHASE ERROR TK 6	CA200DD3	CA200	17-700	
Y1S2U10	–VFC DATA TK 6	CA200DD6	CA200	17-160	
			CA200	17-700	
Y1S2U12	+STEP RIC TK 6	CA200DE1	CA200	17-160	
			CA200	17-700	
Y1S2U13	–VFC PRIME DATA TK 6	CA200DD4	CA200	17-160	
			CA200	17-700	
Y1T2B03	–PHASE ERROR TK 5	CA100DJ5	CA100	17-700	
Y1T2B05	–VFC PRIME DATA TK 5	CA100DJ4	CA100	17-160	
			CA100	17-700	
Y1T2D02	–PE PHASE ERROR TK 5	CA100DJ3	CA100	17-700	
Y1T2D07	–VFC DATA TK 5	CA100DJ6	CA100	17-160	
			CA100	17-170	
			CA100	17-700	
Y1T2D10	–TIME SENSE TRK 5	CA100DH1	CA100	17-160	
			CA100	17-700	
Y1T2D12	+STEP RIC TK 5	CA100DK1	CA100	17-160	
			CA100	17-700	
Y1T2D13	–DEVICE BUS IN 5 TO DF	XC032AK4	CA100	15-060	
			CA100	16-190	
			XC031	17-100	
			XC031	17-150	
			CA100	17-160	
			CA100	17-170	
			XC031	17-180	
			CA100	17-600	
			CA100	17-700	
Y1T2G07	–PHASE ERROR TK 0	CA100DG1	CA100	17-700	
Y1T2G08	–VFC PRIME DATA TK 0	CA100DF6	CA100	17-160	
			CA100	17-700	
Y1T2G09	–VFC DATA TK 0	CA100DG2	CA100	17-160	
			CA100	17-170	
			CA100	17-700	
Y1T2G10	–PE PHASE ERROR TK 0	CA100DF5	CA100	17-700	
Y1T2J12	+NRZI	CB111DL2	CA100	16-190	
Y1T2M02	+STEP RIC TK 0	CA100DG4	CA100	17-160	
Y1T2M03	–TIME SENSE 0	CA100DE4	CA100	17-700	
			CA100	17-160	
			CA100	17-700	
Y1T2M04	–DEVICE BUS IN 0 TO DF	XC032AD4	CA100	15-060	
			CA100	16-190	
			CA100	17-070	
			XC031	17-100	
			XC031	17-150	
			CA100	17-160	
			CA100	17-170	
			XC031	17-180	
			CA100	17-600	
			CA100	17-700	
Y1T2S04	–DEVICE BUS IN P TO DF	XC032CB4	CA100	15-060	
			CA100	16-190	
			CA100	17-020	
			CA111	17-050	
			XC031	17-100	
			XC031	17-150	
			CA100	17-160	
			CA100	17-170	
			XC031	17-180	
			XC032	17-410	
			CA111	17-540	
			CA100	17-600	
			CA100	17-700	
Y1T2S10	–PHASE ERROR TK P	CA100DD5	CA100	17-700	
Y1T2U05	–TIME SENSE P	CA100DC1	CA100	17-050	
			CA100	17-160	
			CA100	17-700	
Y1T2U09	–PE PHASE ERROR TK P	CA001DD3	CA001	17-700	
Y1T2U10	–VFC DATA TK P	CA100DD6	CA100	17-160	
			CA100	17-170	
			CA100	17-700	
Y1T2U12	+STEP RIC TK P	CA100DE1	CA100	17-160	
			CA100	17-700	
Y1T2U13	–VFC PRIME DATA TK P	CA100DD4	CA100	17-160	
			CA100	17-700	

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XF7380 Seq 1 of 2	2736059 Part Number	See EC History	845958 1 Sep 79					

NOTES:

ERROR CORRECTION SENSE ANALYSIS

From: 15-100

Always start with Seq 1 and follow the procedure in sequence unless directed otherwise.
Remember to END all problem or maintenance calls by going to MAP 00-030.

Seq	Condition/Instruction	Action
1	Determine the failing OLT section and routine using the error printout. Go to the sequence number indicated: **Failure** **Go to Seq** F0xxx 2 G01xx 6 G0231 9 G0232 14 G03xx 16 G05xx 23 H0xxx 25	
2	Is Byte 2 all ones ("FF")?	Change Y1J2. If not fixed, go to Seq 26.
3	Is Byte 3 Bit 0 On?	Change Y1J2. If not fixed, go to Seq 26.
4	Is Byte 9, Bit 0 On?	Change A1G2. If not fixed, go to Seq 26.
5	If not:	Change A1K2. If not fixed, go to Seq 26.
6	Is Byte 0, Bit 4 On?	Change A1K2. If not fixed, go to Seq 26.
7	Was Data Check expected? (Check the mask on print.)	Change Y1N2. If not fixed, go to Seq 26.
8	If not:	Change Y1K2/L2/M2. If not fixed, go to Seq 26.
9	Is Byte 5, Bit 5 On?	Go to Seq 12.
10	Is Byte 3, Bit 0 On?	Change in order: 1. Y1F2 2. Y1J2 If not fixed, go to Seq 26.
11	If not:	Change in order: 1. Y1J2 2. Y1F2 3. Y1K2/L2/M2 If not fixed, go to Seq 26.
12	Is Byte 3, Bit 2 On?	Change in order: 1. Y1P2 2. Y1N2 If not fixed, go to Seq 26.
13	If not:	Change in order: 1. Y1N2 2. Y1K2/L2/M2 If not fixed, go to Seq 26.
14	Is Byte 3, Bit 0 On?	Change Y1N2. If not fixed, go to Seq 26.
15	If not:	Change in order: 1. Y1F2 2. Y1J2 If not fixed, go to Seq 26.
16	Is data check On?	Go to Seq 19.
17	Is 7-Track feature installed?	Change Y1D2. If not fixed, go to Seq 26.
18	If not:	Change Y1Q2. If not fixed, go to Seq 26.
19	Is Byte 5, Bit 4 On?	Change Y1K2/L2/M2. If not fixed, go to Seq 26.
20	Is Byte 3, Bit 0 On?	Change in order: 1. Y1K2/L2/M2 2. Y1F2 3. Y1G2 If not fixed, go to Seq 26.
21	Is Byte 3, Bit 2 On?	Change Y1K2/L2/M2. If not fixed, go to Seq 26.
22	If not:	Change in order: 1. Y1F2 2. Y1J2 If not fixed, go to Seq 26.
23	Is Byte 2, All Bits Off?	Change in order: 1. Y1K2/L2/M2 2. Y1P2 3. Y1N2 If not fixed, go to Seq 26.
24	If not:	Change Y1G2. If not fixed, go to Seq 26.
25	Go to Action Column.	Change Y1J2. If not fixed, go to Seq 26.
26	Refer to the OLT Users Guide (level 8 or above) for a description of the failing OLT function. Analyze the error printout using the OLT Users Guide as a reference. Can you define a failing mode (Command sequence, 6250 single or double error correction, Phase Encode mode, diagnostic read or write, etc.)?	Go to Seq 28.
27	If not:	Recheck symptoms.
28	Does the failing mode or sequence require a Diagnostic Mode Set or Set Diagnose command?	Go to Seq 34.
29	Is the failing mode 6250 single error correction?	Go to 17-600.
30	Is the failing mode 6250 double error correction?	Go to 17-600.
31	Can the failing mode be duplicated from the CE panel? Refer to MAP 12-000.	Go to 17-700.
32	Is this the second time through this sequence?	Go to 00-030.
33	If not:	Recheck symptoms. Go to Seq 26.
34	Does the Diagnostic Read in OLT Section F fail? The Diagnostic Read in 6250 mode disables error correction and transfers the ECC character to the channel with the data. Analyze the error printout of the actual and expected data to determine the failing track or tracks.	Utilize the loop-on-error option of the OLTs. Refer to the probe charts on 17-701 and the 6250 timing charts on 17-702, 17-703, 17-704 to determine the failure cause.
35	Does the Diagnostic Write in OLT Section G fail? This diagnostic checks Write Error Checking on a per-track basis in 6250 mode. Analyze the error printout to determine the failing track(s).	Utilize the loop-on-error option of the OLTs. Refer to the probe charts on 17-701 and the 6250 timing charts on 17-702, 17-703, 17-704 to determine the failure cause.
36	Does the Diagnostic Write in OLT Section H fail? This diagnostic checks Write Error Checking circuits in PE mode. Analyze the error printouts to determine the failing track(s).	Utilize the loop-on-error option of the OLTs. Refer to the probe charts on 17-701 and the timing charts on 17-705 to find the failing FRU.
37	If not:	Recheck symptoms.

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