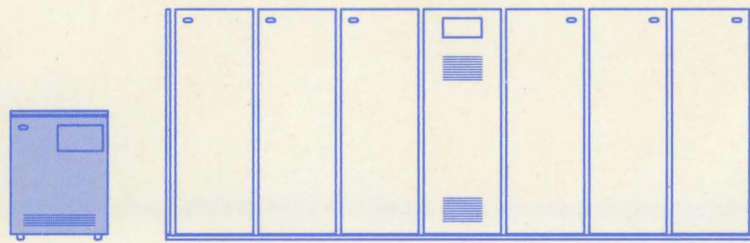




Hardware Maintenance Reference (HMR)



3745
3745
3745
3745



IBM 3745 Communication Controller Models 130, 150, and 170

SY33-2066-2

Hardware Maintenance Reference (HMR)

Third Edition (March 1991)

This major revision obsoletes SY33-2066-1. Extensive changes have been made throughout this edition, and this manual should be read in its entirety.

Changes are made periodically to the information herein. Any such changes will be reported in subsequent revisions or Technical Newsletters. Before using this publication in connection with the operation of IBM systems, consult the latest *IBM System/370, 30xx, 4300, and 9370 Processors Bibliography*, GC20-0001.

The drawings and specifications contained herein shall not be reproduced in whole or in part without written permission. IBM has prepared this service manual for the use of IBM customer engineers in the installation, maintenance, or repair of the specific machines indicated. IBM makes no representations that it is suitable for any other purpose.

Publications are not stocked at the addresses given below. Requests for IBM publications should be made to your IBM representative or to the IBM branch office serving your locality. A form for readers' comments is provided at the back of this publication. If the form has been removed, comments may be addressed to either of the following:

- International Business Machines Corporation
Department 6R1LG
180 Kost Road,
Mechanicsburg, PA 17055
U.S.A.
- IBM France, Centre d'Etudes et Recherches
Service 0762 BP 79
06610 La Gaude
France

© Copyright International Business Machines Corporation 1989, 1991. All rights reserved.

Note to U.S. Government Users — Documentation related to restricted rights — Use, duplication or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corp.

Special Notices

References in this publication to IBM products, programs, or services do not imply that IBM intends to make these available in all countries in which IBM operates.

Any references to an IBM licensed program or other IBM product in this publication is not intended to state or imply that only IBM's program or other product may be used. Any functionally equivalent program that does not infringe any of IBM's intellectual property rights may be used instead of the IBM product. Evaluation and verification of operation in conjunction with other products, except those expressly designated by IBM, is the user's responsibility.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license enquiries, in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

The following terms, DENOTED BY AN ASTERISK (*), used in this publication, are trademarks of the IBM Corporation in the United States or other countries:

IBM
LPDA
MVS
NetView
OS/2
PS/2
RETAIN
VSE
VTAM

Safety

General Safety

For general safety information, see:

- *Telecommunication Products Safety Handbook*, GA33-0126.

Safety Notices

See *Safety Notices* located at the beginning of the *Maintenance Information Procedures* manual.

Service Inspection Procedures

The *Service Inspection Procedures* help service personnel check whether the 3745 conforms to IBM* safety criteria. They have to be used each time the 3745 safety is suspected.

The *Service Inspection Procedures* section is located at the beginning of the *3745 Maintenance Information Procedures (MIP)* manual, SY33-2070.

The 3745 areas and functions checked through service inspection procedures are:

1. External covers
2. Safety labels
3. Safety covers and shields
4. Grounding
5. Circuit breaker and protector rating
6. Input power voltage
7. Power-ON indicator
8. Emergency power OFF.

Federal Communications Commission (FCC) Statement

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

Properly shielded and grounded cables and connectors must be used in order to meet FCC emission limits. IBM is not responsible for any radio or television interference caused by using other than recommended cables and connectors or by unauthorized changes or modifications to this equipment. Unauthorized changes or modifications could void the user's authority to operate the equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.



Contents

| | |
|---|---------|
| Chapter 1. General Information | 1-1 |
| 3745 in a Network | 1-2 |
| Identification and Capacity | 1-5 |
| Controller Structure | 1-6 |
| Programming Support and Network Management | 1-17 |
| Using the Library for Service | 1-21 |
| Maintenance | 1-23 |
| Chapter 2. Central Control Unit (CCU) | 2-1 |
| The CCU in 3745 Data Flow | 2-2 |
| General Description | 2-3 |
| Functional Description | 2-4 |
| CCU Environment | 2-11 |
| Main Storage | 2-12 |
| CCU-to-Storage Interconnection | 2-16 |
| CCU to and from Adapters | 2-19 |
| CCU to and from MOSS | 2-39 |
| CCU Diagnostics | 2-40 |
| Performance Test Points | 2-46 |
| Chapter 3. Buses | 3-1 |
| The Buses in 3745 Data Flow | 3-2 |
| Generalities | 3-3 |
| Bus Propagation Cards (BPC1/BPC2) | 3-28 |
| Adapter Addressing | 3-29 |
| Adapter Bypass Mechanism | 3-44 |
| IOC Bus Scoping Routine | 3-49 |
| Chapter 4. Transmission Subsystem (TSS) | 4-1 |
| Low-Speed Scanner (LSS) | 4-6 |
| LIC Board | 4-7 |
| Serial Link (SL) | 4-12 |
| Communication Scanner Processor (CSP) | 4-12 |
| Front-End Scanner (FES) | 4-22 |
| Front-End Scanner Adapter (FESA) | 4-26 |
| Serial Link (SL) | 4-34 |
| Double Multiplexer Card (DMUX) | 4-35 |
| Single Multiplexer Card (SMUXA/B) | 4-39 |
| LIC Types 1 to 4 Cards | 4-43 |
| LIC Types 5 and 6 DTE Function | 4-54 |
| LIC Type 5 DCE Function | 4-57 |
| LIC Type 6 DSU/CSU Function | 4-80 |
| Problem Determination Aid for LIC Types 1 to 4 | 4-92 |
| Problem Determination Aid for LIC Type 5 and LIC Type 6 | 4-95 |
| TSS interface cables | 4-100 |
| Chapter 5. High Performance Transmission Subsystem (HPTSS) | 5-1 |
| HPTSS in 3745 Data Flow | 5-3 |
| Introduction | 5-4 |
| Internal Interconnections | 5-9 |
| Communication Scanner Processor (CSP) | 5-10 |

| | |
|--|----------|
| Front-End Scanner High-Speed (FESH) | 5-11 |
| Transmit Operation | 5-14 |
| Receive Operation | 5-16 |
| Modem Interface Management | 5-19 |
| Error Detection and Reporting | 5-23 |
| Miscellaneous Status Fields | 5-31 |
| Problem Determination Aid | 5-37 |
| Communication Interfaces | 5-40 |
| Chapter 6. The Token-Ring Subsystem | 6-1 |
| The TRSS in 3745 Data Flow | 6-2 |
| Token-Ring Network | 6-3 |
| The Token-Ring Adapter in the 3745 | 6-9 |
| Token-Ring Interface Coupler (TIC) Card | 6-11 |
| Token-Ring Multiplexor (TRM) Card | 6-15 |
| TRA Resets | 6-19 |
| Error Detection and Reporting | 6-20 |
| Problem Determination Aid | 6-28 |
| Chapter 7. Channel Adapter (CA) | 7-1 |
| Channel Adapters in the 3745 Model 130/170 Data Flow | 7-2 |
| Introduction | 7-3 |
| CA Operating Environment | 7-7 |
| Overall Operation | 7-8 |
| Autoselection | 7-11 |
| Cycle Steal | 7-13 |
| CA/MOSS Connection | 7-14 |
| Interrupt Requests | 7-15 |
| Two-Processor Switch (TPS) | 7-16 |
| Channel Stop | 7-20 |
| Interface Disconnect | 7-20 |
| I/O Error Alert | 7-20 |
| Testing and Checking Hardware | 7-21 |
| CA Initialization | 7-23 |
| Chapter 8. Maintenance and Operator Subsystem (MOSS) | 8-1 |
| MOSS Unit in the 3745 Model 130/150/170 Data Flow | 8-2 |
| Introduction | 8-3 |
| MOSS Reset | 8-4 |
| MOSS Functions | 8-6 |
| MOSS States | 8-7 |
| Branch Trace | 8-9 |
| Mailbox Description | 8-11 |
| LSSD Operation | 8-15 |
| MOSS/Disk Drive Interaction | 8-17 |
| MOSS/Operator Console Connections | 8-18 |
| Chapter 9. Control Panel, Operator Consoles, Disk/Diskette Drives | 9-1 |
| Control Panel | 9-2 |
| Operator Consoles | 9-6 |
| Disk/Diskette Drive | 9-9 |
| Chapter 10. Power System | 10-1 |
| The Power System in 3745 Data Flow | 10-2 |
| Introduction | 10-3 |

| | |
|--|----------|
| AC Voltages Input | 10-4 |
| Power Control Subsystem | 10-14 |
| Power Mode of Operation | 10-19 |
| Power ON/OFF Sequence | 10-21 |
| Power ON Reset (POR) | 10-28 |
| Chapter 11. Error Logging | 11-1 |
| Introduction | 11-4 |
| BER Generalities | 11-6 |
| BERs Which Are Not Machine Errors | 11-12 |
| Specific Mechanisms | 11-13 |
| AutoMaint | 11-17 |
| BER Recovery Procedures | 11-25 |
| Unresolved Interrupts | 11-26 |
| MOSS Error Logging | 11-30 |
| MOSS BERs Used With the IPL Application | 11-34 |
| Diagnostics BER Type 03 | 11-106 |
| Power BER Type 04 | 11-108 |
| NCP CA BER Type 10 | 11-115 |
| NCP TSS/HPTSS BER Type 11 | 11-127 |
| NCP/PEP BER, Type 12 | 11-138 |
| NCP CCU BER Type 13 | 11-141 |
| NCP IOC BER Type 14 | 11-145 |
| NCP TRSS BER Type 15 | 11-147 |
| List of Abbreviations | X-1 |
| Glossary | X-5 |
| Bibliography | X-7 |
| 3745 Models 130, 150, and 170 Customer Documentation | X-7 |
| 3745 Models 130, 150, and 170 Service Documentation | X-8 |
| Index | X-9 |

About This Book

This manual provides:

1. Introductory and how-to-fix information
2. Information for maintaining CSAs (Common Sub-assemblies)
3. Description of IBM 3745 Communication Controller functional units.

The console(s) and operator panel procedures are not provided in this manual, but are in the:

- *3745 Advanced Operations Guide*, SA33-0097, and *3745 Service Functions*, SY33-2069, for the maintenance functions used by service personnel.
- *3745 Basic Operations Guide*, SA33-0146, for the control panel functions.

Who Should Use This Book

This manual is intended for the product support-trained CE (PST CE) to service the IBM 3745 Communication Controller whenever the product-trained CE (PT CE) cannot repair the machine using the *Maintenance Information Procedures* manual.

The person using this *Hardware Maintenance Reference* (HMR) manual should:

- Have an understanding of the telecommunications environment.
- Be trained to service the 3745 Communication Controller.
- Be familiar with the data circuit terminating equipment (modems, autocal units, and so on) and the terminals that attach to 3745s.
- Be familiar with the host channel to which the 3745 can be attached.

Service Personnel Definitions

See *Maintenance Information Procedures* (MIP) SY33-2070, manual.

How to Use the Maintenance Library

Maintenance on the 3745 is performed only when a failure or suspected failure occurs in the machine. The customer is first expected to perform problem determination to see if a 3745 problem exists. He uses the *Problem Determination Guide* and a host or 3745 console to perform the requested procedures. The problem determination guide generally produces a reference code that the customer should provide to the Hardware Central Service (HCS)

If the HCS is contacted, they will confirm that the initial problem determination has been done correctly, and determine if a hardware failure is indicated. Where hardware replacement is required, the HCS will determine which FRU(s) should be replaced, and dispatch a CE with the information needed to identify and replace them. When replacement has been completed, the CE will test the machine as directed by the *MIP* and *Service Functions* manuals, to verify the repair.

At this point, the *Maintenance Information Procedures* portion of the 3745 Maintenance Library has been exhausted. If additional problem analysis is required, the CE should contact the HCS for assistance, since the problem may require

special tools or techniques that are described in the *Hardware Maintenance Reference* and *Service Functions* manuals, and are applied by a Product Support-Trained CE.

Where to Find More Information

See "Bibliography" page X-7.

Chapter 1. General Information

| | |
|---|------|
| 3745 in a Network | 1-2 |
| 3745 Data Flow | 1-4 |
| Identification and Capacity | 1-5 |
| 3745 Model 130 | 1-5 |
| 3745 Model 150 | 1-5 |
| 3745 Model 170 | 1-5 |
| Controller Structure | 1-6 |
| Control Subsystem (CSS) | 1-6 |
| Communication Subsystem | 1-7 |
| Low-/Medium-Speed Transmission Subsystem (TSS) | 1-8 |
| High-Performance Transmission Subsystem (HPTSS) | 1-11 |
| Token-Ring Subsystem (TRSS) | 1-12 |
| Maintenance and Operator Subsystem (MOSS) | 1-13 |
| Programming Support and Network Management | 1-17 |
| Host-Resident Programs | 1-17 |
| Controller-Resident Programs | 1-19 |
| Generating and Loading the Control Program | 1-20 |
| Using the Library for Service | 1-21 |
| Remote Service from Hardware Control Service | 1-21 |
| On Site Service | 1-22 |
| Maintenance | 1-23 |
| Preventive Maintenance | 1-23 |
| Maintenance Philosophy | 1-23 |
| Maintenance Aids | 1-23 |

3745 in a Network

The 3745 can be:

- 1 Channel-Attached** (via channel adapter) to one or more hosts.
- 2 Link-Attached** (via telecommunication facilities) to a host through another IBM Communication Controller (allowing the 3745 to be used as a remote concentrator).

Then, the 3745 allows simultaneous connection to:

- a. Other IBM communication controllers, via high-speed lines (such as T1 or CEPT) and their associated DCEs.
- b. Other IBM communication controllers, via medium- or high-speed lines and their associated DCEs.
- c. Local clusters and terminals, directly attached without DCE.
- d. Remote clusters and terminals, via stand-alone DCEs and telecommunication facilities (switched or non-switched).
- e. Remote communication controllers/clusters/terminals via X.25 public data networks.
- f. Remote communication controllers/clusters/terminals via integrated DCEs and 4-wire nonswitched telecommunication facilities or DDS network in the US.
- g. Communication controllers/clusters/terminals on IBM token-ring local area networks.

See Figure 1-1 on page 1-3.

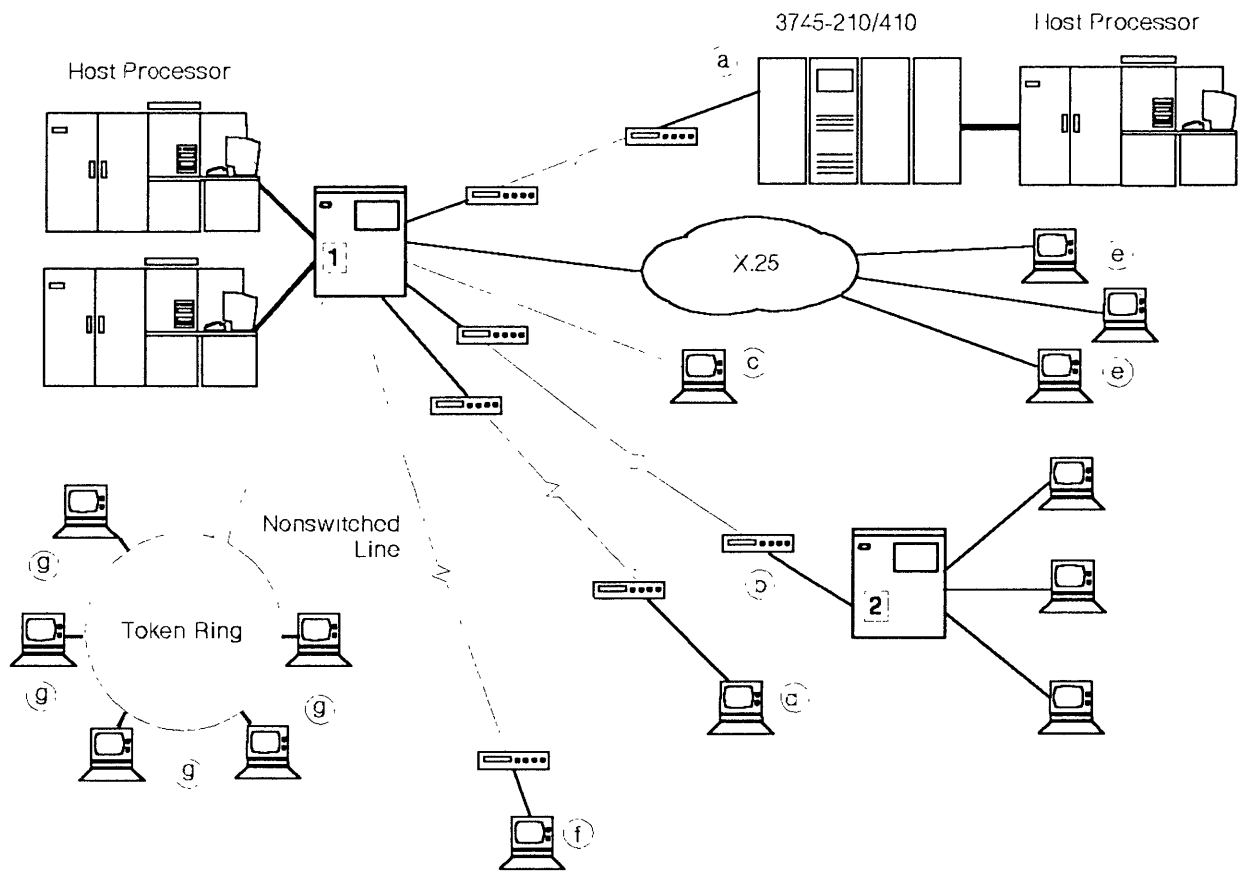
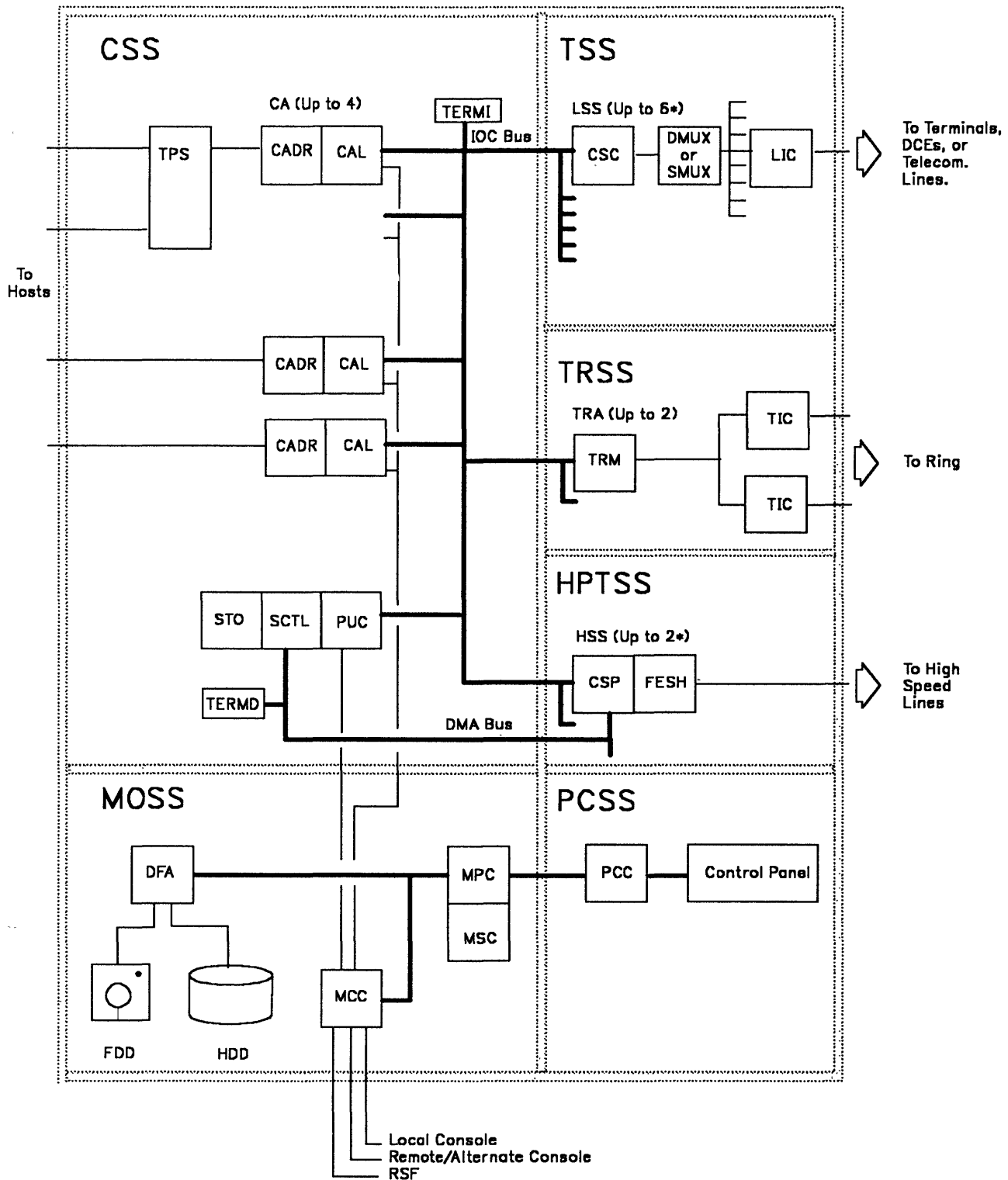


Figure 1-1 3745 in a Network

3745 Data Flow



Identification and Capacity

Note: All the following connection capabilities might not be present at the same time as some items are mutually exclusive (see *3745 Configuration Program*, GA33-0093).

3745 Model 130

- 4 CAs
- 0 low-speed scanner (LSS)
- 2 High-speed scanners (HSS)
- 2 Token-ring adapters (TRA).

3745 Model 150

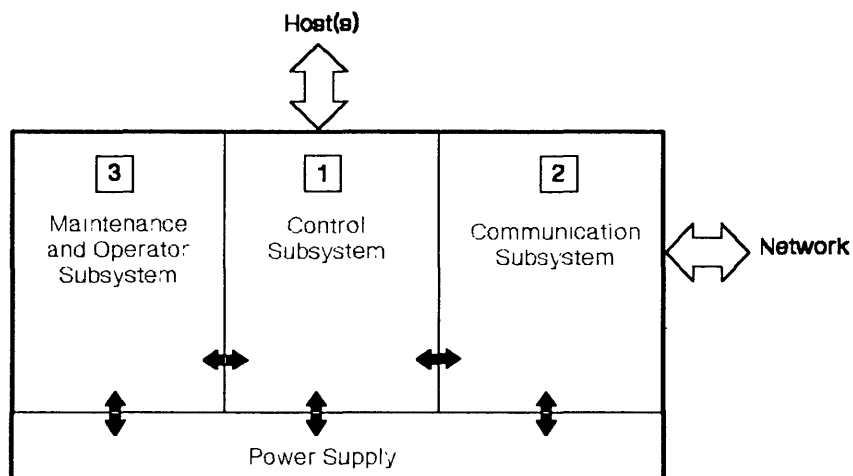
- 0 CA
- 1 low-speed scanner (LSS)
- 1 High-speed scanner (HSS)
- 1 Token-ring adapter (TRA)
- 32 Low-/medium-speed lines
- 16 integrated DCEs 14.4 kbps
- 3 integrated DCEs 56 kbps.

3745 Model 170

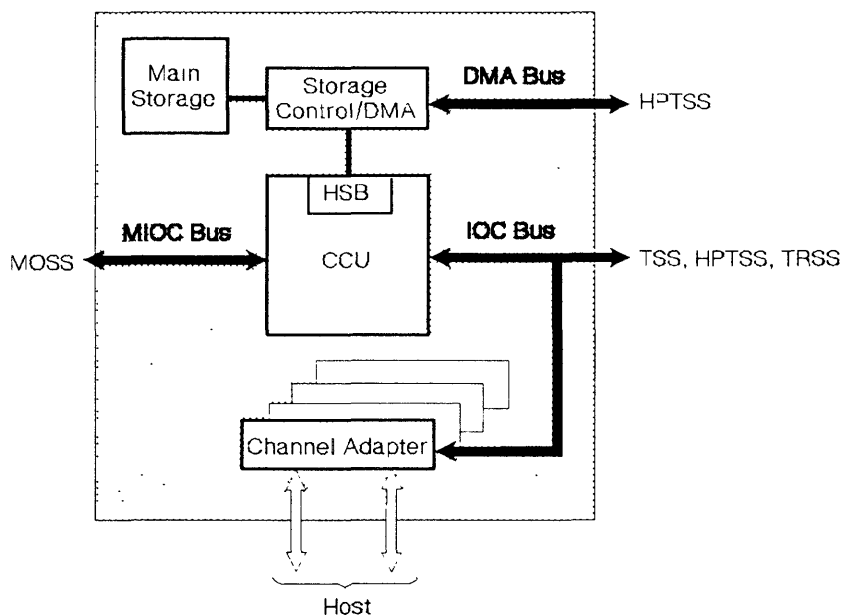
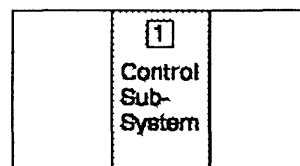
- 4 CAs
- 6 low-speed scanners (LSS)
- 1 Token-ring adapter (TRA)
- 2 High-speed scanners (HSS)
- 96 Low-/medium-speed lines
- 32 Integrated DCEs 14.4 kbps
- 8 Integrated DCEs 56 kbps.

Controller Structure

The 3745 consists of four functional areas:



Control Subsystem (CSS)



The control subsystem contains:

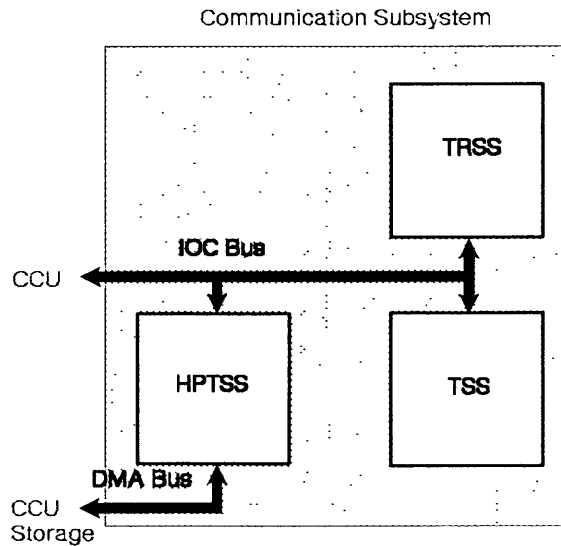
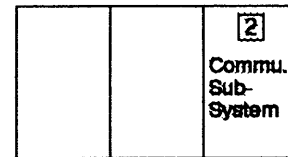
- The central control unit (CCU), with its associated high-speed buffer (HSB).
- The main storage.
- The storage control, equipped with a direct memory access (DMA).

- The channel adapters, eventually associated with two-processor switches (TPS).

Two types of channel adapter are available:

- Channel adapter type 6: Channel adapter data streaming (CADS)
- Channel adapter type 7: Buffer chaining channel adapter (BCCA).
- The input/output control bus (IOC bus).
- The DMA bus.
- The MOSS input/output control bus (MIOC bus).

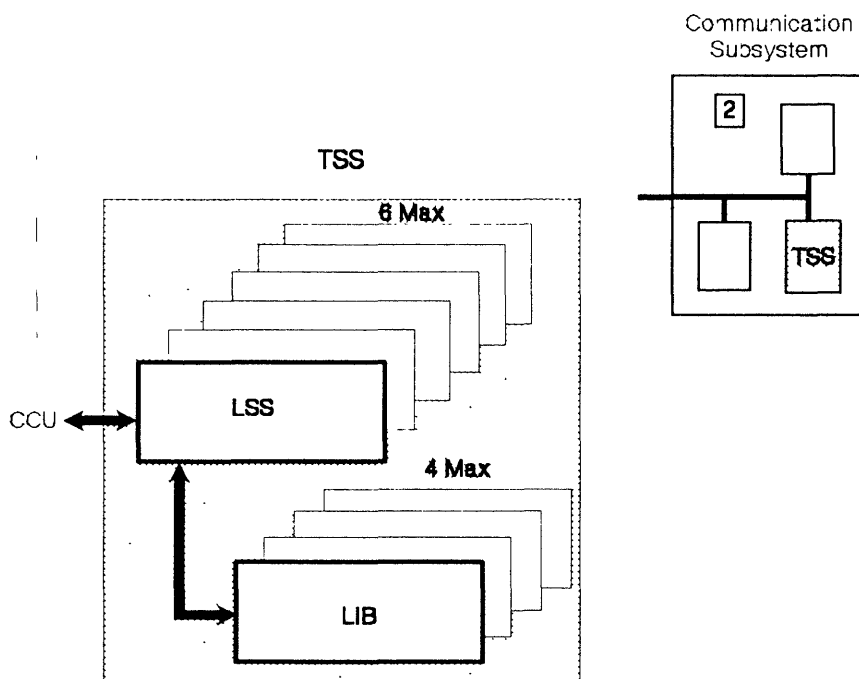
Communication Subsystem



Three types of line connection are used to connect data communication lines:

- The low-/medium-speed transmission subsystem (TSS).
- The high-performance transmission subsystem (HPTSS).
- The token-ring subsystem (TRSS).

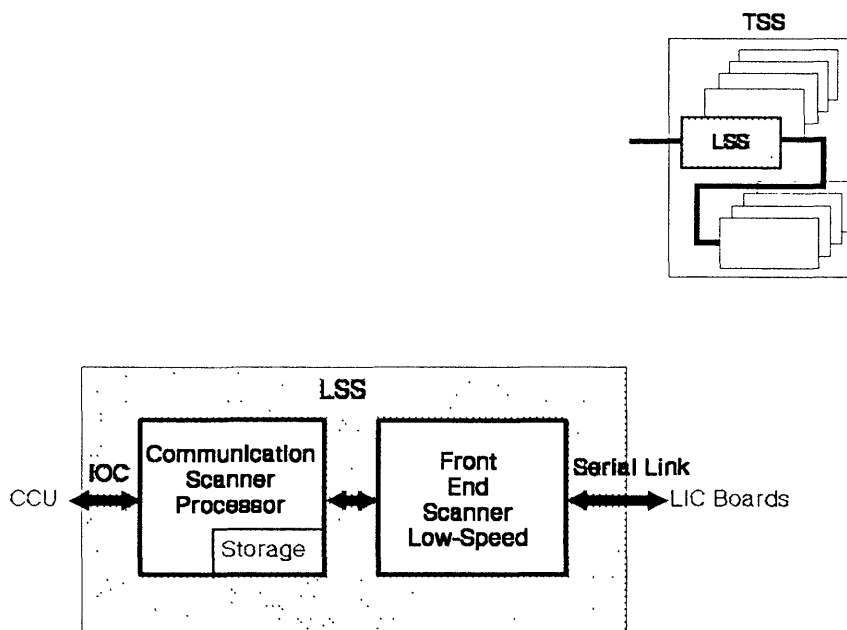
Low-/Medium-Speed Transmission Subsystem (TSS)



The TSS consists:

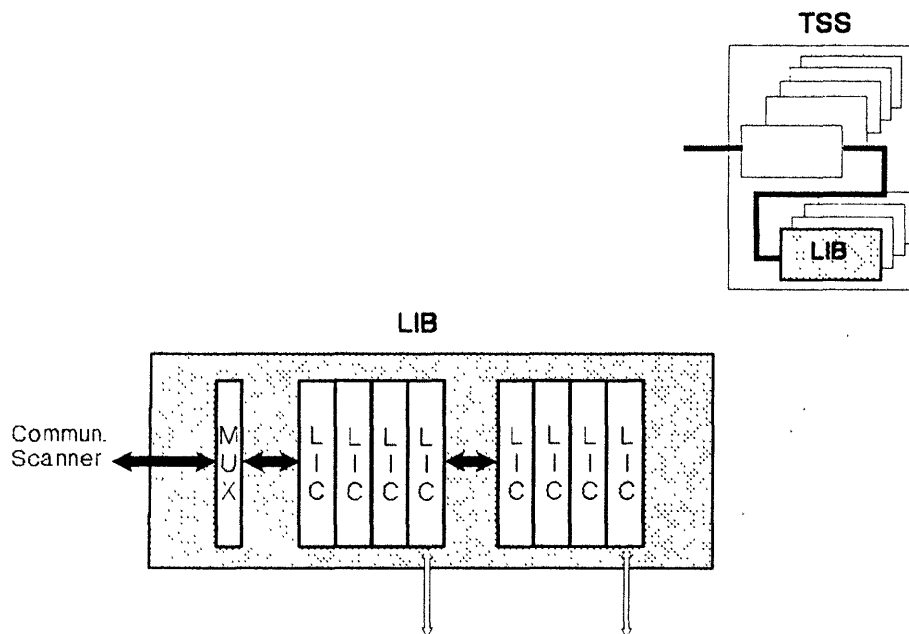
- Up to six low-speed scanners (LSS)
- Up to four LIC boards (LIBs).

Low-Speed Scanner



A low-speed scanner consists of one card housing a communication scanner processor (CSP) associated to a front-end scanner low-speed (FESL).

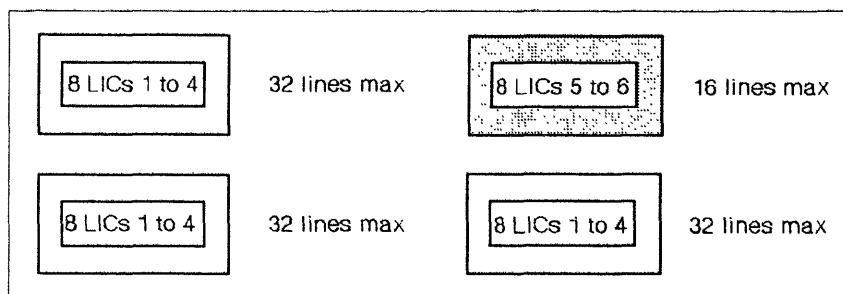
LIC Board (LIB)



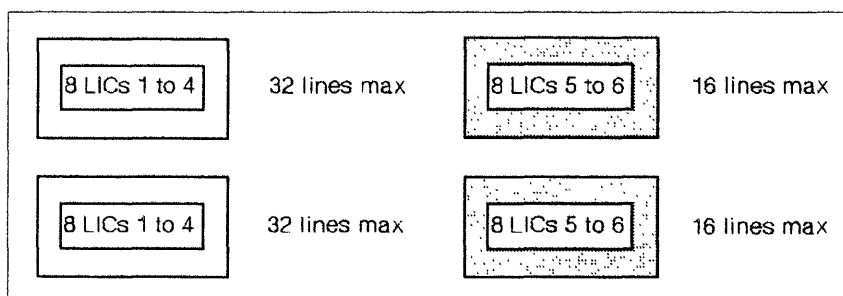
There are up to four LIC boards (LIB).

Each LIB houses:

- One multiplexer (MUX) and
- Up to eight line interface couplers (LICs).



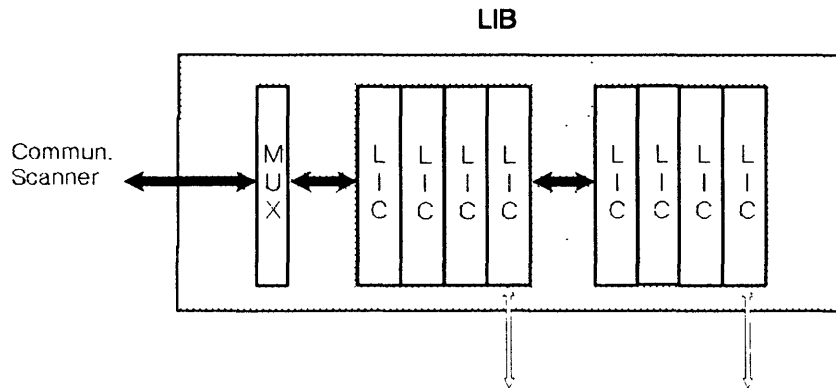
or



Three types of LIB can be installed:

- LIC board type 1 (LIB1) on 3745 models 150 and 170. LIB1 houses up to 8 LICs type 1-4.
- LIC board type 2 (LIB2) on 3745 models 150 and 170. LIB2 houses up to 8 LICs type 5-6.
- LIC board type 3 (LIB3) on 3745 model 150. LIB3 houses up to 4 LICs type 1-4.

Line Interface Couplers (LICs)



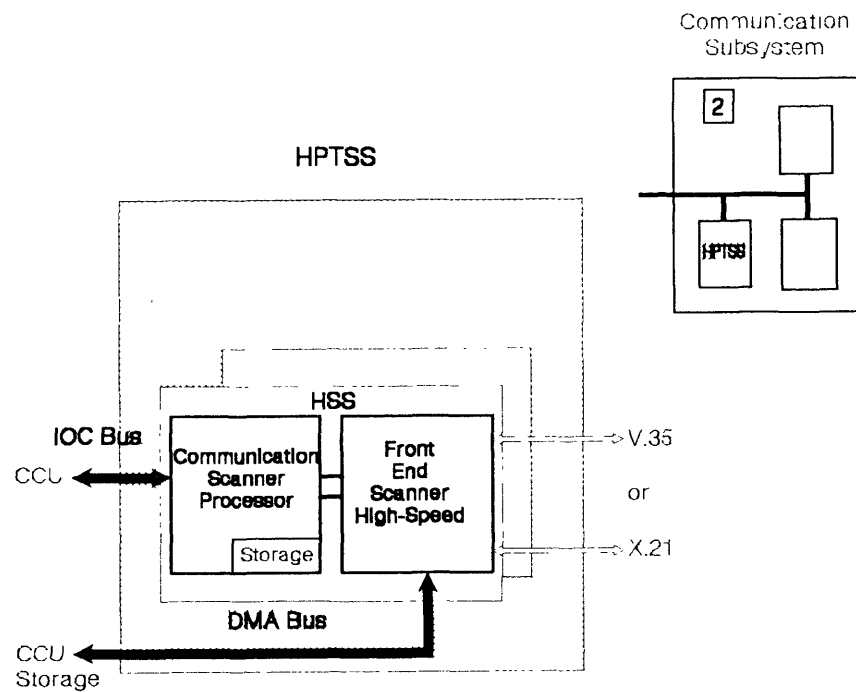
There are six types of LIC, namely:

- **LIC1, LIC3, LIC4A and LIC4B** for attaching to:
 - Local direct-attached terminals (no DCEs)
 - Remote terminals via standalone DCEs and telecommunication facilities.

An internal clock function (ICF) is available on these LICs to provide clocking signals to non-clocked DTEs or DCEs.

- **LIC5 and LIC6**, both housing integrated DCEs providing direct access to the telecommunication facilities for attaching to remote terminals.

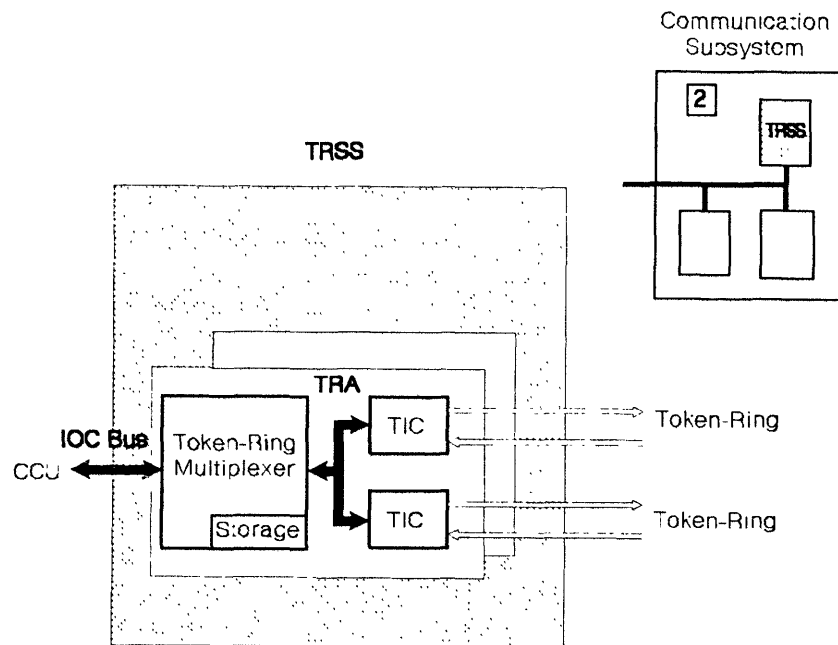
High-Performance Transmission Subsystem (HPTSS)



The HPTSS consists of up to two high-speed scanners (HSS).

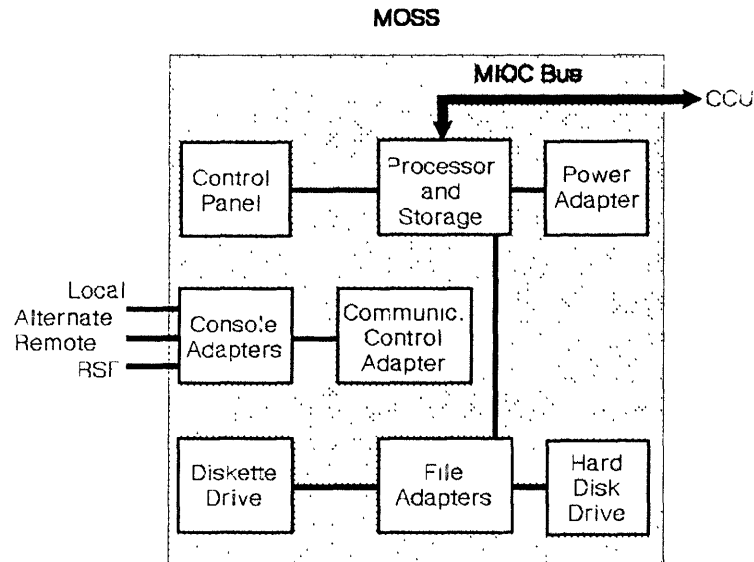
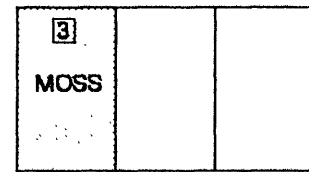
Each HSS consists of a communication scanner processor (CSP) card, associated with a front-end scanner high-speed (FESH) card.

Token-Ring Subsystem (TRSS)



The TRSS consists of one token-ring multiplexer (TRM) driving two token-ring interface couplers (TICs) providing access to two IBM token-rings operating at 4 or 16 Mbps.

Maintenance and Operator Subsystem (MOSS)



The MOSS provides:

- Powerful procedures for the 3745 initialization and IPL functions.
- Host-independent product maintenance and rapid isolation and repair of failures within the controller.
- Easy problem determination procedures for the operator.

The MOSS also provides:

- Controller initialization, IML and IPL control
- Automatic IPL and dump operations
- Operating mode management
- Line configuration management
- Controller supervision
- Controller concurrent diagnostic
- Online event recording and error notification including for the integrated DCEs
- Problem determination (error in the network including the controller)
- Failure isolation and repair (error in the controller)
- Remote support facility link management.

The MOSS continuously monitors the status of the communication controller. Abnormal conditions are analyzed and reported via alarms to the 3745 console(s) and alerts to the network control console.

Among the components of the communication controller, multiple adapters allow the MOSS to monitor the status of the CCU, control DMA, and IOC bus, and to enable and disable channel adapters.

A power control adapter with a dedicated microprocessor monitors 3745 power.

A file adapter provides MOSS storage control. A 72MB hard disk, in addition to a 3.6MB diskette, provides extensive capacity for file and data storage.

The MOSS interfaces to the control panel indicators and switches. These provide an alternative method for controlling the primary power subsystem, activating MOSS functions, and for operator notification.

A console adapter allows 3745 to be controlled from a local console located within 7 m (23 ft), or an alternate console located within 120 m (400 ft), or a remote console connected via a 1200 bps DCE to the controller. Only one console may be active at a time. If the remote support facility is used, it allows communication between the MOSS and the IBM RETAIN system, providing remote service facility (RSF). The RETAIN terminal can be used as an operator console as well as for transferring microcode patches to the MOSS if required.

Operator Consoles and Remote Support Facility

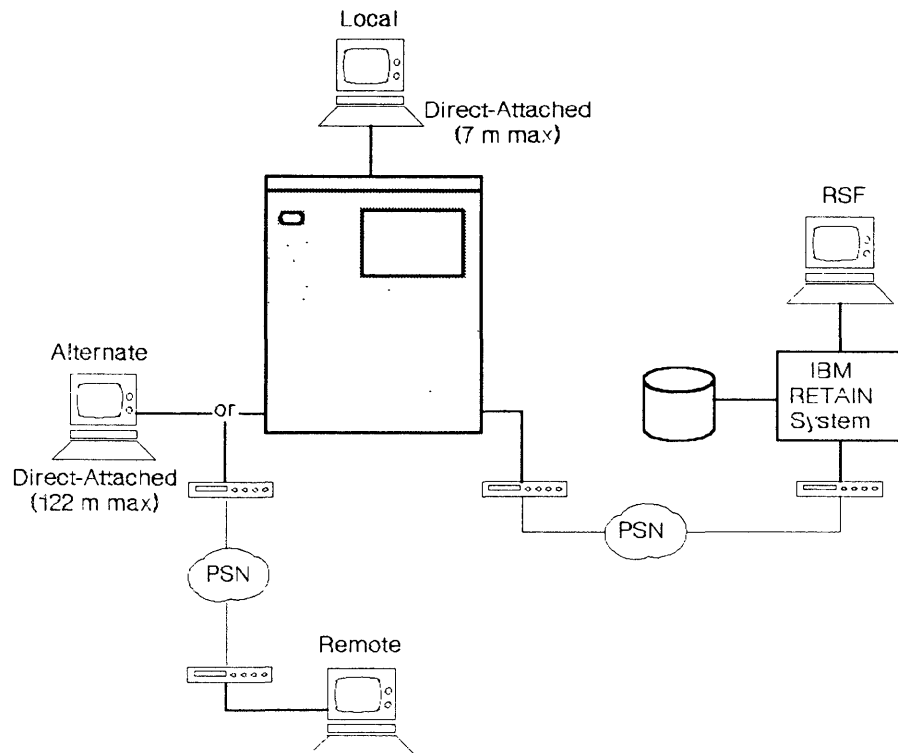
An operator console is required for:

- Installation
- Operation
- Maintenance.

The 3745 provides attachment for three different types of consoles:

- A **local** console, which is mandatory, and
- A **remote** or an **alternate** console.

It also provides attachment for the **remote support facility (RSF)**. The consoles and RSF are connected to the MOSS via a common communication adapter.



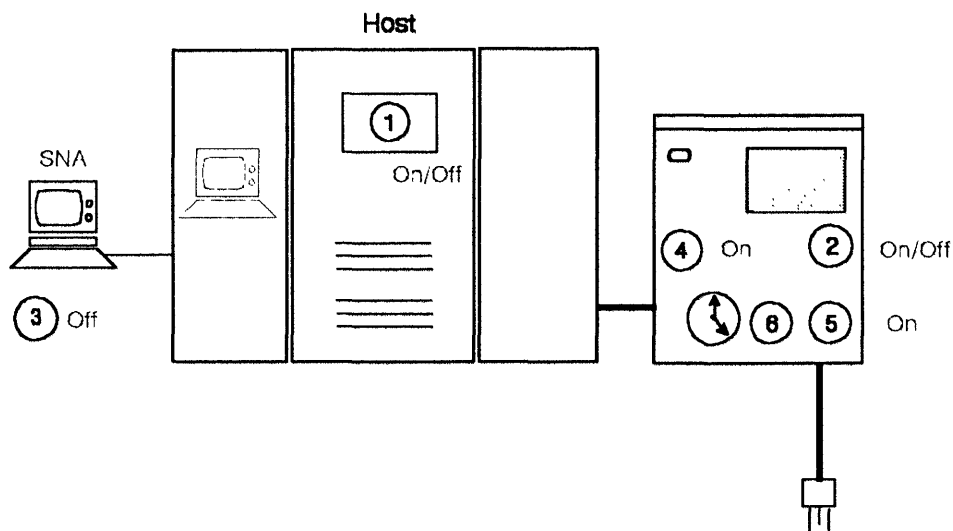
Only one console can be active at a time.

Three types of password enable access to the MOSS from a local, remote or alternate console, and for remote IBM maintenance (via RSF).

Power ON/OFF

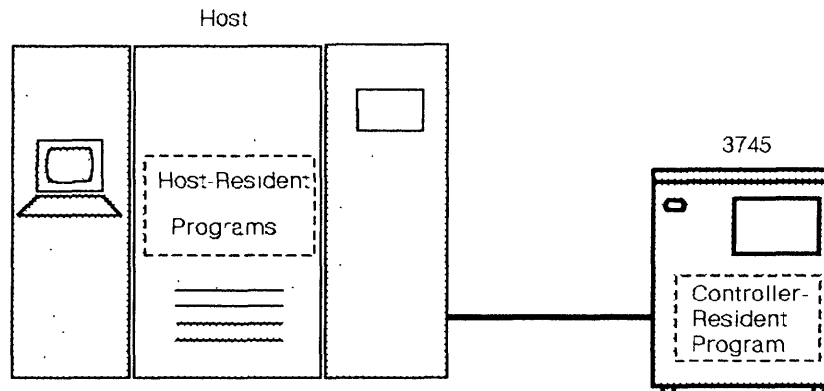
The 3745 can be:

1. Powered ON and OFF by a channel-attached host.
2. Powered ON and OFF locally by the operator.
3. Powered ON by the operator and OFF by a remote SNA command.
4. Powered ON through the scheduled power ON MOSS function.
5. Re-powered ON automatically by the auto-restart function after a power outage.
6. Re-powered ON automatically by a retry function after a power supply or fan problem.



Programming Support and Network Management

The 3745 operates under the control of IBM licensed programs:



Host-Resident Programs

Operating Systems

- MVS*/370
- MVS/XA
- VM/SP
- VM/SP HPO
- VM/XA
- VSE*/AF
- VSE/SP.

Access Methods

Normal Mode:

- Virtual Telecommunications Access Method (VTAM*).

Emulation Mode:

- Basic Telecommunications Access Method (BTAM)
- BTAM Extended Support (BTAM-ES)
- Remote Terminal Access Method (RTAM).

System Support Programs

- Advanced Communications Function for System Support Programs (SSP) in an MVS environment,
- Advanced Communications Function for System Support Programs in MVS, VM, and VSE environments.

SSP is used to generate the 3745 control program.

In addition, SSP provides utilities for loading, dumping, and tracing the 3745 control program.

It also supports:

- Dump transfer of the 3745 storage to the host.
- Dump printing at the host.
- 3745 disk file transfer to the host.

Network Management

The 3745 network management is supported by the NetView* program. By monitoring and managing the controller and its resources, and by diagnosing problems, this program contributes to the optimization of the 3745.

It integrates functions of several network management products and VTAM functions, for example:

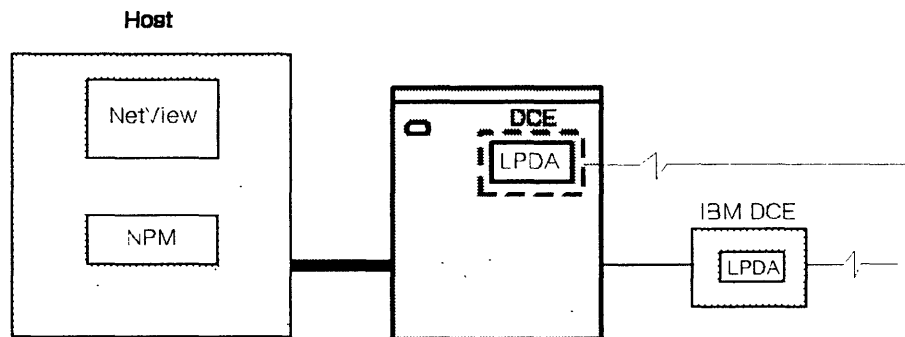
- A command facility, which lets the user control, record, and automate various operator tasks. It can be used as an operator's interface to VTAM in a data communication network.
- A session monitor, which enables the user to examine, from a central control point, information related to the SNA network and to identify network problems.
- A hardware monitor, which helps the user to get problem determination information that is generated at resources that are either link-attached or channel-attached to the host system.

As a cohesive set of SNA host network management services, the NetView program offers:

- Consistency and usability in its support for network management
- Easy installation procedure
- Device support
- Operator usability.

The 3745 supports:

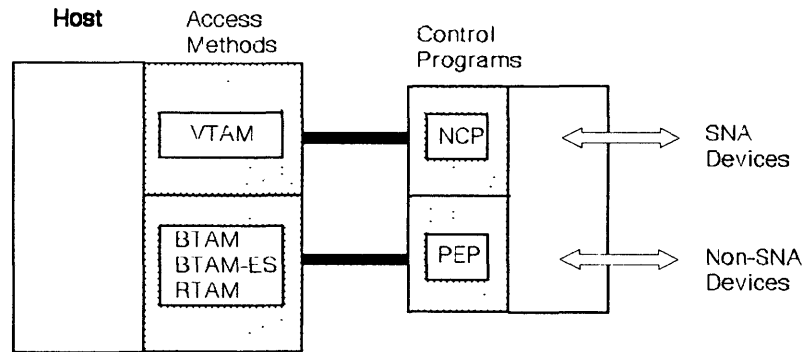
- Link Problem Determination Aid (LPDA*) facilities provided by IBM DCEs.
- NetView Performance Monitor (NPM) under VM and MVS.



Controller-Resident Programs

The 3745 runs under control of one of the following:

- Advanced Communications Function for Network Control Program (NCP) to support SNA devices.
- Emulation programming (EP) to support non-SNA devices.



- Partitioned emulation programming (PEP) extension of NCP to support SNA and non-SNA devices.

Network Control Program (NCP)

NCP provides major capabilities for SNA networks with synchronous data link control (SDLC).

Start-stop and binary synchronous terminals and existing networks can be migrated to a 3745 with the IBM Network Terminal Option (NTO) program. For start-stop protocols, NCP supports a variety of transmission codes including ASCII, EBCDIC, EBCD, and BCD. Additionally, it supports a correspondence code for which it provides translation from and to EBCDIC. For the BSC protocol, this support and translation operation is performed by the scanners.

NCP includes the token-ring interconnection functions.

NCP coexists with the following IBM licensed programs:

- Network Routing Facility (NRF)
- Network Terminal Option (NTO)
- X.25 NCP Packet Switching Interface (NPSI)
- X.25 SNA Interconnection (XI)
- X.21 Short Hold Mode/Multiple Port Sharing (X.21 SH/MPS).

Partitioned Emulation Programming Extension

The partitioned emulation programming (PEP) extension of the NCP allows the Network Control Program and the Emulation Program to coexist in the same 3745. The PEP lets the NCP operate certain lines in network control mode while operating others in emulation mode.

The PEP can run only in a channel-attached controller. Channel attachment must be a byte-multiplexer channel, where one emulated subchannel address is specified per EP line.

The PEP emulates most of the functions of the IBM 2701 Data Adapter Unit, IBM 2702 Transmission Control, or IBM 2703 Transmission Control and can communicate with various access methods running in the host. Most programs written for these machines can operate in a 3745 without modification. However, programs that involve timing or special hardware considerations may have to be changed.

Generating and Loading the Control Program

SSP is used on the owning host to generate the control program load module and to load it into the controller storage. The control program for the controller is generated from standard program modules of the NCP library using the NCP definition facility (NDF) procedure. The control program must reflect the required controller configuration. Several control programs can be generated to handle different subsets of lines attached to the same controller.

Multiple Load Module

The network operator can transfer and save one or two CCU load modules onto the integrated hard disk. Either load module can be used at controller initialization.

Automatic Control Program Load

VTAM and the 3745 MOSS allows the automatic IPL/dump capability. For an automatic IPL from the controller disk, the network operator must have assigned this option during NCP loading.

Coexistence and Migration

The 3745 running under NCP can coexist with other IBM communication controllers.

The 3745 supports networks based on the earlier IBM 2701 Data Adapter Unit, IBM 2702 Transmission Control, or IBM 2703 Transmission Control. It also supports networks in which these units are emulated on a 3725 and the 3745 via PEP. PEP permits migration from the 2701, 2702, 2703, and IBM 3704, 3705, 3720, and 3725 communication controllers that run EP.

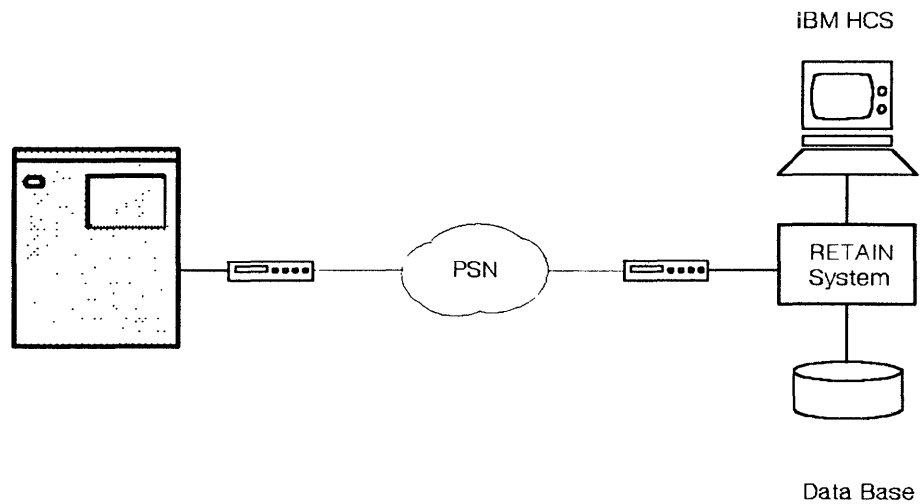
The IBM Transaction Processing Facility program is supported by NCP.

Configurations with EP only, the IBM Network Extension Facility (NEF), or the IBM Non-SNA Interconnection (NSI) are supported.

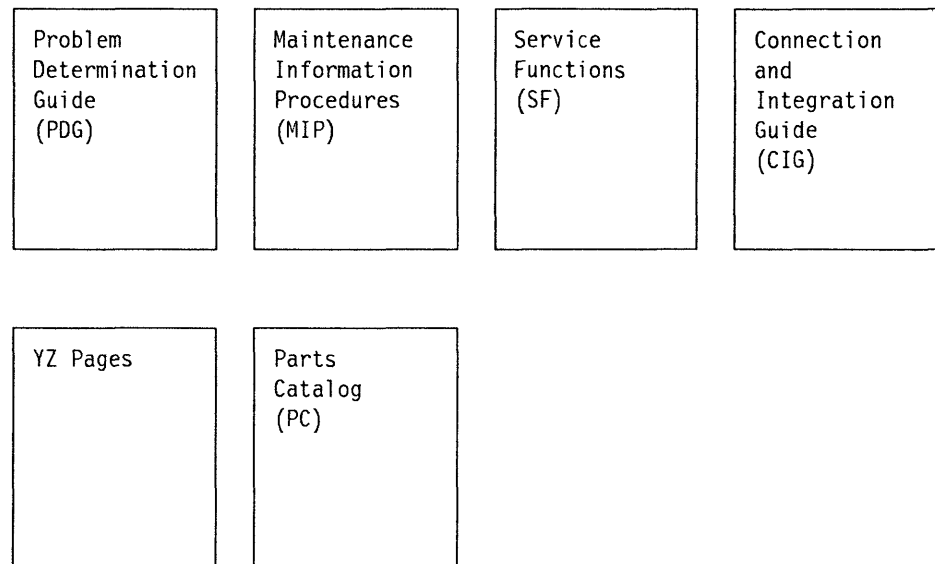
The 3745 offers a path for conversion from existing systems and for continuing growth. A system designed for the IBM 3725 or 3720 may be applied to the 3745 after regeneration of the control program. The control program generation deck that was used in the 3725 or 3720 program generation can be used with some modifications to statements (assuming that the controller has the same line configuration).

Using the Library for Service

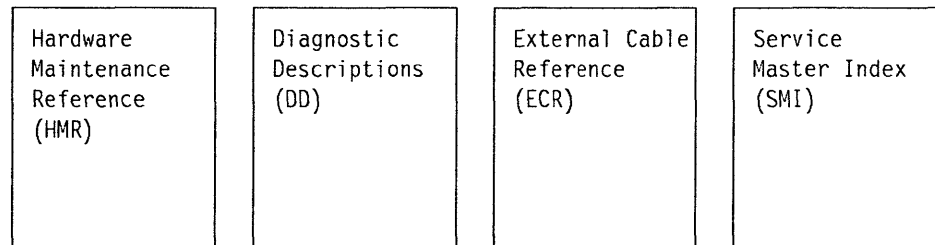
Remote Service from Hardware Control Service



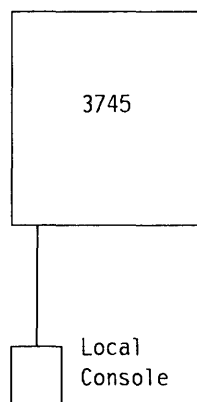
Documentation Used by the PTCE:



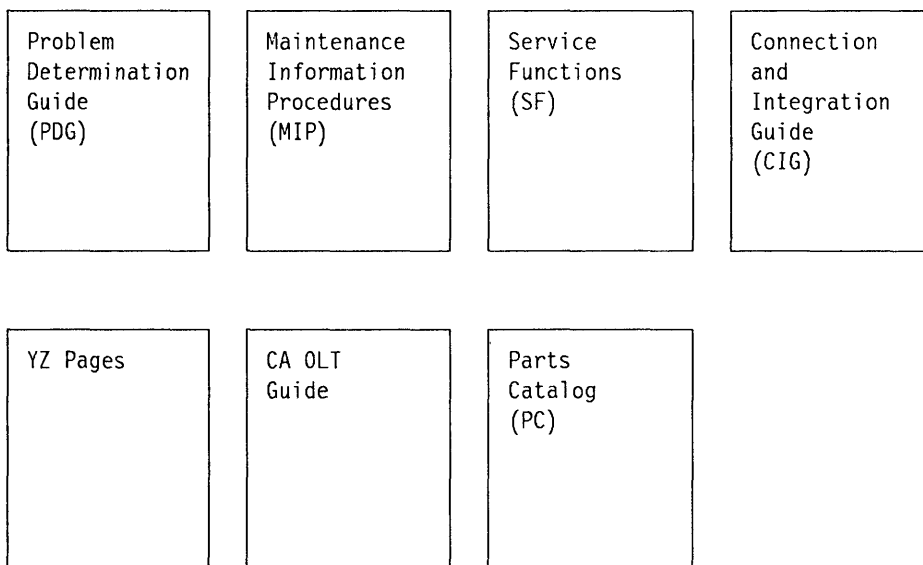
Documentation Used by the PSTCE: Same as PTCE, PLUS:



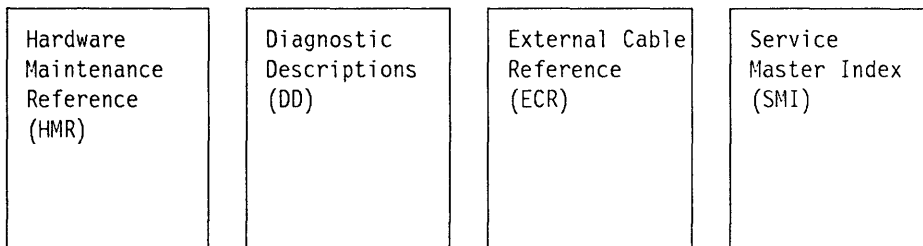
On Site Service



Documentation Used by the PTCE:



Documentation Used by the PSTCE: Same as PTCE, PLUS:



Maintenance

Preventive Maintenance

The battery is replaced by maintenance personnel.

An alert notifies the customer for battery replacement, and provides the CE with a reference code.

The *Maintenance Information Procedures (MIP)*, SY33-2070, guides the maintenance personnel for replacement procedures.

Maintenance Philosophy

The *MIP*, Chapter 1 "Introducing the IBM 3745 Communication Controller."

Maintenance Aids

Tools and Test Equipment

The *MIP*, Chapter 1 "Introducing the IBM 3745 Communication Controller."



Chapter 2. Central Control Unit (CCU)

| | |
|---|------|
| The CCU in 3745 Data Flow | 2-2 |
| General Description | 2-3 |
| Data Flow | 2-3 |
| Packaging | 2-3 |
| Functional Description | 2-4 |
| Program Levels | 2-4 |
| Interrupts | 2-5 |
| Instruction Set | 2-9 |
| CCU Environment | 2-11 |
| CCU Subsystem Power-ON Reset (POR) | 2-12 |
| Main Storage | 2-12 |
| Storage Environment | 2-13 |
| Direct Memory Access and Storage Control (SCTL) | 2-13 |
| CCU-to-Storage Interconnection | 2-16 |
| Cache Storage | 2-16 |
| Storage Protection | 2-17 |
| CCU Timers | 2-18 |
| CCU to and from Adapters | 2-19 |
| IOC Control Logic | 2-19 |
| IOC Data Flow | 2-19 |
| Registers | 2-20 |
| Hardware Registers | 2-38 |
| CCU to and from MOSS | 2-39 |
| CCU Diagnostics | 2-40 |
| CCU Error Handling | 2-40 |
| CCU Error Detection | 2-42 |
| Performance Test Points | 2-46 |

The CCU in 3745 Data Flow

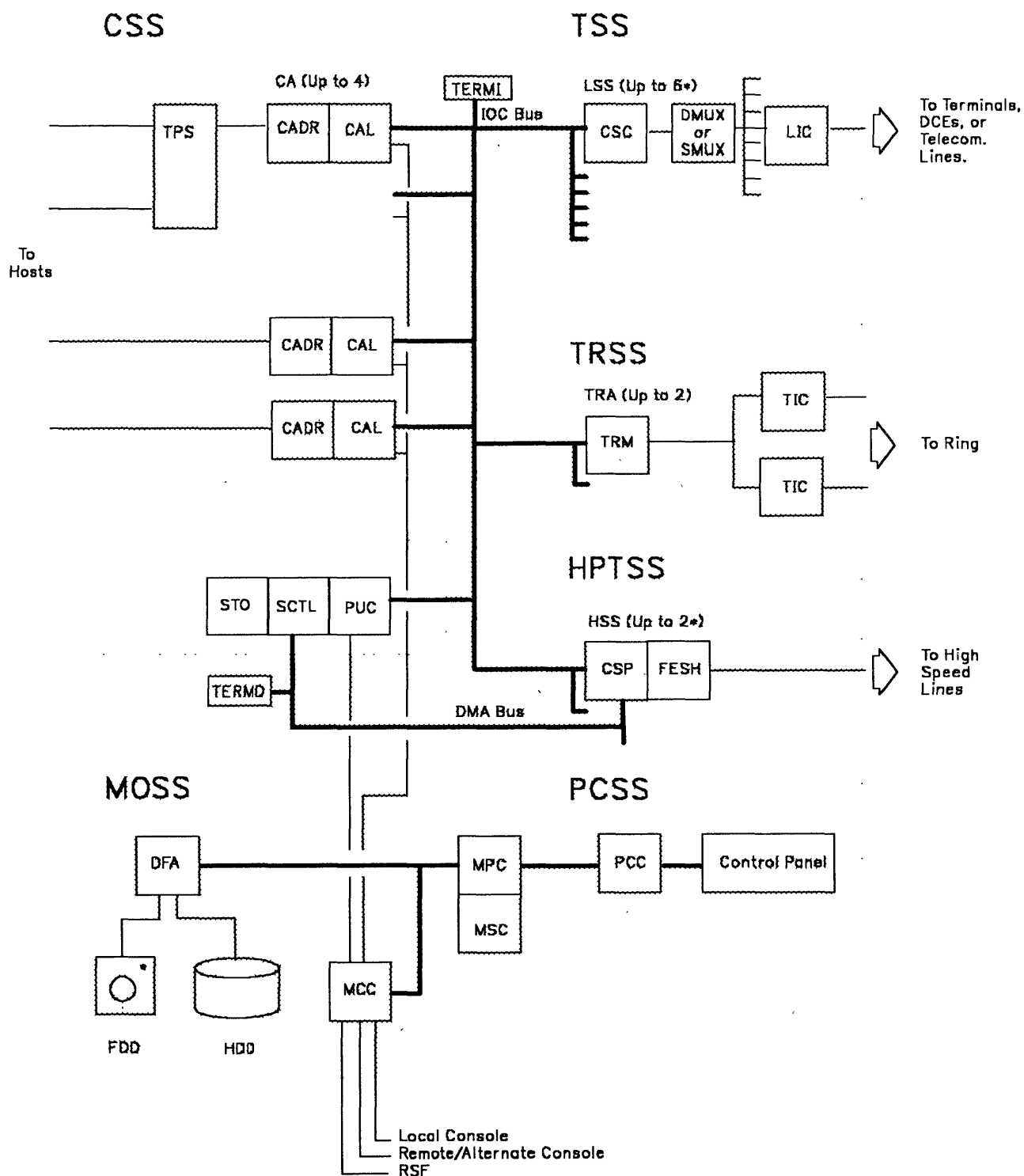


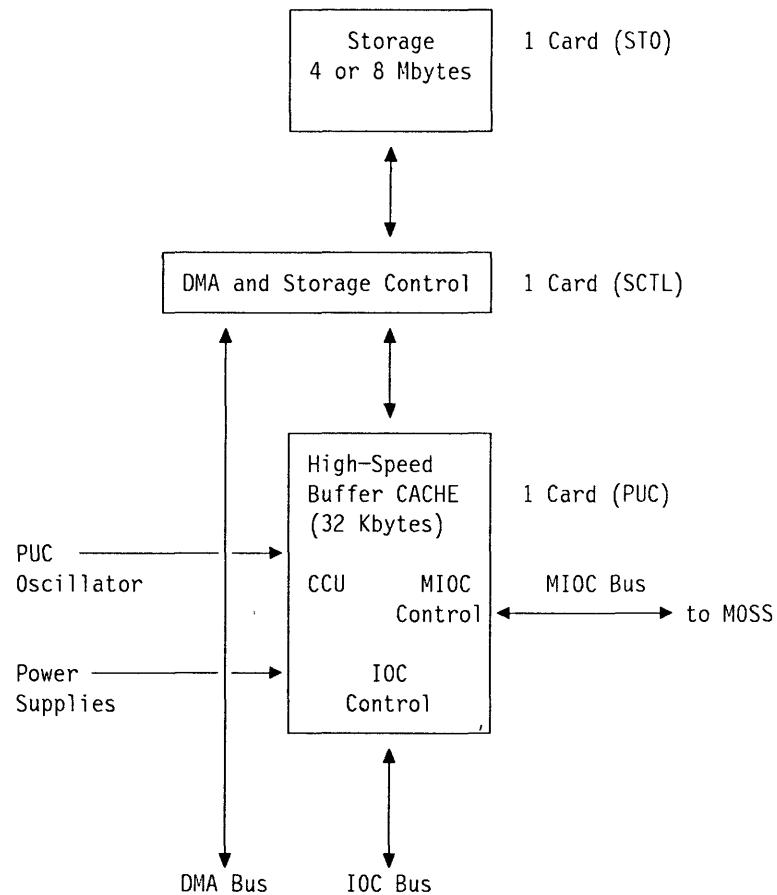
Figure 2-1. The CCU in 3745 Data Flow

General Description

The 3745 is equipped with one CCU.

Data Flow

CSS



Packaging

See YZ pages for locations.

The communication subsystem (CSS) includes the following components:

- Processor unit card (PUC)
- Storage basic card (ST0) 4 or 8 Mbytes
- Storage control card (SCTL).

Functional Description

The central control unit (CCU) is an interrupt-driven processor with a stored program called the 'control program' (CP) in this manual, that controls the data transfers on the channel and transmission interfaces.

The CCU:

- Executes the machine instruction set (CCU cycle = 131.6 ns) to perform arithmetic or logical operations, exchange data between main storage and the work registers, and also between the local store and the work registers.

Data transit between the CCU and main storage is achieved via a high-speed buffer (CACHE) under the control of the SCTL logic.

Data can also transit directly between main storage and high-speed adapters via the direct memory access (DMA) logic.

- Communicates with adapters through the input or output control IOC logic in program-initiated operations (PIO) or in adapter input or output operations (AIO) mode:

PIO mode: The exchange operation is initiated by input or output halfword (IOH) or input or output halfword immediate (IOHI) instructions in the CCU.

AIO mode: The operation uses cycle steal for data exchange between adapters and main storage without control program intervention.

One bus (IOC) gives access to the adapters' environment.

- Communicates with the MOSS through the MOSS IOC (MIOC). The operations performed can be direct or indirect (MIOH/MIOHI).

MOSS uses the CCU level sensitive scan design (LSSD) to read or write any CCU discrete latch.

Program Levels

The controller hardware has five operational program levels:

Program level 1

This is the highest priority program level. Interrupt requests assigned to level 1 include all critical check conditions such as CCU checks, program checks, addressing exceptions, and adapter checks. Initial program load (IPL) and address compare interrupts are also handled in this level.

Program level 2

Normal operational interrupt requests from the communication adapters are assigned to this program level and certain program controlled interrupts (PCIs) are also assigned to this level.

Program level 3

Normal operational interrupt requests from the channel adapters, interval timers and program-controlled interrupt 3 (PCI) requests and panel interrupts are assigned to this level.

Program level 4

Certain program controlled interrupt (PCI) requests and the supervisor call (SVC) request (generated when the exit instruction is executed at program level 5), and MOSS request service and request response are assigned to this interrupt program level. This level is the lowest priority interrupt level.

Program level 5

This level is the lowest priority level and is normally active when none of the other four levels requires program cycles.

Masking Program Level Priorities

Programs at levels 1, 2, 3, or 4 can mask all interrupt requests for program levels 2, 3, or 4 and can mask adapter interrupt requests for level 1. Moreover, program execution in level 5 can be masked.

The normal operational priority structure can be changed by output instructions X'7E' and X'7F' (set or reset mask register).

When the mask is set for one or more of program levels 2, 3, or 4, interrupt requests for those levels will not cause an interrupt. When the mask is set for program level 1, requests by adapters for level 1 will not cause an interrupt though any other request will be honored.

When the mask for level 5 is set, the use of machine cycles for program execution in level 5 is prevented. Thus, level 5 program execution is masked. In this case, when no program is executing in levels 1, 2, 3, or 4, the CCU enters the wait state and no program executes.

To selectively mask one or more program levels, one of the active general registers is loaded with the bits corresponding to those program levels to be masked. Output instruction X'7E' (set mask register) is then executed using the general register as input to the mask register. To selectively unmask one or more program levels, the same procedure is followed except that the output X'7F' (reset mask register) instruction is executed.

Interrupts

The communication controller operates in response to requests from either the control program (CP) or the hardware. Since these requests may have varying degrees of urgency, a priority system is used. Each program, CCU and adapter request, is assigned a particular priority level. A request for use of the controller by the control program or hardware functions is called an interrupt request.

Interrupt Mechanism

The interrupt mechanism determines when an interrupt can be handled. If the interrupt request is to be allowed, the change from the active program level to the interrupting program level takes place immediately after completion of the current instruction. If several interrupt requests having different priorities are present at the same time, the one with the highest priority obtains use of the controller. When an interrupt request is granted use of the controller, it can be interrupted in that use by another request having a higher priority.

When an interrupt occurs, instruction execution at the lower priority program level is suspended until instruction execution is completed at the higher priority level. An interrupt to a specific program level prevents future interrupt requests assigned to either that level or to lower priority program level from causing another interrupt until the servicing of the first interrupt is complete.

Interrupt Request Determination

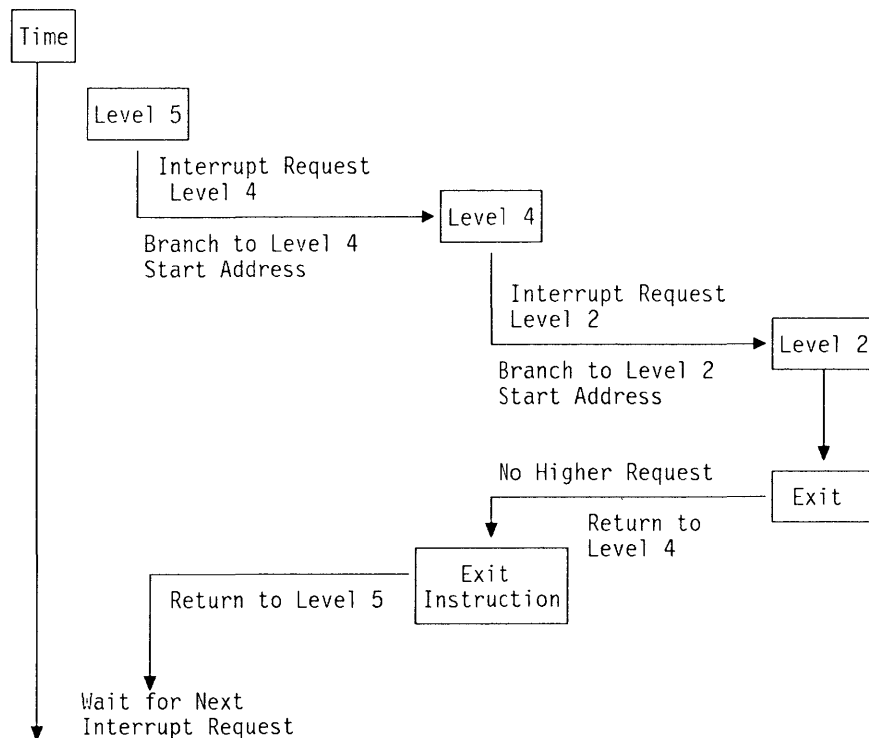
The priority of simultaneous interrupt requests assigned to the same interrupt program level is resolved by the order in which the program tests the set/reset condition of the CCU and adapter interrupt request latches.

Interrupt requests from the CCU and the adapters are grouped together according to their source for ease of identification. The set/reset condition of a specific interrupt request latch can be determined by checking the interrupt request group to which it is assigned. Input X'77' indicates the non-level 1 interrupt requests that are set by the adapters. Input X'7F' indicates the non-level 1 interrupt requests that are set by CCU or program. Input X'7E' indicates all level 1 requests. These inputs load the contents of the appropriate interrupt request group into an active general register. The program may then test the general register to identify the request.

Setting/Resetting Interrupt Requests

A particular interrupt request latch can be set as a result of a hardware-detected condition or, in some cases, by the program through the execution of an output instruction. The latch can be reset by one of several output instructions, depending upon the specific interrupt request. The procedures for setting and resetting individual adapter interrupt requests are described in the adapter sections.

For special service requests, program levels 1, 2, 3, and 4 may issue a program-controlled interrupt (PCI) request to program levels 2, 3, and 4. Output instructions X'7B' (set PCI level 2), X'7C' (set PCI level 3), and X'7D' (set PCI level 4) set the PCI interrupt requests. Certain bits in output X'77' (miscellaneous control) reset the PCI requests and other CCU interrupt requests such as the interval timer level 3 request and the supervisor call (SVC) level 4 request. If any bits are ON in registers X'77', X'7E', X'7F', a request for a particular program level is active and must be reset or masked before the program can execute in a lower level. The following example illustrates the interrupt mechanism.



Interrupt Request Sources

Interrupt Level 1

Adapter level 1 request (error)
 Address compare level 1
 Address exception level 1
 Level 5 I/O check level 1
 Protection check level 1
 Invalid operation check level 1
 IPL request level 1
 MOSS inoperative level 1
 Hard error level 1 (Note 1)
 I/O parity error
 I/O time-out error

Interrupt Level 2

Adapter level 2 request (LA)
 Program-controlled interrupt level 2
 MOSS diagnostic level 2

Interrupt Level 3

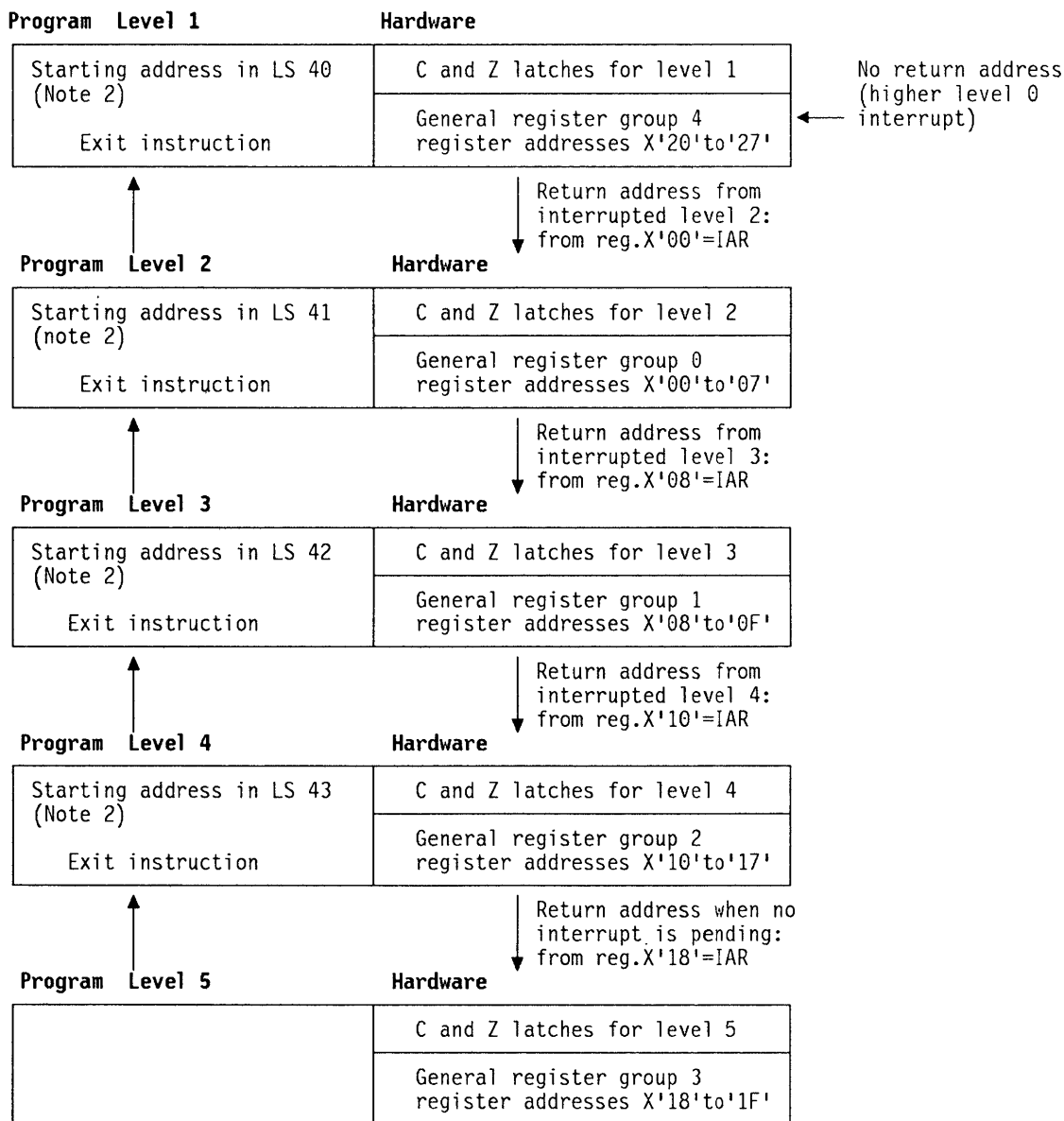
Adapter level 3 request (CA)
 MOSS diagnostic level 3
 Interval timer level 3
 Program-controlled interrupt level 3
 Panel interrupt request level 3

Interrupt Level 4

Adapter level 4 request (not used)
 Program-controlled interrupt level 4
 MOSS request SVC level 4
 MOSS request response level 4
 SVC level 4 (call from level 5)

Level 5 No interrupt (first entry)

The following figure shows the various links between the different priority levels.



Notes:

1. Hard errors stop the CCU unless it is in bypass mode.
2. The interrupt levels 1, 2, 3, and 4 starting addresses are set during IPL via output instructions X'40' through X'43'.

Instruction Set

The 3745 contains 53 executable instructions.

Any attempt at program levels 2, 3, 4, or 5 to execute an operation code other than one of the 53 specified operations results in a level 1 interrupt with the invalid operation check bit set ON in the CCU interrupt request group 1 register X'7E'.

An attempt to execute an invalid operation code in program level 1 sets the hard error bit in the CCU check register along with an invalid operation check bit. In all cases, execution is suppressed.

For details on instruction operation, refer to *3745 Principles of Operation*, SA33-0102. However, hereafter is the list of instructions with their different formats for quick reference only. The formats are described in detail in the *3745 Principles of Operation*, SA33-0102.

| Number of CCU Cycles | | Instruction | | Format | | | | | | | | | | | | | | | |
|----------------------|--------|-------------|--------|-----------|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|
| No Br (1) | Br (1) | | | CZ | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
| - | 3 | B | Branch | 1 0 1 0 1 | | | | | | | | | | | | | | | |

Notes:

1. The number of CCU cycles shown does not include storage cycles when performed after the last CCU cycle (Br= Branch).

| Number of CCU Cycles | | Instruction | | Format | | | | | | | | | | | | | | | | |
|----------------------|--------|-------------|------------------------------------|--------|---|---|-----|---|---|---|----|---|---|---|----|----|----|-------|-------|----|
| No Br (1) | Br (1) | | | CZ | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 3 | - | ICT | Insert character & count | 0 | | | | | 0 | | | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 3 | - | STCT | Store character & count | 0 | | | | | 0 | | | | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 2 | - | IC | Insert character | * | 0 | | | | 1 | R | N | 0 | | | | D | | | | |
| 1 | - | STC | Store character | | 0 | | | | 1 | | | 1 | | | | | | | | |
| 2 | 4 | LH | Load halfword | * | 0 | | B | | 0 | | | 0 | | | | D | | | 1 | |
| 1 | - | STH | Store halfword | | 0 | | | | 0 | R | | 1 | | | | | | | 1 | |
| 3 | 5 | L | Load | * | 0 | | | | 0 | | | 0 | | | | D | | | 1 | 0 |
| 2 | - | ST | Store | | 0 | | | | 0 | | | 1 | | | | | | | 1 | 0 |
| 1 | 3 | LHR | Load halfword register | * | 0 | | | | 0 | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 3 | AHR | Add halfword register | * | 0 | | R2 | | 0 | | R1 | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 3 | SHR | Subtract halfword register | * | 0 | | | | 0 | | | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 3 | CHR | Compare halfword register | * | 0 | | | | 0 | | | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 3 | XHR | Exclusive OR halfword register | * | 0 | | | | 0 | | | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 3 | OHR | OR halfword register | * | 0 | | R2 | | 0 | | R1 | | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 3 | NHR | AND halfword register | * | 0 | | | | 0 | | | | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 3 | LHOR | Load halfword with offset register | * | 0 | | | | 0 | | | | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 3 | LR | Load register | * | 0 | | | | 0 | | | | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 3 | AR | Add register | * | 0 | | | | 0 | | | | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 3 | SR | Subtract register | * | 0 | | | | 0 | | | | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 3 | CR | Compare register | * | 0 | | | | 0 | | | | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 3 | XR | Exclusive OR register | * | 0 | | | | 0 | | | | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 3 | OR | OR register | * | 0 | | | | 0 | | | | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 3 | NR | AND register | * | 0 | | | | 0 | | | | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 3 | LOR | Load with offset register | * | 0 | | | | 0 | | | | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| - | 3 | BALR | Branch & link register | * | 0 | | R2 | | 0 | | R1 | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | IOH | Adapter in or out | * | 0 | | | | 0 | | | | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| | | IOHI | Adapter IO immediate | * | 0 | | 000 | | 0 | | R | | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 2 | - | IN | CCU register in | | 0 | | | | 0 | | | | | | | | 1 | 1 | 0 | 0 |
| 1 | 3 | OUT | CCU register out | | 0 | E | | | 0 | | R | | E | | | | 0 | 1 | 0 | 0 |
| - | 3 | BAL | Branch and link | | 1 | 0 | 1 | 1 | 1 | | R | | 0 | 1 | | | | | | |
| 2 | 3 | LA | Load address | | 1 | 0 | 1 | 1 | 1 | | | | 0 | 0 | | | | A (2) | A (2) | |
| - | 9 | EXIT | Exit | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

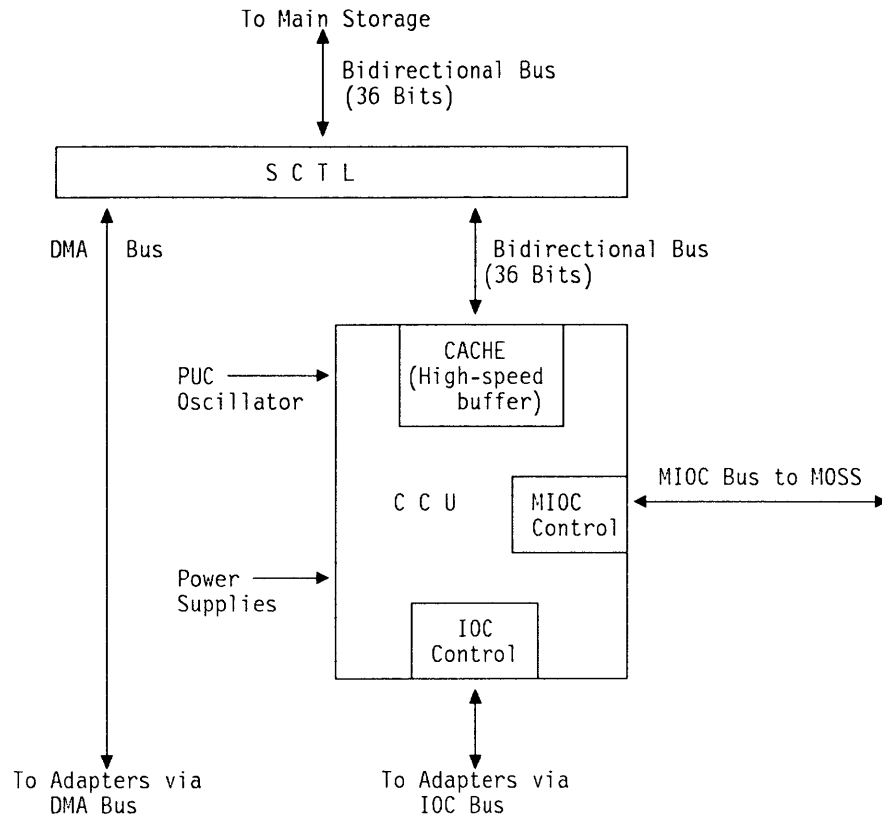
The figure shown is valid for normal instruction cases.

Notes:

1. The number of CCU cycles shown does not include storage cycles when performed after the last CCU cycle (Br= Branch).
2. The A field contains 22 bits, therefore the branch address is always below four megabytes.

CCU Environment

The figure below shows all interconnections to the CCU.



Storage Control Interconnection

Writing data to main storage is performed through the write storage data register (this register is 27 bits wide; 24 data bits + 3 parity bits). Data read from storage is written directly into one or more CCU registers and/or in local storage. Main storage is read and written across the storage data bus (bidirectional, 36 bits wide) which is the only port to/from main storage for the whole machine.

MIOC Interconnection

Through the MIOC interface, the MOSS will be able to obtain or alter the state of 3745.

IOC Bus

This is a multipurpose compatible bus that is used as the base attachment interface for all channel adapters, and line adapters to the CCU.

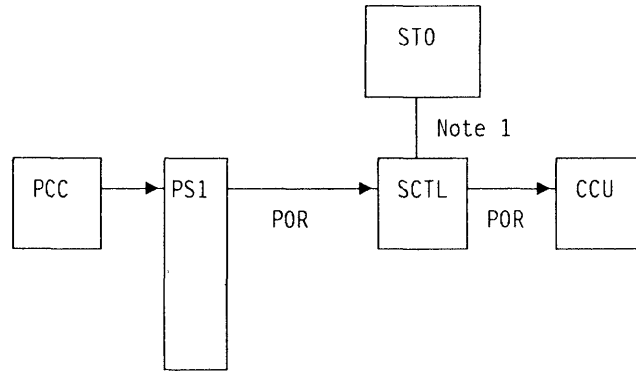
PUC Oscillator Interconnection

The PUC 53.1914 MHz quartz oscillator signal is used by the CCU to generate its timings.

Power Interface

The power interface provides the CCU with all necessary power voltage requirements needed to operate all 3745 functions.

CCU Subsystem Power-ON Reset (POR)



Note: STO is zeroed.

POR is activated at the machine power ON, or at machine reset. The MOSS code can ask the PCC to activate the POR line.

Storage control

At the end of the POR signal, the following sequence of 'warm up' storage is started.

1. Clear all latches and counters,
2. Then, perform 128 cycles to initialize storage,
3. Perform one cycle to configure storage type and size,
4. Then, blank storage with proper ECC.

During all that time, incoming requests are inhibited.

Main Storage

The main storage contains the control program. It is packaged on one card of 4 or 8 Mbytes.

The storage word consists of 4 bytes, referenced as follows:

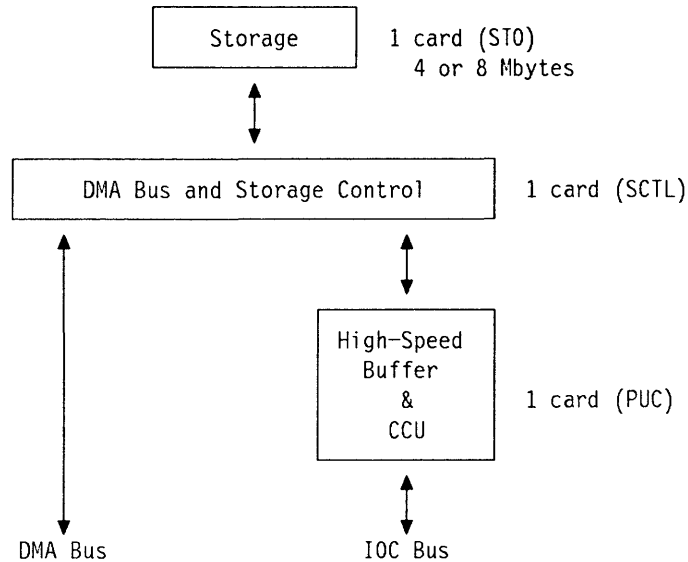
| | | | |
|---|-----|-----|-------|
| Y | X | 0 | 1 |
| 0 | 7 0 | 7 0 | 7 0 7 |

The bytes are addressed from the storage address register, which is 27 bits wide.

Storage Environment

The main storage communicates with:

1. The CCU via the storage control (SCTL)
2. The high-speed adapters via the direct memory access bus (DMA bus) through the SCTL.



Direct Memory Access and Storage Control (SCTL)

The direct memory access and storage control functions are packaged on one card (SCTL) and the main functions are the following:

- Allocate main storage access to the different users (CCU via the cache storage), and high-speed adapters via the DMA function of the SCTL).
- Control the different storage operations and ensure data transfer integrity:
 - CCU read and write

Write requests are buffered in SCTL so that the CCU and the storage operations can overlap.

- Cache storage line loading
- DMA burst transfers.

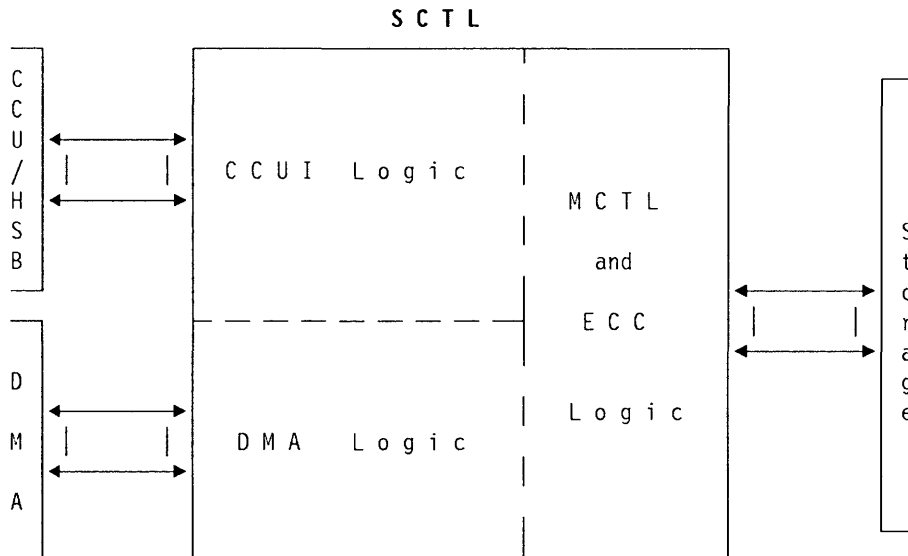
The data is aligned and temporarily stored in a buffer so as to optimize the use of storage bandwidth.

- Control the cache operations (line loading) Maintain cache consistency with storage during DMA write operations, by means of a cache line invalidation mechanism.
- Check for unauthorized DMA write operations with a DMA storage protect mechanism.

Function Partitioning

The SCTL card can be partitioned into three distinct functional parts:

- The central control unit interconnection (CCUI) logic
- The direct memory access (DMA) logic
- The storage control (MCTL) and, error checking and correction (ECC) logic.



CCUI logic

The CCUI logic interconnects the CCU cache storage. It receives and buffers requests from CCU/cache and controls cache line loading. It controls cache line invalidation and accesses the DMA storage protect RAM (during DMA write operations) on behalf of the DMA logic. The CCUI logic makes storage requests to the MCTL/ECC.

DMA Logic

The DMA logic interconnects the DMA bus on which the high-speed adapters are hooked. It receives requests from the high-speed adapters. It performs data alignment, reads or writes its DMA buffer and makes storage requests to the MCTL and ECC. During a DMA write storage transfer, it makes requests to the CCUI logic for cache line invalidations and for access to the DMA storage protect RAM.

MCTL and ECC

The MCTL and ECC interconnects the storage. It receives storage requests from the CCUI logic and the DMA logic. It performs arbitration between these two users, accesses storage and controls the ECC mechanism.

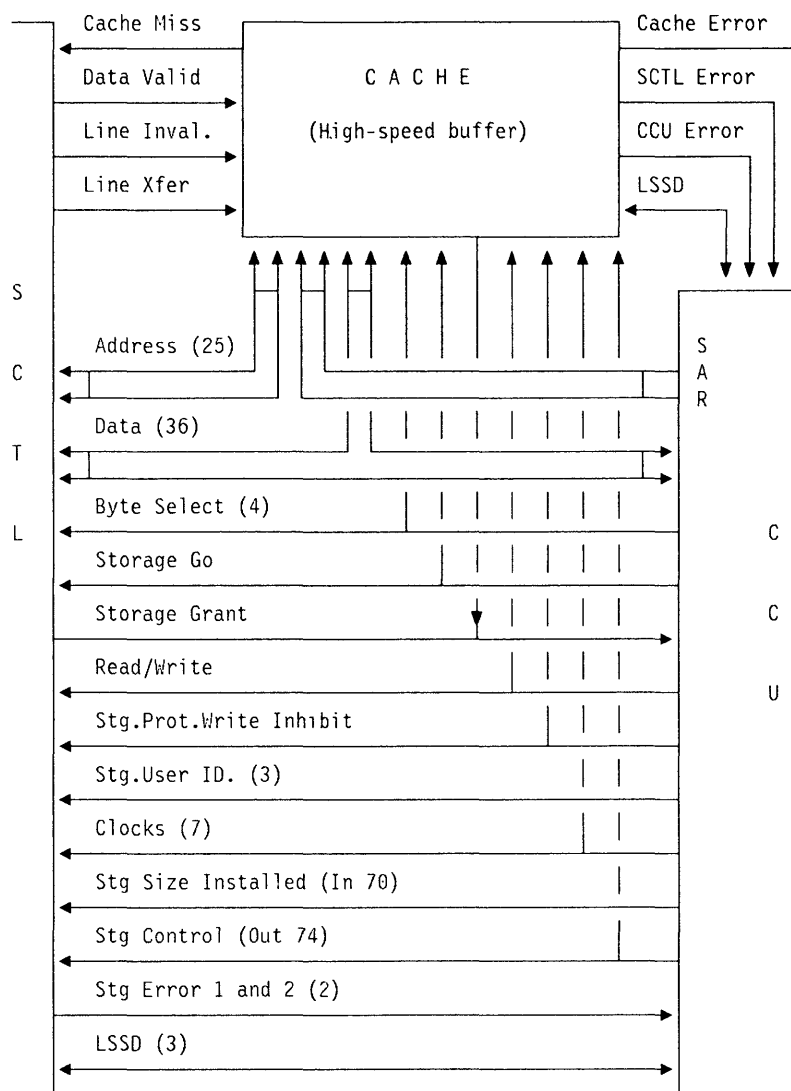
The storage control contains an error correction code (one word) which is permanently stored, either with its original parity or inverted, thus allowing to correct at least one error in addition to the one-bit correction.

The correcting capability of the ECC depends on the type of bit error, whether it is a hard error (storage position stuck to 0 or 1), or a soft (transient) error.

The correction coverage is the following:

| Type of Fault | Coverage |
|-----------------------|----------|
| One hard | 100% |
| One soft | 100% |
| One hard and one soft | 100% |
| Two hard | 100% |
| Two hard and one soft | 50% |
| Two soft | 0% |

SCTL-to-CCU Cache Interconnection



Storage Control Mode

See the output X'74' instruction on page 2-29.

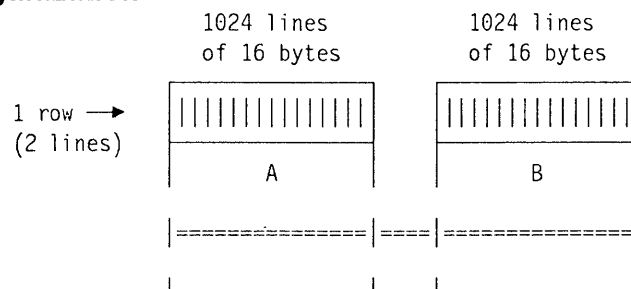
CCU-to-Storage Interconnection

Cache Storage

The cache storage, packaged on the PUC together with the CCU, provides the CCU with instructions and data at cycle rate.

If the instruction or data is not in the cache when it is fetched, the 16 contiguous bytes are automatically transferred into the cache. The probability is high that the next instruction(s) or data will be in those 16 bytes, then, as long as instructions and data are found in the cache, the CCU is not slowed down by main storage and can run at full speed.

Cache Storage Organization



On CCU request, the cache can either write one byte, one halfword, or one fullword. However, the cache is always loaded from storage with 16 contiguous bytes forming a line. The 32K cache is made of 2048 x 16-byte lines and its directory is two-set associative. Cache organization is thus: 1024 rows x 2 sets x 16 bytes. The following table summarizes the various cache data path functions:

| Request | Storage User | Cache Function | Management |
|--------------------|---|---|--------------------------|
| Read | I-fetch prog. read | Hit: cache read Miss: line loaded from storage + cache read | LRU update LRU update |
| | Other than I-fetch and prog. read | Hit: cache read Miss: storage read | LRU update — |
| Write | Any user | Hit: cache write + storage write Miss: storage write | LRU update — |
| Line Invalidate | DMA | Invalidate a line in the cache | LRU update |

LRU: Least recently used

HSB is controlled by means of an X'74' out instruction.

Write Policy

Write requests are always presented both to the cache and main storage (store-through policy). The write request is sent to storage but as soon as it is accepted by the SCTL, the CCU proceeds to the next instruction without waiting for storage update completion. This policy ensures that cache and storage are always consistent with each other and minimizes housekeeping when a cache line must be replaced.

Since on a write request, main storage is always updated (regardless of cache hit or miss), and since the CCU does not wait for write completion, there would be no gain in loading a line in the cache in case of a cache miss. This new line would most probably replace a more useful line in the cache. Therefore, the cache is not loaded with a new line on a write miss.

Read Policy

A CCU read request can come from different sources. The source (called the storage user) can be: The MOSS, the branch trace, the prefetch mechanism, the program, or the IOC (cycle steal mode).

In order to increase the cache hit ratio, the cache is loaded with a new line only when a read miss is caused by an I-fetch or a program read. Any other storage user causing a read miss, results in the data being loaded directly from memory to the CCU without cache involvement.

Line Invalidation

Because of DMA operation, the SCTL requests the cache to invalidate a line. An invalidation request has priority over a CCU request.

When a line invalidation is requested, the SCTL raises the line 'invalid line', which instructs the cache not to propagate the storage address register (SAR) to the storage address data (SAD) bus and to latch the address presented by the SCTL. In the cycle following the address transfer, the cache invalidates the line in the cache and the SCTL ignores requests at the interconnection.

Storage Protection

Storage Protect and Address Exception (SP/AE)

Storage protect is a means of notifying the control program whenever the contents of storage are accessed for unauthorized modification or unauthorized code execution. Attempts to modify storage and attempts to execute instructions are monitored by the following three mechanisms:

1. Address exception based on address exception key.
2. Storage protect based on read-only key.
3. Storage protect based on storage protection key and user key.

Main Storage Protection State

With the storage protect and address exception mechanism, a main storage position can be placed in any of the following states:

- Write free
- Write and instruction fetch controlled
- Read-only
- Write or/and read forbidden.

Storage Protect and Address Exception Instructions

The CCU controls the storage protect and address exception instructions (SP/AE) mechanism with the input X'73' and output X'73' instructions.

SP/AE Keys

Address Exception Key

This key indicates whether an 8-Kbyte block of storage is accessible.

Read Only Key

This key indicates whether a 4-Kbyte block of storage is in the read-only state. For example, machine configuration data is placed in such a storage block.

Storage Protection Key

This key determines the key value (3 bits) for writing in a defined 4-Kbyte block of storage.

User Key

Every user is assigned a 3-bit register that holds the storage protection key it must use for writing in storage and to fetch instructions for execution.

For more details, refer to *Principles of Operations*, SA33-0102.

SP/AE Key Locations

The storage keys are located in a local storage (storage key RAM) and the user keys are located in registers.

To perform the necessary initialization, the program must execute output X'73' instructions for setting the storage keys for all installed 4-Kbyte blocks of storage and up to 6 output X'73' instructions for setting the user keys.

CCU Timers

Two timers are available in the CCU. They are the 100 ms interval timer and the high/low resolution timer.

100 ms Interval Timer

Every 100 ms, this timer requests a CCU level 3 interrupt. Output X'77', byte 1, bit 1 ON is used to reset the timer interrupt. The 100 ms timer is used to:

- Maintains a count of realtime in storage
- Perform long and short time outs
- Perform supervisory functions on a cyclic basis.

High and Low Resolution Timer

The high and low resolution timer does not raise any interrupts. It is driven by clock pulses (every 131.6 ns). Output X'7A' selects the mode and initializes the current timer value to X'00'. Input X'7A' reads the current timer value.

CCU to and from Adapters

The CCU interconnects with the various adapters via the IOC bus. Refer to the Chapter "IOC Bus" for details.

IOC Control Logic

Data, address, and control information exchanges take place between the CCU work registers and the adapters attached to the I/O bus. They use the IOC control logic.

The IOC logic, located in the PUC, operates in two different ways, depending on whether the program initiates the operation (PIO), or an adapter initiates it (AIO).

The data bus carries interrupt requests from the adapters (levels 1, 2, and 3) when it is not busy with PIO or AIO operations.

IOC Data Flow

The I/O bus is an 18-bit (16 for data + 2 for parity) bidirectional bus with necessary tags and controls.

D Register: It is an 18-bit (16 for information + 2 for parity) register. It is the buffer used with the IOC bus for the exchange of all addresses, commands and data to and from the adapters.

A Register: It is a 27-bit (24 for information + 3 for parity) register. In an IOH/IOHI operation it is loaded by the R1 field. In AIO operations it contains the cycle steal address.

The IOC bus operations are under the control of the IOC control logic using a handshaking protocol between the CCU and the adapters.

Level 2 and Level 3 Interrupt Reporting

IOC byte 1, bit 0 produces a single CA level 3 interrupt request to the CCU. IOC byte 0, bit 1 produces a single LA level 2 interrupt request to the CCU. After interrupt recognition, the CCU executes an input X'77' instruction to identify the level 2 and 3 interrupt request origin. (see input X'77' in this chapter.)

Input X'77' byte 0 is dedicated to level 2 interrupts, and byte 1 to level 3. The input X'77' bits are then set according to the logical rules.

Level 1 Interrupt Reporting

IOC bus byte 0, bit 5 produces a single CA level 1 interrupt request.

IOC bus byte 1, bit 5 produces a single LA level 1 interrupt request.

After interrupt recognition, the CCU executes an input X'7E' instruction to identify the level 1 interrupt request origin. (see input X'7E' in this chapter.)

When the CCU executes the input X'76' instruction, the bit assignment of byte 0 is for IOC.

Cycle Steal Pointer Allocation

The IOC bus may address up to four channel adapters. The cycle steal pointer registers are allocated as follows:

| Adapter | IOC | Pointer type |
|------------------|---------|-----------------|
| CAs | 30 - 37 | Dedicated (NCP) |
| LAs (CSC, HPTSS) | 3F | Shared pointer |

For all AIO operations, bit 5 = 0 for CA, bit 5 = 1 for LA and bits 11-14 (pointer number if bit 5 = 0 and scanner ID if bit 5 = 1) of the CSCW are stored in an external register accessible by the control program using input X'75'. (See input X'75' in this chapter.)

Reset or Stop Adapter Input or Output

See output X'76' and output X'79' in this chapter.

Registers

The controller has two types of register: general and external.

General Registers

Forty general registers are available in the controller for program use. The size of each register is 24 bits. The bits are assigned from left to right as byte X, bits 0-7; byte 0, bits 0-7; and byte 1, bits 0-7.

The forty registers are divided into five groups of eight registers each. Each group is assigned to a specific program level. Only one group of general registers is active at a given time (the group associated with the active program level). The registers within the currently active group are directly addressable with program instructions. The control program can access the general registers by specifying them as external registers in input and output instructions.

Instruction Address Register: General register 0 in each group is the instruction address register (IAR). This register is an implied base register and contains the address of the next instruction to be executed for the associated program level. Register 0 of the active group is always incremented to point to the next sequential instruction before the current instruction is executed. However, execution of a branch instruction can cause the IAR to be loaded with a storage address other than that of the current instruction.

External Registers

External registers are registers which are not directly accessible by the control program. Therefore, by using an input instruction, the control program can load the contents of an external register into a general register where it can operate on the data. By using an output operation, the control program can load an external register with the contents of the general register specified in the instruction.

CCU external registers are located in:

- The local store (LS address X'00' to X'7F')

The local store registers at address X '00 to 27' are the five groups of eight general registers. Each group is associated to one program level.

- The hardware registers:
 - Seven work registers
 - Instruction address register (IAR)
 - Lagging address register (LAR).

See "Hardware Registers" on page 2-38 for details.

- Hardware latches

The following tables, list the input and output instructions.

Input Instructions

| Input | Register Function | Local Storage Register |
|---------|---|------------------------|
| 00 - 07 | General register group 0 (level 2) | 00 - 07 |
| 08 - 0F | General register group 1 (level 3) | 08 - 0F |
| 10 - 17 | General register group 2 (level 4) | 10 - 17 |
| 18 - 1F | General register group 3 (level 5) | 18 - 1F |
| 20 - 27 | General register group 4 (level 1) | 20 - 27 |
| 28 - 2F | Not used | |
| 30 - 37 | IOC-CA pointer register 0-7 | 30 - 37 |
| 38 - 3E | Not used | 38 - 3E |
| 3F | IOC-CSP pointer register F | 3F |
| 40 | Program interrupt start address level 1 | 40 |
| 41 | Program interrupt start address level 2 | 41 |
| 42 | Program interrupt start address level 3 | 42 |
| 43 | Program interrupt start address level 4 | 43 |
| 44 | Byte-addressable base register | 44 |
| 45 | Halfword addressable base register | 45 |
| 46 | Fullword addressable base register | 46 |
| 47 | CCU SCTL/cache control | 47 |
| 48 | IOH TA substitution | 48 |
| 49 - 4F | Not used | |
| 50 - 5F | Reserved for program use (see Note 1) | 50 - 5F |
| 60 - 67 | Not used | 60 - 67 |
| 68 | Zero register | 68 |
| 69 | Holding register for IOH, IOHI, BAL instruction | 69 |
| 6A | Holding register for MOSS IOH | 6A |
| 6B | Holding register for IOHI | 6B |
| 6C - 6E | Not used | |
| 6F | Not used | 6F |
| 70 | Storage size installed | Hardware register |
| 71 | Operator address or data entry register | 71 |
| 72 | Operator function select controls | 72 |
| 73 | Read SP/AE key | Hardware register |
| 74 | LAR | Hardware register |
| 75 | AIO CCW | Hardware register |
| 76 | IOC level 1 interrupt requests | Hardware register |
| 77 | Adapter level 2, 3 or 4 interrupt requests | Hardware register |
| 78 | Not used | |
| 79 | Utility | Hardware register |
| 7A | High-resolution timer value | Hardware register |
| 7B | Branch trace address pointer | 7B |
| 7C | Branch trace buffer count | 7C |
| 7D | CCU hard errors register | Hardware register |
| 7E | Level 1 interrupt requests | Hardware register |
| 7F | CCU level 2, 3 or 4 interrupt requests | Hardware register |

Notes:

1. Unassigned fullword registers are available for the program at this location.
2. If the control program tries to read locations 28-2F, 38-3E, 49-4F, 6C-6E, 78 an invalid operation condition is detected and a level 1 interrupt is set.

Output Instructions

| Outputs | Register/Function | Local Storage Register |
|---------|--|------------------------|
| 00 - 07 | General register group 0 (level 2) | 00 - 07 |
| 08 - 0F | General register group 1 (level 3) | 08 - 0F |
| 10 - 17 | General register group 2 (level 4) | 10 - 17 |
| 18 - 1F | General register group 3 (level 5) | 18 - 1F |
| 20 - 27 | General register group 4 (level 1) | 20 - 27 |
| 28 - 2F | Not used | |
| 30 - 37 | IOC-CA pointer register 0-7 | 30 - 37 |
| 38 - 3E | Not used | 38 - 3E |
| 3F | IOC-CSP pointer register F | 3F |
| 40 | Program interrupt start address level 1 | 40 |
| 41 | Program interrupt start address level 2 | 41 |
| 42 | Program interrupt start address level 3 | 42 |
| 43 | Program interrupt start address level 4 | 43 |
| 44 | Byte-addressable base register | 44 |
| 45 | Halfword-addressable base register | 45 |
| 46 | Fullword-addressable base register | 46 |
| 47 | CCU SCTL/cache control | 47 |
| 48 | IOH TA substitution | 48 |
| 49 - 4F | Not used | |
| 50 - 5F | Reserved for programs use | 50 - 5F |
| 60 - 67 | Not used | 60 - 67 |
| 68 | Zero register | 68 |
| 69 | Holding register for IOH,IOHI, BAL instruction | 69 |
| 6A | Holding register for MOSS IOH | 6A |
| 6B | Holding register for IOHI | 6B |
| 6C - 6E | Not used | |
| 6F | Not used | 6F |
| 70 | Hard stop | Hardware register |
| 71 | Display register 1 | Hardware register |
| 72 | Display register 2 | 72 |
| 73 | Write/select SP/AE key | Hardware register |
| 74 | Storage control | Hardware register |
| 75 | Not writable | |
| 76 | Miscellaneous control | Hardware register |
| 77 | Miscellaneous control | Hardware register |
| 78 | Not used | Hardware register |
| 79 | Utility | Hardware register |
| 7A | Resolution/utilisation counter control | Hardware register |
| 7B | Set PCI level 2 | Hardware register |
| 7C | Set PCI level 3 | Hardware register |
| 7D | Set PCI level 4 | Hardware register |
| 7E | Set mask bits | Hardware register |
| 7F | Reset mask bits | Hardware register |

Note:

If the control program tries to read locations 28-2F, 38-3F, 49-4F, 6C-6F, 75 an invalid operation condition is detected and a level 1 interrupt is set.

Input/Output X'7x' Instructions

The control program uses input and output instruction to access CCU registers and/or to control and monitor the status of the CCU.

Input Instructions

Input X'70' (storage size installed):

This instruction loads a general register with a combination of bits that indicates the amount of storage installed.

Input X'71' (operator address or data entry register):

This instruction loads a general register with a combination of bits to indicate data to be used in a control panel function.

Input X'72' (operator function select control):

This instruction loads a general register with a combination of bits to indicate the operator display or function select. Through the use of this instruction, the program can accept information from the operator.

Input X'73' (read storage protection or address exception key):

This instruction loads a general register with the storage protect or address exception key addressed by the last output X'73' instruction executed.

Input X'74' (lagging address register):

This instruction loads a general register with the contents of the lagging address register. When this input is executed, the address transferred into the general register is that of the last instruction executed before the input instruction (this might not be true in case of error. Refer to *Principles of Operations Manual* for more information).

Input X'75' (AIO channel control word):

This instruction loads a general register with bits of the CCW received by the IOC for an AIO which has been suspended or stopped due to an error detected by the hardware. Otherwise, the data loaded in this general register is NOT valid.

Input X'76' (IOC level 1 interrupt requests):

This instruction loads a general register with information that can be used to determine the type of error encountered.

Input X'77' (adapter level 2, 3, or 4 interrupt requests):

This instruction loads a general register with information that can be used to determine which adapter type caused a level 2, 3, or 4 interrupt.

Input X'79' (utility):

This instruction loads a general register with utility information. When it is executed in program level 1, byte 1, bits 0-3 designate the program level that was operating before the level 1 interrupt. When it is executed in program levels 2, 3, or 4 (or level 1 if level 1 is re-entered immediately after a level 1 exit), byte 1, bits 0-3 have no significance and are set to zero. When input X'79' is executed at any level, byte 0, bits 6 and 7 indicate the state of the program level 5, C, and Z condition latches.

Input X'7A' (high-resolution timer):

This instruction loads a general register with the high-resolution timer.

Input X'7B' (BT address pointer):

This instruction loads a general register with the branch trace address pointer.

Input X'7C' (BT buffer count):

This instruction loads a general register with the branch trace buffer count.

Input X'7D' (CCU hard errors register):

This instruction loads a general register with information showing which CCU hard error has been detected.

Input X'7E' (program level 1 interrupt requests):

This instruction loads a general register with bits to indicate interrupt requests for program level 1 interrupt. Also shown is the CCU hard error summary bit.

Input X'7F' (level 2, 3, or 4 interrupt requests):

This instruction loads a general register with bits to indicate interrupt requests for program levels 2, 3, and 4.

Output Instructions

Output X'70' (hard stop):

This instruction causes the CCU to enter a hard stop state. In this state, program execution, program interrupts and adapter cycle steals are prevented. The bit settings of the general register are ignored.

Output X'71' (display register 1):

This instruction loads the contents of the general register into display register 1.

Output X'72' (display register 2):

This instruction causes the contents of the general register to be loaded into display register 2.

Output X'73' (read storage protection or address exception register):

This instruction causes the contents of the general register to be used to address and or set the storage and protect keys.

Output X'74' (storage control):

This instruction causes the contents of the general register to be used to control the operational mode of the cache and the SCTL/ECC mechanism.

Output X'76' and Output X'77' (miscellaneous control):

These instructions cause the contents of the specified general register to be used to set or reset various interrupt requests.

Output X'79' (utility):

This instruction causes the contents of the specified general register to set or reset various hardware latches. It permits 'set IPL request' (byte 0 bit 2). This results in an interrupt to MOSS. It does not stop the control program. If the control program is to stop after setting an IPL request, by using the output X'70' instruction a hard stop must be sent by the control program in addition to output X'79'. It permits remote power OFF (bit 0.4). A remote power OFF line is sent to the power subsystem.

Output X'7A' (utilization counter):

This instruction causes the contents of the specified general register to control the high-resolution timer and the utilization counter.

Output X'7B' (set PCI level 2):

This instruction causes a program-controlled interrupt request to be set for program level 2 (PCI level 2). This allows a program level to transfer a processing requirement to a different priority program level. The bit settings of the general register are ignored. A PCI interrupt request is immediately effective.

Output X'7C' (set PCI level 3):

This instruction causes a program-controlled interrupt request to be set for program level 3 (PCI level 3). This allows a program level to transfer a processing requirement to a different priority program level. The bit settings of the general register are ignored. A PCI interrupt request is immediately effective.

Output X'7D' (set PCI level 4):

This instruction causes a program-controlled interrupt request to be set for program level 4 (PCI level 4). This allows a program level to transfer a processing requirement to a lower priority level. The bit settings of the general register are ignored. A PCI interrupt request is immediately effective.

Output X'7E' (set mask bits):

This instruction causes the mask bits of the program levels to be set according to the contents of the general register. When a mask bit is set ON, interrupt requests for the program level that corresponds to that bit are ignored. When the mask bit for program level 5 is ON, program execution at that level is not allowed.

Output X'7F' (reset mask bits):

This instruction causes the mask bits of the program levels to be reset according to the contents of the general register. If an interrupt for a particular level is pending when the mask bit for that level is reset, an interrupt for that level will occur before the next instruction is executed.

Input and Output X'7x' Register Bits

| X'70' | Input: Storage Size Installed | Output: Hard stop |
|---------------|----------------------------------|----------------------|
| Byte X, Bit 0 | 0 | Ignored |
| 1 | 0 | Ignored |
| 2 | 0 | Ignored |
| 3 | 0 | Ignored |
| 4 | 0 | Ignored |
| 5 | 0 | Ignored |
| 6 | 0 | Ignored |
| 7 | 0 | Ignored |
| Byte 0, Bit 0 | 1 | Ignored |
| 1 | 1 | Ignored |
| 2 | 1 | Ignored |
| 3 | 1 Bit setting depending | Ignored |
| 4 | 1 on storage size. | Ignored |
| 5 | 1 See Table below. | Ignored |
| 6 | 1 | Ignored |
| 7 | 1 | Ignored |
| Byte 1, Bit 0 | 0 | Ignored |
| 1 | 0 | Ignored |
| 2 | 0 | Ignored |
| 3 | 0 | Ignored |
| 4 | 0 | Ignored |
| 5 | 0 | Ignored |
| 6 | 0 | Ignored |
| 7 | 0 | Ignored |

Byte 0 Bit Setting

| Storage Size | Storage Card | Input: Byte 0 Bits 0 1 2 3 4 5 6 7 P |
|--------------|--------------|--|
| 4 | 1 card | 0 0 X X X 0 0 1 X |
| Illegal | Wrong | 0 1 X X X X X X X |

Notes:

1. Byte 0 bits 2, 3, 4 carry the EC level of the SCTL cards.
2. A good parity is delivered to CCUI and DMA (it includes the EC bits).
3. If no card is installed, a storage control error is reported to CCUI and DMA.

| X'71' | Input: Operator Address/Data (LS) Entry Register | Output: Program Display Register 1 (DR1) |
|---------------|---|---|
| Byte X, Bit 0 | Addr/Data Byte X, Bit 0 | DR1 Byte X, Bit 0 |
| 1 | 1 | 1 |
| 2 | 2 | 2 |
| 3 | 3 | 3 |
| 4 | 4 | 4 |
| 5 | 5 | 5 |
| 6 | 6 | 6 |
| 7 | 7 | 7 |
| Byte 0, Bit 0 | Addr/Data Byte 0, Bit 0 | DR1 Byte 0, Bit 0 |
| 1 | 1 | 1 |
| 2 | 2 | 2 |
| 3 | 3 | 3 |
| 4 | 4 | 4 |
| 5 | 5 | 5 |
| 6 | 6 | 6 |
| 7 | 7 | 7 |
| Byte 1, Bit 0 | Addr/Data Byte 1, Bit 0 | DR1 Byte 1, Bit 0 |
| 1 | 1 | 1 |
| 2 | 2 | 2 |
| 3 | 3 | 3 |
| 4 | 4 | 4 |
| 5 | 5 | 5 |
| 6 | 6 | 6 |
| 7 | 7 | 7 |

| X'72' | Input: Operator Function Select Control | Output: Program Display Register 2 (DR2) |
|---------------|--|---|
| Byte X, Bit 0 | 0 | DR2 Byte X, Bit 0 |
| 1 | 0 | 1 |
| 2 | 0 | 2 |
| 3 | 0 | 3 |
| 4 | 0 | 4 |
| 5 | 0 | 5 |
| 6 | 0 | 6 |
| 7 | 0 | 7 |
| Byte 0, Bit 0 | Function select 8 | DR2 Byte 0, Bit 0 |
| 1 | Function select 9 | 1 |
| 2 | Function select A | 2 |
| 3 | Storage address | 3 |
| 4 | Register address | 4 |
| 5 | Function select B | 5 |
| 6 | Function select C | 6 |
| 7 | Function select D | 7 |
| Byte 1, Bit 0 | Function select E | DR2 Byte 1, Bit 0 |
| 1 | Function select 1 | 1 |
| 2 | Function select 2 | 2 |
| 3 | Function select 3 | 3 |
| 4 | Function select 4 | 4 |
| 5 | Function select 5 | 5 |
| 6 | Function select 6 | 6 |
| 7 | Function select 7 | 7 |

| Storage Protection Storage Exception X'73' | Input: | Output: |
|--|-----------------|-------------------------------------|
| Byte X, Bit 0 | 0 | SKA bit 0 |
| 1 | 0 | SKA bit 1 |
| 2 | 0 | SKA bit 2 |
| 3 | 0 | SKA bit 3 |
| 4 | 0 | SKA bit 4 |
| 5 | 0 | SKA bit 5 |
| 6 | 0 | SKA bit 6 |
| 7 | 0 | SKA bit 7 |
| Byte 0, Bit 0 | 0 | SKA bit 8 |
| 1 | 0 | SKA bit 9 |
| 2 | 0 | SKA bit 10 |
| 3 | 0 | SKA bit 11 or UKA bit 0 |
| 4 | 0 | UKA bit 1 |
| 5 | 0 | UKA bit 2 |
| 6 | 0 | UKA bit 3 |
| 7 | 0 | UKA bit 4 |
| Byte 1, Bit 0 | 0 | Ignored |
| 1 | 0 | Enable SP or AE |
| 2 | 0 | I 00 = user key 10 = exception key |
| 3 | 0 | I 01 = stor. key 11 = read only key |
| 4 | 0 | Modify key value |
| 5 | Key value bit 0 | Key value bit 0 |
| 6 | Key value bit 1 | Key value bit 1 |
| 7 | Key value bit 2 | Key value bit 2 |

If byte 1 bits 1, 2, 3 = 1, 1, 0, the storage is not installed for exception key.
If byte 1 bits 1, 2, 3 = 1, 1, 1, prevent write for read-only key.

| X'74' | Input: Lagging Address Register (LAR) | Output: Storage Control |
|---------------|--|---------------------------|
| Byte X, Bit 0 | LAR Byte X Bit 0 | I |
| 1 | 1 | I |
| 2 | 2 | I |
| 3 | 3 | I See Output: Byte X next |
| 4 | 4 | I |
| 5 | 5 | I |
| 6 | 6 | I |
| 7 | 7 | I |
| Byte 0, Bit 0 | LAR Byte 0 Bit 0 | Not used |
| 1 | 1 | Not used |
| 2 | 2 | Not used |
| 3 | 3 | Not used |
| 4 | 4 | Not used |
| 5 | 5 | Not used |
| 6 | 6 | Not used |
| 7 | 7 | Not used |
| Byte 1, Bit 0 | LAR Byte 1 Bit 0 | Not used |
| 1 | 1 | Not used |
| 2 | 2 | Not used |
| 3 | 3 | Not used |
| 4 | 4 | Not used |
| 5 | 5 | Not used |
| 6 | 6 | Not used |
| 7 | 7 | Not used |

| Output: Byte X, Bit | 0 1 2 3 4 5 6 7 |
|---------------------------|---|
| Cache disable | 0 0 0 0 X X X X |
| Cache flush | 1 0 X 0 X X X X |
| Cache normal | 0 0 0 1 X X X X |
| Cache wait state | 0 0 1 1 X X X X Cache functions |
| Cache retry state | 1 0 1 1 X X X X |
| Cache directory test | 0 0 1 0 X X X X |
| Cache data array test | 1 0 0 1 X X X X |
| Disable CCUI interface | X X X X 0 0 1 X |
| Bypass cache | X X X X 0 1 1 X CCUI functions |
| CCUI normal operation | X X X X 0 0 0 X |
| DMA SP RAM init | X X X X 0 1 0 X |
| SCTL normal operation | 0 1 0 0 0 0 0 0 For CCUI and |
| Disable SCTL error action | 0 1 X X 1 1 X X MCTL functions |
| ECC disable | X 1 1 0 1 X X X |
| ECC transparent | X 1 0 1 1 X X X MCTL functions |
| MCTL error wrap | 0 1 1 1 1 X X 0 |
| ECC only mode | 0 1 1 1 1 X X 1 |
| NO refresh mode | 0 1 X X 1 X 1 X |
| Force storage errors | 1 1 X X 1 0 0 0 Force Y.7 at 0 |
| Force storage errors | 1 1 X X 1 0 1 0 Force Y.7 at 1 |
| Force storage errors | 1 1 X X 1 1 0 0 Force Y.7 , X.7 at 0 |
| Force storage errors | 1 1 X X 1 1 1 0 Force Y.7 , X.7 at 1 |
| Force storage errors | 1 1 X X 1 1 0 1 Force Y.7, X.7 & 1.0 at 0 |
| Force storage errors | 1 1 X X 1 1 1 1 Force Y.7, X.7 & 1.0 at 1 |

| X'75' | Input: CSCW | Output: NA |
|---------------|--------------------------|------------|
| Byte X, Bit 0 | | |
| 1 | | |
| 2 | | |
| 3 | | |
| 4 | | |
| 5 | | |
| 6 | | |
| 7 | | |
| Byte 0, Bit 0 | IOC CSCW bit 5 (Note 1) | |
| 1 | IOC CSCW bit 11 (Note 2) | |
| 2 | IOC CSCW Bit 12 (Note 2) | |
| 3 | IOC CSCW Bit 13 (Note 2) | |
| 4 | IOC CSCW Bit 14 (Note 2) | |
| 5 | 0 | |
| 6 | 0 | |
| 7 | 0 | |
| Byte 1, Bit 0 | Not used | |
| 1 | Not used | |
| 2 | Not used | |
| 3 | Not used | |
| 4 | Not used | |
| 5 | 0 | |
| 6 | 0 | |
| 7 | 0 | |

Notes:

1. Bit 0 = 0: AIO from CAs.
Bit 0 = 1: AIO from LAs.
2. Bits 1 to 4 are: either pointer number if bit 0=0, or LAs address if bit 0=1.

| X'76' | Input: IOC Level 1 Interrupt Request | Output: Miscellaneous Control |
|----------------|--------------------------------------|-------------------------------|
| Byte X, Bit 0 | 0 | Not significant |
| 1 | 0 | Not significant |
| 2 | 0 | Not significant |
| 3 | 0 | Not significant |
| 4 | 0 | Not significant |
| 5 | 0 | Not significant |
| 6 | 0 | Not significant |
| 7 | 0 | Not significant |
| Byte 0, Bit 0 | IOC Address excep. See | Reset IOC errors |
| 1 | IOC Storage protec. Note | Not significant |
| 2 | IOC Invalid CCW | Start branch trace mode |
| 3 | 0 | CCU prog. request to MOSS |
| 4 | IOC Timeout | CCU prog. response to MOSS |
| 5 | IOC Bus in parity | Not significant |
| 6 ¹ | IOC Adapter init.operation | Not significant |
| 7 ¹ | IOC MOSS init.operation | Not significant |
| Byte 1, Bit 0 | Not used | Not used |
| 1 | Not used | Not significant |
| 2 | Not used | Not significant |
| 3 | 0 | Not significant |
| 4 | Not used | Not significant |
| 5 | Not used | Not significant |
| 6 ¹ | Not used | Not significant |
| 7 ¹ | Not used | Not significant |

¹ = This bit does not generate a level 1 interrupt.

Note: In byte 0 or 1, if bits 4 and 5 are zero, bits 0, 1, 2, and 3 are as shown.

If bit 4 or bit 5 is one, bits 0, 1, 2, and 3 contain IOC internal status at the time of the error. (See further on input X'76' state meaning for time out or bus-in parity error.)

Input X'76' State Meaning for Time Out or Bus-in Parity

| State Latch Decode | Valid Tags (See Note) | 'Time out' Meanings | "Bus in parity Error" Meanings |
|--------------------|-----------------------|---|--|
| 0 | 08 | I/O tag is OFF | No |
| 1 | 10 | I/O tag raised new AIO or IOH | No |
| 2 | 18-11 | No response to TA or channel grant | No |
| 3 | - | CCW parity error | CCW parity error |
| 4 | 10 | VH didn't fall after TD fall | AIO data read or channel pointer register read 2nd transfer |
| 5 | 18-16 11 | No response to TD for AIO data read, or IOH data read | Bus-in parity error on AIO data read, or IOH data read |
| 6 | 18-16 11 | No response to TD for AIO data write, or IOH data write | No |
| 7 | 10 | VH didn't fall after TD fall (byte boundary transfer with 'STG') | No |
| 8 | 08 | I/O tag is OFF, VH must rise (EOC after channel pointer updating in in local store) | Channel pointer register read transfer last transfer (EOC) |
| 9 | 10 | VH didn't fall after 'CG' fall, AIO CCW: S/L or D/I.D or D/I.D.WR | No |
| A | 08 | I/O tag is OFF, VH must rise (last AIO transfer data read is on byte boundary) | No |
| B | 10 | No | Loading of CCW |
| C | 18-11 | No response to TD for AIO pointer initialization | Bus-in parity error AIO address sent to adapter during AIO direct operation |
| D | - | No | No |
| E | 10 | VH didn't fall after TD fall for AIO pointer initialization | Channel pointer register read 1st transfer |
| F | 08 | I/O tag is OFF, VH must rise (IOH end or AIO end after data exchange) | Last AIO data read (EOC or VB + M) |

Note:

| Tags Encode | Tags |
|-------------|------------|
| 08 | VH |
| 10 | IRR |
| 11 | IRR, EOC |
| 16 | IRR, VB, M |
| 18 | IRR, VB |

| X'77' | Input: Adapter Level 2, 3, 4 Interrupt Requests | Output: Miscellaneous Control |
|---------------|--|--|
| Byte X, Bit 0 | 0 | Not significant |
| 1 | 0 | Not significant |
| 2 | 0 | Not significant |
| 3 | 0 | Not significant |
| 4 | 0 | Not significant |
| 5 | 0 | Not significant |
| 6 | 0 | Not significant |
| 7 | 0 | Not significant |
| Byte 0, Bit 0 | Not used | Reset IPL level 1 and not init.bit |
| 1 | Level 2 bus 1 priority | Reset CCU hard checks |
| 2 | Level 2 on bus 1 | Reset MOSS panel inter.req.level 3 |
| 3 | Not used | Reset MOSS diag request level 3 |
| 4 | 0 | Reset MOSS SVC request level 3 |
| 5 | 0 | Reset MOSS SVC response level 4 |
| 6 | 0 | |
| 7 | 0 | Reset PCI level 2 |
| Byte 1, Bit 0 | Level 3 bus 1 priority | Reset MOSS inoperative level 1 |
| 1 | Not used | Reset interval timer level 3 |
| 2 | Level 3 on bus 1 | Reset PCI level 3 |
| 3 | Not used | Reset MOSS level 2 diagnostic request |
| 4 | 0 | Reset address compare level 1 |
| 5 | 0 | Reset program errors |
| 6 | 0 | Reset PCI level 4 |
| 7 | 0 | Reset SVC level 4 |

Byte 0 pertains to level 2 and byte 1 to level 3. The priority bits in byte 0 for level 2 are independent of those in byte 1 for level 3.

Notes:

1. The following description applies to either byte.

One of the priority bits in a byte will be set ON if and only if one or both of the bus interrupt bits in that byte are ON. However, the priority will be set one cycle after the interrupt bit(s) is set, therefore there is a 1-cycle window in which either or both interrupt bits can be ON without either priority bit. This window occurs at the time interrupts are sampled from the adapter bus, not necessarily at input X'77' time, but may affect the result of input X'77'.

To avoid this window, it is recommended that the program use input X'77' in any one of the following ways.

- a. Test only the priority bits in the appropriate byte, ignoring the interrupt bits. This will insure that single and simultaneous bus interrupts will be serviced in turn without the possibility of missed interrupts or ambiguity. In this case, there is no restriction on when input 77 may be performed.
- b. Test only the interrupt bits, ignoring the priority bits (in this case, the program would have to decide by other means which interrupting bus to service). There is no restriction on when input X'77' may be performed.

- c. If neither procedure above is used, the use of the input X'77' instruction is restricted, as follows: input X'77' should be performed in level 2 or level 3 only if there are no adapter interrupt(s) for that level. If no adapter interrupts are pending, they must be serviced and an exit performed. In addition to this restriction, input X'77' should not be performed more than once in a level.

2. After the control program issues an IOH to clear an adapter interrupt, at least 22 CCU cycles must be performed before executing an exit instruction or an input X'77' or X'7E' (read adapter interrupt) instruction. This is to allow reset and re-sampling of interrupts from the adapters.

| Utility X'79' | Input: | Output: |
|------------------|---------------------------------|--|
| Byte X, Bit 0 | 0 | Not significant |
| 1 | 0 | Not significant |
| 2 | 0 | Not significant |
| 3 | 0 | Not significant |
| 4 | 0 | Not significant |
| 5 | 0 | Not significant |
| 6 | 0 | Not significant |
| 7 | 0 | Not significant |
| Byte 0, Bit 0 | 0 | Not significant |
| 1 | 0 | Not significant |
| 2 | 0 | Set program IPL request |
| 3 | 0 | Not significant |
| 4 | 0 | Remote power OFF |
| 5 | 0 | Inhibit program level 5C and Z latches |
| 6 | Program level 5C condition | Program level 5C latch |
| 7 | Program level 5Z condition | Program level 5Z latch |
| Byte 1, Bit 0 | Program level 2 interrupted (1) | Not significant |
| 1 | Program level 3 interrupted (1) | Not significant |
| 2 | Program level 4 interrupted (1) | Set AIO stop mode on IOC (3) |
| 3 | Program level 5 interrupted (1) | Reset AIO stop mode on IOC (3) |
| 4 | 0 | Set bypass CCU check stop (2/3) |
| 5 | 0 | Reset bypass CCU check stop (2/3) |
| 6 | 0 | Scope synchro pulse 1 |
| 7 | 0 | Scope synchro pulse 2 |

Notes:

1. Only one bit will be ON corresponding to the program level executing when the level 1 interrupt was taken.
2. Bypass CCU checkstop mode bit is not set by the control program. This bit is for potential use by diagnostics only.
3. When there is contention between set and reset bits, the set has priority.

| High-Resolution Timer X'7A' | Input: (LS) Address Pointer | Output: |
|--------------------------------|--------------------------------|-------------------------------------|
| Byte X, Bit 0 | 0 | Not significant |
| 1 | 0 | Not significant |
| 2 | Timer bit 0 | Not significant |
| 3 | Timer bit 1 | Not significant |
| 4 | Timer bit 2 | Not significant |
| 5 | Timer bit 3 | Not significant |
| 6 | Timer bit 4 | Not significant |
| 7 | Timer bit 5 | Not significant |
| Byte 0, Bit 0 | Timer bit 6 | 1 = Reset timer or enable count |
| 1 | Timer bit 7 | 0 = High-resolution, 1 = low resol. |
| 2 | Timer bit 8 | 0 = Timer, 1 = utilization count |
| 3 | Timer bit 9 | Not significant |
| 4 | Timer bit 10 | Not significant |
| 5 | Timer bit 11 | Not significant |
| 6 | Timer bit 12 | Not significant |
| 7 | Timer bit 13 | Not significant |
| Byte 1, Bit 0 | Timer bit 14 | Not significant |
| 1 | Timer bit 15 | Not significant |
| 2 | Timer bit 16 | Not significant |
| 3 | Timer bit 17 | Not significant |
| 4 | Timer bit 18 | Not significant |
| 5 | Timer bit 19 | Not significant |
| 6 | Timer bit 20 | Not significant |
| 7 | Timer bit 21 | Not significant |

| X'7B' | Input: Branch Trace (LS) Address Pointer | Output: Set PCI Level 2 |
|---------------|---|-------------------------|
| Byte X, Bit 0 | Branch trace address bit X.0 | Not significant |
| 1 | Branch trace address bit X.1 | Not significant |
| 2 | Branch trace address bit X.2 | Not significant |
| 3 | Branch trace address bit X.3 | Not significant |
| 4 | Branch trace address bit X.4 | Not significant |
| 5 | Branch trace address bit X.5 | Not significant |
| 6 | Branch trace address bit X.6 | Not significant |
| 7 | Branch trace address bit X.7 | Not significant |
| Byte 0, Bit 0 | Branch trace address bit 0.0 | Not significant |
| 1 | Branch trace address bit 0.1 | Not significant |
| 2 | Branch trace address bit 0.2 | Not significant |
| 3 | Branch trace address bit 0.3 | Not significant |
| 4 | Branch trace address bit 0.4 | Not significant |
| 5 | Branch trace address bit 0.5 | Not significant |
| 6 | Branch trace address bit 0.6 | Not significant |
| 7 | Branch trace address bit 0.7 | Not significant |
| Byte 1, Bit 0 | Branch trace address bit 1.0 | Not significant |
| 1 | Branch trace address bit 1.1 | Not significant |
| 2 | Branch trace address bit 1.2 | Not significant |
| 3 | Branch trace address bit 1.3 | Not significant |
| 4 | Branch trace address bit 1.4 | Not significant |
| 5 | Branch trace address bit 1.5 | Not significant |
| 6 | Branch trace address bit 1.6 | Not significant |
| 7 | Branch trace address bit 1.7 | Not significant |

| X'7C' | Input: Branch Trace (LS) Buffer Count | Output: Set PCI Level 3 |
|---------------|--|-------------------------|
| Byte X, Bit 0 | 0 | Not significant |
| 1 | 0 | Not significant |
| 2 | 0 | Not significant |
| 3 | 0 | Not significant |
| 4 | 0 | Not significant |
| 5 | 0 | Not significant |
| 6 | 0 | Not significant |
| 7 | 0 | Not significant |
| Byte 0, Bit 0 | <div style="display: flex; align-items: center;"> <div style="border-left: 1px solid black; border-right: 1px solid black; height: 100px; margin: 0 10px;"></div> <div style="text-align: center;">Note</div> </div> | Not significant |
| 1 | | Not significant |
| 2 | | Not significant |
| 3 | | Not significant |
| 4 | | Not significant |
| 5 | | Not significant |
| 6 | | Not significant |
| 7 | | Not significant |
| Byte 1, Bit 0 | | Not significant |
| 1 | | Not significant |
| 2 | | Not significant |
| 3 | | Not significant |
| 4 | | Not significant |
| 5 | | Not significant |
| 6 | | Not significant |
| 7 | | Not significant |

Note: Binary indication of branch trace buffer size in number of bytes. Actual length is a multiple of 8 bytes; bits 1.5, 1.6, and 1.7 are ignored by the branch trace mechanism.

CCU Hard Errors

| X'7D' | Input: CCU Hard Errors | Output: Set PCI Level 4 |
|---------------|--------------------------|-------------------------|
| Byte X, Bit 0 | 0 | Not significant |
| 1 | 0 | Not significant |
| 2 | 0 | Not significant |
| 3 | 0 | Not significant |
| 4 | 0 | Not significant |
| 5 | 0 | Not significant |
| 6 | 0 | Not significant |
| 7 | 0 | Not significant |
| Byte 0, Bit 0 | POP parity error | Not significant |
| 1 | MDOR parity error | Not significant |
| 2 | MIOC parity error | Not significant |
| 3 | Storage error 1 | Not significant |
| 4 | Cache/CCU error | Not significant |
| 5 | Cache/SCTL error | Not significant |
| 6 | Storage error 2 | Not significant |
| 7 | Local store parity error | Not significant |
| Byte 1, Bit 0 | Cache internal error | Not significant |
| 1 | A/B bus parity error | Not significant |
| 2 | D1 register parity error | Not significant |
| 3 | Not significant | Not significant |
| 4 | SAR parity error | Not significant |
| 5 | ROS parity error | Not significant |
| 6 | Z register parity error | Not significant |
| 7 | D2 register parity error | Not significant |

Note: Byte 0, bits 3 and 6 are encoded:
 If the value is 01 = interface error
 If the value is 10 = SCTL internal error
 If the value is 11 = unrecoverable storage error.

| X'7E' | Input: Level 1 Interrupt Requests | Output: Set Interrupt Mask |
|---------------|--------------------------------------|-------------------------------|
| Byte X, Bit 0 | 0 | Not significant |
| 1 | 0 | Not significant |
| 2 | 0 | Not significant |
| 3 | 0 | Not significant |
| 4 | 0 | Not significant |
| 5 | 0 | Not significant |
| 6 | 0 | Not significant |
| 7 | 0 | Not significant |
| Byte 0, Bit 0 | MOSS inoperative | Not significant |
| 1 | CCU hard error summary | Not significant |
| 2 | IOC-line adapter | Not significant |
| 3 | Level 5 IO error | Not significant |
| 4 | Invalid operation | Not significant |
| 5 | IOC-channel adapter | Not significant |
| 6 | Not significant | Not significant |
| 7 | IOC level 1 summary | Not significant |
| Byte 1, Bit 0 | Address compare level 1 | Not significant |
| 1 | Address exception inst.fetch | Adapter level 1 request |
| 2 | Storage protection inst.fetch | Level 2 request |
| 3 | Address exception pgm.exec. | Level 3 request |
| 4 | Storage protection pgm.exec. | Level 4 request |
| 5 | Not significant | Program level 5 execution |
| 6 | IPL level 1 | Not significant |
| 7 | Not significant | Not significant |

Notes:

1. For CCU hard error summary see input X'7D'.
2. For IOC level 1 see input X'76'.

When the CCU executes the input X'76' instructions, it places IOC level 1 interrupt requests into byte 0.

| X'7F' | Input: CCU Level 2, 3, or 4 Interrupt Requests | Output: Reset Interrupt Mask |
|---------------|--|------------------------------|
| Byte X, Bit 0 | 0 | Not significant |
| 1 | 0 | Not significant |
| 2 | 0 | Not significant |
| 3 | 0 | Not significant |
| 4 | 0 | Not significant |
| 5 | 0 | Not significant |
| 6 | 0 | Not significant |
| 7 | 0 | Not significant |
| Byte 0, Bit 0 | PCI level 2 | Not significant |
| 1 | MOSS diagnostic level 2 | Not significant |
| 2 | MOSS diagnostic level 3 | Not significant |
| 3 | MOSS request SVC level 4 | Not significant |
| 4 | MOSS response SVC level 4 | Not significant |
| 5 | 0 | Not significant |
| 6 | CE/Operation int.req.level 3 | Not significant |
| 7 | PCI level 4 | Not significant |
| Byte 1, Bit 0 | 0 | Not significant |
| 1 | 0 | Adapter level 1 request |
| 2 | 0 | Level 2 request |
| 3 | 0 | Level 3 request |
| 4 | 0 | Level 4 request |
| 5 | Interval timer level 3 | Program level 5 execution |
| 6 | PCI level 3 | Not significant |
| 7 | SVC level 4 | Not significant |

Hardware Registers

Hardware registers are used to store and pass information essential to controller operation. Some of these hardware registers are available to the control program as external register addresses through the use of input and output instructions.

Instruction Address Register (IAR): See 'General Registers' above.

Lagging Address Register (LAR): The LAR is loaded from the IAR at the beginning of each instruction execution. The lagging address register is a 'came from' register. When displayed by the operator or by the program using input X'74' or MOSS indirect input X'74', it contains the address of the last instruction executed prior to the instruction that is currently being executed if any (this might not be true in case of error. Refer to *Principles of Operations Manual* for more information).

The control program can load the contents of the LAR into a general register by executing an input X'74' instruction. The control program can then either examine the contents of the general register or display the address on the control panel by using the general register as input to the display registers.

Operation Register (OP Register): The operation register is used to hold the first 16 bits of the instruction being executed. This register can be displayed on the control panel.

Storage Address Register (SAR): The storage address register contains the storage address currently used or last used.
The contents of the SAR can be displayed on the control panel.

Program Display Register 1: This register in local storage (LS address X'79') contains a parameter passed from the program running in the CCU to the program running in MOSS for eventual display as display register 1, to an operator.
It can be loaded by executing an output X'71' instruction.

Program Display Register 2: This register in local storage (LS address X'7A') contains a parameter passed from the program running in the CCU to the program running in MOSS for eventual display as display register 2 to an operator.
It can be loaded with data by executing an output X'72' instruction.

Operator Address/Data Value Register: This register in local storage (LS address X'71') contains a parameter passed from the program running in MOSS to the program running in the CCU when an operator wishes to express an address or data value.
It can be read by executing an input X'71' instruction.

Operator Function Select Value Register (16 Bits): This register in local storage (LS address X'72') contains a parameter passed from the program running in MOSS to the program running in the CCU when an operator wishes to express a selected function value.
It can be read by executing an input X'72' instruction.

Maintenance Temporary Address Register (MTAR): This register in local storage (LS address X'7E') contains the main storage address used by any operation initiated by the program running in MOSS and involving main storage.

Maintenance Temporary Data Register (MTDR): This register in local storage (LS address X'7F') contains information read out of main storage for the operations described for the maintenance temporary address register(MTAR) (see above).

CCU to and from MOSS

The CCU interconnects with the MOSS via the MOSS input and output controller (MIOC) logic located in the PUC (part of the CCU).

The MIOC enables the MOSS to:

- Read or write any register or storage location in the CCU.
- Set or reset all CCU latches and read out their status.
- Interrupt the CCU (CCU hardware errors, IPL request, and so on)

Also, the MIOC allows the CCU to interrupt the MOSS.

CCU Diagnostics

The CCU has diagnostic facilities designed to allow the program to perform test procedures on the controller hardware. The test routines can be either part of the online control program or a stand-alone control program used for testing purposes only. If these test routines are part of the online control program, the telecommunication lines and adapters not being tested are allowed to continue operating.

The following operations are available for program use:

Set and Reset the Bypass CCU Check Stop Mode: Output X'79', byte 1, bit 4 set to 1 prevents CCU hard stop and MOSS interrupt from being set due to a CCU hard check. To reset the bypass mode, the control program must execute an output X'79' instruction with byte 1, bit 5 set to 1.

However, MOSS can also issue a bypass CCU check stop or a CCU hard stop. The following table shows the resulting CCU mode.

| MOSS | Program | CCU Mode Result |
|---------------------|---------|-----------------|
| - | - | Normal (2) |
| - | Bypass | Bypass |
| Bypass | - | Bypass |
| Bypass | Bypass | Bypass |
| Bus stop (1) | - | Normal (2) |
| Bus stop (1) | Bypass | Normal (2) |
| Bus stop and bypass | | Bypass |

Notes:

1. Adapter interface check stop causes adapter interface errors to be handled as hard errors.
2. See "CCU Error Handling" and "Program Errors" on page 2-43 for more information.

Set and Reset the Level 1 Adapter Mask: Program level 1 interrupt requests caused by a check condition in an adapter (scanner or CA) can be masked by using an output X'7E', byte 1, bit 1. To unmask the level 1 requests, the control program must execute an output X'7F' (reset mask bits) with byte 1, bit 1 set to 1.

CCU Error Handling

The following are the basic principles of the CCU error handling strategy:

CCU-Detected Hardware Errors: They are high-severity errors, usually hardware failures. They stop the CCU. No retry is performed. The error indication latches are sensed by MOSS through the LSSD path.

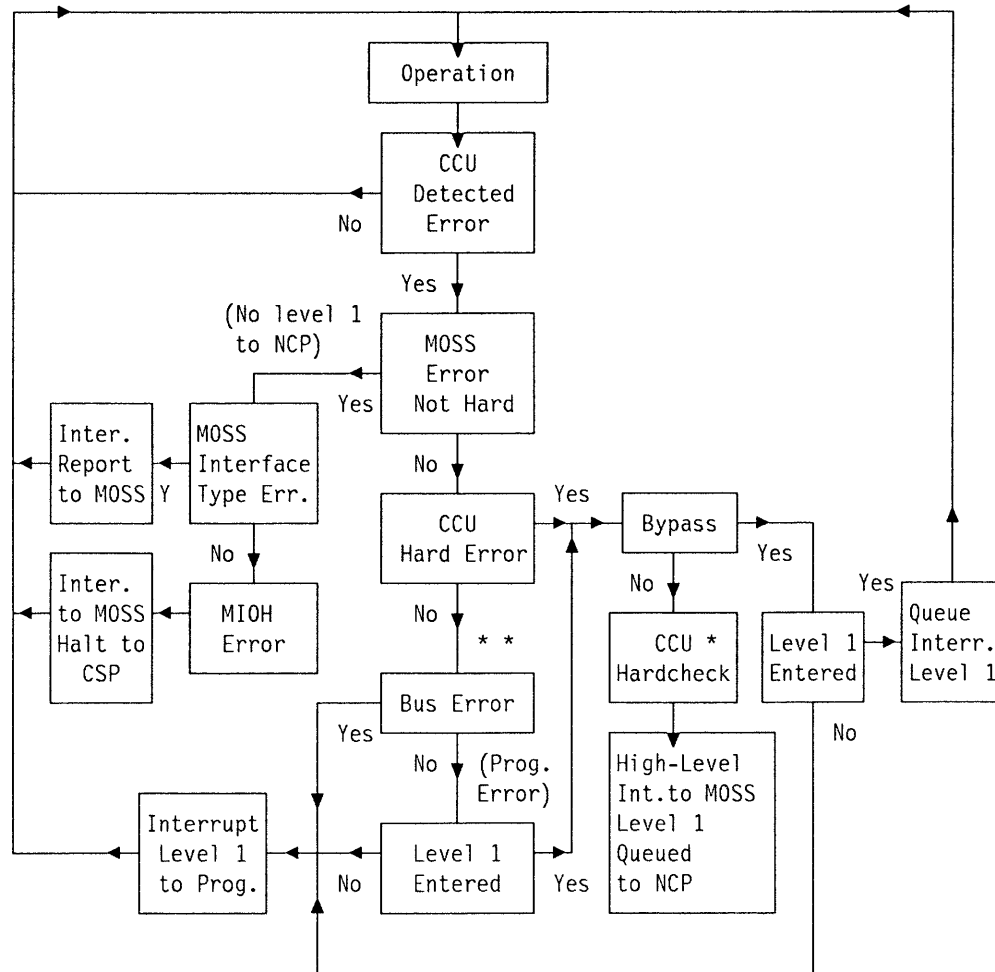
CCU-Detected Not Hard Errors: They are low-severity errors, either program errors, or IOC bus errors, or MOSS 'interconnection' errors. They do not stop the CCU. They can be encountered during the following operations:

1. MOSS operations through the MIOC or adapter operations (AIOs) performed with the MOSS flag.
These errors are reported to MOSS only.
2. Program instructions and adapter operations (non-MOSS):
These errors are reported to the program only.

Checking the Checkers

All checkers can be checked by the LSSD scan path.

CCU Error Handling Summary



- Notes:** *
- * CCU hard check results in stopping the program, AIOs, and branch trace.
 - ** Bus error without adapter interface check stop mode.

CCU Error Detection

Hardware Errors

Control ROS Parity Error: Parity error detected on one of the CCU control word registers (latches receiving one ROS field).

MOSS Data Operand Register (MDOR) Parity Error: Parity error during a read MDOR operation on the MDOR-to-MOSS bus.

MIOC Parity Error: Parity error during MOSS write operation.

Local Storage Parity Error: Parity error detected on data bytes 0 or 1 of the local storage during a read operation. (Possible parity error on byte X is not detected.)

D1/D2 Register Parity Errors (Two Errors): Parity error detected in the IOC D register after each register setting (except when set from adapter bus which results in putting the bus in parity check).

Z Register Parity Error: Parity error detected on any byte X 0 or 1 in the Z register except during input X'7X' instruction execution.

POP Parity Error: Parity error detected in the pre-OP register (containing the pre-fetched instruction) before transferring its contents to the OP register.

SAR Parity Error: Parity error detected in the storage address register at any time.

For other parity errors, see "CCU Hard Errors" on page 2-36.

Notes:

1. At storage initialization time unrecoverable storage errors are inhibited and storage write operations are not prevented when ECC disable is set (see OUT X'74').
2. A CCU clock check is also provided. This check activates an error condition latch in the MOSS.

Handling

These errors are latched inside the CCU. A CCU hard check condition is detected, which stops the CCU, that is:

- Program stop
- AIO stop
- Hard stop
- MOSS direct operations are allowed. Indirect MOSS operations may be performed if the CCU is in bypass hard stop mode.

A high-level interrupt is sent to the MOSS.

An interrupt level 1 to the control program is queued but not executed unless in bypass check stop mode.

When the CCU is stopped the LSSD path is used by the MOSS to collect the error information from the CCU error latches through the 'scan out' line.

This error information can be made available to the operator by MOSS.

When these error latches are set by errors (not forced by diagnostics) they are unavailable to the control programs which reside in main storage.

After error information collection, MOSS may cause a re-IPL to take place.

Program Errors

Storage Protect Program Execution Error: Storage protect keys mismatch or read-only key violation during a program storage instruction.

Address Exception Program Execution Error: Program attempt to read or write uninstalled storage.

Storage Protect Instruction Fetch Error: Attempt to execute an instruction fetched from a storage area whose key did not match the program user key.

Address Exception Instruction Fetch Error: Attempt to execute an instruction fetched from an uninstalled storage location.

Level 5 I/O Error: Attempt to perform an input or output instruction in program level 5.

Invalid OP-Code: Attempt to execute an instruction with an OP-code that does not compare to any of the 53 valid OP-codes, or input, or output instruction to invalid external register addresses.

Handling

These errors result in an interrupt level 1 sent to the control program except if already in program level 1 (in this case a CCU hard check condition occurs).

Error information can be obtained by the control program using the input X'7E' instruction (see "Input Instructions" on page 2-24).

However, storage protect or address exception errors are unrecoverable in program execution (load or store instruction) because, in some cases, the next instruction will be executed before the interrupt to program level 1.

For details on DMA storage protect, see Chapter 5, "High Performance Transmission Subsystem (HPTSS)" on page 5-1.

Adapters Interconnection Errors

IOC Adapter Bus Parity Error: Parity error detected when reading the IOC bus.

IOC Time-Out Error: Erroneous timing sequence on IOC interface.

IOC Adapter CCW Error: Invalid channel control word coming from the adapter.

IOC Storage Protect Error: Storage protect violation detected during an adapter-initiated operation (AIO) write.

IOC Address Exception Error: Attempt to read or write storage not installed during an adapter-initiated operation.

Notes:

1. Parity and time-out errors can be encountered with program user (IOH, IOHI) or with MOSS user (MIOH).
2. All errors can be encountered with AIOs.
3. In adapter interface check stop mode these bus errors are handled as hard errors.

Handling

With Program User (IOH, IOHI): These errors result in an interrupt level 1 sent to the program, and a halt signal is sent to the adapter. Error information can be obtained by the control program, using the input X'7E' and input X'76' instructions.

With MOSS User (MIOH): (MOSS IOCs OP error)

These errors result in a high-level interrupt to MOSS and a halt signal is sent to the adapter. No level 1 interrupt will be issued by the LAs in this case. Error information can be obtained by MOSS, using the input X'76' instruction.

During Program AIOs: These errors result in an interrupt level 1 to the control program and a halt signal is sent to the adapter. No level 1 interrupt will be issued to the MOSS by the LAs.

Error information can be obtained by the control program, using input X'7E' and input X'76' instructions.

The adapter address will be obtained by the program, using the input X'75' instruction which allows sensing the CCW bits.

During MOSS AIOs: These errors during an adapter AIO operation for MOSS will result in a halt signal sent to the adapter. These AIOs are differentiated from the program AIOs by bit 1.0 of the CSCW which is set ON for MOSS.

A high-level interrupt is sent to MOSS, if the error occurs after the CCW is transferred.

Adapter Interface Check Stop Mode: When the CCU is in adapter interface check stop mode, that is, when MOSS has sent the adapter interface check stop bit, any IOC bus error encountered with any user will be handled like a hard error.

Notes:

1. Error detected during MOSS operations (MIOH) are not reported to the control program.
2. Error detected during control program operations (MOSS AIOs) are not reported to the MOSS.

Summary of Actions Taken During AIOs and PIOs

| Event | Action In | | | |
|---|----------------------------|----------------------------|----------------------------|----------------------------|
| | AIO for Program | AIO for MOSS | IOH/IOHI | MIOH |
| AIO stop (by MOSS) | Mask ch.req. * | mask ch.req. * | Mask ch.req. * | Mask ch.req. * |
| SP/AE violation | Halt to add. level 1 | Halt to add HLIR to MOSS | Level 1 (when I fetch) | Not available |
| Add. compare stop | Mask ch.req. * | Mask ch.req. * | Mask ch.req. * | Not available |
| Adapter bus error (wo add. bus check stop mode) | Halt to add level 1 | Halt to add HLIR to MOSS | Halt to add level 1 | Halt to add HLIR to MOSS |
| Hard check | Halt to add mask ch.req. * | Halt to add mask ch.req. * | Halt to add mask ch.req. * | Halt to add Mask ch.req. * |

* "Mask ch.req." means "Mask channel request" for AIOs, that is, AIO stop is set.

MOSS Interconnection Type Errors

MOSS Interconnection Parity Error

- Parity error detected either on MOSS address bus or on MOSS data bus during a write operation.
- Parity error detected on MOSS address bus during a read operation.

MOSS OP Error: Moss initiates an indirect operation while the CCU busy bit is ON, meaning that CCU resources are already used for a previous MOSS indirect operation.

MOSS Address Exception Error: MOSS attempted to read or write storage which is not installed.

Handling

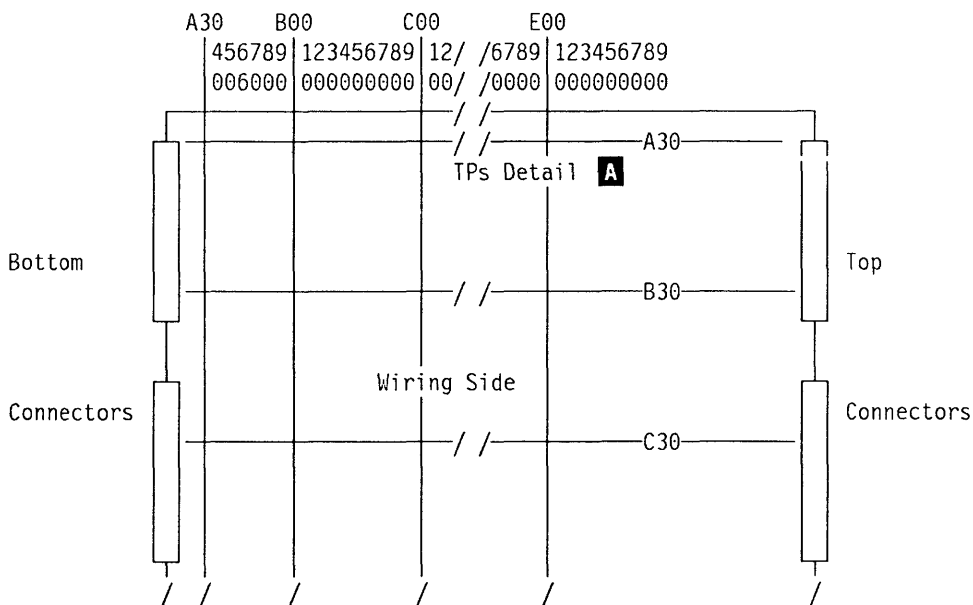
These errors result in a high-level interrupt to MOSS (for MOSS OP error and MOSS address exception error), or in a signal returned to MOSS through an interface line (for MOSS interface parity error).

Performance Test Points

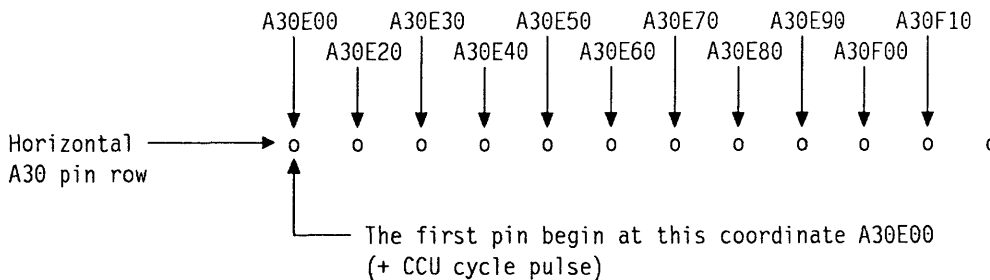
The performance test points (TPs) (see the list on the following table), located on the PUC card, may be used to scope or to count the internal events with the appropriate tools.

| Signal Name | Physical Pin Coordinate | Signal Name | Physical Pin Coordinate |
|------------------------|-------------------------|------------------------|-------------------------|
| + CCU cycle pulse | A30E00 | - Latched scope sync 1 | A30F00 |
| Not used | A30E10 | - Latched scope sync 2 | A30F10 |
| - CCU level 1 | A30E20 | + MOSS current | A30F20 |
| - CCU level 2 | A30E30 | + Stop C clock latched | A30F30 |
| - CCU level 3 | A30E40 | - IOC1 IO tag | A30F40 |
| - CCU level 4 | A30E50 | - IOC1 AIO/hold | A30F50 |
| - CCU level 5 | A30E60 | Not used | A30F60 |
| - Any instruction | A30E70 | Not used | A30F70 |
| + Process ADDR compare | A30E80 | Spare pin | A30F80 |
| -IO wait | A30E90 | Spare pin | A30F90 |

The performance test points (TPs) are located on the wiring side of the PUC card (CCU). The following figure will help in locating the test points.



Test Points Detail **A**



Chapter 3. Buses

| | |
|---|------|
| The Buses in 3745 Data Flow | 3-2 |
| Generalities | 3-3 |
| IOC Bus | 3-3 |
| IOC Bus Protocol | 3-3 |
| CCU-Bus Layout (Maximum Configuration) | 3-4 |
| CCU/Adapters Interconnection | 3-5 |
| DMA Bus | 3-9 |
| PIO Operation | 3-14 |
| AIO Operation | 3-18 |
| Bus Propagation Cards (BPC1/BPC2) | 3-28 |
| Configuration Rules | 3-28 |
| Adapter Addressing | 3-29 |
| Logical Adapter Address | 3-29 |
| Physical Address Wiring | 3-29 |
| CA Addressing | 3-30 |
| Line Adapter Addressing (LSS and HSS) | 3-32 |
| LIC Board Addressing | 3-34 |
| Line Addressing | 3-35 |
| Token-Ring Adapter (TRA) Addressing | 3-42 |
| Token-Ring Line Addressing | 3-43 |
| Adapter Bypass Mechanism | 3-44 |
| For Line Adapters | 3-44 |
| For Channel Adapters | 3-44 |
| Cycle Steal Grant (CSG) and Autoselection Mechanism for Model 170 | 3-45 |
| IOC Bus Scoping Routine | 3-49 |
| How to Start the Routine | 3-49 |
| Adapter Selection | 3-50 |
| RACs Generated | 3-51 |
| Examples of Scoping Routine on Bus Terminator | 3-53 |
| Bus Terminator (TERMI) Connector Pin Assignments | 3-55 |

The Buses in 3745 Data Flow

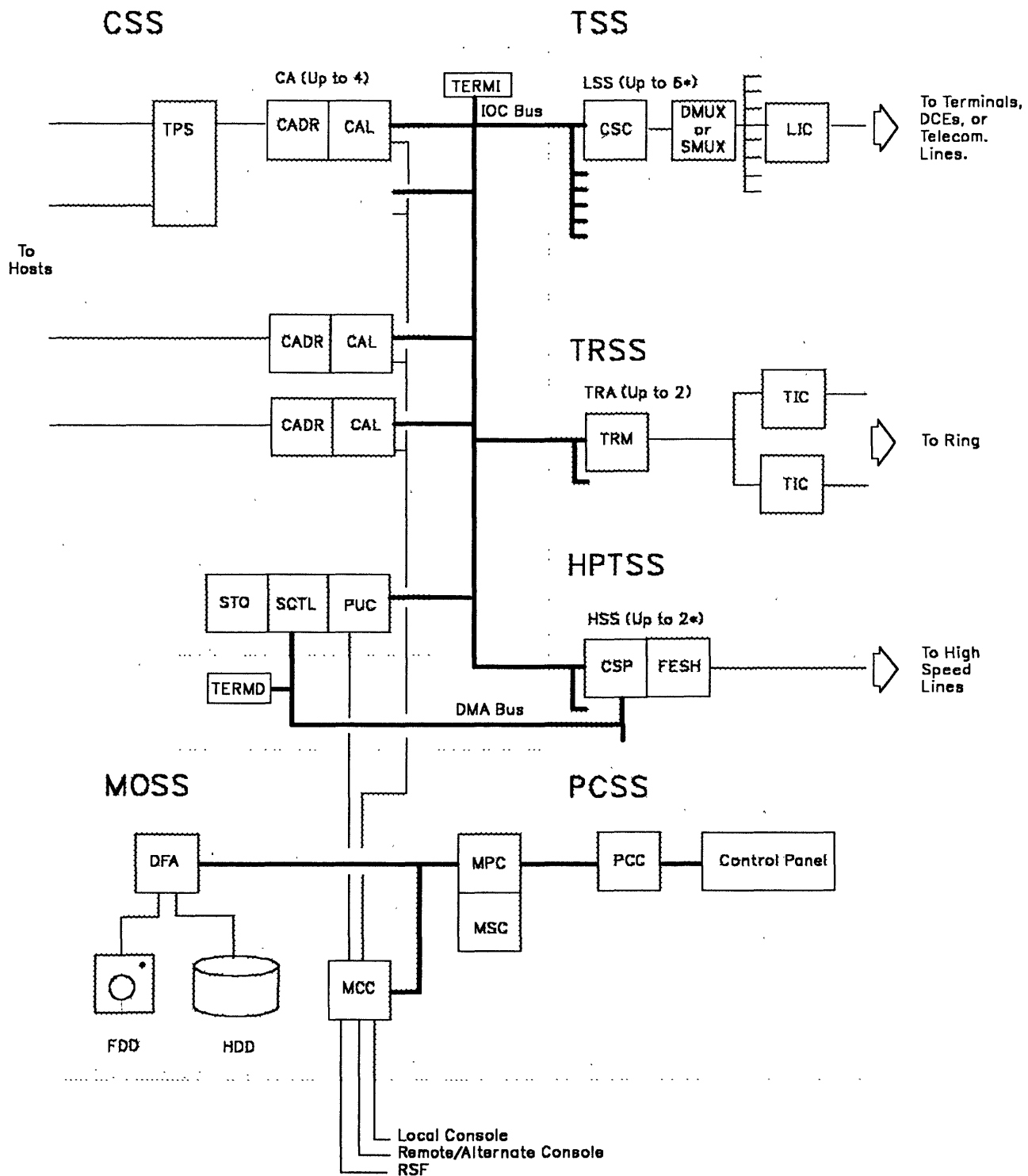


Figure 3-1. The Buses in 3745 Data Flow

Generalities

Two types of bus connect the adapters to the CCU/SCTL.

1. IOC bus: This bus connects the CCU to the adapters.
2. DMA bus: This bus connects the SCTL card to the high-speed adapters.
See "DMA Bus" on page 3-9.

IOC Bus

Data, address, and control information exchanges take place between the work registers and adapters attached to the IOC bus.

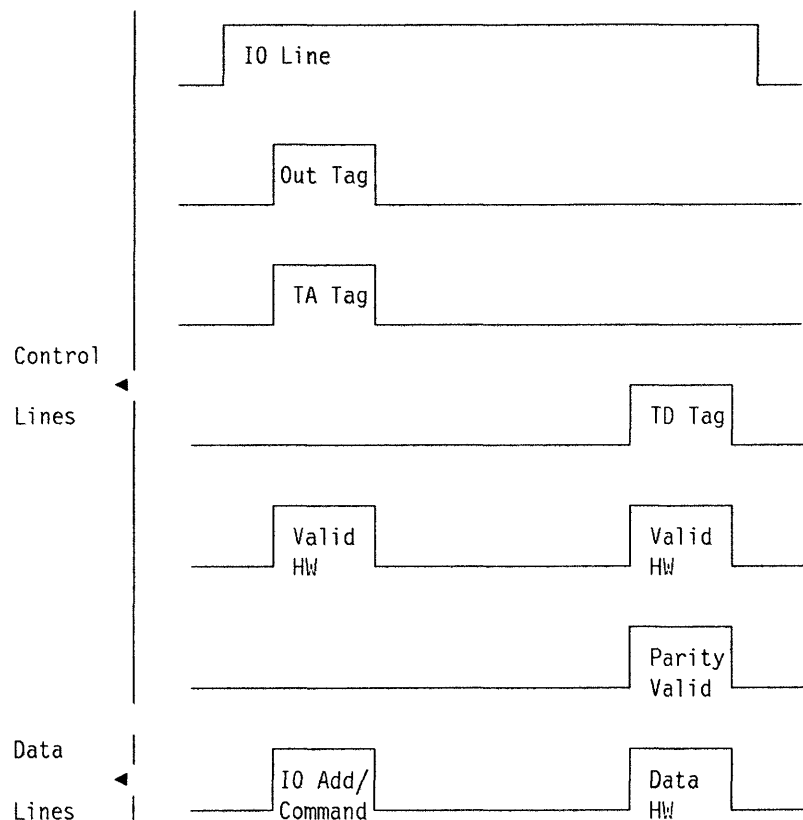
The IOC logic operates differently depending on whether the program initiates an operation (PIO), or the adapter initiates it (AIO).

In both operations, the A (address) and D (data) registers of the data flow controlled by the IOC logic act as buffers between the CCU(s) and the adapters (CAs and LAs).

The IOC bus carries interrupt requests from the adapters (levels 1, 2, and 3) when not busy with PIO or AIO operations.

IOC Bus Protocol

Read PIO example



CCU-Bus Layout (Maximum Configuration)

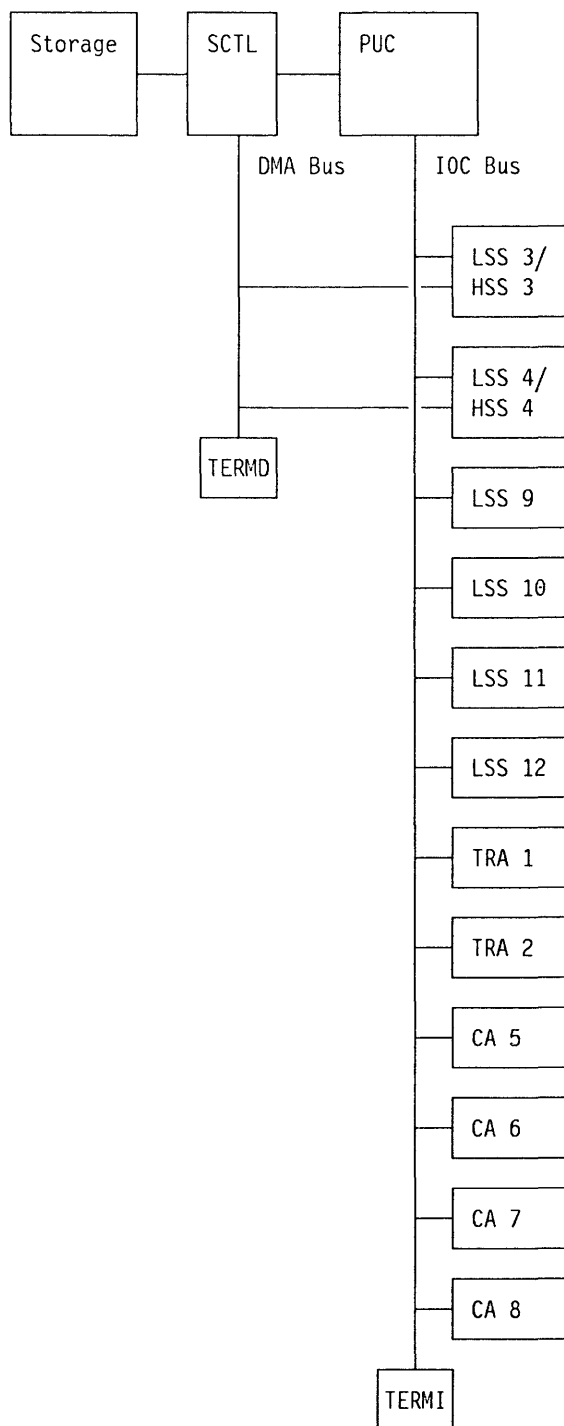


Figure 3-2. CCU-Bus Layout

CCU/Adapters Interconnection

Each interconnection consist of 18 bidirectional lines, (two data bytes plus two parity bits) and 16 tag and control lines.

For details on line function, see Figure 3-3.

For details on bus layout, see Figure 3-2 on page 3-4.

CCU Bus Line Function

| Line Function | Abbr | CCU | CA | LA |
|----------------------------|-------|-----|----|----|
| Address/Command Tag (1) | TA | x | . | . |
| Data Tag (1) | TD | x | . | . |
| Interrupt Req. Removed (1) | IRR | . | x | x |
| CS Req. High (1) | CSRH | . | . | x |
| CS Req. Low (1) | CSRL | . | x | . |
| CS Grant High (1) | CSGH | x | . | . |
| CS Grant Low (1) | CSGL | x | . | . |
| Input/Output (1) | I/O | x | . | . |
| Halt (1) | HLT | x | . | . |
| Out (1) | R/W | x | . | . |
| Valid Byte (1) | VB | . | x | x |
| Valid Halfword (1) | VH | . | x | x |
| End of Chain (1) | EOC | . | x | x |
| Modifier (1) | M | . | x | x |
| Parity Valid (1) | PV | . | x | x |
| CA IPL Detect (1) | CAIPL | . | x | . |
| Reset Tag (See Note 1) | RST | . | . | . |
| Data Byte 0 (9) OUT | DB0 | x | . | . |
| IN | DB0 | . | x | x |
| Data Byte 1 (9) OUT | DB1 | x | . | . |
| IN | DB1 | . | x | x |
| Scan Int (See Note 2) | SCI | . | . | x |

Legend:

(): The contents of the parentheses indicate the number of wires in line function

x : Signal generated

: Indicates where the signal arrives

Notes:

1. Reset line is activated directly from the MOSS.
2. Sent directly to MOSS (MCC card).

Figure 3-3. CCU-Bus Line Function

The following is a short description of each of the lines in the summary table above.

Address/Command Tag (TA): The 'TA' line is activated by the CCU to indicate that the adapter address is in data byte 0 and the command is in data byte 1.

Data Tag (TD): The 'TD' line is activated by the CCU to indicate that the data bus contains write data or that the CCU is ready to receive read data while the 'I/O' line is active.

When the 'I/O' line is not active, the 'TD' line is activated by the CCU to indicate that it is permissible to change the state of any interrupt request on the data bus.

Interrupt Request Removed (IRR): The 'IRR' line is activated by any adapter that has removed its interrupt request from the data bus. Each adapter should activate 'IRR' in response to the 'I/O' line being activated and, of course, remove its interrupt request from the data bus.

Each adapter should allow 'IRR' to change to the inactive level when the 'I/O' line is inactive.

When all the adapters have allowed 'IRR' to drop, this common 'IRR' line going inactive indicates to the CCU that all adapters have placed their interrupt requests, if any, on the data bus and that the CCU may now sample for interrupts.

Cycle Steal Request High (CSRH): A scanner activates 'CSRH' whenever it wishes to start an AIO operation.

The scanner keeps 'CSRH' active until it receives 'CSGH' (Cycle Steal Grant High).

Cycle Steal Request Low (CSRL): A channel adapter activates CSRL whenever it wishes to start an AIO operation.

The channel adapter keeps 'CSRL' active until it receives 'CSGL' (Cycle Steal Grant Low).

Cycle Steal Grant High (CSGH): The CCU activates 'CSGH' in response to 'CSRH' for the purpose of selecting a scanner for an AIO operation, and receiving a 'CSCW' from the selected scanner. 'CSGH' will be deactivated by the CCU when 'valid halfword' is received from the scanner.

Cycle Steal Grant Low (CSGL): The CCU activates 'CSGL' in response to 'CSRL' for the purpose of selecting a channel adapter for an AIO operation, and receiving a 'CSCW' from the selected channel adapter. 'CSGL' will be deactivated by the CCU when 'valid halfword' is received from the channel adapter.

Input/Output (I/O): The 'I/O' line is activated by the CCU to indicate either that an I/O operation is about to start on the IOC bus, or that one is in progress.

For any I/O operation, 'I/O' is the first line activated and the last one deactivated.

When the 'I/O' line is active, all adapters should remove any interrupt requests on the data bus until the I/O is deactivated.

Halt (HLT): The CCU activates the 'halt' line to indicate to the selected adapter that the CCU has detected an error condition associated with the current operation.

The CCU will activate the 'halt' line after 'TA', 'CSGH', or 'CSGL' has been deactivated. The CCU will deactivate the 'halt' line when it deactivates the 'I/O' line. The selected adapter will terminate the current operation and set a check bit active in its status register.

Out (R/W): The CCU activates the 'out' line, while the 'I/O' line is active, to indicate that the direction of information on the data bus is outbound from the CCU. The CCU deactivates the 'Out' line to indicate that the direction of information on the data bus is inbound to the CCU.

Valid Byte (VB): A selected adapter will activate the 'valid byte' line during an AIO operation to indicate a byte transfer instead of a halfword transfer. The valid byte of information will be data bus byte 1.

Valid Halfword (VH): In some places the term 'valid' is used in place of 'valid halfword'. A selected adapter will activate the 'valid halfword' line in response to the activation of the 'TA', 'TD', 'CSGH', or 'CSGL' line from the CCU. 'Valid halfword' line active indicates that the adapter has either placed information on the data bus or has received information from the data bus. It also indicates that the CCU may deactivate its control line.

All adapters will activate 'valid halfword' when the CCU deactivates the 'I/O' line, and deactivate 'valid halfword' when the CCU activates the 'I/O' line.

The CCU will proceed with an IO operation after all adapters have deactivated 'valid halfword'. A selected adapter will activate the 'end of chain' line instead of 'valid halfword' for the last halfword transfer of an AIO operation.

End of Chain (EOC) 'End of chain' active indicates that the AIO operation should be concluded and that the adapter has either placed information on the data bus or has received information from the data bus.

Modifier (M): A selected adapter will activate the 'modifier' line with 'valid byte' line for the last byte transfer of a AIO operation.

'Modifier' line active at this time indicates that the AIO operation should be concluded.

Parity Valid (PV): A selected adapter will activate 'parity valid' to indicate to the CCU that it wishes to have parity checking of data inbound to the CCU.

If 'parity valid' is active and bad parity is detected by the CCU, the CCU will activate the 'halt' line.

If 'parity valid' is deactivated and bad parity is detected by the CCU, the parity is corrected, the data is stored, and a status bit is set.

CA IPL Detect (CAIPL): A CA adapter will activate this line when it detects a "WRITE IPL" command on the host interface. When the CCU receives this signal it will raise a Level 1 interrupt to MOSS.

Reset (RST): The MOSS may activate the 'reset' line at any time to initialize all adapters. This initialization will cause all adapters to immediately terminate current operations, go to a ready state, and prepare to respond to PIO commands.

Data bus bytes 0 and 1: The data bus is halfword wide with 18 bidirectional lines. Each of the two bytes (0 and 1) contains 8 bits plus a parity bit (0-7,P).

Information is transferred between the CCU and the adapters in either direction when the 'I/O' line is active.

Four bits of the bus are used for an additional function when the 'I/O' line is deactivated, as follows:

- Byte 0 bit 1 = LAs Level 2 interrupt request to CCU.
- Byte 0 bit 5 = CAs Level 1 interrupt request to CCU.
- Byte 1 bit 0 = CAs Level 3 interrupt request to CCU.
- Byte 1 bit 5 = LAs Level 1 interrupt request to CCU.

The adapters activate their interrupt requests to the CCU using these paths, but only when the 'I/O' line is inactive.

The CCU will sample the data bus for interrupts after activating the 'TD' line, while the 'I/O' line is inactive.

Scanner Interrupt (Scan Int): Interrupt level 4 generated by the line adapter to the MOSS (MPC).

Physical Interconnection

The physical interconnection is made by board wiring.

See Figure 3-2 on page 3-4.

DMA Bus

This bus is used to transfer data from/to CCU storage to/from the high-speed adapters (FESH cards).

This DMA bus is routed from the SCTL card to the FESH card(s).

See Figure 3-4 for details.

Physical Interconnection

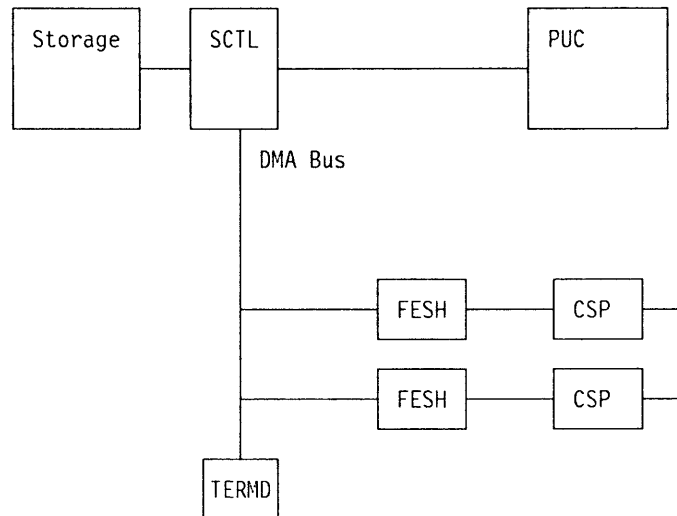
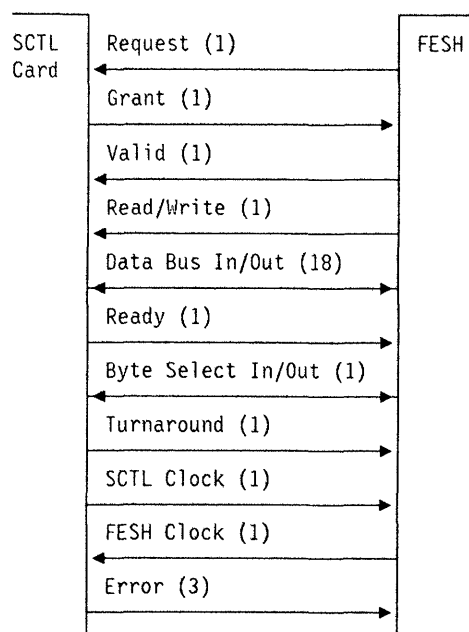


Figure 3-4. DMA Bus Physical Interconnection

Interconnection Layout



(): The figure in parentheses indicates the number of wires in the line function.

Figure 3-5. DMA Bus Interconnection Layout

DMA-to-SCTL Bus Line Function

| Line Function | SCTL | FESH |
|---------------------|------|------|
| Request (1) | . | x |
| Grant (1) | x | . |
| Valid (1) | . | x |
| Read/Write (1) | . | x |
| Data Bus (18) Out | x | . |
| In | . | x |
| Ready (1) | x | . |
| Byte Select (1) Out | x | . |
| In | . | x |
| Turnaround (1) | x | . |
| SCTL Clock (1) | x | . |
| FESH Clock (1) | . | x |
| Error (3) | x | . |

Legend:

(): The figure in parentheses indicates the number of wires in the line function.
 x : Signal from.

Figure 3-6. DMA Bus Line Function

The following is a short description of each of the lines in the preceding summary tables.

Request: Each request indicates that a FESH requests a DMA service (such as a Write or Read data transfer). Write means that storage will be written. Read means that storage data will be sent to the adapter.

Grant: Each grant indicates an answer to a request.

Valid: Indicates that the grant has been taken into account by the adapter and that the DMA data transfer can start.

Read/Write: Indicates the direction of the DMA data transfer.

Data bus: 18 bidirectional lines. Used to transfer the CCU address and burst length from the selected adapter, and to support the data transfers.

Ready: It is an envelope of the actual data transfer, (if the ready bit is ON there is a data transfer).

Byte Select: One bidirectional line. Indicates that only one byte is transferred in the last halfword data transfer.

Turnaround: Indicates a read data transfer.

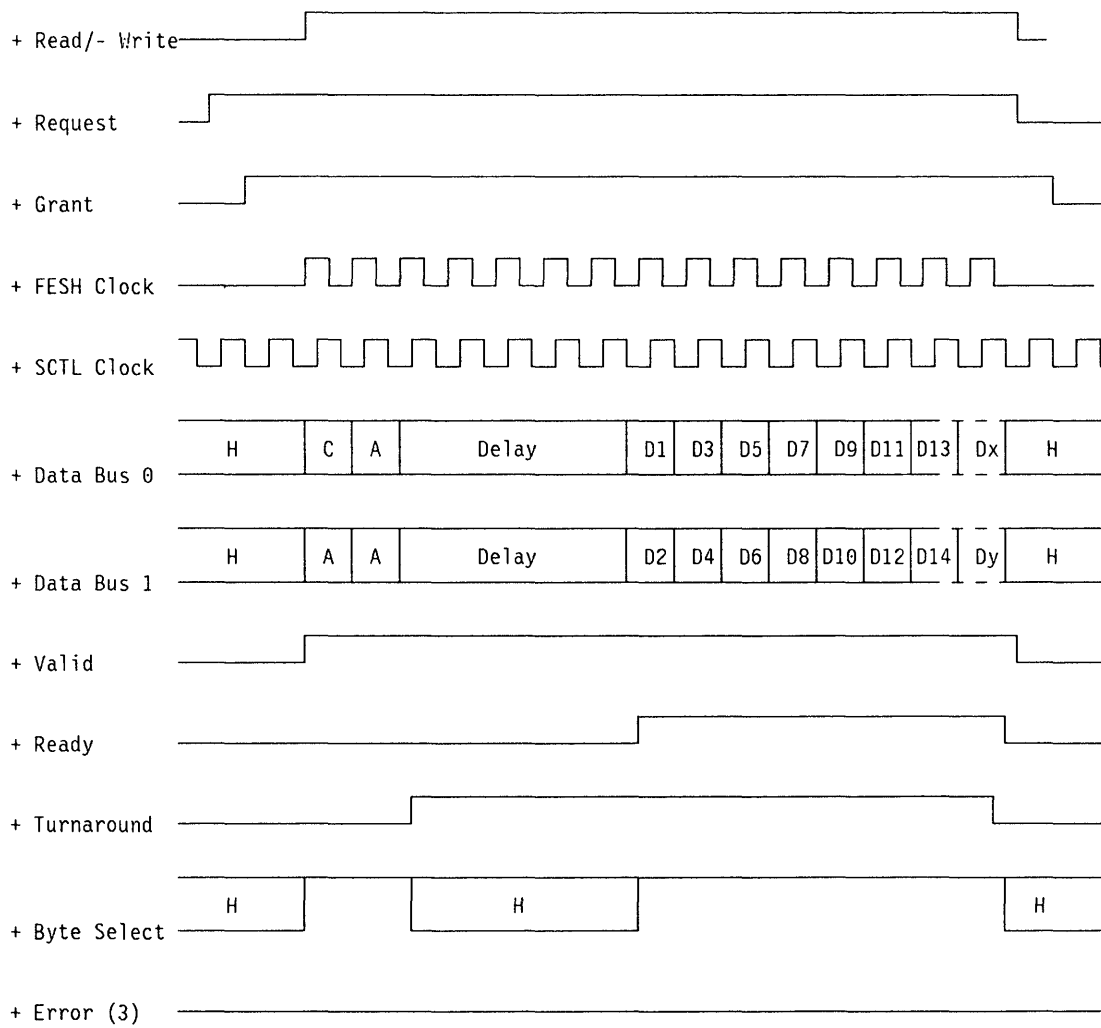
SCTL Clock: Synchronizes the DMA bus operations.

FESH Clock: It consists in the SCTL clock gated by the valid tag in the FESH.

Errors: Used to report errors to the adapter.

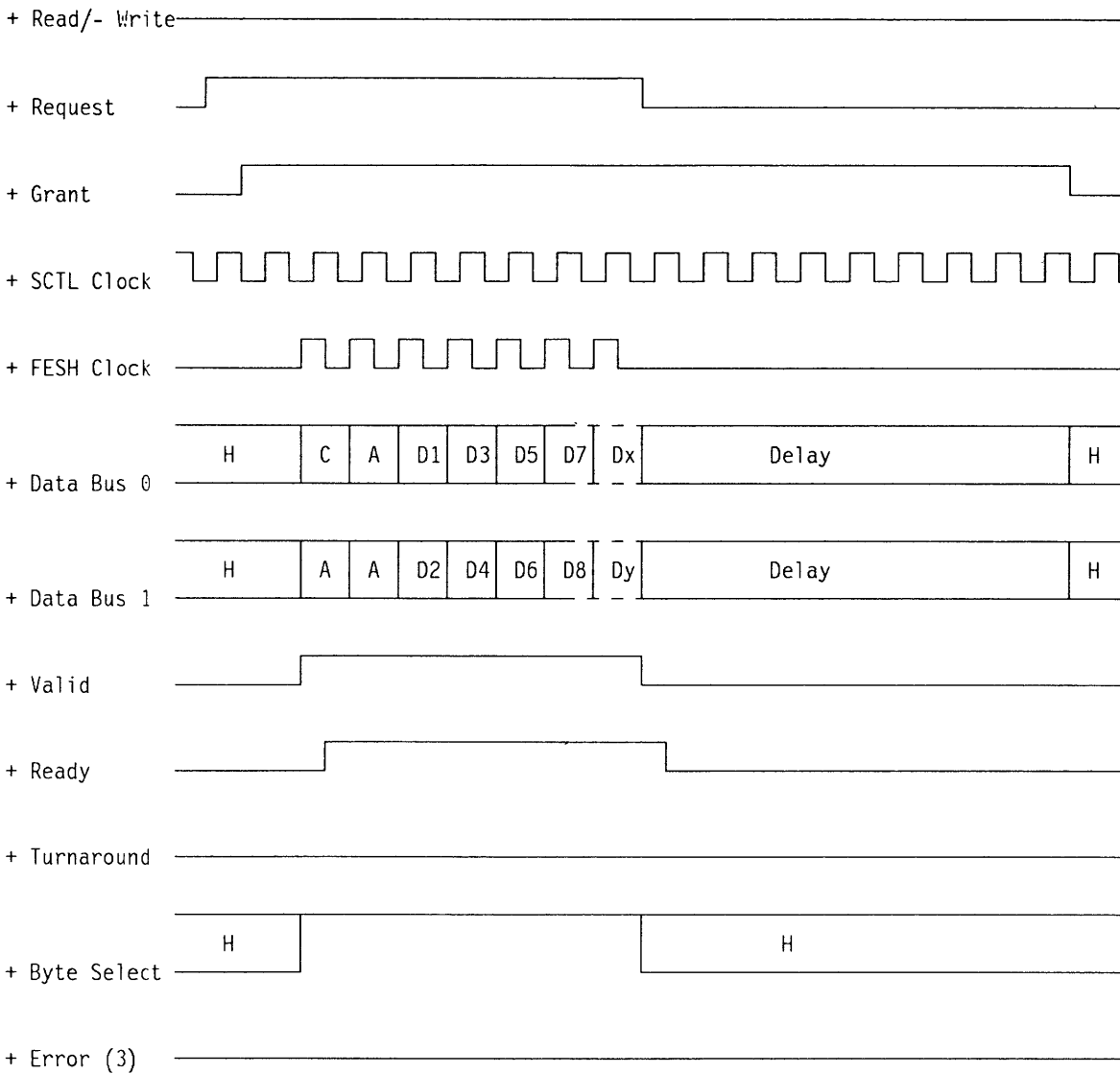
See Chapter 5, "High Performance Transmission Subsystem (HPTSS)" on page 5-1 for details.

DMA Bus During Read Operation



A = Address
 C = Count
 D = Data
 H = High-impedance driver 3 states
 Delay = Delay to transfer data from storage

DMA Bus During Write Operation



A = Address
 C = Count
 D = Data
 H = High-impedance driver 3 states
 Delay = Delay to transfer data to storage

PIO Operation

PIO Operation Sequence

A PIO operation to control a channel or an LA operation may be started either by the control program in the CCU, or by the microcode in the MOSS.

PIO Initiated by the CCU

During such an operation two halfwords (address, command, and data) are exchanged with a selected adapter.

A PIO operation has four steps:

1. IOH or IOHI instruction decode
2. IOC initialization
3. Adapter addressing and selection
- 4 Data transfer:

Write = from CCU

Read = to CCU

At step 1:

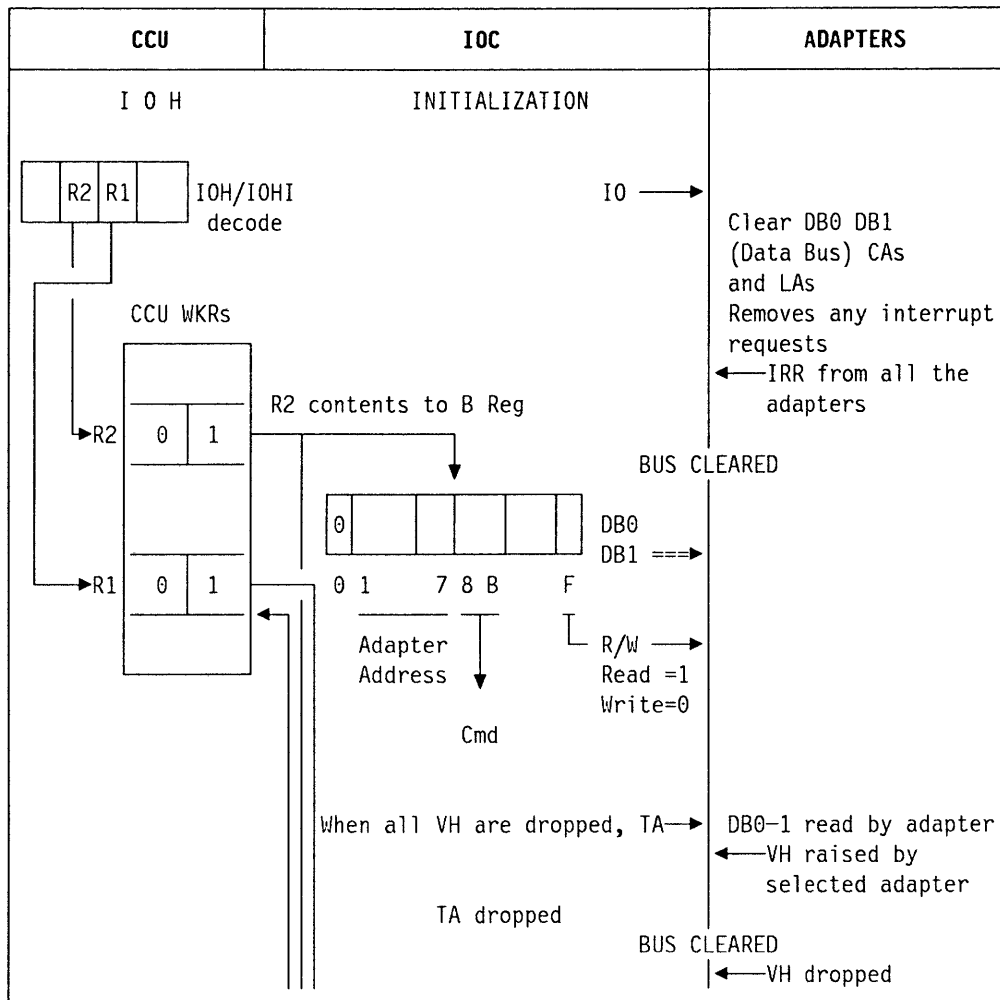
- Instruction code 50 = IOH with R1 and R2.
- Instruction code 70 = IOHI with R1 and the second halfword of the instruction whose contents go into the D register.

PIO Initiated by the MOSS

MIOH/MIOHI instructions are equivalent to IOH/IOHI instructions except that:

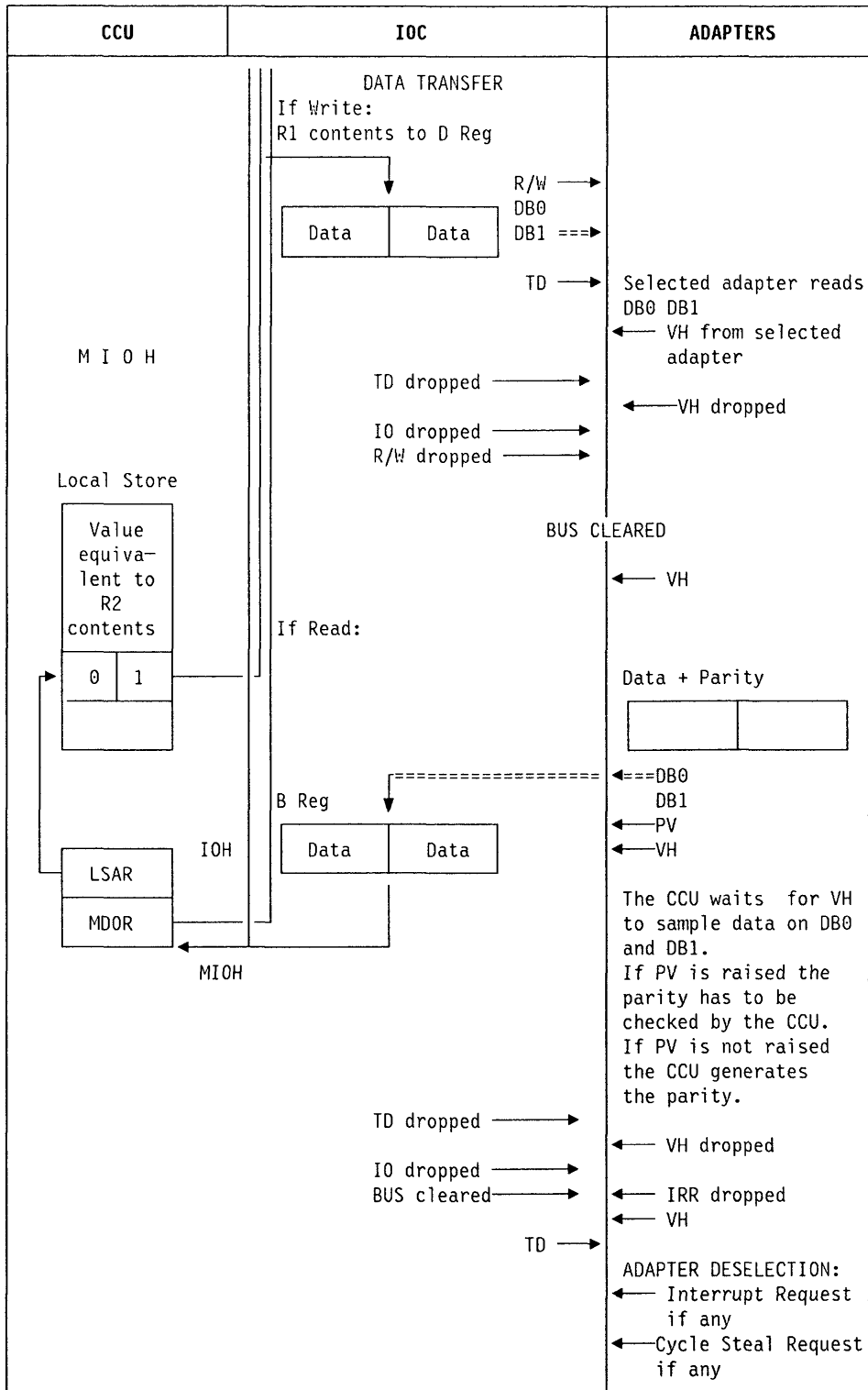
1. The MOSS initiates the operation.
2. R2 contents are found at the LS address given by the LSAR at TA time.
3. The MDOR receives or sends at data TD time instead of R1.

PIO Operation Sequence (Initialization)

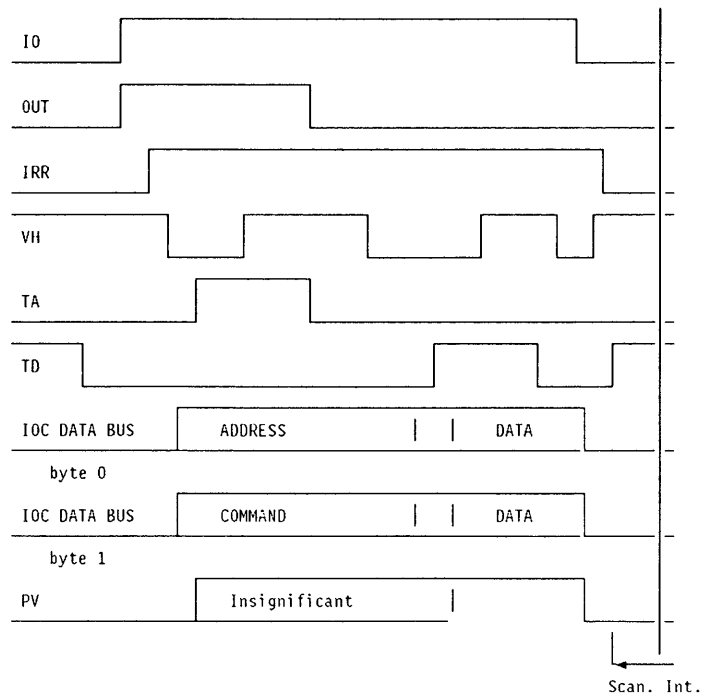


R2 = Address field
R1 = Data field

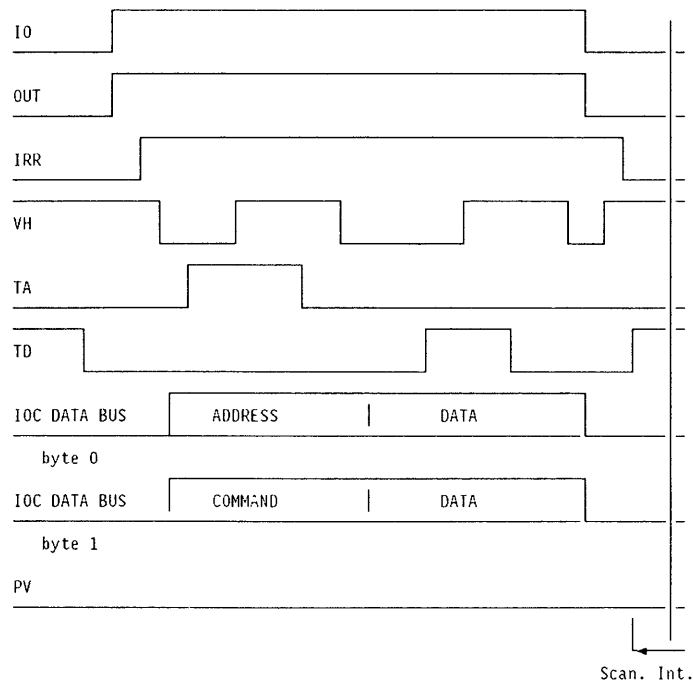
PIO Operation Sequence (Data Transfer)



PIO Read (Halfword Adapter)



PIO Write (Halfword Adapter)



Note: Line explanation is given starting on page 3-6.

AIO Operation

AIO Operation (Cycle Stealing)

During such an operation, several units of data are exchanged between CCU and adapter storage without CP intervention. The maximum burst of data transferred is 256 bytes.

A selected LA provides the storage addresses at which the data bytes are to be stored. For this purpose, a pointer is shared by all LAs cycle steal control word (CSCW).

This information is first placed in the adapter registers by the control program, using the IOH/IOHI instructions in PIO mode.

A selected channel adapter uses its dedicated pointer which was first loaded by the control program.

AIO Operation Sequence (Initialization)

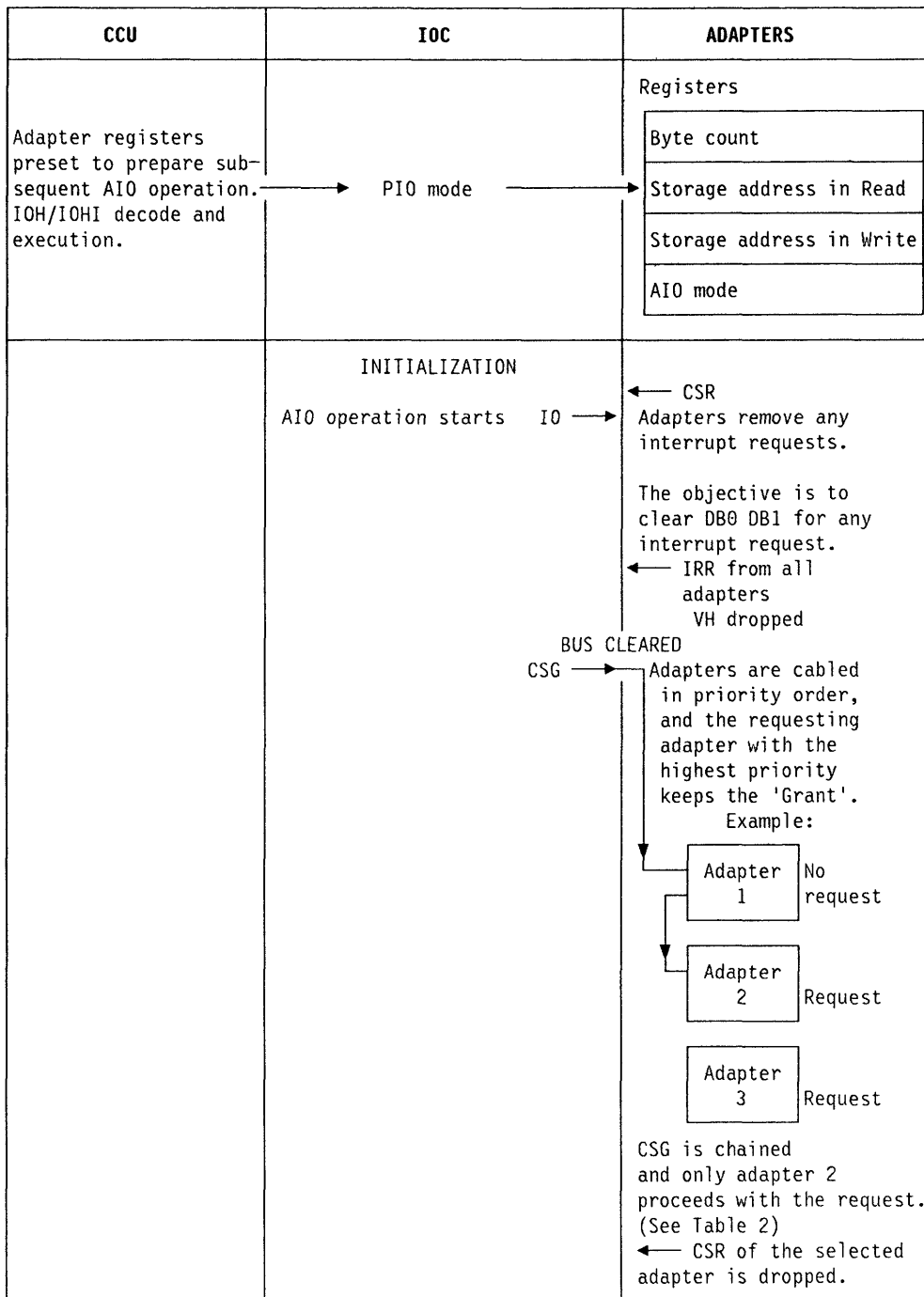


Table 1

AIO Operation Sequence (CSCW Transfer)

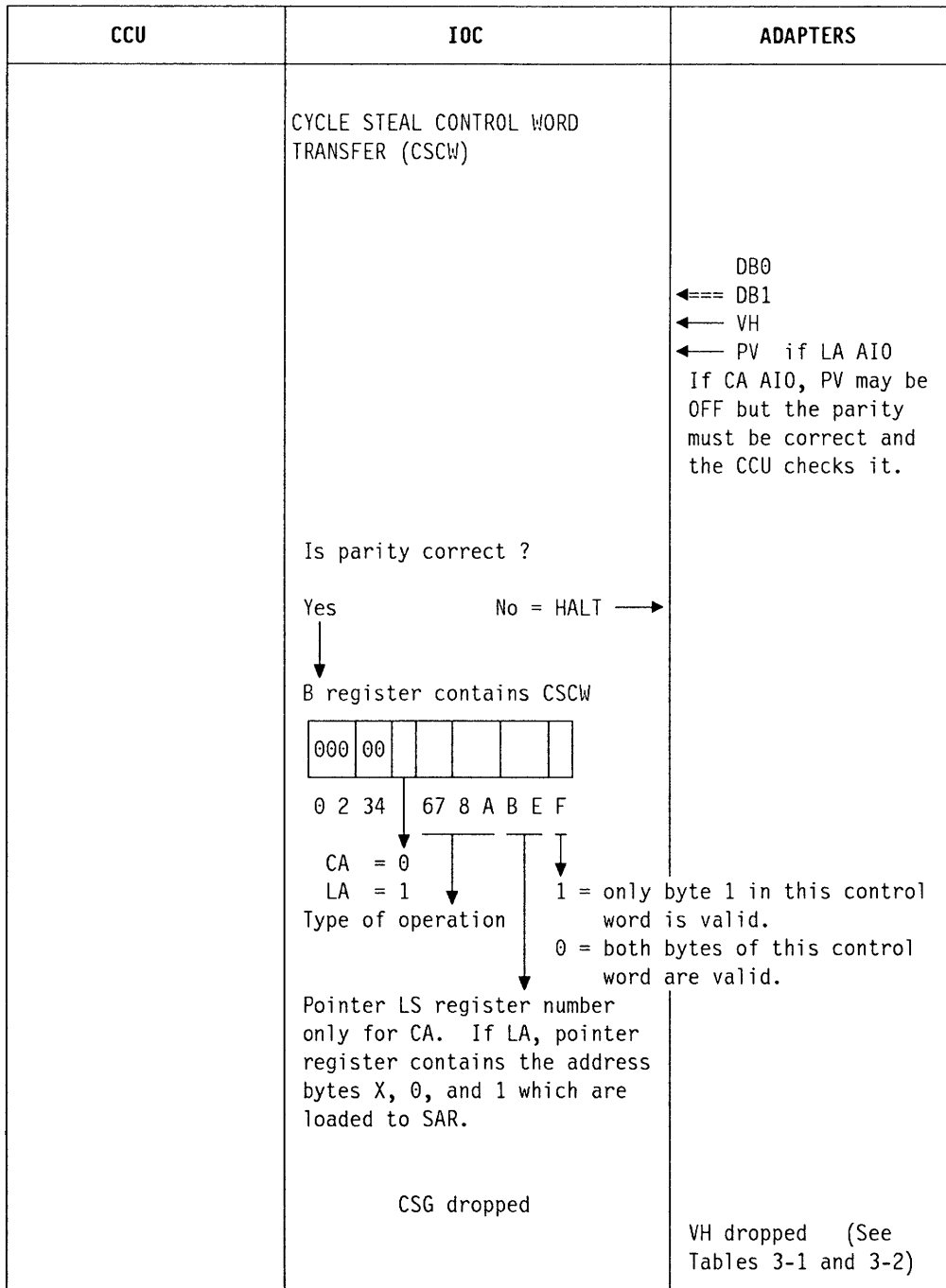


Table 2

AIO Operation Sequence for CA (Storage Address Transfer)

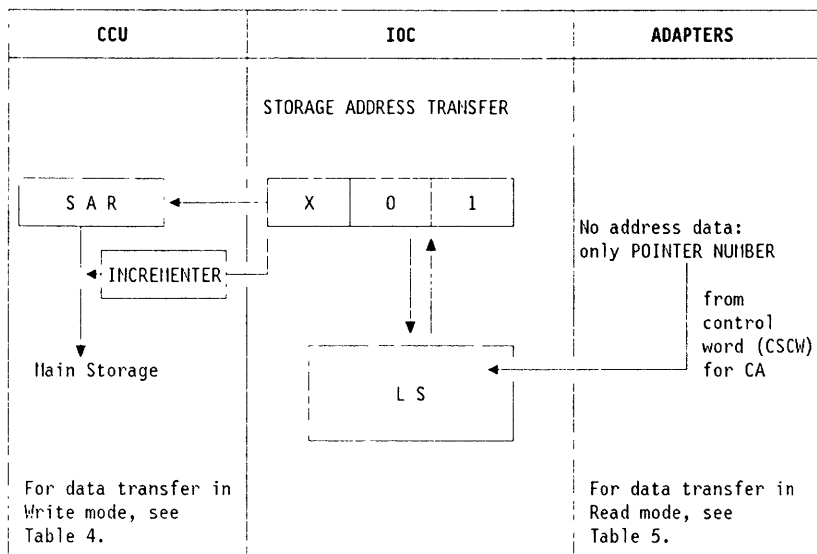


Table 3-1

AIO Operation Sequence for LA (Storage Address Transfer)

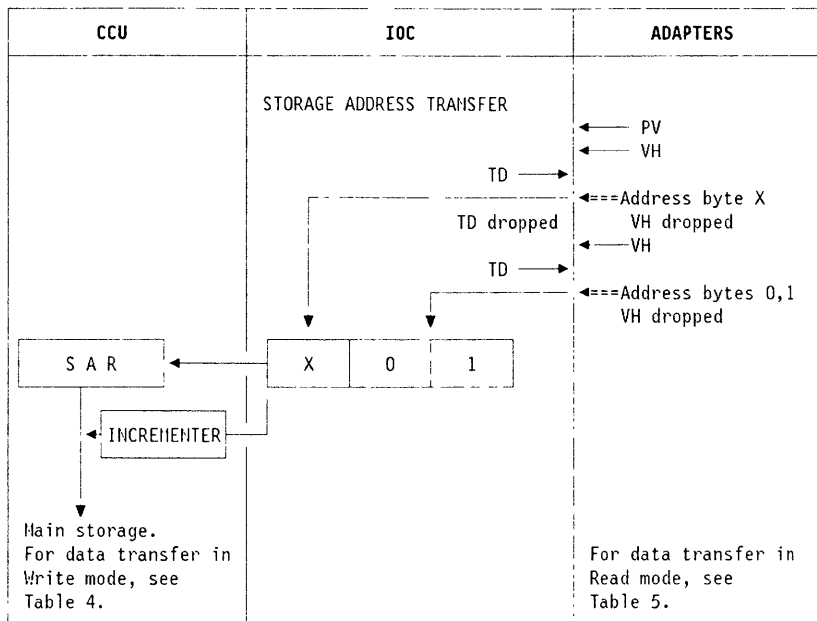


Table 3-2

AIO Operation Sequence (Data Transfer in Write)

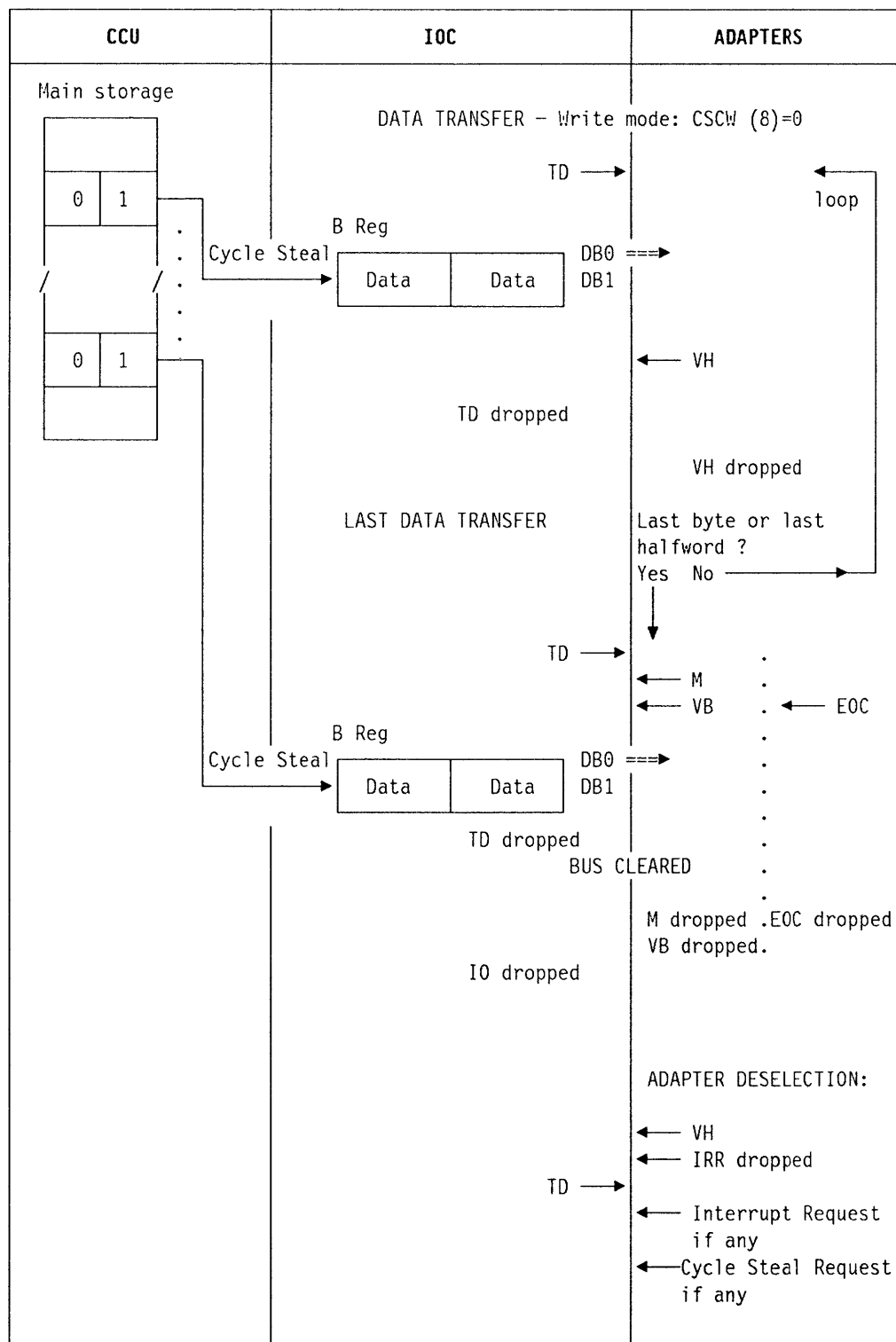


Table 4

AIO Operation Sequence (Data Transfer in Read)

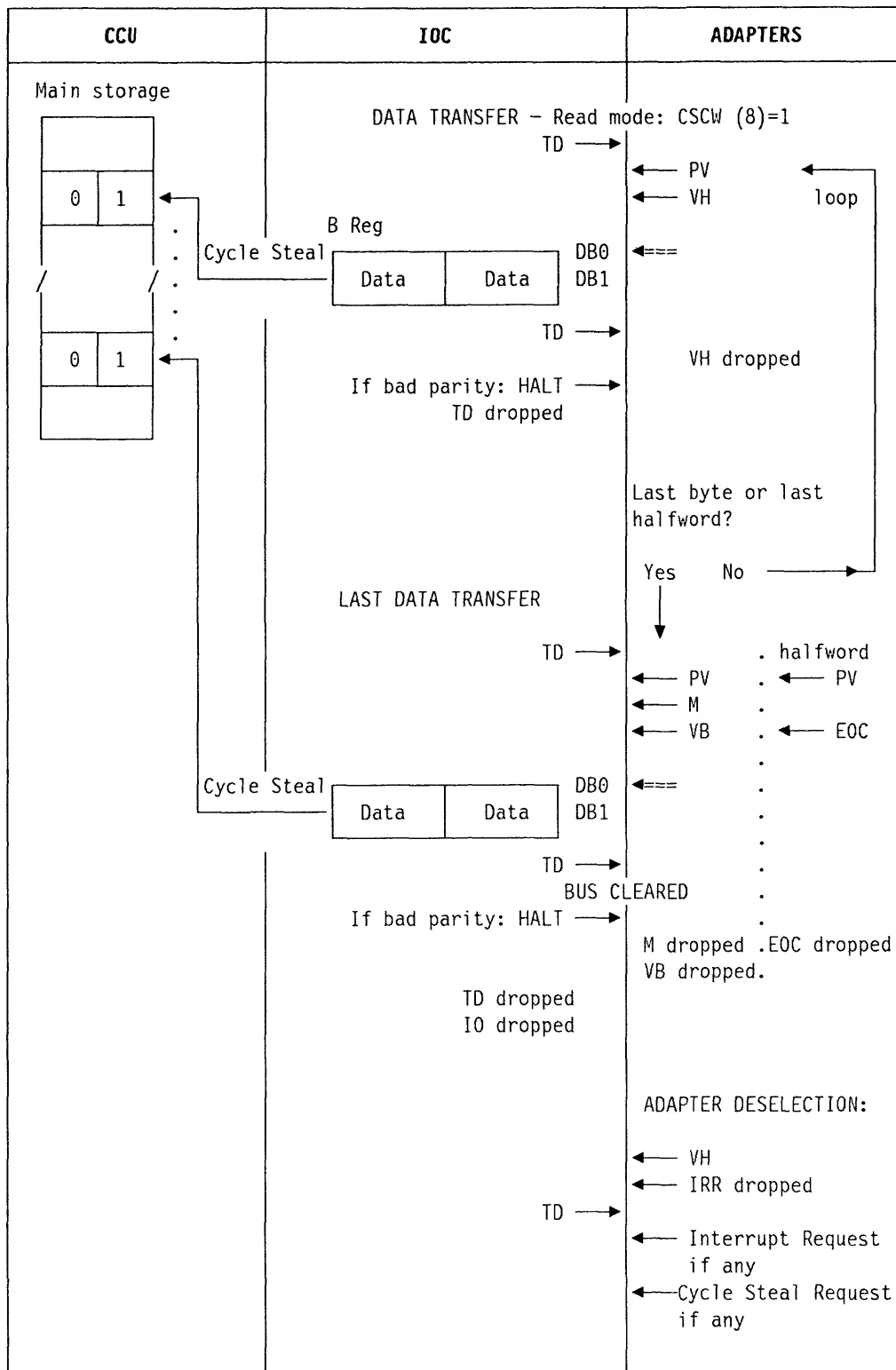
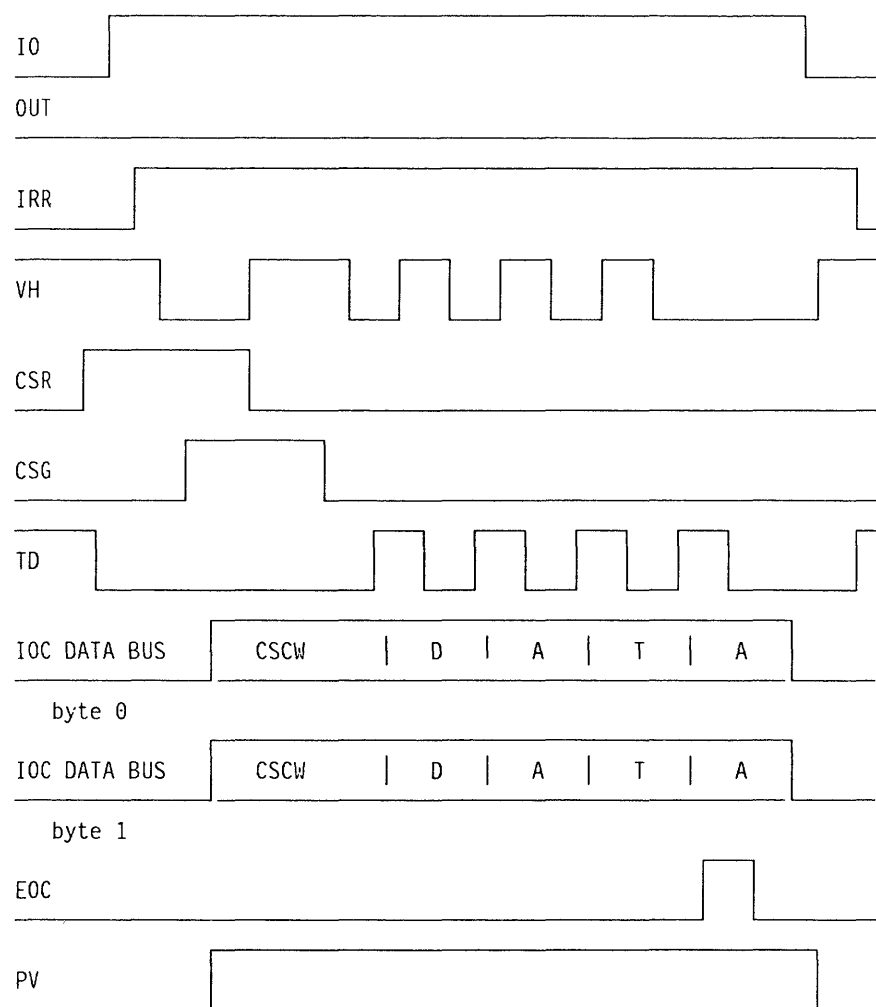


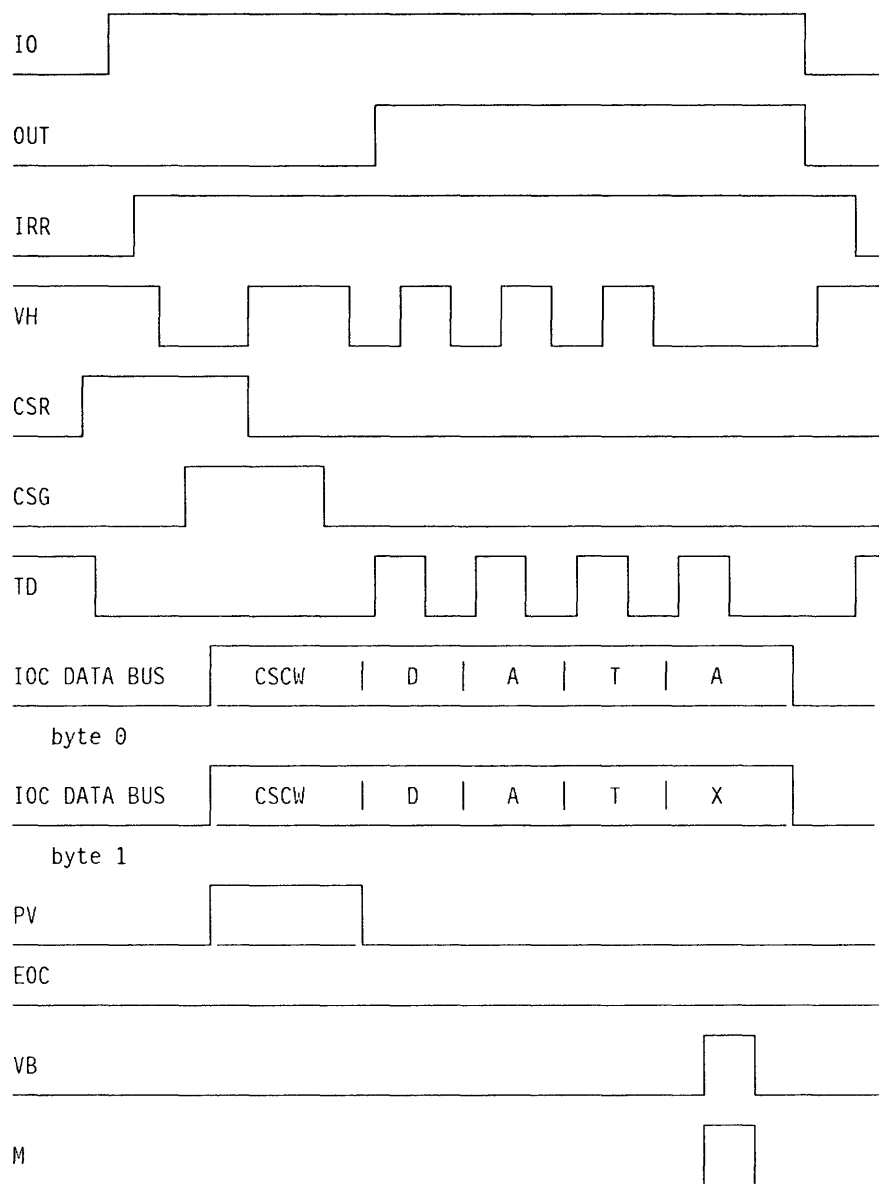
Table 5

AIO CA Read Indirect Operation (8-Byte Transfer)



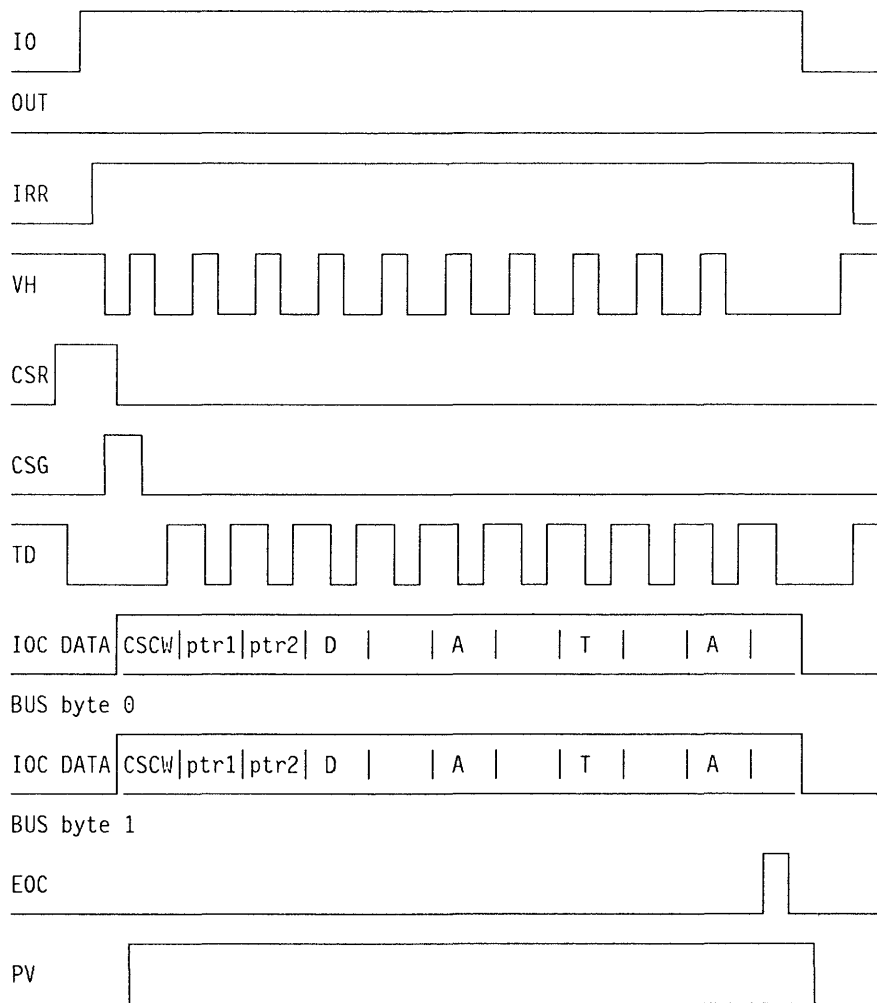
Note: The last data (byte) is in bytes 0 and 1 (same data in bytes 0 and 1 during the inbound operation (VB + M tag).

AIO CA Write Indirect Operation (7-Byte Transfer)



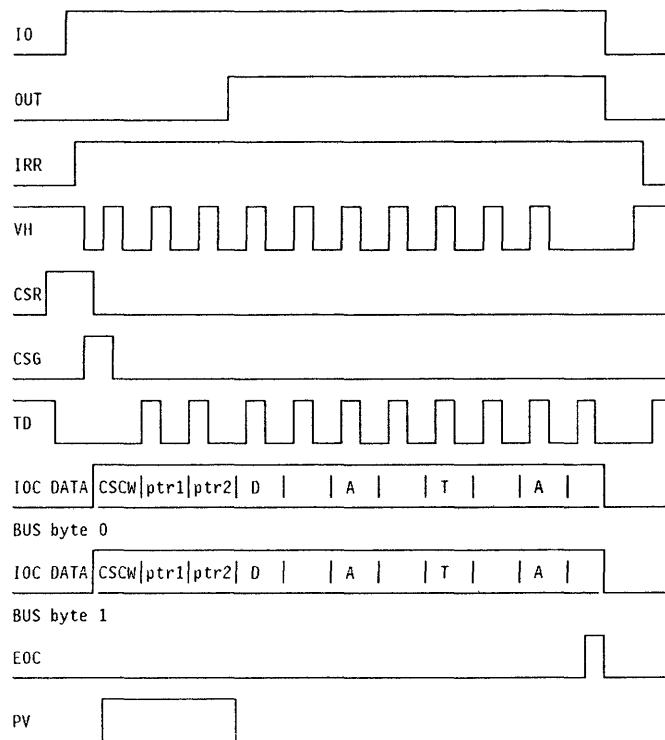
Note: The last data (byte) is in byte 0 during the outbound operation (VB + M tag).

AIO Direct/Indirect LA/TRA Read (16-Byte Transfer)

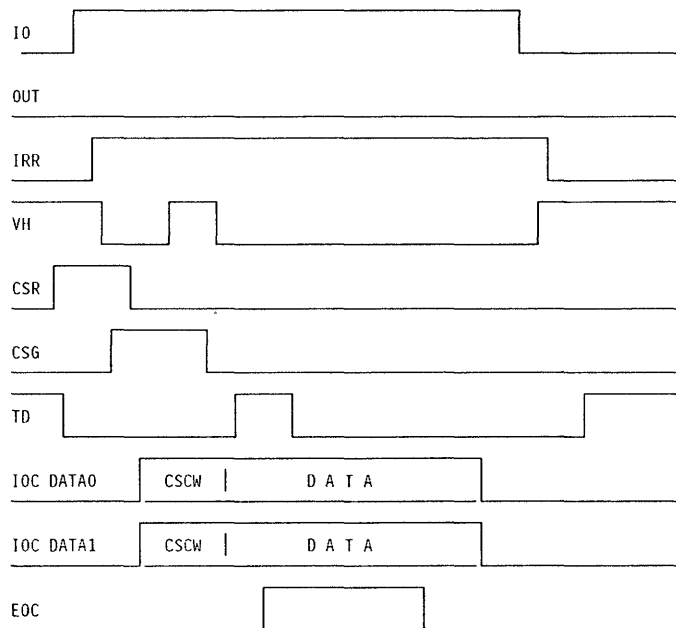


Note: The last data (byte) is in byte 1 during the read operation (VB + M tag).

AIO Direct/Indirect LA/TRA Write (16-Byte Transfer)



AIO TRA Read Direct Operation (2-Byte Transfer)



Bus Propagation Cards (BPC1/BPC2)

Configuration Rules

The bus propagation cards type 1 or type 2 (BPC1/BPC2) are installed on basic board 01G-A1 according to the 3745 model and its configuration.

3745 Model 130

- CAL cards:
 - One BPC1 is required in positions A2 and E2 for TPS.
- CSP/TRM cards:
 - If no TRA is installed:
 - No BPC1 or BPC2 installed
 - If one TRA is installed:
 - One BPC1 is required in position Q2.
 - One BPC1 is required in positions R2 and T2, if no CSP is installed.
 - One BPC2 is required in position P2.
 - If two TRAs are installed:
 - One BPC1 is required in position Q2.
 - One BPC1 is required in positions R2 and T2, if no CSP is installed.

3745 Model 150

One BPC1 is required in position T2, if no CSP is installed.

3745 Model 170

- CAL cards:
 - One BPC1 is required in positions A2 and E2 for TPS.
- CSC/CSP cards:
 - If no TRA is installed:
 - If no CSC is installed in position Q2:
 - No BPC1 or BPC2 installed
 - If a CSC is installed in position Q2:
 - One BPC1 is required in positions R2 and T2, if no CSC or CSP are installed in these positions.
 - If a TRA is installed:
 - One BPC1 is required in the free positions of the CSC and CSP cards.

Adapter Addressing

Logical Adapter Address

A logical address is composed of:

- Type address
- Adapter group
- Slot.

The address is valid at IOH/MIOH command time, in PIO mode. This command is generated by the control program or the MOSS.

- The type address defines the kind of adapter (LA or CA) addressed by the control program, at TA time (and TD time for the CA) of the IOH.
- The adapter group defines the group of two adapters (LA or CA) on the IOC bus contained in the 3745.
- The slot gives the position of the adapter in the adapter group on the IOC bus.

Physical Address Wiring

The logical address sent on the IOC bus at TA time is compared by each adapter with its proper physical address.

- The type address part is provided by the logic of the adapter card.
- The slot and the adapter group part, (the bit of lowest weight), are imbedded in the printed circuit of the board.
- The adapter group part, (the remaining bit(s) of higher weight), is provided by the board.

The physical address of each adapter is provided by the following:

- WU is the IOC bus connection: IOC1 (WU = 0).
- WS is the slot wire: Position 0 or 1 in the group.
- WG1, WG2, WG3 are the group address wires.

CA Addressing

PIO Mode

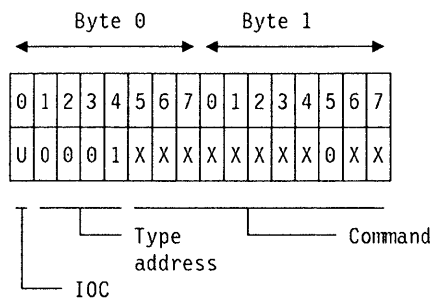
The number of CAs to address is four.

The IOH OUT '07' is the only one which selects a CA. The definition of the IOH/MIOH bit pattern is:

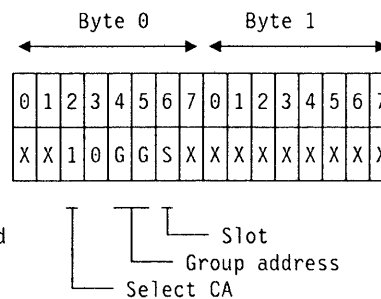
- Byte 0, bit 0 of TA time is the IOC connection:
0 = IOC1
- Byte 0, bits 1-4 is the type address: Code = 0 0 0 1 for all CAs
- Byte 0, bits 5-7 and byte 1, bits 0-7 is the command code = 0 0 0 0 1 1 1 x 0 x x
- Byte 1, bit 4 indicates the origin :
0 = Control program (IOH)
1 = MOSS (MIOH)
- The remaining part of the address is contained in the TD field. Only the MIOH command '07' is able to select a channel adapter with the following convention:
 - Byte 0, bit 2 is equal to 1 to select a CA indicated by byte 0, bits 4 to 6.
 - Byte 0, bits 4 and 5 is the group address:
0 0 = CA Group 1
0 1 = CA Group 2
 - Byte 0, bit 6 is the slot address.
0 = Slot 1
1 = Slot 2

Note: In case of TPS, the B interface uses the slots of the following CA, part of the same CA group. The address of the CA replaced by the B interface is lost.

IOC bus at TA time



IOC bus at TD time



| | GG = 00 | | GG = 01 | |
|---------------|----------|----------|----------|----------|
| | S=0 | S=1 | S=0 | S=1 |
| IOC1 U = 0 | CA 05 | CA 06 | CA 07 | CA 08 |

| IOC bus at TA time | | | | | | | | | | | | | | | IOC bus at TD time | | | | | | | | | | | | | | |
|--------------------|---|---|---|---|---|---|---|--------|---|---|---|---|---|---|--------------------|--------|---|---|---|---|---|---|---|---|---|--|--|--|--|
| Byte 0 | | | | | | | | Byte 1 | | | | | | | | Byte 0 | | | | | | | | | | | | | |
| CA | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | | | | |
| | U | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | G | G | S | 0 | | | | |
| 05 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | | | 1 | | 0 | 0 | 0 | | | | | | |
| 06 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | | | 1 | | 0 | 0 | 1 | | | | | | |
| 07 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | | | 1 | | 0 | 1 | 0 | | | | | | |
| 08 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | | | 1 | | 0 | 1 | 1 | | | | | | |

```

0 8 0 0
┌───┬───┐
│   │   │
│   v   │
xxxx 000x = Byte 0 at TD Time,
    . Bits 4-5 (GG) = 00 and
    . Bit 6 (S) = 0

v
0000 1xxx = Byte 0 at TA Time,
    . Bit 0 (U) = 0 and
    . Bits 1-4 (Type Address) = 0001

```


Line Adapter Addressing (LSS and HSS)

PIO Mode

The number of LSS to address is six (LA3-4 and LA9-12).

Two high-speed lines can be installed in the system at line adapter addresses:
LA 3 and LA 4.

See Figure 3-2 on page 3-4

The HSS are addressed like the LSS.

The LA address is defined at TA time of the IOH.

The line addresses for this LA are given at TD time.

The LA address is given at TA time of the IOH.

- Byte 0, bit 0 is the IOC connection:
0 = IOC1
- Byte 0, bits 1-4 is the type address and slot indicator.
Three type addresses, 0 0 1 0, 0 1 0 0, and 0 1 1 0 are recognized by the line adapters.

Type address 0 1 1 0 has the meaning of command broadcast to all LAs.

Bits 2 and 3 also have a meaning for the slot identification:

Bits 2-3 = 01 indicates slot 1 in a group address of the IOC bus.

Bits 2-3 = 10 indicates slot 2 in a group address of the IOC bus.

Bits 2-3 = 11 broadcast to all LAs.

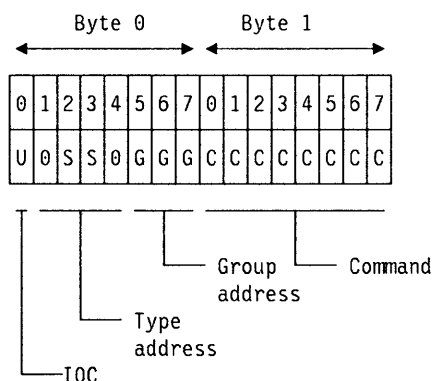
- Byte 0, bits 5-7 is the group address. The group address identifies a pair of scanners. Three group addresses are used:

0 0 1 = Group address 2

0 1 0 = Group address 3

0 1 1 = Group address 4

IOC bus at TA time



| | | | | | | |
|------|-------|----|-------|----|-------|----|
| | G=001 | | G=010 | | G=011 | |
| | SS | SS | SS | SS | SS | SS |
| | = | = | = | = | = | = |
| | 01 | 10 | 01 | 10 | 01 | 10 |
| IOC1 | LA | LA | LA | LA | LA | LA |
| U=0 | 03 | 04 | 09 | 10 | 11 | 12 |

IOC bus at TA time
Byte 0

| LA | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | Hex |
|----|---|---|---|---|---|---|---|---|-----|
| | U | 0 | S | S | 0 | G | G | G | |
| 03 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11 |
| 04 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21 |
| 09 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12 |
| 10 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 22 |
| 11 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13 |
| 12 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23 |

MOSS Screen LA Address Display: As an example, address 12 for LA 9 displayed on the MOSS screen is composed as follows:

1 2

└
v

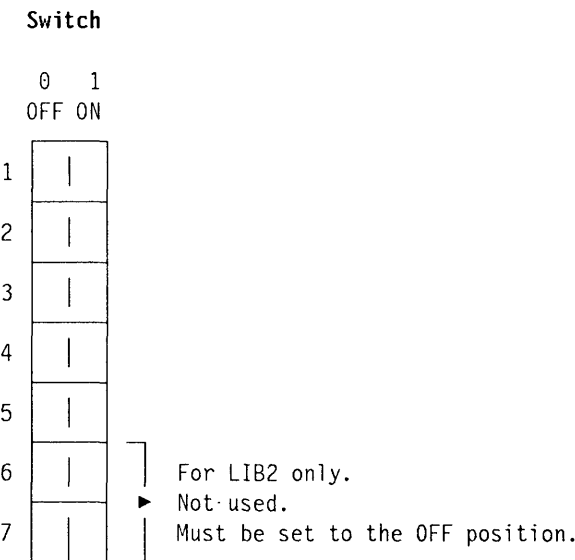
0001 0010 = Byte 0 at TA Time,

- . Bit 0 (U) = 0,
- . Bits 2-3 (SS) = 01, and
- . Bits 5-7 (GGG) = 010

LIC Board Addressing

The LIC board address is set with a seven-position switch located at the A1 position of the LIC board.

For location, see page YZ038 or YZ039.



Switch Position for LIB1/3 Type (LICs 1-4)

| Board Location | Switch | | | | |
|----------------|--------|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 |
| 01M-A1 | 1 | 0 | 0 | 0 | 0 |
| 01M-A2 | 0 | 0 | 0 | 0 | 0 |
| 01L-A2 | 0 | 0 | 0 | 1 | 0 |

Switch Position for LIB2 Type (LICs 5-6)

| Board Location | Switch | | | | | | |
|----------------|--------|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 01L-A1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 01L-A2 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

Figure 3-7. LIC Board Addressing Switch Position

Line Addressing

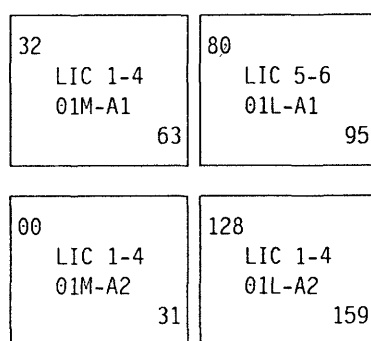
The line address used by the control program is composed of the LA address, previously defined, and of the LIC/PORT address given at TD time of the IOH using byte 1, bits 2 to 7:

Line Numbering

Depending on the configuration, two cases of line numbering are possible:

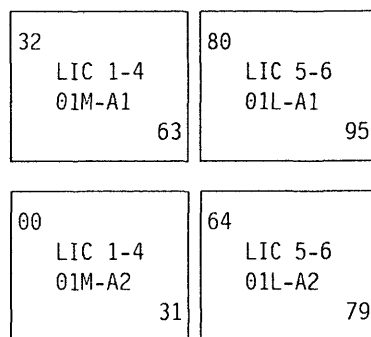
1. The floating LIC board 01L-A2 is LIB1 type (LICs type 1-4).

Possibility of 96 lines, LICs type 1-4 and 16, lines LICs type 5-6 numbered as follows:



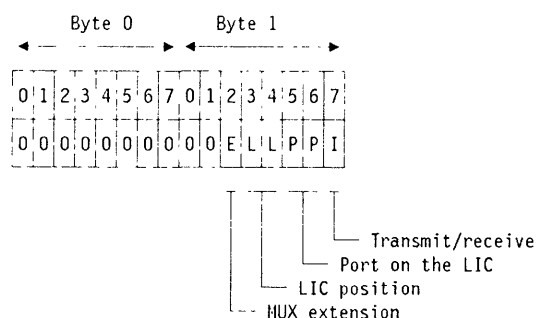
2. The floating LIC board 01L-A2 is LIB2 type (LICs type 5-6)

Possibility of 64 lines, LICs type 1-4 and 32 lines, LICs type 5-6 numbered as follows:



LIC1 LIC3 LIC4A and LIC4B Addressing

IOC bus at TD time



- Byte 1, bit 2 identifies part 1 or 2 in the LIC board (MUX extension).
 - Bit 2 = 0: the scanner controls part 1 in the LIC board
 - Bit 2 = 1: the scanner controls part 2 in the LIC board.
- Byte 1, bits 3-4 indicates the LIC position in part 1 or 2.
 - 00 = First LIC in part 1 or 2
 - 01 = Second LIC in part 1 or 2
 - 10 = Third LIC in part 1 or 2
 - 11 = Fourth LIC in part 1 or 2
- Byte 1, bits 5-6 indicates the port of the LIC.
 - 00 = First port
 - 01 = Second port
 - 10 = Third port
 - 11 = Fourth port

LIC Type 1 and LIC Type 4A have four ports.

LIC type 3 and LIC type 4B have only one port.

- Byte 1, bit 7 indicates the transmit or receive address.
 - When bit 7 = 1: receive address.
 - When bit 7 = 0: transmit address.

| | | LIC Position | | | | | | | | |
|---|--|--------------|----|----|----|----|----|----|----|---------|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | |
| D | | 00 | 04 | 08 | 12 | 16 | 20 | 24 | 28 | PP = 00 |
| H | | 01 | 05 | 09 | 13 | 17 | 21 | 25 | 29 | PP = 01 |
| U | | 02 | 06 | 10 | 14 | 18 | 22 | 26 | 30 | PP = 10 |
| X | | 03 | 07 | 11 | 15 | 19 | 23 | 27 | 31 | PP = 11 |

| | | | | | | | |
|---------------|-------|-------|-------|---------------|-------|-------|-------|
| LL=00 | LL=01 | LL=10 | LL=11 | LL=00 | LL=01 | LL=10 | LL=11 |
| Part 1, E = 0 | | | | Part 2, E = 1 | | | |

TSS Line Addressing for LICs 1-4

During Transmit Operation

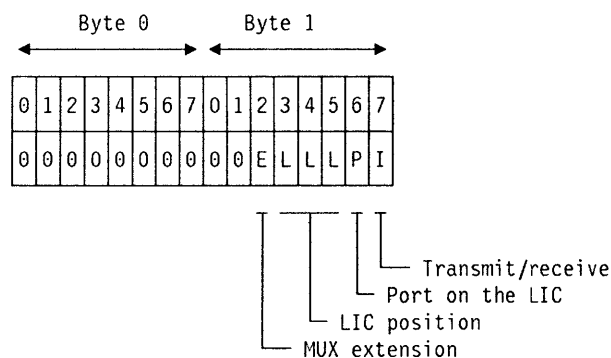
| Line | Byte 1 | | | | | | | Hex |
|------|--------|---|---|---|---|---|---|-----|
| | 0 | 0 | E | L | L | P | I | |
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| 01 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 02 |
| 02 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 04 |
| 03 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 06 |
| 04 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 08 |
| 05 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0A |
| 06 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0C |
| 07 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0E |
| 08 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 10 |
| 09 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 12 |
| 10 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 14 |
| 11 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 16 |
| 12 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 18 |
| 13 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1A |
| 14 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1C |
| 15 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1E |
| 16 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 20 |
| 17 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 22 |
| 18 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 24 |
| 19 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 26 |
| 20 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 28 |
| 21 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 2A |
| 22 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 2C |
| 23 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 2E |
| 24 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 30 |
| 25 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 32 |
| 26 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 34 |
| 27 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 36 |
| 28 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 38 |
| 29 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 3A |
| 30 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 3C |
| 31 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 3E |

During Receive Operation

| Line | Byte 1 | | | | | | | Hex |
|------|--------|---|---|---|---|---|---|-----|
| | 0 | 0 | E | L | L | P | I | |
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 |
| 01 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03 |
| 02 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05 |
| 03 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 07 |
| 04 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 09 |
| 05 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0C |
| 06 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0D |
| 07 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0F |
| 08 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 11 |
| 09 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 13 |
| 10 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 15 |
| 11 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 17 |
| 12 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 19 |
| 13 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1B |
| 14 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1D |
| 15 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1F |
| 16 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 21 |
| 17 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 23 |
| 18 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 25 |
| 19 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 27 |
| 20 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 29 |
| 21 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 2B |
| 22 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 2D |
| 23 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 2F |
| 24 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 31 |
| 25 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 33 |
| 26 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 35 |
| 27 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 37 |
| 28 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 39 |
| 29 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 3B |
| 30 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 3D |
| 31 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 3F |

LIC5 and LIC6 Addressing

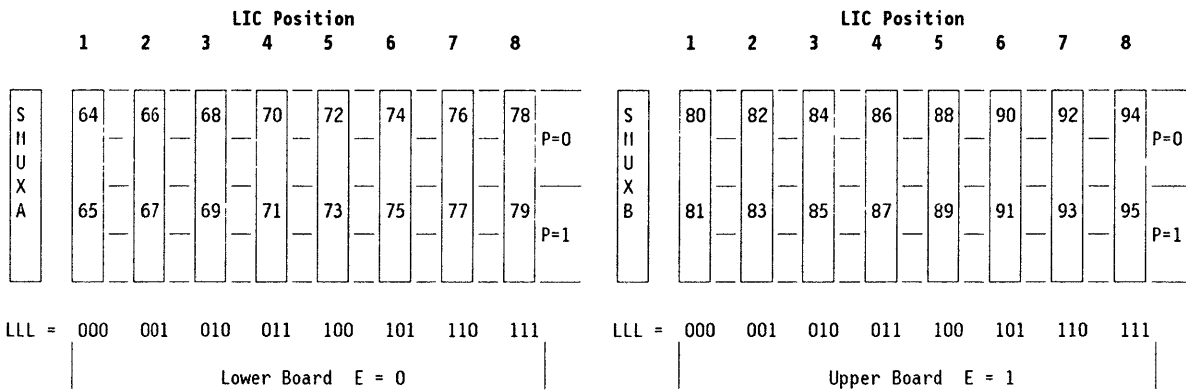
I/O bus at TD time



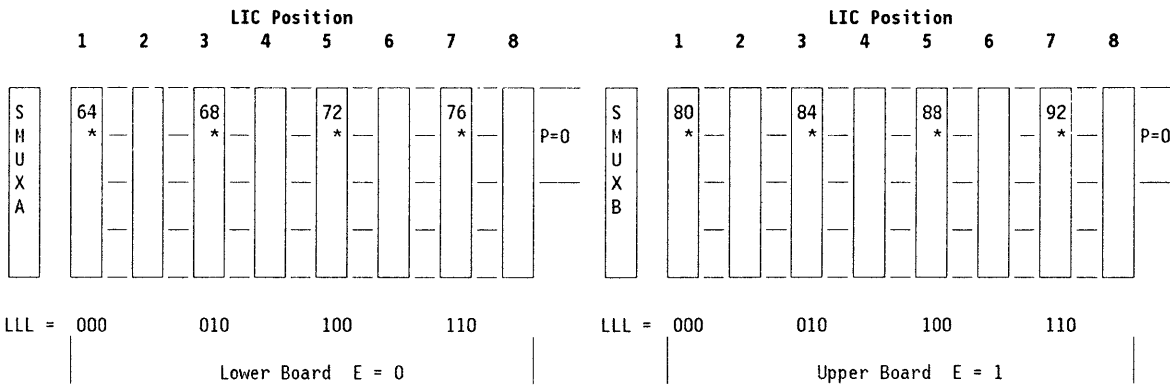
- Byte 1, bit 2 identifies the LIC board in the LIC unit.
 - Bit 2 = 0: the scanner controls the lower board in the LIC unit.
 - Bit 2 = 1: the scanner controls the upper board in the LIC unit.
- Byte 1, bits 3-5 indicates the LIC position in the LIC board.
 - 000 = LIC position 1
 - 001 = LIC position 2
 - 010 = LIC position 3
 - 011 = LIC position 4
 - 100 = LIC position 5
 - 101 = LIC position 6
 - 110 = LIC position 7
 - 111 = LIC position 8
- Byte 1, bit 6 indicates the port of the LIC.
 - 0 = First port
 - 1 = Second port

LIC type 5 has two ports.
LIC type 6 has only one port.
- Byte 1, bit 7 indicates the transmit or receive address.
 - When bit 7 = 1: receive address.
 - When bit 7 = 0: transmit address.

Port Position for LIC Type 5 and LIC Type 6 at 9.6 and 19.2 kbps



Port Position for LIC Type 6 at 56 kbps



* = The LIC cassette can be plugged in an odd position only.

For plugging restrictions refer to "LIC Type 6, Plugging Limitations" on page 4-10.

Note: LIC type 5 and LIC type 6 are installed starting from line address 064.

TSS Line Addressing for LICs 5-6

During Transmit Operation

| Line | Byte 1 | | | | | | | Hex |
|------|--------|---|---|---|---|---|---|-----|
| | 0 | 0 | E | L | L | P | I | |
| 64 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| 65 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02 |
| 66 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04 |
| 67 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 06 |
| 68 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 08 |
| 69 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0A |
| 70 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0C |
| 71 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0E |
| 72 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 |
| 73 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12 |
| 74 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 14 |
| 75 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 16 |
| 76 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 18 |
| 77 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1A |
| 78 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1C |
| 79 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1E |
| 80 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 20 |
| 81 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 22 |
| 82 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 24 |
| 83 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 26 |
| 84 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 28 |
| 85 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 2A |
| 86 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 2C |
| 87 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 2E |
| 88 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 30 |
| 89 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 32 |
| 90 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 34 |
| 91 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 36 |
| 92 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 38 |
| 93 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 3A |
| 94 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 3C |
| 95 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 3E |

During Receive Operation

| Line | Byte 1 | | | | | | | Hex |
|------|--------|---|---|---|---|---|---|-----|
| | 0 | 0 | E | L | L | P | I | |
| 64 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 |
| 65 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03 |
| 66 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05 |
| 67 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 07 |
| 68 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 09 |
| 69 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0C |
| 70 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0D |
| 71 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0F |
| 72 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11 |
| 73 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13 |
| 74 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 15 |
| 75 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 17 |
| 76 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 19 |
| 77 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1B |
| 78 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1D |
| 79 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1F |
| 80 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 21 |
| 81 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 23 |
| 82 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 25 |
| 83 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 27 |
| 84 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 29 |
| 85 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 2B |
| 86 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 2D |
| 87 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 2F |
| 88 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 31 |
| 89 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 33 |
| 90 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 35 |
| 91 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 37 |
| 92 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 39 |
| 93 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 3B |
| 94 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 3D |
| 95 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 3F |

HPTSS Line Addressing

Up to two lines can be addressed for each HPTSS, but only one is active at a time.

Byte 1 bit 6 selects the port:

- 0 = port 1
- 1 = port 2

Line numbers 1028 through 1031 are dedicated for HPTSS use.

| Adapter Number | Line Address | Tailgate Position |
|----------------|--------------|-------------------|
| 3 Port 1 | 1028 | 01Q-C0 J2 |
| Port 2 | 1029 | 01Q-C0 J1 |
| 4 Port 1 | 1030 | 01Q-D0 J2 |
| Port 2 | 1031 | 01Q-D0 J1 |

Token-Ring Adapter (TRA) Addressing

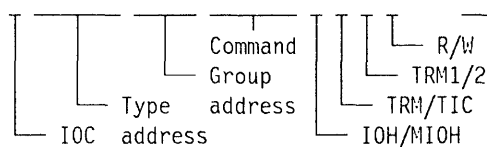
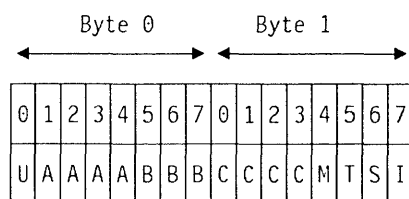
Up to two TRMs can be installed on the 3745.

They are addressed at TA time of the IOH.

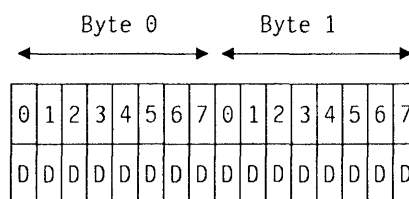
The TRM address is included in the TA halfword of the IOH.

- Byte 0, bit 0 is the IOC connection.
- Byte 0, bits 1-4 is the type address and is equal to 1 0 0 1.
- Byte 0, bits 5-7 is the group address. This group address is unique and set to 0 0 0.
- Byte 1, bit 4 indicates the origin: 0 = Control program
1 = MOSS
- Byte 1, bit 5 indicates whether a TRM or a TIC is addressed:
 - Bit 5 = 0 indicates a command to a TIC.
 - Bit 5 = 1 indicates a command to a TRM.
- Byte 1, bit 6 is the slot address: 0 = Slot 1
1 = Slot 2

IOC bus at TA time

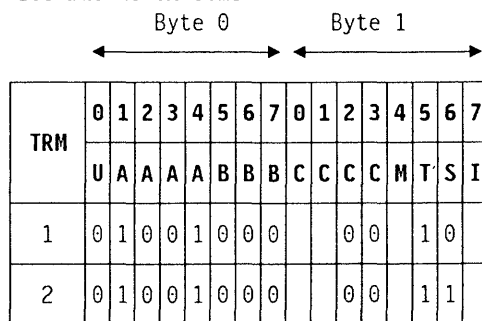


IOC bus at TD time



Data bits

IOC bus at TA time



Token-Ring Line Addressing

Two token-ring adapters (TRA) can be installed.
See Figure 3-2 on page 3-4.

The TRA is addressed at TA time of the IOH

One TRM controls 2 TICs. Byte 1, bits 2 and 3 from the command are used to identify one of the TICs.

- If bits 2 and 3 = 0 0, TIC 1 is addressed.
- If bits 2 and 3 = 0 1, TIC 2 is addressed.

The TIC is addressed when byte 1, bit 5 = 0.

Token-Ring Address

| | | IOC bus at TA time | | | | | | | | | | | | | | | |
|-----|-----|--------------------|---|---|---|---|---|---|---|--------|---|---|---|---|---|---|---|
| | | Byte 0 | | | | | | | | Byte 1 | | | | | | | |
| TRM | TIC | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | U | A | A | A | A | B | B | B | C | C | C | C | M | T | S | I |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | | | 0 | 0 | | 0 | 0 | |
| | 2 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | | | 0 | 1 | | 0 | 0 | |
| 2 | 3 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | | | 0 | 0 | | 0 | 1 | |
| | 4 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | | | 0 | 1 | | 0 | 1 | |

Line numbers 1088 and 1091 are dedicated for TRSS use.

| TIC Number | Line Address |
|------------|--------------|
| 1 | 1088 |
| 2 | 1089 |
| 3 | 1090 |
| 4 | 1091 |

Adapter Bypass Mechanism

For Line Adapters

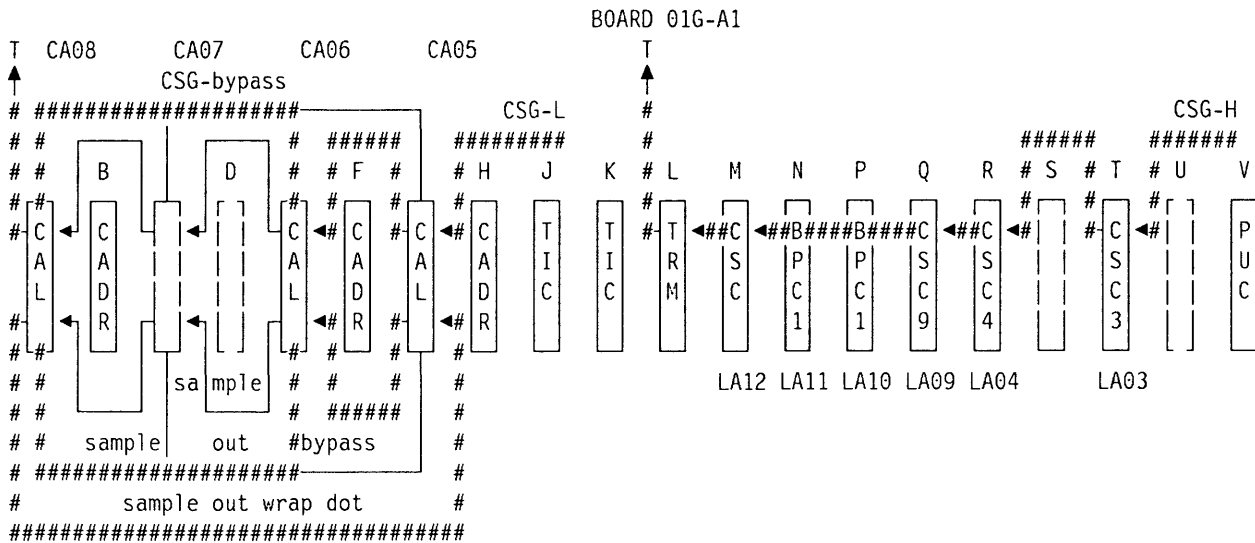
There is no bypass mechanism. Any missing LA must be replaced by a BPC card except if it is the last in the chain.

For Channel Adapters

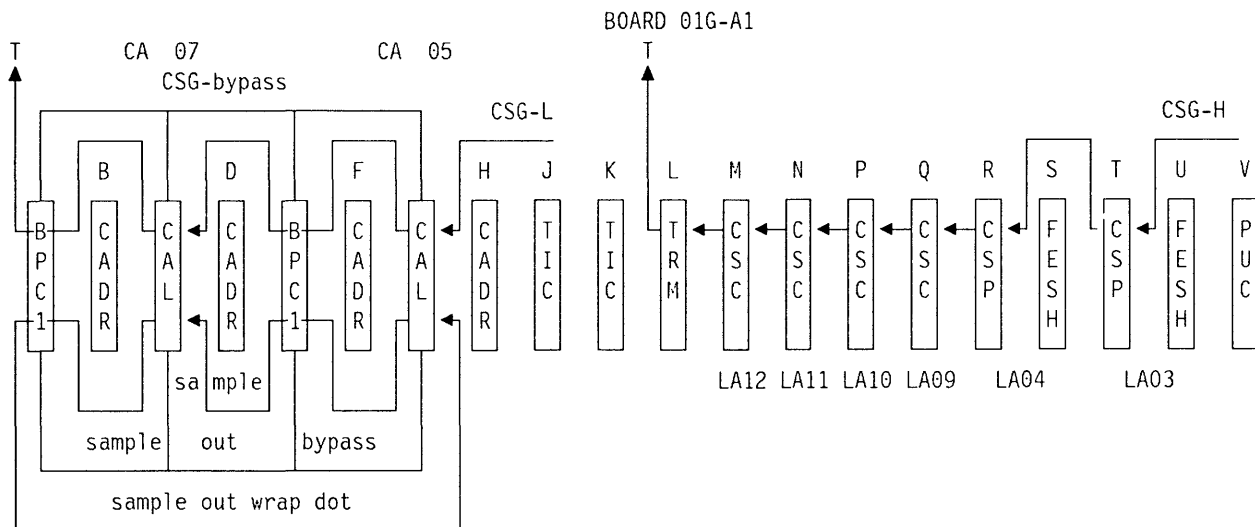
- The bypass mechanism is under MOSS and NCP control through the CDF (at IPL time or by a 'shut-down' command).
- The MOSS tells the CAs what the adapter configuration is on the bus (each CA must know if the preceding and the next adapter are present or not).
- Two chains are involved in this mechanism:
 - Cycle Steal Grant (CSG).
 - Autoselection chain.

Cycle Steal Grant (CSG) and Autoselection Mechanism for Model 170

Without TPS and Without HPTSS



With TPS and HPTSS



CSG and sample paths defined by the bypass mechanism for this example of configuration

Cycle Steal Grant (CSG-L) Scenario for CAs

As an answer to 'CSR' from any CA, the CCU raises 'CSG-L' line to the CAs.

This line is propagated as follows:

- INPUT:
 - The first CA in the chain is looking at 'CSG-L' from the CCU.
 - Other CAs are looking at:
 - 'CSG-through' line if the previous CA is in the chain.
 - 'CSG-bypass' line if the previous CA is not in the chain.
- OUTPUT:
 - The CA which has raised 'CSR' keeps the 'CSG' and breaks the chain.
 - Other CAs raise:
 - 'CSG-through' if the next CA is in the chain.
 - 'CSG-bypass' if the next CA is not in the chain.

One CA only can be looking at 'CSG-bypass' and one CA only can raise 'CSG-bypass', the consequence is that only one CA or group of consecutive CAs can be missing on the bus.

If a CA is TPS (CA01 in the drawing), the next CA must be replaced by a BPC card to propagate the 'CSG-through' line.

Autoselection Scenario for CAs

As an answer to 'level 3' interrupts from any CA, the CCU issues an IOH X'0F' to the bus.

There is always one CA initially selected in the chain.

This IOH start the propagation of the 'sample' line from the initially selected CA as follows:

- INPUT:
 - The first CA on the bus is looking at 'sample out wrap dot' from the last CA.
 - Other CAs are looking at:
 - 'Sample' line if the previous CA is in the chain.
 - 'Sample-bypass' line if the previous CA is not in the chain
- OUTPUT:
 - The CA which is to be selected keeps the 'sample' and breaks the chain.
 - The last CA on the bus raises 'sample out wrap dot'.
 - Other CAs raise:

- 'Sample' if the next CA is in the chain.
- 'Sample out-bypass' if the next CA is not in the chain.

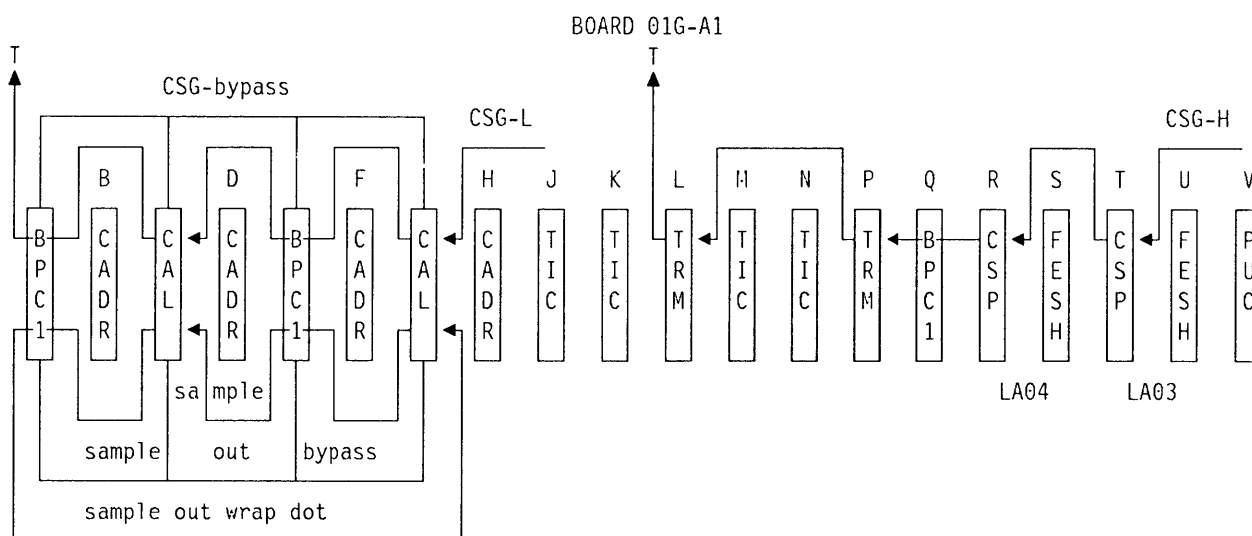
One CA only can be looking at 'sample-bypass' line and one CA only can raise 'sample-bypass', the consequence is that only one CA or group of consecutive CAs can be missing on the bus.

If a CA is TPS, the next CA must be replaced by a BPC card to propagate the 'sample' line.

BPC Card Installation Rules (Model 170)

- Channels adapters:
 - One BPC1 card is required in positions A2 and E2 for TPS.
- Line adapters:
 - If no TRA is installed:
 - If no CSC is installed in position Q2:
No BPC1 or BPC2 are required.
 - If a CSC is installed in position Q2:
One BPC1 is required in positions R2 and T2 if no CSC or CSP are installed in these positions.
 - If a TRA is installed:
One BPC1 is required in the free positions of the CSC and CSP cards.

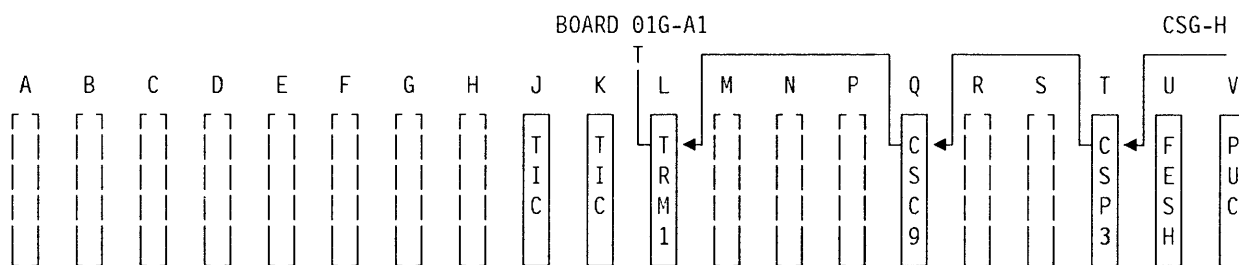
Cycle Steal Grant (CSG) and Autoselection Mechanism for Model 130 With TPS



BPC1 card installation rules

- Channels adapters:
One BPC1 card is required in positions A2 and E2 for TPS.
- Line Adapters:
 - If no TRA is installed: No BPC1 or BPC2 are required.
 - If a TRA is installed:
One BPC1 is required in position Q2. One BPC1 is required in positions R2 and T2 if no CSP is installed. One BPC2 is required in position P2.
 - If two TRAs are installed:
One BPC1 is required in position Q2. One BPC1 is required in position R2 and T2 if no CSP is installed.

Cycle Steal Grant (CSG) for Model 150



BPC1 card installation rules

- One BPC1 is required in position T2 if no CSP is installed.

IOC Bus Scoping Routine

The purpose of the PIO scoping routine is to allow scoping of the PIO tags and data bus.

The following adapters can be exercised using MIOH commands sent from the MOSS:

- CAs
- LAs

How to Start the Routine

1. Start the routine by calling routine WA01.

DIAG == > WA01

2. Put in the ADP field the IOC bus number (1) on which scoping is planned.

IOC adapter bus = 1

ADP ≠ == > 1

3. Put the adapter number in the LINE field

LINE == > 3 (for adapter 03)

- 4 The screen should look like this:

DIAG == > WA01 ADP == > 1 LINE == > 3 OPT == > N

5. Then press SEND.

A check is made to see if the selected IOC bus can be used, (checking of bits: enable, present, available, concurrent).

If the conditions are not satisfied for the selection, a message:

'ADAPTER NOT IN CDF', or
'ADAPTER NOT INSTALLED', or
'INVALID REQUEST' is displayed.

If the inputs are correct, a message is then returned to the operator:

'xx¹ 03² SELECTED - ENTER : Rooccdddd'

¹ = xx may be TSS, HPTSS, TRSS, or CA

² = 03 is the adapter number (3-4 and 9-12)

The first part of the message allows the operator to check that the right adapter is selected. The second part of the message prompts the operator to send the three parameters which define the MIOH operation.

Adapter Selection

ENTER: 'Roocccddd' THEN PRESS SEND.

R : is mandatory

oo : defines the OPTION (hexadecimal)

cc : defines the COMMAND (hexadecimal)

ddd : defines the DATA to/from adapter (hexadecimal)

These parameters are checked:

If the inputs are valid the MIOH operation is started according to the specified parameters.

If the inputs are not valid, a message is then returned to the operator :

'INVALID INPUTS - ENTER : Roocccddd'

Parameter Description

Option 'oo': Four options are possible:

1. 'oo' = '01' The requested MIOH is executed **only once**. The '01' option may be repeated as long as needed. A message is sent to the operator after each MIOH :

'ENTER : R for another cycle or REE to leave'

Therefore if the answer is 'R', the operator is prompted for another MIOH with the selected adapter:

'ENTER: 'Roocccddd' THEN PRESS SEND'

This allows to perform a write followed by a read operation, because inputs may be different.

2. 'oo' = '02' The requested MIOH is executed and **loops** on this MIOH until an error is found. The error is reported only once via a RAC . To continue 'G' (for go) has to be typed, the routine then loops indefinitely until the Power On Reset key is pressed or another error is found.
3. 'oo' = '03' This option is identical to option '02', except that **no checking** is made. This allows looping about four times faster, and therefore easier scoping. The routine loops indefinitely until the Power On Reset key is pressed.
4. 'oo' = '04' This option is **reserved for the TSS**, and is used to scope Adapter Level 1 and Level 2 interrupt requests to the CCU.
Commands 10 to 21 can be used only with option 04.
Because this option needs a Power On Reset on the CSP, each operation lasts about 10 seconds.

For option 04 at TD time on the IOC bus, byte 1 bit 5 will be ON for level 1 interrupts and byte 0 bit 1 ON for level 2.

COMMAND (or MIOH operation) 'cc' Since the purpose of the scoping routine is only to activate the bus lines and the tag lines on the IOC bus, it is only necessary to be able to execute one type of write operation and the corresponding read operation to check the data previously written.

For this reason the command codes are limited to:

1. 'cc' = '01' Defines a write operation to any adapter type. TA values are automatically generated, according to the adapter type and the write operation defined for this adapter.

2. 'cc' = '02' Defines a read operation from any adapter type. TA values are automatically generated, according to the adapter type and the read operation defined for this adapter.

In loop mode, (OPTION 'oo' = '02' or '03'), when a read operation is requested, the first operation is a write in order to store the data in one register of the addressed adapter. All subsequent operations are read operations in order to recall the data from the register previously written.

3. 'cc' = '10' Special for the TSS, requests to the selected adapter used with option 04 only, to reset the level 1 interrupt to the CCU. This level 1 is then tested at CCU level and a message: 'LEVEL 1 INTRPT IS RESET' is displayed.

4. 'cc' = '11' Special for the TSS, used with option 04 only, requests to the selected adapter to set the level 1 interrupt to the CCU. This level 1 is then tested at CCU level and a message: 'LEVEL 1 INTRPT IS SET' is displayed.

5. 'cc' = '20' Special for the TSS, used with option 04 only, requests to the selected adapter to reset the level 2 interrupt to the CCU. This level 2 is then tested at CCU level and a message: 'LEVEL 2 INTRPT IS RESET' is displayed.

6. 'cc' = '21' Special for the TSS, used with option 04 only, requests to the selected adapter to set the level 2 interrupt to the CCU. This level 2 is then tested at CCU level and a message: 'LEVEL 2 INTRPT IS SET' is displayed.

DATA: 'dddd' (mandatory for any command) defines either:

- The data (TD value) sent to the adapter through the IOC bus at TD time during a write operation or,
- The data (TD value) received from the adapter through the IOC bus at TD time during a read operation.

For example, data can be hexadecimal:
'5555', 'AAAA',

RACs Generated

When the scoping routine does not run, the following RACs are generated. These RACs must not be entered with the BRC function. Run the corresponding adapter diagnostic.

RAC Meaning

- 231 Unexpected interrupt CA operation
- 232 Unexpected interrupt TSS operation
- 233 Unexpected interrupt HPTSS operation
- 234 Unexpected interrupt TRSS operation
- 235 Level 2 not set by TSS or HPTSS
- 236 Level 2 not reset by TSS or HPTSS
- 237 Level 1 not set by TSS

- 238 Level 1 not reset by TSS
- 241 Unexpected data from CA
- 242 Unexpected data from TSS
- 243 Unexpected data from HPTSS
- 244 Unexpected data from TRSS

ERC Meaning

The error reference codes displayed with the RAC have the following meanings:

- 0001 Error during selection
- 0002 Error during write (01 operation)
- 0003 Error during read (02 operation)
- 0004 Error during first write (02 requested)

Error Bit (ERR)

The error bit patterns displayed with the RAC have the following meanings:

For RACs 231 to 238:

Byte 0

- Bit 0 = CA to CCU level 1
- Bit 1 = CA to CCU level 3
- Bit 2 = CA to MOSS level 1
- Bit 3 = CA to MOSS level 4
- Bit 4 = TSS to CCU level 1
- Bit 5 = TSS to CCU level 2
- Bit 6 = Not used
- Bit 7 = TSS to MOSS level 4

Byte 1

- Bit 0 = MOSS level 1 IOC time out
- Bit 1 = MOSS level 1 IOC invalid CCW
- Bit 2 = MOSS level 1 IOC other error
- Bit 3 = CCU level 1 SAR parity error
- Bit 4 = CCU level 1 IOC time out
- Bit 5 = CCU level 1 IOC invalid CCW
- Bit 6 = CCU level 1 IOC other error
- Bit 7 = CA to MOSS level 1 CAIPL

For RACs 241 to 244:

ERR bits = Data received from the adapter

Examples of Scoping Routine on Bus Terminator

A good quality oscilloscope is required (high luminosity).

For pin locations, see "Bus Terminator (TERMI) Connector Pin Assignments" on page 3-55.

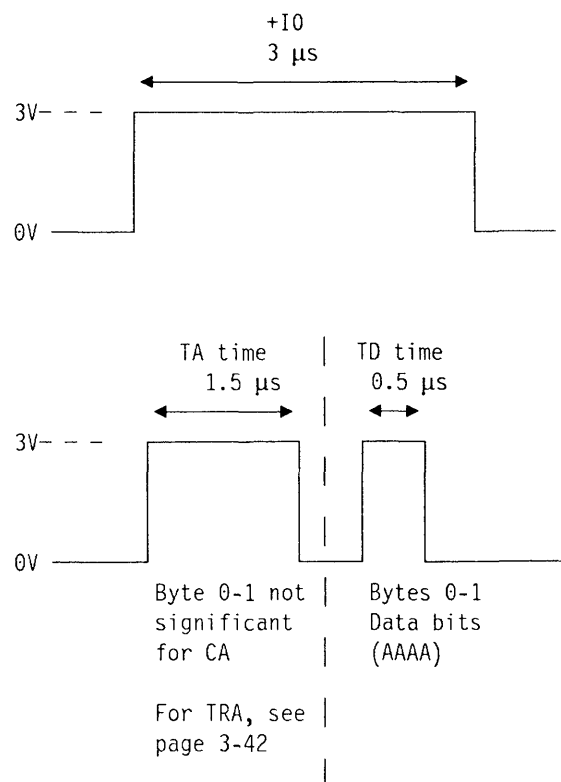
Channel Adapter or Token-Ring Adapter

CA 05 or TRA 1
Options: 02 or 03
Command: 02 (read)
Data: 'AAAA'

Oscilloscope:
Sync: +IO line
Calibration: $0.5 \mu\text{s}$

+IO cycle option 2 = 40 ms

+IO cycle option 3 = 13 ms

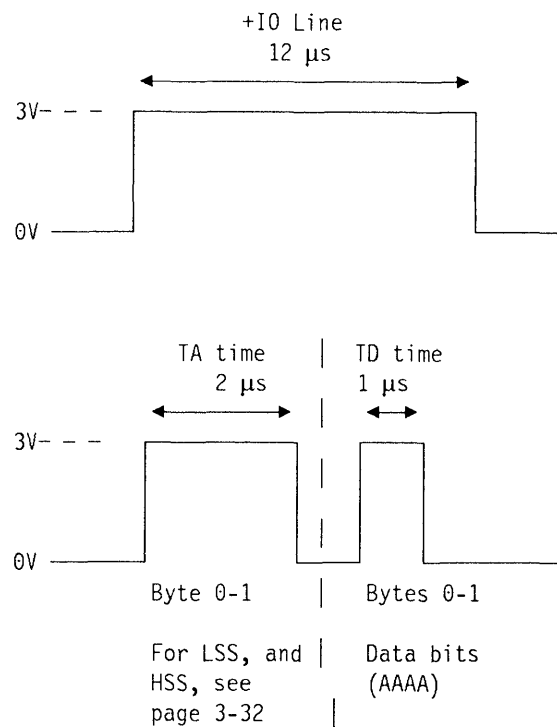


TSS or HPTSS

LSS 03 or HSS 04
Options: 02 or 03
Command: 02 (read)
Data: 'AAAA'

Oscilloscope:
Sync: +IO line
Calibration: $2\mu\text{s}$

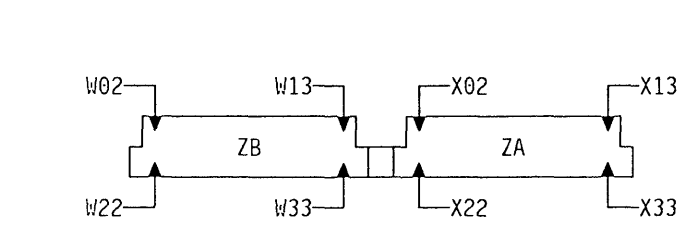
+IO cycle option 2 = 40 ms
+IO cycle option 3 = 13 ms



At TA time, for LSS 03 (TSS):
Byte 0 bits P, 3, and 7 are ON
Byte 1 bits 1 and 3 are ON

At TA time, for HSS 04 (HPTSS):
Byte 0 bits P, 2, and 7 are ON
Byte 1 bits 1 and 3 are ON

Bus Terminator (TERMI) Connector Pin Assignments



Basic Board Rear Side, TERMI Location

| ZB | | | |
|---------------------|-----|-----|----------------------|
| + TA Tag. | W22 | W02 | + Data Byte 1 Bit P |
| + TD Tag. | W23 | W03 | + Data Byte 1 Bit 0 |
| + IO Tag. | W24 | W04 | + Data Byte 1 Bit 1 |
| + OUT Tag. | W25 | W05 | + Data Byte 1 Bit 2 |
| + Halt Tag. | W26 | W06 | + Data Byte 1 Bit 3 |
| + CS Req. Priority. | W27 | W07 | + Data Byte 1 Bit 4 |
| + Level 2 Priority. | W28 | W08 | Ground |
| + Valid Byte. . . . | W29 | W09 | + Data Byte 1 Bit 5 |
| + Modifier. | W30 | W10 | + Data Byte 1 Bit 6 |
| + End of Chain. . . | W31 | W11 | + Data Byte 1 Bit 7 |
| + Parity Valid. . . | W32 | W12 | + Reset Tag |
| + Valid Halfword. . | W33 | W13 | + CA Nohold |
| ZA | | | |
| + IRR | X22 | X02 | + CA MOSS POR |
| + CS Req. Low (CA). | X23 | X03 | + CA Level 1 to MOSS |
| + CS Req. High (CS) | X24 | X04 | + CA Level 4 to MOSS |
| + Data Byte 0 Bit P | X25 | X05 | + CA CSG Bypass |
| + Data Byte 0 Bit 0 | X26 | X06 | + CA CSG Bypass |
| + Data Byte 0 Bit 1 | X27 | X07 | + CA Valid Feed Auto |
| + Data Byte 0 Bit 2 | X28 | X08 | Ground |
| + Data Byte 0 Bit 3 | X29 | X09 | + CA Valid Feed Auto |
| + Data Byte 0 Bit 4 | X30 | X10 | + CA Sample Bypass |
| + Data Byte 0 Bit 5 | X31 | X11 | + CA Sample Bypass |
| + Data Byte 0 Bit 6 | X32 | X12 | + CA Sample Wrap DOT |
| + Data Byte 0 Bit 7 | X33 | X13 | + CS Grant Low |



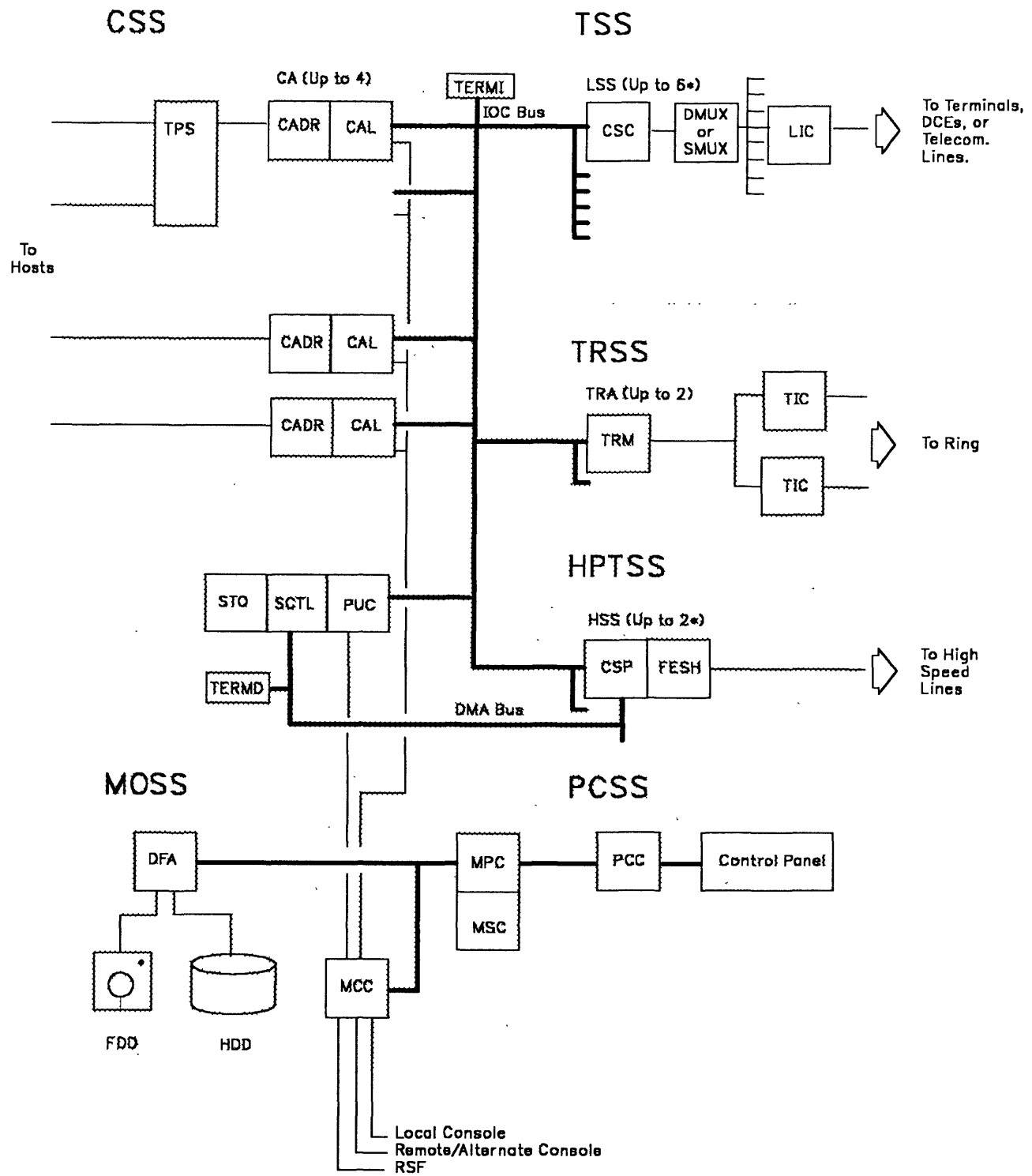
Chapter 4. Transmission Subsystem (TSS)

| | |
|---|------|
| 3745 Data Flow | 4-4 |
| Definitions | 4-5 |
| Low-Speed Scanner (LSS) | 4-6 |
| Definition | 4-6 |
| Communication Scanner Processor (CSP) | 4-6 |
| Front-End Scanner Low-Speed (FESL) | 4-6 |
| LIC Board | 4-7 |
| Definition | 4-7 |
| Multiplexer Card (MUX) | 4-7 |
| Line Interface Coupler (LIC) | 4-9 |
| LIC Types 1 to 4 Characteristics | 4-9 |
| LIC Types 5/6 Characteristics | 4-10 |
| Line Weights | 4-10 |
| LIC Internal Clock Function (ICF) | 4-11 |
| Serial Link (SL) | 4-12 |
| Communication Scanner Processor (CSP) | 4-12 |
| Components | 4-12 |
| Local Storage | 4-14 |
| Read-Only Storage | 4-14 |
| Control Storage | 4-14 |
| CSP External Registers | 4-14 |
| CCU/CSP Register Use | 4-17 |
| Ping/Pong Buffers | 4-17 |
| Processor Characteristics | 4-17 |
| Error Management | 4-17 |
| Scanner States | 4-18 |
| Scanner Commands | 4-20 |
| Front-End Scanner (FES) | 4-22 |
| Throughput | 4-22 |
| Data Flow | 4-22 |
| Storages | 4-23 |
| FESL Reset | 4-24 |
| FESL Reset Flow | 4-24 |
| Power ON Reset | 4-25 |
| Programmed Reset | 4-25 |
| Front-End Scanner Adapter (FESA) | 4-26 |
| FESA Data Flow | 4-26 |
| FESA-CSP Interconnection | 4-27 |
| FESA-Serial Link Interconnection | 4-27 |
| FESA Description | 4-28 |
| FESA RAM Organization | 4-28 |
| FESA Inbound/Outbound RAMs Addressing | 4-29 |
| FESA-FES Interconnection Management | 4-31 |
| Serial Link (SL) | 4-34 |
| Connection to LIC Type 5 and LIC Type 6 | 4-34 |
| Double Multiplexer Card (DMUX) | 4-35 |
| DMUX Functions | 4-35 |
| MUX 1 or 2 Data Flow | 4-36 |
| DMUX Functional Description | 4-37 |
| DMUX Reset | 4-37 |
| DMUX Hot Plugging | 4-38 |

| | |
|---|------|
| Single Multiplexer Card (SMUXA/B) | 4-39 |
| SMUX Functions | 4-39 |
| Transmit Level | 4-40 |
| SMUX Data Flow | 4-41 |
| SMUX Functional Description | 4-42 |
| SMUX Reset | 4-42 |
| SMUX Hot Plugging | 4-42 |
| LIC Types 1 to 4 Cards | 4-43 |
| Interface Lines | 4-43 |
| Transmit/Receive Data Mechanism | 4-44 |
| LIC Reset | 4-44 |
| Line Enable/Disable | 4-44 |
| Selective Scanning | 4-45 |
| LIC Logical Addressing Function | 4-46 |
| LIC Swap | 4-46 |
| LIC Address Register Contents | 4-47 |
| LIC Control Register | 4-47 |
| Enable Clock Mode | 4-47 |
| Transmit Clock Gating by RFS (LICs 1, 2, and 3) | 4-48 |
| LIC 4 Personalization | 4-48 |
| LIC Wideband with Line Speed Higher than 128 kbps | 4-48 |
| RTS Through DCE or Data Paths | 4-48 |
| LIC Modem-In Process for Non-X.21 Lines | 4-48 |
| LIC Modem-In Process for X.21 Lines | 4-48 |
| Internal Clock Function (ICF) | 4-50 |
| LIC Wraps | 4-51 |
| Hot Plugging of LICs | 4-53 |
| LIC Types 5 and 6 DTE Function | 4-54 |
| Transmit/Receive Data Mechanism | 4-54 |
| LIC Reset | 4-55 |
| Line Enable/Disable | 4-55 |
| Selective Scanning | 4-55 |
| LIC Swap | 4-55 |
| LIC Address Register Contents | 4-55 |
| LIC Control Register | 4-55 |
| LIC Wraps | 4-55 |
| LICs Hot Plugging | 4-56 |
| LIC Type 5 DCE Function | 4-57 |
| Maintenance Approach | 4-57 |
| Data Flow | 4-57 |
| Speeds | 4-57 |
| Configurations | 4-58 |
| Data Encoding and Modulation | 4-61 |
| DCE to Telephone Line Interface | 4-63 |
| Transit Time | 4-64 |
| RFS Delay | 4-64 |
| LIC Type 5 Panel | 4-65 |
| Line Specifications | 4-65 |
| Options and Configurations | 4-67 |
| Host Support | 4-71 |
| Manual Tests | 4-72 |
| Alarm Tone Detection | 4-73 |
| DCE Configuration | 4-73 |
| Portable Keypad Display (PKD) | 4-74 |
| PT2/3 | 4-79 |

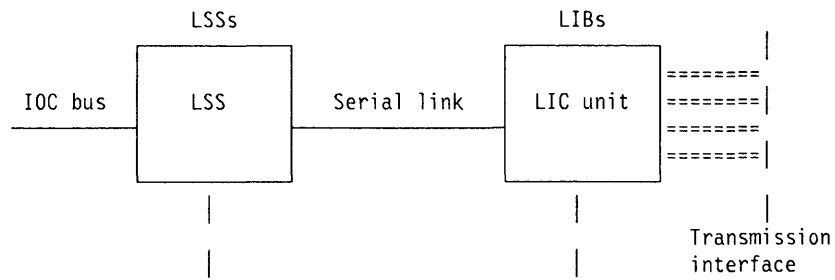
| | |
|---|-------|
| LIC Type 6 DSU/CSU Function | 4-80 |
| Connection to US DDS | 4-80 |
| Limited Distance Connection | 4-80 |
| Maintenance Approach | 4-80 |
| Data Flow | 4-80 |
| Speeds | 4-81 |
| Configurations | 4-81 |
| Data Format | 4-82 |
| Modulation Technique | 4-82 |
| DSU/CSU to Line Interface | 4-82 |
| Transit Time | 4-83 |
| RFS Delay | 4-83 |
| LIC Type 6 Panel | 4-84 |
| Line Specifications | 4-84 |
| Options and Configurations | 4-85 |
| Host Support | 4-87 |
| DDS Loop | 4-87 |
| Alarm Tone Detection | 4-87 |
| DSU/CSU Configuration | 4-88 |
| Portable Keypad Display (PKD) | 4-88 |
| Manual Tests | 4-91 |
| PT2/3 | 4-91 |
| Problem Determination Aid for LIC Types 1 to 4 | 4-92 |
| Intermittent Error Messages or Messages Lost | 4-92 |
| Wrap Tests Controlled from the Host | 4-93 |
| Wrap Tests Controlled from the MOSS | 4-94 |
| Problem Determination Aid for LIC Type 5 and LIC Type 6 | 4-95 |
| Wrap Tests Controlled from the Host | 4-95 |
| Wrap Tests Controlled from the MOSS | 4-95 |
| Manual Tests Controlled from the PKD | 4-95 |
| LIC Line Analysis Procedures (LLAP) | 4-100 |
| TSS interface cables | 4-100 |

3745 Data Flow

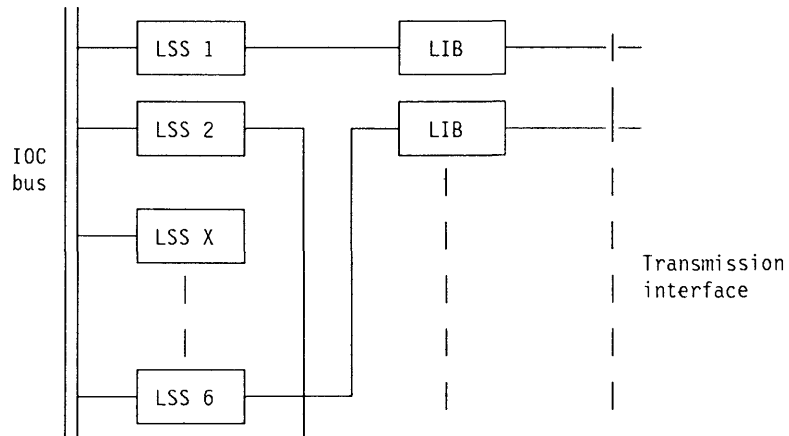


Definitions

The TSS consists of low-speed scanners (LSSs) associated to LIC a board through serial links.



However, it is possible to connect any LIC board to any low-speed scanner (LSS) by simply moving the serial link cables.

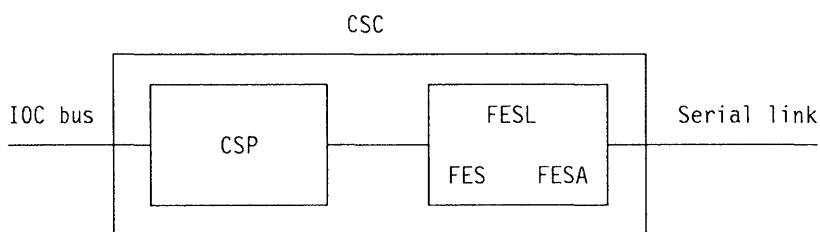


Low-Speed Scanner (LSS)

Definition

A low-speed scanner (LSS) is located on a communication scanner card (CSC) consisting of:

- A communication scanner processor (CSP)
- A front-end scanner low-speed (FESL).



Communication Scanner Processor (CSP)

The communication scanner processor (CSP):

- Supports various line protocols with partial handling of the data link control for BSC and SDLC lines. (The microcode allows the implementation of specific customer protocols.)
- Provides character buffering and cycle steal transfer into CCU main storage
- Supports start-stop with: 8/5, 9/7, 10/7, 10/8, 11/8 bits, BSC (EBCDIC, ASCII), SDLC, DIAL, X.21 native and X.21 bis
- Controls transmission interfaces
- Handles a variable number of lines depending on the protocol and transmission speed
- Provides four types of operating mode with NCP/EP
- Performs the checkout of the ROS code
- Interconnects the IOC buses through the receivers and drivers.

Front-End Scanner Low-Speed (FESL)

The front-end scanner low-speed (FESL) provides logical connection between the CSP and the LIC unit. It is composed of:

- The front-end scanner (FES)
- The front-end scanner adapter (FESA).

FES: It is composed of two layers:

- The front-end layer serializes and deserializes the characters, provides line service management depending on the protocols and exchanges the characters with the scanner processor.
- The scanner base layer communicates with the CSP via several paths:
 - An asynchronous path is used by the CSP microcode to initialize and send commands to the FESL and the LICs.
 - A cycle steal path supports data exchange of one halfword with the CSP control store.

An interrupt mechanism is used to request line service management.

FESA: The FESA converts FES parallel data into a serialized bit stream and conversely to communicate with the LIC units. In addition, the FESA performs modem-in control lead confirmation.

LIC Board

Definition

A line interface coupler (LIC) board consists of:

- Multiplexer cards (MUXs) and
- Line interface coupler cards (LICs).

Depending on the type of LIC implemented, the above elements are named:

LIB1 for LICs 1 to 4 on models 150-170

LIB2 for LICs 5 and 6 on models 150-170

LIB3 for LICs 1 to 4 on model 150.

| | |
|---|--|
| Model 130: N0 150: LIB1 170: LIB1 | Model 130: N0 150: LIB2 170: LIB2 |
| Model 130: N0 150: LIB3 170: LIB1 | Model 130: N0 150: N0 170: LIB1 or LIB2 |

Boards viewed from the rear
part of the machine

Multiplexer Card (MUX)

Double Multiplexer Card (DMUX)

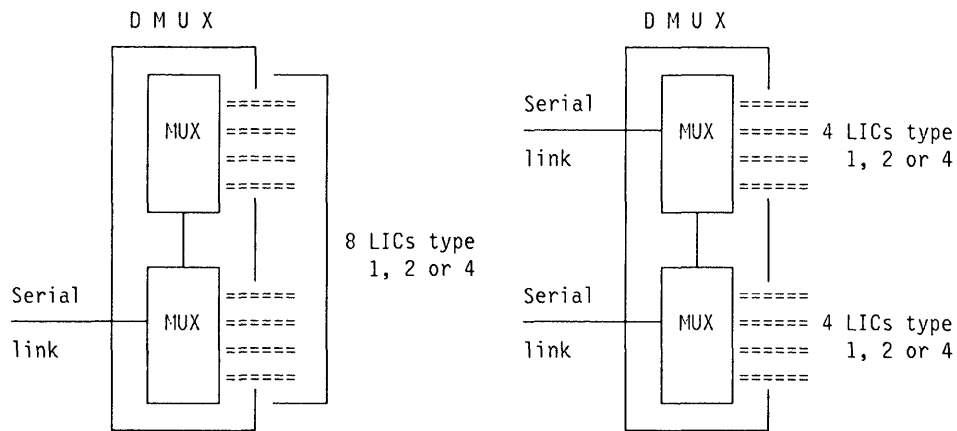
DMUX is associated with LIC1s to LIC4s on LIB1.

It provides two serial link attachments to connect to two scanner units. Each of them:

- Converts the serial link bit stream in a suitable form for LIC buses
- Performs the serial link clock recovery, synchronization, and repowering
- Manages LIC control and clocking.

The first MUX can attach up to:

- 8 LICs to one scanner if the second one is not used.
- 4 LICs to one scanner and the second MUX either (see TSS definition).

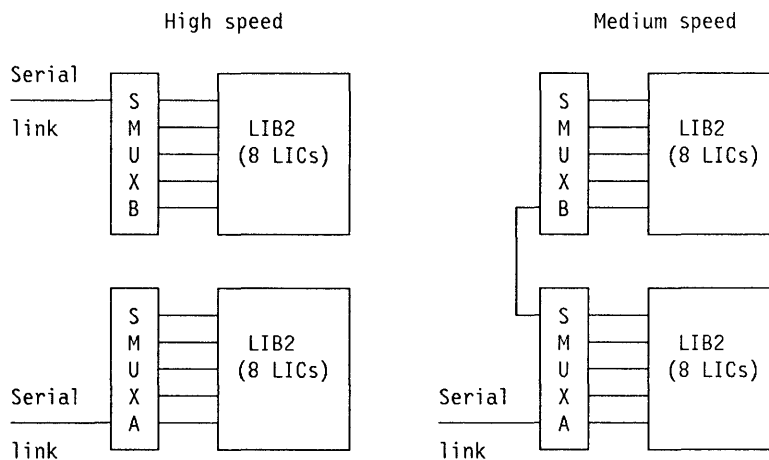


Single Multiplexer Card (SMUX)

SMUXA and SMUXB are slightly different in packaging but are functionally identical.

- SMUXA is associated with eight LIC type 5 and LIC type 6 on lower LIB2.
- SMUXB is associated with eight LIC type 5 and LIC type 6 on upper LIB2.

Depending on the transmission rate in a given LIB2, only one scanner may be needed for that LIB2. In that case, the SMUXB only bypasses the signals and controls from the SMUXA to the upper LIB2.



The SMUX cards provide one or two serial link attachment(s) to one or two scanner unit(s). Each of them:

- Converts the serial link bit stream in a suitable form for LIC buses
- Performs the serial link clock recovery, synchronisation and repowering
- Manages LIC control and clocking
- Provides 1 MHz clock signal to the LIC type 5 and LIC type 6
- Provides a 4-bit transmit level bus to the LIC type 5 DCEs.

Line Interface Coupler (LIC)

One line interface coupler (LIC) attaches up to four FDX/HDX lines to the controller. Two main families of LICs are available:

- Types 1 to 4 (DTE functionally) to attach up to four:
 - Stand-alone DCEs and/or
 - Direct-attached DTEs.
- Types 5 and 6 (DTE plus DCE functions) to attach up to two telecommunication lines.

LIC Types 1 to 4 Characteristics

| | LIC Type 1 | LIC Type 2 (RPQ) (note 5) | LIC Type 3 | LIC Type 4A (note 4) | LIC Type 4B high-speed (note 4) |
|---|--|---|----------------------------------|----------------------------|---------------------------------------|
| Line interface | V.24 (RS-232C), V.25 autocal (RS-366), X.21 bis X.20 bis V.25 bis | US wideband. Services 8751, 8801 and 8803 Bell 303 | V.35 high-speed | X.21 medium- speed | X.21 high-speed |
| Transmission speed | Up to 19 200 bps (Note 1) | Up to 230 400 bps (Note 1) | Up to 256 000 bps (Note 1) | Up to 9600 bps (Note 1) | Up to 256 000 bps (Note 1) |
| Number of lines | Up to four | One | One | Up to four | One |
| Transfer mode | Half-duplex or duplex | Half-duplex or duplex | Half-duplex or duplex | Half-duplex or duplex | Half-duplex or duplex |
| Protocols | Start-stop, BSC, SDLC | BSC and SDLC | BSC and SDLC | SDLC | SDLC |
| DTE clocking (Note 2) | Up to 19 200 bps | Not allowed | Not allowed | Not allowed | Not allowed |
| Direct attach- ment (Note 3) | Up to 19 200 bps | Not allowed | Up to 245 760 bps | Up to 9600 bps | From 19 200 to 245 760 bps |

Notes:

- The total number of LICs per CSC is not limited by performance considerations (refer to "Selective Scanning" on page 4-45 for description).
- Called 'internal clock' on CDF information screen.
- Direct attachment allowed with internal clock function (ICF).
- LIC type 4A and LIC type 4B are physically identical (same part number). The microcode sets the LIC to the appropriate type at set mode time.
- LIC type 2 is available only on RPQ basis.

LIC Types 5/6 Characteristics

| | LIC Type 5 | LIC Type 6 |
|--------------------|--|--|
| Line interface | Normal quality or M.1020/1025 4-wire telecommunication lines | DDS, local loop, or unloaded baseband 4-wire lines |
| Transmission speed | <ul style="list-style-type: none">• 4800 bps• 9600 bps• 14 400 bps | <ul style="list-style-type: none">• 9600 bps• 19 200 bps• 56 000 bps |
| Number of lines | Two | One |
| Transfer mode | Half-duplex or duplex | Half-duplex or duplex |
| Protocols | BSC and SDLC | BSC and SDLC |
| DTE clocking | Not allowed | Not allowed |
| Direct attachment | Not allowed | Not allowed |

LIC Type 6, Plugging Limitations

Speeds \leq 19 200 bps

The LIC type 6 can be plugged contiguously in all card positions of the board.

Speed = 56 000 bps

Only the odd position out of a pair (even/odd) of card positions can be used to plug the LIC type 6. In this case:

- The LIC type 6 must be plugged in the odd position.,
- Any attempt to plug a LIC in the empty position associated with the LIC type 6 makes the latter inoperative with its yellow LED flashing to signal that condition.
- Any CDF change involving a 56 000 bps LIC 6 plugged in even position will be ignored.

Line Weights

The weight of a line is a value (0.4 through 100) that represents the percentage of scanner occupation. The total weight of all the lines connected to a scanner must be less than or equal to 100.

The maximum number of LIC positions supported per low-speed scanner depends on the line with the highest transmission speed connected to the scanner, and is limited to:

- Eight LIC1s to LIC4s per scanner (LIB1), or
- Four LIC1s to LIC4s per scanner (LIB3, on model 150 only), or
- Sixteen LIC type 5 or LIC type 6 per scanner (LIB2)

For each speed, LIC types 1/4A/5 have two weights per protocol depending on the number of LICs per scanner.

The line weight can be calculated by using the formula:

$$\text{Weight} = \frac{\text{Speed (bps)}}{K}$$

where K is specified by the chart below:

| Line Protocol | LIC Types 1/4A/5 | | LIC Types 3/4B/6 |
|--|---|------|------------------|
| | Number of LIC 1/4A or Number of LIC 5 Pairs per LSS | | |
| | ≤ 4 | > 4 | |
| SDLC FDX | 1920 | 1536 | 2560 |
| <ul style="list-style-type: none">• SDLC HDX• BSC EBCDIC NCP• BSC EP | 3456 | 3072 | 4052 |
| BSC ASCII NCP | 2420 | 2016 | 3041 |
| Start/stop (burst mode) | 43 x B, where B is the number of bits/character (for example 430 if 10-bit characters) | | |

Refer to the *Connection and Integration Guide*, SA33-0129 Appendix B, for more information to calculate the line weights.

Complete information to populate the 3745 properly can be displayed or printed from the *3745 Configuration Program* diskette, GA33-0093 running in any IBM PC.

Inactive Lines

Unlike earlier communication controllers, 3745 LICs are not scanned if **all** the lines connected to them are inactive, and hence do not load the scanner.

LIC Internal Clock Function (ICF)

Implemented on each LIC 1 to 4, the internal clock function (ICF) provides the clock control to:

- Non-clocked DCEs
- Direct-attached terminals.

Serial Link (SL)

A serial link interconnects a LIC board and a scanner unit via MUX and CSC cards.

Communication Scanner Processor (CSP)

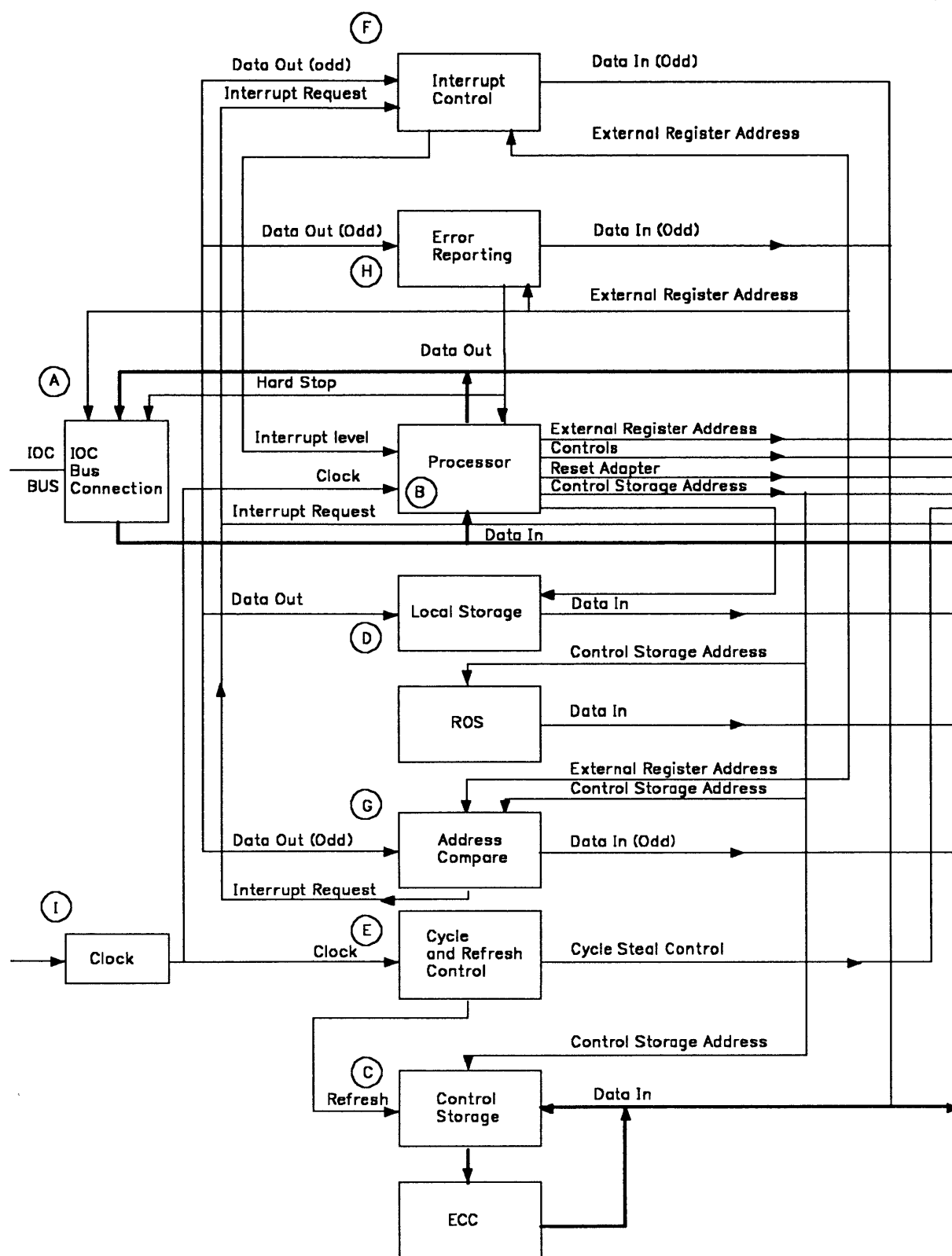
The communication scanner processor (CSP) operates under the control of the scanner microcode loaded from the hard disk drive or diskette drive into CSP storage during IML.

The CSP is located on the communication scanner card (CSC).

Components

As shown on the next data flow the CSP:

- (A) Connects to the IOC bus to receive or transmit data and controls
- (B) Executes the instructions of the microcode to transmit and receive data, supports the link protocols, translates characters, and controls the communication interface.
- (C) Stores the microcode, the transmitted/received data, the line interface parameters, and the diagnostics
- (D) Provides registers in local storage for current CSP operation and permanent code in the ROS to start the microcode IPL.
- (E) Controls the storage and manages (by hardware only) the cycle steal with the FESL.
- (F) Controls the CSP interrupts.
- (G) Provides control storage address compare, and generates a CSP interrupt when the selected address is encountered.
- (H) Detects and reports the CSP errors via the CSP error register.
- (I) Generates clocking signals to the processor, to the FESL and their associated logic from the basic 49.152 MHz clock.



Local Storage

The local storage is 128 bytes long (64 halfwords) addressed by byte or by halfword. It is organized in 16 blocks (or pages) of eight local storage registers (LSRs), each of them being one-byte long, used to store the microcode pointers, the cycle steal and command queue control blocks, the program status words, and working register.

The local storage registers can be displayed or altered from the operator console, using the TSS functions.

Read-Only Storage

The read-only storage (ROS) is 8K bytes long (4K halfwords) addressed by halfwords. It includes all the permanent code needed to IML or dump the microcode and to perform diagnostics.

The ROS can be displayed from the operator console, using the TSS functions.

Control Storage

The control storage is 64K halfwords long addressed by halfword.

In each module, an error checking and correction (ECC) mechanism detects and corrects the single or double bit errors (soft or hard) of that module.

When an unrecoverable double error is detected, register X'03' bit 1 is set ON, a hardstop condition is raised, and two data bytes with parity are sent to the CCU.

The control storage is used to store:

- The scanner microcode.
- The buffers for the transmitted and received data, and the line control blocks and parameters.
- Tables and service buffers.

The control storage can be displayed or altered from the operator console, using the TSS functions.

CSP External Registers

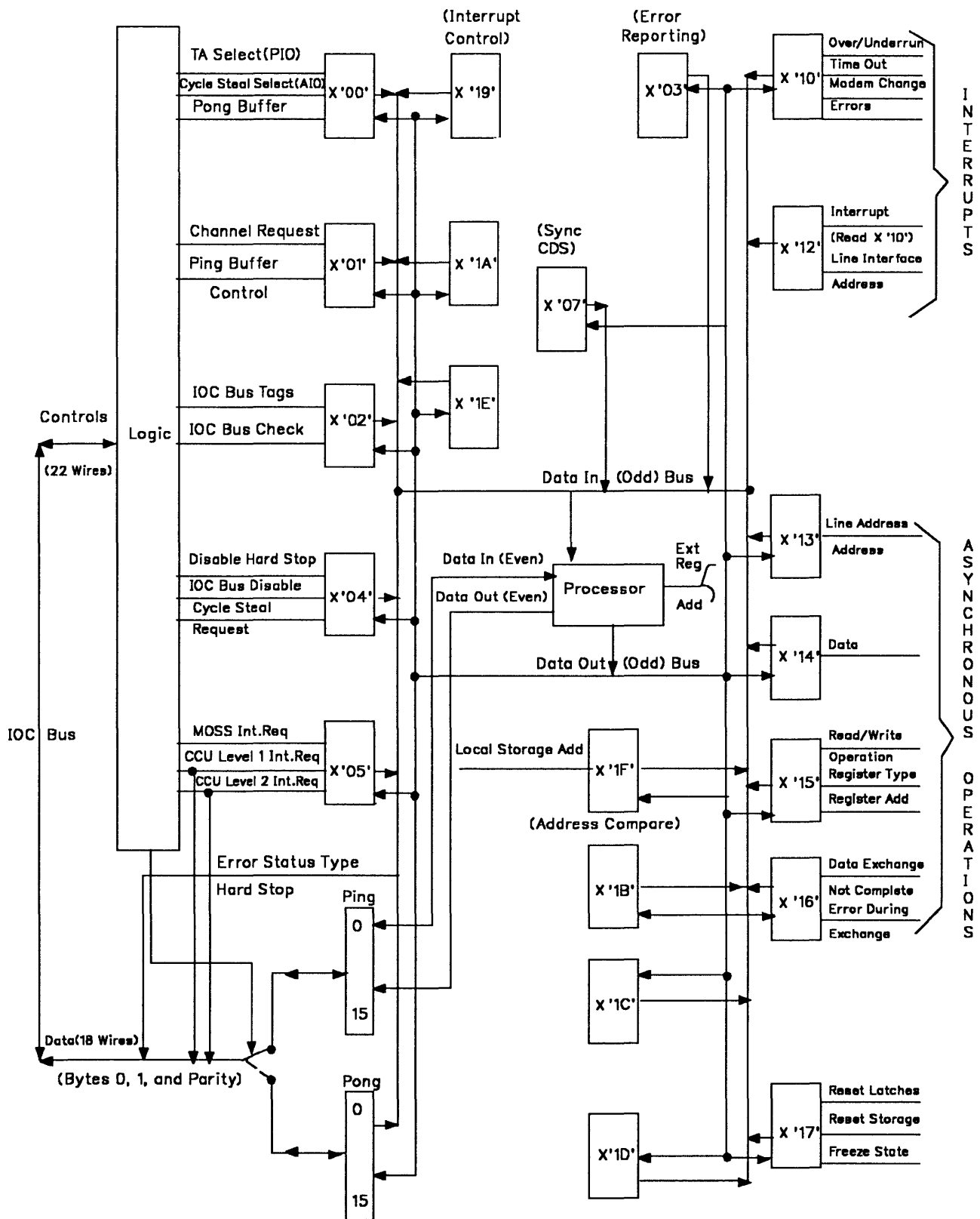
The CSP uses 32 eight-bit external registers located in the main communication scanner components: IOC bus connection, address compare, error reporting, and front-end scanner.

The external registers are connected to the CSP via the data in (odd) bus during read operations, and data out (odd) bus during write operations. Their bits are set ON or OFF by the hardware or the microcode.

The external registers can be displayed or altered from the operator console, using the TSS functions.

| Address | Function |
|---------|--|
| 00 | Miscellaneous control |
| 01 | IOC bus control |
| 02 | IOC bus service |
| 03 | CSP error |
| 04 | CSP miscellaneous |
| 05 | External interrupt request |
| 06 | Not used |
| 07 | Synchro/configuration data set |
| 08 | Not used |
| 09 | Not used |
| 0A | Fast get line ID byte 0 |
| 0B | Fast get line ID byte 1 |
| 0C | Scanner alternate address |
| 10 | Extended interrupt request |
| 11 | Not used |
| 12 | Interrupt request line interface address |
| 13 | Asynchronous access RAM A/B/C |
| 14 | Data in/out |
| 15 | Asynchronous access RAM A/B/C |
| 16 | Asynchronous operation status |
| 17 | FESL general command |
| 18 | Not used |
| 19 | PCI/IO interrupt level request |
| 1A | Current CSP interrupt |
| 1B | Address compare control |
| 1C | Address compare byte 0 |
| 1D | Address compare byte 1 |
| 1E | CSP interrupt masks |
| 1F | Local storage page register (hex) |

FESL
(Scheduler and Address Selector)



CCU/CSP Register Use

The CSP external registers are used by the following operations:

- Program-initiated operation (PIO)
- Adapter-initiated operation (AIO)
- Interrupt operation.

Ping/Pong Buffers

Two half-word registers, called the ping and pong buffers, located in the local storage, are alternately connected to the IOC bus in flip/flop mode.

They are used for transferring commands, data, and control words between the IOC bus and the CSP.

Switching from one buffer to the other is controlled by the IOC logic.

Processor Characteristics

Program Levels

The interrupts are raised by the microcode (all levels) or by hardware (levels 0, 1, and 2). Levels 0 through 3 can be masked by the microcode.

| Level | Function |
|-------|--|
| 0 | Error handling and address compare |
| 1 | CCU instruction processing |
| 2 | FESL interrupt processing |
| 3 | Queue and command processing |
| 4 | Not used |
| 5 | Not used |
| 6 | Not used |
| 7 | Timer control and disconnect stop initialization |

Clock

An oscillator on the CSC card provides the 49.152 MHz square wave to generate the scanner processor's clock. The 49.152 MHz is also sent to the FES and FESA for clock generation.

Two other clocks are generated in the CSP:

- A 100 ms clock used for timer purposes
- A 15.4 μ s clock used to refresh the storage.

Error Management

Internal CSP errors detected by the CSP hardware cause a CSP hardstop. Two bytes of status information are presented by the CSP either to the CCU control program (NCP) or to the MOSS after the hardstop condition is detected.

Hardstop

A hardstop condition is handled by the CSP hardware as follows:

1. A permanent cycle steal request is forced internally to the CSP processor, preventing any cycle steal operation.

Cycle steal having the highest priority with CSP storage, the CSP microcode processing stops, but the CSP clocks keep running.

- A level 1 interrupt request is presented to the CCU control program (NCP) if the CSP is in 'Connect' mode.
 - A level 4 interrupt request is presented to the MOSS processor control program if the CSP is in 'Disconnect' mode.
2. The CCU control program (NCP) responds to its level 1 interrupt request by sending a 'get error status' command, as long as the CSP which has raised the level 1 is found.

The CSP then sends the two bytes of 'error status type hardstop' if the CSP clocks are not stopped by the hardstop condition.

3. The MOSS control program responds to its level 4 interrupt request by sending a 'get command completion' command. The CSP then sends the two bytes of 'MOSS command completion' if the CSP clocks are not stopped by the hardstop condition. Then the MOSS control program sends a 'get error status' command to which the CSP responds with the two bytes of 'error status type hardstop'.

The error status type hardstop does not transit through the ping/pong buffers, but is directly presented on the IOC bus data bytes.

The hardstop is reset from the CCU or the MOSS via a programmed reset command or a general reset.

Scanner States

The state of a scanner is shown on the console display (refer to the 3745 *Service Functions*, SY33-2069). The state may be:

- | | |
|---------------------|--|
| Inoperative | The scanner is inoperative when it is not in any other state. |
| Initialized | The scanner is initialized when the CSP is loaded with the microcode and the FESL storage is initialized to all zeros. There is no operation with the control program. |
| Connected | The scanner is connected when it runs under control of the control program. Errors on CCU I/O instructions are reported to the control program, and errors on MOSS I/O instructions to the MOSS. |
| Disconnected | The scanner is disconnected when it does not run under control of the control program but under control of the MOSS microcode. |

Only MOSS I/O instructions are executed. Any instructions from the CCU are not answered.

When disconnected from the control program, the scanner may be:

Running (disconnected-go)

The scanner can be in this state while being IMLed, dumped, or being fixed using the TSS services.

Stopped (disconnected-stop)

The microcode continues to react to the MOSS instructions. The scanner can be in this state while being fixed using the TSS services.

Any errors are reported to the MOSS.

The scanner may be disconnected by the :

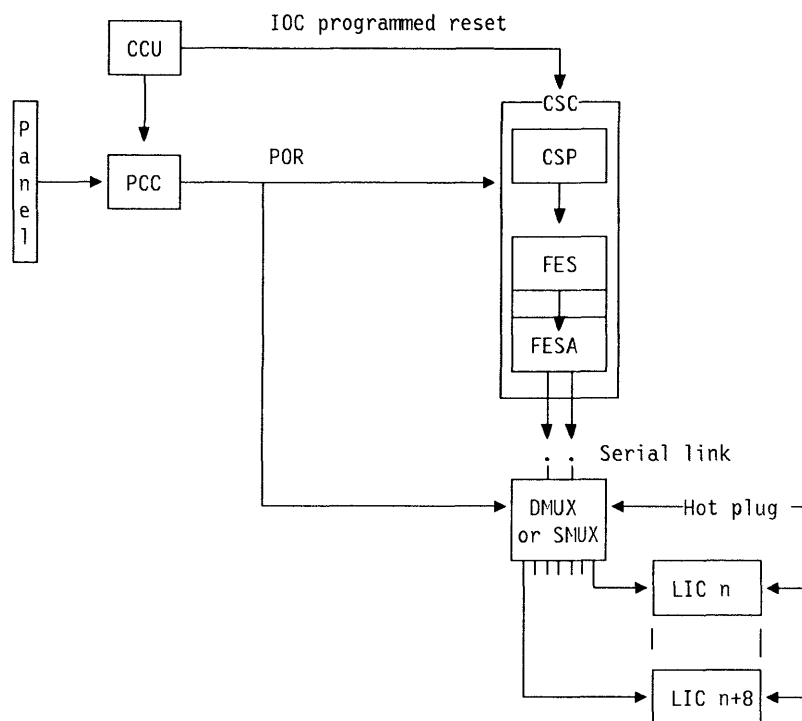
- Operator when entering a service command (stop or address compare with the stop option selected, for example)
- Microcode when certain errors are detected (a CCU interrupt level 1 is requested with the disconnect indication).

CSP Reset

Resetting a CSP can be done by:

- A specific power ON reset (POR) line coming from the power box for each CSP.
- A programmed reset PIO for each CSP, sent by the control program or by the TSS services (operator console).

In these two cases, the state of the CSP is reset. In case of individual POR, the MOSS microcode waits 12 s, before attempting to start an operation with the CSP again.



Power ON Reset

When the CCU activates the line POR (on the IOC bus) during a general IPL or a power ON, the register X'04' bit 2 is set in every scanner, which:

1. Forces a CSP interrupt level 0.
2. Starts microcode execution at address 0, initiating the following functions:
 - General reset with a reset of the CSP storage
 - Start of ROS diagnostics
 - Reset of clocks
 - Reset of external registers X'03' (CSP error) and X'08' (error indicators/bad parity generator).
3. Disables the IOC bus and reset the FESL (by setting ON the reset adapter). The LICs and ICFs are reset at the same time.

Programmed Reset

The control program can reset a specific scanner by sending a write command in PIO mode, with the operation code 'programmed reset', along with the scanner address.

This command is latched on external register X'04' bit 1, then, the selected scanner:

1. Disables the hardstop (X'04' bit 3 ON).
2. Starts the microcode at level 0 address 0, with a jump to the end of diagnostics to wait for a dump or re-IML.
3. Resets the interrupt requests to the MOSS and CCU (X'05' bits 0 and 2 ON).
4. Stops the connected FESL (FESL status: freeze) but the storages of the CSP and FESL are not reset and the CSP storage can be dumped.

The 'reset to adapter' is activated by the microcode, rising the X'04' bit 2 during a few instructions.

Scanner Commands

The following commands may be used from the operator console to modify the scanner state.

| Current State | Possible Scanner Commands | Resulting State |
|-----------------|------------------------------|--|
| Connected | Stop Reset Dump IML | Disconnected/stop Reset Reset Initialized |
| Disconnected/go | Stop Reset Dump IML | Disconnected/stop Reset Reset Initialized |

| Current State | Possible Scanner Commands | Resulting State |
|-----------------------------|---|---|
| Disconnected/stop | Start Reset Dump IML | Disconnected/go Reset Reset Initialized |
| Reset or Unknown mode | Reset Dump IML | Reset Reset Initialized |
| Initialized | Stop Connect Reset Dump IML | Disconnected/stop Connected Reset Reset Initialized |
| Inoperative | Reset Dump IML | Reset Reset Initialized |

Front-End Scanner (FES)

The front-end scanner (FES) is an adapter of the CSP. It is part of the communication scanner card (CSC). Its scanning circuit supports, under the control of the CSP, a wide range of protocols and line interfaces.

Throughput

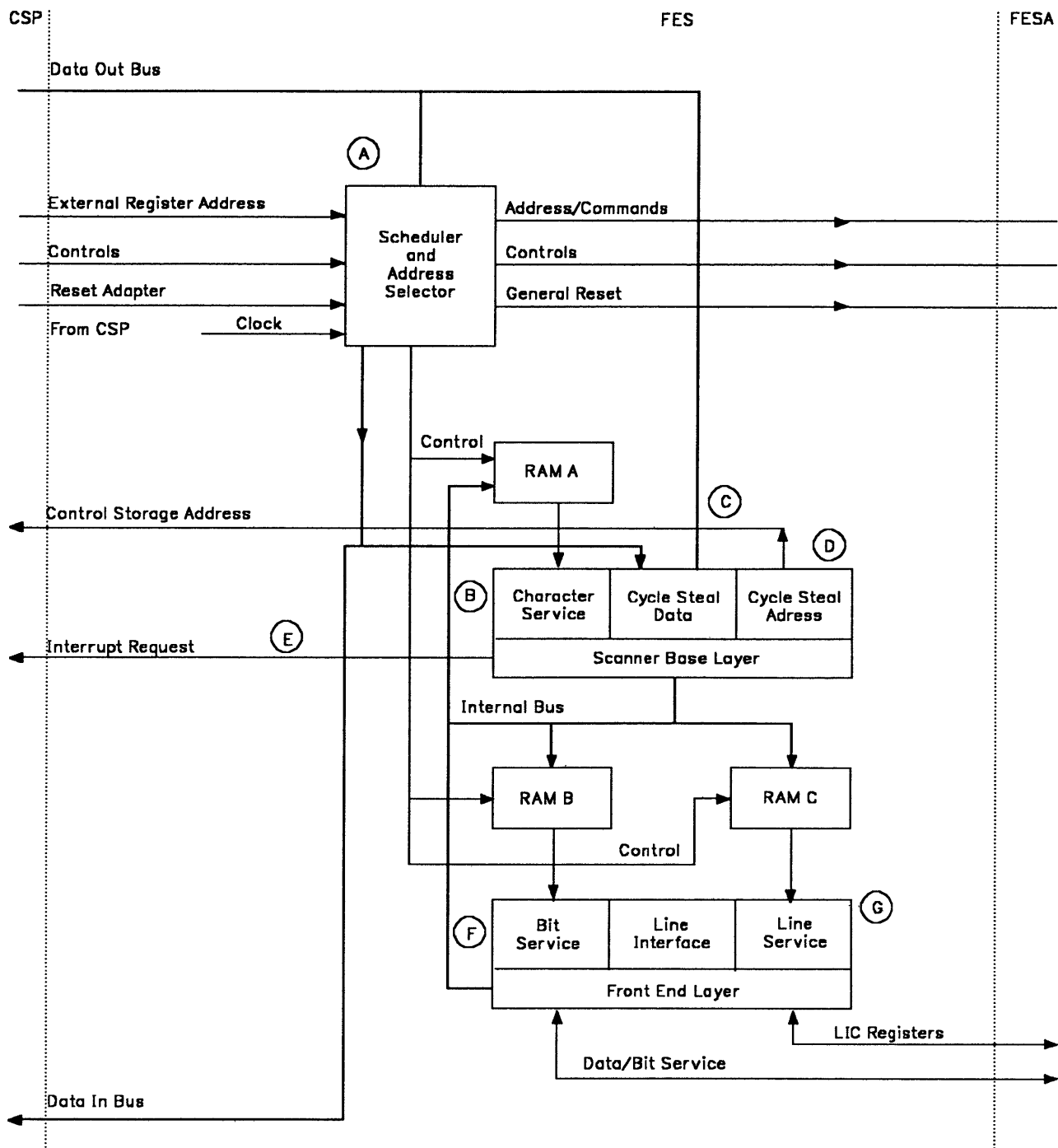
The FES maximum throughput varies from 256 kbps (for one line attached), to 307.2 kbps (for 32 lines at 9600 bps distributed over eight LICs).

The throughput is spread over the LICs up to the last one enabled on the LIC unit. If only one LIC is enabled, all the throughput is devoted to that LIC.

Data Flow

As shown on the next data flow, the FES:

- (A) Controls the FES timing, the exchange with the CSP, and the RAM operation.
- (B) Controls the transfer of characters between the front-end and the CSP.
- (C) Handles the data halfwords coming from or going to the control storage.
- (D) Provides cycle steal control for the CSP.
- (E) Interrupts the CSP on level 2 for buffer and data management, and for error reporting.
- (F) Serializes/deserializes the data bits transmitted to or received from the FESA.
- (G) Provides line services related to link protocol and modem control by managing the LICs via the FESA and the serial link.



Storages

The FES includes three random access storages (RAMs):

- RAM A for character service
- RAM B for bit service
- RAM C for line service.



-

Power ON Reset

The FES 'reset line' signal is driven by CSP R'04' bit 2. This bit is set by the hardware in case of POR, or by the microcode in case of programmed reset. It is reset by the microcode. This 'FES reset' signal:

1. Resets the FES latches and sets the FESA reset tag.
2. Disables the lines between the CSP and the FES.
3. Resets the FES RAMs: all bits are set to zero and the correct parities are written.
4. Stops all scanning (the FES remains in the freeze state after this reset).

The reset tag from FES starts the following sequence in the FESA:

1. Reset FESA latches and set FESA serial link to 'no transmission'.
2. When reset OFF, reset FESA RAMs.
3. Then, set FESA to normal mode.

Programmed Reset

The FESA can also be reset by the microcode by setting bits 0, 1, and 2 of the control register common address X'A' with line address '00'.

- Bit 0 resets FESA latches and sets FESA serial link to 'no transmission'.
- Bit 1 resets FESA RAMs.
- Bit 2 freezes FESA.

Front-End Scanner Adapter (FESA)

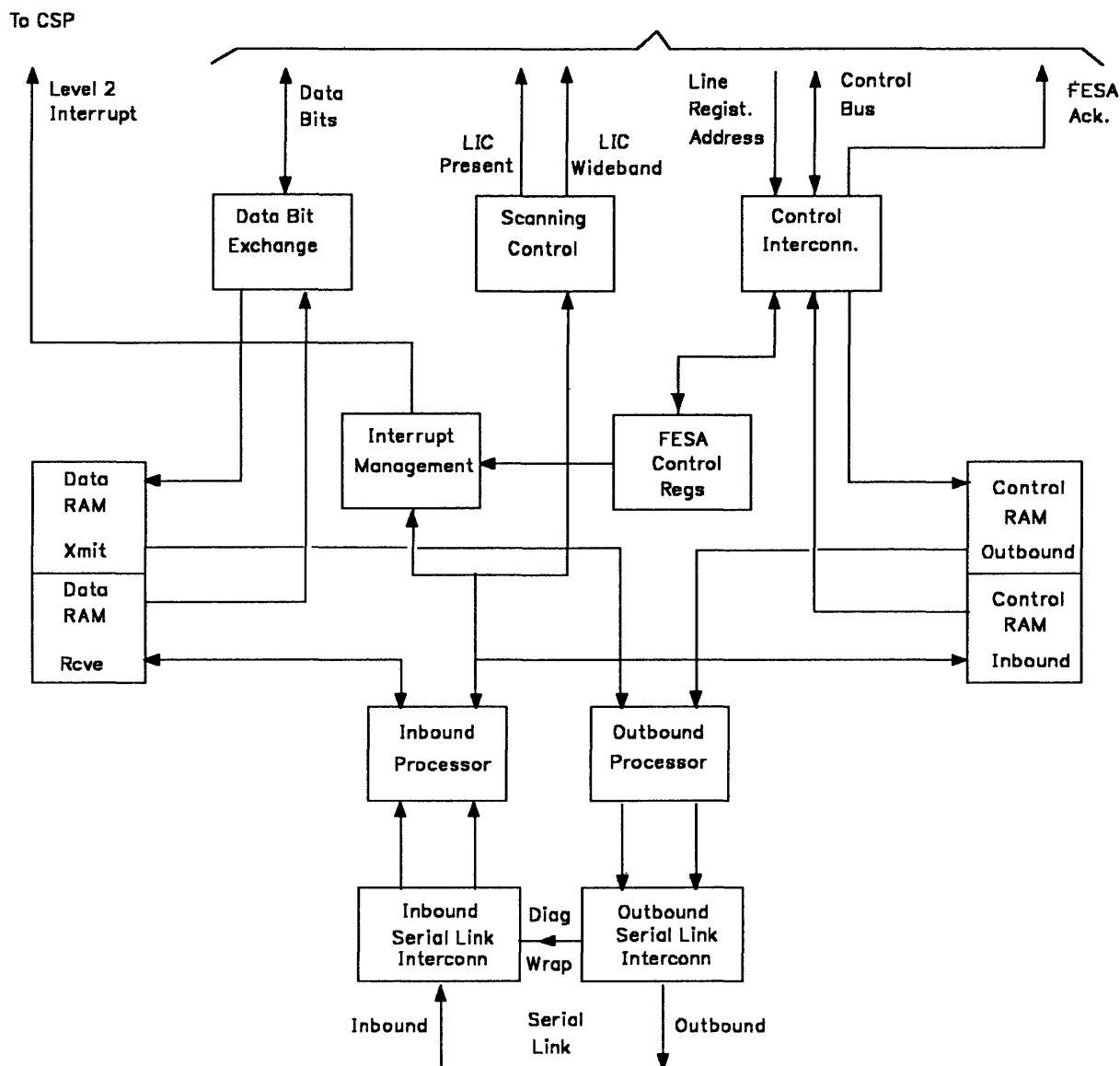
The front-end scanner adapter (FESA) is the third part of the CSC card

The first purpose of the FESA is to convert the FES parallel bus into the serial link bit stream and conversely.

FESA Data Flow

The FESA data flow shows:

- The interconnection of FESA with the two serial link processors (inbound and outbound).
- The FESA to FES interconnection.
- The internal organization around the FESA RAMs to manage the data and control information exchanged by the FES and the serial link.



FESA-CSP Interconnection

The FESA level 2 interrupt tag allows the FESA to directly communicate with the CSP.

FESA-Serial Link Interconnection

The FESA is connected to the associated LIC units (through the DMUX/SMUX cards) by means of two twisted pairs:

- One pair for the outgoing frames (outbound serial link)
- One pair for the incoming frames (inbound serial link).

FESA Description

The FESA converts FES parallel data into a serial bit stream.

Three RAMs are implemented in the FESA to be used as LIC/MUX registers (inbound and outbound control RAMs), and to be used as data buffer during the process (data RAM).

- The outbound control RAM stores the FES and microcode commands to MUX and LICs (set mode) before being carried by the proper slots of the outgoing frames sent on the outbound serial link.
- The inbound control RAM stores the MUX and LIC registers information sent by the LICs, and transferred to the CSP on microcode request.
- During the transmit and receive process, the data RAM stores data and control bits for each line. The FESA uses the RAM as a working area to serialize and assemble the data bursts.

Each RAM is divided into 32 areas (one area per line). In the control RAMs, each area contains the line register information.

The RAMs are time-shared by the FES and the two serial link interconnections (inbound and outbound).

The FESA synchronizes the various RAM requests. It monitors the FES RAM access requests and monitors the outbound and inbound serial link frames.

RAMs can be displayed or altered, using the TSS functions.

In addition, the FESA:

- Controls the FES scanning mechanism by generating the LIC present and the LIC wideband patterns
- Controls the modem-in leads according to parameters loaded by microcode in the FESA control RAMs
- Detects and reports the errors occurring on the LIC, the MUX, the serial link, or the FESA itself
- Generates the FESA level 2 interrupts to the CSP microcode to report DCE management events or errors
- Performs the diagnostic functions to test the FESL card, the DMUX or SMUX card and the serial link
- Synchronizes the frame and superframe with the MUXs.

FESA RAM Organization

There are three RAMs in the FESA:

- Two 1-Kbyte control RAMs
- One data RAM of 128 halfwords.

FESA Inbound and Outbound Control RAMs

The control RAMs contain all the information required by the FES and the microcode to manage the lines.

The control RAMs are divided into 32 areas. Each area stores the contents of the MUX/LIC registers associated to one line.

FESA Inbound/Outbound RAMs Addressing

The CSP microcode uses two CSP external registers (X'13' and X'15') to access the outbound and inbound RAMs,

The FESA external registers are located in the outbound and inbound RAMs. The following tables show the bits of registers X'13' and X'15' used to access the FESA inbound and outbound RAMs.

X'13': Line Interface Address

| Bits | Functions |
|-----------------|--|
| 0 0 | Not used, always 00 |
| . . x x x . . . | Card address |
| x x . | Line address |
| Z | See 'FESA inbound/outbound RAM layout' |

X'15': Asynchronous Operation Command

| Bits | Functions |
|-----------------|--|
| x | OFF = read, ON = write |
| . x x | External |
| . . . I R R . . | See 'FESA Inbound/Outbound RAM layout' |

Local Store 6 (CHHITMIO Input)

| Bits | Functions |
|-----------------|--|
| x | OFF = read, ON = write |
| . . x | OFF = outbound RAM, ON = inbound RAM |
| . . . I R R E Z | See 'FESA Inbound/Outbound RAM Layout' |

FESA Inbound/Outbound RAM Layout

FESA control register bit 5, controls the type of operation:

OFF Write or output operation
ON Read or input operation.

| Bit Decoding | Write (FESA ctrl reg bit 5=0) Outbound RAM | Read (FESA ctrl reg bit 5=1) Inbound RAM |
|--------------|---|---|
| E I Z R R | | |
| 0 0 0 0 0 | Not used | Not used |

| Bit Decoding E I Z R R | Write (FESA ctrl reg bit 5=0) Outbound RAM | Read (FESA ctrl reg bit 5=1) Inbound RAM |
|---------------------------|---|---|
| 0 0 0 0 1 | Modem out | Driver check pattern |
| 0 0 0 1 0 | Line control | Line control |
| 0 0 0 1 1 | Driver check mask | Clock failure timer |
| 0 0 1 0 0 | FESA modem control | Modem in |
| 0 0 1 0 1 | RFS parameters | RFS work timer |
| 0 0 1 1 0 | Wrap control | Wrap ctrl/ cable id |
| 0 0 1 1 1 | LIC clock mode | LIC card ID/clock mode |
| 0 1 0 0 0 | Receive interrupt control | Receive interrupt stack |
| 0 1 0 0 1 | Xmit interrupt control | Xmit interrupt stack |
| 0 1 0 1 0 | FESA/MUX/LIC registers (See note) | FESA/MUX/LIC registers (See note) |
| 0 1 0 1 1 | Not used, FES diag | Not used, FES diag |
| 0 1 1 0 0 | DSR/RI parameters | DSR/RI work timer |
| 0 1 1 0 1 | RLSD parameters | RFS/TI drop w.rlsd |
| 0 1 1 1 0 | ICF RAM 4C | ICF RAM 4C |
| 0 1 1 1 1 | Not used, FES diag | Not used, FES diag |

Note: These registers are called 'FESA general registers'. General register '00' is dedicated to line 0, general register '01' is dedicated to line 1, and so on. To extend FESA/MUX/LIC register addressing, the microcode sets the FESA control register with the external register address bit ON (E).

| Bit Decoding E I Z R R | Write (FESA ctrl reg bit 5=0) Outbound RAM | Read (FESA ctrl reg bit 5=1) Inbound RAM |
|---------------------------|---|---|
| 1 0 0 1 1 | Not used | Line error register |
| 1 0 1 0 0 | SDF | SDF |
| 1 0 1 0 1 | Control SDF/burst size | Control SDF |
| 1 0 1 1 0 | PDF | PDF |
| 1 0 1 1 1 | Control PDF | Control PDF |
| 1 1 0 0 0 | Line diagnostic register | Line diagnostic register |
| 1 1 0 0 1 | Logical address | Physical add./EC number |
| 1 1 0 1 0 | Not used, FESA/MUX reg | Not used |
| 1 1 0 1 1 | Not used, FES diag | Not used FES diag |
| 1 1 1 0 0 | ICF RAM 4D1 | ICF RAM 4D1 |
| 1 1 1 0 1 | ICF RAM 4D2 | ICF RAM 4D2 |
| 1 1 1 1 0 | Not used | Modem-in immediate |
| 1 1 1 1 1 | Not used FES diag | Not used FES diag |

FESA Data RAM

The FESA data RAM is divided into 32 areas (one area per line) of four halfwords each:

| Halfword | Byte 0 (Even address) | Byte 1 (Odd address) |
|----------|--------------------------|-------------------------|
| 0 | Receive SDF | Receive control |
| 1 | Receive PDF 0 | (Not used) |
| 2 | Receive PDF 1 | (Not used) |
| 3 | Transmit SDF | Transmit control 1 |
| 4 | Transmit PDF | Transmit control 2 |

The data RAM is shared by the inbound and outbound serial link data processors, and by the FES for data exchange.

FESA-FES Interconnection Management

LIC Enabled Leads

The LIC enabled leads are used by the microcode to dynamically modify the FES scanning range. A LIC is enabled when at least one line of that LIC is enabled (line control register bit 1 ON).

The LIC is disabled when all lines of the LIC are in the disabled state (line control register bit 1 OFF in all lines.)

The FESA builds the LIC enabled pattern by monitoring the line enabled information sent by the LICs over the inbound serial link.

Note: Disabled LICs are seen as not present by the FES and, consequently, these LICs are not scanned in order to accept higher throughput on remaining active lines. The 'LIC 0 present' is not given to the FES, which always assumes that the first LIC is present, as a minimum configuration.

The FESA makes no difference between the LIC's physical and logical addresses:

- For the FESA, the position of a LIC is determined by the slots occupied by this LIC in the inbound frame.
- When a line is enabled by the microcode, and presents 'line enabled' to the FESA, the FESA does not set 'LIC present' immediately. Instead, it sets line control register bit 6 in the inbound control RAM ('line enabled remembrance'), and waits for the next 'line enabled' (at next superframe), to set line control register bit 1, and update 'LIC present'.
- The 'LIC enabled' pattern can be read by the microcode, by successively addressing the two corresponding registers in the FESA.

Note: For example, assuming a LIC plugged in physical position 0 on the LIC board:

- If this LIC receives logical address 7, it occupies the slots assigned to LIC number 7 and will be seen as LIC in physical position 7 by the FESA and FES.
- If this LIC has no line enabled, it will not be scanned.

LIC Wideband Leads

The LIC wideband information is used by the FES to scan wideband lines four times faster than non-wideband lines.

DCE Lead Management

Modem-in: The modem-in information coming from the lines, is stored in the inbound control RAM address X'1E' of each line. When a line is scanned by the FES, modem-in is passed by the FESA to the FES for DCE change detection.

To perform the modem-in control, the FESA keeps the confirmed modem-in patterns in the inbound control RAM (Address X'04') for the FES requests, and monitors.

Control of DSR, RI, and RLSD: For any line, the FESA is able to confirm the changes of any of these signals by using specific timers. DSR, RI, and RLSD are confirmed for both raising and falling edges.

Integration of I (X.21) is performed for I drop only (I going ON is immediately reported to FES in any case.

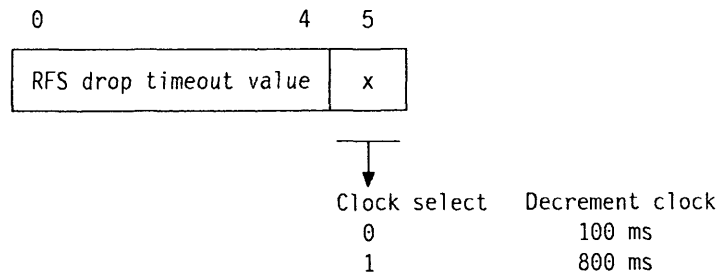
A different timer starts each time the associated signal switches. The change is confirmed when the time out is reached.

The confirmation delay is specified, for each signal, in a 3-bit parameter field, loaded by the microcode, in the outbound control RAM.

| Parameter Value | Time out |
|------------------------|---|
| 0 0 0 | 0 (Immediate reporting) |
| 0 0 1 | 1 ms |
| 0 1 0 | 4 ms |
| 0 1 1 | 16 ms |
| 1 0 0 | 32 ms |
| 1 0 1 | 64 ms |
| 1 1 0 | 128 ms |
| 1 1 1 (RI, I, or RLSD) | 256 ms |
| 1 1 1 (DSR drop) | 10 s |
| 1 1 1 (DSR raising) | Parameter value loaded elsewhere for RI |

Control of RFS: Only the drop of RFS is controlled. The FESA monitors the drop on microcode request, in the following way: The FESA controls the drop of RFS when the microcode loads the RFS drop time out value in the outbound control RAM, along with the clock select bit which chooses the decrement clock.

Outbound control RAM address: X'05' (00101)



Control of TI: The immediate value of TI is passed by the FESA to the FES in the modem-in field for DCE change detection. When TI is masked in the FES, the FESA memorizes (for microcode information) that TI has raised, by setting bit TI 'remembrance' (saved in the inbound control RAM). TI remembrance is reset by the microcode.

Confirmation of Clear (X.21): The 16-bit time confirmation of the X.21 steady states is performed in the LIC. The only X.21 steady state confirmed by the FESA is 'clear' when the protocol requires a 10 ms confirmation instead of the 16-bit time.

Modem-out: The modem-out pattern coming from the FES, is stored by the FESA in the outbound control RAM. The FESA also controls the integrity of the modem-out patterns up to the LICs output (LIC driver check).

Serial Link (SL)

All information between the LIC board and the scanner unit is exchanged via the TSS serial link in two modes:

- Inbound mode from DMUX/SMUX to FESA.

All LIC information is stacked in FESA RAM and is available for the FES synchronously or asynchronously.

- The LICs give the data received from transmission lines to the FESA.
- The FESA reads the registers from the MUXs or LICs.

- Outbound mode from FESA to DMUX/SMUX.

- The FESA gives to the LICs the data to transmit.
- The FESA writes into the MUXs or LICs registers.

Connection to LIC Type 5 and LIC Type 6

Information exchange between the scanner and LIC type 5 and LIC type 6 DCEs is performed via a serial link, which consists in:

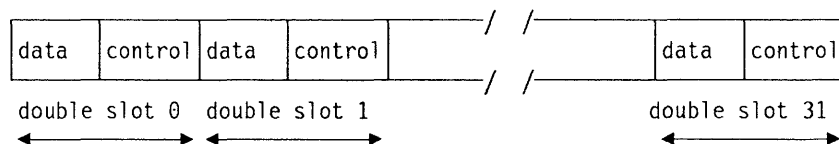
Inbound link From LIC to scanner

Outbound link From scanner to LIC.

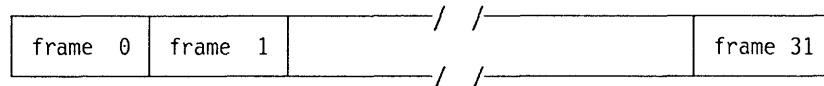
This information is carried in a frame structure.

Frames

A frame is a sequence of 32 double slots (data + control).



A superframe is defined as a sequence of 32 frames. A corresponding delimiter is put in control slots of frame 31, to signal the end of a superframe.



Slots

A double slot is made of:

- A data slot
- A control slot.

A slot is an eight-bit element of information.

Data Slots

Data exchange between the scanner and the DCE is performed on a request/answer basis, in order to enslave the serial link data speed to the DCE transmit and receive clocks.

The transmit and data slots carried by the serial outbound and inbound links, contain bursts of data or are empty.

Up to five data bits can be sent or received in a data burst.

A data delimiter indicates the actual length of a data burst.

An empty data slot is ignored by the LIC and RTS remains at the previous state.

Control Slots

Control slots are used by the SMUX or DTE (LIC) registers, according to the frame number: inside a superframe, control slots of all even frames are dedicated to the V.24 registers.

Notes:

1. One double slot is used for DCEs working at speeds less than 20 kbps.
2. Four double slots are needed for DCEs working at 56 kbps.
3. A maximum of four DCEs working at 56 kbps can be attached to a same scanner.
4. When an even (resp. odd) DCE cassette address is used by a 56 kbps DCE, the odd (resp. even) corresponding address must be left free.

Double Multiplexer Card (DMUX)

For LIC types 1 to 4 (DTE function only).

DMUX Functions

The two MUXs (on the DMUX card) convert the serial link bit stream coming from the FES into the LICs bit stream.

On the serial link side the DMUX:

- Monitors the frames coming from the FESA.
- Retrieves and decodes the serial link bit stream encoded information (code Manchester).
- Detects the frame sync and transmits it to the LICs.
- Copies in the proper register the incoming information addressed to the DMUX.

On the LIC bus side the DMUX:

- Monitors the serial information coming from the LICs.
- Transmits it to the FESA via the serial link after Manchester encoding.
- Sends control data stored in DMUX registers to FESA.

In addition the DMUX provides:

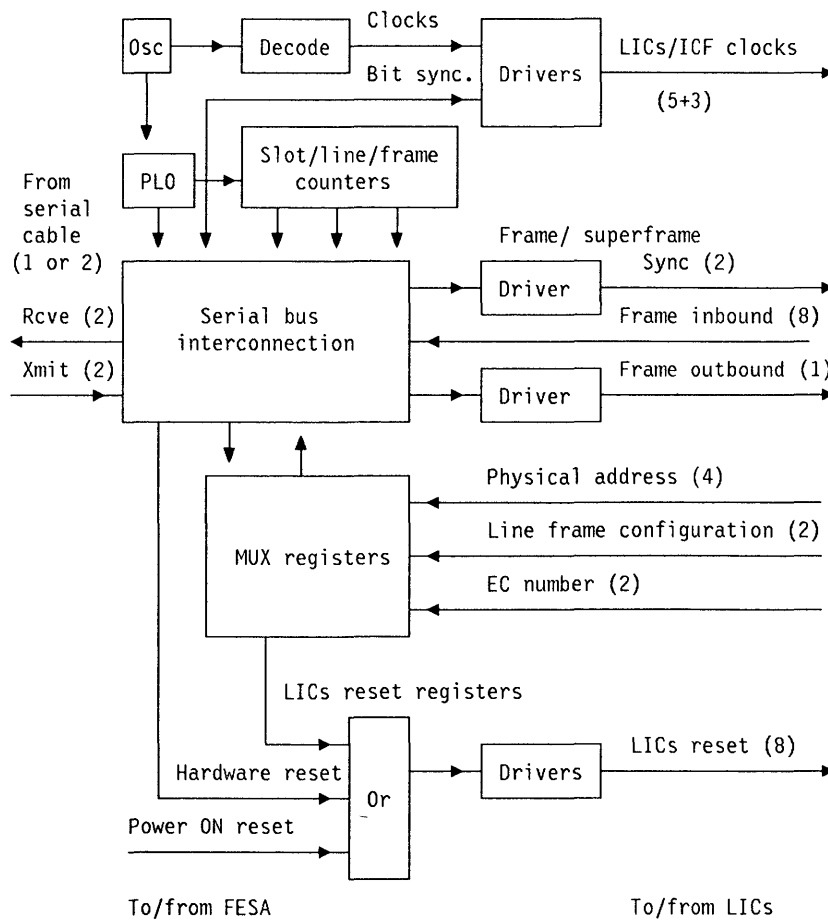
- A bit timing synchronized from the received data (PLO function)

- Three clocks for LIC internal clock function (ICF)
- Three functional clocks for LICs synchronized on the outbound data flow
- Two clocks for clock failure detection function assumed by the LIC
- Eight LIC reset commands (to isolate any LIC from the inbound data flow)
- DMUX physical address, machine frame configuration, and DMUX_EC number information to the FESA
- Error detection
- Diagnostic facilities.

MUX 1 or 2 Data Flow

There are two multiplexors (MUX) within a DMUX card. Each MUX attaches to one serial link.

The data flow of the two MUXs is identical and is as follow:



Note: Numbers in parentheses are the number of leads.

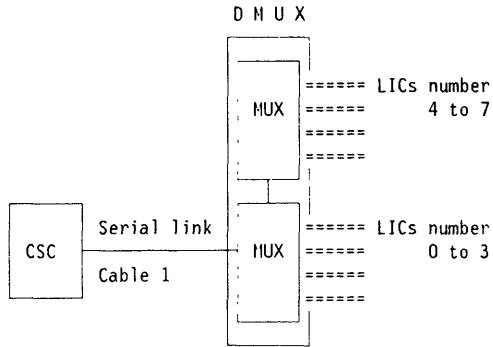
DMUX Functional Description

Only one or both of the two MUXs of the DMUX card can be used depending on connecting to one or two scanners.

Connection to one scanner

In this 'MUX extended configuration', up to 8 LICs (physical address 0 to 7) are connected to the scanner.

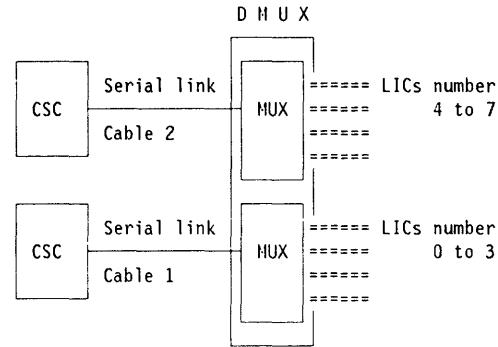
The 'Cable 2 Present' bit is set OFF in the DMUX card



Connection to two scanners

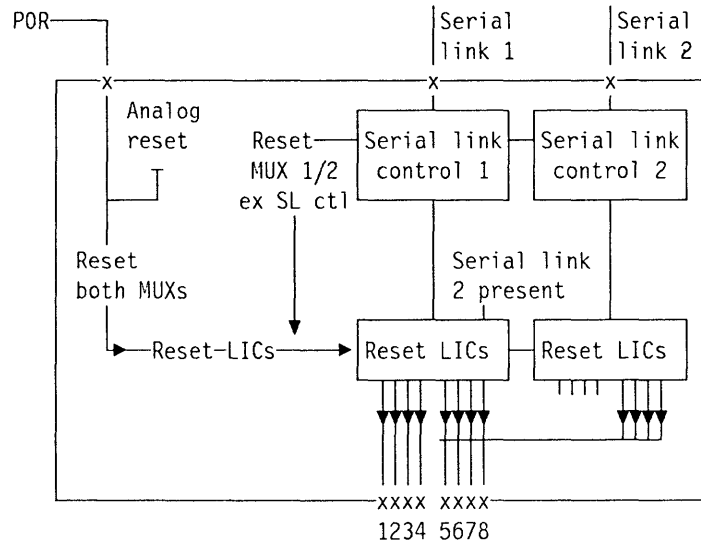
In this 'Not extended configuration', up to 4 LICs (physical addresses 0 to 3, or 4 to 7) are connected to each scanner.

The 'Cable 2 Present' bit is set ON in the DMUX card



DMUX Reset

The DMUX card and, consequently, the two MUXs can be reset:



1. A POR line coming from the power supply (one line for two DMUX cards). In that case a MUX reset is done and a reset LIC is sent to each associated LIC.
2. The DMUX card being **hot pluggable**, an analog reset circuit allows to perform the reset as for a POR line.
3. If there is a detection of 'no transmission' on the serial link, the MUX itself generates a reset MUX, except on the serial link control part and generates a reset on the associated LICs (extend mode or not.)

LIC Reset

LIC reset is done either by the selective reset LIC line coming from the MUX or by an analog reset circuit on the LIC itself in case of hot plugging.

A selective reset can be done by the microcode through the serial link by selecting the appropriate bit in the LIC reset register of the MUX.

The reset allows to isolate the LIC from the MUX (via the LIC bus), and from the attached lines.

DMUX Hot Plugging

Bottom connectors with several level of indentations and an analogic power ON reset delay provide the required power sequences.

Single Multiplexer Card (SMUXA/B)

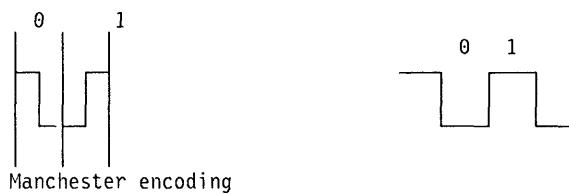
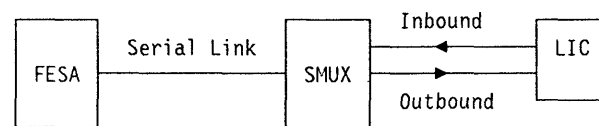
For LIC types 5 and 6 (DTE plus DCE functions):

- The SMUXA is associated to the lower board.
- The SMUXB is associated to the upper board.

SMUXA and SMUXB are slightly different in packaging (cable connector), but are functionally identical; therefore, SMUXA or SMUXB will be referred to as SMUX cards.

SMUX Functions

The SMUX cards convert the serial Manchester-encoded bit stream into the LIC serial outbound bit stream and, conversely, the serial inbound bit stream from the LICs into serial Manchester-encoded bit stream for the FES.



On the serial link side:

- Monitors the frames coming from the FESA.
- Retrieves and decodes the Manchester-encoded information.
- Detects the frame synchronization pattern and transmits sync pulses to the LICs.
- Loads the information devoted to the SMUX into the proper register.

On the LIC bus side:

- Monitors the serial information coming from the LICs.
- Transmits it to the FESA after Manchester-encoding.
- Sends the control information from the SMUX registers to the FESA.

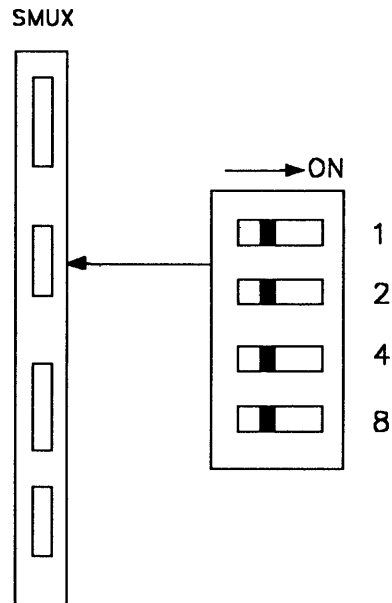
In addition the SMUX provides:

- A bit timing synchronized from the received data (PLO function)
- Two functional clock signals to the LICs (synchronized from the outbound data flow)
- Eight LIC reset commands (to isolate any LIC from the inbound data flow)
- SMUX physical address, machine frame configuration, SMUX EC number and 'LIC5/6 present' indication
- Error detection
- Diagnostic facilities
- 1 MHz clock signal to the LICs for PKD operation
- Four binary coded bits to LIC type 5 for transmit level setting (see transmit level hereafter).

Transmit Level

The transmit level is country-dependent.

The correct transmit level for a given country must be set at installation time by the CE each SMUX card by means of four switches (0 to -15 dBm).



At IML, those switch values are read into each corresponding LIC type 5 non-volatile RAM. However, if one of these transmit levels has to be slightly modified in the field (for example to compensate for line impairments), it can be modified from the PKD by the CE.

Card Replacement

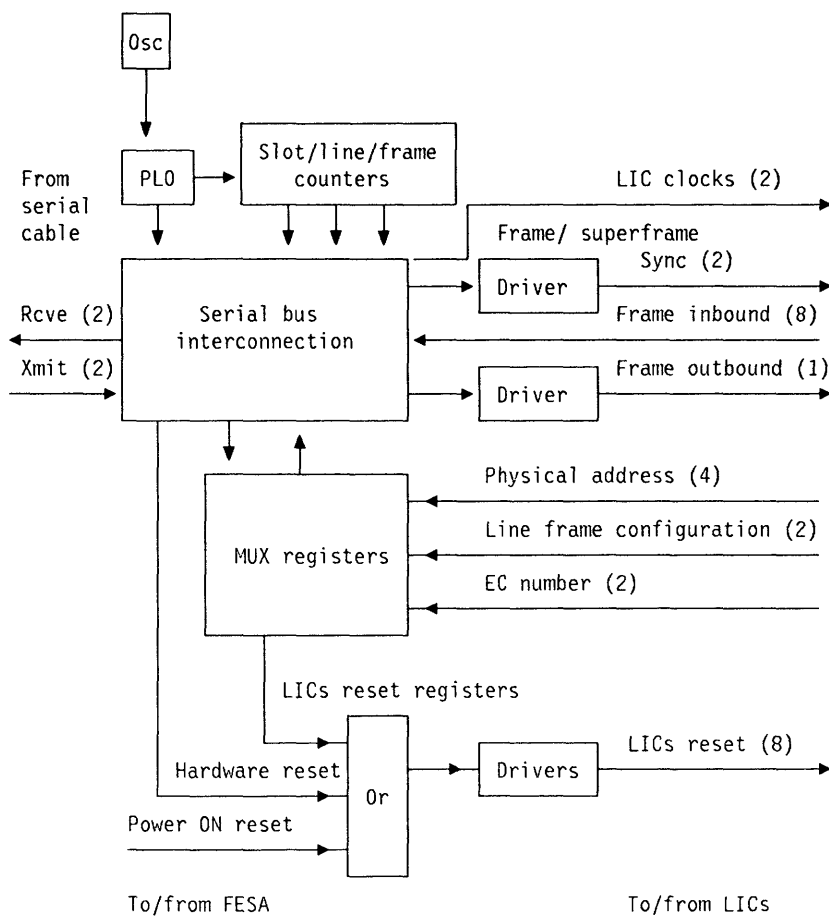
In case of SMUX replacement, carefully note down the previous SMUX switch settings or use the following table to determine the maximum authorized transmit level in your country.

| Country (non-switched lines) | Transmit level |
|------------------------------|----------------|
| AG and A/PG (generally) | 0 |
| Australia | -13 |
| Canada | 0 |
| Chile | -6 |
| Denmark | -10 |
| EMEA (generally) | -6 |
| Finland | -10 |
| France | -15 |

| Country (non-switched lines) | Transmit level |
|------------------------------|----------------|
| Greece | 0 |
| Hong-Kong | - 9 |
| Iceland | -10 |
| Ireland | 0 |
| Italy | -10 |
| Japan | -15 |
| Sweden | -10 |
| UK | -13 |

SMUX Data Flow

The data flow of the SMUX A/B is as follows:



Note: Numbers in parentheses are the number of leads.

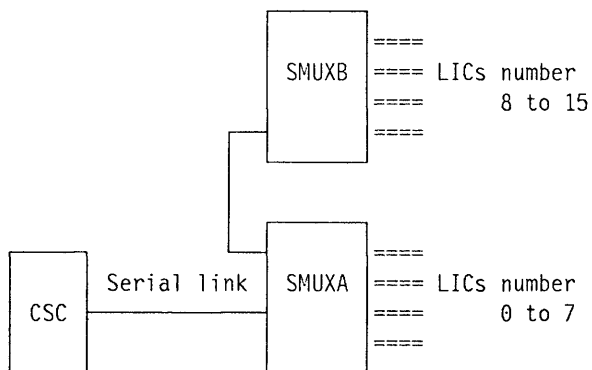
SMUX Functional Description

Although SMUXB might not be used, SMUXA and SMUXB are permanently installed on both LIB2s.

If a serial link cable is connected to a SMUXB, it works exactly as a SMUXA.

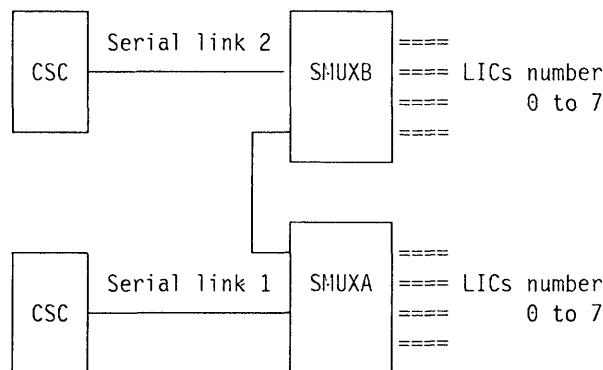
Connection to one scanner

Up to 16 LICs (addresses 0 to 15) are connected to the scanner



Connection to two scanners

Up to 8 LICs (addresses 0 to 7) are connected to each scanner



SMUX Reset

SMUX A and B cards can be reset by either of the following ways:

- By the POR line coming from the power supply. The POR line acts on both SMUX A and B cards. Both SMUX A and B are reset and send a 'LIC reset' to each associated LICs.
- By an 'analog reset' when a SMUX card is hot-plugged.
- When absence of signal is detected on the outbound serial link.

LIC Reset

LIC reset is done either by the 'selective reset line' coming from the SMUX or by an analog reset circuit when the LIC is hot-plugged.

Selective reset can be done:

- Either by microcode through the serial link
- Or by selecting the appropriate bit in the LIC registers of the SMUX.

SMUX Hot Plugging

Bottom connectors with several levels of indentations and an analogic power ON reset delay provide the required power sequences.

LIC Types 1 to 4 Cards

The LIC types 1 to 4 provide DTE function only. They connect the DMUX card to various types of DCEs or direct-attached DTEs.

There are four types of LICs according to the CCITT interfaces.

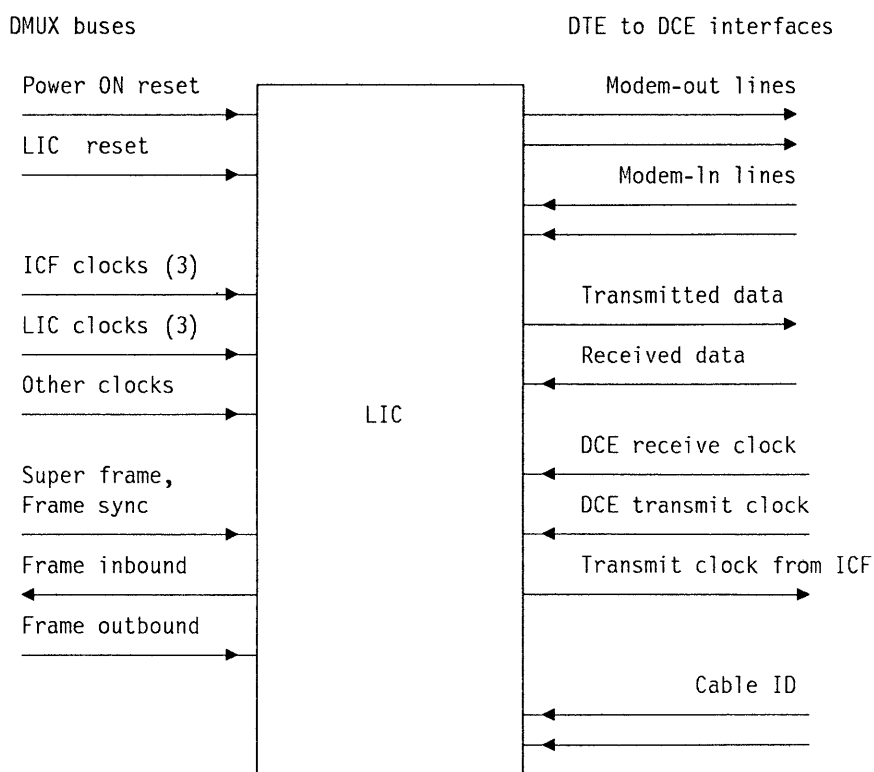
LIC1s to LIC4s to DMUX interconnection is identical (the number and meaning of bits may however differ according to the type of DCE attachment).

Some LICs require internally generated clock signals for either:

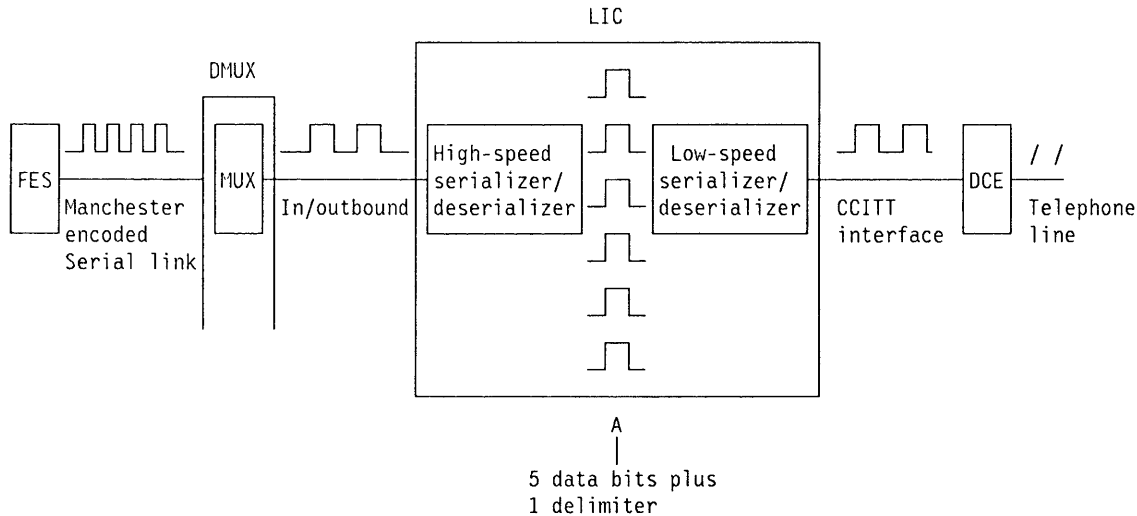
- Low-speed DCE attachment
- Direct attachment to terminals.

The internal clock function (ICF) on the LIC card itself, provides these clock facilities.

Interface Lines



Transmit/Receive Data Mechanism



The data is passed from/to the FES to the telecommunication line via the MUX and LIC as shown above.

The LIC communicates with the FES to:

- Request new data to be transmitted (when in transmit mode)
- Signal 'transmit overrun/underrun': 'LIC line error register bit 3' (when in transmit mode)
- Signal 'overrun': 'LIC line error register bit 2' if more than 5 data bits are received between two serial link requests (when in receive mode).

LIC Reset

See also "DMUX Reset" on page 4-37.

The purpose of the LIC reset command is to isolate the LIC from the LIC bus and from the attached lines (DMUX card provides one reset lead per LIC).

- At power ON, all leads are activated during the power ON reset, until the DMUX detects a start pattern from the FESA.
- After power ON, one reset lead may be activated on request, to reset the logic in the corresponding LIC and to disable all the line interface drivers.
 - In the reset state, no information can be exchanged with this LIC.
 - Any command to a LIC in reset state ends with a LIC check at the FES-FESA interconnection.

Line Enable/Disable

When a line is enabled, it accepts read/write operations as well as data transmission/reception and DCE interface handling.

After a LIC reset, all lines are automatically disabled and do not handle any more data transmission/reception, nor DCE interface handling.

- On one-line LICs, when the line is disabled (but not in the reset state), it can be written **and** read.
- On four-line LICs:

- When the four lines are disabled (but not in the reset state), it can be written **but cannot be read**.
- When at least one line is enabled, it can be written **and** read.

Each LIC (not under reset state) monitors the incoming and outgoing frames to receive and send register information belonging to its lines. This allows the lines, even disabled, to receive commands from the microcode and the FES, and to pass status information to the scanner.

These facilities allow the FESA to:

- Handle the line enabled/disabled bits to generate the LIC present pattern
- Modify the FES scanning and dynamically adapt the FES resources to the line configuration changes, without manual intervention.

For example, assuming a LIC plugged in physical position 0 on the LIC board:

- If this LIC receives logical address 7, it occupies the slots assigned to LIC number 7 and is seen as LIC in physical position 7 by the FESA and FES.
- If this LIC has no line enabled, it will not be scanned.
- See "LIC Enabled Leads" on page 4-31 for the microcode handling of these leads.

Selective Scanning

Selective scanning gives more flexibility for backup configurations using the same scanner, as only the LICs which have at least one line enabled, are scanned.

As a result, the total weight of the LICs which can be installed or connected physically to one scanner may be more than the supported weight of the scanner (100), as long as the total weight of the lines enabled at any time, does not exceed the scanner's supported weight.

Selective scanning enables the customer to install on the same scanner, LICs which are enabled only for one configuration at one time, and LICs which will be enabled only for a second configuration later (the first configuration having to be disabled first).

Selective scanning is managed by the CSP microcode.

Notes:

1. When modifying a configuration containing one or several LIC4s, the scanner must be re-IMLed.
2. No checking is made to verify that a scanner is overloaded.

LIC Logical Addressing Function

LIC logical function allows selective scanning.

In the example of configuration changes hereafter:

- The logical address function allows multi-configuration changes without card plugging or unplugging.

| LIC board | | | | | | | | |
|--------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Physical addresses | | | | | | | | |
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| DMUX Card | LIC A | LIC B | LIC C | LIC D | LIC E | LIC F | LIC G | LIC H |
| | 9.6 | 256 | 1.2 | 1.2 | 1.2 | 64 | 64 | 9.6 |
| Line speeds (kbps) | | | | | | | | |

- The customer may define several configurations without any physical LIC changes. For example:

| | | | | |
|--------------------|-----------|-------|-------|--|
| Physical addresses | 0 | 2 | 7 | |
| Configuration 1 | DMUX card | LIC A | LIC C | LIC H |
| | | | | 8 lines at 9.6 kbps 4 lines at 1.2 kbps |

| | | | | | | |
|--------------------|------|-----|-----|-----|-----|----------------------|
| Physical addresses | 2 | 3 | 4 | 7 | | |
| Configuration | DMUX | LIC | LIC | LIC | LIC | 12 lines at 1.2 kbps |
| 2 | card | C | D | E | H | 4 lines at 9.6 kbps |

| | | | | | | |
|--------------------|-----------|-------|-------|-------|-------|---|
| Physical addresses | 0 | 2 | 3 | 6 | 7 | |
| Configuration 3 | DMUX card | LIC A | LIC C | LIC D | LIC G | LIC H |
| | | | | | | 1 line at 64 kbps 8 lines at 9.6 kbps 8 lines at 1.2 kbps |

| | | |
|--------------------|-----------|--------------------|
| Physical addresses | 1 | |
| Configuration 4 | DMUX card | LIC B |
| | | 1 line at 256 kbps |

LIC Swap

The logical addressing function implemented in the 3745 LICs, allows LIC address swap.

Supposing two LICs, one plugged at physical address A (LICA) and the other one plugged at physical address H (LICH).

The logical addressing function allows to 'swap' the logical addresses between LICA and LICH. For example, assign logical address A to LICH, and logical address H to LICA.

Before the swap

| | | | | | | | | | |
|--------------------|--------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Physical addresses | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | |
| | DMUX card | LIC A | LIC B | LIC C | LIC D | LIC E | LIC F | LIC G | LIC H |
| Logical addresses | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | |

After the swap

| | | | | | | | | | |
|--------------------|--------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Physical addresses | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | |
| | DMUX card | LIC A | LIC B | LIC C | LIC D | LIC E | LIC F | LIC G | LIC H |
| Logical addresses | '7' | 1 | 2 | 3 | 4 | 5 | 6 | '0' | |

After the swap, on the serial link, LICA takes the slots of LICH and LICH takes the slots of LICA.

LIC Address Register Contents

| Write mode | | Read mode | |
|------------|----------------------------|-----------|-------------------------|
| Bits | Meaning | Bits | Meaning |
| 0 | LIC logical address bit 0 | 0 | LIC wired address bit 0 |
| 1 | LIC logical address bit 1 | 1 | LIC wired address bit 1 |
| 2 | LIC logical address bit 2 | 2 | LIC wired address bit 2 |
| 3 | Enable/disable logical add | 3 | Not used |
| 4 | Not used | 4 | EC number |
| 5 | Not used | 5 | EC number |

LIC Control Register

The LIC control register X'02' bit 1 and bit 3 (Line enable E0 and E1) controls the swapping.

| Bits | Meaning |
|------|----------------------------|
| 0 | High-speed line |
| 1 | Line enable E0 |
| 2 | X.21 CCITT used by FESA 80 |
| 3 | Line enable E1 |
| 4 | Not used |
| 5 | Transmit bit echo |

Enable Clock Mode

Register X'03' bits 4 and 5 select the clock mode. They are OFF after a reset command (that is 00 = diag mode).

There is no clock until the enable clock mode bit is set, except if the LIC detects that the cable ID is a local attach cable.

After the reset the LIC forces the local attach clock mode: 11 (speed given by ICF after reset: 2400 bps).

Transmit Clock Gating by RFS (LICs 1, 2, and 3)

If LIC control register X'02' bit 2 is set for a given line, it allows gating the interface transmit clock by the modem-in lead RFS (despite the clock mode setting).

There is no clock failure reporting if the transmit clock on the interface is stopped because RFS is OFF.

LIC 4 Personalization

There is only one LIC type 4 part number. The LIC type 4A or 4B (personalization) is defined at IML by the microcode.

The LIC 4 'wideband bit', when set, specifies LIC 4A depending on the NCP speed parameter definition at set mode time.

LIC Wideband with Line Speed Higher than 128 kbps

The wideband LIC is scanned four times faster than the non-wideband LIC. The wideband LIC line takes four data slots in the frame.

- With a line speed less than 128 kbps, the four data slots dedicated to the LIC in a frame are sufficient for the four lines attached.
- With a line speed higher than 128 kbps, only one line may be attached to the scanner (the 'high-speed line' bit is set in the control register).

RTS Through DCE or Data Paths

According to the value of modem-out bit 5, the lead RTS of the DCE interface will change with the new modem-out register or at the boundary of transmit data burst as follows:

- RTS through the DCE path:

When modem-out bit 5 is ON, RTS changes according to the modem-out bit 1 sent to the LIC by the FESA in even frames. RTS change occurs as soon as the new modem-out is loaded.

- RTS through the data path:

When modem-out bit 5 is OFF, RTS changes according to the value of bit 0 of the transmit data burst. The RTS change occurs at the boundary of the transmit burst, that is, with the last data bit.

LIC Modem-In Process for Non-X.21 Lines

The LIC sends the modem-in information without any process to the FESA. The FESA then processes this information in order to raise an interrupt to the FES only with confirmed modem-in information.

For more information see "DCE Lead Management" on page 4-32 in the FESA section.

LIC Modem-In Process for X.21 Lines

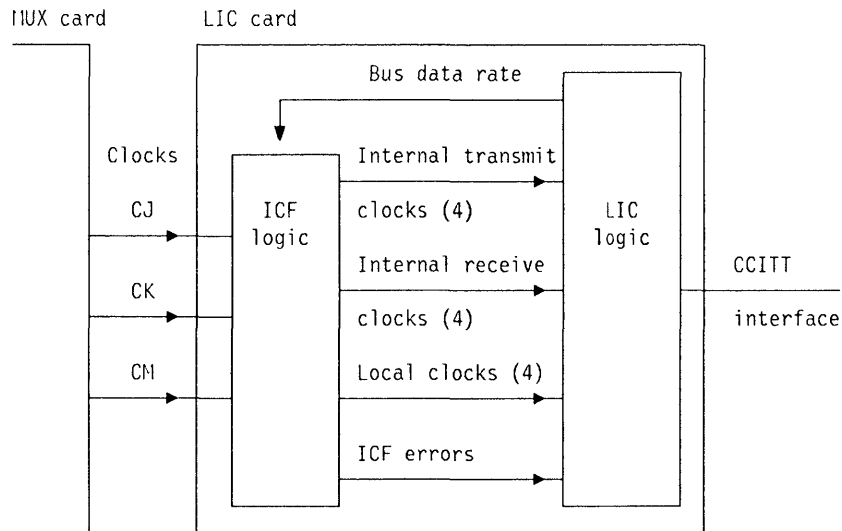
The LIC performs the confirmation of X.21 steady states by scanning a 16 bits time.

The LIC sends the modem-in information to the FESA and when the state is confirmed after 16-bits count, the 'bit state confirm' of X.21 modem-in register is raised.

An option is provided to the microcode (when register X'06' is ON) to perform a 10 ms confirmation instead of a 16-bits time. In that case, the LIC sends modem-in to the FESA and the FESA itself confirms the state for 'DCE clear' after a 10 ms count, state confirm still being delivered after a 16 bits time for the other three states.

Internal Clock Function (ICF)

ICF Data Flow



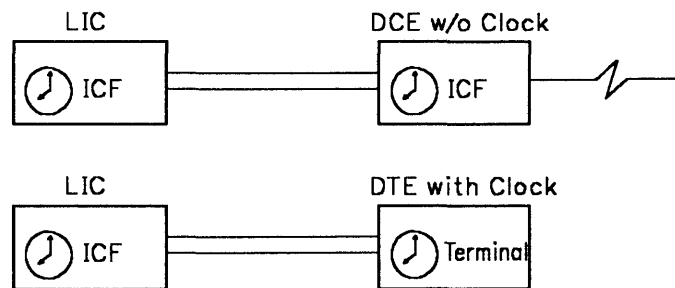
For each line, the transmission speed is selected at initialization by the micro-code (set mode depending on NCP generation). The internal clock function (ICF) provides the transmit and/or receive clocks to:

- The LICs and their low-speed non-clocked DCEs.
- The LICs only when their direct-attached terminals use their own clock.
- The LICs and their direct-attached unclocked terminals.

The ICF is not used when a LIC is attached to a clocked DCE.

Depending on the above configurations, the ICF mode can be 'Internal', '3745' or 'External', and the clockings are provided as follows.

Internal Mode



The internal clocking mode is set by the microcode at initialization time in the LIC card (ICF activated).

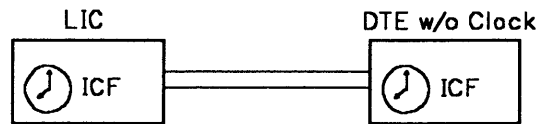
NCP parameters: clock = internal, speed = xxx.

The following data rates are available:

- Asynchronous lines (start-stop)
 - From 50 to 19 200 bps
 - 1200 bps transmit / 75 bps receive (for test purposes).

- Synchronous lines (BSC or SDLC)
 - From 50 to 4800 bps.

3745 Mode



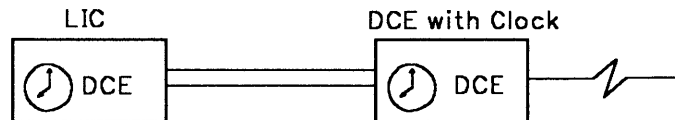
The 3745 clocking mode is set by the microcode at initialization time in the LIC card (ICF activated).

NCP parameters: = direct attach, speed = xxx.

The following data rates are available:

- Asynchronous lines (start-stop)
 - From 50 to 19 200 bps.
- Synchronous lines
 - Up to 245 760 bps for SDLC
 - Up to 55 845 bps for BSC

External Mode



The external clocking mode does not activate the ICF since the DCE provides the transmit and receive clocks to both the LIC and itself.

LIC Wraps

Refer to:

- "Problem Determination Aid for LIC Types 1 to 4" on page 4-92 for more information on wraps
- *Advanced Operations Guide*, SA33-0097, to invoke these function from the MOSS console
- *Diagnostic Descriptions*, SY33-2059, for diagnostics using LIC wraps.

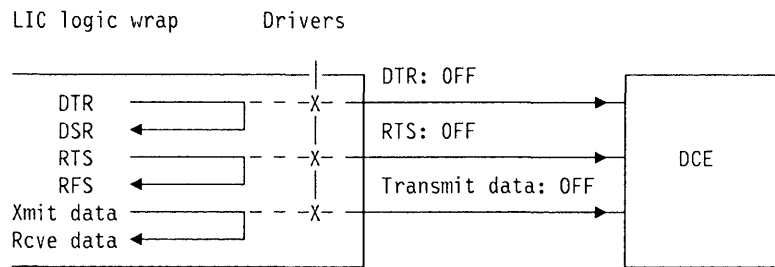
Two LIC wraps are available on the CCITT interface of the LICs:

- Loop 1 (line wrap)
- Loop 3 (loop back).

(LIC register X'2' bit 'Loop 1' or bit 'Loop 3').

Loop 1 on V.24

Loop 1 on the V.24 interface performs the following wraps:

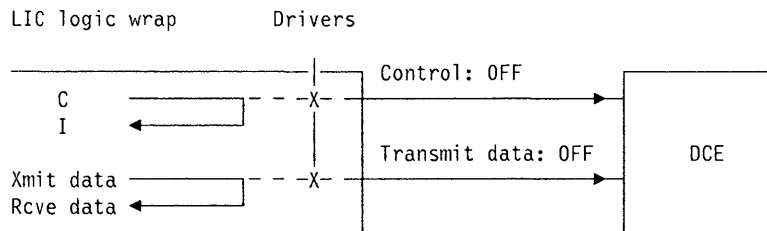


Loop 1 on V.25

For the V.25 autocall interface, transmit data line is replaced by digit present line inside LIC1 hardware and no transmit or receive clock is available.

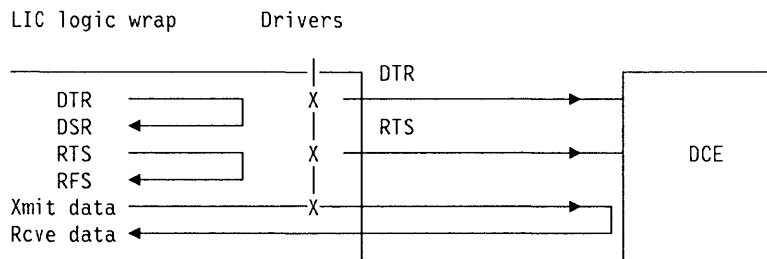
Loop 1 on X.21

Loop 1 on the X.21 interface performs the following wraps:



Loop 3 on V.24

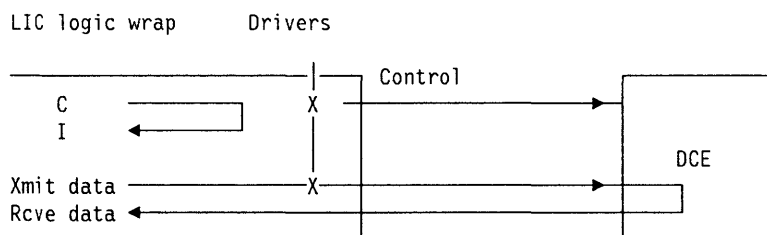
Loop 3 on the V.24 interface performs the following wraps:



Only DTR and RTS are wrapped to DSR and RFS before the drivers.

Loop 3 on X.21

Loop 3 on the X.21 interface performs the following wrap:



Hot Plugging of LICs

The bottom of the LIC card has three levels of indentation to provide the required power sequences.

When plugged power ON, the LIC logic gets into the reset state long enough to avoid transient disturbances on the interfaces.

LIC Types 5 and 6 DTE Function

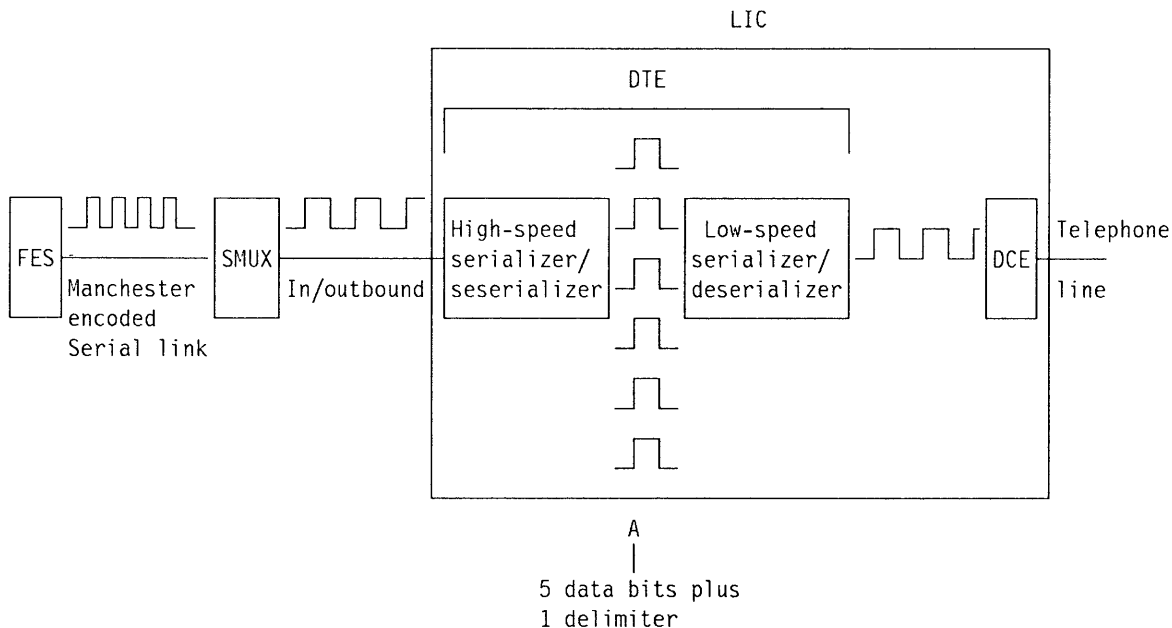
The LIC types 5 and 6 provide DTE and integrated DCE functions. They connect SMUX cards to telecommunication lines.

- LICs type 5 connect to normal quality or M.1020/1025 4-wire telecommunication lines
- LICs type 6 connect to DDS, local loops or unloaded baseband 4-wire lines in the US only.

Here follows information about the DTE part of LICs type 5 and LICs type 6 which is common to both LICs. Refer to the specific LICs type 5 or LICs type 6 section for DCE function.

Transmit/Receive Data Mechanism

LICs type 5 and LICs type 6 interconnection to SMUX cards is identical (the number and meaning of bits may however differ according to the type of line).



The data is passed from/to the FES to the telecommunication line via the MUX and LIC as shown above.

The LIC communicates with the FES to:

- Request new data to be transmitted (when in transmit mode)
- Signal 'transmit overrun': 'LIC line error register bit 3' (when in transmit mode)
- Signal 'transmit underrun': 'LIC line error register bit 3' (when in transmit mode)
- Signal 'overrun': 'LIC line error register bit 2' if more than 5 data bits are received between two serial link requests (when in receive mode).

LIC Reset

See “SMUX Reset” on page 4-42, and “LIC Reset” on page 4-44.

Line Enable/Disable

See “Line Enable/Disable” on page 4-44.

Selective Scanning

See “Selective Scanning” on page 4-45.

LIC Swap

See “LIC Swap” on page 4-46, keeping in mind that LICs type 5 have only four logical addresses per SMUX card.

LIC Address Register Contents

| Write mode | | Read mode | |
|------------|----------------------------|-----------|-------------------------|
| Bits | Meaning | Bits | Meaning |
| 0 | LIC logical address bit 0 | 0 | LIC wired address bit 0 |
| 1 | LIC logical address bit 1 | 1 | LIC wired address bit 1 |
| 2 | LIC logical address bit 2 | 2 | LIC wired address bit 2 |
| 3 | Enable/disable logical add | 3 | Odd position |
| 4 | Not used | 4 | EC number |
| 5 | Not used | 5 | EC number |

LIC Control Register

The LIC control register X'02' bit 1 and bit 3 (line enable E0 and E1) controls the swapping.

| Bits | Meaning |
|------|-------------------|
| 0 | Not used |
| 1 | Line enable E0 |
| 2 | Not used |
| 3 | Line enable E1 |
| 4 | Not used |
| 5 | Transmit bit echo |

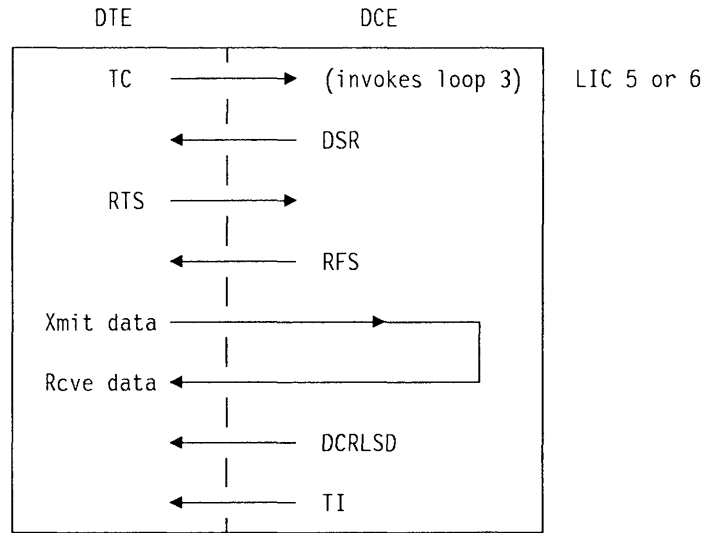
LIC Wraps

Refer to

- “Problem Determination Aid for LIC Types 1 to 4” on page 4-92 for more information on wraps
- *Advanced Operations Guide*, SA33-0097 to invoke these functions from the MOSS console.

Loop 3 on V.24

Loop 3 on the V.24 interface performs the following wraps:



Loop 3 is performed between the transmitter output and the receiver input (before the line transformers) in the DCE part of LIC type 5 and LIC type 6.

A 700 Ω load is maintained on the line during loop 3. Loop 3 is started by 'test control' (TC) rise. The DCE answers back by rising 'test indicator' (TI), then starts data looping.

LICs Hot Plugging

LIC card bottom connector have three levels of indentation to provide the required power sequences.

When plugged power ON, the LIC logic gets into the reset state for a time long enough to avoid transient disturbances on the interfaces.

LIC Type 5 DCE Function

Maintenance Approach

Four basic methods are used to identify network/link problems or DCE failures:

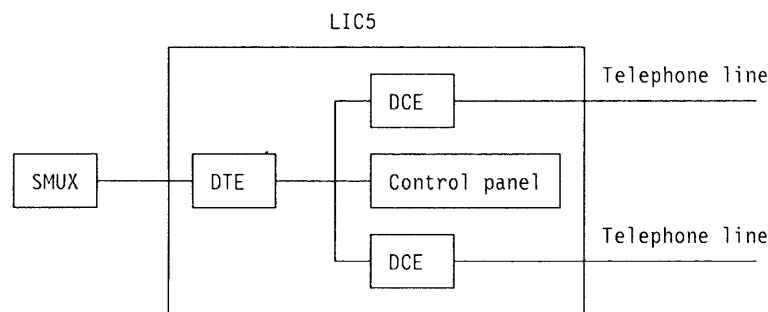
1. Link problem determination aid (LPDA-2) hardware function implemented in each LIC type 5 DCE.

LPDA-2 is used in conjunction with the NetView program and console at host location. LPDA-2 commands and report messages are given in *LPDA Description*, SY33-2064.

2. MOSS wrap tests.
3. Diagnostics invoked from the MOSS console.
4. Manual tests from:
 - LIC type 5 panel or
 - 5869 portable keypad display (PKD).

For details, see "Problem Determination Aid for LIC Type 5 and LIC Type 6" on page 4-95, and appropriate 786X and 5822 documentation listed in the MIP bibliography.

Data Flow



Logic Part

- DTE serializer/deserializer
- DCE microprocessor and signal processor
- DCE ROS, RAM, and NVROM.

Analog Part

- DCE coder/decoder
- DCE transmit/receive filters
- DCE line transformers.

Speeds

Each LIC type 5 houses two DCEs which can operate at: 4800 bps (2400 bps backup), or 9600 bps (7200 bps backup), or 14 400 bps (12 000 bps backup) over non-switched 4-wire telephone lines

In the event of severe degradation due to temporary line problems, the backup speed may be used.

In multipoint network, the backup inbound speed may be required for only one or several drops, while the other drops continue to operate at full speed.

Speed Setting

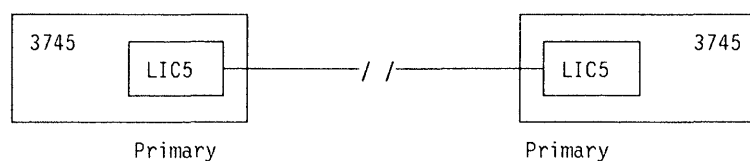
The speed is set at LIC installation from the PKD, and can be different for each DCE of a given LIC type 5

The speed setting cannot be done either by NetView or by MOSS.

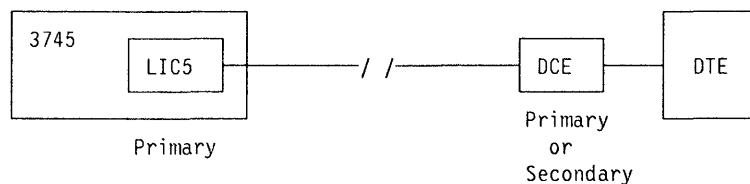
Configurations

LIC type 5 DCEs are compatible with IBM 586X and 786X DCEs. They operate in point-to-point or multipoint configurations as follows.

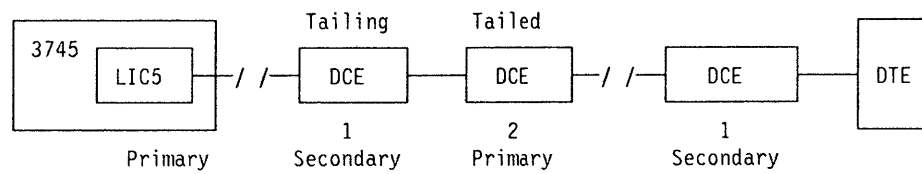
Point-to-Point - LIC Type 5 to LIC Type 5



Point-to-Point - LIC Type 5 to 586X or 786X

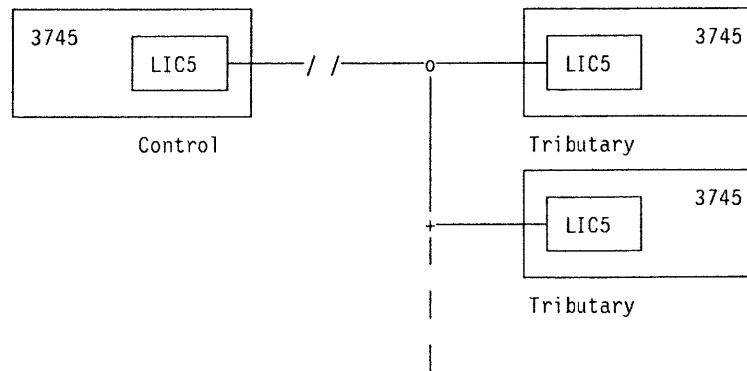


Point-to-Point - LIC Type 5 to Tailed 586X

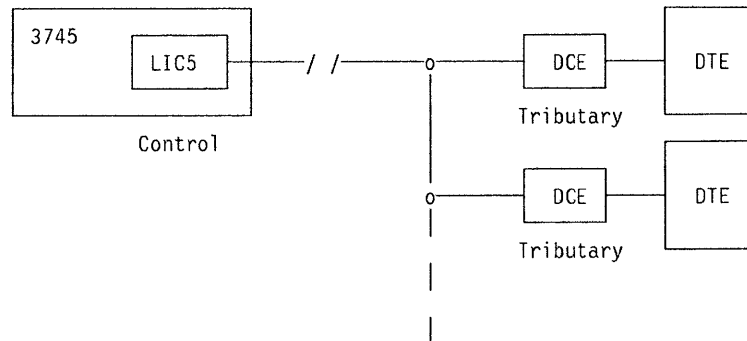


1: Transmit clock = received
 2: Transmit clock = external
 Speed control = DTE.

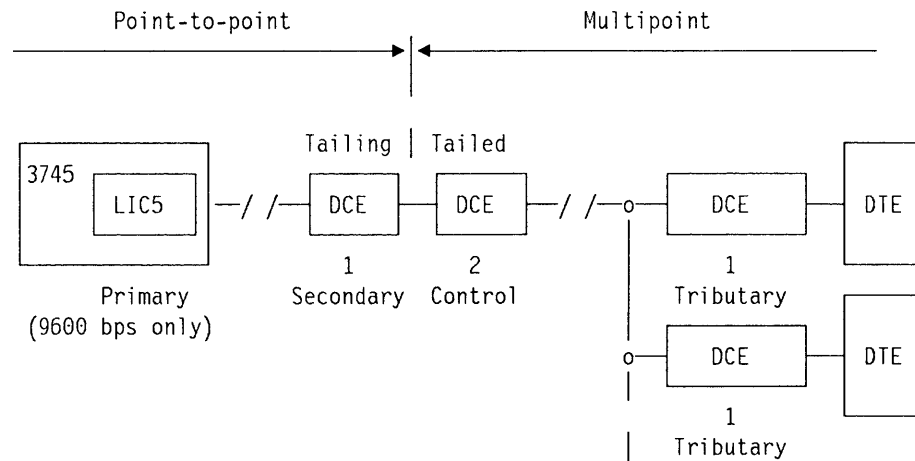
Multipoint - LIC Type 5 to LICs Type 5



Multipoint - LIC Type 5 to 586Xs



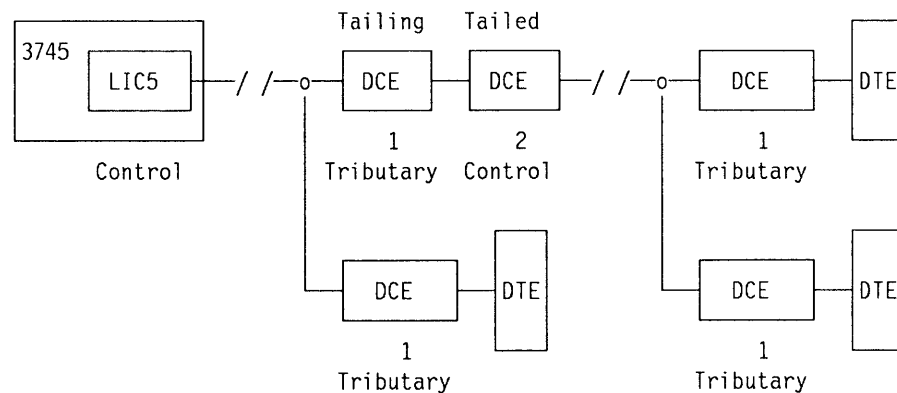
Multipoint - LIC Type 5 to One Tailed 586X



1: Transmit clock = received
 2: Transmit clock = external
 Speed control = DTE.

Multipoint - LIC Type 5 to 586Xs (Including Tailed)

This configuration does not support LPDA2.



1: Transmit clock = received
 2: Transmit clock = external
 Speed control = DTE.

Configuration Options

Depending on the 'IBM native' or CCITT type of modulation, the different ways of setting the various CNM functions are as follows:

| CNM functions | Modulation | | Settable by | | |
|------------------------|------------|-------|-------------|-----|------|
| | IBM native | CCITT | NetView | PKD | MOSS |
| Manual commands | Yes | Local | No | Yes | No |
| Local wrap (loop 3) | Yes | Yes | No | Yes | Yes |
| Remote wrap (loop 2) | Yes | Yes | No | Yes | No |
| Local self-test | Yes | Yes | Yes | Yes | Yes |
| LPDA-2 | Yes | Local | Yes | No | No |
| Sense/operate contacts | Remote | No | Yes | Yes | No |

Although LIC type 5 has no 'sense/operate' contact feature, it is possible to have these functions implemented in the remote 586X, and use them through a LIC type 5.

Data Encoding and Modulation

LICs type 5 use combined amplitude and bi-phase differential modulation encoding. Each couple (phase, amplitude) corresponds to a single bit pattern.

In addition, the data is scrambled/descrambled to avoid single frequencies over the telephone line when repetitive data patterns appear at the DCE interface.

Below are the:

- Modulation rate
- Carrier frequency
- Number of encoded bits per signaling period
- Modulation type.

For the A to E configurations shown in the following table:

| | A | B | C | D | E | F | G |
|---------------------|---|---|---|---|---|---|---|
| 14 400 bps | * | * | | | | | |
| 9600 bps | | | * | * | * | | |
| 4800 bps | | | | | | * | * |
| Native | * | | * | * | | * | |
| CCITT V.27 bis | | | | | | | * |
| CCITT V.33 | | * | | | | | |
| CCITT V.29 | | | | | * | | |
| Point-to-point | * | * | | * | * | * | * |
| Multipoint inbound | | | * | * | | * | * |
| Multipoint outbound | * | | | * | | * | * |

| A - Native Mode | | |
|---|-------------------|-------------------|
| Speed | 14 400 bps | 12 000 bps |
| Modulation Rate | 2400 | 2400 |
| Carrier Frequency | 1700 Hz | 1700 Hz |
| Number of encoded bits per signalling periods | 6 | 5 |
| Modulation | QAM trellis coded | QAM trellis coded |
| RTS/RFS Delay | 2 ms | 2 ms |

| B - CCITT Mode | | |
|---|------------|------------|
| Speed | 14 400 bps | 12 000 bps |
| Modulation Rate | 2400 | 2400 |
| Carrier Frequency | 1800 Hz | 1800 Hz |
| Number of encoded bits per signalling periods | 6 | 5 |
| Modulation | QAM V.33 | QAM V.33 |
| RTS/RFS Delay | 2 ms | 2 ms |

| C and D - Native Mode | | |
|---|----------------------|----------------------|
| Speed | 9600 bps | 7200 bps |
| Modulation Rate | 2400 | 2400 |
| Carrier Frequency | 1700 Hz | 1700 Hz |
| Number of encoded bits per signalling periods | 4 | 3 |
| Modulation | QAM, or QAM with TCM | QAM, or QAM with TCM |
| RTS/RFS Delay | 2 ms | 2 ms |

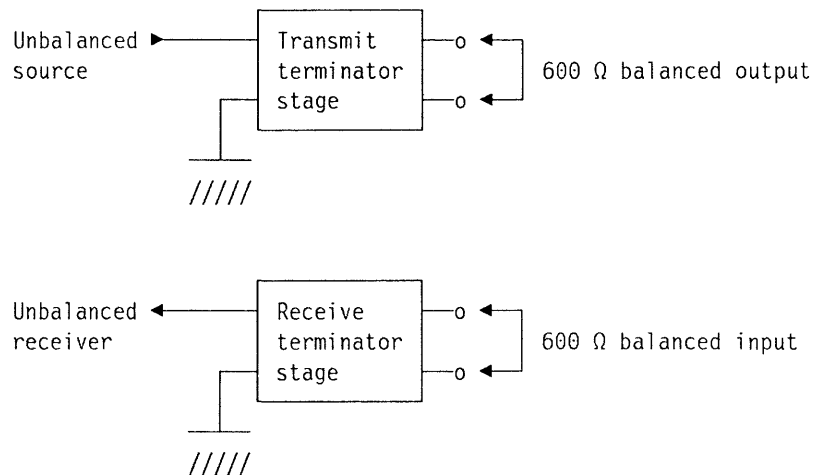
| E - CCITT Mode | | | |
|---|----------|----------|----------|
| Speed | 9600 bps | 7200 bps | 4800 bps |
| Modulation Rate | 2400 | 2400 | 2400 |
| Carrier Frequency | 1700 Hz | 1700 Hz | 1700 Hz |
| Number of encoded bits per signalling periods | 4 | 3 | 2 |
| Modulation | QAM V.29 | QAM V.29 | QAM V.29 |
| RTS/RFS Delay | 2 ms | 2 ms | 2 ms |

| F - Native Mode | | |
|---|-------------------------------|-------------------------------|
| Speed | 4800 bps | 2400 bps |
| Modulation Rate | 2400 | 2400 |
| Carrier Frequency | 1700 Hz | 1700 Hz |
| Number of encoded bits per signalling periods | 2 | 1 |
| Modulation | 4-phase differential encoding | 4-phase differential encoding |
| RTS/RFS Delay | 2 ms | 2 ms |

| G - CCITT Mode | | |
|---|-------------------------------|-------------------------------|
| Speed | 4800 bps | 2400 bps |
| Modulation Rate | 1600 | 1200 |
| Carrier Frequency | 1800 Hz | 1800 Hz |
| Number of encoded bits per signalling periods | 3 | 2 |
| Modulation | 8-phase differential encoding | 8-phase differential encoding |
| RTS/RFS Delay | 2 ms | 2 ms |

DCE to Telephone Line Interface

LIC type 5 interfaces the telephone line through balanced impedances matching the networks (both input and output circuitries may be regarded as 2-port networks).



The circuits are not damaged:

- Under open circuit condition
- By a short circuit between the leads
- By a short circuit from either lead to ground.

The DC isolation between input and output leads with regard to ground is greater than 20 M Ω .

Surge Protection

1. **Primary protection:** a telephone line surge protection (carbon block or gas tube) should also be provided by the line connector before the DCE wall plug
2. **Secondary protection:** three protection devices connected from tip to frame ground, from ring to frame ground, and tip to ring.

In the countries where it is authorized, this limits the maximum voltage to 80 V peak (line to ground) or 80 volts peak (line to line). In addition, the transformer saturation characteristics, and the Zener diode network across the line transformer secondary windings, limit the maximum peak voltage to 12 V (line to ground).

Transit Time

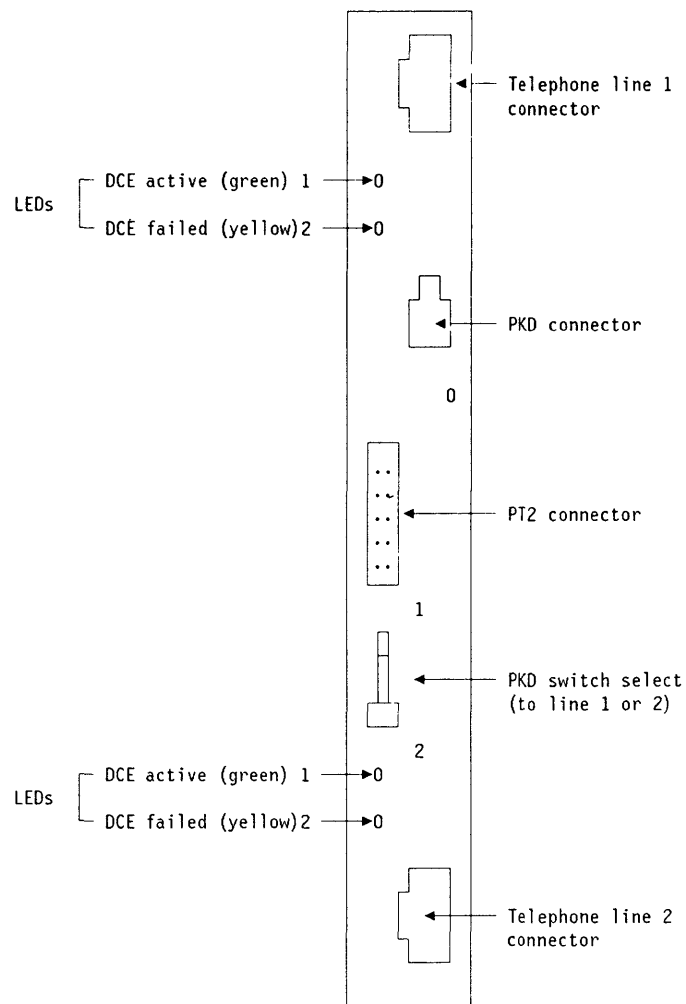
The transit time is the time that elapses between the input of a bit in the local transmitter and the output of this bit from the remote receiver, assuming a zero transmission delay over the telephone line.

| Modulation type | Transit time (ms) | | | | | |
|-----------------|-------------------|--------|------|------|------|------|
| | 14 400 | 12 400 | 9600 | 7200 | 4800 | 2400 |
| IBM Native | 21.4 | 21.4 | 17.2 | 18.0 | | |
| CCITT V.33 | 21.4 | 21.4 | | | | |
| IBM Native | | | 18.0 | 18.0 | | |
| CCITT V.29 | | | 16.8 | 16.8 | 16.8 | |
| IBM Native | | | | | 17.4 | 21.4 |
| CCITT V.27 bis | | | | | 12.2 | 15.6 |

RFS Delay

The RFS delay is 2 ms for LICs type 5 in any configuration. It must be added to the transit time to evaluate the turnaround time.

LIC Type 5 Panel



1 lit DTR is ON (green LED)
2 lit Severe local DCE error is detected (yellow LED)
1 and 2 flashing LIC card plugged in a wrong place

Line Specifications

- 4-wire non-switched lines
- US and Canada: non-conditioned
- Other countries: CCITT M.1020 or M.1025 conditioning.

Line Spectrum

- V.27 bis
 - Centered on 1800 Hz
 - Spreads from 1000 to 2600 Hz.
- Native and V.29
 - Centered on 1700 Hz
 - Spreads from 450 to 3050 Hz, including a 12.5 % roll-off.

- V.33
 - Centered on 1800 Hz
 - Spreads from 600 to 3000 Hz.

3002 Channel (US) Characteristics

| | |
|-----------------------------------|--|
| Attenuation distortion | (Overall loss relative to that at 1004 Hz) -2 to + 8 dB from 500 to 2500 Hz -3 to +12 dB from 300 to 3000 Hz |
| Delay distortion | Less than 1750 μ s from 800 to 2600 Hz |
| Insertion loss at 1004 Hz | 16 dB |
| Non-linear distortion (H2) | 25 dB minimum |
| Non-linear distortion (H3) | 30 dB minimum |
| Phase jitter | No more than 10° peak-to-peak |
| Frequency shift | \pm 5 Hz |
| Signal to noise ratio | 24 dB |
| Impulse noise | Threshold of -6 dB to signal level at an average rate of 15 impulses per 15 mn. |

M.1020 Line Characteristics

| | |
|---------------------------------|--|
| Attenuation distortion | (Overall loss relative to that at 800 Hz): -2 to +6 dB from 300 to 500 Hz -1 to +3 dB from 500 to 2800 Hz -2 to +6 dB from 2800 to 3000 Hz |
| Delay distortion | (Group delay relative to the minimum group delay): Less than 500 μ s from 1000 to 2600 Hz Less than 1500 μ s from 600 to 2600 Hz Less than 3000 μ s from 500 to 2800 Hz |
| Insertion loss at 800 Hz | 13 dB \pm 4 |
| Harmonic distortion | 25 dB minimum (below received level) |
| Phase jitter | No more than 15° peak-to-peak (normally 10°.) |
| Frequency shift | \pm 5 Hz |
| Signal to noise ratio | 24 dB |
| Impulse noise | Threshold of -8 dB to signal level, at an average rate of 18 impulses per 15 mn. |

M.1025 Line Characteristics

| | |
|---------------------------------|--|
| Attenuation distortion | (Overall loss relative to that at 800 Hz): -2 to +12 dB from 300 to 500 Hz -2 to + 8 dB from 500 to 2500 Hz -2 to +12 dB from 2500 to 3000 Hz |
| Delay distortion | (Group delay relative to the minimum group delay): Less than 300 μ s from 600 to 2800 Hz Less than 1500 μ s from 1000 to 2600 Hz |
| Frequency error | Less than \pm 5 Hz |
| Insertion loss at 800 Hz | 13 dB \pm 4 |
| Harmonic distortion | 25 dB minimum (below received level) |
| Phase jitter | No more than 15° peak-to-peak (normally 10°) |
| Frequency shift | \pm 5 Hz |
| Signal to noise ratio | 24 dB |
| Impulse noise | Threshold of -8 dB to signal level at an average rate of 18 impulses per 15 mn. |

Specific Country Line Characteristics

In the following countries, the line characteristics are specified by the PTT:

- **France**

The French PTT offer a 4-wire normal quality line with the following specifications:

| | |
|-------------------------------|---|
| Attenuation distortion | (Overall loss relative to that at 800 Hz): -2.6 to +4.5 dB from 500 to 2000 Hz -2.6 to +6.0 dB from 300 to 2600 Hz -3 to +9 dB from 1700 to 2300 Hz -3 to +12 dB from 2300 to 2800 Hz Loss at 800 Hz: 6.4 dB, with a possible variation of less than 4.5 dB. |
| Delay distortion | (Group delay relative to the minimum group delay): Less than 1000 μ s from 1000 to 2400 Hz Less than 1500 μ s from 800 to 2600 Hz The DC loop resistance of a wholly metallic line is less than 4000 Ω . |

- **Japan**

The NTT offer a normal quality line (3.4 kHz service). According to NTT-supplied information, these lines should have the following specifications:

| | |
|-------------------------------|--|
| Attenuation distortion | (Overall loss relative to that at 800 Hz over carrier section): -3.8 to +13.0 dB from 300 to 400 Hz -3.8 to +5.8 dB from 400 to 600 Hz -3.8 to +3.8 dB from 600 to 2400 Hz -3.8 to +9.4 dB from 2400 to 3000 Hz -3.8 to +17.4 dB from 3000 to 3400 Hz |
| Delay distortion | (Group delay relative to the minimum group delay): Less than 1750 μ s from 1000 to 3000 Hz |

- **UK**

The Post Office provides a quality telephone line according to CCITT recommendation M.1025.

Options and Configurations

The options are entered from the PKD, using the 'CONF' command or via LPDA-2 commands. They are stored into a non-volatile RAM except for micro-code and EC levels.

These options are:

- Read and set by the customer
- Read and set by the CE only
- Read-only.

They can be read and set:

- Through the PKD
- Through the LPDA-2 commands

- In the local LIC type 5 DCE
- In the remote DCE (LIC type 5 or IBM 586X DCE).

The table below shows the various ways of reading and setting these options.

Keying 'LOCAL CONFIGURATION' will cause the DCE to display and scroll field by field its own configuration; the operator may update each configuration field which appears on the display.

If the operator does not update the configuration, TI is **not** raised and data traffic can take place without interruption.

If the operator updates the configuration, (keying 'ERASE'), TI is raised, CD and RFS are dropped at local interface, and the **data traffic through the DCE is interrupted**.

Keying 'REMOTE CONFIGURATION' causes the DCE to display and scroll the configuration of the selected remote DCE.

During the operation, TI is raised, CD and RFS are dropped at the local and the remote interface, and the DATA traffic through the DCE is interrupted.

| Options | Settable in the Local LIC Type 5 | | Settable in the Remote LIC Type 5 (if not CCITT) | |
|-----------------------------|-------------------------------------|--------|--|--------|
| | PKD | LPDA-2 | PKD | LPDA-2 |
| DCE address | * | | * | |
| Default speed | * | * | * | * |
| Point-to-point - Multipoint | * | * | * | * |
| Control - Tributary | * | * | * | * |
| Type: IBM native | * | | * | |
| Long training sequence | * | * | * | * |
| Anti streaming | * | * | * | * |
| Transmit clock control | * | * | * | * |
| RFS delay | * | * | * | * |
| Line quality threshold | * | * | * | * |
| Receive level threshold | * | * | * | * |
| Hit count threshold | | * | | * |
| Nonswitching transmit level | ☐ | | | |
| CCITT | ☐ | | | |
| CD sensitivity | ☐ | | | |
| LPDA-1 enable | | | | |
| LPDA-2 enable | * | | * | |
| 2nd backup speed | * | * | * | * |
| Auto self-test | * | * | * | * |
| Switched transmit level | | | | |
| Autoanswer | | | | |
| Ring protection | | | | |
| Autodisconnection | | | | |
| Telephone numbers | | | | |
| Serial number | | | | |
| Base card EC level | Δ | Δ | | |
| Machine EC level | | | | |
| Microcode EC levels | Δ | Δ | | |
| Customer information | | * | | * |

* Read and set by customer

☐ Set by CE only

Δ Read-only.

Note: As options and some other configuration items can be set either locally or remotely, contentions may occur. The last received configuration, either from the line or from the attached operator panel, overrides the previous one.

Some of the above options are self explanatory; the others are explained hereafter.

DCE address

- Control and primary LIC type 5s : always 01
- Tributary and secondary LIC type 5s : any value

Default speed The non-volatile RAM holds the default speed indication, defined at configuration time, which is used at each power ON.

Point-to-point/multipoint

LIC type 5 can be 'Primary', 'Control', 'Secondary', or 'Tributary'.

Transmit clock control

Two options are available:

Internal clock The transmit clock is provided internally by the LIC type 5.

Receive clock The local transmit clock is locked onto the receive clock (decoded from the received data).

Line quality threshold

From 0 to 15, displayed in hexadecimal (0 to F)

- LPDA-2 setting ranges from 0 to E
- Control panel setting ranges from 0 to F. F means 'no threshold'.

If the line quality parameter is above or equal to that threshold, the line quality indication 'LQ' in the background information blinks on the displayed value, and the buzzer gives an audible alarm.

At installation, the threshold value is 8 which corresponds to a 10^{-5} bit error rate.

Receive level threshold

This is to specify the threshold above which a warning indication will be reported during LPDA-2 modem and line status report.

The range is from 0 to -43 dBm.

Carrier detector sensitivity

Two sensitivities are provided:

Low CD sensitivity Received signal below 31 dBm is not detected

Normal CD sensitivity Received signal is detected down to 43 dBm.

LPDA-2 hit count threshold

From 0 to 64. This field cannot be accessed from the control panel.

LPDA-2 setting ranges from 0 to 63. (64 means 'no threshold').

Transmit level See SMUX A/B section for authorized levels and settings.

CCITT Applied to point-to-point, makes the LIC type 5 compatible with CCITT V.27 bis, V.29 or V.33 recommendation for 4800, 9600 or 14 400 bps.

LPDA-2 enabled

Enabled Default option. The DCE intercepts and executes LPDA-2 commands.

Disabled the DCE ignores LPDA-2 commands.

Since LPDA-2 commands flow into the DCE as other pieces of data, the disable option may be selected if there is a chance that the LPDA-2 header may be erroneously detected in the data bit stream. The LPDA-2 header is guaranteed unique for the following data transmission protocols:

- SDLC NRZI
- BSC USACII or EBCDIC
- ALC.

First/second backup speed

Only used with CCITT V.29 option, to specify whether the 7200 or 4800 bps backup speed is used.

Card EC level One digit, from 0 to 3, wired on the LIC5 card, that specifies the level of the electronic components.

Microcode EC level

The EC level of the ROS and UVPROMs can be read on the PKD from the ROS themselves. They cannot be updated.

Host Support

Host support for LIC type 5 is NetView from R3, using LPDA-2 functions. See *LPDA Description*, SY33-2064 for LPDA-2 protocols, formats, and commands. Three sets of commands are available for:

- Problem determination
- DCE configuration
- Testing from the TSS.

Problem Determination Commands

Supported commands are:

- DCE status and test
- Line status
- Transmit/receive test
- Line analysis.

DCE Configuration Commands

The following 'operational commands' are supported:

- Read local configuration
- Write local configuration
- Set local transmit speed
- Read remote configuration
- Write remote configuration
- Set remote transmit speed
- Remote contact sense/operate.

Note: The following commands are **not supported**:

- Call-out
- Disconnect
- Local contact sense/operate in local LIC type 5
- Read local coupler
- Read remote coupler
- Write local coupler
- Write remote coupler.

TSS Commands

Two commands can be initiated from the TSS (FESA) to test the LIC type 5:

- CCITT loop 3 (with or without line wrap block)
- Self-test.

CCITT loop 3

This test is initiated by the 3745 TSS (FESA) on the DTE interface. The FESA has to detect RFS going ON before sending the data to be looped. For security purpose, the FESA can set up a timer (2100 ms maximum) to guard against no answer from a failing DCE.

The TSS/FESA follows the following sequence:

1. Start loop
 - Put RTS OFF
 - Detect RFS OFF in less than 50 ms
 - Set TC ON
 - Detect TI ON in less than 700 ms
 - Set RTS ON
 - Detect RFS ON in less than 200 ms
 - Send data to be looped on TD.
2. End loop
 - Stop data transmission
 - Put RTS OFF
 - Detect RFS OFF in less than 50 ms
 - Put TC OFF
 - Detect TI OFF in less than 100 ms.

Self-test The self-test from OFFline diagnostics pre-empts any other DCE functions.

It can be run only when the DCE is not connected to the network, and it doesn't need any line wrap plug.

The 'MODEM FAILED' bit is set to 1 in case of error. The 'MODEM BUSY' bit is raised solely as an answer to the self-test request from the 3745.

The test sequence is as follows:

1. Read interface
 - 'Modem failed' bit ON = error
 - 'Modem busy' bit staying ON for more than 4 s = error.
2. Set 'Self-Test Request' ON
 - 'Modem busy' should come ON in less than 200 ms.
3. Put 'Self-Test Request' OFF (to avoid continuous self-test)
 - 'Modem busy' should come OFF in less than 4 s.
 - 'Modem failed' OFF = self-test successful.

Manual Tests

The following manual tests are all initiated from the PKD:

- | | |
|--------------------|------------------|
| • Local loop back | Data disruptive |
| • Remote loop back | yes ¹ |
| • Local self-test | yes ¹ |
| • Local status | yes ¹ |
| • Remote self-test | no |
| | yes |

- Remote status yes
- Digital test (xmit/receive test) yes¹
- Analog test (line analysis) yes
- LIC line analysis procedures (LLAP) yes

¹ Run continuously until keying 'EXIT'.

Descriptions of the above manual tests are given later in this chapter, under 'Problem Determination Aid' for LIC type 5/LIC type 6.

Alarm Tone Detection

A failure tone is sent when a hard internal failure is detected. However, LIC type 5 DCEs detect both:

- Remote power OFF tones
- Remote failure tones.

Alarm tones are not detected if the DCE is executing a self-test.

If a failure tone and a power OFF tone are detected while executing a local status, only one of them is displayed.

Tone Characteristics

Frequency 325 Hz \pm 10 Hz

Level As written in NVRAM (default value provided by the switches on the SMUX card)

Power OFF tone duration

- 100 ms \pm 20 ms if power OFF lasts more than 100 ms
- Equals the power OFF duration if power OFF lasts less than 100 ms.

Failure tone duration

300 ms (repeated every 90 s until the DCE is powered OFF or the internal error disappears).

Tone Reception

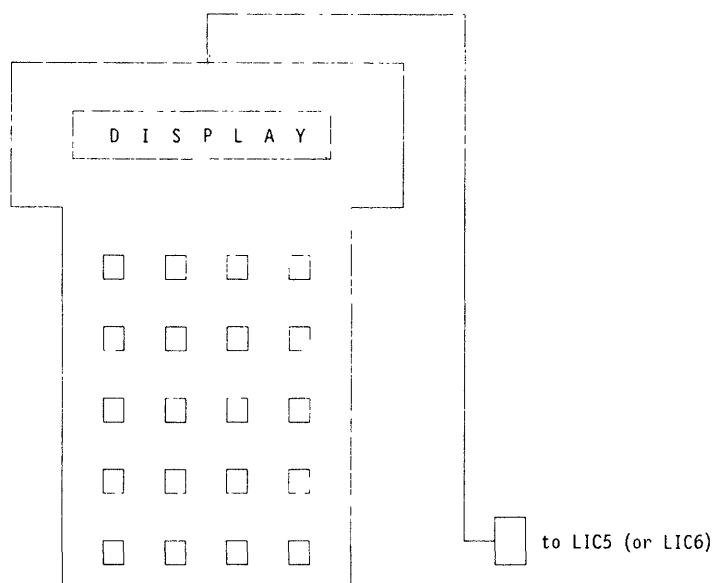
The detection is controlled by the microprocessor, which monitors the tone duration in order to differentiate the power OFF tone from the failure tone.

DCE Configuration

DCE (LIC type 5 or 586X) configuration (local or remote) is achieved by keying a set of commands from the IBM 5869 PKD connected to the relevant LIC type 5. See the *MIP*, SY33-2054 for detailed command procedures.

Portable Keypad Display (PKD)

The IBM 5869 PKD consists of a keyboard of 20 keys associated with a 16-character alphanumeric display, and audible alarm.



KEYPAD

| | | | | |
|-----|--------|---------|-------|-----------|
| | TEST | STATUS | SPEED | CONFIG |
| LOC | 0 | 1 | 2 | 3 |
| | TEST | STATUS | FULL | CONFIG |
| REM | 4 | 5 | 6 | 7 |
| | ANALOG | DIGITAL | BCKUP | CMD |
| | 8 | 9 | A | B |
| | PD | | | LOC. LOOP |
| | C | D | E | F |
| | GO | ERASE | EXIT | STOP |
| | | | | |

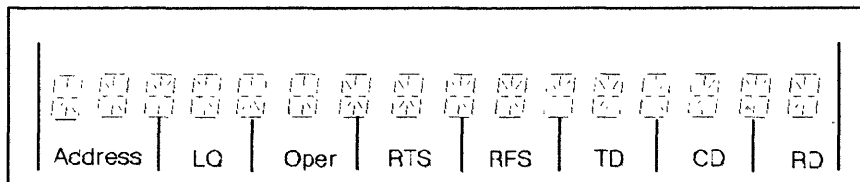
the following are the available main display operations. For procedures, display analysis, and actions, refer to:

- 3745 Problem Determination Guide, SA33-0096

- 3745 Connection and Integration Guide, SA33-0096.

Lamp Test

The 'GO' key displays all positions during 5 s on the screen to test the LEDs.



A specific key display can also be tested (by keeping that key pressed longer than 5 s).

Background Information

This is the default information that appears on the screen in normal mode. You find, from left to right:

- 3745 line physical (or logical in case of LIC swap) address: 2 characters
- Line quality irrelevant = x: x from 0 to F (0 is the best)
- Operate OFF = x: L = Non-switched, W = Local wrap via TC
- RTS OFF = 0 ON = 1
- RFS OFF = 0 ON = 1
- CD OFF = 0 ON = 1
- TD blinks on TD activity, indicates also speed of transmission: F = full, B = backup
- RD blinks on RD activity, indicates also speed of reception: F = full, B = backup.

Notes:

1. 'WRAP' is displayed instead of line address and line quality if a manual loop back test is running.

Transitions between 0 and 1 on the screen indicate that activity is taking place on the lead (except for RD and TD). If there is no activity the actual status is displayed.

- 2.

When CD = 0, RD indicates the speed of last data reception.
When RFS = 0, TD indicates the speed of last data transmission.

DCE Information

When the background information is displayed, keeping the **ERASE** key pressed will give you a display of the form:

aaaa bbb cc

where:

aaaa 4800 bps or 9600 bps or 14 400 bps or V.27 or V.29 or V.33

bbb Transmit clock option

- INT for internal (from local)
- RCV for received (from remote).

- cc** Network configuration
- PP for point-to-point primary
 - PS for point-to-point secondary
 - MC for multipoint control
 - MT for multipoint tributary
 - MT for CCITT V.29 or V.33.

This operation is not data disruptive. Releasing the **ERASE** key returns to background display.

LIC 5 Physical Address

When the background information is displayed, press the EXIT key for more than 0.5s. The LIC physical position on the board is then displayed.

POR - Bring-Up Information

At power ON reset time all the segments on the screen are lit (**), then 'COPY-RIGHT IBM 88' appears on the screen.

Normally, after the initial self-test is completed, the screen displays the background information. In the normal case, the DCE goes to 'operate'. If a severe problem occurs, the '**' remain on the screen.

If the initial self-test detects a severe error, the message:

LIC 5 FAILED

appears on the screen during 2 s and the DCE loops on bring-up.

Keying Procedures

Each function is performed in three steps:

1. Selection
2. Execution
3. Report.

Command Rejection

In some cases commands are rejected:

No response The remote did not answer, disruption of data transmission has already taken place.

Bad response The remote gave an invalid answer (wrong FCS), disruption of data has already taken place.

Busy TC ON If the lead TC is ON, all operator commands are rejected with the following message:

BUSY TC ON

The buzzer sounds one beep, and the message stays on the screen until the operator presses EXIT. There is no disruption of data.

Not executed The command can also be rejected with the 'NOT EXECUTED' message. Either it was a remote command and the DCE is in CCITT mode or the DCE is continuously busy with host commands (this may be an abnormal condition). If the message is caused by CCITT mode there is no disruption of data.

A remote speed change is not executed if the clock option of the remote DCE is not set to internal clock.

The buzzer sends the audible attention at the beginning of the report.

In report step, pressing a function key causes the return to selection step. This is a means to chain several commands without being pre-empted by commands coming from the host or the line (see contentions).

Self-Tests

The following self-tests are available:

- Local self-test (key 0)
- Remote self-test (key 4).

Status

The following status can be examined:

Local status Key 1. Not disruptive but forbidding LPDA-2 commands, informs on:

- Logged warnings
- Line quality end received level in dBm
- Hit count since the last 15 mn
- DTE interface local status and transitions

Remote status Key 5. Disruptive

- Logged warnings
- Line quality end received level in dBm
- Hit count since the last 15 mn
- DTE interface local status and transitions

Analog Test

This test (key 8) provides line analysis. It involves both local and remote DCEs and lasts 6 s on each side.

Digital Test

This test (key 9) is a transmit/receive test. It involves both the local and remote DCEs. Blocks of data are sent from the local to the remote DTE which wraps them back to the local one.

Block errors are counted on both sides and displayed on both screens. See page 4-99.

Local Loop

This command (key F) prepares the DCE for a loop 3 test. See page 4-56.

Speed Change

This option allows to change the speed locally and/or remotely from nominal to backup, and conversely. The speed cannot be changed if the remote DCE:

- Has the DSRS option
- Already runs at requested speed.

Configuration

The PKD being connected to a given DCE, the local DCE or the remote DCE configuration settings may be:

- Scrolled and displayed
- Updated.

Some fields are modifiable by the CE only, some others fields are 'read only' (for example, model).

If vital fields have been modified, returning to background causes a self-test to take place.

The table on page 4-69 shows the various configuration fields for local LICs type 5.

Contact Sense/Operate

These facilities are not available on LIC type 5, but on remote 586Xs only. They are:

- Open the 'contact operate' relay
- Close the 'contact operate' relay
- Get the status of the 'contact operate' and 'contact sense'.

Commands

The following commands can be executed in CE mode only:

- Send a 1004 Hz tone on the telephone line
- Load the default configuration (transmit level not changed)
- Update the configuration (all fields may be updated)
- Address a specific DCE via its serial number
- Long timer (10 mn) for LLAP
- Contact sense/operate (remote only).

All the above commands are reset at:

- Power OFF
- DCE re-initialization.

Buzzer Control

Each time a valid key is pressed there is a short bip. The absence of bip means that the key is either irrelevant to the current protocol or has not been taken in account by the keypad hardware.

Contentions

A request to execute an LPDA-2 command can come from:

- The local host
- The remote via the telephone line
- The panel.

Contentions are solved on a 'first request/first to be served' basis.

From the moment you release the GO key, until the end of the test, the DCE does not answer commands either from the line or from the DTE.

While executing a non-disruptive command the DCE does not answer LPDA requests from the host or from the line.

Re-synchronization is inhibited for remote commands.

Unsolicited Messages

These messages appear on the screen, without any operator intervention. If a PKD operator session is in progress the unsolicited messages are delayed. They can appear only when the screen displays background information. For complete information, refer to the *Configuration and Integration Guide*.

CMD FROM LINE (2 s)

CMD FROM DTE (2 s)

REM MODEM FAILED

Stays on screen until the operator presses EXIT. This message is not displayed if the PKD was not present when the condition occurred.

REM PWR LOSS In point-to-point, this message remains until CD goes ON or the operator presses EXIT. It appears as soon as the PKD is present if CD is still 0.

CONFIG FROM LINE When the DCE is being configured from the line or from the host.

CONFIG FROM HOST

Disappears at end of configuration, or if a power loss or failure tone is detected. If end of configuration has not been received the message stays on the screen during 5 mn. This message appears as soon as the PKD is present if the condition still holds.

CONFIG MISMATCH Configuration error.

KEY n STUCK

When the indicated key appears to be pressed during more than 5 s. The message stays 10 s then the control panel is reinitialized. This indicates a mechanical or electrical problem.

aa LIC5 FAILED

At power ON, the initial self-test failed. If the operator presses GO, the DCE attempts to start.

TEST FROM HOST

A test from the 3745 has been initiated.

WRONG SLOT

The cassette has been plugged in a wrong position.

TEST FAILED

A host self-test has failed.

SELF TEST FAILED

A self-test failed after a configuration change.

TEST OK

A self-test requested by the host was successful.

SELF TEST OK

A self-test was successful after a configuration change.

TEST OK NOWRP

A manual self-test without tel wrap plug was successful.

TEST OK WRAP

A manual self-test with tel wrap plug was successful.

PT2/3

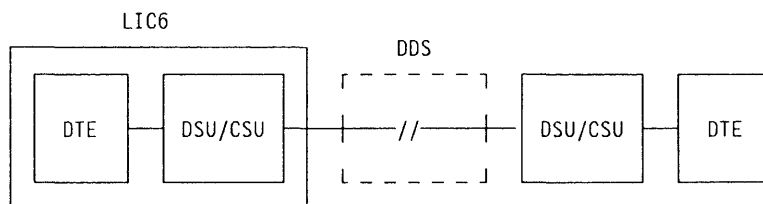
A 10-pin connector is available on the LIC type 5 panel to connect a PT2/3 used to investigate and record control and data signals.

LIC Type 6 DSU/CSU Function

DSU/CSU stands for: 'Data service unit/channel service unit', which is, in the LIC type 6, the equivalent of the DCE function of a LIC type 5.

Connection to US DDS

The DSU/CSU allows DTE-to-DTE communication through the digital data service (DDS) in the US.



Limited Distance Connection

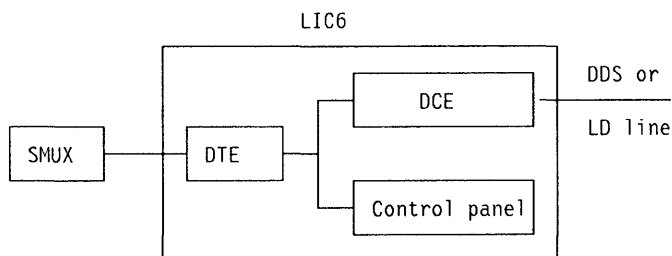
The DSU/CSU also allows DTE-to-DTE communication through private limited distance lines. The data is encoded and decoded as for DDS (protocols, rules, and so on).

Note: The LIC type 6 offers no local area data channel (LADC) attachment facility.

Maintenance Approach

Same as LIC type 5; see page 4-57.

Data Flow



Logic part

- DTE serializer/deserializer
- DCE microprocessor and signal converter
- DCE ROS, RAM, and EEPROM.

Analog part

- DCE coder/decoder
- DCE transmit/receive filters
- DCE line transformers.

Speeds

Each LIC type 6 houses one DCE which can operate at the following speeds, depending on the network it is connected to.

US digital data service network

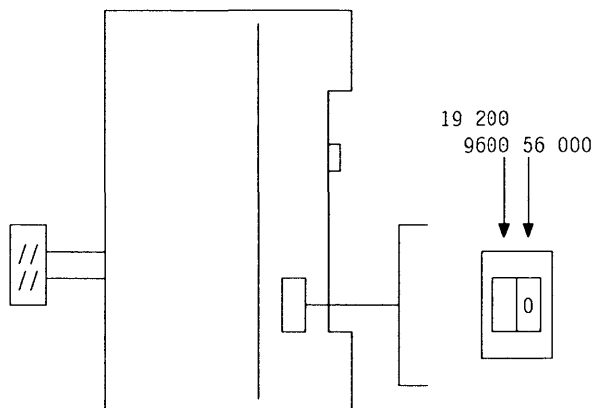
- 56 000 bps
- 19 200 bps
- 9600 bps

Non-switched 4-wire limited distance lines

- 56 000 bps
- 19 200 bps
- 9600 bps.

Speed Setting

The speed is set at installation time by a microswitch on the LIC type 6 card



- In V.35-like mode (56 000 bps), only one speed is available.
- In V.24-like mode (19 200 and 9600 bps), two speeds are available and must also be set at installation time from the PKD.

The speed setting cannot be changed either by NetView or by the MOSS.

Configurations

LIC type 6 DSU/CSUs are compatible with IBM 5822-10 DSU/CSUs. They operate in:

- Point-to-point and multipoint when connected to DDS
- Point-to-point only when connected to a limited distance line

Configuration Options

The following table shows the different ways of setting the CNM functions.

| CNM Functions | Settable by | | |
|---------------------|-------------|-----|------|
| | NetView | PKD | MOSS |
| Manual Command | No | Yes | No |
| Local wrap (loop 3) | No | Yes | Yes |
| Local self-test | Yes | Yes | Yes |
| LPDA-2 | No | No | No |

Data Format

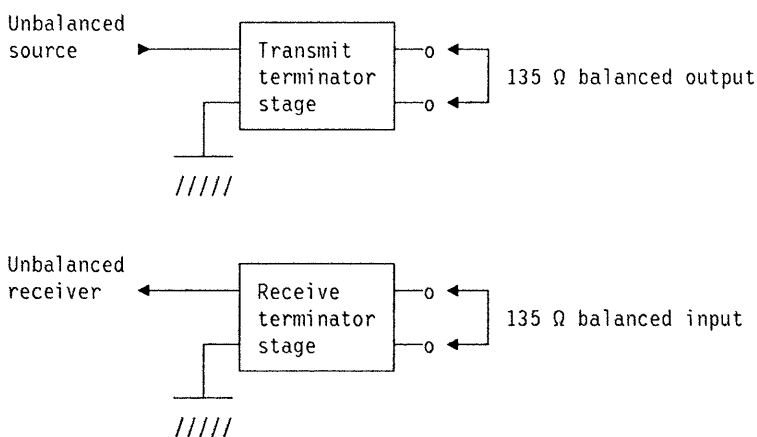
Synchronous, binary serial.

Modulation Technique

Bipolar, return-to-zero.

DSU/CSU to Line Interface

The LIC type 6 interfaces the DDS/LDM through balanced impedances matching the networks (both input and output circuitries may be regarded as 2-port networks).



The circuits are not damaged under the following conditions:

- Open circuit
- Short circuit between the leads
- Short circuit from either lead to ground.

The DC isolation between input and output leads with regard to ground is greater than 20 M Ω .

Surge Protection

Primary protection

A line surge protection (carbon block or gas tube) should also be provided by the line connector before the DCE wall plug.

Secondary protection

One protection device connected from tip to ring and two capacitors, from tip to frame ground, and from ring to frame ground.

This limits the maximum voltage to 80 V peak (line to line).

Transit Time

The transit time is the time that elapses between the input of a bit in the local transmitter and the output of this bit from the remote receiver, assuming a zero transmission delay over the telephone line.

Transmitter and receiver refer to the V.24 interface.

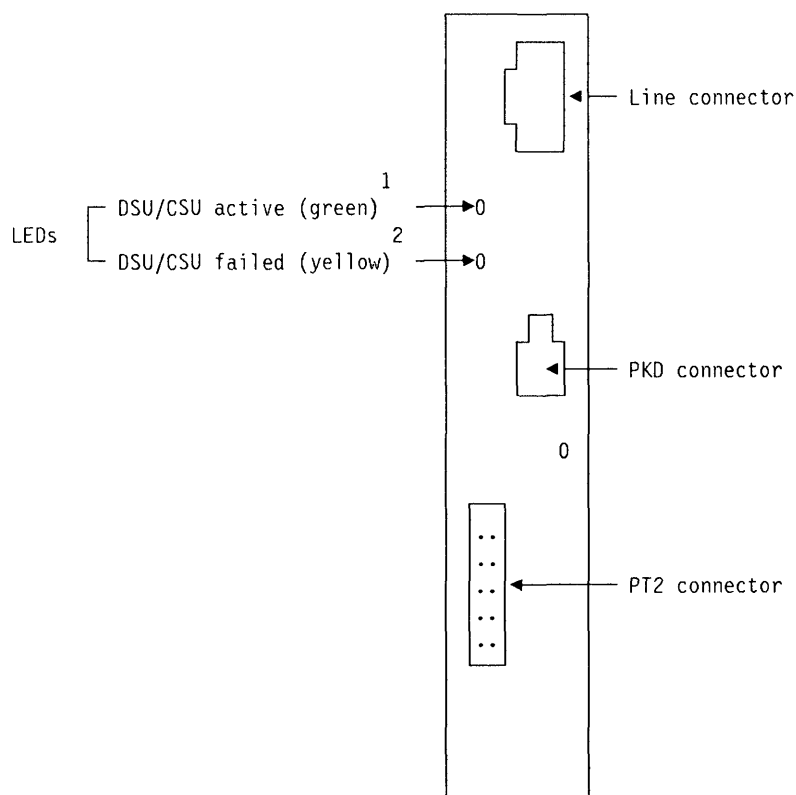
| | Transmission Speed (bps) | | |
|-------------------|--------------------------|--------|------|
| | 56 000 | 19 200 | 9600 |
| Transit time (ms) | 35 | 33 | 33 |

RFS Delay

The RFS delay is 7 to 20 bit-time for LIC type 6 in any configuration. It must be added to the transit time to evaluate the turnaround time.

| | |
|------------|--------|
| 9600 bps | 2.5 ms |
| 19 200 bps | 1.5 ms |
| 56 000 bps | 0.5 ms |

LIC Type 6 Panel



| | |
|------------------|---|
| 1 lit | DTR is ON (green LED) |
| 2 lit | Severe local DSU/CSU error is detected (yellow LED) |
| 1 and 2 flashing | LIC card plugged in a wrong place. |

Line Specifications

DDS network Refer to DDS documentation

Limited distance connection

The line specification depends on the length and the gauge of the wires.

Lengths and Gauges

The next table gives the maximum lengths in km (and miles) for the most common gauges used.

| Table 4-1. Maximum line length, according to wire diameter and transmission speed | | | | |
|---|-----------------------------|-----------------------|------------------------|-------------------------|
| Transmission Speed | Wire Diameter in mm/(Gauge) | | | |
| | 0.4 (26) | 0.5 (24) | 0.6 (22) | 0.8 (20) |
| 56 000 bps | 4.2 km (2.6 miles) | 6.0 km (3.7 miles) | 8.1 km (5.0 miles) | 13.7 km (8.5 miles) |
| 19 200 bps | 5.8 km (3.6 miles) | 7.9 km (4.9 miles) | 10.2 km (6.3 miles) | 15.7 km (9.7 miles) |
| 9600 bps | 7.3 km (4.5 miles) | 9.8 km (6.0 miles) | 12.6 km (7.8 miles) | 18.7 km (11.6 miles) |

Note: The most commonly used lines are 0.4 and 0.6 mm.

The distances given in the previous table (in kilometers and miles) are calculated for 34 dB of attenuation at the Nyquist frequency and associated with the following line parameters:

Line ic capacitor 50 nF / km
Line ic inductance 650 μ Henry / km
Line ic resistor 44/(DxD) in $\mu\Omega$ / km with D = line diameter in mm
Load impedance 135 $\mu\Omega$ (resistive).

Using an IBM cabling system type 1 (cable PN 4716748) or type 6 (cable PN 4716743) the expected distances will be:

- 4 km up to 19 200 bps
- 3 km at 56 000 bps.

On loops which meet the noise requirements defined in the *Bell PUB 62310* the bit error rate will not exceed 4/100 000.

At data rate over 19 200 bps, lines with a diameter greater than 0.6 mm will increase the group delay distortion.

Options and Configurations

The LIC type 6 is **not** configurable via LPDA-2 commands.

The speed option (V.35/V.24) is set from a switch on each LIC type 6 card but the speed option (19 200/9600) is set from the PKD. See "Speed Setting" on page 4-81.

The options are set in a non-volatile PROM, except for microcode and machine EC level.

The next table shows the options available to both customer and CE on local LIC type 6.

| Options | Local LIC Type 6 |
|-------------------------------|------------------|
| Point-to-point - Multipoint | Yes |
| DSU/CSU - Limited distance | Yes |
| Timing source | Yes |
| Network services ¹ | Yes |
| Byte 1 (speed V.35/V.24) | Switch |
| Speed 19 200/9600 | Yes |
| DCE address | Read only |
| Anti streaming | No |
| TC enabled | No |
| Buffer enable | Yes |
| Serial number | No |
| Machine EC level | No |
| Microcode level | Yes |

Point-to-point/multipoint

LIC type 6 can be 'Primary', 'Control', 'Secondary', or 'Tributary'.

DSU-CSU/LD Defines attachment to DDS network or limited-distance connection.

Timing source The receive clock provided by the LIC type 6 to the host is always recovered from the received signal.

The transmit clock can be provided by the LIC type 6 to the host in two different modes:

- Internal clock generation within the LIC type 6: this mode gives better performances in LDM connections
- Network clock used to generate transmit clock (synchronous mode).

Network services

- If selected (default option) the LIC type 6 intercepts and executes LPDA-2 commands
- If disabled, the LIC type 6 ignores LPDA-2 commands
- Since LPDA-2 commands flow into the LIC type 6 as other pieces of data, the disable option may be selected if there is a chance that the LPDA-2 header may be erroneously detected in the data bit stream. The LPDA-2 header is guaranteed unique for the following data transmission protocols:
 - SDLC NRZI
 - BSC USACII or EBCDIC.
 - ALC.

¹ If the option 'Network Services' is selected on the local LIC type 6, the option 'Network Services' or 'LPDA-2 Enable' must be selected on the remote DSU/CSU.

DCE address

- Control and primary LIC type 5 : always 01
- Tributary and secondary LIC type 5 : any value

Speed control See 'Speed Setting' on page 4-81.

Host Support

Host support for LIC type 6 is NetView, using LPDA-2 functions. See *LPDA Description manual*, form SY33-2064 for LPDA-2 protocols, commands, and formats.

Two sets of commands are available for:

- Problem determination
- Testing from the TSS.

Problem Determination Commands

Supported commands are:

- DSU/CSU status
- Line status
- Transmit/receive test.

TSS Commands

Two commands can be initiated by the 3745 TSS (FESA) to test the LIC type 6:

- CCITT loop 3 (with or without line wrap block)
- Self-test.

CCITT loop 3 This test is initiated by the 3745 TSS (FESA) on the DTE interface. It is the same as for LIC type 5. See page 4-72.

Self-test This test is the same as for LIC type 5. See page 4-72.

DDS Loop

This test is initiated by the DDS link via a bipolar code violation or a DC line current polarity reversal, as defined in the preliminary *ATT PUB 62310* dated September 1983. It consists in a wrap at the DTE interface:

1. Detect bipolar code violation or current polarity reversal
2. Raise TI
3. Set 'modem busy' bit ON in DTE registers
4. Drop CD and RFS, DSR kept ON
5. Force data to 'mark' at the host side, while looping back data from DDS
6. Detect end of bipolar code violation and current polarity reversal
7. Drop TI and reset the 'modem busy' bit.

The test lasts as long as a code violation or polarity reversal is detected. It runs only if the LIC type 6 is in operate mode.

Alarm Tone Detection

A failure signal is sent when a hard internal failure is detected, provided that 'network services' are enabled. This signal contains in a long sequence of bipolar zeroes.

However, LICs type 6 detect both:

- Remote power OFF tones
- Remote failure tones.

Tone Characteristics

| | |
|-------------------------------------|--|
| Speed | data speed |
| Duration | |
| | Power OFF 126 zeroes |
| | Failure 252 zeroes |
| End-to-end passthrough delay | varies from 32 to 64-bit times depending on the configuration. |

Tone Reception

The LIC type 6 receiving the alarm signal detects the alarm pattern and interprets the information as a remote failure or power OFF.

This information is kept in storage and is reported to the NCP on request.

DSU/CSU Configuration

DSU/CSU (LIC type 6 or 5822-10) configuration is achieved locally only by keying a set of commands from the IBM 5869 PKD connected to the relevant LIC type 6.

Portable Keypad Display (PKD)

See PKD, page 4-74.

Lamp Test

See page 4-75.

Background Information

This is the default information that appears on the screen in normal mode. You find, from left to right:

- 3745 line physical address (logical in case of LIC swap): 2 characters
- Line quality irrelevant = x : x from 0 to F (0 is the best)
- Operate OFF = X : L = leased, W = local wrap via TC, D = DDS loop test
- RTS OFF = 0 ON = 1
- RFS OFF = 0 ON = 1
- CD OFF = 0 ON = 1
- RD blinks on TD activity, indicates also speed of transmission: F = full, B = backup
- TD blinks on RD activity, also indicates speed of reception: F = high, B = low.

Notes:

1. 'WRAP' is displayed instead of DSU/CSU address and line quality if a local manual loop back test is running.
2. Transitions between 0 and 1 on the screen indicate that activity is taking place on the lead.

If there is no activity the actual status is displayed.

DSU/CSU Information

When the background information is displayed the operator can request the local DSU/CSU main information, by keeping the 'ERASE' key pressed. The display show the information in the form:

ttt ccc nn mmm

where:

- ttt** Type of functioning
 - 56 000 bps
 - 19 200 or 9600 bps
- ccc** Transmit clock option
 - INT for internal (from local)
 - NC for network clocking (from remote)
- nn** Network configuration
 - PP** Point-to-point primary
 - PS** Point-to-point secondary
 - MC** Multipoint control
 - MT** Multipoint tributary
- mmm** Connection mode
 - DDS for connections to DDS network
 - LDM for limited distance connections

The DSU/CSU information is displayed as long as the operator keeps pressing the ERASE key. Release the ERASE key to return to background display.

This operation is not data disruptive.

POR - Bring Up Information

Same as for LIC type 5; see page 4-76.

Keying Procedures

Same as for LIC type 5; see page 4-76.

Command Rejection

Same as for LIC type 5, see page 4-76.

Notes:

1. 'DTE ONLY' command rejection not available.
2. 'DDS LOOP ACTIVE' brings a command rejection.

Digital Test

See page 4-99.

Local Loop Back

This command prepares the DCE for a loop 3 test. See page 4-96.

Speed Change

Only for 19 200/9600 bps. See "Speed Settings". page 4-81

Configuration

The PKD being connected to a given LIC type 6, the **local** DSU/CSU configuration settings may be:

- Scrolled and displayed
- Updated.

Some fields are 'read only' (for example, machine level).

If vital fields have been modified, returning to background causes a self-test to take place.

The table on page 4-85 shows the various configuration fields for local LIC type 6:

Buzzer Control

Same as for LIC type 5; see page 4-78.

Contentions

Same as for LIC type 5, see page 4-78.

Note: If a function is selected while a loop (loop 3 or DDS loop) is being executed, a message (BUSY TC ON or DDS LOOP ACTIVE) appears on the screen.

If TC raises after selection but before execution BUSY TC ON is displayed.

Unsolicited Messages

These messages appear on the screen, without any operator intervention. If a PKD operator session is in progress the unsolicited messages are delayed. They can appear only when the screen displays background information. For complete information, refer to the *Configuration and Integration Guide*.

LDM LINE DOWN or DDS LINE DOWN

Lack of receiver timing or error on received block.

DDS OOS or DDS OOF

DDS out frame or DDS out of service indication.

CMD FROM LINE (2 s)

CMD FROM DTE (2 s)

REM DSU/CSU FAILED

Stays on the screen until the operator presses EXIT. This message is not displayed if the PKD was not present when the condition occurred.

REM PWR LOSS

In point-to-point, this message remains until CD goes ON or the operator presses EXIT. It appears as soon as the PKD is present if CD is still 0.

KEY n STUCK

When the indicated key appears to be pressed during more than 5 s. The message stays 10 s then the operator panel is reinitialized. This indicates a mechanical or electrical problem.

aa LIC6 FAILED DEFAULT CONFIG

At power ON, the initial self-test failed. Operator intervention is required to reconfigure the DSU/CSU.

INV PATTERN RCV TEST FROM HOST WRONG SLOT

Invalid pattern received (ex: a DDS pattern in LDM mode). A test has been initiated from the 3745. The cassette has been plugged in a wrong position.

| | |
|-------------------------|---|
| MAND DDS LOOP | A mandatory DDS loop has been initiated from the DDS (reversal polarity loop). |
| OPT DDS LOOP | An optional DDS loop has been initiated from the DDS (bipolar code violation loop). |
| TEST FAILED | A manual self-test failed or a host self-test failed. |
| SELF TEST FAILED | A self-test failed after a configuration change. |
| TEST OK | A self-test requested by the host is successful. |
| SELF TEST OK | A self-test is successful after a configuration change. |
| TEST OK NOWRP | A manual self-test without tel wrap plug is successful. |
| TEST OK WRAP | A manual self-test with tel wrap plug is successful. |
| DEFAULT CONFIG | Operation intervention is required to reconfigure the CSU/CSU. |

Manual Tests

The following manual tests are all initiated from the PKD:

| | |
|--|------------------|
| | Data disruptive |
| • Local loop back | yes ¹ |
| • Local self-test | yes ¹ |
| • Digital test (transmit/receive test) | yes ¹ |
| • LIC line analysis procedures (LLAP) | yes |

¹ Run continuously until keying 'EXIT'.

Descriptions of the above manual tests are given later in this chapter, under 'Problem Determination Aid' for LIC type 5 and LIC type 6.

PT2/3

A 10-pin connector is available on the LIC type 6 panel to connect a PT2/3 used to investigate and record control and data signals.

Problem Determination Aid for LIC Types 1 to 4

In addition to the TSS diagnostics, several aids are available to help in problem determination on a line or TSS problem:

- Line interface display (LID) function (refer to *Advanced Operations Guide*, SA33-0097).
- Wrap tests (WTT) function (refer to "Wrap Tests Controlled from the MOSS" on page 4-94 and *Advanced Operations Guide*, SA33-0097).
- Control program procedure (CPP) function (refer to *Advanced Operations Guide*, SA33-0097).
- TSS services (refer to *3745 Service Functions* manual, SY33-2069).
- Traces: external, internal SIT traces, checkpoint trace, NCP line trace.
- TSS dump.
- Port swap (refer to *Advanced Operations Guide*, SA33-0097).

Note: Internal SIT trace and TSS dumps can be transferred via RSF to be analyzed remotely by the PST CE.

Intermittent Error Messages or Messages Lost

Intermittent error messages or messages lost without alarm or BER-created, may come from an intermittent hardware failure of the LIC card or of the CSC card (data bit failure).

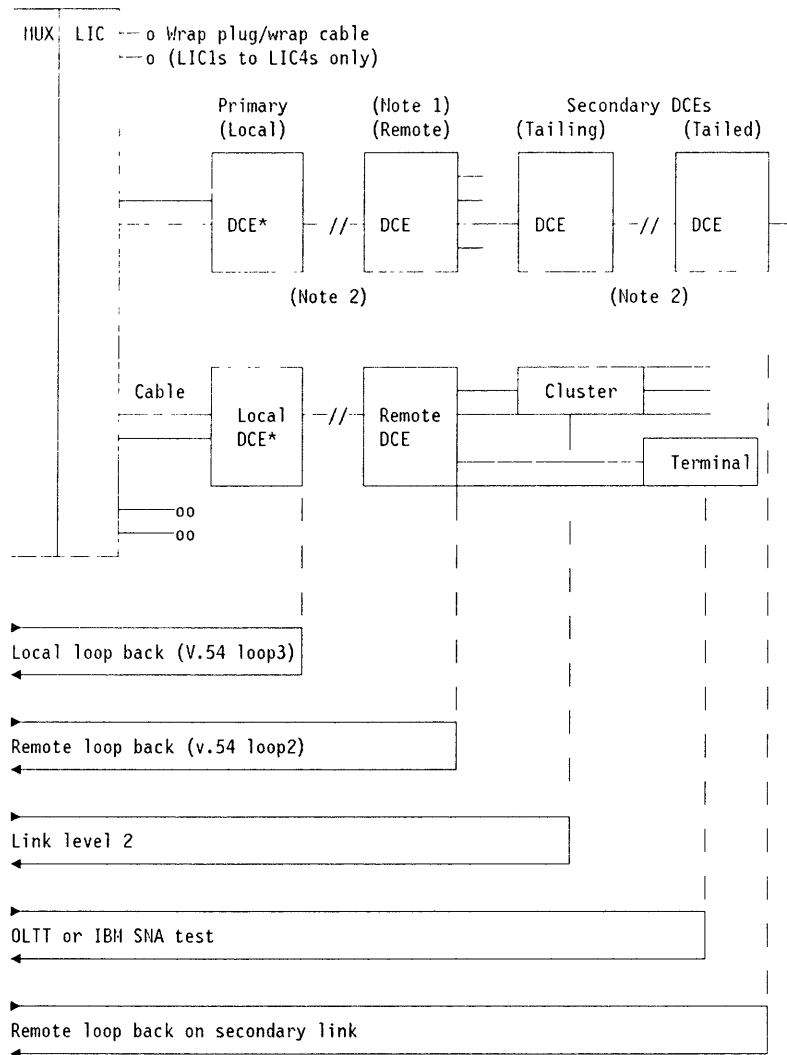
For that kind of symptom, run diagnostics to isolate the FRU:

- A LIC card hardware failure affects only the one to four lines of this LIC.
- A CSC card hardware failure, affects all lines attached.

Wrap Tests Controlled from the Host

Below are the different wrap test possibilities from the TSS to the terminal.

The wrap tests at the DCE (or NTT) cable level are part of the line functions and are described in the *3745 Advanced Operations Guide*, SA33-0097.



* Stand-alone for LIC type 1 to LIC type 4
Integrated for LIC type 5 and LIC type 6.

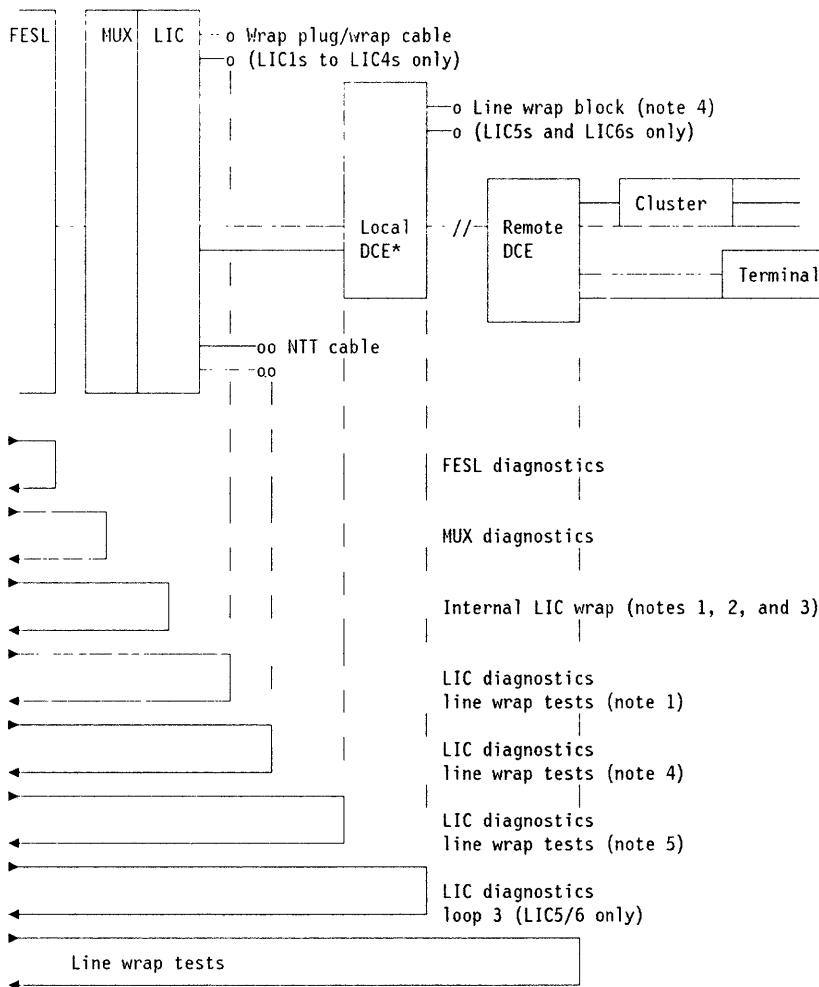
Notes:

1. The primary DCE is equipped with the data multiplexing feature or FIFO feature.
2. The telecommunication line is a 4-wire non-switched or switched line.

Wrap Tests Controlled from the MOSS

Below are the wrap tests controlled from the MOSS.

The wrap tests at DCE (or NTT) cable level are part of the line functions and are described in the *3745 Advanced Operations Guide*, SA33-0097.



* Stand-alone for LIC type 1 to LIC type 4
Integrated for LIC type 5 and LIC type 6.

Notes:

1. A line position can be plugged with a line cable, with a wrap plug (LIC type 1, 2, 4) or with a wrap cable (LIC type 3).

When the TSS diagnostics are run, the hardware for a selected line is:

- Tested up to the LIC drivers.
- Fully tested if a wrap plug or a wrap cable is present on the selected line. Plugging a wrap plug or wrap cable selects the section 'RC'.

2. During LIC wrap mode operation, the transmit data line and the control lines are not deactivated at the DCE interface (the DCE may be power ON or OFF).
3. Although this is not a user-activated test, an 'echo-check' mechanism (inline) checks the transmitted data in wrap mode.

4. For manual intervention routines, refer to *Maintenance Information Procedures*, SY33-2070.
5. If the cable is NTT with the connector switch set to 'operate', the test indicator (TI) signal is not forwarded to the connected DCE, so that the received pattern differs from the expected one.

Problem Determination Aid for LIC Type 5 and LIC Type 6

Wrap Tests Controlled from the Host

To test the DTE part of a LIC type 5 and LIC type 6, these tests are the same as for LICs type 1 to LICs type 4. See page 4-93.

Wrap Tests Controlled from the MOSS

To test the DTE part of LICs type 5 and LICs type 6, these tests are the same as for LICs type 1 to LICs type 4 (see page 4-94). In addition, the following tests are available:

- Wrap test up to DCE output (with or without line wrap block).
- Self-test (which occurs before 'control lead wrap' command takes place)
- LIC line analysis procedures (LLAP).

See the *Advanced Operations Guide*, and the *Problem Determination Guide* for details.

Manual Tests Controlled from the PKD

To test the DCE part of the LIC type 5 and LIC type 6, all the following tests are manually initiated from the PKD:

| Manual Test | Data Disruptive | LIC Type 5 | LIC Type 6 |
|--------------------------------------|------------------|------------|------------|
| Local loop back | Yes ¹ | * | * |
| Remote loop back | Yes ¹ | * | |
| Local self-test | Yes ¹ | * | * |
| Local status | No | * | |
| Remote self-test | Yes | * | |
| Remote status | Yes | * | |
| Digital test (transmit/receive test) | Yes ¹ | * | * |
| Analog test (line analysis) | Yes | * | |
| LIC line analysis procedures (LLAP) | Yes | * | * |

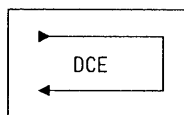
Notes:

1. The above tests run continuously until keying 'EXIT'. See the *Connection and Integration Guide* for details.
2. The process of the 'status bits' from the PKD is independent from the LPDA-2.

They are:

- Alarm tone received (remote DCE power loss)
- Alarm tone received (remote DCE failure)
- Carrier loss
- DCE re-initialization.

Local Loop Back (Loop 3)

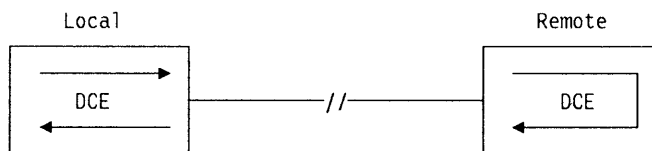


The DCE transmitter is wrapped to the DCE receiver, through the whole analog front-end section, except the line driver and receiver.

Receiver is set compatible with the transmitter, that is, for a multipoint control DCE, the receiver is set to multipoint tributary.

This test is a CCITT loop 3 wrap. It is the host's responsibility to send data under RFS control, and check receive data when CD is ON.

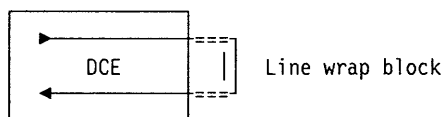
Remote Loop Back (Loop 2)



The DCE modem performs a digital loop, sending back the data it is receiving from the line. It is executed in CCITT mode only.

This test is a CCITT loop 2 wrap. It is the host's responsibility to send data under RFS control, and check receive data when CD is ON.

Local Self-Test for LIC Type 5



A line wrap block may be plugged into the line interface to allow line interface checking.

If the line wrap block is not plugged when 'local self-test' is selected from the PKD, a 'remote power loss' indication may appear at the remote DCE.

During the test execution, TI is raised at the local DTE interface, CD and RFS are dropped, and the data traffic through the DCE is interrupted.

DSR is dropped if DTR was OFF; otherwise DSR is kept ON.

During the test, the same sequence of operations is continuously repeated. The number of such cycles already performed since the beginning of the test is continuously displayed and incremented. Whenever an error is encountered, the test stops, the number of cycles is preserved, and an error code may be displayed by pressing the 'GO' key.

If during a self-test, the remote DCE sends an alarm tone, this tone is ignored by the DCE in self-test.

Local Self-Test for LIC Type 6

This tests checks the following components/functions:

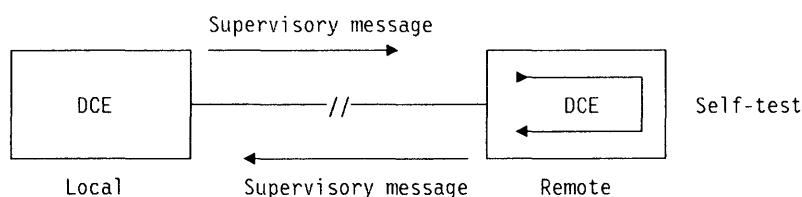
- Microprocessor
- ROS
- Internal and external RAM
- NVRAM (RAM part and configuration parameters)
- Read/write registers
- DTE module
- Line loop circuitry
- SDLC adapter
- Alarm signal (transcode test)
- CSU (stress test).

This test is automatically performed at each power ON. In this case, a check of the CMOS modules LSSD string hardware is added.

If an error is found during the tests of the configuration parameters in the NVRAM (checksum error which could be due to a blank area), then:

1. A default configuration is transferred from the RAM in the NVRAM.
2. The indication is recorded for a future LPDA-2 report if applicable.
3. The LIC type 6 is put in idle mode.
4. A warning is displayed.

Remote Self-Test



A supervisory message is sent from the local DCE to the remote (along with the DCE address). On reception of this message, the addressed DCE starts a self-test (less than 5 s) and sends back the result of the test in a supervisory message.

During the test execution, 'WAIT' is displayed on the local and the remote DCEs, TI is raised, RFS and CD dropped at the local and remote DTE interfaces, and the DATA traffic through the DCEs is interrupted.

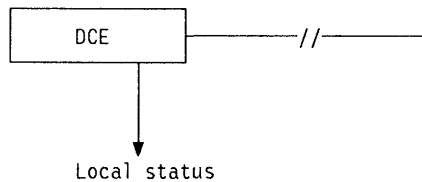
DSR drops at the local DCE, if DTR is OFF.

At the end, a report is displayed on the local DCE and normal background information on the remote DCE.

If the request causes the remote DCE to fail, the alarm tone is sent, and a report is displayed.

If a non-productive time out occurs after the request, a report is displayed.

Local Status



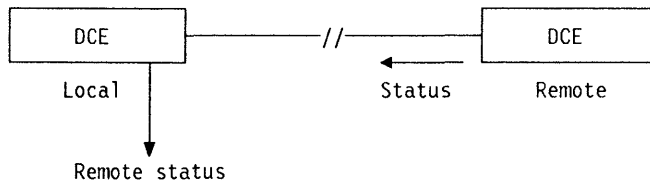
When initiated on the local DCE, the following information is displayed:

- Local line status (current quality, number of hits within the last 15 mn, warnings logged, current receive level)
- Local DTE interface status and activity.

Data traffic through the DCE is not interrupted. Normal operation take place at the DTE interface and TI is **not** raised. Then this test displays line quality and received level, until the 'STOP' key is pressed, or a 30 s time out is reached.

Any LPDA-2 command issued to the DCE from the DTE is ignored (TI is kept OFF).

Remote Status



When initiated on the local DCE, along with the remote DCE address, the following information is received (within 5 s maximum) and displayed at local DCE in the following sequence:

- Remote line status (current quality, number of hits within the last 15 mn, warnings logged, current receive level).
- Remote DTE interface state and transition since the last request.

During execution, TI is raised, RFS and CD dropped at the local and remote DTE interfaces, and the data traffic through the DCE is interrupted.

At local and remote DCE, DSR drops if DTR is OFF; otherwise, DSR is kept ON.

Digital Test (Transmit/Receive) for LIC Type 5

Loop test with a tributary station is performed in chopped carrier mode and half-duplex protocol. This protocol allows different inbound and outbound speeds in the control DCE of a multipoint network.

For each test 16 blocks (256 bytes each), are transmitted in each direction. The blocks missed or in error, are counted as erroneous.

In point-to-point, the test is run in continuous carrier operation.

During the test execution, TI is raised, RFS and CD dropped at the local and remote DTE interfaces, and the data traffic through the DCE is interrupted.

DSR drops at the remote DCE, if DTR is OFF.

This test loops on local and remote error counters, until the 'STOP' key is pressed.

Digital Test (Transmit/Receive) for LIC Type 6

This test, which is not protocol-transparent, can be selected only if LPDA-2 is enabled. During this test, local and remote DSU/CSUs exchange predefined bit patterns.

Analog Line Analysis Test

Causes the DCE, after about 10 s, to display some parameters of a telecommunication line between two DCEs (defined as local 'L' and remote 'R').

At test initialization some parameters are already available, because they are derived from data signal and continuously carried out during normal transmission, these values are inserted into line analysis report.

The other parameters are measured during the test itself:

- Data driven parameters:
 - Received level 'RL'
 - Minimum received level (last 15 mn) 'MRL'
 - Number of impulse hits (" ") 'HIT'
 - Number of line breaks (" ") 'LBK'

Larger than 10 dB below average value, for a duration longer than 10 ms (typical values).

- Impairments measured during test:
 - Line round trip delay, 'RTD'

Measured at local side, is the difference between command sending and acknowledgment receiving times. The measure does not include the DCEs passthrough delay.

- Non linear distortion 'H2' and 'H3'
- Signal-to-noise ratio 'S/N'

Measured from a 1004 Hz tone, into voiceband.

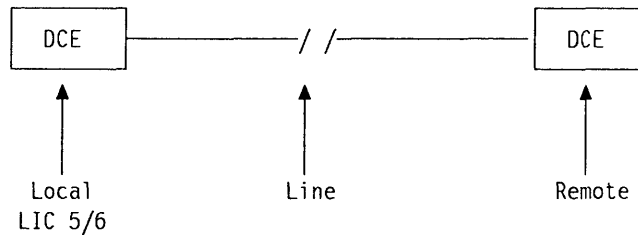
- Phase jitter 'PJ'

Phase modulation imposed by the channel to a 1004 Hz tone. Peak-to-peak phase jitter is measured in a 300 Hz bandwidth.

— Frequency shift 'FS'

LIC Line Analysis Procedures (LLAP)

The LLAP is a set of tests initiated manually from the PKD and which are automatically chained. They are intended to test a communication facility: the line itself and the two DCEs.



The following areas are successively tested :

- Local self-test
- Local self-test with telephone wrap plug
- Remote self-test
- Local/remote configuration compatibility
- Received and transmitted data activity on both DCEs
- Received line signal quality.

Note: Devices beyond the remote DCE (such as tailed DCEs and lines) are not tested.

Detailed LLAP procedures are described in the *Problem Determination Guide*.

TSS interface cables

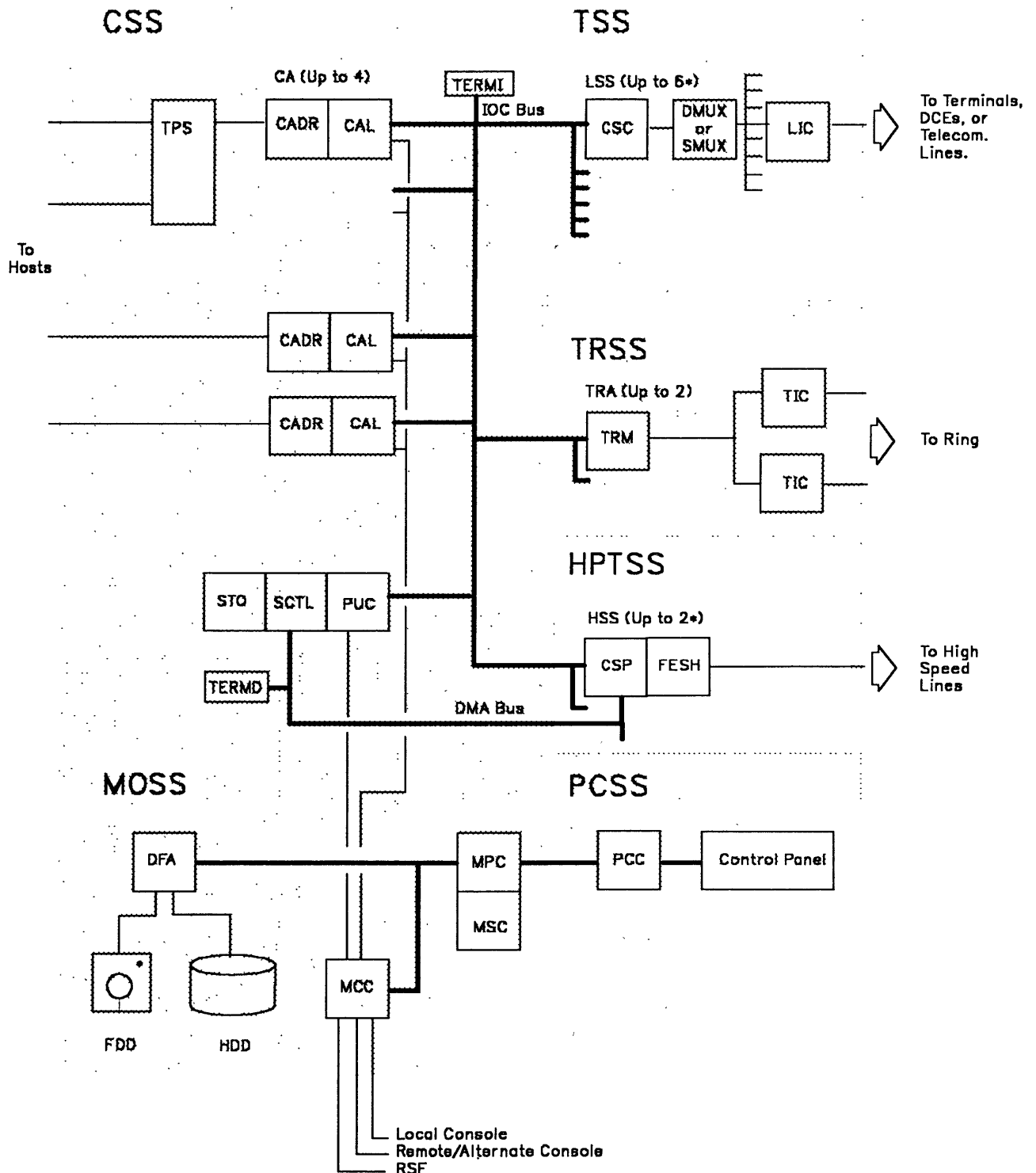
For details on interface cables and connectors, see the *External Cable Reference*, SY33-2075.

Chapter 5. High Performance Transmission Subsystem (HPTSS)

| | |
|--|------|
| HPTSS in 3745 Data Flow | 5-3 |
| Introduction | 5-4 |
| System Environment | 5-4 |
| HSS Packaging | 5-4 |
| Line Addressing | 5-5 |
| HSS Commands | 5-6 |
| Interface Types | 5-6 |
| HPTSS Data Flow | 5-7 |
| CSP Microcode Summary | 5-7 |
| Internal Interconnections | 5-9 |
| CSP-to-IOC Bus | 5-9 |
| FESH to CSP | 5-9 |
| FESH to DMA Bus | 5-10 |
| Communication Scanner Processor (CSP) | 5-10 |
| Front-End Scanner High-Speed (FESH) | 5-11 |
| Transmit Layers | 5-12 |
| Receive Layers | 5-12 |
| Modem-Out Layer | 5-12 |
| Modem-In Layer | 5-12 |
| Data Management Layer | 5-13 |
| DMA Manager Layer | 5-13 |
| CSP Layer | 5-13 |
| Scanner Status After the IML | 5-13 |
| Reset FESH | 5-14 |
| Transmit Operation | 5-14 |
| Microcode Functions | 5-14 |
| FESH Hardware Functions | 5-14 |
| Receive Operation | 5-16 |
| Microcode Functions | 5-16 |
| FESH Hardware Functions | 5-16 |
| Modem Interface Management | 5-19 |
| Modem-In Management | 5-19 |
| Modem-Out Management | 5-21 |
| Modem Retrain | 5-21 |
| Time Out Values | 5-22 |
| Customization Parameters | 5-23 |
| Error Detection and Reporting | 5-23 |
| Program/Hardware Checks | 5-23 |
| Hardware Error Detection and Reporting | 5-24 |
| DMA Interconnection Errors Detected by FESH (Register X'10') | 5-25 |
| CSP Interconnection Errors | 5-27 |
| FESH Internal Checkers | 5-28 |
| Line Interface Check | 5-29 |
| Error Status | 5-29 |
| Miscellaneous Status Fields | 5-31 |
| Status Control Field (SCF) Bit Definition | 5-31 |
| Secondary Status Field (SES) Bit Definition | 5-31 |
| Line Communication Status (LCS) | 5-31 |
| Initial Status Field (ISF) Bit Definition | 5-32 |

| | |
|--|------|
| Final Status Field (FSF) | 5-33 |
| Diagnostic Facilities | 5-37 |
| Problem Determination Aid | 5-37 |
| NCP Buffer Prefix Validity Checking in Receive | 5-37 |
| Problem Isolation and Network Management | 5-38 |
| External Wrap Facility | 5-38 |
| Communication Interfaces | 5-40 |
| FESH-DCE Interface | 5-40 |
| Cable Diagrams | 5-42 |
| Clocking | 5-42 |
| Local Attachment | 5-42 |

HPTSS in 3745 Data Flow



(* The number of LSS+HSS does not exceed 6)

Figure 5-1. HPTSS in 3745 Data Flow

Introduction

The high performance transmission subsystem (HPTSS) is a combination of one or several high-speed link scanners (HSSs) and NCP for the 3745.

The HSS is capable of clear channel, duplex, leased-line, HDLC/SDLC transmission using satellite, Transfix, and any other transmission link (fiber, direct attachment of 3745, 3725, and so on) requiring high-speed data transmission up to 2.048 Mbps.

This point-to-point non-switched connection can be attached to any network with the proper network adapter like data communication equipment (DCE) or network communication terminal equipment (NCTE).

The HSS operates with the Network Control Program (NCP) and is transparent to the SDLC data traffic.

System Environment

Since the HSS is transparent to the data, the NCTE or DCE must conform to the network standards. The HPTSS adapters (HSSs) can operate as secondary to the network clock connected to a network. When operating as a secondary, the HSS operates with any clock speed up to 2.048 Mbps.

The HSSs can also be directly connected back-to-back without a network.

When directly attached to each other, the adapters can operate at any one of the three speeds set by the NCP: 245.76 kbps, 1.47456 Mbps or 1.8432 Mbps. The connection to a 3725 is limited to 245.76 kbps.

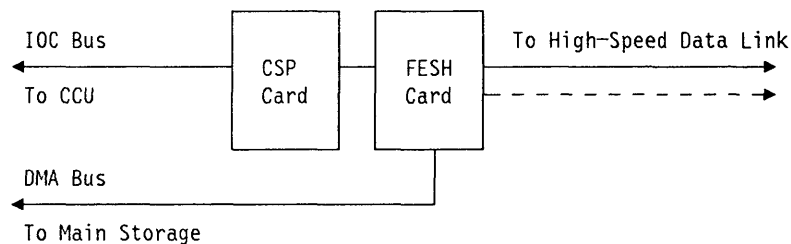
The HSS provides two separate V.35 or X.21 interfaces to a network. However, only one V.35 or X.21 interface to the NCTE or DCE can be active and enabled at a time.

HSS Packaging

The handling and management of such a high-speed data link is achieved by two cards:

- One communication scanner processor packaged on one card, the CSP card identical to those of the low-speed scanner (LSS) but with a different CSP microcode load module (Refer to "CSP Microcode Summary" on page 5-7).
- One high-speed front-end scanner packaged on one card, the FESH card.

For board and card locations, refer to the *Maintenance Information Procedures* manual, SY33-2070.



Up to two HSSs (coupled CSP/FESH cards) may be installed on the basic board of the base frame, to control up to two high-speed data links at one time.

On each FESH, a fan-out (standard feature) allows two high-speed data links to be connected at the tail gate to that FESH. But only one of them must be active at a time.

No line interface coupler card (LIC) needs to be installed as for the lines connected to the low-speed scanner (LSS).

Line Addressing

Each HSS supports a maximum of two line addresses. However, only one line at a time may be active.

With two possible HSSs, the maximum number of lines is 4. Line numbers 1028 through 1031 are dedicated for HSS use.

The two lines associated with a particular HSS are addressed by the TD1 field of the IOH. TD1 bit 6 selects one of the two lines. TD1 bit 7 selects an interface: '0' for the transmit and '1' for the receive.

| Line Adapter and Port Number | | Scanner Line | Line Address | Board Card and Connector Position | Tailgate Position |
|------------------------------|--------|--------------|--------------|-----------------------------------|-------------------|
| 3 | Port 1 | 1028 | 404 | 01G-A1U-J1 | 01Q-C0-J2 |
| 3 | Port 2 | 1029 | 405 | 01G-A1U-J2 | 01Q-C0-J1 |
| 4 | Port 1 | 1030 | 406 | 01G-A1S-J1 | 01Q-D0-J2 |
| 4 | Port 2 | 1031 | 407 | 01G-A1S-J2 | 01Q-D0-J1 |

HSS Commands

Commands are set in TD0 of the start line or start line initial instructions. The following NCP commands are supported by the HSS:

| Commands | Codes (Hex) |
|---------------------------------|-------------|
| Set mode | 01 |
| Enable | 02 |
| Disable | 03 |
| Change | 06 |
| Flush data | 09 |
| ResetD | 0B |
| ResetN | 0C |
| SDLC transmit control | 10 |
| SDLC transmit data | 11 |
| SDLC receive | 13 |
| SDLC receive continue | 14 |
| Trace | 2C |
| Stop trace | 2D |
| Halt | F0 |
| Halt immediate | F1 |
| Dump Control blocks (no status) | F4 |
| Dump Control blocks (status) | F5 |

The following MOSS command is supported by the HSS:

| Commands | Codes (Hex) |
|----------|-------------|
| Wrap | 2E |

Interface Types

Two types of line interface are available at the exit of the FESH card: (Refer to "Communication Interfaces" on page 5-40 for more details)

1. V.35
2. X.21 leased (including French Transfix).

They allow the 3745 to be connected to:

- U.S. T1 type line
- European high-speed lines (CEPT lines)
- Satellites
- In-plant transmission link for direct-attached adapters.

HPTSS Data Flow

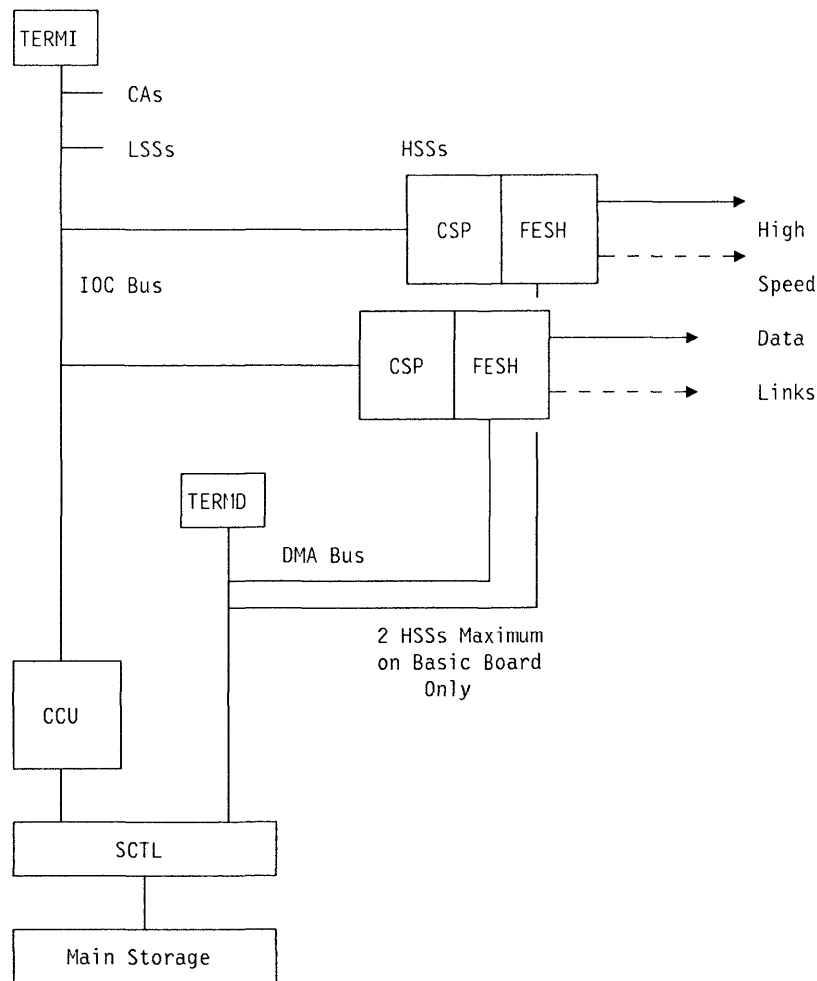


Figure 5-2. HPTSS Data Flow

CSP Microcode Summary

The HSS requires a different CSP microcode load module than the LSS to take advantage of the hardware buffer management for supporting speeds up to 2.048 Mbps.

Listed below are the main microcode functions supported by the HSS.

- Supported line speed: up to 2.048 Mbps
- Supported line interfaces: V.35 and X.21 (called X.21 Transfix in France) leased line
- SDLC/HDLC duplex protocol on point-to-point leased line

A network adapter may be required, such as DCE or network communication terminal equipment (NCTE).

- Echo suppression
- Frame up to 64 kbytes long (SNA maximum size)
- CSP ROS common with other microcode load modules
- SDLC address compare performed by FESH

- NCP buffer prefixes automatically handled by FESH via DMA bus (except for SIT buffers)
- The HSS transfer of data between adapter and NCP differs from the LSS:
 - When the LSS transfers data to the NCP buffers, via the IOC bus, it uses the cycle steal mechanism.
 - When the HSS transfers data to the NCP buffers, via the DMA bus, it uses the FESH hardware.
- One PIO per SDLC frame for transmit
- One or several PIOs per SDLC frame are possible for receive
- IOC cycle steal is not used (except for IML, dump or back-up for LSS services).

Main Differences with LSS

- Buffering of the receive and transmit frames is done in a FESH buffer instead of CSP storage.
- SDLC transmit continue command not supported.
- SDLC receive monitor command not supported.
- No multiplexing (only one line).
- HSS microcode deals with buffer prefixes only with scanner interface trace (SIT). The remaining buffer prefix handling is done by the FESH.
- CCU storage access for NCP buffer data is done through DMA instead of IOC cycle steals as in LSS.

However, IOC is still used for the following:

1. Dump, IML, diagnostics.
2. Sending status (followed by CCU level 2 interrupt) when FESH, DMA or SCTL error has to be reported.
3. Facilities (Refer to "Problem Determination Aid" on page 5-37) invoked from the operator console (MOSS) to:
 - a. Perform diagnostics.
 - b. Access FESH registers and random access memory.
4. IOH transfer between NCP and CSP.
5. MOSS exchange with HSS.

Internal Interconnections

As shown in "HPTSS Data Flow" on page 5-7, each HSS interconnects with the communication subsystem (CSS) and the MOSS via the IOC bus and the DMA bus.

CSP-to-IOC Bus

This connection is used for:

- Communication with the NCP (through the same IOH high level commands as the other LSS scanners)
- MOSS command exchange
- HSS IML
- Diagnostics.

The physical interconnection between the HSS CSP and the CCU is identical to that between the LSS CSP to the CCU (Refer to the Chapter "Transmission Subsystem").

For board and card locations, refer to the *Maintenance Information Procedures* manual, SY33-2070.

NCP-HSS Microcode

The CCU uses IOH and IOHI to exchange data, commands and statuses with the HSS CSP in the same way as with the LSS, but cycle steal is not used when the FESH is running.

CLDP-HSS Microcode

The controller load/dump program (CLDP) is used in a remote 3745 to interconnect the CCU and the HSS CSP microcode. The main functions performed are:

- IPL of the remote 3745
- Dump of the remote 3745

The CLDP never:

- Issues SDLC transmit continue or receive monitor commands
- Uses data areas, but NCP buffer pointers for both transmit and receive operations.

FESH to CSP

The physical interconnection between the FESH and the CSP is identical to that of the internal interconnection between the FES fonction and the CSP of the LSS.

For board and card locations, refer to the *Maintenance Information Procedures* manual, SY33-2070.

Microcode to FESH

The picocode is loaded from the CSP in each layer of the FESH RAM at IML time. The FESH-to-CSP interconnection is activated and controlled via external registers and control words (CW). A CW is built by the CSP microcode and specifies the actions to be performed by the FESH. The CW is cycle stolen by FESH, then executed. The FESH informs the CSP microcode when the action is completed.

Data Transmission

The CSP microcode can issue the following commands to the FESH:

- Start transmit initial
- Start transmit
- Soft stop transmit (For example; it causes the FESH to transmit the error sequence, which is a MOSS init parameter from the NCP)
- Hard stop transmit (For example; it forces the transmit data line to a mark level all ones).

Data Reception

The CSP microcode can issue the following commands to the FESH:

- Start receive
- Start receive continue
- Stop receive
- Flush the current frame.

Data and Modem Management

The CSP microcode can issue the following commands to the FESH:

- Start modem monitor
- Start modem-out
- Start data management

FESH to DMA Bus

This connection is used for direct CCU storage access and specifically:

- NCP buffer prefix exchange
- Data transfer between the high-speed line and main storage
- Parameters and status exchange between the NCP and the HSS microcode.

Communication Scanner Processor (CSP)

The HSS CSP hardware is identical to that of the LSS CSP (Refer to the Chapter "Transmission Subsystem" for details).

Front-End Scanner High-Speed (FESH)

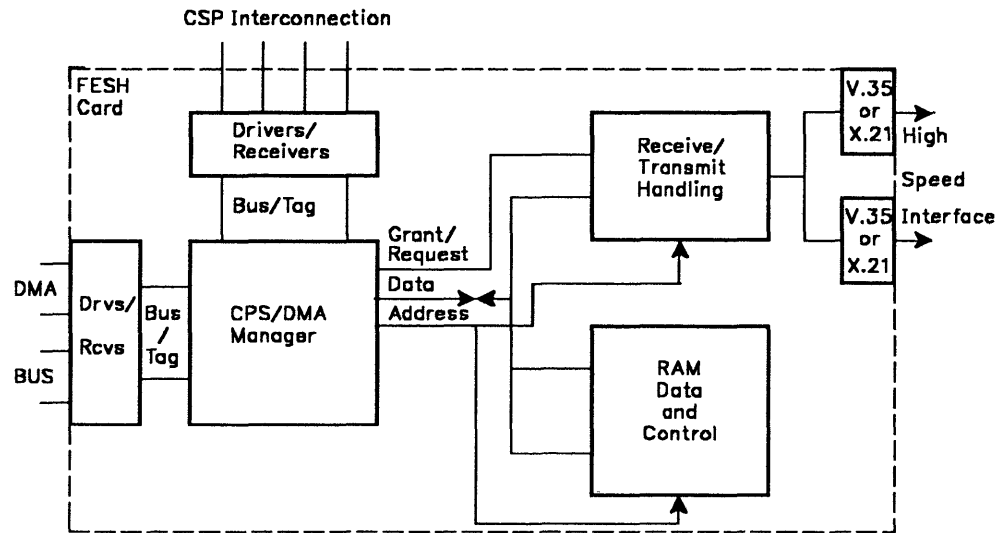


Figure 5-3. FESH Data Flow

The transmit/receive handling of the FESH is functionally organized in layers as follows:

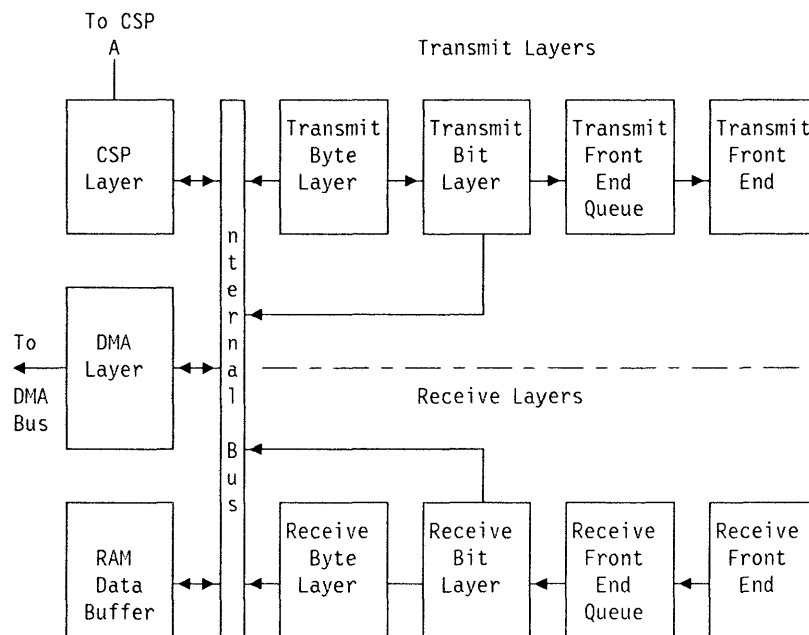


Figure 5-4. Transmit and Receive Layers

Transmit Layers

The transmit layers are composed of:

- The front-end circuits which perform the following functions:
 - Serialization of data
 - Flag generation
 - Zero insertion
 - CRC generation.
- The transmit bit layer which:
 - Handles byte transfer between transmit front-end buffers and the FESH RAM.
- The transmit byte layer which:
 - Handles NCP buffer prefixes for transmission.
 - Interconnects with the CSP layer (external registers and control words).

Receive Layers

The receive layers are composed of:

- The front-end circuits which perform the following functions:
 - Deserialization of data
 - Zero deletion
 - Flag detection
 - Early flag detection
 - Abort detection
 - Idle detection
 - Overrun detection
 - CRC calculation error detection
 - Address compare/satellite echo suppression
 - Interconnection with receive queue buffer.
- Receive bit layer:
 - Handles byte transfer between receive front-end buffer and FESH RAM.
- Receive byte layer:
 - Handles NCP buffer prefixes for receive
 - Interconnects with CSP layer (external registers and control words).

Modem-Out Layer

The modem-out layer:

- Interconnects with the CSP layer control word (CW).
- Activates output modem control leads according to the modem-out CW prepared by the CSP microcode.

Modem-In Layer

The modem-in layer:

- Interconnects with the CSP layer (control word and external registers).
- Performs input modem control lead status confirmation.

- Reports input modem control lead changes and X.21 steady states according to the modem-in CW prepared by the microcode and stored in the FESH RAM.

Data Management Layer

The data management layer:

- Handles transfer from/to the NCP, to/from CSP storage of any information exchange between the NCP and the CSP storage (mainly NCP parameters/status).
- Interconnects with the CSP layer (control word and external registers).

DMA Manager Layer

The DMA manager layer:

- Interconnects on one side with:
 - FESH RAM
 - Data management buffer
- Interconnects on the other side with the DMA bus.
- Handles the DMA bus protocol.
- Performs data transfer from/to CCU main storage, to/from transmit/receive/data management buffers.
- Handles priorities of DMA bus requests from transmit/receive data management layers.

CSP Layer

The CSP layer:

- Interconnects on one side with the CSP storage and microcode.
- Interconnects on the other side with the various FESH layers via CSP external registers and cycle steal operations.
- Handles the protocols of CSP external registers and cycle steal operations.
- Handles cycle steal requests from transmit/receive/data management/modem-in/out layers on a priority basis.

Scanner Status After the IML

At the end of scanner IML it is possible to get from the CCU storage, the status of the scanners associated with their mailbox.

The 16-byte mailboxes are located from CCU storage address 3F8000.

The status of the scanners just IMLed are in the last two bytes of the mailbox. These values must be displayed before any mailbox exchange between the CCU storage and the corresponding scanner (for example: CCU functions).

Below are the possible statuses of the scanner after an IML:

| Values | Description |
|---------|--|
| X'nnFF' | No answer from scanner following the MOSS command 'nn' |
| X'C900' | Normal status IML OK |
| X'C901' | FESH picocode failed |
| X'C902' | FESH card and picocode level not compatible |
| X'C904' | FESH card not installed |

Figure 5-5. Values of the Last Two Bytes of the Mailboxes after IML

Reset FESH

All latches are reset, the DMA and modem interfaces are disabled, the card is kept in 'freeze mode' (FESH not operational) until the CSP loads the microcode in those storage locations which are not reset.

Transmit Operation

Microcode Functions

The microcode:

- Handles NCP transmit commands through PIO operations on the IOC bus.
- Gets transmit parameters and sends transmit status from/to the NCP via the DMA bus.
- Builds the transmit control word (CW) to be sent to the FESH.
- Indicates to the FESH transmit layer (external register setting) the:
 - Transmission coding mode (NRZI or non-NRZI) at set mode
 - Start of transmit initial
 - Start of transmit
 - Stop of transmit operation (hard and soft).

FESH Hardware Functions

Transmit Initial Command

The transmit initial command is used between the CSP and FESH hardware to perform a wrap test on the X.21 interface. The NCP issues a wrap command to the FESH with modifier bits indicating the type of wrap to be performed.

Then, the CSP issues the transmit initial command with the loop bit ON to the FESH, to support X.21 network testing, or to send a data pattern other than flags between SDLC frames.

On reception of a start transmit initial command from the microcode, according to a control bit (loop bit), the FESH sends in 'non-zero insert mode' to the transmit line:

- Loop bit OFF:
 - An initial character sequence (7 characters maximum) prepared by the microcode at initialization time.
 - Then, the SDLC frame with the receipt of the transmit command (Refer to the "Transmit Command" on the next paragraph).
- Loop bit ON:
 - The initial character sequence (7 characters maximum)
 - Then sends *the last two characters of the sequence continuously* until the microcode sets the start transmit command or the stop transmit command (used by the X.21 wrap command from the CSP to the FESH).

Transmit Command

On reception of a start transmit command, the FESH transmit layer cycle steals the transmit control word prepared by the microcode in CSP storage.

When the control word is loaded, the transmit byte layer:

- Cycle steals the A/C fields prepared by the microcode in CSP storage.
- If the SDLC frame contains A/C fields only the transmit byte layer starts the transmission.
- If the SDLC frame contains an I-field, the FESH begins a DMA operation to load the I-field from the CCU storage to the FESH RAM via the DMA bus.

Note: The maximum size of an A/C field is four bytes.

For an SDLC I-frame transmission, the bit layer machine and the byte layer machine operations are overlapped so that the transmission of data can continue while data is being obtained from the CCU via the DMA interconnection.

This overlap of operations continues until a zero buffer pointer is detected.

- When a zero buffer pointer is detected the bit layer instructs the front-end to send the CRC and ending flag, followed by the ending sequence specified at set mode (line at mark or continuous flags).
- The byte layer also sets the end of transmit bit in the transmit status register and generates a level 2 interrupt to the CSP.

During the transmission over the line, the hardware may detect that no data has been loaded in the external RAM whereas the FESH bit layer requests a new buffer (DMA transfer up to the buffer count not completed), in that case the hardware:

- Sets the underrun and the end transmit bits in the transmit status register.
- Raises a level 2 interrupt to the CSP.
- Sends the transmission error sequence initialized at set mode.

Soft Stop Transmit Command

On reception of this command, the hardware:

- Stops transmitting the data.
- Stops any transmit DMA transfer in process.
- Sends the transmission error sequence initialized at set mode.

Hard Stop Transmit Command

On reception of this command, the hardware:

- Stops transmitting data.
- Stops any transmit DMA transfer in process.
- Puts the line at mark.

Receive Operation

Microcode Functions

The microcode:

- Handles NCP receive commands through PIO operations on the IOC bus.
- Gets receive parameters from the NCP.
- Sends receive status from/to the NCP through data management exchanges on the DMA bus.
- Prepares the receive control word (CW) for the FESH:
 - The CSP cycle steals the storage address of the received SDLC frame address/control fields.
 - If a non-I frame is to be transmitted, the number of bytes of the A/C field is indicated(4 bytes maximum).
- Indicates to the FESH (external register setting) the:
 - Transmission coding mode (NRZI or non-NRZI) at set mode
 - Start of receive command
 - Receive continue command
 - Stop of receive operation command
 - Flush command.

FESH Hardware Functions

Receive Command

When the FESH is enabled it always:

- Monitors for flag (flush other characters).
- Performs address compare.
- On flag recognition, starts accumulating received characters in the receive queue buffer.
- Performs zero deletion.
- Performs CRC accumulation (The two CRC characters are not stored in the receive queue buffer).
- On flag recognition, checks the CRC.
- Stores the receive ending conditions in the receive queue buffer and then in external register X'10' for the microcode:

- End of receive CRC OK
- End of receive CRC bad
- Flag OFF boundary
- Abort (not followed by idle)
- Idle
- Overrun.
- Accumulates multiple frames in the receive buffer queue.
- If receive queue full:
 - Indicates overrun as ending condition in receive queue.
 - Flushes further incoming characters of the frame on which the overrun occurred.
 - Ignores subsequent data and flags until the CSP issues a receive command.

Receive Flow

On reception of a receive command from the microcode, the FESH receive layer:

- Cycle steals the receive control word (CW) prepared by the microcode in CSP storage.

When the CW fetch is completed, the receive byte layer:

- Cycle steals the A/C field into CSP storage starting at the address specified in the receive CW.

If the ending condition is reached (no I-frame) the byte layer:

- Generates a level 2 interrupt to the CSP.

If no ending condition is detected in the receive queue (I field), the following operations are performed.

Receive Operation For I-Frame:

The receive operations are overlapped so DMA operations are done in parallel with the extraction of the data characters from the transmission line.

The process is continued until the ending condition is detected.

End of Receive:

When an ending condition is detected in the receive queue, the byte layer sends the address of the last NCP buffer used, plus the residual byte count of the last buffer, in CSP storage, and generates a level 2 interrupt to the CSP.

Receive Continue Command

During the receive flow, the byte layer detects the end of message:

- Stops reading characters from the receive queue, but the FESH continues receiving characters from the line.
- Raises an interrupt to the CSP and indicates to the microcode that a new buffer pool is needed.
- Waits for start receive continue from the microcode.
- On reception of start receive continue from the microcode, the hardware resumes the normal process.

Flush End of Frame Command

When receiving I-frames to be flushed, a 'frame reject' frame (FRMR) can be received and must not be flushed. For this purpose, the NCP issues a receive command to get the A/C field of the received frame.

In that case the FESH performs an action similar to the receive continue process and:

- Stops reading characters from the receive queue after having sent the A/C fields into CSP storage.
- Raises a level 2 interrupt to the CSP and indicates to the microcode that a new buffer pool is requested.
- Waits for start receive continue from the microcode in case of FRMR frame, or for a flush end of frame command.

Flush Command

On reception of this command, the hardware reads and flushes the remaining data characters of the frame out of the receive queue, until an ending condition is reached. This ending condition is reported to the microcode.

Stop Receive Command

On reception of the stop receive command from the microcode, the hardware clears out the contents of the receive queue buffer.

Modem Interface Management

Modem-In Management

To manage the DCE input leads, the microcode:

- Prepares a CW in CSP storage.
- Starts the process by sending the start modem monitoring command to the FESH.

The modem-in layer monitors the modem input leads.

On a modem control lead change, according to the CW, and after possible lead state confirmation, the modem-in layer interrupts the microcode (level 2 interrupt) which can then get the modem input lead status at the time of the change.

After a modem change has been reported to the microcode, the hardware does not report a new change until the microcode sends a new modem-in monitoring command.

Confirmation parameters are defined in the configuration data file and are loaded in the FESH at initialization time.

V.35 Modem-In Lead State Confirmation

On V.35 lines, the FESH is capable of monitoring:

- Data set ready (DSR)
- Clear to send (CTS)

However, in normal operation, the CSP microcode only monitors the DSR and CTS leads.

The FESH modem-in layer starts a count before delivering the new modem-in value to the CSP, in order to avoid unwanted interrupts caused by modem-in leads bouncing, or specific DCE behavior.

The confirmation delay is adjustable by the customer, through the CDF function, to adapt to the DCE characteristics.

DSR Confirmation:

Confirmation is performed on DSR going ON and OFF.

The confirmation delay is specified for each signal in a 3-bit parameter field loaded by the microcode. A specific timer starts each time the associated signal switches. The change is confirmed when the timer elapses.

| Parameter Value | Confirmation Delay |
|-----------------|--------------------|
|-----------------|--------------------|

| | |
|-------|----------|
| 0 0 0 | No delay |
| 0 0 1 | 1 ms |
| 0 1 0 | 4 ms |
| 0 1 1 | 16 ms |
| 1 0 0 | 32 ms |
| 1 0 1 | 64 ms |
| 1 1 0 | 128 ms |
| 1 1 1 | 256 ms |

Note that the actual confirmation delays can be greater than the above values due to the fact that the timers restart at each signal change.

CTS State Confirmation:

The CTS state confirmation is set in indirect register X'09'.

The transmit clock and the transmit data requests made to the bit layer are gated by CTS in the FESH, in order to perform data transmission only when CTS is ON (refer to "Modem-Out Management" on page 5-21 and "Modem Retrain" on page 5-21 for explanation). However, this gating can be disabled by the microcode.

CTS drop reporting can be controlled by the microcode.

One timer step value is available:

- 400 ms step

If the timer value is zero (default value), CTS drop is reported without delay.

If this value is not zero, the hardware handles CTS drop according to the timer value. If the timer expires (25.2 s maximum) before CTS drops, a modem-in change is reported.

X.21 Modem-in Lead State Confirmation

In X.21, the modem-in microcode layer immediately reports to the microcode any change of the X.21 steady states and performs, in parallel, the confirmation of the following steady states which are detected by the FESH hardware:

| | I | R |
|----------------------------|-----|-----------------------------------|
| Clear | OFF | 0 |
| Controlled Not Ready (CNR) | OFF | 0/1 (16-bit time) |
| Controlled Ready (CR) | OFF | 1 |
| Ready for Data (RD) | ON | X (don't care) |
| Local Wrap (LW) | OFF | X'0F' data received (16-bit time) |
| Remote Wrap (RW) | OFF | X'33' data received (16-bit time) |

To confirm any state, the hardware verifies that the state remains unchanged during a count of 16-bit times.

When a state is confirmed, a modem-in change is reported to the microcode with the indication steady state ON.

DCE Clock Failure

The hardware monitors the receive and transmit DCE clocks of each line to detect clock failures.

If one or both DCE clocks disappear during a period of time exceeding 2.5 s, the FESH reports a clock failure to the microcode in indirect register X'11' (no level 2 interrupt is sent to the CSP).

Modem-Out Management

To manage the DCE output leads, the microcode prepares a CW in CSP storage and starts the process by setting the send modem-out command to the FESH.

On reception of this command, the hardware activates the output leads according to the contents of the CW.

The microcode can, at any time, read the modem-out lead register which contains the output leads activated by the hardware.

Modem Retrain

The term 'modem retrain' is used here to mean the temporary inability of a modem to respond to requests from the attached business machine (DTE). On V.35 lines, this typically occurs when two modems lose carrier synchronization. While 'retraining' the carrier, they are unable to provide service.

On X.21 lines, a 'retrain' means that the network or DTE places the line under test and during this time, the line is unable to provide service.

V.35 Modem Retrain

'Modem retrain' is detected on V.35 lines as a drop of clear to send (CTS). When this occurs:

1. The FESH starts a timer derived from the set mode enable time out value.
2. The FESH continues any transmission until the end of message is reached.
3. If a transmission is in progress when CTS drops, and the retrain timer has not expired, the following ending status is sent to the CCU when the transmission completes:
 - SCF = X'22' (underrun/data transmitted)
 - SCF = X'20' (underrun)
 - SES = X'80' (modem retrain)
 - LCS = X'00'
4. If CTS does not recover, and the retrain timer expires while a transmission is in progress, the ending status sent to the CCU is:
 - SCF bit 3 = 1 (modem check)
 - LCS = X'E2' (CTS dropped)

If CTS does not recover, but there is no transmission in progress, the error will be detected and reported on the next transmit command as:

- SCF bit 3 = 1 (modem check)
 - LCS = X'F2' (CTS failed to come up)
5. Data reception is not affected.

X.21 Modem Retrain

On X.21 lines, modem retrain is entered when a DCE uncontrolled not ready or DCE controlled not ready steady state is detected. When this occurs:

1. The CSP microcode starts a 20 second timer.
2. The FESH continues any transmission until the end of message is reached.
3. If a transmission is in progress when the retrain starts, the following ending status is sent to the CCU when the transmission completes:
 - SCF = X'22' (underrun/data transmitted)
 - SCF = X'20' (underrun)
 - SES = X'80' (modem retrain)
 - LCS = X'00'
4. If data reception is in progress when the retrain starts, the incoming frame is flushed (to avoid filling the NCP buffers) and the receive command is ended with the following status:
 - SCF = X'04' (end of message)
 - SES = X'10' (data check)
 - LCS = X'00'
5. If the DCE does not return to a 'ready' or 'ready for data transfer' state before the time out expires, the following ending status is sent to the CCU:
 - SCF bit 3 = 1 (modem check)
 - LCS = X'EE'

Time Out Values

The following is a list of the various timer values used by the HSS along with their sources:

| | |
|---------------------------|---|
| Enable time out | Taken from the set mode data, it is used during enable command execution and also during transmit command execution (to monitor CTS, if it is down). |
| Disable time out | Taken from the set mode data, it is used during disable command execution to allow the modem, time to respond to the changes on the modem-out leads. |
| Reply time out | Taken from the set mode data, it is used during receive command execution to monitor for a reply to a transmission. |
| DSR confirmation | A MOSS init value, it confirms a steady state on DSR for the stated period. |
| X.21 modem retrain | A fixed 20-second value. |
| V.35 modem retrain | The enable time out value is used if it is less than or equal to 25.2 seconds. A retrain timer of 25.2 seconds is forced if the enable time out exceeds this value. If the enable time out is not a multiple of 400 ms, the modem retrain timer is rounded to the next 400 ms increment. For example: |

| Enable time out | Resulting retrain value |
|------------------------|--------------------------------|
| 0 ms | 0 ms |
| 100 ms | 400 ms |
| 400 ms | 400 ms |
| 25.2 s | 25.2 s |
| 40 s | 25.2 s |

Customization Parameters

Using the CDF Display/Update option 1 at the MOSS console, the CE or the customer can have access to the HSS parameters. The CE or the customer can choose two parameters: the DMA size (see note 3 hereunder) and the DSR integration timer.

The DMA size (see note 3 hereunder) is a function of the number of HSS line adapters installed. A DMA size of 64 is correct for one HSS line adapter installed.

The DSR integration timer is a function of the manufacturer's equipment attached to the network. Normally 16 ms is adequate. However, the CE or the customer must read the manufacturer's installation guide to determine if 16 ms can be used.

The following parameters are default values for the HSS port:

- DMA size (see note 3 hereunder) (2 to 64, even values only): 64
- Error sequence: 7FFF
- DSR integration timer (0, 1, 4, 16, 32, 64, 128, 256): 16

Notes:

1. The DMA size and error sequence are valid for attachment to the X.21 or V.35 interface for the SDLC protocol.
2. The integration timers are valid only for the V.35 interface.
3. DMA size (length of burst. Depending on the 3745 microcode level, this field may no longer be displayed and modifiable. Its default values are set as follows:
64 for receive operations
253 for transmit operations.

Error Detection and Reporting

Program/Hardware Checks

In addition to the program/hardware errors reported in the command status via level 2 interrupts, the CCU may be notified by a CCU level 1 interrupt that a program or hardware check occurred.

To obtain the error information, the control program issues a get error status instruction, which transfers a two-byte error status to the CCU.

The control program also resets the check and the interrupt, and performs the recovery actions. The following conditions may cause a level 1 program or hardware check:

1. CCU/HSS problems:
 - IOH/IOHI instruction not supported.
 - IOH/IOHI rejected because there is already an outstanding command on the interconnection. For example, a second transmit command has been sent while a transmit command is already outstanding.

- IOH/IOHI rejected because a set mode command has not yet been received for that line.
- Abnormal conditions detected during I/O operations on the IOC bus. These errors may be detected by the CCU or by the HSS. Errors are related to CCU storage and address checks, invalid sequences, and invalid timed-out IOH/IOHI instructions.

2. HSS problems:

- Invalid interrupts.
- Microcode-detected program failures. (These set the microcode check bit in the error status and cause the NCP to issue a get microcode check instruction.)
- CCU level 2 interrupt stack overflow.
- CSP or FESH hardware check (for example parity or address check).

After receiving a level 1 interrupt from the FESH, the CSP microcode, builds the error status, freezes the FESH, and waits for the get error status IOH.

Once the get error status has been answered, the CSP enters the disconnect/stop environment and ignores all IOH instructions generated by the NCP. Re-IML of the CSP microcode is required to return to an operational state. The only exception to this sequence of events is a level 1 interrupt caused by a command reject.

Refer to "Error Status" on page 5-29 for the error status description.

Hardware Error Detection and Reporting

Two types of error:

- DMA and modem interface errors which raise the level 2 interrupt to the CSP.
- Errors which raise the level 0 interrupt to the CSP.

Internal Box Error (IBE) Reporting

The internal box errors generate box event records (BERs). For details on BERs, refer to the "Box Event Records (BER)" Chapter.

The IBEs can be divided into three categories:

1. CSP and FESH internal errors or events (similar to the errors defined for the CSP/FES in the LSS):
 - Adapter interconnection check
 - CSP interconnection error
 - FESH failing to answer
 - No interrupt from FESH
 - Invalid interrupt from FESH
 - Command rejected
 - Trace already active (event, not error)
 - FESH internal error
 - Local attach clock failure
 - AIO error
 - Line not accessible (one of the two possible lines is already active)

2. DMA errors detected by the FESH:

- DMA parity error during write or read
- DMA time out during write or read
- DMA burst count error
- DMA interconnection errors for improper DMA tag sequence.

3. Errors detected in the SCTL card:

- Storage internal error
- SCTL internal error
- DMA internal error
- DMA logical error
- DMA storage protect/address exception
- DMA interconnection error in read or write (a)
- DMA parity check. (b)

Notes:

1. The following errors can occur concurrently:
 - a and b
2. All the above-listed errors are reported to the NCP via a level 2 interrupt and associated status area as an LCS and ELCS code (Refer to "Line Communication Status (LCS)" on page 5-31 and "Extended Line Communication Status (ELCS) (Initial Status = B'110') for HSS" on page 5-35 for code description).
3. The SCTL errors and the FESH DMA interconnection errors are mutually exclusive. There is no double-reporting of errors.

DMA Interconnection Errors Detected by FESH (Register X'10')

DMA Tag Sequence

The FESH circuitry monitors the sequence of the DMA interconnection signals from the SCTL card.

An error is reported when the tag sequence does not occur properly.

DMA Data Bus Parity Checker

This parity checker verifies the validity of the data received/sent, from/to the DMA data bus byte 0 and byte 1 by the FESH.

DMA Time Out

One hardware timer is implemented to detect possible time out conditions on the DMA bus.

The duration of the timer is in the range of 100 ms to cover a complete transfer operation on the DMA bus.

DMA Burst Count Checker

This checker verifies that the transfer is satisfactorily completed on the DMA bus when the burst count in the FESH reaches zero

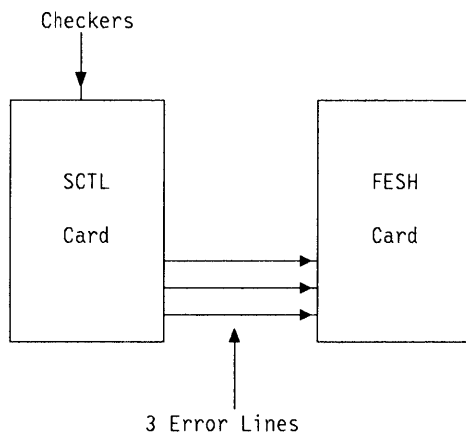
SCTL Card Detected Errors Reported By FESH

The SCTL card has internal checkers which detect the following error conditions which may occur during a DMA transfer initiated by an HSS (Refer to the figure "Line Error Hexadecimal Code" next).

| Line Error Hexadecimal Code | SCTL Error Conditions | | | | | |
|-----------------------------|------------------------|---|---|---|---|---|
| | a | b | c | d | e | f |
| 0 | Normal mode (no error) | | | | | |
| 1 | x | | | | | |
| 2 | | x | | | | |
| 3 | | | x | | | |
| 4 | | | | x | | |
| 5 | | | | | x | |
| 6 | | | | | | x |
| 7 | | | | | | |

Figure 5-6. Line Error Hexadecimal Code

- SCTL error detection:
 - a. DMA internal error (SCTL detection code 001)
 - b. DMA logical error (SCTL detection code 010)
 - c. DMA storage protect/address exception error (SCTL detection code 011)
 - d. Storage unrecoverable error or control error (SCTL detection code 100)
 - e. DMA interconnection error (SCTL detection code 101)
 - f. DMA parity check



Reporting

Reporting DMA errors is done by issuing a level 2 interrupt to the CSP. The nature of the error is set into an LCS/ELCS (Refer to "Line Communication Status (LCS)" on page 5-31 and "Extended Line Communication Status (ELCS) (Initial Status = B'110') for HSS" on page 5-35 for code description).

When any of the above checkers becomes active:

1. The hardware:

- Stores the corresponding error condition in an error register X'10' and X'11'.
- Interrupts the CSP microcode.

2. The CSP microcode

- Stops the transmit and receive operations in process.
- In case of transmit, puts the transmit data line at mark.
- In case of receive, stops the receive command and modem monitoring.

DMA Bus Errors Reported by the FESH

They are reported by the FESH through a level 2 interrupt and then both interface are disabled by the microcode.

The CSP microcode fills the LCS field of the PSA status with a status byte telling the reason for the error (Refer to "Line Communication Status (LCS)" on page 5-31 and "Extended Line Communication Status (ELCS) (Initial Status = B'110') for HSS" on page 5-35 for code description).

The microcode then raises CCU level 2 interrupt.

Line interfaces are started again by the CSP microcode when the NCP sends the proper SDLC command sequence.

CSP Interconnection Errors

The CSP communicates with the FESH through the external registers located in the FESH (register range X'0D' to X'17').

The FESH completes the operation with the 'acknowledge' signal to the CSP if no error conditions were detected.

The FESH monitors the CSP interconnection for the following errors:

- Interconnection error signal from the CSP
- Bidirectional cycle steal data bus parity error
- External register address and select out parity error
- Data out odd parity error during an external register write operation.
- External register address invalid.

If an error occurs in the external register address because of a parity error or because the external register does not exist in the FESH, the 'acknowledge' signal is not sent to the CSP.

Also, if the data bus parity is incorrect during an external register write, the 'acknowledge' signal is not sent to the CSP.

When 'acknowledge' is not returned to the CSP by the FESH, the CSP sets the adapter interconnection check bit ON (external register X'03' bit 6 = 1) and terminates the operation.

The FESH does not report any error condition.

Parity errors occurring on the cycle steal interconnection can be detected by the FESH or by the CSP.

If the FESH detects a parity error on the data bus during a cycle steal write, the FESH sets a level 2 interrupt to the CSP with the CSP interconnection error bit ON (external register X'10' bit 3 = 1) after completing the operation.

The parity checking on the cycle steal address bus and the CSP data bus during a cycle steal or external register read operation is performed by the CSP.

When the CSP detects a parity error, the CSP sets the adapter interconnection check in CSP register X'03' and activates the 'cycle steal error' line.

When the FESH detects this signal, the cycle steal operation ceases and the FESH activates a level 2 interrupt to the CSP.

The CSP interconnection error bit is set ON in FESH external register X'10'.

Detection of this error causes a level 2 interrupt to the CSP.

If an NCP transmit or receive operation is in progress, it continues until the CSP microcode stops reception of data for the receive command, or stops transmission of data and sets the transmission line to mark.

FESH Internal Checkers

Data Parity Checkers

All the microcode (DMA layer, CSP layer, bit-layer, byte-layer) and data are checked for parity when the FESH internal buffers are read or written.

NCP Buffer Handling Logic Checker

In order to check that the hardware logic which calculates the NCP buffer data area address from the NCP buffer prefix is working properly, the transmit and receive byte layer microcodes perform a predetermined calculation during inactivity periods.

If there is a mismatch between the result of the calculation and the predetermined result, the FESH hardware reports an internal error condition.

Reporting

When any of the above checkers becomes active:

- The FESH:
 - Stores the corresponding error condition in an error register.
 - Interrupts the CSP microcode at level 0.
- The CSP microcode:
 - Stops the transmit and receive operations in process.
 - In case of transmit, puts the transmit data line at mark.
 - In case of receive, stops the phase monitor.

Line Interface Check

A driver check function is implemented on the line interfaces of the FESH (V.35 / X.21).

When a driver check is detected, the hardware:

- Sets the driver check bit in the transmission status register.
- Interrupts the CSP.

No other action (no line interface disabling) is taken by the hardware.

Error Status

Error Status Byte 0

| Bit | Type 1 | Type 2 | Type 3 |
|-----------|-----------------|-------------------|------------------------|
| x... .. | R/W (IOH) | R/W (AIO) | Always ON |
| .x.. .. | I/O bus check | I/O bus check | Invalid lev.0 interr. |
| ..x. | Not used | Cycle steal grant | Invalid lev.1 interr. |
| ...x | I/O bus tag I/O | I/O bus tag I/O | Invalid lev.2 interr. |
| x... | Halt | Halt | Microcode check |
|x.. | TA | Not used | CS/CCU L2 stack overf. |
|x. | TD | TD | Reject: command on cmd |
|x | Not used | Not used | Disconnect state |

Error Status Byte 1

| Bit | Type 1 | Type 2 | Type 3 |
|-----------|-------------------|------------------------------|----------------------------|
| x... .. | TA select | Not used | Command reject |
| .x.. .. | Not used | Cycle steal select | Invalid output IOH type |
| ..x. | Not used | Not used | } See note below |
| ...x | Not used | Line interface address bit 0 | |
| x... | Not used | Line interface address bit 1 | |
|x.. | Not used | Line interface address bit 2 | |
|x. | Not used | Line interface address bit 3 | |
|x | Invalid input IOH | Line interface address bit 4 | } Adapter interconn. check |
|x | | | |

Note: Next comes the decoding of bits 0 to 7 when command reject occurs.

| Bit | Normal Command Reject | Trace Command Reject | Invalid Output IOH |
|---|--|--|--|
| x... .. .x...x.x x...x..x.x | Command reject Always OFF } Line interface address (0 to 3F) | Command reject Always ON Not used Not used } Slot number (0 to F) | Always OFF Invalid output IOH Not used } Line interface address (0 to 1F) |

Four types of error may be reported:

- Type 1** Error detected by the CCU during PIO. A halt is send to the CSP, which results in a CCU or MOSS level 1 interrupt.
- Type 2** Error detected by the CCU during AIO. A halt is send to the CSP, which results in a CCU or MOSS level 1 interrupt.
- Type 3** Internal logical errors detected by the CSP microcode. A CCU level 1 or MOSS level 4 interrupt is set.
- Hard Stop** A CSP microprocessor check has been encountered. The CSP hardware responds with the error status.

The following tables shows the detailed responses that may be presented to a get error status command:

Hard Stop Error Status (Detected by CSP Hardware)

Byte 0

| Bit | Meaning |
|-----------------|---------------------------------------|
| * * * * . . . | Not used |
| x . . | Control store data check |
| x . | LSR or external register parity check |
| x | Internal check |

Byte 1

| Bit | Meaning |
|-----------------|-----------------------------------|
| x | Unexpected adapter acknowledgment |
| . x | Control store write data check |
| . . x | Processor check |
| . . . x | External register address check |
| x . . . | Control store address check |
| x . . | LSR address check |
| * * | Not used |

Miscellaneous Status Fields

Three status fields, the status control field (SCF), the secondary status field (SES), and the line communication status field (LCS), have so many different meanings, dependant on the type of line control used, that they are grouped here for easy reference.

Status Control Field (SCF) Bit Definition

The bits of the SCF byte describe the progress of the operation being executed.

| Bit | Meaning |
|-------------------|---------------------------|
| X | Halt/abort |
| . X | Service request |
| . . X | Scanner underrun/overrun |
| . . . X | Modem check |
| X | Data stored |
| X . . | End of message (EOM) |
| X . | Data transmitted occurred |
| X | Receive sequence |

Secondary Status Field (SES) Bit Definition

The bits of the SES byte identify errors encountered during the execution of the command.

When any bit is ON in this byte, the service request bit (bit 1) in the SCF must be OFF, except for 'modem retrain' in NCP BSC.

| Bit | Meaning |
|-------------------|--|
| X | Modem retrain |
| . X | Idle detection (SDLC) or format exception (NCP BSC, EP BSC) |
| . . X | LPDA reply received, but TI failed to come up /transient error |
| . . . X | Data check (SDLC, NCP BSC, EP BSC) |
| X | Flag off boundary (SDLC) or bad PAD (NCP BSC) |
| X . . | In phase (EP BSC)/TI ON (NCP BSC & SDLC) |
| X . | DLE error (NCP BSC) |
| X | Early flag (SDLC)/length check (NCP BSC) |

Line Communication Status (LCS)

The bits of the LCS byte contain statuses applicable to the line being serviced. The byte is divided into three fields as shown below:

| | | | | | | | | |
|------|-----|---|---|-----|---|---|---|---|
| Bits | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | ISF | | | FSF | | | F | |

ISF = Initial status field

FSF = Final status field

F = Leading graphics / timeout during X.21 clear

The indicator field (bit 7) specifies whether or not, leading graphics were the first characters received.

Initial Status Field (ISF) Bit Definition

The ISF (LCS bits 0 - 1) indicates essentially the type of line control that is used. The ISF is decoded as follow:

NCP BSC Receive Only: See paragraphe "Initial Status = B'0xx'" on page 5-33 for more explanation.

| ISF | | | FSF | | | | F | Meaning |
|-----|---|---|-----|---|---|---|---|---|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | |
| 0 | 0 | 0 | . | . | . | . | . | Control mode, no text received (receive only) |
| 0 | 0 | 1 | . | . | . | . | . | Text mode , STX is first character |
| 0 | 1 | 0 | . | . | . | . | . | Transparent text mode, DLE STX are first char |
| 0 | 1 | 1 | . | . | . | . | . | Header mode, SOH is first character |

Special: See paragraphe "Initial Status = B'100' (Special)" on page 5-33 for more explanation.

| ISF | | | FSF | | | | F | Meaning |
|-----|---|---|-----|---|---|---|---|----------------|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | |
| 1 | 0 | 0 | . | . | . | . | . | Special status |

Errors: See paragraphe "Initial Status = B'110' (Internal Box Error)" on page 5-34 and paragraphe "Initial Status = B'111' (Hardware Error)" on page 5-36 for more explanation.

| ISF | | | FSF | | | | F | Meaning |
|-----|---|---|-----|---|---|---|---|--------------------|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | |
| 1 | 1 | 0 | . | . | . | . | . | Internal box error |
| 1 | 1 | 1 | . | . | . | . | . | Hardware error |

Final Status Field (FSF)

The FSF (LCS bits 3 - 6) gives further status information. The encoding is based upon the ISF configuration and is defined as follows:

Initial Status = B'0xx'

| ISF | FSF | F | |
|-------|---------|---|---|
| 0 1 2 | 3 4 5 6 | 7 | Meaning |
| 0 x x | 0 0 0 0 | x | Timeout occurred after reception has begun and ISF is not 000 |
| 0 x x | 0 0 1 1 | x | ENQ received |
| 0 x x | 0 1 0 0 | x | EOT received |
| 0 x x | 0 1 0 1 | x | DLE/xxx was received (xxx=any valid second character) |
| 0 x x | 0 1 1 0 | x | Wrong ACK received |
| 0 x x | 0 1 1 1 | x | NAK received |
| 0 x x | 1 0 0 1 | x | ETX received |
| 0 x x | 1 0 1 0 | x | ETB received |
| 0 x x | 1 1 0 1 | x | RVI received |
| 0 x x | 1 1 1 0 | x | Positive ACK (0 or 1) received |
| 0 x x | 1 1 1 1 | x | WACK received |

Initial Status = B'100' (Special)

| ISF | FSF | F | |
|-------|---------|---|--|
| 0 1 2 | 3 4 5 6 | 7 | Meaning |
| 1 0 0 | 0 0 0 0 | x | Timeout (nothing received); ACR, COS, DLO, or PND failed to drop; X.21 timeout on ready for data |
| 1 0 0 | 0 0 0 1 | x | Ending condition on start/stop |
| 1 0 0 | 0 0 1 0 | x | X.21 timeout during clear |
| 1 0 0 | 0 0 1 1 | x | 386x/58xx test control active/X.21 timeout on proceed to select |
| 1 0 0 | 0 1 0 0 | x | DLE-EOT disconnect sequence received |
| 1 0 0 | 0 1 0 1 | x | Lost data |
| 1 0 0 | 0 1 1 0 | x | Poll entry too long |
| 1 0 0 | 1 1 0 0 | x | EOT transmitted |
| 1 0 0 | 1 1 0 1 | x | X.21 call progress signal (CPS) error |
| 1 0 0 | 1 1 1 0 | x | Disconnected/X.21 DCE clear received |
| 1 0 0 | 1 1 1 1 | x | Connected |

Notes:

1. When a special status occurs, the line is set to the disable state.
2. For X.21, if 'DTE clear' or 'DCE clear' confirmation is required, the 'X.21 timeout during clear' flag (bit 7) is added to the final status to indicate the result of the clear operation. Bit 7 is set to zero if the clear was successful, and to one if it was not.

Initial Status = B'110' (Internal Box Error)

| ISF | FSF | F | |
|-------|---------|---|------------------------------------|
| 0 1 2 | 3 4 5 6 | 7 | Meaning |
| 1 1 0 | 0 0 0 0 | x | AIO error |
| 1 1 0 | 0 0 0 1 | x | Adapter check |
| 1 1 0 | 0 0 1 0 | x | Scanner interconnection error |
| 1 1 0 | 0 0 1 1 | x | Scanner failed to answer |
| 1 1 0 | 0 1 0 0 | x | Scanner internal error |
| 1 1 0 | 0 1 0 1 | x | Multiplex failure |
| 1 1 0 | 0 1 1 0 | x | Transient counter overflow |
| 1 1 0 | 0 1 1 1 | x | LIC / ICF error |
| 1 1 0 | 1 0 0 0 | x | No interrupt from scanner |
| 1 1 0 | 1 0 0 1 | x | Command rejected |
| 1 1 0 | 1 0 1 0 | x | Trace already active |
| 1 1 0 | 1 0 1 1 | x | Scanner error reporting path check |
| 1 1 0 | 1 1 0 0 | x | Invalid level 2 interrupt |
| 1 1 0 | 1 1 0 1 | x | Modem already in test mode |
| 1 1 0 | 1 1 1 1 | x | Line not accessible |

Notes:

1. For NCP operations, the line is set to the disable state.
2. For NCP operations on duplex lines, the command on the failed interface is ended; the LCS indicates the cause of the error, and a level 2 interrupt is raised to the CCU. The command on the other interface is cleared; no ending status is set, and no interrupt is raised to the CCU.
3. For EP operations, the line is set to the NO-OP state.
4. After hardware error, the only commands accepted for that line is 'enable', 'monitor incoming call', or 'dial' (if autocal interface).

Initial Status = B'110' (Internal Box Error HSS)

The code is the value of the LCS bits 0 to 7 (fields ISF, FSF, F).

Code Description

- | | |
|-----------|--|
| C0 | AIO error indicates a hardware error during an adapter-initiated operation (cycle-steal). |
| C2 | Adapter interconnection check indicates a FESH hardware error. |
| C4 | CSP interconnection error indicates a CSP/FESH interconnection hardware error. |
| C6 | FESH failed to answer to a microprogram-initiated operation. |
| C8 | FESH internal error indicates hardware error in the FESH detected by the FESH itself. |
| CE | Local attach clock failure (F5 only). This is returned as an F5 command status if the local attach clock has failed while in use. |
| D0 | No interrupt from FESH indicates that the FESH has failed to respond to a microcode request. |
| D2 | Command rejected indicates that the command issued by the control program has been rejected by the CSP. |
| D4 | Trace already active indicates that the SIT is already running on this interface. |

- D8** Invalid FESH level 2 interrupt indicates that an unexpected CSP level 2 interrupt from the FESH has occurred.
- DC** ELCS is valid.
- DE** Line not accessible indicates that one of the two possible lines is already active and a set mode is received for the other line.

Extended Line Communication Status (ELCS) (Initial Status=B'110') for HSS

When the LCS = X'DC', additional statuses, as on internal box errors, may be found in byte 4 of the status area. These additional statuses are:

Code Description

- 02 (a)** SCTL/DMA internal error
- 04 (e)** SCTL/DMA interconnection error
- 06** Combination of (f) and (g)
- 08 (3)** DMA time out on write
- 0A (1)** DMA interconnection error in write
- 10 (c)** SCTL/DMA storage protect/address exception
- 12 (b)** SCTL/DMA logical error
- 14 (f)** DMSW main bus parity check
- 16** Combination of (f) and (h)
- 18 (4)** DMA time out on read
- 1A (2)** DMA interconnection error on read
- 22 (d)** Storage unrecoverable error/SCTL internal error
- 24** Combination of (e) and (f)
- 28 (g)** DMSW parity check on primary/secondary bus
- 2A (5)** DMA bus driver fault
- 34** Combination of (e), (f) and (g)
- 3A (6)** DMA burst count error
- 44** Combination of (2), (e), (f) and (g)
- 4A (h)** DMSW driver fault
- 5A** Combination of (1), (e), (f), and (g)
- 6A** Combination of (2) and (g)
- 7A** Combination of (2) and (h)
- 9A** Combination of (5), (e), (f) and (g)
- AA** Combination of (6) with any of (a) through (h)
- BA** Combination of (1) through (6) with any of (a) through (h) which are not listed above.

Initial Status = B'111' (Hardware Error)

Detailed descriptions of hardware errors:

| ISF | | | FSF | | | | F | Meaning |
|-----|---|---|-----|---|---|---|---|--|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | x | CTS dropped during command/modem retrain |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | x | RLSD failed to drop on disable command (not used by NCP) |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | x | DSR dropped during command/ external clock error (F5) |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | x | TI/CTS failed to come up |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | x | DSR failed to come up |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | x | No cable installed or wrong cable |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | x | TI/DSR and/or CTS failed to drop (on disable and transmit data commands on half-duplex lines without duplex facilities |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | x | X.21 disconnected DCE clear receive, with or without timeout |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | x | Autocall check |

Notes:

1. For NCP operations, the line is set to the disable state.
2. For NCP operations on duplex lines, the command on the failed interface is ended; the LCS indicates the cause of the error, and a level 2 interrupt is raised to the CCU. The command on the other interface is cleared; no ending status is set, and no interrupt is raised to the CCU.
3. For EP operations, the line is set to the NO-OP state.
4. After hardware error, the only commands accepted for that line is 'enable', 'monitor incoming call', or 'dial' (if autocall interface).

Initial Status = B'111' (Hardware Error HSS)

The code is the value of the LCS bits 0 to 7 (fields ISF, FSF, F).

Code Description

| | |
|----|---|
| E2 | CTS dropped indicates clear to send failed during transmission. |
| EE | V.35 DSR dropped/X.21 DCE not ready, or external clock failure indicates that DSR failed for V.35 connection, or that the DCE is not ready for an X.21 connection in response to an F5 command. |
| F2 | CTS failed to come up. Clear to send did not rise after request to send was set. |
| F4 | DSR failed to come up. Data set ready did not rise after data terminal ready was set. |
| F6 | No cable installed. There is no cable connected to the modem. |
| F8 | DSR/CTS failed to drop on a disable. On a disable command, data set ready or clear to send did not drop. |
| FA | X21 DCE not ready. An X.21 DCE not ready state was detected. |

Note: In all cases of internal box errors and hardware errors, the line is disabled by the CSP. The command on the failed interface is ended (LCS contains the error and a level 2 interrupt request is raised to the CCU).

The command on the other interface is cleared without any ending status or level 2 interrupt request to the CCU.

After such an error the only commands that are accepted on the line are 'set mode' or 'enable'.

Diagnostic Facilities

Refer to the *3745 Diagnostic Descriptions* manual, SY33-2076, for more details.

Problem Determination Aid

The following tools are provided to help define which area is failing:

1. Scanner interface trace (SIT) and checkpoint trace
2. Line interface display (LID).
3. LSS functions from the MOSS service menu (Refer to the *Service Functions* manual, SY33-2069).

Microcode Service Aid

The FESH registers, the microcode RAM locations and the external data control RAM locations can be accessed, using the following facilities (Refer to the *Service Functions* manual, SY33-2069, and *Advanced Operations Guide* manual, SA33-0097):

1. Alter/display
2. CSP address compare
3. CSP dumps.

These facilities, invoked from the operator console, help in analyzing/modifying the contents of the HSS storage and registers (CSP and FESH).

Programming Support for Problem Determination

It includes, as for LSS microcode:

1. Error detection
2. Error collection
3. Error reporting.

Types of error tracked are:

- CSP/IOC bus interconnection errors
- CSP internal errors
- CSP/FESH interconnection errors
- DMA/SCTL errors
- FESH errors
- FESH-to-line interface errors.

NCP Buffer Prefix Validity Checking in Receive

This test is performed by the microcode for the first buffer only, by using the parameters coming from the PSA.

Problem Isolation and Network Management

External Wrap Facility

After a power-ON reset, the interface defaults to the 245.76 kbps clock speed if the cable ID bits specify local attach.

The interface is neither selected nor enabled after a power-ON reset.

A different clock selection can be made by the NCP at set mode time with indirect register X'11'.

The FESH also provides an external interface wrap facility by inserting a wrap plug at the tail gate connection. Commands initiating the wrap are sent from the MOSS console.

Notes:

1. The wrap plugs are described in the *External Cable Reference* manual, SY33-2075.
2. The procedure to perform a wrap test at the tail gate, using a wrap plug, is described in the *IBM Maintenance Information Procedures (MIP)*.

The cable ID bits are changed by the wrap plug. The X.21 or V.35 signals are wrapped as specified by the interface ID bit (indirect register X'06' bit 1) and the clock defaulted to the clock speed selected by the NCP at set mode during a wrap.

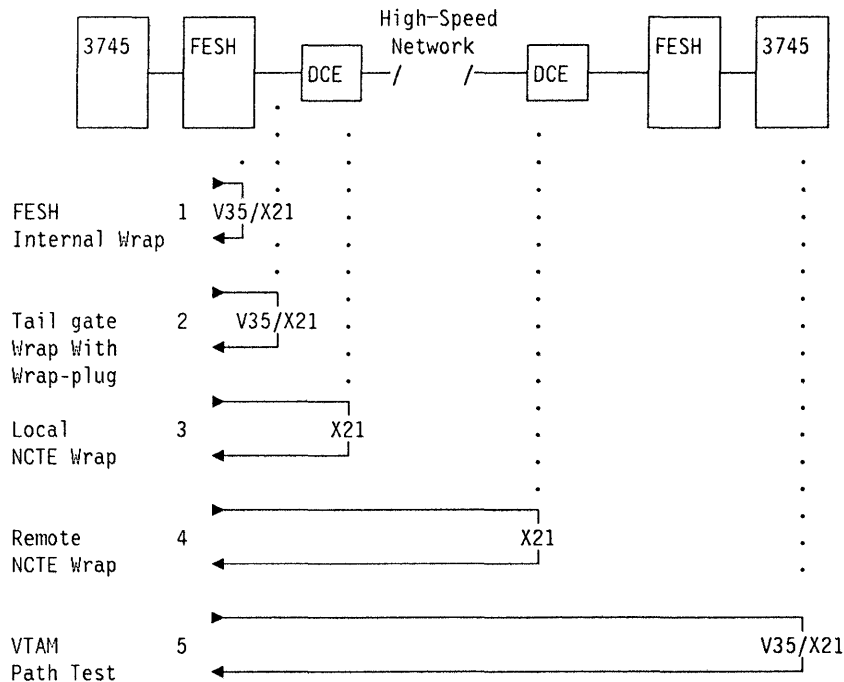
The external clock is under microcode control as specified by external register X'11'.

Wrap Mode at DCE Level

The wrap is started from the MOSS console.

The diagnostics can perform a wrap function from the transmit to the receive interface on the logic side of the line drivers/receivers, at a speed of 1.966 Mbps or at a speed controlled by the diagnostics.

The following figure illustrates the problem determination and testing configuration for V.35/X.21 network attachment.



Note: Test is also available from the right hand side.

Figure 5-7. V.35/X.21 Configuration Showing Wrap Tests or Loop Tests 1 to 5

Manual V.35/X.21 Wrap or Loop Tests

The manual wrap or loop tests are initiated from the MOSS console. (Loop test 3 and 4 are for X.21 only).

Internal Wrap

Or **Loop Test 1** checks the ability of the HSS to transmit and receive, up to the output of the FESH card.

Tail Gate Wrap

Or **Loop Test 2** in addition to loop test 1 checks the cables between the FESH card and the tail gate. A wrap plug is required.

Local NCTE Wrap Test

Or **Loop Test 3** checks the transmit and receive ability of the 3745, up to the first network communication terminal equipment (NCTE).

Remote NCTE Wrap Test

Or **Loop Test 4** checks the transmit and receive ability of the 3745, up to the second NCTE and including the communication media.

VTAM Path Test

Or **Loop Test 5** checks the transmit and receive ability of the two controllers.

Communication Interfaces

The HSS interfaces external high-speed data links to either the 3745 or the 3725:

- Remotely via DCE attachment
- Locally via direct attachment to another HSS or LIC type 3/4 on the 3725.

The physical and logical interfaces are either:

- CCITT V.35 or,
- CCITT X.21 leased (including French Transfix).

The high-speed data links access the HSS directly through the FESH via the tail gate without a LIC card.

FESH-DCE Interface

The FESH is physically able to support two interfaces. However, only one interface can be active and communicating, while the other interface is disabled.

The NCP controls the enabling and disabling of each interface.

On reception of the line address activation from the NCP, the microcode sets the corresponding bit in the FESH to select the proper fan-out.

To determine which interface was selected by the hardware (V.35 or X.21) on the selected fan-out, the microcode reads the cable ID in the FESH.

The FESH is also capable of supporting different electrical interfaces.

Each of the two physical interfaces can independently support the following interfaces to the network communication terminal equipment (NCTE):

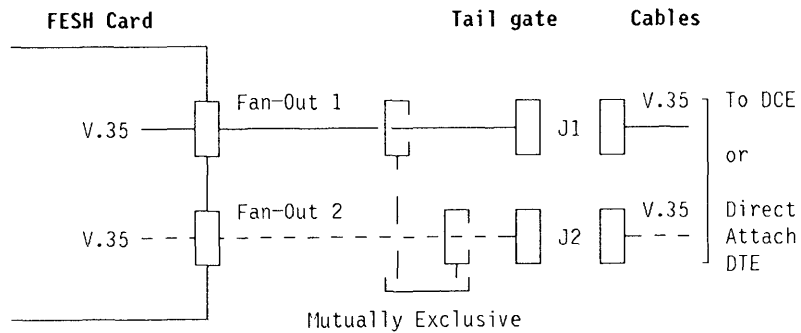
V.35
X.21

Any combination of physical interfaces are supported. The physical interface is identified by cable ID signals in the cable. The following combinations are possible:

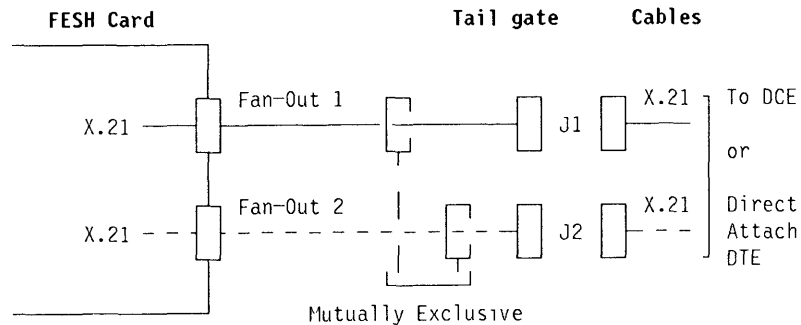
- Two V.35 interfaces
- Two X 21 interfaces
- One V.35 and one X.21 interface

NOTE: Before unplugging the cable from the tail gate or DCE, ensure that the line is not active by disabling the interface, using VTAM commands. Failure to perform this step can cause an FESH adapter check.

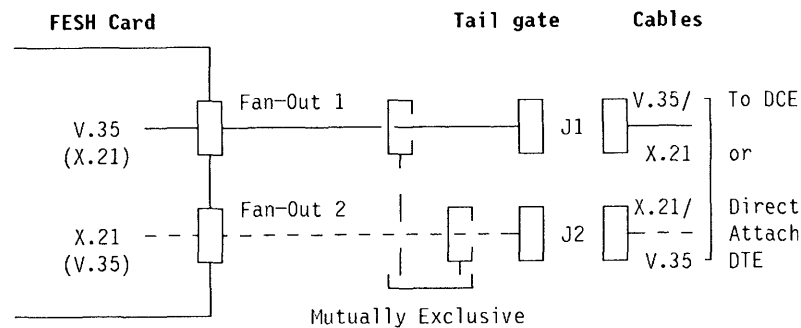
Two V.35 Cables Connected (Example)



Two X.21 Cables Connected (Example)



One V.35 and One X.21 Cables Connected (Example)



The FESH supports the CCITT standard V.35 interface. All interface signals conform to the electrical specifications as stated in the various CCITT standards.

X.21 Interface

The HSS supports the 1987 CCITT X.21 standard for transmitting data at speeds up to 2.048 Mbps.

Cable Diagrams

DCE interface signals exit the FESH using two top card connectors. one for interface 1 and one for interface 2.

Each interface cable contains the V.35, X.21, and cable ID signals to the 3745 tail gate.

All balanced signals use twisted pairs from the tail gate to top card connector.

Unbalanced signals use a twisted pair of wires with one signal wire and one ground wire to eliminate any noise problems.

The **external cable** attached to the tail gate determines the physical interface supported, using the cable ID bits and the V.35 or X.21 identifier.

The FESH hardware gates the appropriate drivers and receivers to the network adapters.

Cable Length Limitations

For cable length limitations, refer to *External Cable References*, SY33-2075.

Clocking

Because of the high transmission speeds and propagation delays in the cable, the transmit clock received from the DCE or NCTE is re-driven and sent to the DCE or NCTE in synchronization with the data.

Local Attachment

The HSS supports direct attachment (no DCE) with another HSS using the X.21 or V.35 interface.

When directly connected together, one FESH is designated as local attach by the cable ID bits and automatically provides the receive clock to the other FESH.

The other FESH attaches in DCE mode with the external clock supplied by the local attach HSS. Three attachment speeds are offered as specified in indirect register X'11'.

1. 1.8432 Mbps
2. 1.47456 Mbps
3. 245.76 kbps

Chapter 6. The Token-Ring Subsystem

| | |
|---|------|
| The TRSS in 3745 Data Flow | 6-2 |
| Token-Ring Network | 6-3 |
| IBM Token-Ring Network | 6-3 |
| Cabling System (Ring) | 6-4 |
| Token-Ring Adapter | 6-4 |
| Access Protocol | 6-6 |
| Major System Components | 6-7 |
| The Token-Ring Adapter in the 3745 | 6-9 |
| Introduction | 6-9 |
| Packaging | 6-9 |
| Token-Ring Interface Coupler (TIC) Card | 6-11 |
| TIC Data Flow | 6-11 |
| The Front End | 6-12 |
| The Protocol Handler | 6-12 |
| The Message Processor | 6-12 |
| TIC Bus Interconnection Control | 6-13 |
| Receive Operation | 6-13 |
| Transmit Operation | 6-14 |
| Token-Ring Multiplexor (TRM) Card | 6-15 |
| IOC Bus Interconnection | 6-15 |
| Summary of the IOC Bus Interface Signal Lines | 6-16 |
| TIC Bus Interconnection | 6-16 |
| Summary of the TIC Bus Signal Lines | 6-17 |
| TRM Arbitration Mechanism | 6-18 |
| TRA Resets | 6-19 |
| Power ON Reset and Tag Reset | 6-19 |
| Programmed Reset | 6-19 |
| TIC Reset | 6-19 |
| Diagnostic Section TA0A | 6-19 |
| Error Detection and Reporting | 6-20 |
| TRM Level 1 Error Status Register | 6-20 |
| TRM Level 2 Error Status Registers | 6-22 |
| MOSS Error Status Register | 6-24 |
| TIC Adapter Check Register | 6-25 |
| Problem Determination Aid | 6-28 |
| Token-Ring Wrap Tests | 6-28 |

The TRSS in 3745 Data Flow

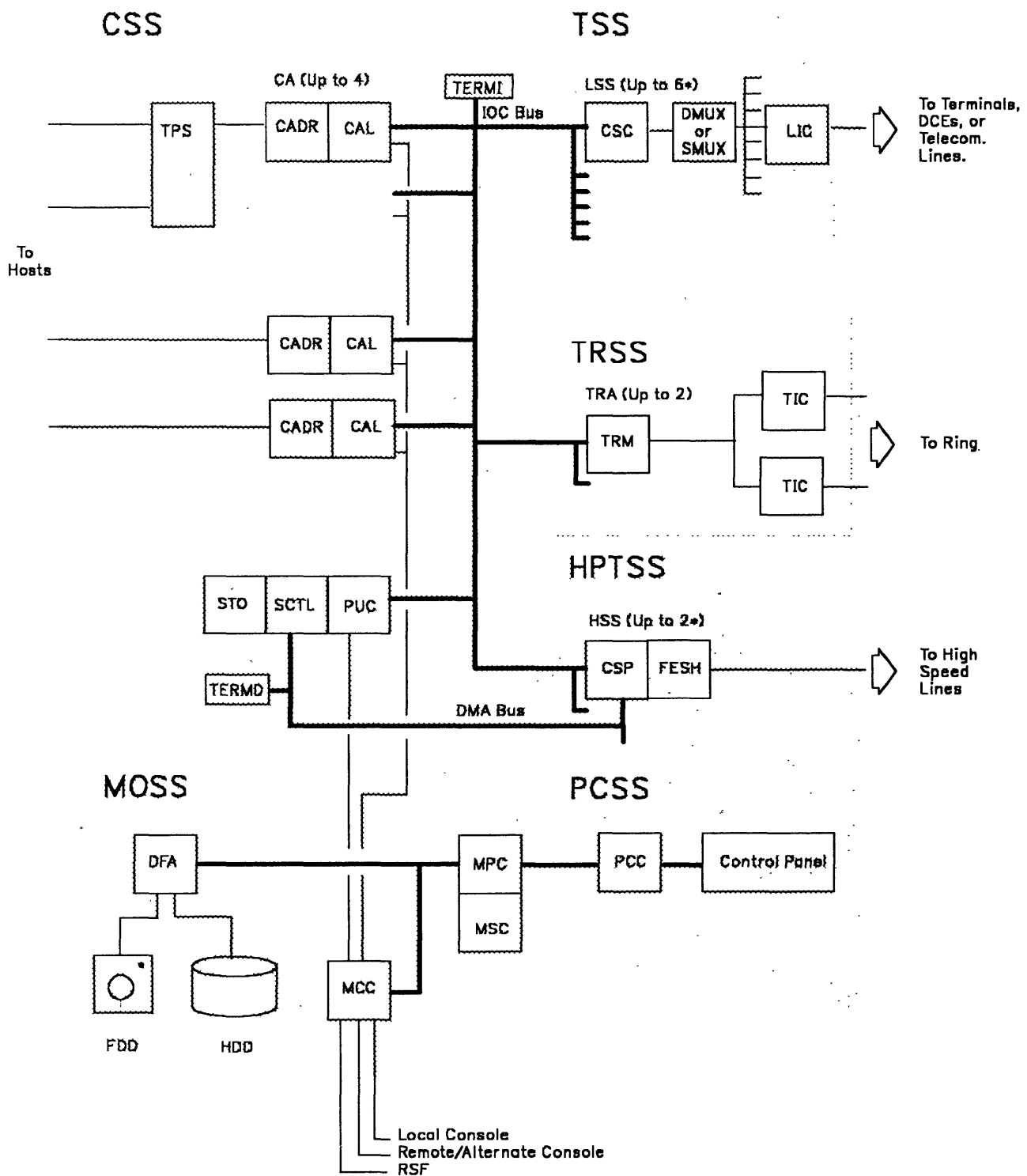


Figure 6-1. TRSS in 3745 Data Flow

Token-Ring Network

The token-ring networks are designed specifically to provide an integrated approach to communications in a particular location.

In case of large companies with multiple, widely separated sites, individual token-ring networks will almost always be interconnected.

In a token-ring network the data rate is much higher than is possible using common carrier communications.

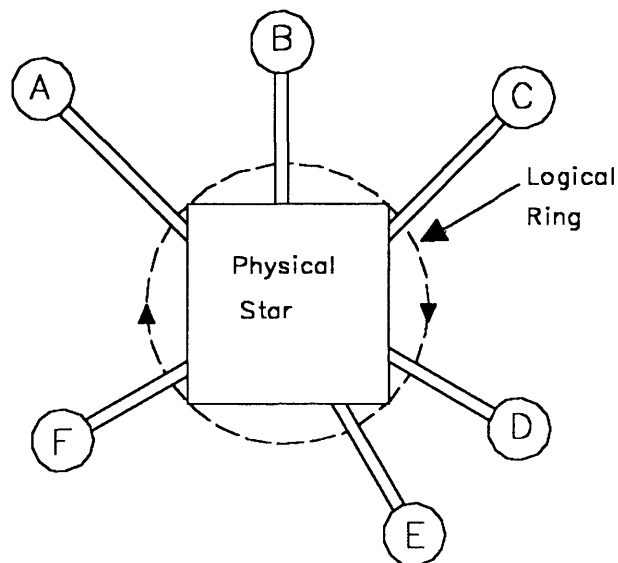
A token-ring network can replace switched and non-switched telephone lines and also allow voice communications over the same cabling system that carries data communications.

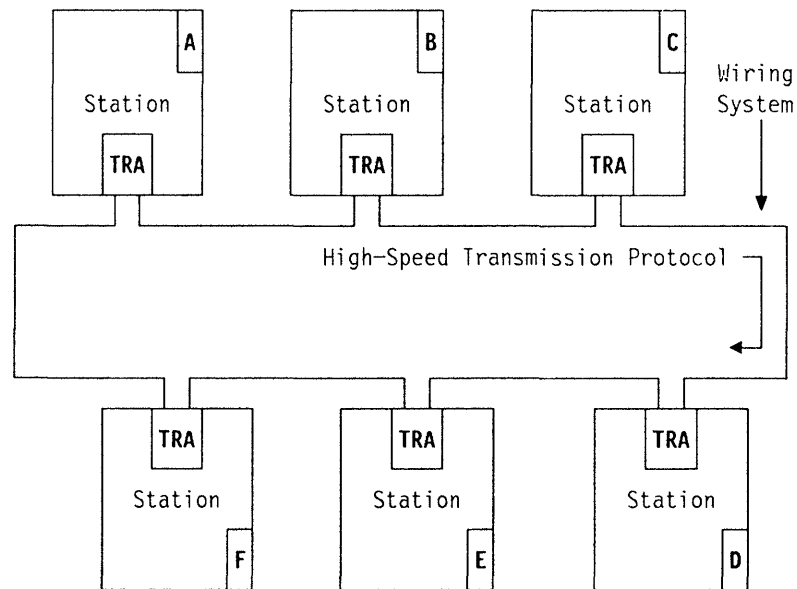
The token-ring complies with the recommendation 802.5 of IEEE and the ISO 8802/5.

IBM Token-Ring Network

It is an information transport system that provides high-speed (4 Mbps or 16 Mbps) connection between users within a single building complex through the implementation of a common:

- Cabling system
- Communication adapter
- Access protocol





Legend: TRA : Token-ring adapter
 Station : Can be controller, display/keyboard terminal, node...

Figure 6-2. Token-Ring network Configuration Example

Cabling System (Ring)

Several transmission media may be used together:

- IBM Cabling System (twisted-pair of copper wire)
- Telephone communication facilities
- Optical fiber.

Token-Ring Adapter

The adapter in the 3745 has the following functions:

- Frame and address recognition
- Token generation
- Error checking and logging
- Buffering (transmit and receive)
- Time out controls
- Connect the product to the token-ring network.

For Example

The 3745 is connected to the IBM Token-Ring network through the token-ring interface coupler card (TIC). A cable composed of two pairs of copper wires (transmit and receive pairs), connects the controller to the multistation access unit (MSAU) through a wall connector.

The cable running from the controller or a station to the MSAU, is called a lobe.

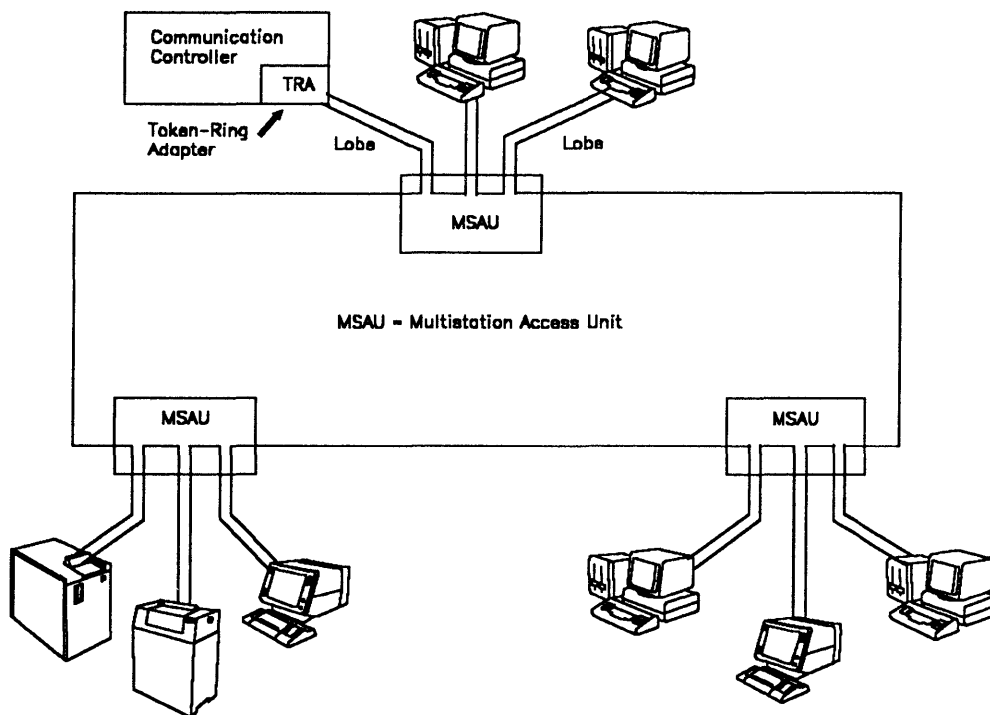


Figure 6-3. Example of Lobes

Multistation Access Unit

The multistation access unit (MSAU) provides insertion service to the main ring for its attached lobes. Nodes or stations are attached to the lobes.

The multistation access units that include electronic or electro-mechanical switching elements, are shown below:

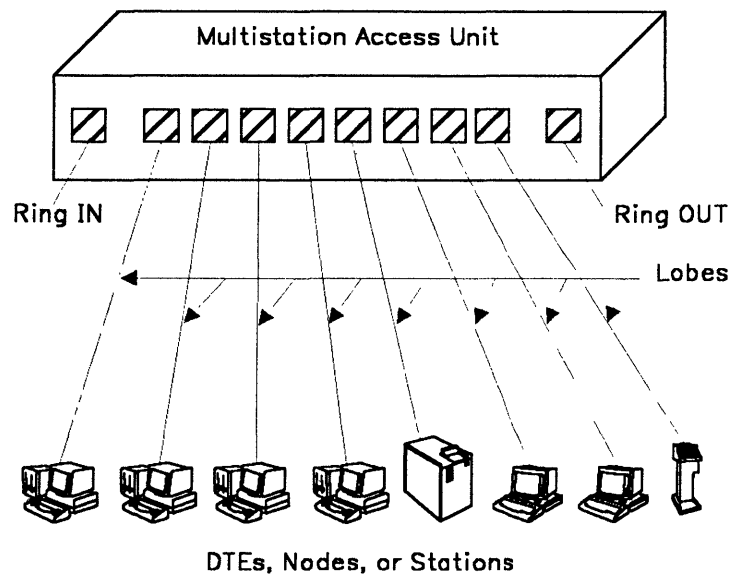


Figure 6-4. Multistation Access Unit

Access Protocol

A token is a short message. It travels around a communication ring that allows attaching different systems to the communications facilities provided by that ring. When a token is used for transmission by an attachment, it is known as a frame. Actually, a token is a very short frame (3 bytes) that has no addressing, message, or error-checking capabilities. Those are added when the token becomes a true frame.

General Frame Format

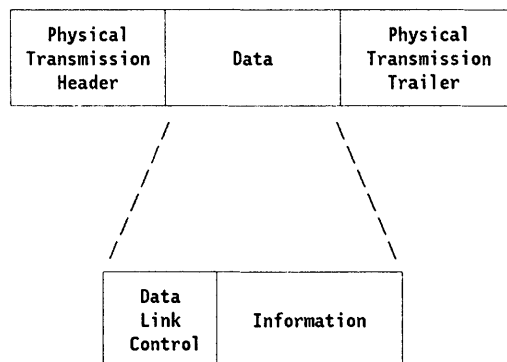


Figure 6-5. Frame Format

Once a station is physically attached to a ring, it first synchronizes itself to the data patterns passing through it over the ring.

Token-Ring Access Control Protocol

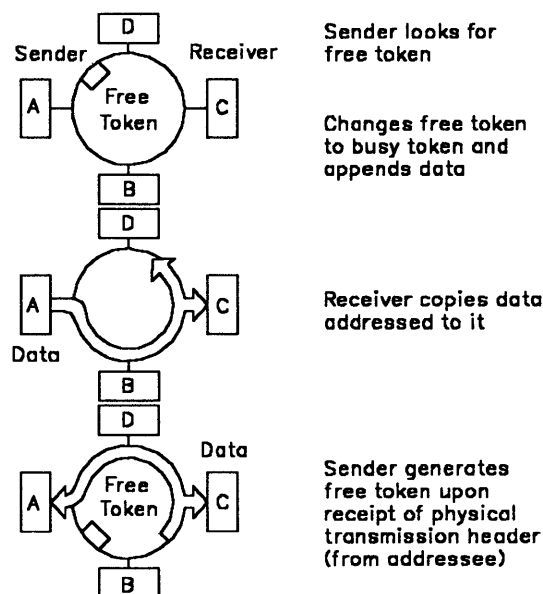


Figure 6-6. Token-Ring Access Protocol Example

Token-Ring Encoding

The differential Manchester protocol is used as means to transmit information around the ring, to all devices connected to that ring and power-ON.

Major System Components

Nodes

A node may be one of the following machines:

- Communication controller
- Intelligent workstation
- Keyboard/display terminal
- Printer
- Terminal control unit
- Processor
- Facsimile device
- Personal computer
- Protocol converter.

Interface Couplers

Each node has its own token-ring interface coupler card to gain access to the token-ring network or ring.

The 3745 has up to eight token-ring interface coupler cards type 2 (TIC2) which can work at 4 or 16 Mbits.

Bridges

A bridge is a high-speed switching device that allows linking multiple rings and maintaining a physical ring separation.

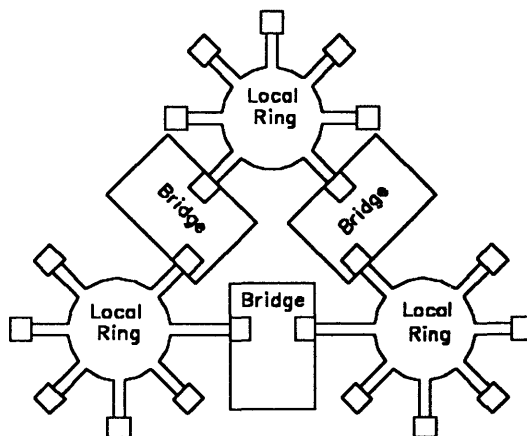


Figure 6-7. Ring-to-Ring via Bridge Example 1

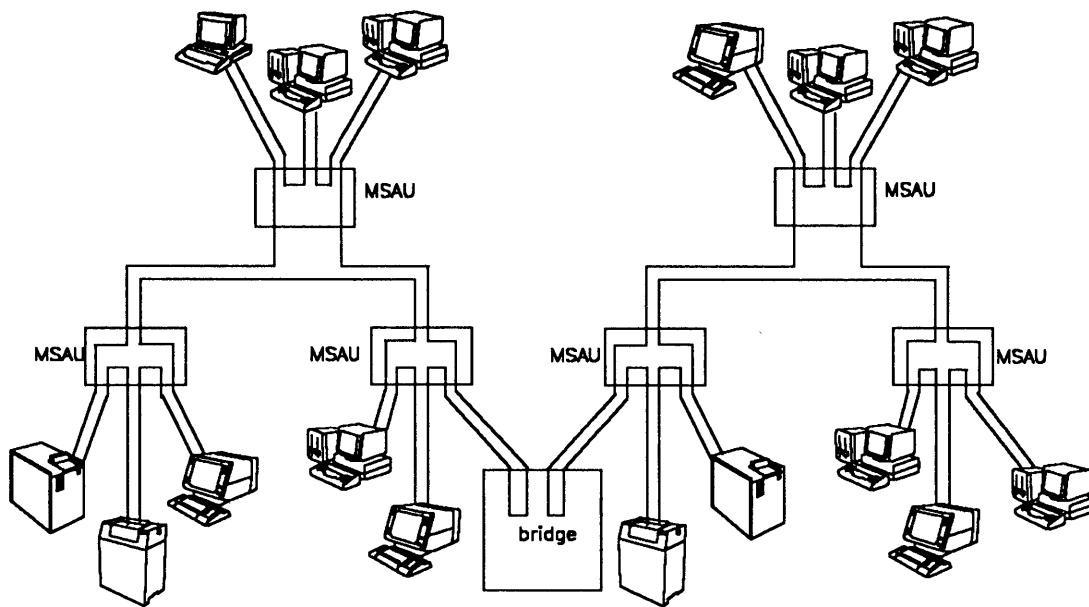
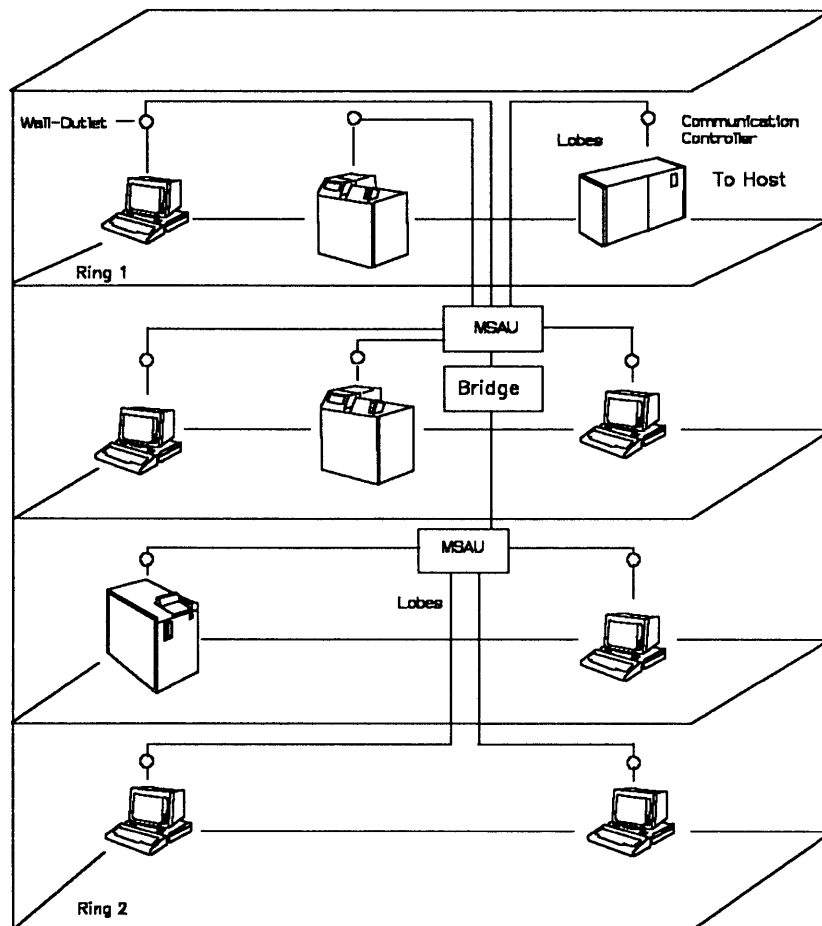


Figure 6-8. Ring-to-Ring via Bridge Example 2

Typical Multi-Floor Wiring



The Token-Ring Adapter in the 3745

Introduction

The token-ring subsystem (TRSS) allows connection to an IBM Token-Ring network which uses the token-ring protocol.

The TRSS in a communication controller is controlled by the NCP token-ring interconnection function.

The hardware is based on a processor-driven card named token-ring interface coupler card (TIC) and the token-ring multiplexer card (TRM). There are two types of TIC: TIC type 1 (TIC1) and TIC type 2 (TIC2). TIC1 runs at ring-speed of 4 Mbps only. TIC2 runs at a ring-speed of 4 Mbps or 16 Mbps (the speed is set through software).

The combination of a TRM and the associated TICs (up to two) is called a token-ring adapter (TRA). The TICs installed with a TRM must both be either TIC1's or TIC2's. A mixture of TIC types with the same TRM is not allowed. The combination of all the TRAs in a controller is called the TRSS.

One token-ring network can be accessed by each TIC card.

Packaging

Only one TRA may be installed on the basic board of the Models 00A and 00C and up to two TRAs in the Model 00B. Each TRA may control up to two token-rings. The TRM interconnects with the input/output control bus (IOC bus) and it is accessed from the CCU with a unique address as for the scanner. The two TIC cards are connected to the TRM by a bidirectional bus called the TIC bus.

For board and card locations, see the *Maintenance Information Procedures* manual, SY33-2070.

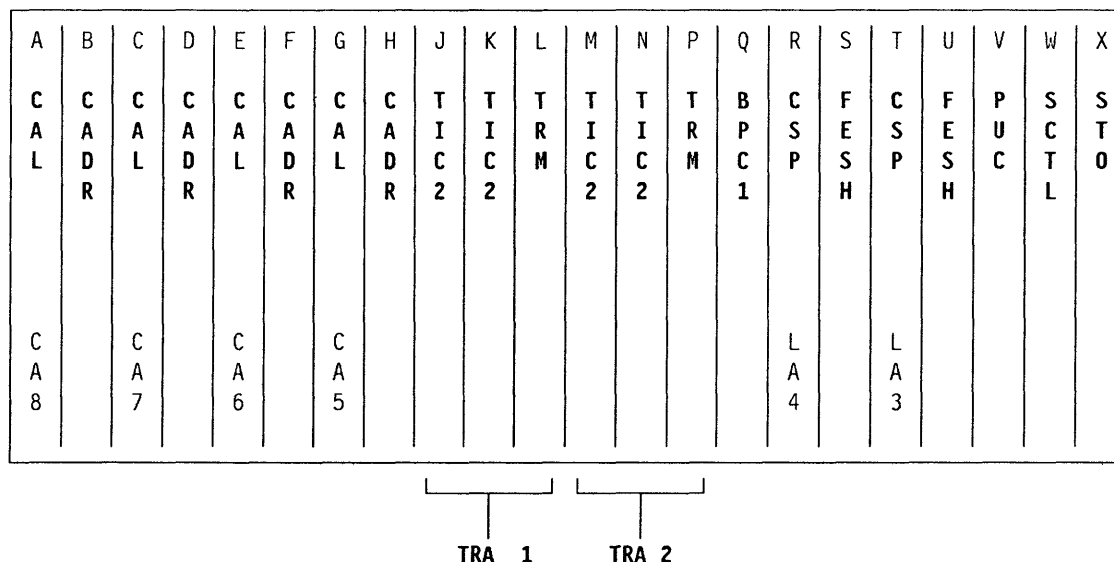


Figure 6-9. Basic Board Model 130

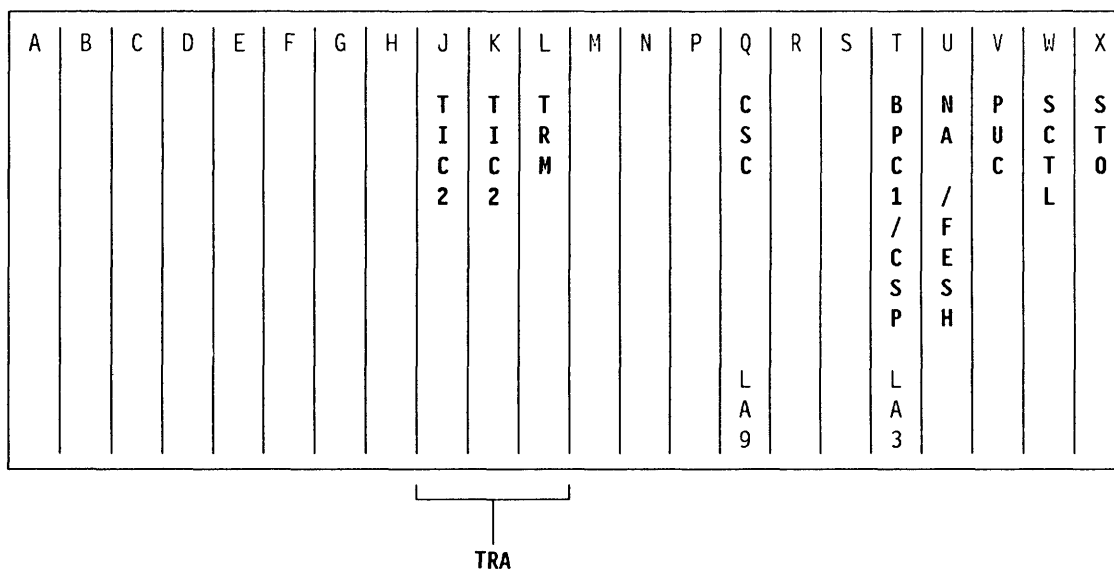


Figure 6-10. Basic Board Model 150

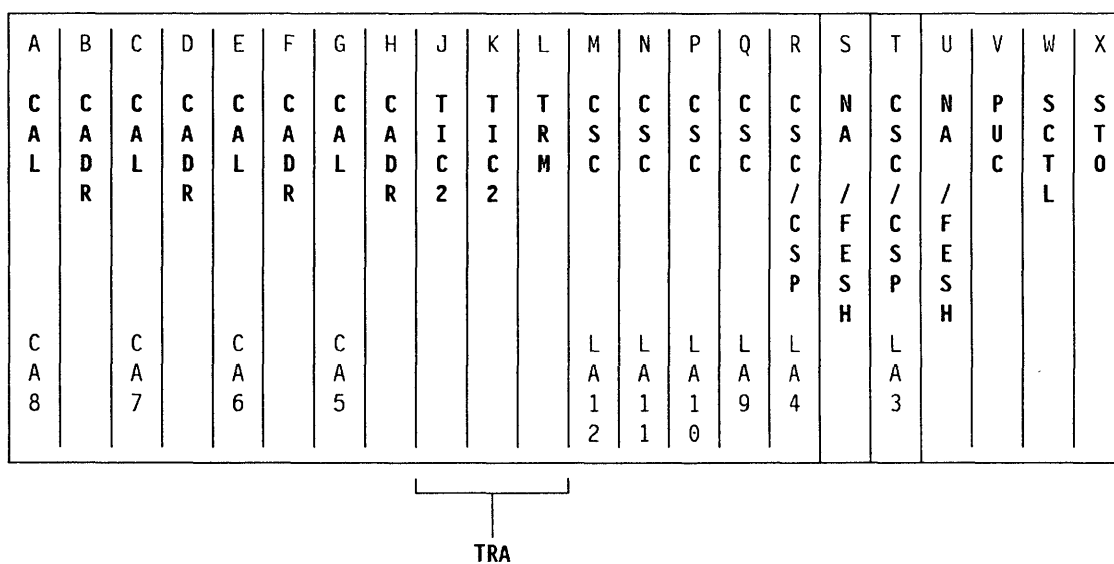


Figure 6-11. Basic Board Model 170

Token-Ring Interface Coupler (TIC) Card

The TIC card has a low profile connector for connection to the ring.

The card consists of four high-level functional areas.

- The front end that interfaces to the ring
- The protocol handler
- The message processor
- The TIC bus interconnection control.

TIC Data Flow

The TIC can perform the following operations on the data stream that passes through it on the ring:

1. Repeat the received data without copying it.
2. Repeat and copy the received data.
3. Change the state of single bits in the received data before retransmitting it.
4. Originate the transmission of data.
5. Remove from the ring messages that it has previously transmitted.

The next figure shows the relationship between the message processor and the other functional areas of the TIC card.

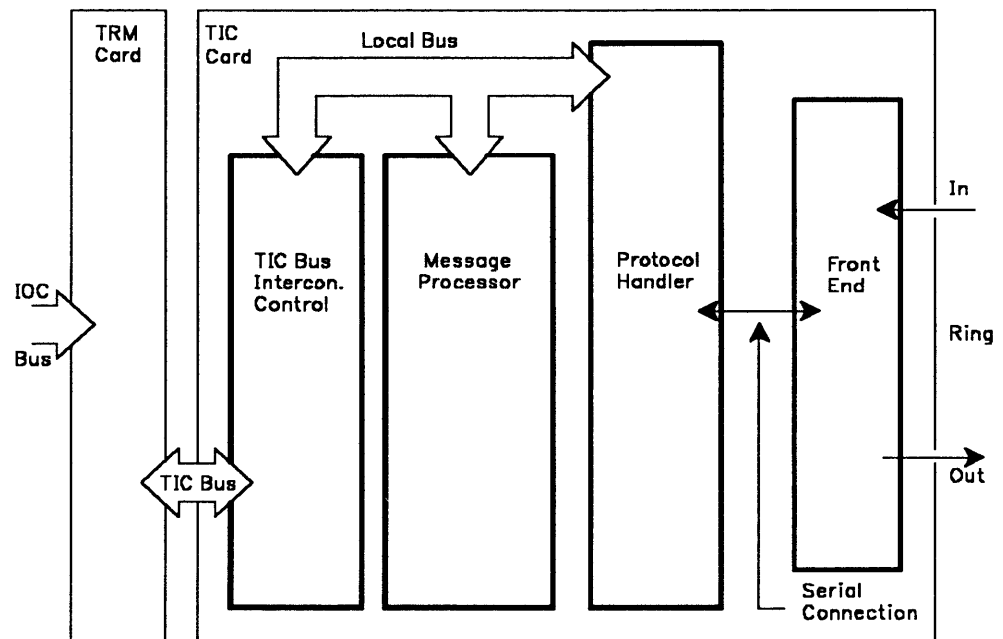


Figure 6-12. TIC Card Data Flow

The Front End

The front end is the direct interface with the transmission line of the ring.

The front end transmits and recovers Manchester-encoded data as it passes around the ring.

The front end synchronizes itself with the received data stream and develops a clock which is boundary-aligned to the bit stream.

The bit stream, along with the derived clock, is passed to the protocol handler.

The front end requires monitoring and control by the protocol handler.

The Protocol Handler

The protocol handler acts as the logical interconnection between the front end and the local bus.

It prepares received data for processing by the microcode operating in the microprocessor of the message processor.

It also prepares data that has been assembled by the microprocessor for transmission through the front end onto the ring.

It decodes addresses for recognizing received messages and strips messages from the ring that have been previously transmitted.

It checks that the ring is active and operational.

These logs are used to isolate the faulty element in the IBM Token-Ring network.

The protocol handler controls and maintains the low-level bit and byte protocols on the ring.

The Message Processor

The message processor acts as the master control element for the protocol handler and the TIC bus interconnection control in the TIC card. Interaction with these functional areas is across an 18-bit local bus. The message processor is the general name for the microprocessor (microcode and the hardware). It consists of the following items:

- A microprocessor
- Static random access modules (RAM) for message data
- Static random access modules (RAM) for parity
- Read-only storage modules (ROS) for microcode.

The microprocessor uses the random-access memory (RAM) as workspace when processing instructions.

The message processor can set up control conditions or interrogate status across the local bus using MMIO-type operations.

Data is accessed and stored in the RAM by the protocol handler and TIC interconnection control using direct memory access protocol.

The RAM is also used as buffer space for messages to be passed from the ring to the TIC bus interconnection, and messages to be passed from the TIC bus interconnection to the ring.

Access to the buffer space by the protocol handler and the TIC bus control is also controlled by the microprocessor.

Transfers into and out of the RAM are performed using direct memory access (DMA) protocols.

TIC Bus Interconnection Control

The TIC interconnection control provides a mechanism for transferring data between TIC storage (RAM) and CCU storage, via cycle steal. It operates in halfword bus mode.

The function performed by the TIC bus interconnection control can be visualized as a double interface DMA controller with a 128-byte hardware store-and-forward buffer. The 128-byte buffer can logically connect either to the TIC bus interconnection control or to the local bus, but not to both at the same time.

When DMA data transfer is occurring at the TIC bus interconnection control, the TIC is the bus master, and the data can flow in only one direction (read or write) at a time.

In addition to its DMA function, the TIC bus interconnection control can also transfer data to or from TIC storage.

This function is intended for adapter initialization and to obtain TIC status.

Receive Operation

On receive, data is taken from the ring into the front end, where it is reshaped into distortion-free digital signaling elements.

The front end synchronizes itself with the received data stream and develops a clock which is boundary-aligned to the bit stream.

This bit stream, along with the derived clock, is passed to the protocol handler.

The protocol handler converts the encoded data stream into coding usable by the adapter.

By counting received clock pulses, the protocol handler assembles the bit stream into halfwords units.

Parity is generated on the received data de-serialized from the ring to check data validity through the adapter.

During the receive sequence, cyclic redundancy check (CRC) calculation is begun on the received data.

The destination address is compared against the stored values in the protocol handler to determine if the message is to be copied by the adapter. If so, the protocol handler conditions itself to begin the copy, and transfer is started to the message processor.

The destination and source addresses, the physical control field, the data portions, and the CRC characters of the in-progress received message are now passed to the message processor in sequence.

When the end of the CRC-protected field is received, the previously received CRC characters are compared to the calculated CRC.

- If there is a match, message reception is considered complete by the protocol handler.
- If there is a mismatch on the CRC check, the message processor is signalled that the message should not be considered valid.

The message processor assembles into multi-byte blocks the information received from the protocol handler.

When that assembly is complete, the message processor begins a transfer into CCU storage. These segment transfers continue until the complete message has been transferred.

When the transfer is completed, the message processor completes the receive operation by reporting the status of the transfer to the CCU.

Transmit Operation

Data flow during transmit operations is essentially the reverse of that during receive operations.

The message is accumulated by the CCU in CCU storage, and the message processor is set up with the storage location and length information. The message processor then does a storage-to-storage transfer of the message, including the destination and source addresses, from CCU storage to the message processor.

The message processor signals the protocol handler to begin transferring the message from the message processor resident storage into the hardware buffers of the protocol handler.

When the protocol handler senses that a transmission is pending, it begins the transfer into its buffers. After enough characters have been buffered, the protocol handler searches for a free token on the ring. When one is found, the token is changed to a busy token.

The control characters are generated, and transmitted.

Sequential transmission out of the buffers continues with the destination and source addresses.

When the entire information field has been transferred, the protocol handler inserts the CRC characters that have been accumulated in the message.

The protocol handler begins to remove (strip) any data from the ring that is being received.

The incoming data stream is searched for a match of the source address with the address of the TIC.

After a match is found and transmission is complete, the TIC encodes and transmits a free token on the ring.

The transmission of the free token is followed by a continuous transmission of idle characters.

The TIC also begins repeating the received data stream, and the transmit operation is considered complete.

Token-Ring Multiplexor (TRM) Card

The TRM card handles the operations between the CCU and the token-ring interface couplers (TICs).

On one side, the TRM interconnects the CCU and the MOSS through the IOC bus, and on the other side, the TRM interconnects the TICs through the TIC bus.

The TRM functions are:

- Receive and re-drive the lines toward the IOC bus
- Provide the clocking generation
- Perform the daisy chain continuity for the IOC bus serial lines
- Convert PIO operations into MMIO operations
- Convert DMA operations into cycle steal operations
- Can generate three different types of interrupt
- Check the validity of the transactions between the CCU or the MOSS and the TICs.

To perform these functions, several registers are located in the TRM:

- Buffer and the extended buffer
- TIC control register
- Interrupt request and bus request register
- Diagnostic register
- Level 1 error status register
- Level 2 error status register
- MOSS error status register.

IOC Bus Interconnection

The IOC bus interconnection allows communication between the TRAs and the CCU (NCP), or between the TRAs and the MOSS.

The IOC bus signal lines go to/from the TRM card bottom connector I/O pins.

See Chapter 3, "Buses and Switching" for more information.

Summary of the IOC Bus Interface Signal Lines

| Signal Line Names | Mnemonic | Initiated by | PIO/TRM | AIO | Interrupt |
|--|------------|--------------|---------|-----|-----------|
| Card present IN | + PREIN | Adp.before | X | X | |
| Card present OUT | + PREOUT | TRM | X | X | |
| Cycle steal request high | + CSRH | TRM | | X | |
| Cycle steal grant high | + CSGH | CCU | | X | |
| Cycle steal grant high previous | + CSGHP | CCU | | X | |
| Cycle steal priority line | + CSPRY | TRM/adapt. | | X | |
| CSG through tag | + CSGT | TRM | | X | |
| IOC data bus | +D0 - +D15 | TRM/CCU | X | X | X |
| End of chain | + EOC | TRM | | X | |
| Halt | + HALT | CCU | X | X | |
| Input/output | + I/O | CCU | X | X | |
| Interrupt request removed | + IRR | TRM | X | X | |
| Interrupt to MOSS | +ITMOSS | TRM | X | X | X |
| Level 2 priority line | +L2PRY | TRM/adapt. | | | X |
| Level 2 serial select line in | +L2SSLIN | Adp.before | | | X |
| Level 2 serial select line in previous | +L2SSINP | Adp.prev. | | | X |
| Level 2 serial select line out | +L2SSL0U | Adp.prev. | | | X |
| Modifier | + M | TRM | | X | |
| Parity valid | + PV | TRM | X | X | |
| Parities | +P0,+P1 | TRM/CCU | X | X | X |
| Power on reset | - POR | Power blick | | | |
| Reset | + RESET | Switch | | | |
| TA | + TA | CCU | X | | |
| TD | + TD | CCU | X | X | |
| Valid halfword | + VH | TRM | X | X | X |
| Valid byte | + VB | TRM | | X | |

Figure 6-13. Summary of the IOC Bus Interconnection Signal Lines

TIC Bus Interconnection

The TIC bus is a bidirectional bus which connects the TRM card to the TIC cards via the card bottom connector I/O pins and the board.

Three types of operation are used on this interface:

- Direct memory access (DMA)
- Memory mapped input/output (MMIO)
- Interrupt acknowledgement (IACK).

DMA Operation

The DMA operation allows transferring a burst of data between the TRM and the TIC.

During DMA operations, the TIC controls the bus and the TRM is the tributary unit.

MMIO Operation

The MMIO allows access to the registers of the IOC interconnection control of the TIC.

Interrupt Acknowledge (IACK) Operation

Interrupt acknowledge (IACK) cycles are used to access a vector in the TIC when the TIC requests an interrupt to the TRM. The vector indicates the cause of the interrupt.

Summary of the TIC Bus Signal Lines

| Signal Line Names | Mnemonic | Initiated by | PIO/MMIO | DMA | Inter-rupt |
|---------------------------|---|--------------|----------|-----|------------|
| Address bus | +A1, +A2, +A3 - +A23, +APL, +APH, +APX, +A0 | TRM, TIC | X | X | |
| Data bus | +D0 - +D15, +DPL, +DPH | TRM, TIC | X | X | X |
| Address strobe | - AS | TRM, TIC | X | X | X |
| Card select(2) | - CS | TRM | X | | |
| Read/write | - RNW | TRM, TIC | X | X | X |
| Upper data strobe | - UDS | TRM, TIC | X | X | X |
| Lower data strobe | - LDS | TRM, TIC | X | X | X |
| Data transfer acknowledge | - DTACK | TRM, TIC | X | X | X |
| Bus error | - BERR | TRM | | X | |
| Bus request(2) | - BR | TIC | | X | |
| Bus grant(2) | - BGR | TRM | | X | |
| Bus busy | - BBSY | TIC | | X | |
| Bus release | - BRLS | | | X | |
| Interrupt request (2) | - IR | TIC | | | X |
| Interrupt acknowledge(2) | - IACK | TRM | | | X |
| Reset (2) | - RESET | TRM | | | |
| System clock | + BCLK | TRM | X | X | X |
| System last Transfer | - SLT | TIC | | X | |

Figure 6-14. Summary of the TIC Bus Signal Lines

TRM Arbitration Mechanism

Since two TIC cards can be attached to the TRM, the TRM can simultaneously receive up to two bus requests for DMA, and up to two interrupt requests from the TIC cards.

The arbitration logic comprises two scan wheels, one for bus requests (BR), the other for interrupt requests (IR). Each wheel in turn can point to either of the two attached TICs.

TRA Resets

Three functions are implemented to reset the TRA (TRM and TICs) or a part of the TRA:

1. The power-ON/tag reset function
2. The programmed reset function
3. The TIC reset function.

Power ON Reset and Tag Reset

These resets are activated in two ways:

1. By the power-ON reset line coming from the power blocks.
2. By the reset tag coming from the switch card.

It completely resets the TRA:

- All requests on the IOC bus are deactivated.
- The TRM reset bit is forced ON in the TRM control register (which indicates a reset has been done).
- The TIC reset bits are forced ON (and the reset leads on the TIC bus) in the TIC control register.
- All the interrupts and their associated statuses are reset.
- The disconnect bit and the CCU PIO disable bit are reset.
- The entire control logic is forced to idle state.
- The BR and IR scan wheel is pointed to the TIC 1.
- More generally, all other functions and all other registers are forced in their inactive state.

Programmed Reset

The programmed reset is initiated by a PIO (IOH or MIOH). It allows the program to reset the TRM without resetting the attached TIC(s) and the connect or disconnect state of the TRM.

The result is the same as the hardware reset except the TIC reset bits, the disconnect mode latch, and the CCU PIO disabled latch are left in their current state.

TIC Reset

The program can perform a selective reset of the TIC by setting or resetting the TIC control register TIC reset bit. The reset bits are connected to the TIC reset leads on the TIC bus. The reset lead is active as long as the reset bit is ON in the TIC control register. The TIC reset lead causes the TIC to disconnect itself from the ring and perform a reset.

Diagnostic Section TA0A

The TRM must be 'disconnected' before running the diagnostic section TA0A. The 'disconnect' command must be performed after each power-OFF to power-ON.

Error Detection and Reporting

TRM Level 1 Error Status Register

TD Field

| | | | | | | | |
|--------------|--------------|-----------------|--------------------|-------------|----|----|---------------|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| R/W | I/O Check | CSG | I/O | Halt | TA | TD | Discon. |
| 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| TA Select | CS Select | TIC Bus Idle | CCU PIO Disabl. | TRM/ TIC | | | Inval. IOH |

TIC number for DMA
or interrupt

Level 1 interrupts can be generated by the:

- TRM on disconnect
- IOC on time out, bus-in parity, CSCW, storage protect or address exception errors.

Error reporting using IOC level 1 interrupts is limited to errors occurring on the IOC bus and errors detected by the IOC.

TRM internal errors and the TIC interconnection errors found during PIO/MMIO, DMA/CS, or read interrupt vector operations, are reported by a level 2 interrupt for the appropriate TIC.

The pattern in the level 1 status register for a disconnect level 1 interrupt has the following value B'1000000100000000'.

When the CCU IOC logic detects an error, it raises the halt tag.

When the TRM detects the halt tag, it sets the level 1 status register with the exception of bits 7 and 11.

Bits 7 and 11 reflect the status of the indicated latches when the get level 1 error status register PIO is executed.

During an IOC level 1 interrupt, bits 0-3, 5-6, 8-10 and 12-15 are valid only if bit 4 is ON.

Bit 0 This bit (R/W bit) is ON if a read PIO/AIO is being executed. It is OFF if a write PIO/AIO is being executed. The R/W bit is always ON for a disconnect level 1 interrupt. It is valid only if bit 8 or 9 is ON for an IOC level 1 interrupt.

- Bit 1** This bit (I/O check) is ON if the TRM detects a parity error on the IOC bus when the halt tag is activated.
- Bit 2** This bit (CSG) is ON if the CSG tag in the TRM is active when the halt tag is activated.
- Bit 3** This bit (I/O) is ON if the I/O tag in the TRM is active when the halt tag is activated.
- Bit 4** This bit (halt) is ON if the TRM has detected the activation of the halt tag on the IOC.
- Bit 5** This bit (TA) is ON if the TA tag into the TRM is active when the halt tag is activated.
- Bit 6** This bit (TD) is ON if the TD tag into the TRM is active when the halt tag is activated.
- Bit 7** This bit (disconnect) is ON if the TRM is in disconnect mode when the read level 1 error status register PIO is executed.
- Bit 8** This bit (TA select) is ON if the TRM has recognized its address (with good parity) and the PIO has not completed when the halt tag is activated.
- Bit 9** This bit (CS select) is ON if the TRM has trapped CSG for an AIO and the AIO has not completed when the halt tag is activated.
- Bit 10** This bit (TIC bus idle) is ON if the TRM detects that the TIC bus is idle when the halt tag is activated.
- Bit 11** This bit (CCU PIO disable) is ON if the TRM is disabled for CCU PIOs when the read level 1 error status register is executed.
- If the TRM is CCU PIO disabled, the level 1 error status register can be successfully read only by an MIOH.
- Bit 12** This bit (TRM/TIC) is ON if an AIO or a get line ID PIO is being executed by the TRM when the halt tag is activated.
- If this bit is ON, it means that bits 13 and 14 are valid.
If this bit is OFF, it means that the error cannot be associated with any particular TIC.
- Bits 13 and 14** Bits 13 and 14 are used to encode the TIC number for some errors.
- During a cycle steal operation, bits 13 and 14 are used to identify the TIC that was doing the DMA operation when the halt tag was received. They also indicate the originator of the level 2 interrupt for an error during a get line ID PIO. These bits are valid only if bit 12 is ON.
- 00 = TIC 1
01 = TIC 2
- Bit 15** This bit (invalid IOH) is ON if the TRM decodes an invalid PIO type when the halt tag is activated. This bit is valid only if bit 5 is ON.

TRM Level 2 Error Status Registers

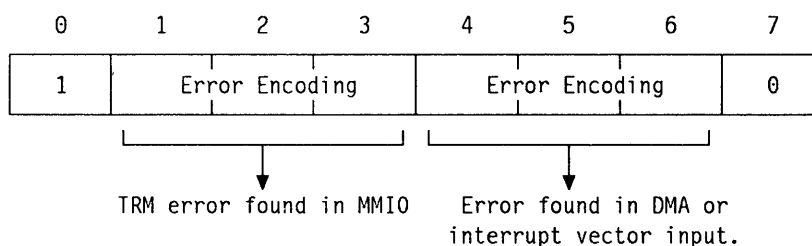
The TRM provides two level 2 status registers (one per TIC).

The level 2 status information is set by the TRM when an error is found in the TRM (not on the IOC bus), an error is detected on the TIC interconnection, or the TIC requests an interrupt.

This information can be read by the program through a get TRM level 2 error status command. The error or status is reset if the PIO read operation completes with no errors. After the status is successfully read, the TRM is able to log another error or status.

FORMAT 1 (Error Detected by TRM)

TD Field Byte 0 (Byte 1 not Used)



Error Encoding:

0 0 0 No error
0 0 1 TRM internal
0 1 0 TIC interconnection type 1
0 1 1 TIC interconnection type 2

Internal The TRM is suspected.

Type 1 The working TIC is suspected.

Type 2 All TICs can be suspected (idle state error).

This error encoding is performed by the TRM using the checkers in the TRM (See "Error Detection and Reporting" on page 6-20).

The status provides two independent error fields:

1. PIO/MMIO operations which require program retry
2. Operations which do not require program retries:
 - DMA (TIC retries automatically)
 - Input interrupt vector (TRM automatically retries)

Both fields can be significant at a given time.

When a field is set, another error will not be set in the same field until it is reset by a successful 'get TRM level 2 error status'.

A DMA or input interrupt vector operation is retried automatically when the error in the level 2 error status register is reset by a successful 'get TRM level 2 error status' PIO.

FORMAT 2 (Interrupt Request by the TIC)

TD Field Byte 0 (Byte 1 not Used)

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | x | x | 0 | 0 | 0 | 0 |

TIC from TIC interrupt vector

Format 2 is used when a TIC requests an interrupt.

The contents of this register will be:

B'00100000' for the SCB clear vector.

B'00010000' for the adapter check vector.

B'00000000' or B'00110000' for the other TIC vectors.

NCP initializes the TIC interrupt vectors to

B'xx10xxxx' for SCB clear.

B'xx01xxxx' for adapter check.

B'xx00xxxx' or B'xx11xxxx' for the remainder.

A format 1 entry will cause the type B line ID to be used.

A format 2 entry with bits 2 and 3 = B'10' or B'01' will also use the type B line ID. All other cases use the type A line ID (See next paragraph "Line Identification (Line ID) Generation" for type line ID definitions).

If the level 2 error status register contains a format 2 entry and the TRM detects an error that requires logging a format 1 entry, the TRM will overlay the format 2 entry.

After the format 1 entry is read and reset, the interrupt vector will again be fetched from the TIC and the format 2 entry set in the register again.

Line Identification (Line ID) Generation

When the CP receives a level 2 interrupt, it places a PIO get line ID command on the IOC bus.

This command is decoded by all adapters. However only one, according to the level 2 interrupt priority mechanism, will answer with a line ID.

For adapters set to the same priority, the first adapter on the IOC bus will be serviced first.

The line ID allows the program to identify the requesting adapter and to process the interrupt.

There are 2 different line IDs per TIC:

- Type A. For the TIC interrupts for which the system status is cycle-stolen to the CCU.
- Type B. For the TIC interrupts for which the system status is not cycle-stolen to the CCU (SCB clear or adapter check) and interrupts generated for TRM-detected errors.

The get line ID command resets the level 2 interrupt and the TRM is now free for another operation including an interrupt (IR) from another TIC.

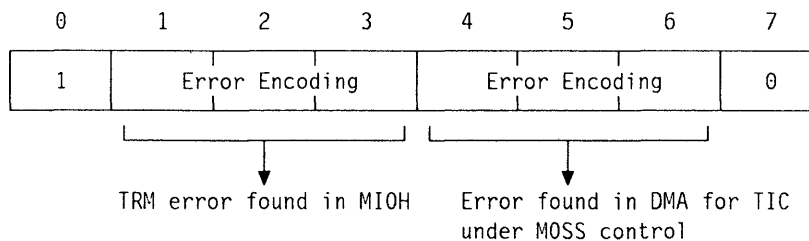
The CCU interrupt code sequence ends with a reset interrupt PIO/MMIO to the concerned TIC.

The TIC will lower its interrupt line and this will allow the TRM to treat another interrupt coming from the same TIC. In its turn the TIC is free for other operations.

MOSS Error Status Register

Format 1 is used for errors detected by TRM in MOSS PIO/MMIO operations or in direct memory access (DMA) operations (TIC to CCU storage).

TD Field Byte 0 (Byte 1 not Used)



Error encoding:

0 0 0 No error
 0 0 1 TRM internal
 0 1 0 TIC interconnection type 1
 0 1 1 TIC interconnection type 2

Internal The TRM is suspected.

Type 1 The working TIC is suspected.

Type 2 All TICs are suspected.

The MOSS error status register is used to log errors associated with MOSS operations. If a MOSS control bit in the TIC control register is ON, all MMIO and DMA errors for that TIC will be logged in the MOSS error status register.

If the TRM is connected, all MIOH/MMIO errors will be logged in the MOSS error status register.

If the TRM is disconnected and the associated MOSS control bit is OFF, all MMIO and DMA errors for a TIC are logged in the normal level 2 error status register.

Format 2 is not used for the MOSS error status register.

TIC Adapter Check Register

The adapter check interrupt is generated when the TIC has encountered an unrecoverable hardware or microcode error. In this case the TIC is waiting for a reset.

The reason for the TIC check is located in 8 bytes beginning at address X'05E0'. The TIC check status is defined as follows:

X'5E0' (TIC adapter storage)

| Byte 0 and 1 | Byte 2 and 3 | Byte 4 and 5 | Byte 6 and 7 |
|---------------|--------------|--------------|--------------|
| Adapter check | Parameter 0 | Parameter 1 | Parameter 2 |

Each bit of the TIC adapter check gives the error type and the contents of parameters 0 to 2 give additional information. More details are given in the following table.

TIC Adapter Check Register Decoding Byte 0

| Bit | Error Type | Error Description | Parameters 0-2 Contents |
|-----------|------------------------------------|---|---|
| x... | MMIO parity error | Data parity error between CCU and TIC | Contents is ignored |
| .X.. | DMA abort read | DMA read operation abort for time out or parity error or bus error | Parm 0=0000 time out error 0001 parity error 0002 bus error Parms 1-2 contain the failing CCU address + or - 6 Bytes |
| ..X. | DMA abort write | DMA write operation abort | Same as for DMA abort-read |
| ...X | Illegal OP code | Illegal OP code detected | Parm 0 = TIC register 13 Parm 1 = TIC register 14 Parm 2 = TIC register 15 |
| X... | Parity error | Local bus parity error detected by TIC processor | Same as for illegal OP code |
|X.. | Parity error external | Local bus parity error detected by TIC during operation with CCU | Same as for illegal OP code |
|X. | Parity error - IOC bus interf. | Local bus parity error detected by TIC during operation with CCU | Same as for illegal OP code |
|X | Parity error PH (protocol handler) | Local bus parity error detected by TIC during operation with the protocol handler | Same as for illegal OP code |

TIC Adapter Check Register Decoding Byte 1

| Bit | Error Type | Error Description | Parameters 0-2 Contents |
|-----------|-------------------------|--|--|
| x... .. | Parity error receive | Local bus parity error detected by TIC during receive operation | Parm 0 = buffer address |
| .x... .. | Parity error transmit | Local bus parity error detected by TIC during transmit operation | Parm 0 = buffer address |
| ..x. | Ring underrun | DMA underrun detected during ring transmit | Parms 0-2 are ignored |
| ...x | Ring overrun | DMA overrun detected during receive operation | Parms 0-2 are ignored |
| x... | Invalid interrupt | Unrecognized error interrupt was generated | Parm 0 = TIC register 13 Parm 1 = TIC register 14 Parm 2 = TIC register 15 |
|x.. | Invalid error interrupt | Unrecognized error interrupt was generated | Parm 0 = TIC register 13 Parm 1 = TIC register 14 Parm 2 = TIC register 15 |
|x. | Invalid XOP | Unrecognized transmit operation request was generated | Parm 0 = TIC register 13 Parm 1 = TIC register 14 Parm 2 = TIC register 15 |
|x | Program check | TIC processor program check detected | Parm 0 = ABEND code Parm 1 = Address location that detected the error |

Problem Determination Aid

Token-Ring Wrap Tests

Using NCP

Under NCP a wrap test is performed at each TIC open command processing as a first step before inserting itself into the ring.

The TIC internal lobe media test, tests the ring up to and including the logic (relay contact normally closed) pertaining to the position of the IBM 8228 MSAU or equivalent where the lobe connector is plugged-in (the 8228 is a wiring concentrator).

It also tests the ring up to the point where it is unplugged before the 8228. (that is, at the tailgate, at the wall connector, and so on.)

The lobe media test is only invoked on the open command and is not performed as a result of the reset or initialization commands.

Note that a disconnected cable during the lobe media test will cause a lobe wire fault check to appear in both the display token-ring status function and the ring status field (field E) of the token-ring interconnect function. (Refer to the *Problem Determination Guide*, GA33-0096.)

When a lobe wire fault is detected the TIC will be frozen and the status will remain unchanged until the next open is issued

Using TRA Diagnostics

Using the TRA diagnostic routine TG01, a wrap test is also performed up to and including the 8228 or up to the point at which the ring is unplugged before the 8228.

Diagnostic Section TA0A: The TRM must be 'disconnected' before running the diagnostic section TA0A. The 'disconnect' command must be performed after each power-OFF to power-ON.

However, no open commands are issued by the diagnostic routine so a lobe wire fault will not be detected.

Chapter 7. Channel Adapter (CA)

| | |
|--|------|
| Channel Adapters in the 3745 Model 130/170 Data Flow | 7-2 |
| Introduction | 7-3 |
| Buffer Chaining Channel Adapter (BCCA) | 7-3 |
| Packaging | 7-3 |
| Supported Features | 7-4 |
| Non-Supported Features | 7-4 |
| Configuration | 7-4 |
| CA Operating Environment | 7-7 |
| Modes of Operation | 7-7 |
| Host Unit Control Word (UCW)/Host I/O Configuration Data Set (IOCDS) | 7-7 |
| Overall Operation | 7-8 |
| Data Transfer Methods (PIO and AIO) | 7-8 |
| CA Instructions | 7-8 |
| CA States | 7-8 |
| CA Interrupt Requests | 7-9 |
| Accessing CA Registers | 7-9 |
| Channel Interface Tag Signals Used by the CA | 7-10 |
| Autoselection | 7-11 |
| Autoselection Mechanism | 7-11 |
| Autoselection (AS) Chain | 7-11 |
| Autoselection Error | 7-12 |
| Cycle Steal | 7-13 |
| Cycle Steal (CS) Chain | 7-13 |
| Removing a CA from the Cycle Steal Chain | 7-13 |
| CA/MOSS Connection | 7-14 |
| Interrupt Requests | 7-15 |
| Level 1 Interrupt Request | 7-15 |
| Level 3 Interrupt Request | 7-15 |
| Two-Processor Switch (TPS) | 7-16 |
| TPS/TCS Mode | 7-16 |
| Loosely Coupled Host Attachment | 7-16 |
| Alternate Path Host Attachment | 7-16 |
| Alternate Path Host Operations | 7-17 |
| Presentation of Status | 7-18 |
| Effect of System Reset | 7-18 |
| Effect of Selective Reset | 7-19 |
| Channel Stop | 7-20 |
| Interface Disconnect | 7-20 |
| I/O Error Alert | 7-20 |
| Testing and Checking Hardware | 7-21 |
| Autodiagnostics | 7-21 |
| Functions Provided by Diagnostic Program | 7-21 |
| CA Interface Wrap Plugs | 7-22 |
| CA Services | 7-23 |
| CA Interface Display | 7-23 |
| CA Initialization | 7-23 |
| Initialization First Part (Checkout) | 7-23 |
| Initialization Second Part | 7-24 |
| Initialization Third Part (Chaining) | 7-24 |

Channel Adapters in the 3745 Model 130/170 Data Flow

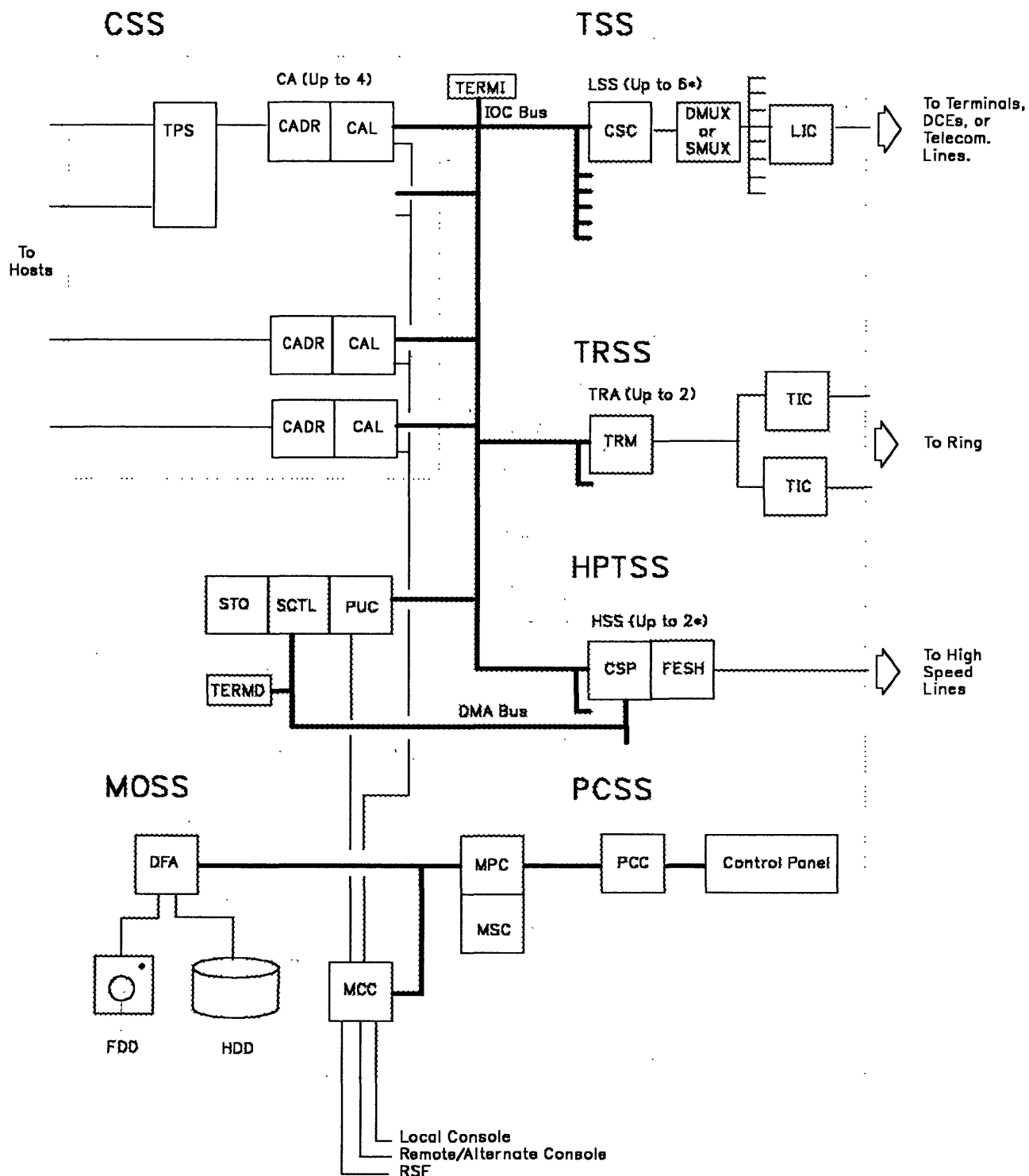


Figure 7-1. Channel Adapters in the 3745 Model 130/170 Data Flow

Introduction

The microcoded CA attaches the 3745 Communication Controller to one or more System 308X/309X/4341/4361 (for **CADS** only) /4381/9370/ES/9000 host processors via selector, block multiplexor, or byte multiplexor channels.

The 3745 supports the channel adapter data streaming (CADS) (CA type 6), and the buffer chaining channel adapter (BCCA) (CA type 7).

From the 3745 MOSS console, an operator can:

- Enable/disable a CA
- Reset a CA
- Display a CA status
- Display CA storage and registers
- Display CA initialization parameters
- Enter/modify CA initialization parameters
- Get a CA dump
- Start/stop a CA trace
- Allow CA concurrent maintenance.

Buffer Chaining Channel Adapter (BCCA)

The **BCCA** is a new type of channel adapter which improved the performance capability. The BCCA is based on CADS design and improves the CADS throughput and channel efficiency. Without NCP intervention, the BCCA handles buffer chaining in write channel program, and both buffer chaining and PIU chaining in read channel program.

BCCA and CADS may be mixed in the 3745. The BCCA operates in native mode only under the Network Control Program (NCP), it does not support the Partitioned Emulation Program (PEP).

The BCCA acts as a CADS when buffer chaining mode is not set, except that it does not support ESC mode.

Note:

In the following pages, specifics of a **type 7 CA** will be indicated by **BCCA**. **CA** stands for **CADS** and **BCCA**.

Packaging

One CADS or BCCA is packaged on one channel adapter logic (CAL) card, and one channel adapter driver/receiver (CADR) card (see Figure 7-3 on page 7-5). See page YZ 052 for CA board and I/O bus test points.

A built-in two-processor switch (TPS) feature is available. The TPS allows a single CA to connect two separate host channels (TCS mode), or two channels of a single host (TPS mode). A CA can have two host interfaces (TPS operative) by adding a second CADR card. Only odd-numbered CAs support the TPS feature (see Figure 7-2 on page 7-5). If a CA is equipped with the TPS support, the next CA cannot be installed. A bypass card assuring serial line continuity must be installed instead.

Refer to Figure 7-4 on page 7-6 for a diagram of components and interconnections.

Supported Features

The following features are supported by **CADS** and **BCCA**:

- I/O error alert
- Two-processor switch (TPS)
- High speed transfer (Data in/Data out)
- Data streaming with selectable speeds for 1 MB, 2 MB, 3 MB or 4.5 MB channel speed. These values are the host channel speeds, not the actual transfer rates which are much lower. (The 3745 may be connected to a 4.5 MB channel attachment even if operating at its own speed. In this case, it must be attached beyond the last control unit on the I/O interface which is capable of the 4.5-MB data-transfer rate.)

WARNING: Data streaming cannot be used when the 3745 is connected to systems 308X or 43XX. When a CA defined with the data streaming option is connected to a host which does not support data streaming, abend code 300A is issued.

Non-Supported Features

The following features are not supported:

- Bus extension
- Command retry
- Suppress data (interlock transfer)
- Dynamic reconnection

Configuration

Four channel interfaces are available by means of the IOC BUS. The maximum configuration is four CAs without TPS, or two CAs with TPS. Thus, a maximum of 4 channel interfaces may be installed on a 3745, numbered from 5 to 8.

The Control Program (CP) addresses the CAs by way of the IOC BUS as shown in the following table (Table 7-1):

| Table 7-1. CA Addresses | |
|-------------------------|-------------------|
| CP Address | Channel Addressed |
| 000 | CA 5 |
| 001 | CA 6 |
| 010 | CA 7 |
| 011 | CA 8 |

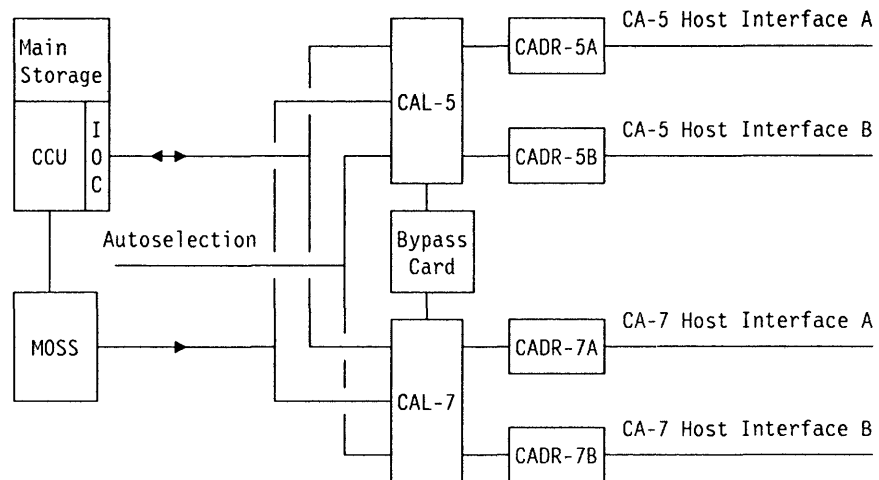


Figure 7-2. CA Configuration with TPS Feature

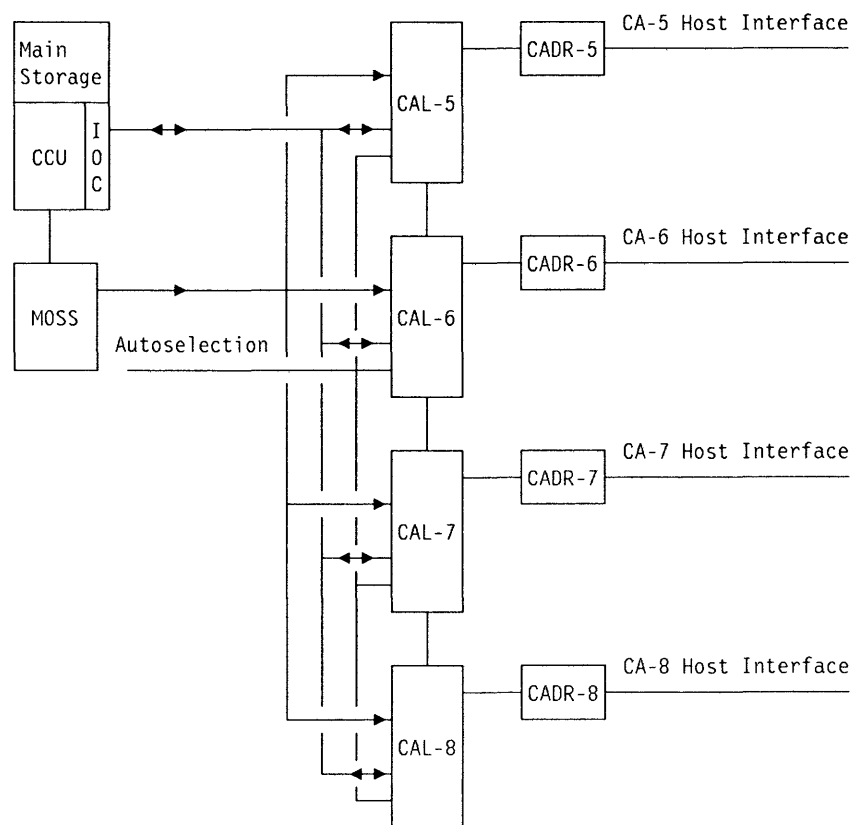


Figure 7-3. CA Configuration without TPS Feature

CA Operating Environment

The CA is used by the 3745 control program (NCP or PEP) to communicate with an application program in the host(s) through various telecommunication access methods.

Physically, channel interface tags and buses attach the CA to the host channels, and IOC buses attach internally the CA to the CCU.

Modes of Operation

The CA can run in either native subchannel (NSC) mode or in emulation subchannel (ESC) mode. The CA operates in the following modes:

- NSC with the Network Control Program (NCP)
- NSC and ESC simultaneously with the Partitioned Emulation Program (PEP)

Notes:

1. With PEP, the NSC is used for loading and dumping.
2. Initial program load (IPL) must always be done in NSC mode.
3. **BCCA** works only in native mode (NCP).

NSC Mode

The NSC mode is supported for all types of host channel (byte multiplex, selector, or block multiplex), and allows servicing any number of lines using only one host subchannel address. Line address decoding is handled entirely by the NCP.

ESC Mode

The ESC mode is supported for byte multiplex channels only, and allows the controller to emulate the 2701 Data Adapter Unit, 2702 Transmission Control, and 2703 Transmission Control using existing host programs and subchannel addresses. This mode requires the Partitioned Emulation Program (PEP) in the 3745, and a separate subchannel address for each PEP line. The ESC mode is not supported with BCCA.

Host Unit Control Word (UCW)/Host I/O Configuration Data Set (IOCDS)

The host system UCW/IOCDS requirements for the controller vary according to the type of control program and features. They are described in the appropriate host *I/O Configuration Program (IOCP) User's Guide and Reference*. UCW/IOCDS requirements are determined as follows:

- One UCW/IOCDS is required for each unique NSC address.
- An additional UCW/IOCDS is required for each emulated subchannel address. For example, a controller running PEP with two ESCs needs three UCW/IOCDS.
- All UCW/IOCDS must be unshared and unfolded.

Overall Operation

The CA is connected to the 370 channel and to the IOC bus, and enables communications over these two data paths.

Data Transfer Methods (PIO and AIO)

Two methods are used to transfer data between the CA and the CCU (via the IOC bus, the switching device, and the adapter bus):

- **Program-initiated operation (PIO):**

PIO mode provides data buffering for up to four bytes, with program intervention required every four bytes.

PIO mode may be used when performance is not critical.

- **Adapter-initiated operation (AIO):**

- When the buffer chaining mode is not set, AIO mode provides a 255-byte buffering. A program intervention is required after each 255-bytes transfer.
- When the buffer chaining mode is set, **BCCA** provides two 255-bytes buffers. A program intervention is required at end of PIU in the write channel program, or at end of PIU chain in the read channel program.

AIO mode should always be used when performance is critical.

CA Instructions

The CA is controlled by instructions issued from the control program.

The NCP and PEP exclusively use adapter input/output halfword (IOH) instructions and input/output immediate halfword (IOHI) instructions.

These instructions examine or set the CA registers, load or read buffers, and initiate cycle stealing.

Note: Throughout this chapter, the channel IOH/IOHI instructions are referred to as input X'nn' or output X'nn'.

CA States

The CA may be in one of the following states:

- **Ready**

In the ready state, the CA accepts instructions, but is not in one of the three active states (initial selection, data transfer, or status transfer).

- **Initial Selection**

The CA enters the initial selection state when an initial selection is started by the host processor. The CA continuously monitors its channel interface for one of its assigned addresses. When it detects one of these addresses, the CA enters the initial selection state, and proceeds with the operation.

- **Data Transfer**

The CA enters the data transfer state when the control program initiates a data transfer sequence. Data is transferred across the interface from the host channel to the CA, or from the CA to the host, by the hardware.

- **Status Transfer**

The CA enters the status transfer state when the control program initiates a status transfer sequence.

- **Disabled**

When the CA is in the disabled state, it does not reply to selection signals coming from the host.

CA Interrupt Requests

The CA can raise interrupt requests to the CCU at level 1 and level 3 (normal mode), and interrupt requests to MOSS at level 1 and level 4 when the MOSS is the owner of the resource.

- **Level 1 Interrupt**

Level 1 interrupt requests to the CCU are caused by check or error conditions.

Level 1 interrupt requests to MOSS are caused by check or error conditions when the MOSS is the owner of the resource (IPL).

- **Level 3 Interrupt**

(See "Level 3 Interrupt Request" on page 7-15.) Level 3 interrupt requests are caused by:

1. Initial selection interrupt requests.
2. Data/status interrupt requests.

- **Level 4 Interrupt**

Level 4 interrupt requests are raised to MOSS in diagnostic mode only.

Accessing CA Registers

The CA registers are accessed by:

- CCU input/output (IOH) or input/output immediate (IOHI) instructions from the CP.
- MOSS input/output (MIOH) instructions, used to initialize or diagnose the CA from MOSS.
- The operator selecting the CA services when using MOSS functions.

The CCU IOH and IOHI instructions are used to transfer the contents of one of the CCU general registers to a selected CA register, or conversely.

Channel Interface Tag Signals Used by the CA

Address in
Address out
Bus in
Bus out
Command out
Data in ¹
Data out ¹
Disconnect in
Operational in
Operational out
Request in
Select in
Select out, and Hold out
Service in
Service out
Status in
Suppress out

¹ Used only with 'High Speed Transfer' and 'Data Streaming' options.

Autoselection

In order to work with a CA, the control program must first select that CA. Two methods are available: output X'07' giving the CA address or autoselection.

Autoselection Mechanism

To perform autoselection, a CA must already be selected, and an output X'07' with bit 0.0 = 1 (enable autoselection) must be executed.

Autoselection will be effective on an input X'0F' execution. At that time, the CA having the highest priority pending level 3 interrupt becomes automatically selected, and the currently selected CA will deselect. If no CA has a level 3 interrupt request, the previously selected CA remains selected.

The priority for the level 3 autoselection mechanism is as follows (from highest to lowest):

1. Priority outbound data transfer L3 interrupt (output X'02' bit 1.4 = 1).
2. Other level 3 interrupts (see "Level 3 Interrupt Request" on page 7-15)

Autoselection (AS) Chain

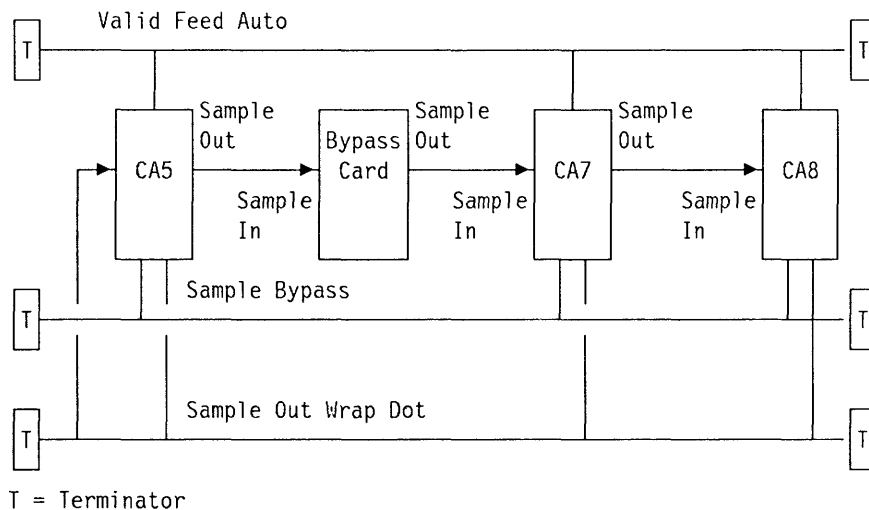


Figure 7-5. Example of Autoselection Chain

The AS chain allows up to four CAs to be installed without specific jumpering, that would be configuration-dependent. The AS chain carries the following signals:

- **Valid Feed Auto:** A bi-directional line is used to synchronize the IOC bus 'Valid Tag' line for all PIO broadcast commands.
- **Sample Out:** Unidirectional line going out from the CA. This line is addressed to the next installed CA in the loop if it has not been removed from the AS chain. The 'Sample Out' line is connected to the 'Sample In' line of the next installed CA.
- **Sample In:** If the previous CA is installed, this line is connected to 'Sample Out' of the previous CA.

- **Sample Bypass:** Bidirectional line used to bypass the CA if the previous CA, or the next installed CA, has been removed.
- **Sample Out Wrap Dot:** Unidirectional line going out from the CA, used by the last CA installed and returned to the first CA (CA 5).

'CA Sample Out' connects all CAs. This line enables the circular-poll function of the AS sequence. That is, polling for the highest priority interrupt starts with the CA following the previously selected CA (or the one after that, if it is no longer in the AS chain): CA 5 follows CA 8, CA 6 follows CA 5,

Autoselection Error

When the hardware detects a problem on the 'sample' chain, no CA will answer at 'TD' time, and an IOC bus timeout will be set.

The control program must determine the failing CA.

Cycle Steal

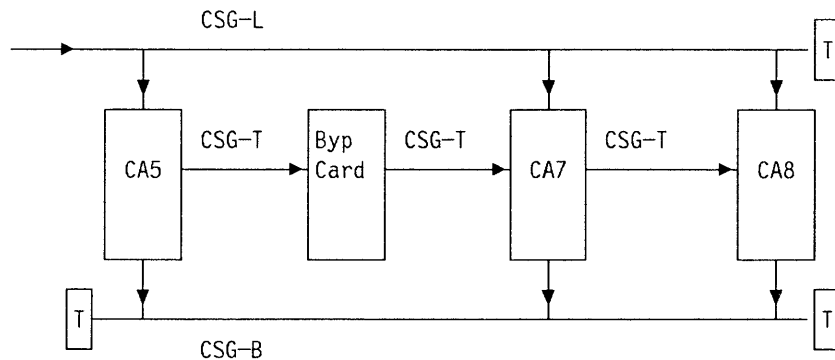
In CS operation, the first halfword sent by the CA is the CSCW, in order to make the following information known to the IOC:

- Adapter type
- Adapter address
- Read/Write operation.

Cycle Steal (CS) Chain

Depending on whether the CA is the first installed, or a previous CA is in the CS chain, the CA will have to monitor either:

- 'CS grant low priority' (CSG-L), or
- 'CS grant low-thru-out' (CSG-T), or
- 'CS grant low-bypass-out' (CSG-B).



Byp = Bypass
T = Terminator

Figure 7-6. Example of Cycle Steal Chain

Removing a CA from the Cycle Steal Chain

To avoid potential host system hangup, no data transfer must be in progress for the CA which has to be removed from the CS chain.

The control program must remove the CA from the cycle steal chain.

CA/MOSS Connection

A 16-line link connects the MCC card to the channel adapters.

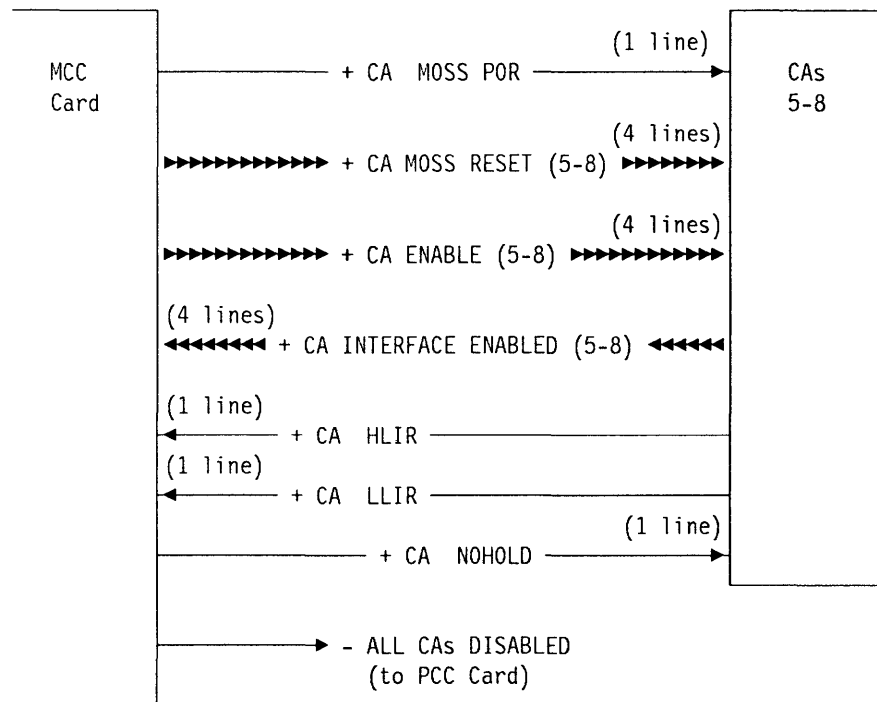


Figure 7-7. CA Link to MOSS

Note: The 'CA NOHOLD' line coming from the MOSS (broadcast line) is used to validate the 'CA MOSS POR', 'CA x MOSS RESET', and 'CA x ENABLE' lines.

Interrupt Requests

The CA generates two major classes of interrupt: CA level 1 and CA level 3 interrupt requests.

Level 1 Interrupt Request

This request is associated with hardware detection of errors in the CA. When an error condition is detected in the CA, a bit is set in the CA level 1 interrupt check bit register X'0D'.

These errors raise a level 1 interrupt request to the CCU by activating IOC bus byte 0, bit 5 (if register X'09' bit 0.4, 'interrupt request disabled', is OFF).

Level 3 Interrupt Request

A CA raises a level 3 interrupt request to the CCU by activating IOC bus byte 1, bit 0 when the I/O is not active (if register X'09' bit 0.4, 'interrupt request disabled', is OFF). There are two types of level 3 interrupt request:

1. CA initial selection request:

- An initial selection sequence occurs if buffer chaining is not set
- An initial selection sequence occurs for commands other than Read, TIO or NO-OP when buffer chaining outbound is set
- An initial selection sequence occurs for commands other than Write, Write-Break, TIO or NO-OP when buffer chaining inbound is set
- NSC status cleared if buffer chaining is not set
- A system reset sequence occurs
- ESC TIO status cleared
- Selective reset
- Interface disconnect
- Channel bus out check

2. Data/status transfer request:

- End of an inbound data transfer if buffer chaining is not set
- End of an outbound data transfer if buffer chaining is not set
- End of a status transfer if buffer chaining is not set
- End of the last inbound data transfer if buffer chaining is set (for example end of PIU)
- End of the last outbound data transfer if buffer chaining is set (for example end of PIU chain)
- Suppress out monitor interrupt.
- A program requested interrupt occurs.
- Any CA level 1 check occurs when the adapter is in a data/status transfer sequence.
- A data streaming time out interrupt occurs
- A channel bus out check
- A selective reset or an interface disconnect when the CA is in data/status/IO error alert sequence.

Two-Processor Switch (TPS)

To be operational, the channel interfaces must be enabled. Both channel interfaces may be enabled, but simultaneous operation over the two interfaces is not permitted. Emulator subchannels are not available when both CA interfaces are enabled.

Any interface may be enabled or disabled from the MOSS. If a channel adapter has a TPS and is attached to a loosely-coupled host, or hosts, only one interface may be enabled at a time on the affected channel adapter. Only ESC operation is allowed in this partitioned mode.

TPS/TCS Mode

When the TPS feature is present, either TPS or TCS mode can be selected in the 3745.

- In **TPS mode** the A and B interfaces are connected to the **same host** and can be enabled at the same time.
- In **TCS mode** the A and B interfaces are connected to **two different hosts** and cannot work at the same time.

Loosely Coupled Host Attachment

The term 'loosely coupled' means either:

1. Two separate hosts each running its own access method (VTAM) with each host attached to an interface of a CA with TPS, or
2. A single host running different access methods, one access method associated with one interface of a CA via a TPS, and the other access method associated with the other interface of the same CA.

When running in a loosely coupled environment, only one of the interfaces may be enabled.

Alternate Path Host Attachment

'Alternate path attachment' is a single access method in a single host having access to both interfaces of a CA with TPS. With alternate path, if the access method issues a start I/O over one channel and that channel is busy with another device, the start I/O can then be issued over the alternate channel.

Note: More than one access method can operate in alternate path hosts, but only one can access both interfaces of a CA with TPS.

When running in an alternate path environment, both CA interfaces can be enabled.

Alternate Path Host Operations

The following TPS definitions must be understood:

1. **Neutral:** The CA is not in communication with either interface, and no active commands exist in the CA.
2. **Switched:** The CA is actively communicating with an interface. If the CA is active with a command, all additional communications are to be made through this interface. The switched state comprises three substates:
 - a. **Instantaneous Allegiance:** The CA enters this state when it traps 'select out' during a channel-initiated sequence, or a poll during a control unit-initiated sequence. If the CA presents DE without unit check (UC) during initial selection, and chaining is not indicated, the CA returns to the neutral state.
 - b. **Long-Term or Implicit Allegiance:** The CA enters this state when accepting a command without presenting DE, or when a No-Op is chained to the next command. This state lasts until the CA presents DE without UC to the channel. The CA remains switched to the same interface throughout. If chaining is not indicated and DE is not stacked, the CA returns to the neutral state.
 - c. **Contingent Allegiance:** This state is an extension of long-term allegiance. When a command ends with a UC status (because of some error), the CA enters this state, even though DE is presented to the command. The CA remains switched to the same interface, and does not return to neutral. The host, on receiving the UC status, issues a sense command to determine the cause of the error. The CA returns to neutral when receiving a command other than No-Op or Test I/O.

| Table 7-2. States of Allegiance | | |
|---------------------------------|--------------------------|---|
| State | Substate | Meaning |
| Neutral | | No allegiance. |
| Switched | Instantaneous Allegiance | Initial selection sequence, present async status, present tagged DE. |
| | Long-Term | From the initial selection till the end of the CCW chain execution. |
| | Contingent | UC status presented to host during initial selection or final status. |
| Return Neutral | | At command end with DE acceptance and no chaining, DE accepted or stacked after busy, async status accepted or stacked, command other than No-Op or Test I/O in contingent state. |

Ending statuses to the host are as follows:

1. **Normal Tagged Status.** This status is presented to the host in response to an initial selection command. The CA remains switched in long-term allegiance to the interface until the control program presents the normal ending status tagged for that interface.
2. **Tagged DE Status.** When the CA has presented a busy status to an interface because the other was in long-term or contingent state, that interface presents the DE status to the host when the CA returns to the neutral state.

This DE status is tagged for that interface by the hardware to clear the busy status previously presented to the host. The tagged DE status frees the host so that it can issue the next command.

3. **Untagged Asynchronous Status.** When operating with tightly coupled processors, the control program can present asynchronous status to the host to initiate a command. This occurs when the CA is in the neutral state with no commands active.

'Request in' is raised to both interfaces, and both interfaces compete for service. The first channel to poll the CA wins. Acceptance of the status causes a level 3 interrupt request, and the CA returns to neutral. If the channel stacks the status, the CA returns to neutral and interrupts the control program. The untagged asynchronous status is then re-offered to both interfaces by the CA when the interrupt is serviced by the control program.

Presentation of Status

Although the CA has two channel interfaces, simultaneous operation of both interfaces is impossible. Therefore, when the CA is switched to one interface, they cannot operate simultaneously. The other interface refuses all channel-initiated sequences. When the CA is in long-term or contingent allegiance on one interface, the other interface presents the status X'10' (short busy sequence) to the channel. When 'select out' is trapped by the non-switched interface, it raises 'status in' and presents X'10'. The host channel responds by dropping 'hold out' or 'select out' and 'address out', thereby disconnecting the interface. The host does not issue further commands until a tagged DE status is received. This status is presented when the active CA interface returns to the neutral state. The CA hardware raises 'request in' and presents the DE status. If the DE status is stacked instead of accepted, the CA automatically tries to present the status again, independently of the control program.

Effect of System Reset

System Reset over Interface with Allegiance: When the CA recognizes the system reset, the CA is completely reset, ending any allegiance condition, and sets an initial selection interrupt request on level 3. However, if a DE status resulting from a previous busy status on the opposite interface is still pending, the CA is not reset.

During system reset, if the opposite channel polls the CA in response to a 'request in' from some other control unit, the resulting 'select out' tag is bypassed. Similarly, any channel-initiated initial selection sequence to either interface causes the CA to switch to that interface, to present the busy status, and to return to the neutral state.

System Reset over Interface without Allegiance: When a system reset occurs on the interface without allegiance, any tagged DE status pending is reset. The rest of the CA is not reset, and no level 3 initial selection interrupt request is made.

System Reset when the CA is in Neutral: When a system reset occurs on a neutral CA, only the pending tagged DE status is reset on the interface, if any. The rest of the CA hardware is not reset, and no level 3 initial selection interrupt request is made.

Note: If a system reset is presented to both interfaces simultaneously, the CA is completely reset, and a level 3 interrupt request is made.

Effect of Selective Reset

Selective Reset over Interface without Allegiance: A selective reset cannot occur on the interface without allegiance. Therefore, the CA hardware is not reset, and no level 3 initial selection interrupt request is made.

Selective Reset over Interface with Allegiance: When the CA recognizes the selective reset, it returns to the neutral state, and issues a level 3 initial selection interrupt request.

No hardware reset occurs, except for a tagged DE status caused by a previous busy status on the opposite interface.

During the initial selection, if the opposite channel polls the CA in response to 'request in' from some other control unit, the resulting 'select out' tag is bypassed.

Similarly, if a channel-initiated initial selection sequence occurs on either interface, the CA switches to that interface, enters the instantaneous allegiance state, presents control unit busy X'70' as the initial status, and returns to the neutral state.

Channel Stop

Channel stop is an error if it occurs during an outbound data transfer. This sequence is detected by the CA hardware when passing bytes over the channel interface. The host processor responds to the CA tag lines 'service in' or 'data in' by raising the 'command out' tag line.

If operating on a byte multiplexer channel, the hardware will disconnect from the channel interface and cause a CA data/status L3 interrupt request.

If operating on a block or selector channel, the hardware will present channel end and request a data/status L3 interrupt. When an input X'02' is executed, bit 0.5 = 1 (channel stop/interface disconnect) will be active.

Interface Disconnect

This condition is detected by the CA hardware when the adapter is either in an initial selection, data transfer or status transfer sequence. 'Operation in' is up, and the host CPU has the 'address out' tag line up, and the 'select out' (hold out) tag line down before the completion of either of the above sequences.

The hardware will then cause either a CA initial L3 interrupt request, or a CA data/status L3 interrupt request, depending on when this condition was detected. Also, the CA will disconnect from the channel interface when working on the channel.

If this condition occurred during an initial selection sequence, the hardware will set 'interface disconnect' which is accessible by an input X'00' instruction (bit 0.1 = 1). If it occurs during a data/status transfer, the hardware will set 'channel stop/interface disconnect' which is accessible by an input X'02' instruction (bit 0.5 = 1).

I/O Error Alert

I/O error alert is a channel interface feature that detects a CA malfunction ('disconnect in' tag line raised).

I/O Error Alert from the CP: The I/O error alert sequence is executed when the CP cannot disable a host interface with an Out X'07' bit 1.7 (set allow channel interface disable). The I/O error alert feature must be present and enabled (out X'02' bit 0.7 = 1).

I/O Error Alert from MOSS: The sequence is executed by the CA when the MOSS raises the 'CA MOSS reset' line and the 'CA nohold' line

Testing and Checking Hardware

The channel adapter contains hardware which allows exercising the checking logic that controls the various error indicators accessible by program with input X'0D', and channel bus checkout which is accessible by inputs X'00' and X'02'.

An imbedded checkout microcode already insures a partial test of the hardware. The checkout result is read via the command 'MOSS in X'4B'. Some functions must be checked by diagnostic program

Autodiagnostics

Autodiagnostics are routines which are run sequentially whenever the microcode is not processing an interrupt.

If an autodiagnostic routine is interrupted, it will not be resumed at the point of interruption, but the next routine will be interrupted instead. This is to avoid a complex save/restore mechanism.

Functions Provided by Diagnostic Program

Selection Modes

Two selection modes ('concurrent' or 'non-concurrent') are available via the command 'MOSS out X'07'. The difference between these two modes resides in the validation of the commands received over the IOC interface. Interrupt requests for these two modes are routed to the CCU or MOSS, as specified in the definition of command 'MOSS out X'07'.

Channel Wrap Possibilities:

Refer to the *MIP* for test procedures.

Internal Wrap: A wrap possibility (on the CADR card) exists which helps the diagnostics in FRU detection. This may also be used to simulate some channel interface sequences. This function is executed via the command 'MOSS out X'4C'.

External Wrap: This function is executed via the command 'MOSS out X'4C'. Two external wrap connectors must be provided in order to wrap the CAs at the channel tailgate, one to wrap tags-out to tags-in, and one to wrap bus-out to bus-in. The CA tag wrap connector P/N 26F1754, and the bus wrap connector P/N 26F1755 can be used (see Figure 7-8, and Figure 7-9 on page 7-22).

Bus and tag terminators must be plugged in the controller out connectors (light gray). This external wrap possibility is provided only to test the drivers/receivers and tailgate wiring of the channel interface.

CA Interface Wrap Plugs

Tag Wrap Plug P/N 26F1754

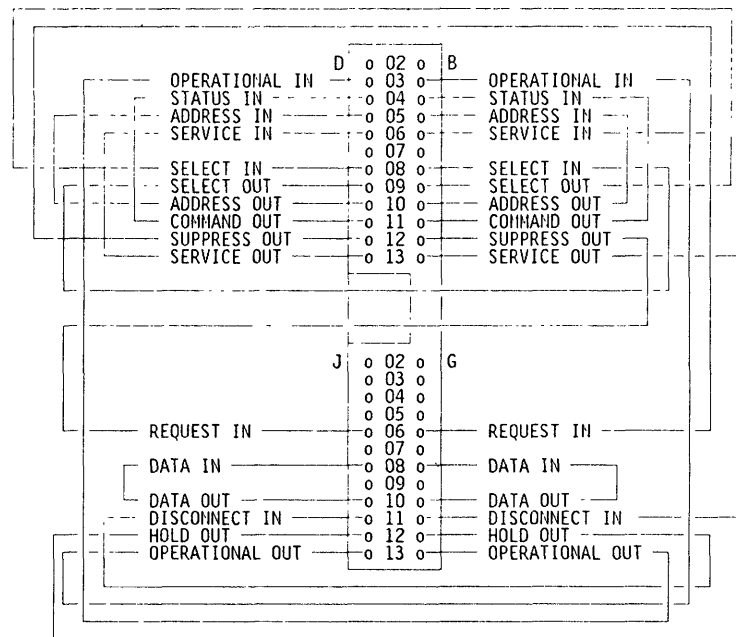


Figure 7-8. Tag Wrap Plug Wiring (P/N 26F1754 - Mating Side)

Bus Wrap Plug P/N 26F1755

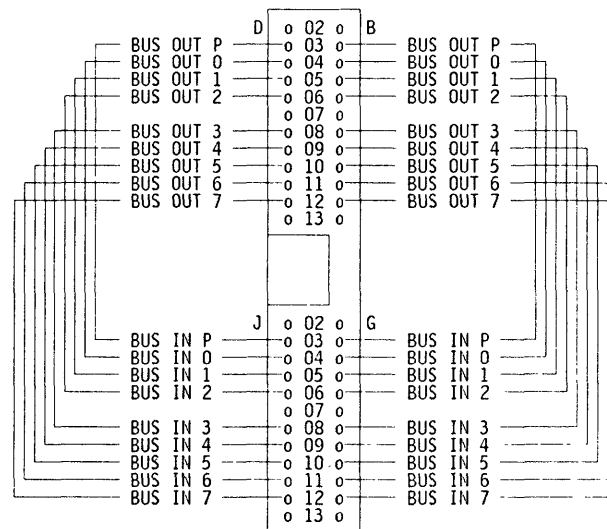


Figure 7-9. Bus Wrap Plug Wiring (P/N 26F1755 - Mating Side)

CA Services

Refer to the *Service Functions*, SY33-2069, for more details.

The command Out X'07' from MOSS with bit 0.2 = 1 is provided to select a specified CA in order to enable CA services from MOSS. This function allows to:

- Display CA status.
- Display interface test points.
- Enter host attachment information at installation time.
- Issue specific commands to the CA, such as:
 - Start/stop trace
 - Dump
 - Display storage and registers
 - Reset
 - Initialization.

CA Interface Display

Refer to the *Advanced Operations Guide*, SA33-0097, for more details.

As soon as the local console is powered ON, the CA interface display screen appears. This screen can also be displayed by selecting the channel interface display (CID) function from MOSS menu 2.

The information displayed is:

- Host attachment information
- NSC address
- MOSS enable/disable request
- Interface status (enabled/disabled).

The CID screen also allows to modify the enable/disable request.

CA Initialization

The CA initialization is performed when a CA receives a POR signal, either at general power ON, or through the MOSS 'Reset' command.

Initialization First Part (Checkout)

At checkout completion, the CA is in the following state:

1. IOC bus interconnection enabled.
2. MOSS interconnection enabled.
3. Host interfaces disabled.

The results of the checkout are available to the MOSS microcode.

Initialization Second Part

This part is performed during IPL phase 1A, or during the 'Restore' CACM command. The MOSS microcode initializes each CA.

Initialization Third Part (Chaining)

Only those CAs that passed the first and second parts of the initialization can be installed in autoselection and cycle steal chains. Chaining process is performed during IPL.

Only when all the CAs are initialized, can the control program start.

Chapter 8. Maintenance and Operator Subsystem (MOSS)

| | |
|---|------|
| MOSS Unit in the 3745 Model 130/150/170 Data Flow | 8-2 |
| Introduction | 8-3 |
| MOSS Processor | 8-3 |
| Packaging | 8-3 |
| MOSS Reset | 8-4 |
| MOSS Functions | 8-6 |
| MOSS States | 8-7 |
| MOSS Changes of State | 8-7 |
| Branch Trace | 8-9 |
| Branch Trace Buffer | 8-9 |
| Conditional Branch Trace | 8-10 |
| Mailbox Description | 8-11 |
| Exchange Time Outs | 8-11 |
| CCU to MOSS Communication (Out Mailbox) | 8-12 |
| MOSS-to-CCU Communication (In Mailbox) | 8-12 |
| Mailbox Commands | 8-13 |
| LSSD Operation | 8-15 |
| Data Flow | 8-15 |
| LSSD Testing Circuit | 8-15 |
| MOSS/Disk Drive Interaction | 8-17 |
| Disk Commands | 8-17 |
| Read/Write Operations | 8-18 |
| MOSS/Operator Console Connections | 8-18 |
| Remote Support Facilities (RSF) | 8-18 |

MOSS Unit in the 3745 Model 130/150/170 Data Flow

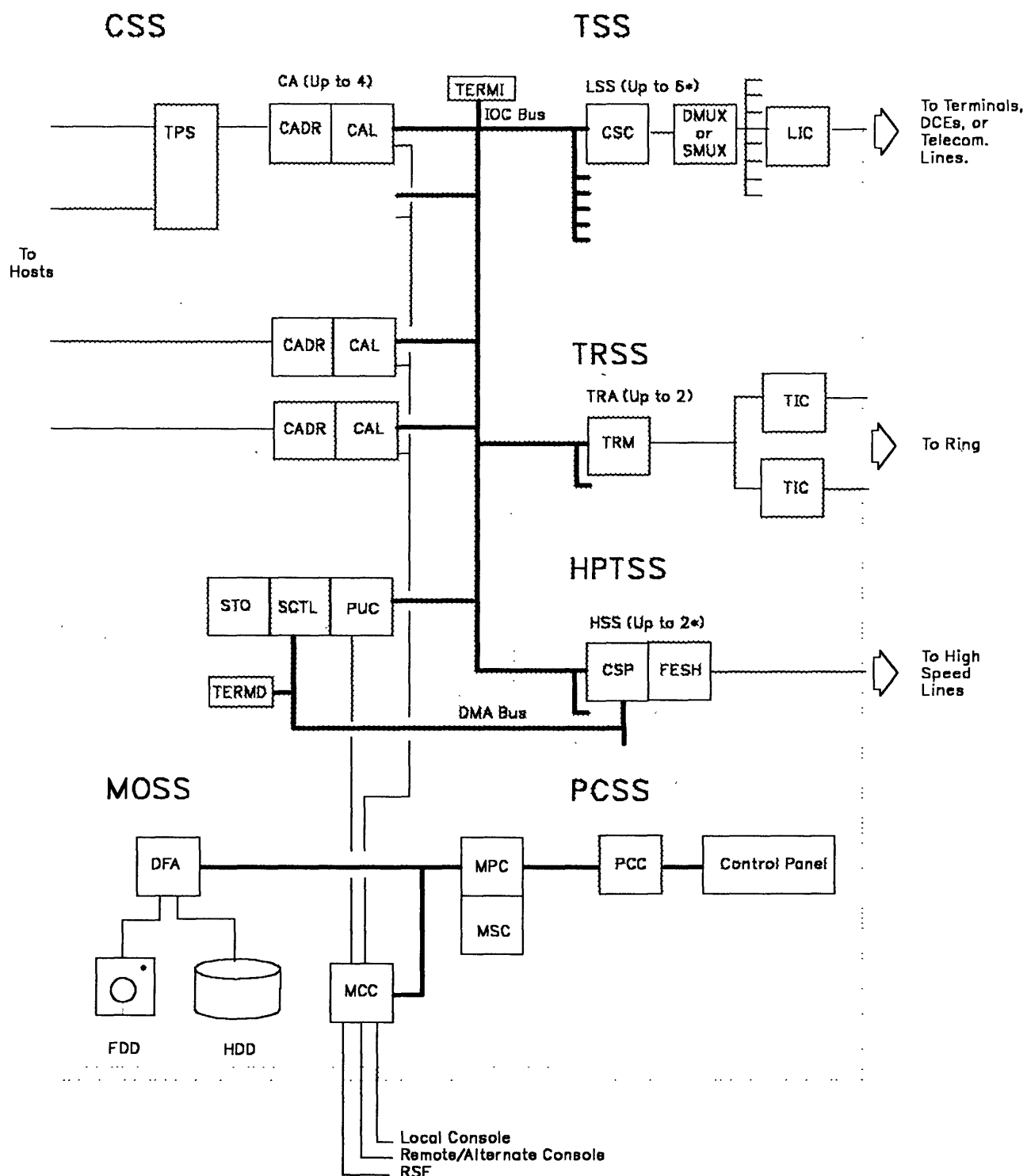


Figure 8-1. MOSS Unit in the 3745 Model 130/150/170 Data Flow

Introduction

MOSS is the service processor of the communication controller. It performs IPL functions, machine initialization, and provides the operator with tools for problem determination.

The 3745 Model 130/150/170 MOSS is based on a microprocessor which controls a 2MB main storage, the MIOC buses, the channel adapters, the consoles (local, remote/alternate, and RSF), the disks (hard disk and flexible disk).

MOSS interconnects with the power control card which drives the control panel. The MOSS logic, the flexible disk drive, and the hard disk drive are powered by a specific power supply, so that removing power from the MOSS board does not impair the operation of the system.

MOSS Processor

The MOSS processor drives the MOSS. It has its own instruction set, and does the usual processing activities: instruction fetching, instruction decoding, and instruction execution.

The MOSS processor responds to interrupts from the CCU, from its attached adapters (LAs, CAs), and from its own error detection circuits. It controls access to the MOSS storage. The MOSS processor is packaged on the MPC card.

Packaging

Refer to Figure 8-3 on page 8-5 for MOSS structure. The MOSS board includes:

- A MOSS processor card (MPC) with a 32-KB ROS, a time-of-day (TOD) clock, a storage error correction and checking circuit. The MPC card connects UC buses, the MSC card and the power control card (PCC).
- Note:** Each time that the MOSS is reset, a led is lit on the MPC card. This led is turned OFF by the ROS microcode when the connection with the PCC card is established.
- A 1-MB RAM MOSS storage card (MSC card).
- A power control card (PCC), which interconnects the MOSS control panel to the MPC card. The PCC card is powered by PS2 in the primary power box, in order to allow the remote power function, and manages the whole power control subsystem (see Chapter 10 for details).
- A MOSS and console adapter card (MCC) containing:
 - One adapter module for CCU bus
 - One adapter module for 4 channel adapters
 - Three console adapter modules providing three ports for:
 - A local console
 - A remote/alternate console
 - An RSF modem
 - One oscillator, and drivers/receivers (EIA V.28/RS-232-C).

- A disk file adapter card to attach:
 - One flexible disk drive (FDD),
 - One hard disk drive (HDD).

Note: See pages YZ-031 for MOSS card and connector locations, and pages YZ-331 for test points.

MOSS Reset

When a MOSS reset occurs, the led on the top of the MPC card is turned ON. The panel displays code 001, a read MMIO bus is started by the MOSS code. If the result is good, the led is turned OFF and the display code goes to 002. If the result is not good after a two-second time out, the led starts blinking.

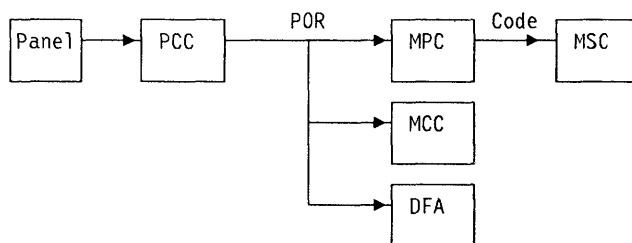


Figure 8-2. MOSS POR Flowchart

- MPC reset consists of terminating the operation in progress and initializing internal registers. The reset sequence does not initialize main storage, or register space. Those are initialized by storing into them with good parity. Several specific control areas are also initialized by the IML program.
- A MOSS reset ONLY is performed with *Function = 1* (MOSS IML) at the control panel.

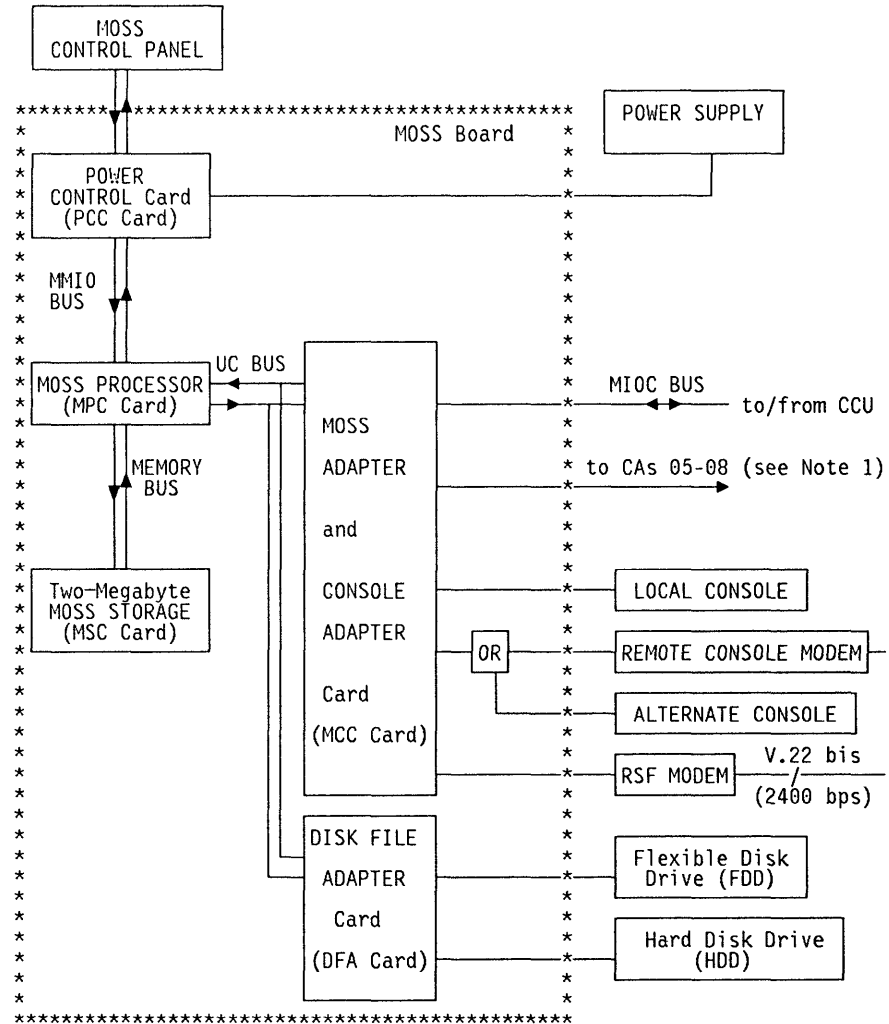


Figure 8-3. MOSS Structure

Note 1: 'To CAs 05-08' is a control line that allows enabling/disabling or resetting the CAs.

MOSS Functions

The maintenance and operator subsystem (MOSS) provides access to the 3745 and makes the following components easier to maintain:

- Control program (NCP, PEP).
- Central control unit (CCU).
- Channel adapters (CA).
- Line adapters (TSS, HPTSS, TRSS, and LA microcode).
- Line interface cards (LICs/TICs).
- The MOSS processor itself, its microcode, and the I/O adapters used to attach the control panel, the consoles, the flexible and hard disk drives, the CCU, and the channel controls.

Using the MOSS, the service personnel can:

1. Initialize the 3745 with:
 - Standalone IPL from disk
 - Hardware checkout diagnostics
 - IML/IPL from the control panel or the console
 - CCU IPL
 - Line adapter IML.
2. Maintain the 3745 with:
 - Remote support facility (RSF)
 - Concurrent diagnostics.
 - LIC hot plugging
 - Box event handling (error recording, analysis and display, alert/alarm generation)
 - Line services (line wrap tests, line interface display, token-ring interface display)
 - CCU control program procedures
 - Machine history files: configuration data file (CDF), machine level table (MLT), IPL port table
 - Password management
 - Microcode utilities (dumps and file transfer to host, MCF, RECFMS)
 - CA control/status display from the console
 - Machine status area display.
3. Use 3745 services such as:
 - CCU services
 - TSS services
 - TRSS services
 - CA services
 - Power services
 - Time services.

MOSS States

Some states are viewed by the NCP or PEP (DOWN OFFLINE, ONLINE). Other states exist when the NCP or PEP is not loaded in the CCU (DOWN, ALONE).

- **MOSS DOWN** indicates that no program is running in the MOSS or that MOSS IML is in progress. In this state the 'MOSS Inoperative' line is up and the CCU interface is disabled.
- **MOSS ALONE** indicates that the MOSS microcode is loaded and operational (CP not loaded).
- **MOSS OFFLINE** indicates that the MOSS microcode is running in the MOSS, but that communication cannot be established with the NCP/PEP (except for exchange with CLDP, and NCP/PEP initialization, which are part of the 3745 system IPL). In this state, the CCU is enabled.
- **MOSS ONLINE** indicates that the MOSS microcode is running and allows communications with the NCP/PEP. In this state, the CCU interface is enabled.

(Numbers refer to the steps of "MOSS Changes of State")

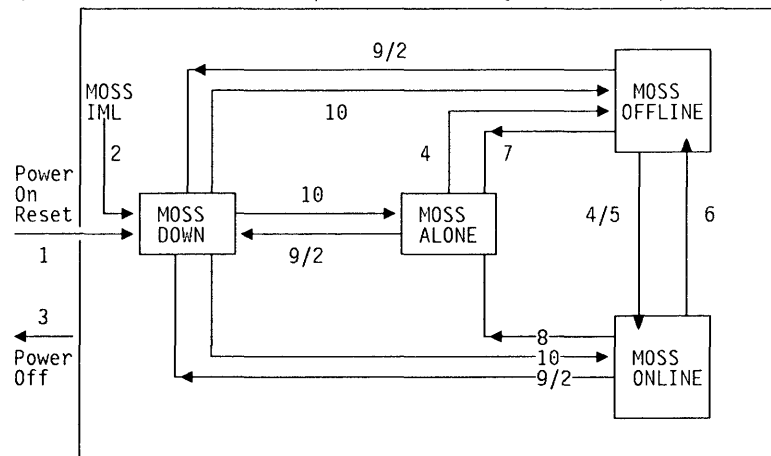


Figure 8-4. MOSS Changes of State

MOSS Changes of State

The following is a description of the events and actions that cause a MOSS state change. Step numbers identify events and actions in Figure 8-4.

Step 1. POWER ON RESET, according to panel option:

- Panel option = MOSS IML ('Function' = 1). The MOSS DOWN state is entered during the time MOSS IML is performed, then MOSS ALONE [10] is entered and is kept until further action.
- Panel option = NORMAL or DISKETTE MODE. The MOSS DOWN state is entered during the time MOSS IML is performed, then MOSS ALONE [10] is entered, then MOSS OFFLINE [4], then MOSS ONLINE [5]. This is the full system IPL.

Step 2. MOSS IML request at panel (Function = 1). The same sequence occurs as in step 1 above, according to the panel option.

Step 3. POWER OFF. The full system leaves its current state.

Step 4.

- A NORMAL IPL has been requested, [1] or [2].
- 3745 IPL has been requested from the console menu.

Step 5.

- A NORMAL IPL has been requested, [1] or [2].
- 3745 IPL has been requested from the console menu.
- The MOSS operator enters a MOSS ONLINE command from the console to exit from the OFFLINE MODE.

Step 6.

- The MOSS operator enters a console MOSS OFFLINE command.
- In case of hardware error on the MOSS/CCU interface during the processing of a mailbox.
- In case of a time out occurring while processing exchanges from the NCP.

Step 7.

- During a NORMAL IPL the process aborts and cannot be completed successfully.
- A channel or program IPL request is presented to MOSS.
- A CCU hard check is presented to MOSS.

Step 8.

- A channel or program IPL request is presented to MOSS.
- A CCU hard check is presented to MOSS.

Step 9.

- A MOSS abend occurred.
- START panel request while the MOSS was in the OFFLINE, ONLINE, or ALONE state.
- IML command entered at the console.

Step 10.

- If the reason to enter the MOSS DOWN state was an abend or an IML command entered at the console, after MOSS re-IML the final state is the one which was interrupted by the abend.
- If the reason to enter the MOSS DOWN state was a START panel request or an IML command entered at the console, after MOSS re-IML the final state depends on the function option selected. In case of START IML MOSS, the final state is the same as the one which was interrupted, except for MOSS ONLINE which is forced to MOSS OFFLINE.

Branch Trace

The branch trace facility allows the CCU hardware to record the non-sequential operations occurring in the flow of the CCU control program, into a predefined buffer.

Any time a branch actually occurs in the CCU, the 'come from' and the 'go to' addresses are stored into the buffer, as well as the corresponding 'come from' and 'go to' program level(s).

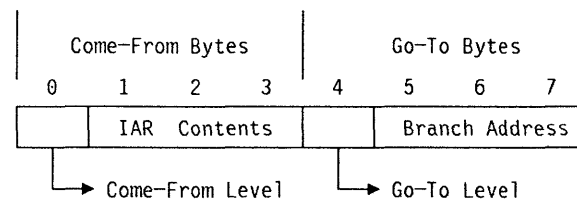
A non-sequential operation takes place when:

- A conditional or unconditional branch instruction is executed.
- An instruction modifies the instruction address register (reg 0 of the active program level).
- A new program level is entered, due either to a program control interrupt issued by the CCU control program, or to an external interrupt caused by any adapter, or to an EXIT instruction.

When requested, the MOSS loads the branch trace registers with the upper and lower branch trace limits, and with the branch trace table definition (address in main storage and length). The branch trace registers are located in CCU local storage.

The MOSS then requests the CCU to record the 'come from' and 'go to' information of any actual branch in the branch trace buffer.

The branch trace information is stored in two contiguous storage positions as follows:



Branch Trace Buffer

The branch trace buffer allocation is made at Control Program generation time, by providing the buffer starting address and the buffer length as system generation parameters. When IPL is performed on the CCU, the buffer allocation values are passed over to MOSS.

The MOSS defines the branch trace buffer with MOSS Write LS (indirect operations). When the buffer is full, either the CCU is stopped and the MOSS is interrupted, or the MOSS only is interrupted.

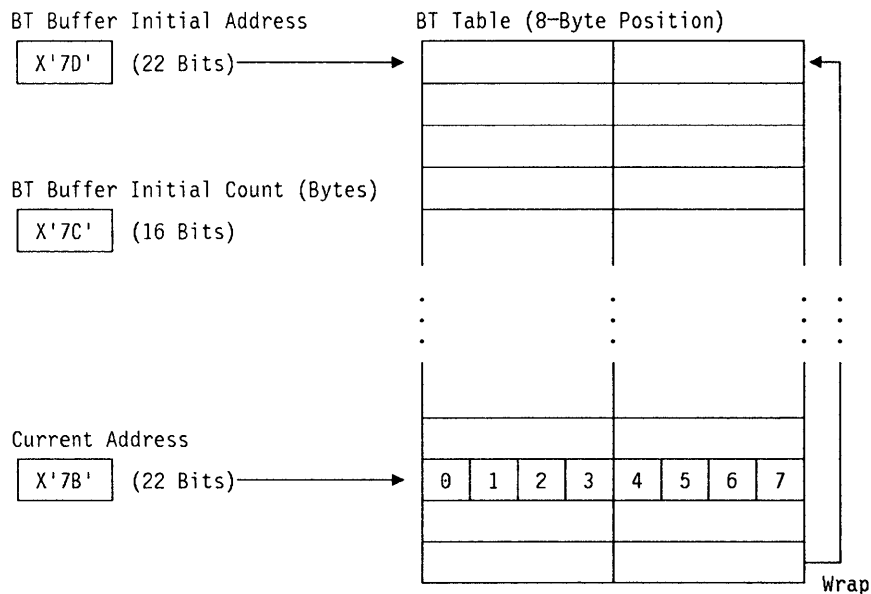


Figure 8-5. Branch Trace Buffer

If wrap is specified, 'branch trace buffer full' causes the branch trace count to be reinitialized, and the branch information to overlay the start of the branch trace buffer.

Under certain circumstances, the branch trace buffer may contain extra records showing the entry and the exit of the CCU through some program level, without instruction execution at that level.

Conditional Branch Trace

The conditional branch trace allows to start and stop a branch trace from the control program itself without MOSS intervention. The branch trace default values are initialized by MOSS at IPL time.

In order to avoid contention between MOSS and CP requests with different options, starting a branch trace is inhibited if there is one already active.

Mailbox Description

The NCP/PEP and the MOSS communicate through CCU storage areas called mailboxes. These mailboxes are located in the 32-KB area reserved for MOSS use, at the top of CCU main storage (see Table 8-1).

Table 8-1. Mailbox Addressing in CCU Storage

| CCU Storage (32K Top Area) | Address in 4MB Storage |
|---|------------------------|
| Spare (192 bytes) | X'3FFFFF' X'3FFF40' |
| NCP Out Mailboxes (32 bytes) | X'3FFF3F' X'3FFF20' |
| NCP In Mailboxes (32 bytes) | X'3FFF1F' X'3FFF00' |
| Unused | X'3FFEFF' X'3FA400' |
| MOSS to Line Adapter Data Area (8704 bytes) | X'3FA3FF' X'3F8200' |
| Line Adapter Mailboxes (512 bytes) | X'3F81FF' X'3F8000' |
| Top of Non-Reserved Storage | X'3F7FFF' |

For a detailed description of the mailbox contents, see the *3745 Principles of Operation*, GA33-0102.

Exchange Time Outs

The requestor fills in his mailbox and posts an interrupt to the receiver. The receiver grants the interrupt, decodes the mailbox contents, posts a status in the mailbox, and interrupts the requestor. Throughout this time, the mailbox is busy with the requestor. A timer is used to provide a protection against requests that are not answered.

On the NCP side, if a time out occurs, the MOSS is considered down and an alert is sent to the host.

On the MOSS side, if a time out occurs, a return code is passed to the requesting application to signal this situation. In this case, the NCP/PEP is probably down and operator intervention may be required.

CCU to MOSS Communication (Out Mailbox)

The out mailbox is used to pass requests from the NCP/PEP to the MOSS and for the MOSS to post the status response.

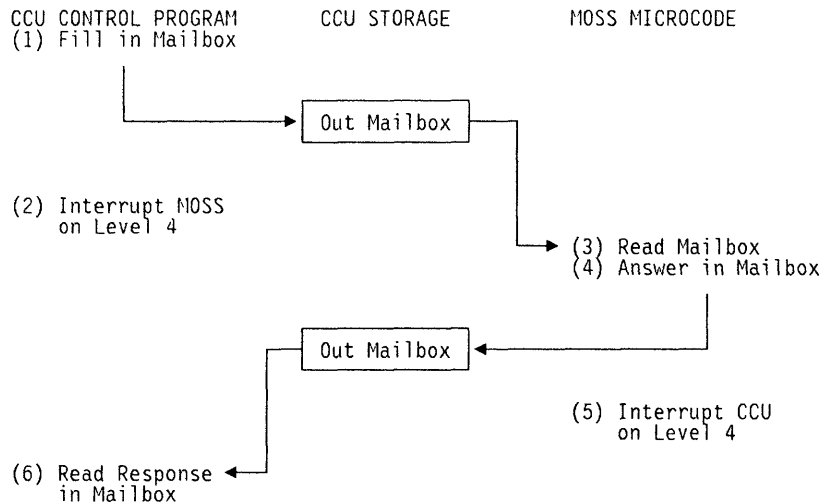


Figure 8-6. Out Mailbox Exchange Procedure

MOSS-to-CCU Communication (In Mailbox)

The in mailbox is used to pass MOSS requests to the NCP/PEP and for the NCP/PEP to post the status response.

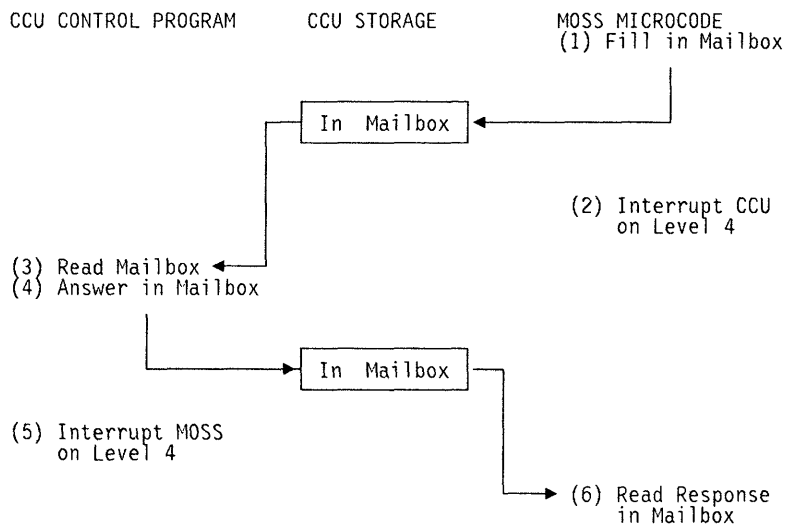


Figure 8-7. In Mailbox Exchange Procedure

Mailbox Commands

The following table (Table 8-2) shows the commands sent by the MOSS to the CCU control program (IN mailboxes), and in which functions they are involved.

| Table 8-2. NCP Mailbox In Commands | | |
|------------------------------------|-----|--|
| Function | Hex | In Command |
| CLDP | C1 | Line adapter IML complete |
| | C2 | Roll in complete |
| | C3 | IPL from disk complete |
| | C4 | Control information response |
| | C5 | Dump records saved |
| Initialization | A3 | CP parameter saved |
| | A4 | CDS information available |
| | B2 | Reissue port swap |
| Normal | 86 | Transfer PIU: <ul style="list-style-type: none"> • Solicited response • Unsolicited reply • Dump storage response |
| | 89 | Wrap test request |
| | 8A | Stop wrap test |
| | 8C | Connect line adapter |
| | 8D | Disconnect line adapter |
| | 8E | Request buffer |
| | 8F | Free buffer |
| | 90 | MOSS offline |
| | 91 | MOSS online |
| | 92 | Port swapped |
| Reconfiguration | 84 | Update CDS |
| | | 01: Delete ports, 02: Add ports |
| | | 03: Delete line, 04: Add line |
| | | 05: Change CDS header |
| | | 06: Insert CA, 07: Delete CA, 08: Change CA |
| CA Services | 93 | Disconnect CA |
| | 94 | Connect CA |
| | | 01: Initialize procedure |
| | | 02: Cancel procedure |
| | 95 | AS/SC chain update |
| | | 01: Remove CA from AS chain |
| | | 02: Remove CA from CS chain |
| | | 03: Insert CA into AS chain |
| | | 04: Insert CA into CS chain |
| | 96 | Install CA |
| | | 01: Start INSTALL procedure |
| | | 02: Cancel INSTALL procedure |

The following table (Table 8-3) shows the commands sent by the CCU control program to the MOSS (OUT mailboxes), and in which functions they are involved.

| Table 8-3. NCP Mailbox Out Commands | | |
|-------------------------------------|-----|-----------------------------|
| Function | Hex | Out Command |
| CLDP | 41 | CP loaded |
| | 42 | Roll in saved storage |
| | 43 | IPL from disk |
| | 44 | Control information |
| | 45 | Dump records built |
| Initialization | 23 | CP parameter |
| | 24 | Request hardware CDS |
| | 25 | CP initialization complete |
| | 26 | Request hardware CDS (swap) |
| | 27 | Request reissue port swap |
| Normal | 06 | Transfer PIU: |
| | 07 | • Request from NCP |
| | 08 | • Dump storage request |
| | 09 | NCP/PEP BER transfer |
| | 0C | Buffers now available |
| | | Wrap test results |
| | | Time/date valid |

LSSD Operation

Level sensitive scan design (LSSD) operations are powerful diagnostic tools used especially during IML, or when running CCU diagnostics.

LSSD datas are kept in the file CDF. They can be displayed with the CDF file.

In LSSD operations, the MOSS can verify or change the status of any discrete CCU latch. Such operations can be performed after any CCU cycle, by stopping the CCU clock.

Data Flow

Figure 8-8 on page 8-16 is a simplified representation of the data flow. Normally, the complete CCU can be represented with 12 strings each having an average of 100 SRL statuses.

The 'SRL out' lines present their status to the following combinational logic at clock pulse B. The resulting combinational logic values set the 'SRL In' lines at the next clock pulse C.

LSSD Testing Circuit

For testing purposes, the above 'SRL Out' are connected to 'SRL In' lines in a sequential string as follows (Figure 8-9 on page 8-16). The 'In' and 'Out' lines go to their combinational logics. 'Scan In' is the string input; 'Scan Out' is the string output.

With LSSD operations the MOSS can:

1. Read the CCU SRLs for diagnostic purposes ('scan out' to MOSS scan register).
2. Set/reset the CCU SRLs to a preset value for initial CCU reset (scan register to 'scan in').

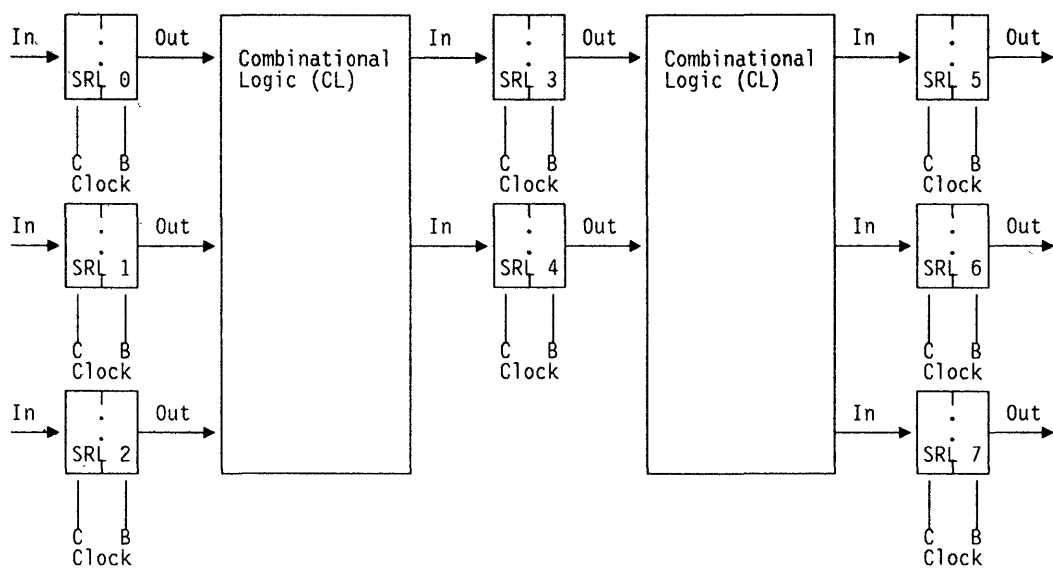


Figure 8-8. Simplified Data Flow

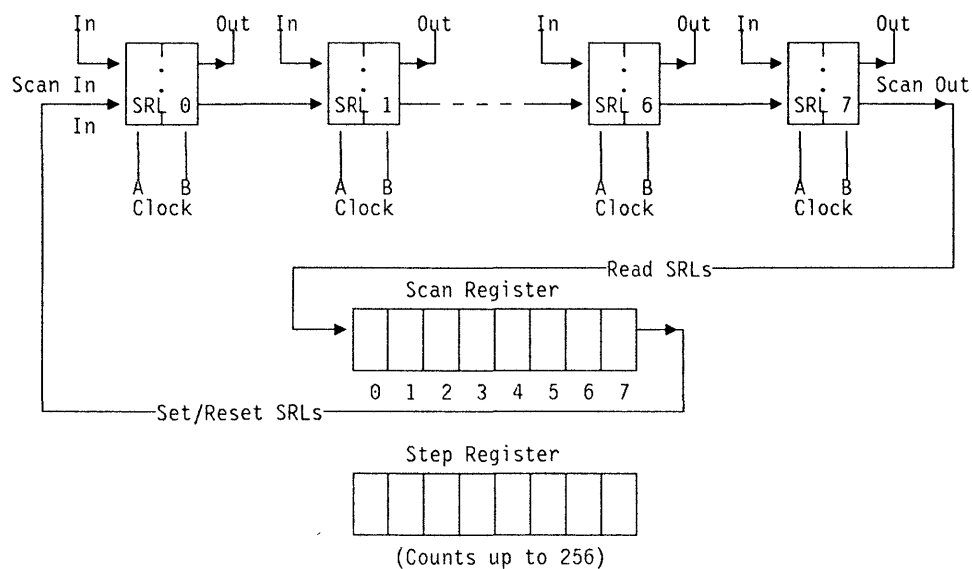


Figure 8-9. LSSD Testing Circuit

MOSS/Disk Drive Interaction

The hard/flexible disk drives are described in Chapter 9 of this manual.

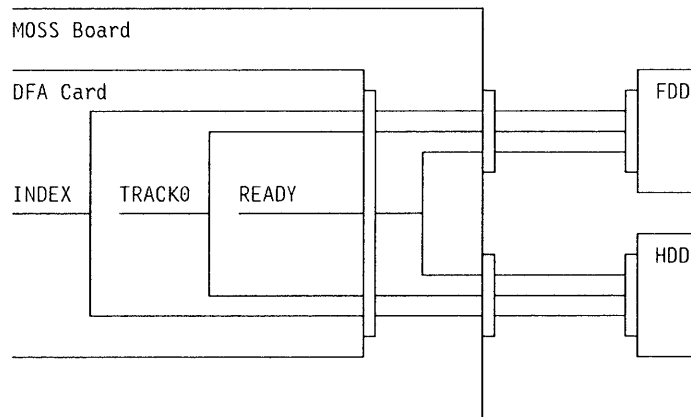
Disk Commands

The MOSS processor controls the disk file adapter (DFA) and its attached drives via program or channel I/O commands on the MOSS external UC bus. These commands allow the MOSS to:

1. Start or stop the flexible and hard disk drives.

Notes:

- DC voltages to disk drives are stopped when there is no activity on disks for 15 minutes (see "Disk and Diskette Drive On/Off Control" in Chapter 9 for details).
- There are three lines READY, INDEX, and TRACK0 which are common to both the HDD and the FDD. READY line is doted on the MOSS board; INDEX and TRACK0 are doted on the DFA card.



2. Set or sense the file adapter registers.
3. Seek head carriage.
4. Engage the heads (position the heads close to the disk/diskette surface).
5. Read data from the disk/diskette.
6. Write data to the disk/diskette.
7. Read back the data for checking purposes.

The DFA rejects commands that are invalid, or have a bad parity. A command that temporarily cannot be serviced by the disk/diskette drive is considered invalid.

The command is not retried. It causes a machine check/program check end status indication.

Read/Write Operations

Read or write operations are initiated via PIO commands. Data is exchanged directly with the MOSS storage through the DFA. (Halfword cycle stealing operation.)

MOSS/Operator Console Connections

The operator consoles can be attached to the processor via the MCC card. The MOSS can control only one console at a time.

Chapter 9 of this manual gives details on operator consoles themselves, and the *3745 Models 130/150/170 Service Functions*, SY33-2069, describes how the service functions are used from the 3745 console.

Remote Support Facilities (RSF)

The MOSS-to-RETAIN connection is made with a BSC protocol at 1200/2400 bps (V.22 Bis or V.23 CCITT interface, depending on the country), via a duplex external modem with the auto-answer feature.

The IBM RSF Modem operating characteristics are as follows:

- Connection over a switched line
- Duplex transmission
- Synchronous transmission
- Auto-answer feature
- Transmission speed: 1200/2400 bps
- Clocking by the modem clock
- DSR control by the modem

Chapter 9. Control Panel, Operator Consoles, Disk/Diskette Drives

| | |
|--|------|
| Control Panel | 9-2 |
| Overview | 9-2 |
| Control Panel Layout | 9-3 |
| Control Panel Connection | 9-5 |
| Control Panel Operation | 9-5 |
| Operator Consoles | 9-6 |
| Highlights | 9-6 |
| Console Connection | 9-7 |
| 3161 Console 3727 Console Key Conversion | 9-8 |
| Console Setup and Maintenance | 9-8 |
| Disk/Diskette Drive | 9-9 |
| Hard Disk Drive (HDD) | 9-9 |
| Flexible Disk Drive (FDD) | 9-10 |

Control Panel

Overview

The control panel consists of:

- A ten-digit alphanumeric display
- A key pad with seven keys
- A unit emergency power OFF switch
- An overlay corresponding to national language requirements
- A power ON lamp.

See "Control Panel Layout" on page 9-3 for details.

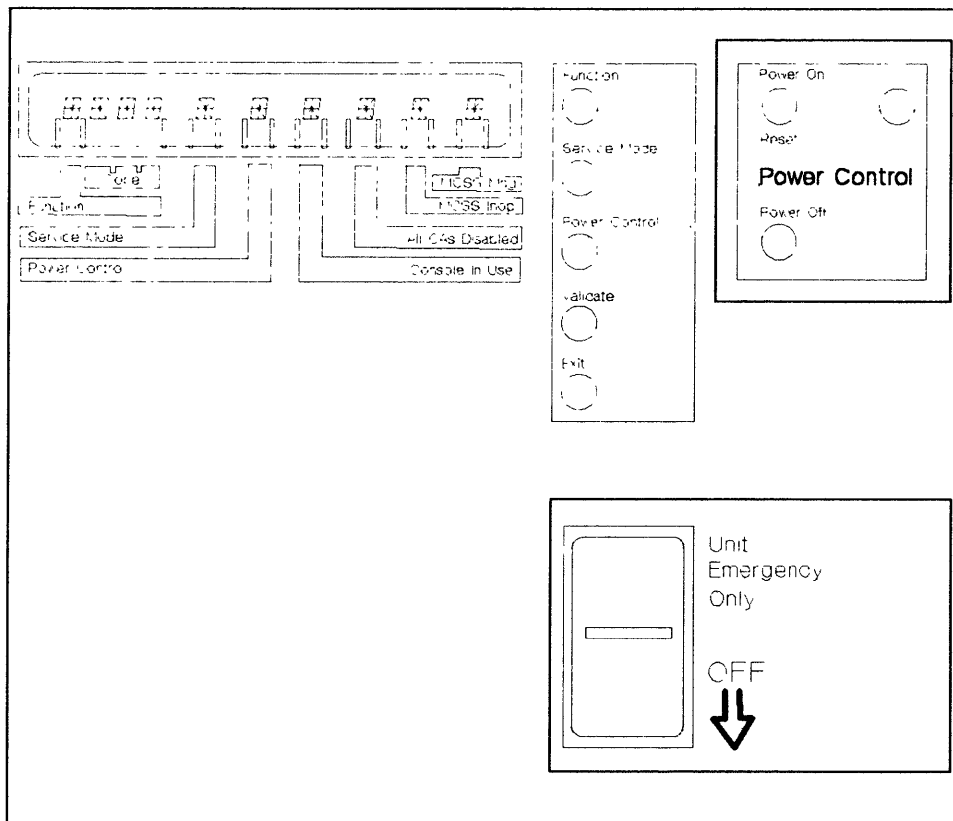
The control panel carries keys and indicators required for:

- Controlling the power system
- Activating MOSS functions, control panel test, power bus test
- Hexadecimal display code to operator.

The 3745 control panel stays powered ON when the 3745 is powered OFF. This allows information on power control and service to be displayed.

The 'Function', 'Service' and 'Power control' keys allow the operator to scroll the different options. The option is performed by pressing the 'Validate' key, or cancelled by pressing the 'Exit' key. Refer to the *Basic Operation Guide* for more details on the control panel functions.

Control Panel Layout



(*) For code definitions, refer to Appendix A in the *MIP*.

Figure 9-1. Control Panel

Control Panel Reference Card

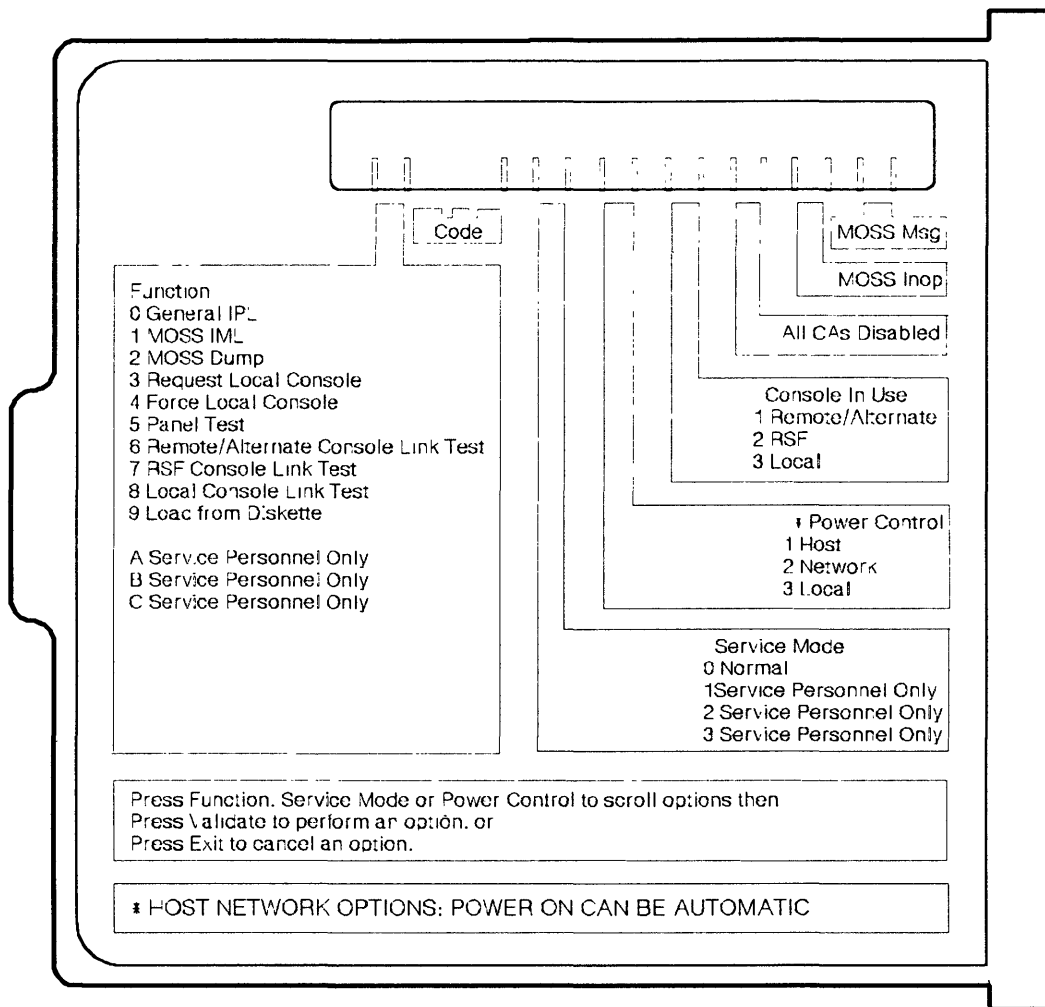


Figure 9-2. Control Panel Reference Card

Control Panel Connection

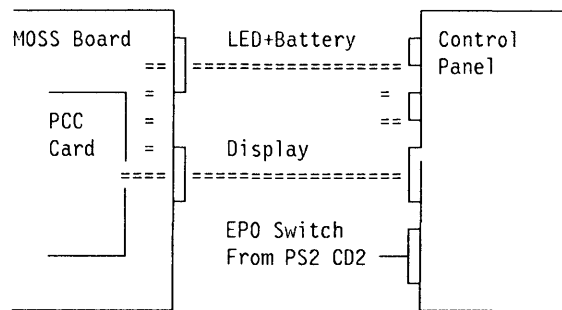
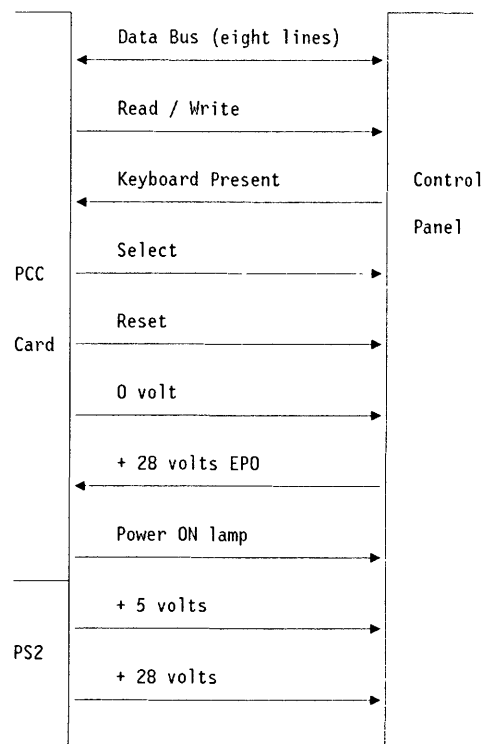


Figure 9-3. Control Panel Connection

For component locations on MOSS board and control panel, see YZ pages.



Control Panel Operation

For control panel operation and tests, refer to *Basic Operation Guide* and *MIP*.

Operator Consoles

Highlights

The 3745 offers three different console interfaces. Activation of these attachments are under MOSS control via the MCC card. Only one of these attachments may be active at a time.

The consoles whose characteristics are listed below are used either by the customer or by IBM service personnel.

For more details on console configuration, see *Console Setup Guide* SA33-0158.

Local Console and Alternate Console

The local console, which is mandatory, and the alternate console operate with interface CCITT V.24 in duplex start-stop mode at 2400 bps.

- IBM 315x Model 110, 160, 310, 360, 410 or 460 Display Station in native mode or in IBM 3101 emulation mode.
- IBM 316x Display Station Model 11, 12, 21 or 22 in IBM 3101 emulation mode.
- IBM 3727 Display Station (keyboard overlay provided in shipping group).
- IBM PS/2* able to run under OS/2* extended edition with Communication Manager emulating the 3101.
- Any equipment providing equivalent functions operating in IBM 3101 emulation mode.

For details about the consoles to be used on the 3745, refer to the *Console Setup Guide*.

Remote Console

Operates in duplex start-stop mode at 1200 bps.

- IBM 315x (in the USA and Canada only, and only if an IBM 5841, 5842, or 5853 modem for USA or 5853 modem for Canada is used at the 3745 end) in native mode.
- IBM 316x Display Station Model 11, 12, 21 or 22 in IBM 3101 emulation mode.
- IBM PS/2 able to run under OS/2 extended edition, with Communication Manager emulating the 3101.
- IBM PC in IBM 3101 emulation mode.
- Any equivalent equipment emulating the IBM 3101 and having an interface CCITT V.24, (EIA 232D).

For details about the consoles to be used on the 3745, refer to the *Console Setup Guide*.

Console Sharing Via IBM 7427

The IBM 7427 Console Switching Unit can be used with the 3745 for 31XX and 3727 consoles.

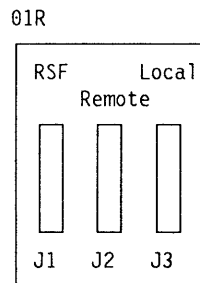
A maximum of four communication controllers can share a local console.
A maximum of six communication controllers can share an alternate console.

Remote Support Facility (RSF)

Attached to the 3745 over the public switched network via a modem.

For details, see page 8-18.

Consoles Tail Gate



- The J1 connector is for the RSF console.
- The J2 connector is for the remote or alternate console.
- The J3 connector is for the local console.

See YZ pages for details.

Console Connection

For console connection, cable wiring, cable length, and cable part number, see *IBM External Cable Reference* manual, SY33-2075.

3161 Console 3727 Console Key Conversion

| 3161 | 3727 |
|-------|-----------|
| BREAK | ATTN |
| PF1 | SELN AREA |
| PF2 | CCU FNCTN |
| PF3 | MSG |
| PF4 | PF1 |
| PF5 | PF2 |
| PF6 | PF3 |
| PF7 | PF4 |
| PF8 | PF5 |

Adhesive keytop labels part number = 03F7773

Console Setup and Maintenance

See appropriate console documentation.

Disk/Diskette Drive

Hard Disk Drive (HDD)

Description

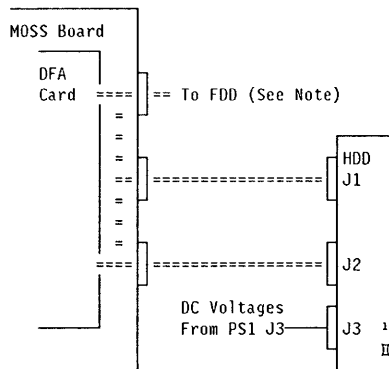
The 3745 hard disk drive has the following characteristics:

- 5.25 in.
- 4 disks
- 7 heads
- 733 cylinders
- 733 tracks
- 17 sectors per track
- 512 bytes per sectors
- The maximum readiness time after power ON is about 25 s
- The average access (seek) time is about 75 ms.

If the disk drive has not been used within 15 minutes, it is powered OFF by the MOSS.

The heads are automatically parked in the landing zone when the power is OFF.

The hard disk drive is an FRU.



¹ = Jumper for drive select, set on position 1.

Note: Three Dot ORed lines (INDEX, READY, and TRACK 0) are common to the HDD and the FDD.

Figure 9-4. HDD Connection

For component locations, see YZ pages.

For connector pin assignment, see page YZ543.

Removal and Replacement Procedures

See *MIP*, Chapter 4 and *Service Functions*, Chapter 11 for HDD initialization.

Part Number

See *3745 Parts Catalog*, S135-2012.

Flexible Disk Drive (FDD)

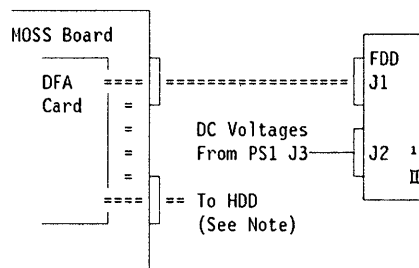
Description

The 3745 diskette drive has the following characteristics:

- 5.25 in.
- 2 heads
- 154 tracks
- 15 sectors per track
- 512 bytes per sector
- The average readiness time after power ON is about 1 s
- The average access (seek) time is about 92 ms.

If the diskette drive has not been used within 15 minutes, it is powered OFF by the MOSS.

The diskette drive is an FRU with its own power supply.



¹ = Jumper for drive select, set on position 0.

Note: Three Dot ORed lines (INDEX, READY, and TRACK 0) are common to the HDD and the FDD.

Figure 9-5. FDD Connection

For component locations, see YZ pages.

For connector pin assignment, see page YZ542.

Removal and Replacement Procedure

See *MIP* Chapter 4.

Part Number

See *Parts Catalog*.

Chapter 10. Power System

| | |
|--|-------|
| The Power System in 3745 Data Flow | 10-2 |
| Introduction | 10-3 |
| AC Voltages Input | 10-4 |
| AC Voltages Limits | 10-4 |
| Frequency | 10-4 |
| Primary Power Box | 10-5 |
| Power Supply 1 (PS1) | 10-7 |
| Power Supply 2 (PS2) | 10-12 |
| Disk and Diskette Drive ON/OFF Control | 10-13 |
| Power Control Subsystem | 10-14 |
| Power Control Data Flow | 10-15 |
| Power Control | 10-16 |
| Power Mode of Operation | 10-19 |
| Local Mode | 10-19 |
| Host Mode | 10-19 |
| Network Mode | 10-19 |
| Switching From One Mode to Another. | 10-20 |
| Power ON/OFF Sequence | 10-21 |
| Power ON Sequence | 10-21 |
| Power OFF Sequence. | 10-22 |
| Scheduled Power ON Function | 10-22 |
| AC Detection and AC Monitoring | 10-25 |
| Air Flow Detector | 10-26 |
| Power ON Reset (POR) | 10-28 |
| POR Principle | 10-28 |
| Power ON Reset Paths | 10-29 |

The Power System in 3745 Data Flow

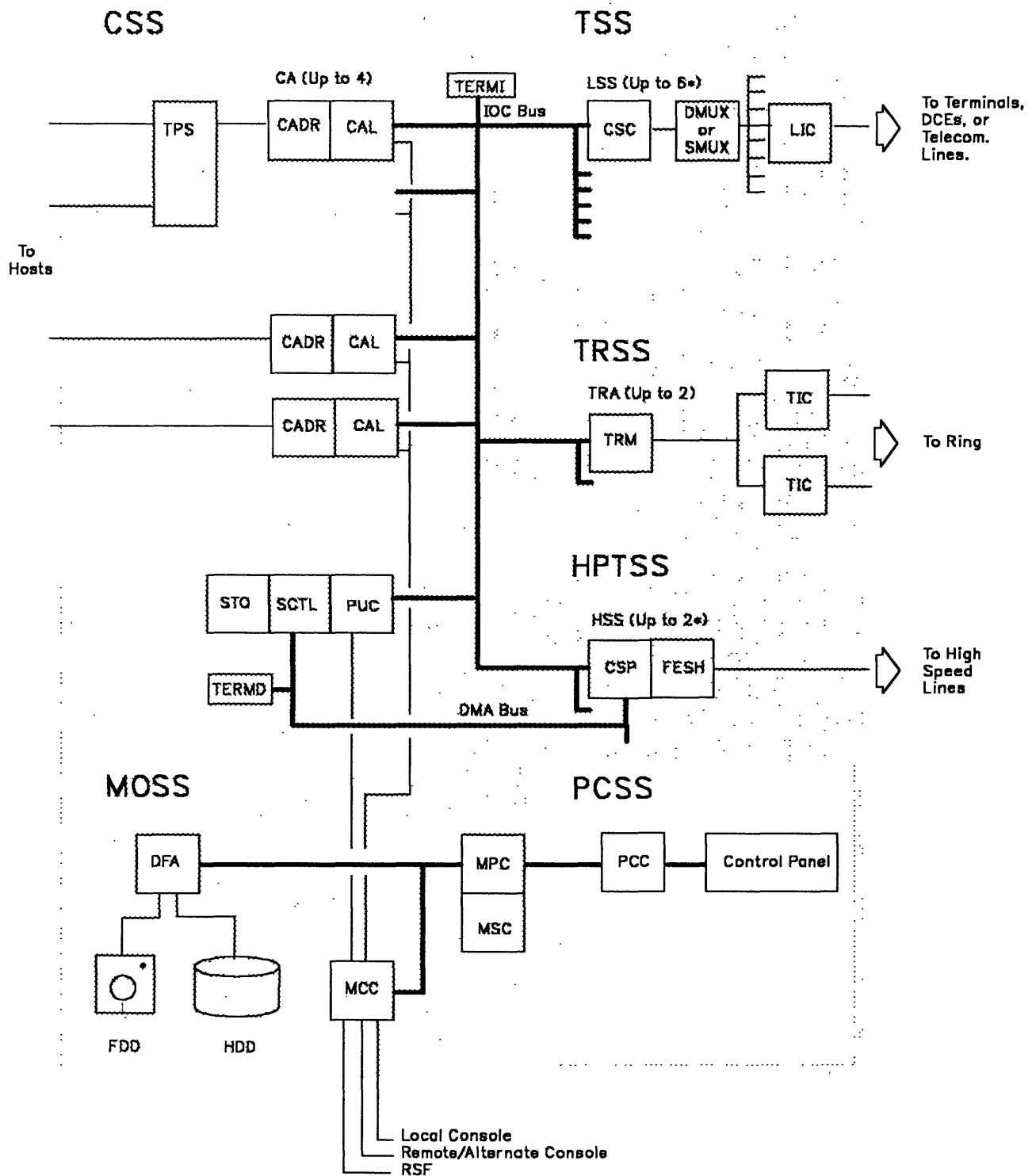
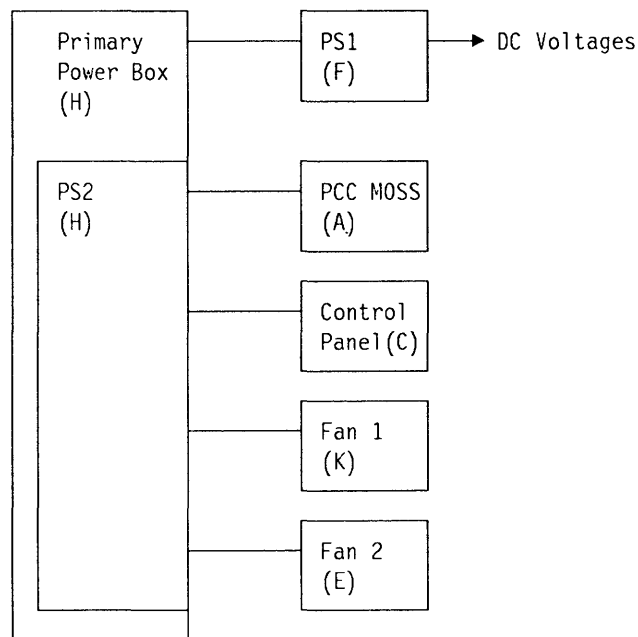


Figure 10-1. The Power System in 3745 Data Flow

Introduction

The power system consists of:

- One primary power box for AC distribution.
- One power control card (PCC) for power control subsystem function.
- One power supply 1 (PS1) for DC voltages.
- One power supply 2 (PS2) for DC voltages to fans, control panel, and PCC card (PS2 is located inside the primary power box).



(x) = Component location on pages YZ010 and YZ011.

AC Voltages Input

The power subsystem operates with a single phase distribution.

AC Voltages Limits

| Voltages | | | |
|----------|---------|-----|-----|
| Nominal | 200/208 | 220 | 240 |
| Minimum | 180 | 193 | 210 |
| Maximum | 220 | 240 | 260 |

AC Voltage Input Adjustment

AC voltage input adjustment must be done on the primary power box using the SW1 switch. Three positions are possible: 200, 220, and 240 volts. See Figure 10-2 on page 10-5 for SW1 switch location.

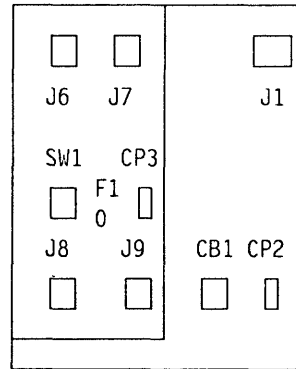
Frequency

The 3745 can operate at one of the following frequencies:

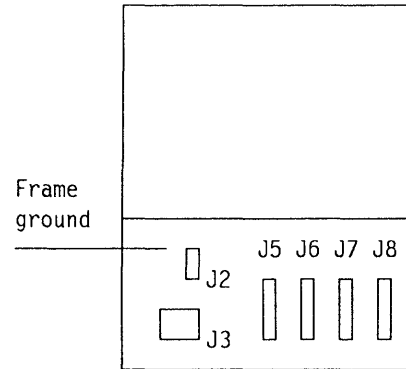
- 50 Hz \pm 1 Hz
- 60 Hz \pm 1 Hz

Primary Power Box

Primary Power Box Component Location



Front View



Rear View

CB1 = Main CB
CP2 = AC for PS2
CP3 = DC for fans
F1 = 28-volt fuse for
control panel and PCC card
J1 = AC to PS1
J6 = DC to fan 2
J7 = DC to fan 1
J8 = To UEPO switch
J9 = PS control to MOSS
SW1 = Voltage adjustment switch
(200, 220, or 240 volts)

J2 = Customer plug (see following details)
J3 = AC input
J5-J8 = EPO plugs

Figure 10-2. Primary Power Box Component Location

Customer Plug

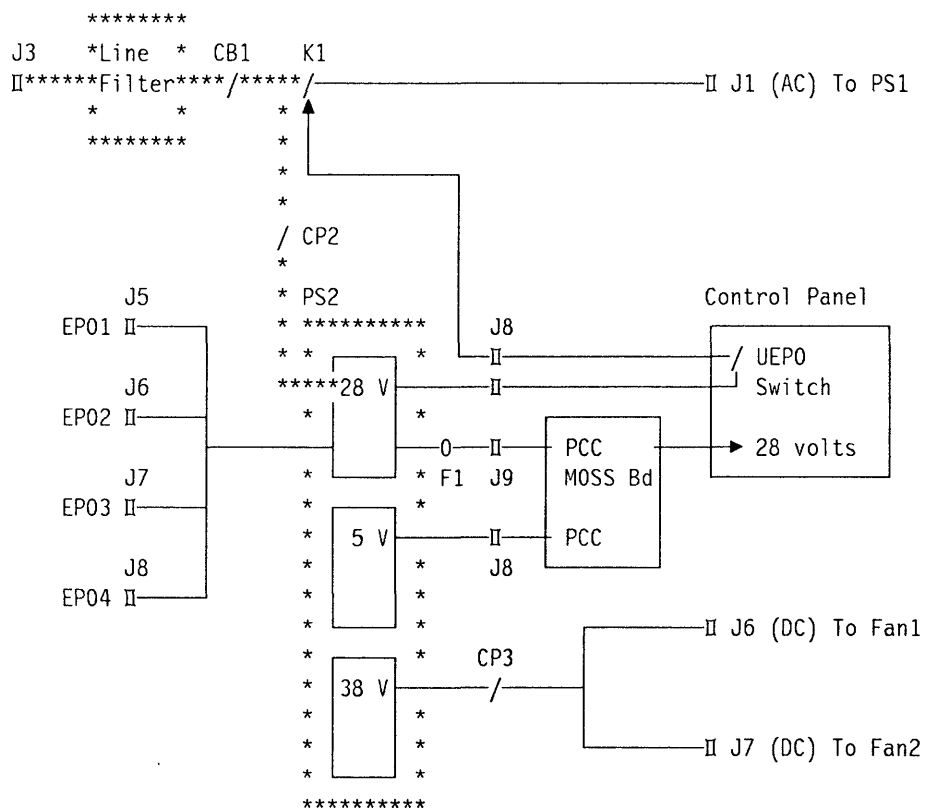
The J2 connector is for the customer and provides a normal-open contact when the power is OFF, and reverse its state when the power is ON.

Electrical Characteristic:

30 volts AC or 42.4 volts peak or DC, at 20 to 500 mA.

For details, see page YZ561.

Primary Power Box Distribution



*** = Lines show hazardous areas where hazardous AC voltages are still present when power is switched OFF at the control panel.

See YZ pages for details.

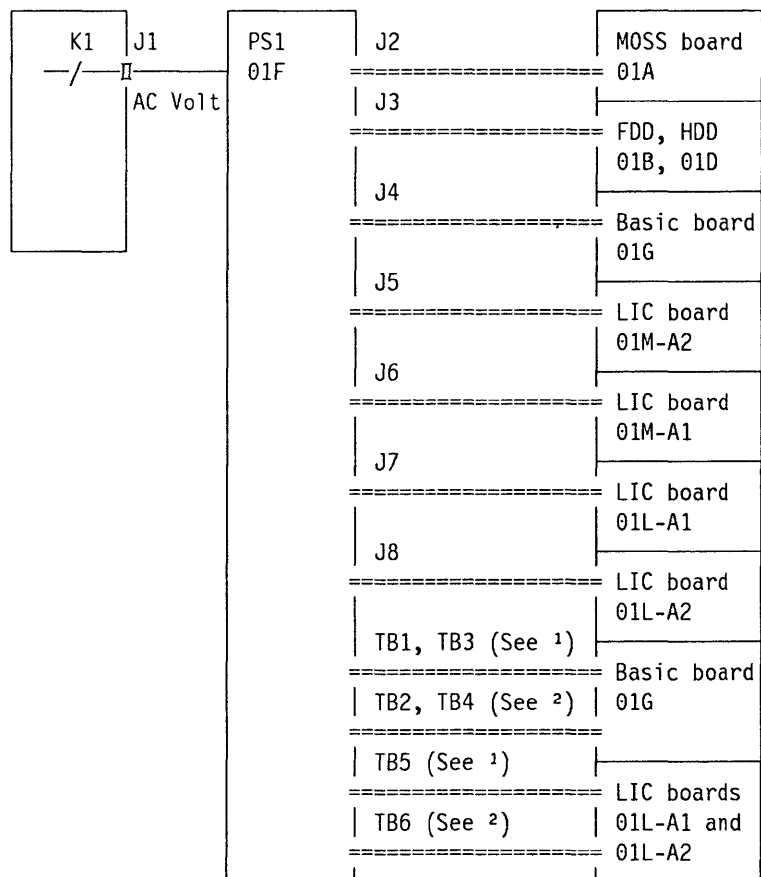
Power Supply 1 (PS1)

IMPORTANT

Power supply PS1 is a sealed unit. It cannot be opened for maintenance.

PS1 Connection Layout

Primary
Power Box
(01H)

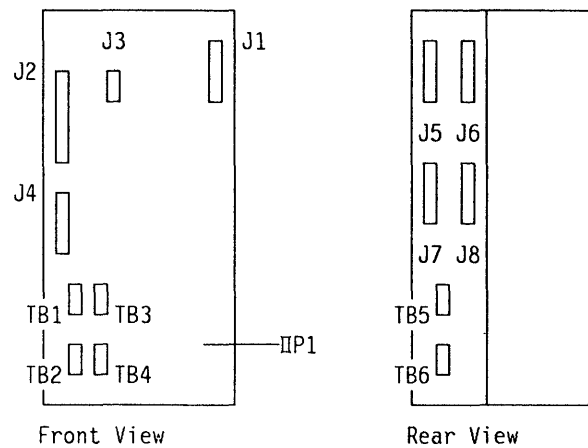


¹ = + 5 volts level 6

² = + 5 volts return level 6

See YZ pages for details.

PS1 Component Locations



Connectors J2 to J8 and TBs, see YZ pages for details.
Test connector J1, see "PS1 DC Voltage Test Points." for pin assignment.

PS1 DC Voltage Test Points.

| | | |
|----|---|--------------------------|
| J1 | o | 1 = + 12.0 volts level 1 |
| | o | 2 = + 12.0 volts level 2 |
| | o | 3 = + 8.5 volts level 3 |
| | o | 4 = + 5.6 volts level 4 |
| | o | 5 = + 5.0 volts level 5 |
| | o | 6 = + 5.0 volts level 6 |
| | o | 7 = + 5.0 volts level 7 |
| | o | 8 = - 5.0 volts level 8 |
| | o | 9 = - 8.5 volts level 9 |
| | o | 10 = PS fault test |
| | o | 11 = OC fault test |
| | o | 12 = DC common |

PS1 DC Voltages and Tolerances

Test points on the power supply are for DC voltage Vmin or Vmax measurement only.

| Table 10-1. PS1 Voltages and Tolerances | | | | |
|---|-------|---------|---------|----------------------------|
| VDC | Level | Vmin | Vmax | J1 Test Point ¹ |
| + 12.00 | 1 | + 11.00 | + 13.00 | 1 |
| + 12.00 | 2 | + 11.60 | + 12.60 | 2 |
| + 8.50 | 3 | + 7.90 | + 9.35 | 3 |
| + 5.60 | 4 | + 5.43 | + 5.88 | 4 |
| + 5.00 | 5 | + 4.85 | + 5.25 | 5 |
| + 5.00 | 6 | + 4.85 | + 5.25 | 6 |
| + 5.00 | 7 | + 4.85 | + 5.25 | 7 |
| - 5.00 | 8 | - 4.80 | - 5.50 | 8 |
| - 8.50 | 9 | - 7.90 | - 9.35 | 9 |

¹ = These values are referenced to test point 12.

Voltage Test Points and Tolerances on Board

For + 12 volts levels 1 and 2, and + 5 volts level 7, see "Disk Voltages and Tolerances (From PS1)" on page 10-13.

Recommendation: Ripple evaluation is a delicate measurement and should be performed only under the supervision of Product Engineering. A differential probe attached to a 10 MHz bandwidth scope shall be used. Using a scope with a larger bandwidth may give larger ripple values.

MOSS Board DC Voltages and Tolerances

| Table 10-2. MOSS Board Voltages and Tolerances | | | | |
|--|-------|--------|--------|----------|
| VDC | Level | Vmin | Vmax | Ripple |
| + 8.50 | 3 | + 7.65 | + 9.35 | 0.15 p-p |
| + 5.00 | 5 | + 4.75 | + 5.25 | 0.10 p-p |
| - 5.00 | 8 | - 4.70 | - 5.50 | 0.10 p-p |
| - 8.50 | 9 | - 7.65 | - 9.35 | 0.15 p-p |

For test point pin locations, see page YZ331 or YZ031 for ripple measurement.

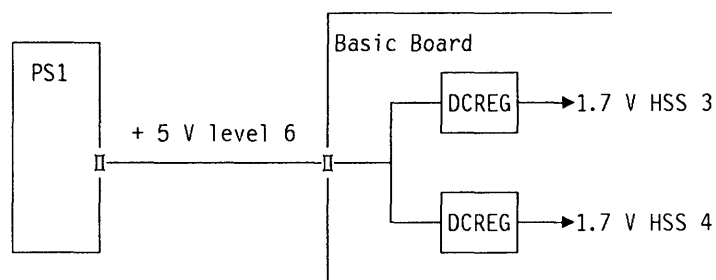
Basic Board DC Voltages and Tolerances

| Table 10-3. Basic Board Voltages and Tolerances | | | | |
|---|-------|--------|--------|----------|
| VDC | Level | Vmin | Vmax | Ripple |
| + 8.50 | 3 | + 7.65 | + 9.35 | 0 15 p-p |
| + 5.60 | 4 | + 5.43 | + 5.88 | 0 10 p-p |
| + 5.00 | 6 | + 4.75 | + 5.25 | 0.10 p-p |
| - 5.00 | 8 | - 4.70 | - 5.50 | 0 10 p-p |
| - 8.50 | 9 | - 7.65 | - 9.35 | 0.15 p-p |
| + 1.70 ¹ | - | + 1.70 | + 1.79 | 0 10 p-p |

For test point pin locations, see page YZ331.

¹ This voltage is for HSS line adapters. It is generated by two DC regulator cards (DCREG) located on the basic board:

- DCREG located in 01G-A1 ZG supplies HSS line adapter number 3.
- DCREG located in 01G-A1 ZE supplies HSS line adapter number 4.



For DCREG card location see page YZ033.

CSP and FESH Voltages and Tolerances

| VDC | Vmin | Vmax |
|--------|--------|--------|
| + 8.50 | + 7.60 | + 9.35 |
| + 5.00 | + 4.75 | + 5.25 |
| + 1.70 | + 1.60 | + 1.79 |
| - 5.00 | - 4.50 | - 5.50 |
| - 8.50 | - 7.60 | - 9.35 |

For test point pin locations, see page YZ732.

LIC Boards 01M-A1 and 01M-A2 DC Voltages and Tolerances

Table 10-4. LIC Boards 01M-A1 and 01M-A2 DC Voltages and Tolerances

| VDC | Level | Vmin | Vmax | Ripple |
|--------|-------|--------|--------|----------|
| + 8.50 | 3 | + 7.65 | + 9.35 | 0.15 p-p |
| + 5.00 | 5 | + 4.75 | + 5.25 | 0.10 p-p |
| - 5.00 | 8 | - 4.70 | - 5.50 | 0.10 p-p |
| - 8.50 | 9 | - 7.65 | - 9.35 | 0.15 p-p |

For test point pin locations, see page YZ738 for LIB1/3 boards (LICs 1-4), and page YZ739 for LIB2 board (LICs 5-6).

LIC Boards 01L-A1 and 01L-A2 DC Voltages and Tolerances

Table 10-5. LIC Boards 01L-A1 and 01L-A2 DC Voltages and Tolerance

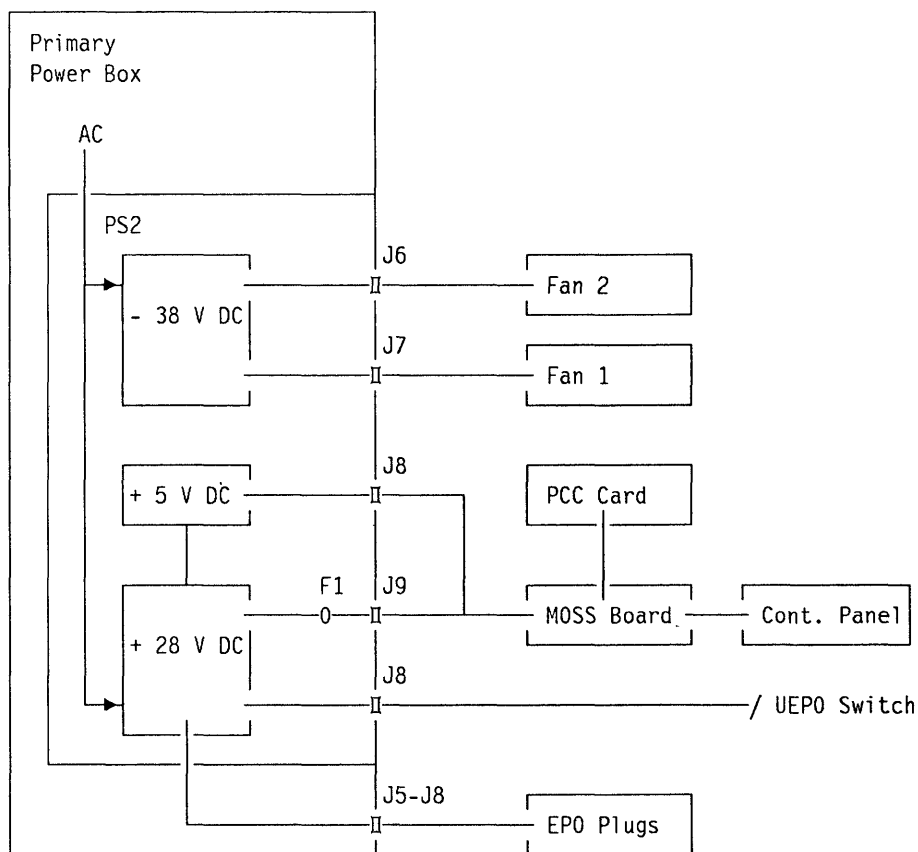
| VDC | Level | Vmin | Vmax | Ripple |
|--------|-------|--------|--------|----------|
| + 8.50 | 3 | + 7.65 | + 9.35 | 0.15 p-p |
| + 5.00 | 6 | + 4.75 | + 5.25 | 0.10 p-p |
| - 5.00 | 8 | - 4.70 | - 5.50 | 0.10 p-p |
| - 8.50 | 9 | - 7.65 | - 9.35 | 0.15 p-p |

For test point pin locations, see page YZ738 for LIB1/3 boards (LICs 1-4), and page YZ739 for LIB2 board (LICs 5-6).

Power Supply 2 (PS2)

PS2 is a FRU and is located inside the primary power box
For component location see YZ pages.

PS2 Connection Layout



F1 = Fuse
For details, see YZ pages.

PS2 DC Voltages and Tolerances

| Table 10-6. PS2 Voltages and Tolerances | | | |
|---|---------|---------|---------------------------------|
| VDC | Vmin | Vmax | Test Point |
| + 5.00 | + 4.75 | + 5.25 | 01A-A1 J3 pin 22 ¹ |
| + 28.00 | + 24.90 | + 29.50 | 01A-A1 J3 pin 21 ¹ |
| - 38.00 | - 34.20 | - 41.80 | 01H-B1 J6/J7 pin 2 ² |

¹ = These values are referenced to test point 01A-A1 J3 pin 8.
See page YZ331 for pin location.

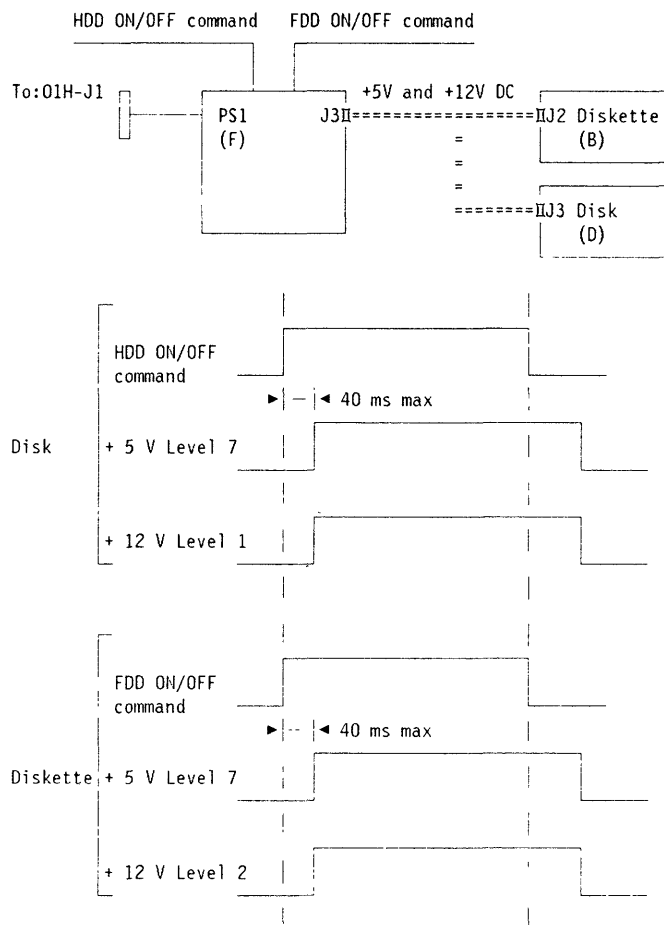
² = This value is referenced to 01H-B1 J6/J7 pin 1.
See page YZ060 for connector location.

Disk and Diskette Drive ON/OFF Control

DC voltages +5V and +12V are supplied by the PS1 to the disk (HDD) and diskette (FDD) drives, when the PS1 receives a 'HDD ON' or 'FDD ON' command from the MOSS through the PCC card.

If the disk and diskette drives have not been used within 15 minutes, the PS1 receives from the MOSS the 'HDD OFF' and 'FDD OFF' commands, and DC voltages are no longer applied to the drives.

Disk and diskette can be also controlled manually (DIF function 7).



Disk Voltages and Tolerances (From PS1)

Table 10-7 Disk Voltages and Tolerances (From PS1)

| VDC | Level | Vmin | Vmax | Ripple |
|---------|-------|---------|---------|----------|
| + 12.00 | 1 | + 10.80 | + 13.00 | 0.10 p-p |
| + 12.00 | 2 | + 11.40 | + 12.60 | 0.10 p-p |
| + 5.00 | 7 | + 4.75 | + 5.25 | 0.10 p-p |

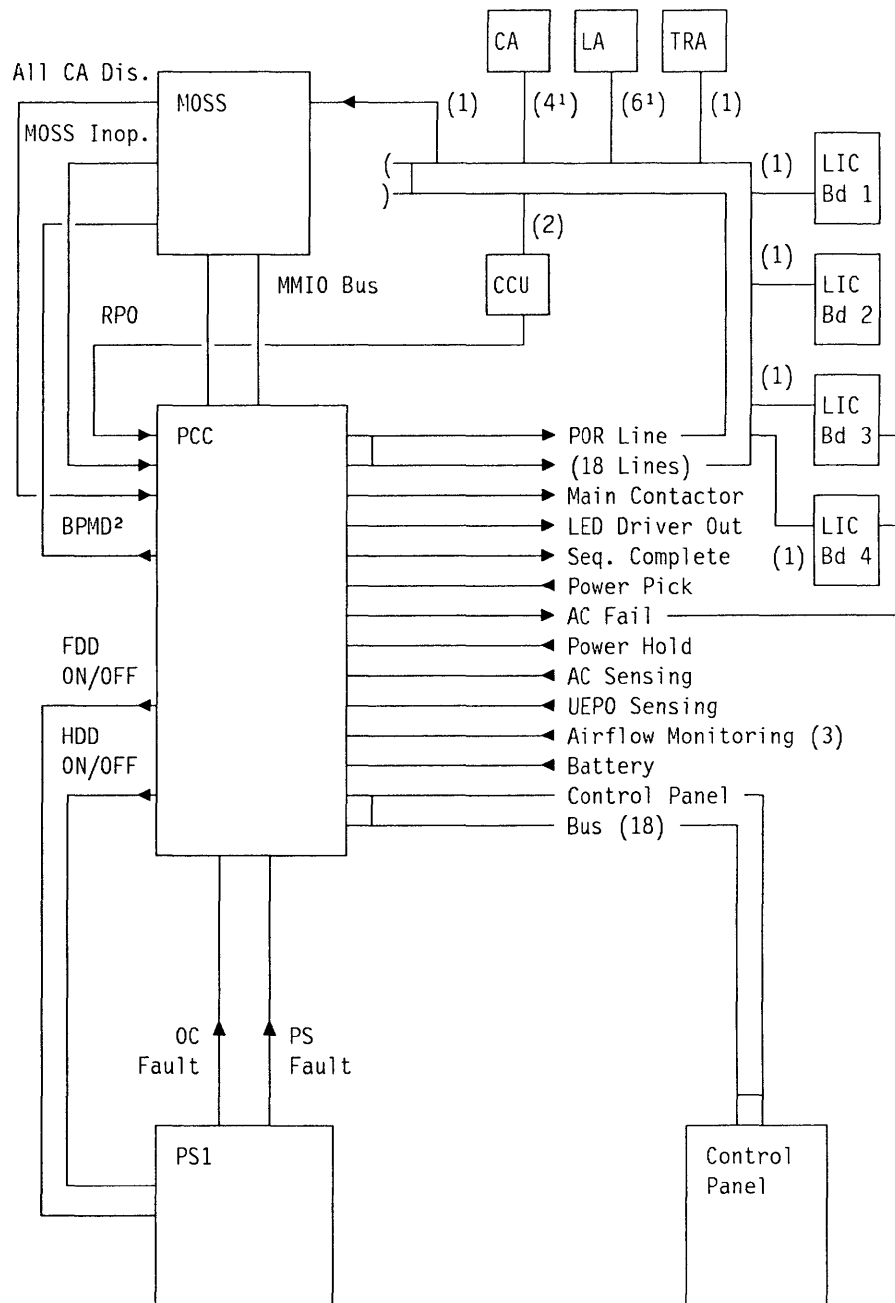
For DC test points, see pages YZ.

Power Control Subsystem

The power control subsystem has in charge the following functions:

- Powering the machine ON/OFF either in local, host or network mode.
- Monitoring the power supply state.
- Monitoring the airflow.
- Individual reset function for any dedicated subsystems or adapter.
- The time function in order to give to the MOSS the local time and to allow the scheduled power ON function.
- The Scheduled Power ON of the whole machine (only in network mode).
- The communication between the control panel and the MOSS.
- The display on the control panel of the stacked power or fan faults.
- The main line survey in order to detect AC main utility failures.
- The automatic restart function on an AC main utility failure.
- The diagnostic tests of the power control subsystem and the control panel.
- The monitoring of the remote power OFF signal coming from the CCU
- The logging of all faults to report them to the MOSS
- Power ON retry after a power OFF due to a fan or power supply fault.
- PCC dump process.

Power Control Data Flow



- () = Number of lines
¹ = One POR line per adapter
² = Bypass MOSS diagnostic

Figure 10-3. Power Control Data Flow

Power Control

The power control subsystem is made of two parts:

1. The power control card (PCC)
2. The control panel.

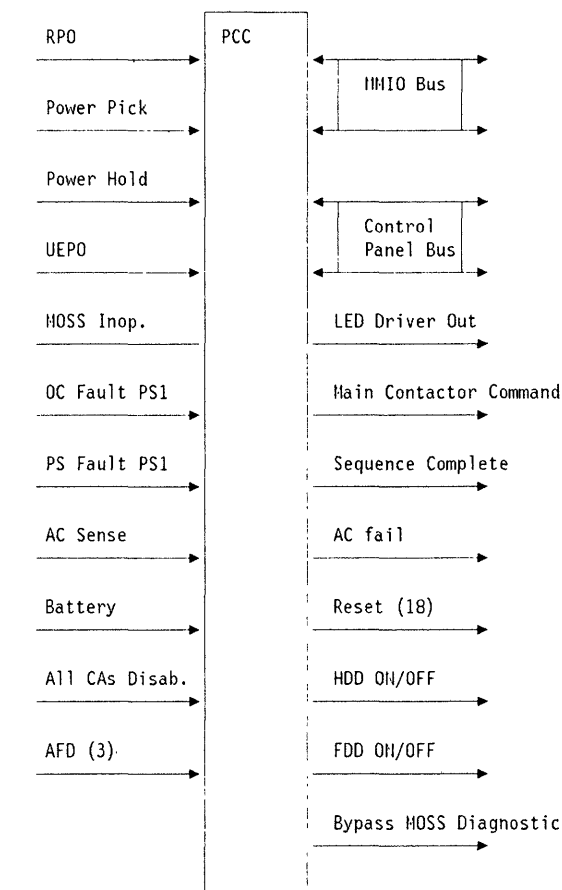
When AC is ON and the machine is switched OFF from the control panel, the power control subsystem is the only part of the machine powered ON.

The PCC card is located in the MOSS board .

The PCC is dedicated to the interconnection with the MOSS, the control panel, the power supplies PS1, and to the following signals:

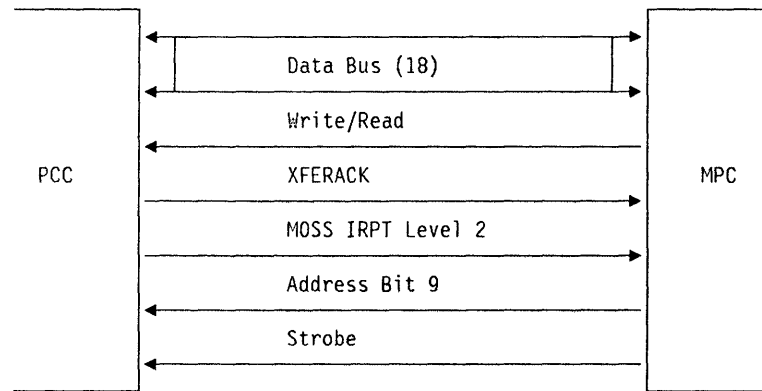
- Power pick and hold signals
- Sequence complete signal
- AC fault signal
- Air flow detectors outputs
- Remote power OFF signal
- Main contactor command
- UEPO sense
- Battery monitoring
- AC fail.

PCC Interconnection

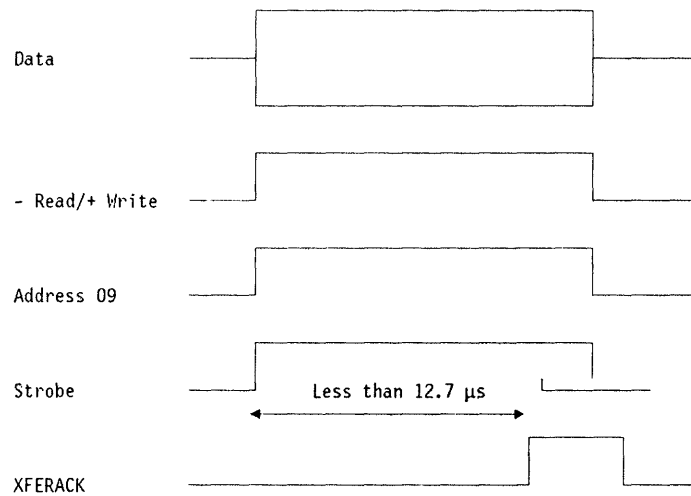


() = Number of lines

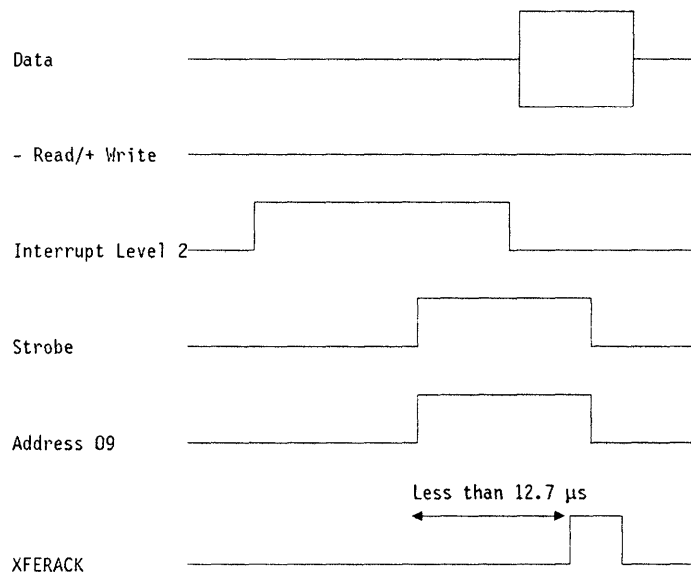
PCC Card MOSS Interconnection



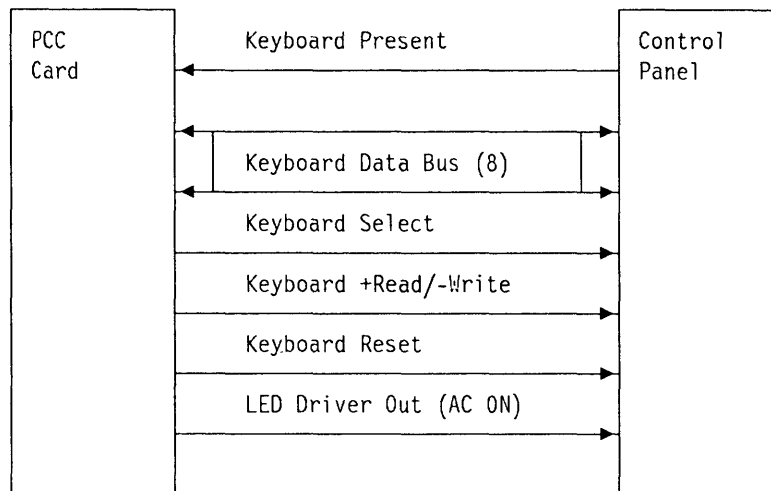
Data from MOSS to PCC Card



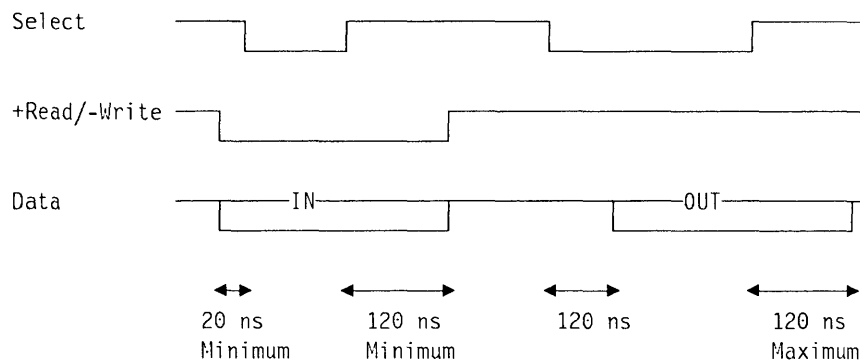
Data from PCC Card to MOSS



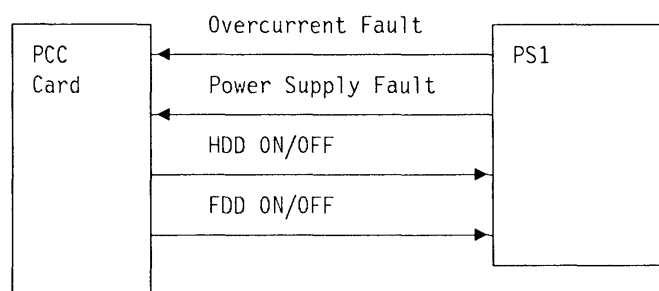
PCC Card Control Panel Interconnection



PCC Card Control Panel Data Timing



PCC Card Power Supply Signal Interconnection



Power Mode of Operation

Local Mode

In local mode (3 at the power control window) the only way to power ON/OFF the 3745 is to do it manually from the control panel.

In this mode, for safety reasons, the Automatic Restart and the scheduled power ON functions are not available. In this mode the Power ON Reset of the machine is available from the control panel.

Host Mode

In host mode (1 at the power control window) the only way to power ON/OFF the 3745 is to do it from the locally-attached hosts, via external control cables. When any of these hosts goes ON, the 3745 powers ON with a power pick command.

When all attached hosts have turned OFF (all power hold dropped) the 3745 turns OFF.

An EPO plug Part 8482303 must be installed in position J5 if no host EPO cables are installed. This plug prevents powering OFF the 3745 if the power control is set to position 1 (host mode), when no EPO cables are installed.

In this mode, the automatic restart and power ON retry functions are available.

Network Mode

In network mode (2 at the power control window) and only in this mode, the scheduled power ON function is available. As for all the other communication controllers, in this mode you can power ON the 3745 manually from the control panel, and you can power OFF the 3745 through the NCP (RPO function). The scheduled power ON function does not disable the manual power ON or RPO functions. This means that you always have the ability to power ON the 3745 manually before the scheduled power ON time.

In this mode, the automatic restart and power ON retry functions are available.

In this mode the Power ON Reset of the machine is available from the control panel.

Switching From One Mode to Another.

- Switching from host or network to local does not impact the machine's Power ON/OFF status.
- Switching from local to host:

If OFF in local, the machine will be maintained OFF in host. It will be turned ON later by a power pick pulse from one attached host (if an AC main utility fault occurs, the Automatic Restart function will not apply even if one attached host is ON).

If ON in local, the machine will remain ON if at least one attached host is ON. Otherwise, the machine will go OFF.

- Switching from local to network:

If OFF in local, the machine will be maintained OFF in network, waiting for a manual power ON at the control panel or for a scheduled power ON action. If an AC main utility fault occurs after switching from local to network, the machine being OFF, the automatic restart function will not apply.

If ON in local, the machine will be maintained ON in network.

- Switching from host to network:

The machine power ON/OFF status is not impacted.

- Switching from network to host:

If OFF in network, the machine will be maintained OFF in host. It will be turned ON later by a power pick pulse from one attached host (if an AC main utility fault occurs, the automatic restart function will not be applied even if one attached host is ON).

If ON in network, the machine will remain ON if at least one attached host is ON. Otherwise, the machine will go OFF.

Power ON/OFF Sequence

Power ON Sequence

The normal power ON sequence is initiated by:

- Manual power ON at the control panel if the machine is in local or network mode.
- Power pick command (from one attached host) if the machine is in host mode.
- Automatic restart function on an AC main utility failure if the machine was powered ON in host or network mode when the failure occurred.
- Scheduled power ON function if the machine is in network mode.

The PCC card first activates the reset lines of all the adapters

Then the main contactor command signal will turn ON the power supplies.

Then the LED driver out signal is activated.

After a 1 second wait the PCC checks the fault signals (overcurrent (OC) and power supply (PS) faults) of both power supplies. If no fault, the reset lines are deactivated 100 ms later.

Then the disk (HDD) and the diskette (FDD) are powered ON.

MOSS IML will start, and at the end of IML the MOSS will ask the PCC card which type of power ON was done (local, host, network, scheduled, automatic restart), the power ON time and the last power OFF time.

At the end of the power ON sequence, and if the machine is in host mode, the sequence complete signal is sent to the host.

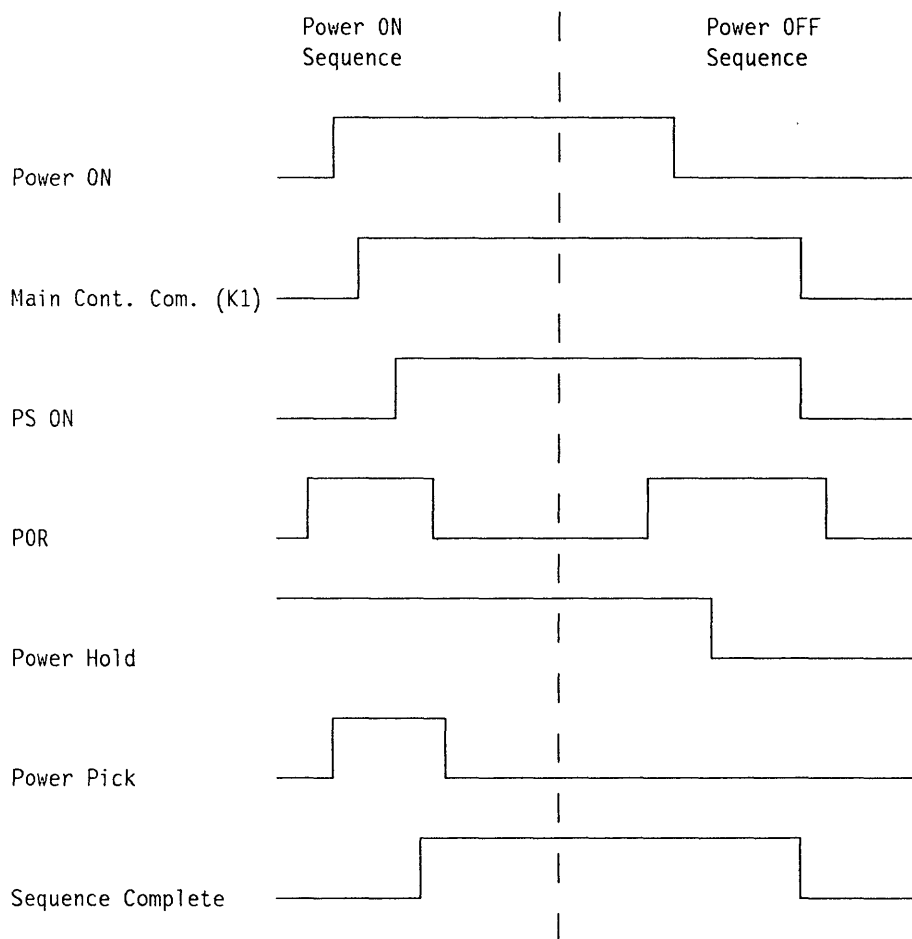
Note: When the machine is in local or network mode, this signal is forced permanently, whether the machine is power ON or OFF.

In host or network mode, if there is a fault on a power supply, the power ON sequence is stopped, the PCC deactivates the AC via the main contactor command signal, waits ten seconds and then re-issues another power ON sequence. This is done two more times before the final power OFF.

Power OFF Sequence.

The normal power OFF sequence is initiated by :

- Manual power OFF at the control panel if the machine is in local mode.
- The remote power OFF (RPO) signal, if the machine is in network mode.
- The drop of the last host power hold signal if the machine is in host mode.



Scheduled Power ON Function

The purpose of the clock used in the power control subsystem is to keep time and calendar date through extended power OFF periods. This will allow scheduled power ON actions to be taken at a predetermined time and day of the week, independently of any intervening AC main power failures. Each day of the week may be associated with a different power ON time.

The logic for the scheduled power ON function is in the PCC card and is powered by a battery during AC main failures.

This function is available in network mode (2 at power control window) only, and is allowed or inhibited by the customer through the MOSS.

Manual Versus Scheduled Power ON

Manual power ON or power OFF through the NCP has priority over scheduled power ON. If power OFF through the NCP completes prior to a scheduled power ON point, then the power control subsystem will turn power ON when the predetermined point is reached.

The scheduled power ON times of the current week will be considered valid for the following weeks if they are not changed.

Automatic Restart Function

For safety reasons, this function is not available in local mode. The automatic restart function intends to assure a re-power ON of the system when the AC main is restored. There is a 10-second wait between the AC is restored and the auto restart takes place.

If one AC main fault is detected, a fault event is sent to the MOSS (if the power supply of the MOSS is still operative):

The information will be stacked in the PCC card if the MOSS is inoperative.

When the AC main is restored, a machine auto-restart will take place if the AC main fault has resulted in a machine power OFF.

This is done after a 10-second wait. The machine automatically starts with a general IPL (function 0, service 0).

Power ON Retry Function

This function allows an automatic repower of the machine after an automatic power OFF due to any power supply or fan fault. This function is only available in host and network modes. The machine starts automatically with a general IPL (function 0, service 0).

Retry Sequence

1. A fault is detected
2. The machine is powered OFF
3. The fault is displayed on the control panel
4. A 10-second wait is performed
5. The machine is powered ON (retry).

The above sequence is performed up to three times before a final power OFF. The retry counter is cleared if there is no fault after IML completed and when the fan speed establishment time (one minute) is reached.

After three retries the display of the last fault is replaced by a display ('010') indicating to use the 'display stacked errors' function.

Power Status Monitoring

The power status is scanned cyclically to determine an eventual fault. If a fault occurs during this scanning, the machine is powered OFF, this fault is displayed on the control panel and stacked in the PCC card. After a 10-second wait, the machine is powered ON again.

The same operation can be done three times. After three times the machine stays power OFF. See "Retry Sequence" on page 10-23.

Individual Reset Function

This function allows the MOSS, via the power control, to perform selective resets for diagnostic purposes, or a general reset at power ON. The PCC card has 18 reset lines to reset the different machine adapters. See Figure 10-3 on page 10-15 for details.

AC Detection and AC Monitoring

Main Line Survey

Major disturbances are defined as follows:

A 35 % or more dip in the minimum nominal voltage.

When this input is under the specified threshold during 40 ms, an AC failure is detected by the PCC card and the AC fail signal is generated. Two types of AC failure can be reported to the MOSS:

1. Valid AC failure:

a. Transient AC failure:

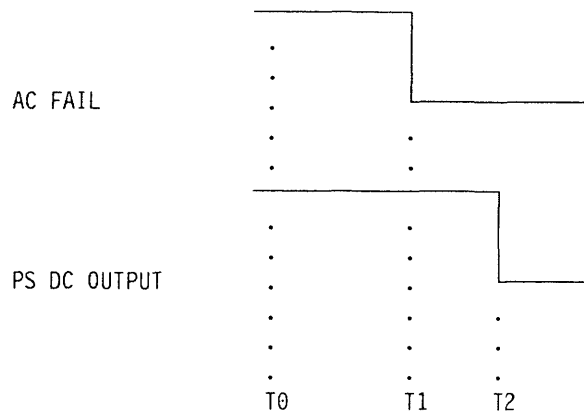
A failure defined as above (40 ms minimum) with a duration lower than T2 (45 ms).

b. AC failure:

An AC failure longer than T2 (45 ms). The whole machine is powered OFF.

2. Invalid AC failure:

The PCC card detects an AC failure, but the AC is still present after two seconds (false AC failure detection).



T0 : At this time the AC is going under the threshold

T1 : At this time the AC failure detection occurs

T2 : At this time the DC output is falling down

T0-T1 : AC failure detection time (40 ms minimum)

T0-T2 : PS hold up time (45 ms minimum)

Air Flow Detector

The fans have a speed detection (opto-coupler device) for the air flow detection.

The opto-coupler device sends a signal to the PCC card.

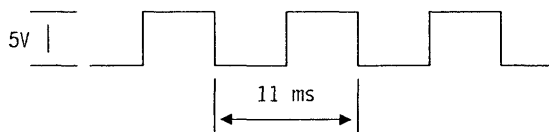
Air Flow Monitoring

The status of the fan is scanned cyclically to determine an eventual fault. If a fault occurs during this scanning the machine is powered OFF, this fault is displayed on the control panel and stacked in the PCC card. After a 10-seconds wait, the machine is powered ON again.

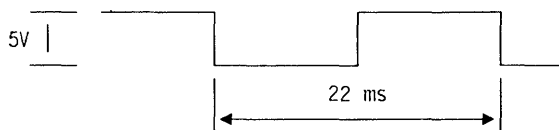
The same operation can be done three times. After three times the machine stays power OFF.

Opto-Coupler Device Output

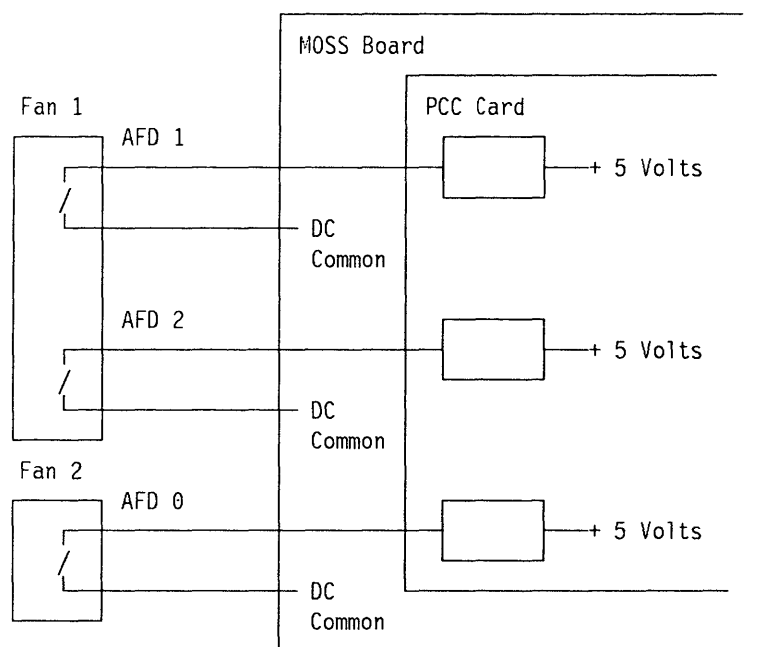
AFD 1 and AFD 2



AFD 0



Air Flow Detection Principle



Power and Fan Stacked Faults

After three unsuccessful machine power ON retries, the power control displays code '010' on the panel (machine OFF due to three unsuccessful power ON).

This function allows to display the last four stacked faults. This can be done only by entering service 1 prior entering the function B .

Faults Logging

After any fault the power control sends a fault event to the MOSS. If the MOSS is not operative, this fault is stored in the PCC card and restored to the MOSS when it becomes operative.

Power ON Reset (POR)

POR Principle

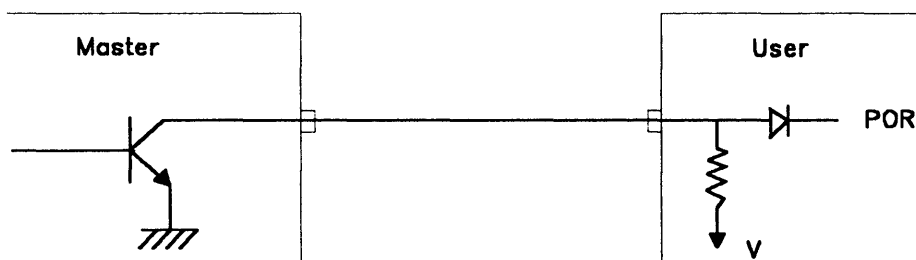


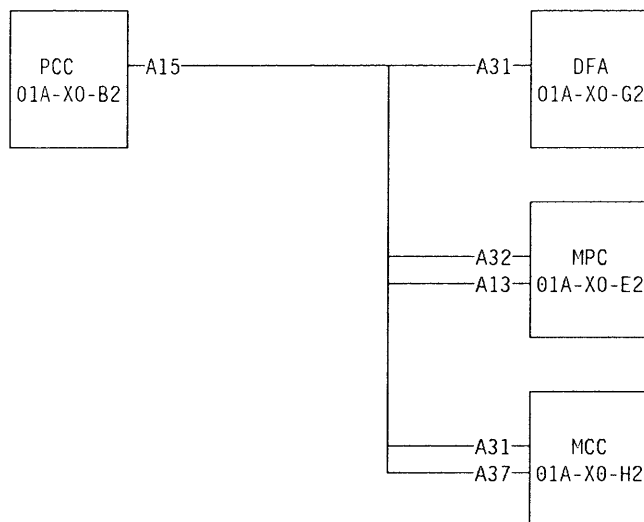
Figure 10-4. POR Principle

POR is always down level when active

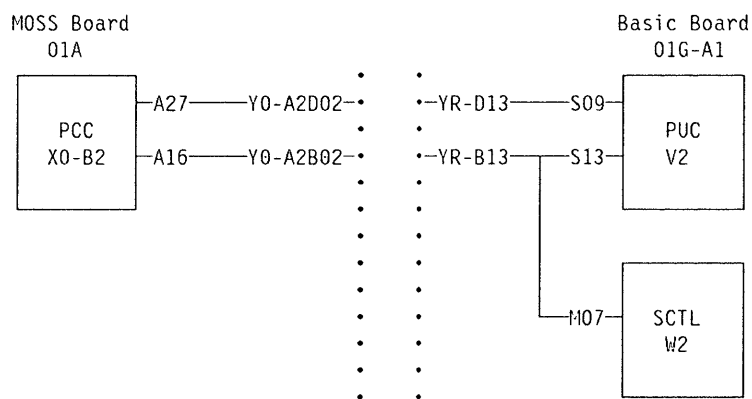
Voltage level is provided by the user.

Power ON Reset Paths

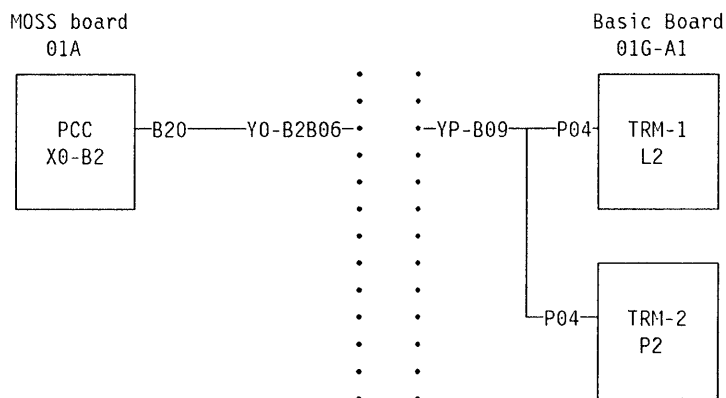
MOSS Board



Basic Board (CCU)



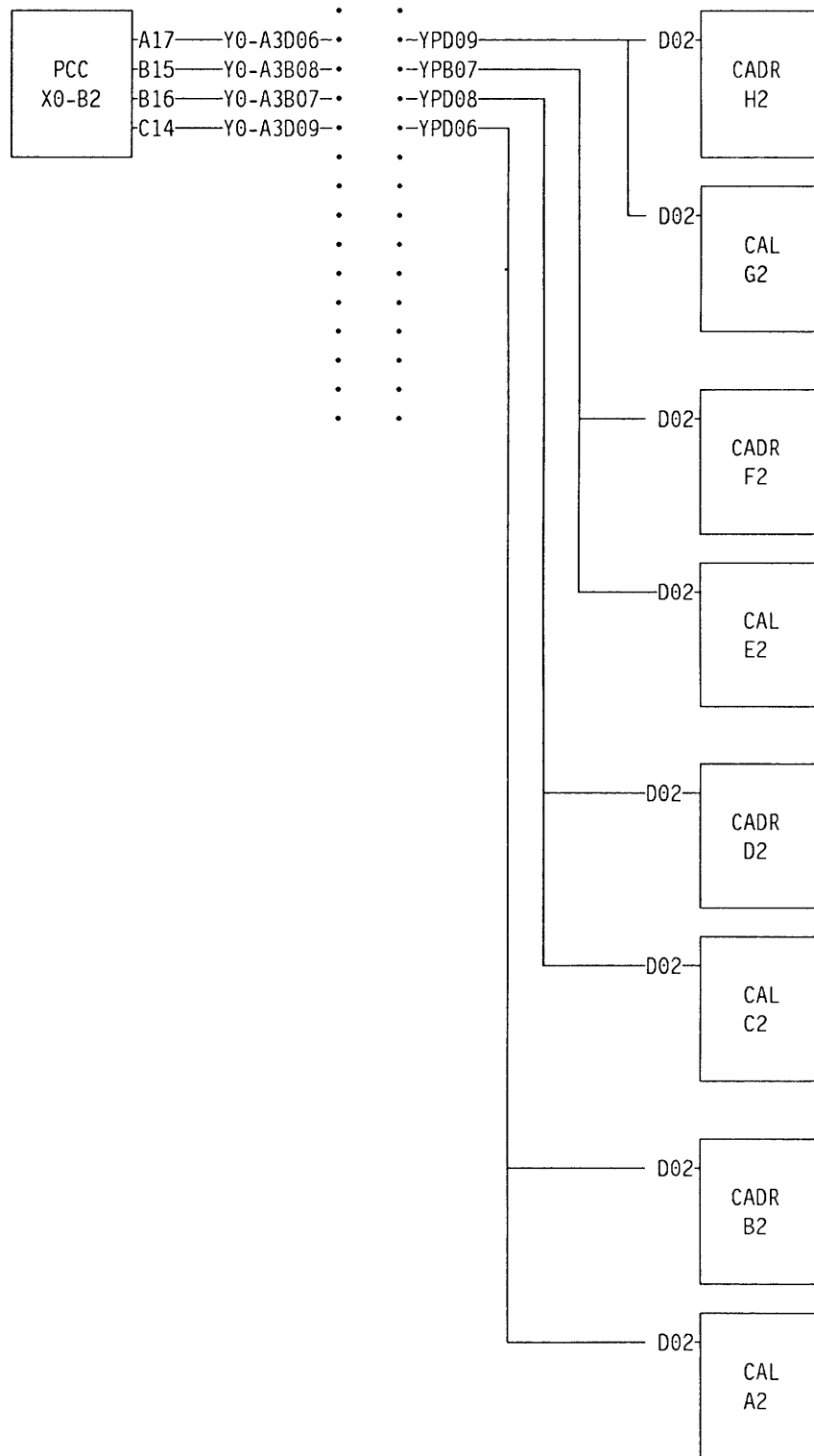
Basic Board (TRM)



Basic Board (CA)

MOSS Board
01A

Basic Board
01G-A1



Basic Board (CSC/CSP)

MOSS Board
01A

PCC
X0-B2

C15—Y0-A3B02—
C16—Y0-A3D02—
C17—Y0-A3B04—
C18—Y0-A3D03—
C19—Y0-A3B05—
C20—Y0-A3D05—

• —YPB13
• —YPD13
• —YPB11
• —YPD12
• —YPB10
• —YPD10
•
•
•
•
•
•
•
•

Basic Board
01G-A1

CSC/CSP
T2

FESH
U2

CSC/CSP
R2

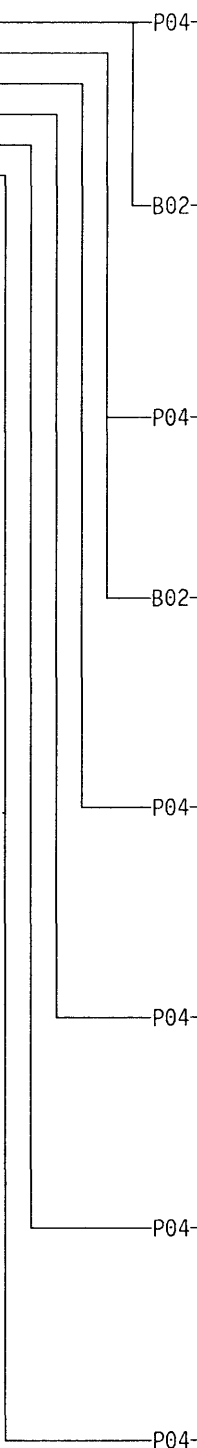
FESH
S2

CSC
Q2

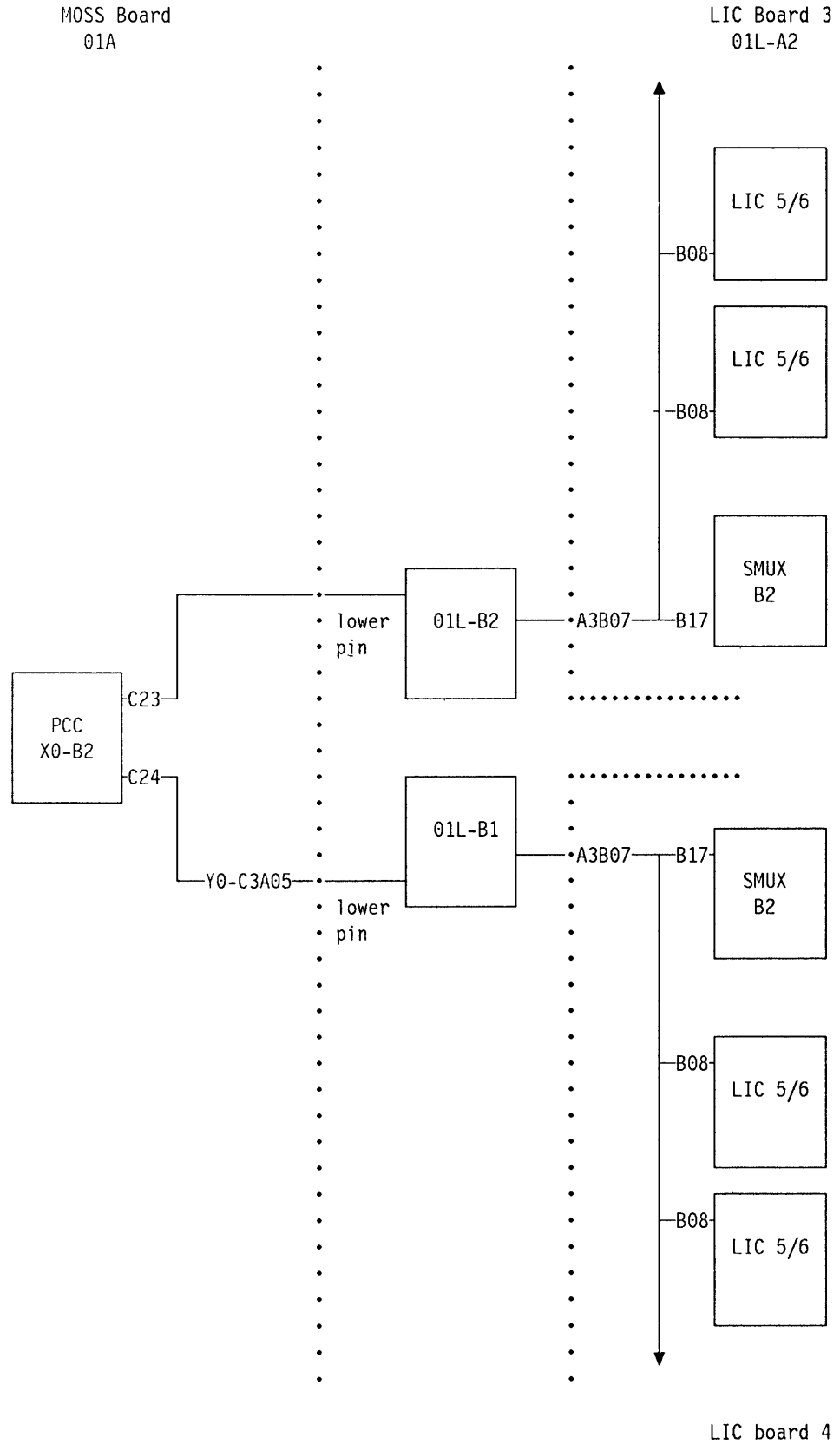
CSC
P2

CSC
N2

CSC
M2



LIC Board Type 2



Chapter 11. Error Logging

| | |
|---|-------|
| Introduction | 11-4 |
| Hexadecimal Codes | 11-4 |
| Box Event Records (BERs) | 11-4 |
| BER Generalities | 11-6 |
| BER Generation | 11-6 |
| BER Type and Identification | 11-9 |
| BER Structure | 11-9 |
| BER Handling Tools | 11-11 |
| BERs Which Are Not Machine Errors | 11-12 |
| Specific Mechanisms | 11-13 |
| BER/Alarm/Alert Mechanism on a 3745 Down | 11-13 |
| Analysis of a BER/Alarm/Alert Sequence | 11-14 |
| BER Display | 11-14 |
| AutoMaint | 11-17 |
| AutoMaint Strategy | 11-17 |
| Automatic BER Analysis | 11-19 |
| General Process Flow | 11-19 |
| CE Field Updating | 11-20 |
| BER Reference Code | 11-20 |
| Manual FRU Correlation | 11-21 |
| Automatic FRU Correlation | 11-21 |
| Reference Code Structure | 11-22 |
| BER Recovery Procedures | 11-25 |
| MOSS Handling of 3745 Down | 11-25 |
| IOC Bus and Adapters | 11-25 |
| Scanner Errors Without BERs | 11-25 |
| Unresolved Interrupts | 11-26 |
| MOSS Error Logging | 11-30 |
| Hexadecimal Codes | 11-30 |
| Hexadecimal Codes Versus MOSS BER ID 00 | 11-30 |
| MOSS BERs Used With the IPL Application | 11-34 |
| MOSS BER Type 01 - Summary | 11-35 |
| MOSS BER Type 01 ID 00 (Detailed BER Display) | 11-40 |
| MOSS BER Type 01 ID 00 - Field Description | 11-40 |
| BER TYPE 01 ID 00 Error Code Description | 11-41 |
| MOSS BER Type 01 ID 01 | 11-51 |
| MOSS BER Type 01 ID 01 - Field Description | 11-51 |
| MOSS BER Type 01 ID 02 | 11-53 |
| MOSS BER Type 01 ID 02 - Field Description | 11-53 |
| MOSS BER Type 01 ID 03 | 11-56 |
| MOSS BER Type 01 ID 03 - Field Description | 11-56 |
| MOSS BER Type 01 ID 04 | 11-60 |
| MOSS BER Type 01 ID 05 | 11-63 |
| MOSS BER Type 01 ID 05 - Field Description | 11-65 |
| MOSS BER Type 01 ID 06 (Error 01 or 02) | 11-66 |
| MOSS BER Type 01 ID 06 (Error 03 or 06) | 11-66 |
| MOSS BER Type 01 ID 06 (Error 04) | 11-67 |
| MOSS BER Type 01 ID 06 (Errors 05/08 Ext 05/07) | 11-72 |
| MOSS BER Type 01 ID 06 (Error 07) | 11-73 |
| MOSS BER Type 01 ID 06 (Error 08 Ext 07) | 11-73 |
| MOSS BER Type 01 ID 06 (Error 09) | 11-73 |

| | |
|--|--------|
| MOSS BER Type 01 ID 07 | 11-75 |
| MOSS BER Type 01 ID 08 | 11-78 |
| MOSS BER Type 01 IDs 10 and 11 | 11-79 |
| MOSS BER Type 01 IDs 12, 13, and 14 | 11-79 |
| MOSS BER Type 01 ID 15 | 11-80 |
| MOSS BER Type 01 IDs 16 and 1A to 1D | 11-80 |
| MOSS BER Type 01 ID 17 | 11-81 |
| MOSS BER Type 01 ID 19 | 11-82 |
| MOSS BER Type 01 ID 20 | 11-83 |
| MOSS BER Type 01 ID 21 | 11-88 |
| MOSS BER Type 01 IDs 24 to 29, and 37 | 11-89 |
| MOSS BER Type 01 ID 30 | 11-89 |
| MOSS BER Type 01 ID 32 | 11-89 |
| MOSS BER, Type 01 ID 36 | 11-91 |
| MOSS BER Type 01 ID 38 | 11-91 |
| MOSS BER Type 01 ID 39 | 11-91 |
| MOSS BER Type 01 ID 43 | 11-93 |
| MOSS BER Type 01 ID 44 | 11-97 |
| MOSS BER Type 01 ID 50 | 11-98 |
| MOSS BER Type 01 ID 80 | 11-98 |
| MOSS BER Type 01 IDs 91, B3, C1, C2 | 11-98 |
| BER Formats on Disk | 11-99 |
| MOSS BERs Type 01 Formats | 11-99 |
| Diagnostics BER Type 03 | 11-106 |
| Diagnostics BER Type 03 - Summary | 11-106 |
| Diagnostics BER Type 03 - Detailed BER Display | 11-106 |
| Diagnostic BERs Type 03 - Formats | 11-107 |
| Power BER Type 04 | 11-108 |
| Power Subsystem BER Type 04 - Summary | 11-108 |
| Power BER Type 04 (Detailed BER Display) | 11-108 |
| Power BER Type 04 - Field Description | 11-110 |
| Power BER Type 04 - Formats | 11-114 |
| NCP CA BER Type 10 | 11-115 |
| CA BER Type 10 - Summary | 11-115 |
| CA BER Type 10 (Detailed BER Display) | 11-120 |
| CA BER Type 10 - Field Description | 11-123 |
| CA BER Type 10 - Formats | 11-124 |
| NCP TSS/HPTSS BER Type 11 | 11-127 |
| TSS/HPTSS BER Type 11 - Summary | 11-127 |
| TSS/HPTSS BER Type 11 (Detailed BER Display) | 11-131 |
| TSS/HPTSS BER Type 11 - Field Description | 11-134 |
| TSS/HPTSS BER Type 11 - Formats | 11-136 |
| NCP/PEP BER, Type 12 | 11-138 |
| NCP/PEP BER Type 12 Summary | 11-138 |
| NCP/PEP BER Type 12 (Detailed BER Display) | 11-139 |
| NCP/PEP BER Type 12 - Field Description | 11-139 |
| NCP/PEP BER Type 12 - Formats | 11-140 |
| NCP CCU BER Type 13 | 11-141 |
| CCU BER Type 13 - Summary | 11-141 |
| CCU BER Type 13 (Detailed BER Display) | 11-142 |
| CCU BER Type 13 - Field Description | 11-143 |
| CCU BER Type 13 - Formats | 11-144 |
| NCP IOC BER Type 14 | 11-145 |
| IOC BER Type 14 - Summary | 11-145 |
| IOC BER Type 14 (Detailed BER Display) | 11-145 |

| | |
|---|--------|
| IOC BER Type 14 - Field Description | 11-146 |
| IOC BER Type 14 - Format | 11-146 |
| NCP TRSS BER Type 15 | 11-147 |
| TRSS BER Type 15 - Summary | 11-147 |
| TRSS BER Type 15 (Detailed BER Display) | 11-149 |
| TRSS BER Type 15 - Field Description | 11-152 |
| TRSS BER Type 15 - Formats | 11-153 |

Introduction

Hexadecimal Codes

During 3745 initialization, the hardware is checked before loading the NCP or PEP. While the different tests are running, they may encounter an error or an unusual event. The logging routines are in charge of indicating the anomaly, analyzing it and displaying a hexadecimal code on the operator's panel. The MIP gives an exhaustive list of all the errors and progression codes.

If a 3745 control panel error occurs, or if a MOSS IML threshold is reached, the control panel displays hexadecimal codes indicating the cause of the error. In parallel with the display of the hexadecimal code, a BER (box event record) may be built if the state of the machine's hardware permits it.

Thus very often there is a connection between a hexadecimal code and a BER. (See page 11-30).

Box Event Records (BERs)

The event logging procedure of the MOSS reports each error caused by either an intermittent failure or a 3745 down (controller re-IPL).

Any such event in a 3745 subsystem is reported first to the NCP/PEP, and then to the MOSS for logging. In this case, a BER is built in a place called check record pool (CRP), where MOSS has access to it. In some cases, a BER is built directly by the MOSS itself. In any case, the BER is stored in a buffer in the MOSS RAM. The BER built by the MOSS is called composite MOSS BER, and may contain several BERs (usually three). The MOSS also generates the power BERs and the diagnostic BERs. For the generation, the formatting, and the storage of the BERs, see page 11-6.

Note: Some BERs, generated during IML may have a date/time stamp of '00/00 00:00', because the MOSS has not yet fetched the date and time. These BER will appear in the correct sequence in the BER log and should be considered in problem determination.

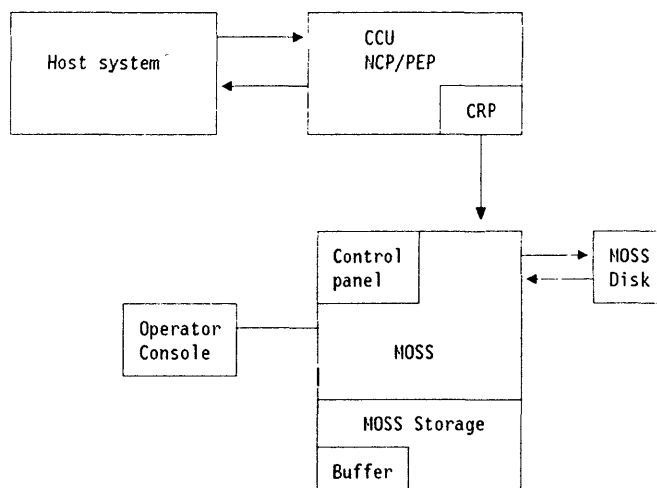


Figure 11-1. Box Event Records Handling

Thresholds

Errors are normally retried by the control program, or the microcode, in order to achieve fault tolerance and eliminate abends or loss of resources on intermittent failures.

When the count is maintained by the Control Program, the threshold values are found in the CDS at initialization (each NCP IPL).

For the whole machine, exhausting a threshold does not change the BER.

| Table 11-1. Threshold Table | |
|-----------------------------|-----------|
| Function or Adapter | Threshold |
| PIO-CA | 8 |
| PIO-LA | 8 |
| AIO-1 | 2 |
| ADP-CA | 2 |
| ADP-LA | 2 |
| Unresolved Level 1 | 2 |
| Unresolved Level 2 | 2 |
| Unresolved Level 3 | 2 |
| Unresolved Level 4 | 2 |
| PCI-2 | 2 |

BER Generalities

BER Generation

The MOSS creates the BERs from information supplied either by the NCP/PEP or by the MOSS itself.

If the MOSS is offline or not operational, the NCP/PEP stores the event or error information in the check record pool (CRP) located in main storage. When the CRP is full, each attempt to store more information increments a count in the CRP, but the information itself is lost. This count is entered into the last BER of the CRP (field **lost** in NCP/PEP BERs). When the MOSS comes back online, the contents of the CRP are transferred to the MOSS. The Figure 11-1 on page 11-5 describes how the information is handled (see also "BER Recovery Procedures" on page 11-25).

In case of MOSS I/O errors the error information supplied by the MOSS itself is stored in a composite BER with ID 85 (see page 11-31).

Automaint builds a reference code for each BER (see page 11-17).

BER Formatting

The MOSS identifies the BER with a number and formats the information together with date, time, flag and other control bytes in the MOSS storage buffer as follows:

| Table 11-2. Format of a BER | |
|-----------------------------|---|
| Byte Number | Contents |
| 1-2 | Total BER length in bytes |
| 3-4 | BER number (identification) |
| 5-12 | Reference code |
| 13-18 | Reserved |
| 19 | Flag |
| 20 | CCU |
| 21-24 | Time of day (binary value in seconds) |
| 25 | Month (in packed decimal) |
| 26 | Day (in packed decimal) |
| 27 | Year (in packed decimal) |
| 28 | BER Type |
| 29 | BER ID |
| 30-nnn | Error information (hexadecimal) (nnn is the total BER length) |

Notes:

1. The MOSS formats the labels for BER display, and supplies both date and time given via time services.
2. The NCP date and time of the BERs may differ from that of the MOSS. The date and time is built by the MOSS when the BER is logged on the disk, and does not necessarily match the moment this event is acknowledged by the NCP.

3. The exact layout depends on the BER type and BER ID (see the BER formats description at the end of each BER type xx section).

| | | | | | | | |
|----------|---|----|----|----|-----|------|----|
| Byte | 21 | 22 | 23 | 24 | 25 | 26 | 27 |
| Contents | 00 | 00 | F5 | 8F | 12 | 21 | 87 |
| Meaning | One bit = 1 sec 62 863 sec = 17h 27m 43s | | | | Dec | 21st | 87 |

Figure 11-2. Example of Date and Time

NCP/PEP BER Formats Versus MOSS BER Formats: The following chart explains why the BER formats and contents of NCP/PEP-generated records are different from the MOSS-generated records.

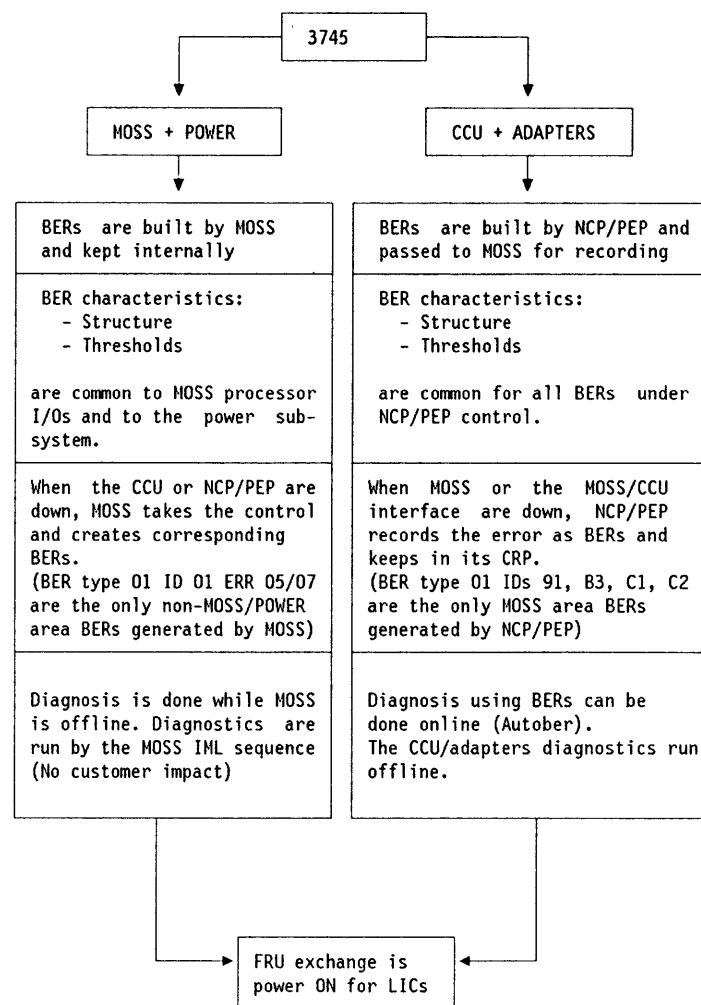


Figure 11-3. BER Formatting by MOSS and NCP/PEP

BER Storage on Disk

The MOSS stores the BERs, prepared in the MOSS RAM, on the **wraparound** BER file on disk in the order of their arrival.

When the BER file is full, the next BER to arrive overwrites the oldest BER (or BERs) in the BER file. No count is kept of such overwrites. The BER file may store several hundred BERs.

BER Storage when the Disk is not Operational: When the disk is not operational, the MOSS keeps the BERs in a buffer in the MOSS RAM. This buffer is preserved during MOSS IML (see Chapter 7). When the buffer is full, new BERs are lost, but a count of lost BERs is kept in a byte of the buffer. This is called the lost record count.

When the disk becomes operational again, MOSS stores the buffer in the BER file on disk, together with a BER giving the number of lost BERs in the event/error description line.

BER File Erasure: The entire BER file can be erased by using the DUMP/DPLY/DEL utility program. **The BER file should not be erased, except in exceptional cases,** since:

- It is not possible to erase individual BERs in the file, but only the entire BER file.
- The service personnel may need old BERs for history purposes.
- The BER file, when full, writes the most recent BERs on the disk space used by the oldest BERs (wraparound file). When the BER file is erased, a BER is logged to that effect in the file. For more details, see *Service Functions*, SY33-2069.

BER Display

Normally, you may access the BER file on the MOSS disk using the 'ELD Function' from the console. For more details on 'How to', see *Service Functions*.

The ELD detail display screen gives you the main information (also called 'fields') on the event represented by the BER.

Some of the fields may not appear on the ELD detail display, but they are part of the BER and they are listed as they appear in the BER file. See the section 'BER Formats on Disk' page 11-99. For more details, refer to *Service Functions* manual.

BER Type and Identification

BER Type

The first byte of information concerning the event, points to the general area of BER occurrence:

Table 11-3. BER Types Description

| Type | Description |
|------|--|
| 01 | MOSS-related events or errors (plus events or errors recorded by MOSS when MOSS takes control of the box, or operations such as CCU hardcheck, scanner errors... |
| 03 | Diagnostic error detection (CE option) |
| 04 | Power subsystem errors, and events reported to MOSS by the power control |
| 10 | Events/errors related to channel adapter operations |
| 11 | Events/errors related to transmission subsystem operations |
| 12 | Control program exceptions (software errors detected by the hardware) |
| 13 | CCU-related events/errors when NCP/PEP has control (excluding CCU hardcheck) |
| 14 | IOC bus-related errors, when not possible to attribute them to a specific adapter |
| 15 | TRSS events/errors related to token-ring subsystem operations |

BER ID

The second byte identifies the category of error or event:

BER Created by the NCP/PEP

bit 0 Probable cause of the error.

OFF The most probable cause is the control program

ON The most probable cause is the hardware or the microcode

bits 1 to 3 Program level that recorded the error/event.

001 Control program level 1

010 " " " 2

011 " " " 3

100 " " " 4

BER Created by the MOSS: When a BER is created by the MOSS, a byte identifies the origin of the error or event.

The complete list of MOSS BER IDs is given in "MOSS BER Type 01 - Summary" on page 11-35.

Here the ID does not refer to event/error categories as in the NCP/PEP. For MOSS BERs, the event/error categories are found in another byte, called 'MOSS-CHECK'.

BER Structure

The BERs have a hierarchical structure, which allows going from the general problem area to the specific failing element.

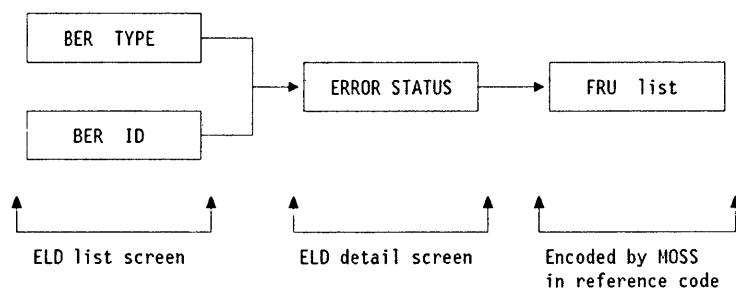


Figure 11-4. Hierarchical Structure of a BER

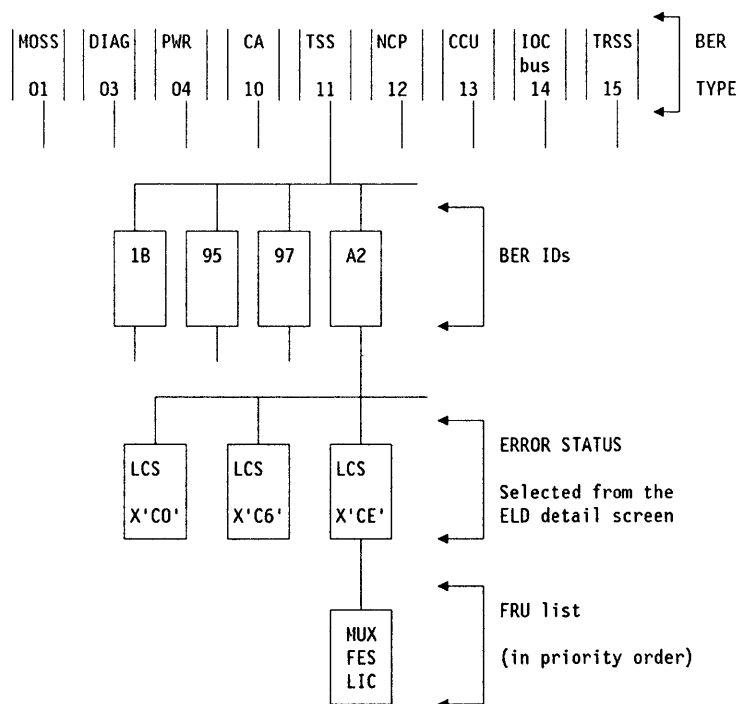


Figure 11-5. Example of a BER Tree Structure

Note: The **error status** is a predetermined field, characteristic of the error. BERs have a different **error status**, according to their type and ID.

BER Handling Tools

Table 11-4. References for BER Handling

| Function | Reference |
|---|--|
| Hexadecimal display at console | <i>3745 Maintenance Information Procedures</i> |
| Hexadecimal display versus MOSS BERs | HMR page 11-30 |
| Host print request for BERs (MOSS ID 00 only) | For software information on BERs originated by NCP/PEP, refer to the associated product documentation. |
| BER formats | HMR, end of every 'BER Type xx' section. |
| BER save, purge, display | <i>3745 Service Functions</i> |
| CE BER updating | HMR, page 11-20, and <i>3745 Service Functions</i> |
| CE manual analysis | HMR, page 11-20. |
| Auto BER analysis | HMR, page 11-19. |

BERs Which Are Not Machine Errors

| Type | ID | EXT | Description |
|------|----|-----|---|
| 01 | 06 | 01 | BER file deleted |
| | | 02 | BER stack overflow |
| | | 07 | MOSS offline request by the operator |
| | 19 | | MOSS IML successful |
| | 20 | 01 | IPL complete without error |
| | 21 | 01 | IPL started |
| | 24 | | Concurrent maintenance started |
| | 25 | | Concurrent maintenance ended |
| | 26 | | Concurrent maintenance cancelled |
| | 27 | | Concurrent maintenance rejected due to traffic |
| | 38 | | Concurrent maintenance NCP request to cancel |
| 03 | 01 | | Diagnostic started |
| | 02 | | Diagnostic completed successfully |
| 04 | 0A | | Power control mode change |
| | 0D | | Set time of day |
| | 14 | | Air flow detected is OK |
| | 15 | | General power OFF (remote, network) |
| | 29 | | End of IML data due to an event |
| | 31 | | Set time of day |
| 11 | 96 | | Battery changed |
| | | | |
| 15 | 96 | | Scanner disconnect state: The scanner has been disconnected by a request from the MOSS operator, and is reporting this to the control program. |
| | | | TRM disconnect state: The TRM has been disconnected by a request from the MOSS operator, and is reporting this to the control program. |

Figure 11-6. BERs which are not Machine Errors

Specific Mechanisms

BER/Alarm/Alert Mechanism on a 3745 Down

Whenever a 3745 down condition is detected, there is a BER/alert/alarm generation mechanism started during the 3745 re-IPL initiated by the MOSS (see table hereafter). The possible causes of a 3745 down condition are:

- CCU hardcheck
- Hardware error
- Software error, hardware-detected
- Software error, software-detected.

| Description | BER ID- Check- Ext field | Alert (m) | Alert (a) | Alarm (m) | Alarm (a) |
|--|--------------------------------|--------------|----------------|--------------|----------------|
| IPL started | 21-01 | - | - | - | - |
| IPL completed W/O error | 20-01 | D0 | - | D0 | - |
| Re-IPL due to hardw. check, completed with error and dump | 06-05-05 | - | 27 | - | 27 |
| Re-IPL due to hardw. check, completed with error, no dump | 06-05-05 | - | 20 | - | 20 |
| Re-IPL due to softw. error, completed W/O error, with dump (depends on abend code) | 06-05-07 | - | 41 42 47 | - | 41 42 47 |
| Re-IPL due to force dump from VTAM | 06-05-07 | - | 48 | | 48 |
| Re-IPL for CP abend | 06-08-07 | - | 40 | | 40 |
| Re-IPL due to softw. error, completed OK, no dump | 06-05-07 | - | 46 | | 46 |
| IPL/re-IPL completed with errors | 06-03-01 | D1 | D1 | D1 | D1 |
| IPL/re-IPL completed with error and dump | 06-06-01 | - | - | 44 | 44 |
| IPL/re-IPL completed with error, no dump | 06-06-01 | - | - | 49 | 49 |

Figure 11-7. Alarm and Alerts Generated by IPL

Notes:

In the header of the above table:

- (m) means Manual
- (a) means Automatic

Analysis of a BER/Alarm/Alert Sequence

Any error detected by the MOSS during the re-IPL checkout tests, and during the re-IPL process is also logged between the BERs signalling the start and the end of re-IPL.

Also, any pending BER found by the MOSS in the CRP, is fetched and logged during re-IPL phase 1B.

Therefore, a typical sequence would appear like this, as seen on the BER file retrieval screen, option **all**:

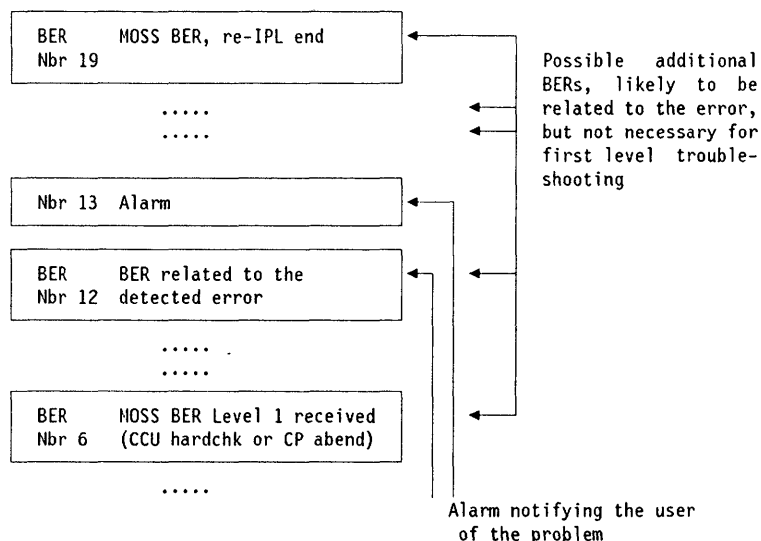


Figure 11-8. Example of a BER/Alarm/Alert Sequence

Note that BERs are displayed in inverted chronological sequence (most recent first).

BER Display

There are three kinds of BER display screens:

- ELD summary
- ELD list
- ELD detail.

When troubleshooting, you should normally display the ELD summary, then the ELD list, and last the ELD detail(s) pertaining to the fault. The BER display procedures and details are given in the *Service Functions* manual, SY33-2069.

Finding the Appropriate ELD Detail Screen

Use the following table to find the page for ELD detail screen explanations for a given BER type and BER ID. This table also shows whether the control program or the MOSS created the BER.

For software information on BERs originated by the NCP/PEP, refer to the associated product publications.

In the ELD detail screens of this chapter, 'hh..' represents an hexadecimal value, 'bbb..' a binary value.

Table 11-5. References for ELD Detail Screen

| Type | Meaning | Created by | Page Number |
|------|---|------------|-------------------------|
| 01 | MOSS-related BERs | MOSS | 11-40 to 11-91 11-98 |
| | All IDs except: 91, B3, C1, C2 | NCP/PEP | |
| 03 | Diagnostic | MOSS | 11-106 |
| 04 | Power control | MOSS | 11-108 |
| 10 | CA-related BER | NCP/PEP | 11-120 |
| 11 | TSS-related BER | NCP/PEP | 11-131 |
| 12 | NCP/PEP related BER | NCP/PEP | 11-139 |
| 13 | CCU-related BER | NCP/PEP | 11-142 |
| 14 | IOC-related BER | NCP/PEP | 11-145 |
| 15 | TRSS-related BER | NCP | 11-149 |
| 02 | A BER type 02 may appear on the ELD list file. It is the type for the alarms logged on the disk. This BER type must be ignored. | | |

Field Common to Many ELD Detail Screens: X'76' and X'76'U: The control program stores the error information in the IOC bus error register in X'76', in order to place its contents in the BER fields. If another IOC bus error occurs while filling in the BER fields, the contents of the IOC bus error register for the second error are placed in the X'76'U field of the IOC BER.

MOSS BER IDs List

| Table 11-6. List of BERs Built by the MOSS | | | |
|--|----------|----------------|-------------------|
| Description | BER Type | BER ID | Refer to page |
| Level 0 error handler | 01 | 00 | 11-40 |
| Level 1 error handler | 01 | 01 | 11-51 |
| MCC error handler | 01 | 02 | 11-53 |
| DFA error handler | 01 | 03 | 11-56 |
| CCA error handler | 01 | 04 | 11-60 |
| MOSS/scanner | 01 | 05 | 11-63 and 11-63 |
| Events when no IPL | 01 | 06 | 11-66 |
| IPL Tasks | 01 | 06 | 11-67 |
| MOSS/TRSS | 01 | 07 | 11-75 |
| CADS dump function | 01 | 08 | 11-78 |
| Disk function | 01 | 10 11 12 | 11-79 and 11-79 |
| Keyboard function | 01 | 13 | 11-79 |
| MIOC function | 01 | 14 | 11-79 |
| Mailbox interface function | 01 | 15 | 11-80 |
| MOSS-CP Interface | 01 | 16 | 11-80 |
| RSF function | 01 | 17 | 11-81 |
| IML complete with error | 01 | 19 | 11-82 |
| MOSS-CP Interface | 01 | 1A to 1D | 11-80 |
| IPL complete with error | 01 | 20 | 11-83 |
| Concurrent maintenance | 01 | 24 to 29 | 11-89 |
| Adapter error on diags | 01 | 30 | 11-89 |
| MCAD error | 01 | 32 | 11-89 |
| Cyclic hour notification | 01 | 36 | 11-91 |
| Concurrent maintenance | 01 | 37 and 38 | 11-89 and 11-91 |
| MMIO interface error | 01 | 39 | 11-91 |
| MOSS composite BER | 01 | 85 | 11-31 and 11-104. |
| MOSS CP interface | 01 | 91 B3 C1 C2 | 11-98 |

Note: The composite BER is displayed only in the ELD list. When you choose the SEL# of BER ID 85 you will see displayed the ELD detail screen of the last BER built by the MOSS.

Scrolling over the composite ELD detail, and using key F8 (F8: NEXT), you get only the last part of the composite BER whose description appears in the BER list. The other parts of the BER can be displayed using key F7 (F7: PREVIOUS) see page 11-31.

AutoMaint

AutoMaint Strategy

The automatic BER analysis (AutoBER) provides a **reference code** (see, "Reference Code Structure" on page 11-22). It identifies, either the faulty FRU(s), the software/microcode errors, or other error causes (for example, CP sysgen).

This reference code is sent both to the network console through alert and to the MOSS console through alarm. When the host operator receives it within the alert, the NetView panels or the *Problem Determination Guide (PDG)* for alarm, may ask him to contact the HCS/HSC, and to give them the reference code.

If NetView is not available, once the alert is received on VTAM it is logged on the LOGREC disk. In this case, the customer must consult the alarm displayed at the MOSS console

The reference code is put in the header of the analyzed BER on disk, and:

- If an alarm must be generated, the reference code is appended to:
 - The alarm on disk, and
 - The alarm on the console.
- If an alert must be generated, the reference code is provided as one of the variable data.

Note: If alarms can always be generated when applicable, alerts need to have a CP loaded and operational to be transmitted from MOSS to NetView through NCP and VTAM. Then, it is not unusual to have some alarms with no alert.

In addition, for some specific cases, only a panel hexadecimal error code is available. Customers have to use the PDG, service personnel will refer to the MIP.

Using the ELD function, CEs and customers can have access to the complete list of alarms, BERs, reference code in the BER file itself, through the MOSS console.

In case of alarm, the CE can log specific information, which will be kept by the system (alarm).

This type of information can be useful to keep a history file of CE interventions.

The different alarms are identified through a two-digit hexadecimal value called the alarm number. When existing, related alert always carries this number through a field called Product Alert Reference Code, not to be confused with the Automaint Reference Code which appears in alert through a field called IBM 3745 Reference Code.

Alerts on NetView screens are generally self explanatory. Code points transmitted in Generic Alerts are translated by NetView into understandable text, except product variable data which is displayed as specified in alert. Then if

the PDG gives the list of alerts with their contents. it is only for information to customers so that they can prepare Clists for automated operations (for example, automatic resource reactivation after a successful error recovery).

Some BERs and related alarms/alerts have no reference code, as they are only reporting major events to the external world (no case of error, for example, CCU (re-)IPL complete, or scanner (re-)IML complete).

When applicable, a valid or meaningful reference code must be retrieve from previous BER(s) and related alarm(s). In the PDG and according to the alarm number, possible causes and recommended actions are given (as for alerts).

- The customer can fix the problem by himself (for example, CP sysgen error, modem power OFF...) or,
- The customer calls the IBM hardware central service (HCS) and gives the reference code and the alarm number.

Automatic BER Analysis

The analysis automatically starts when a BER occurs:

- It is called by the BER-logging task and processes the current BER just after it has been moved from the MOSS buffer into the sector image of the disk.
- It returns control to the logging task upon completion.
- Its purpose is to:
 - Build a reference code, according to the current BER contents and/or the contents of the BER file as output of an automatic correlation process.
 - Send this reference code to the MOSS console, within the ALARM.
 - Send this reference code to the host console, within the ALERT.
 - Write the reference code(s) within the BER and the alarm on the disk

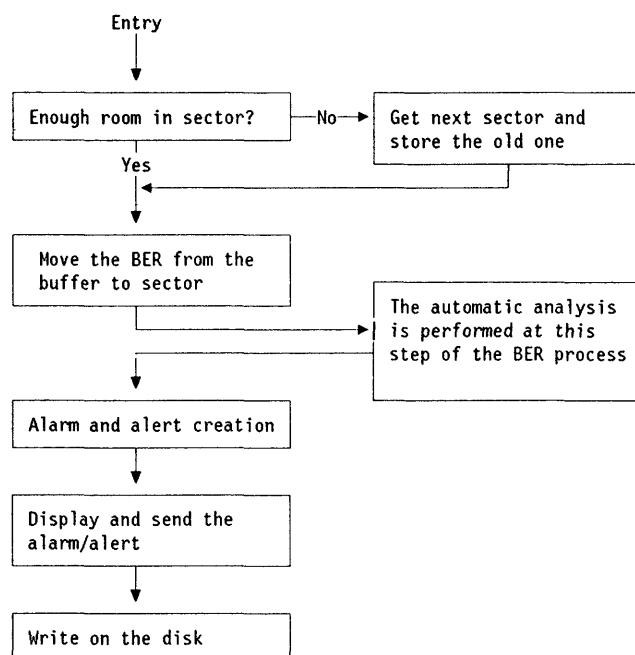


Figure 11-9. Automatic BER Analysis Process Flow

Note: Some BERs will never have an alarm/alert even if they get a reference code and only those reference codes in alarms/alerts must be considered first.

General Process Flow

The automatic BER analysis activates the following functions:

- Analysis of the type and ID of the current BER with either:
 - Direct translation of this BER into a reference code.
 - 'Other BER' analysis, when the last BER refers to another one.
 - Secondary field analysis. Analysis of fields other than type and ID, according to a decision table.

- Correlation with BERs generated before (see correlation process in the *Service Functions* manual).
- Logging of the collected information into the alarm and the alert.

All the information collected in the above steps is stored in a data block called interface block.

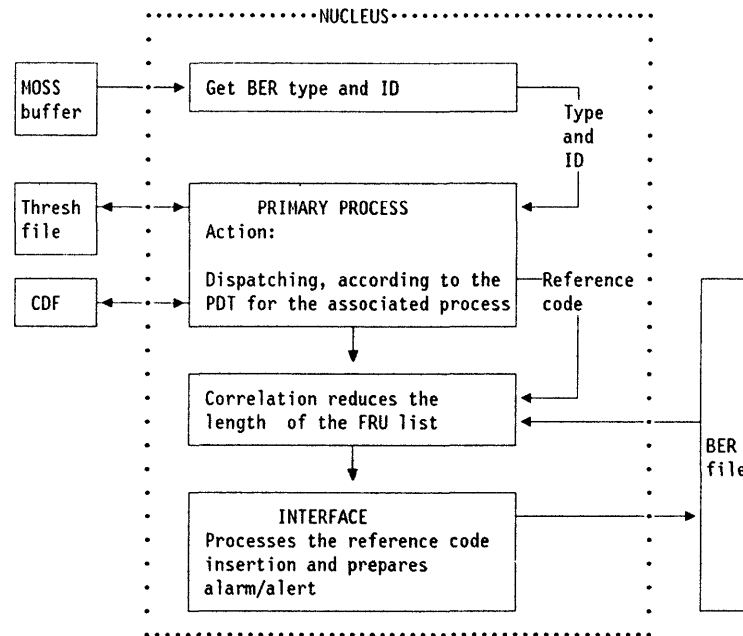


Figure 11-10. Automatic BER Analysis General Process

CE Field Updating

A 40-byte field (CE field), located at the end of the alarm, is made available to the CE so that he can leave some 'personal notes' for himself or for another CE.

Refer to the *Service Functions* manual, for description and updating of that field.

BER Reference Code

In case of a non-permanent failure, different BERs can be logged in the BER file at different times for this intermittent failure.

The automatic process gives, for each BER, a reference code pointing either at an FRU list, or a software/microcode problem. Then the network operator can call the HCS when too many hits occur in a given period.

When the CE arrives at the customer's site and diagnostics do not reproduce the error, the CE will first try to change the FRU(s) which has (have) been called previously (see reference code interpretation), but if this method fails (immediately or in the few days following this intervention), the CE or HCS/HSC will use the MOSS BRC function through RSF:

- **Reference Code Interpretation**

This function displays the FRU list and location, or the list of primary causes associated to a given reference code. It also displays additional information (other causes to be suspected).

Note: Reference code interpretation is also available through RETAIN/URSF and 3745 RDB.

- **Manual FRU Correlation**

Correlation over a user's defined range of BERs.

Correlation only applies to reference code pointing to hardware FRUs. It is only meaningful in the context of a single fault at a time.

Manual FRU Correlation

This procedure ignores the diagnostic BERs (BER type 03) reference codes.

This process correlates all FRUs called by reference codes in the range, to produce a list of suspected FRUs with a priority order based on occurrence times. This process is almost the same as the one described in the FRU correlation process of the automatic BER analysis. The only differences are:

- Manual correlation gives the complete ordered FRU list (by level of occurrence), rather than a reference code (given by the automatic correlation) pointing to the most probably failing FRU(s) (1 or 2).
- Manual correlation is done in a range of BER sequence numbers selected by the CE, whereas automatic correlation is done on a predefined time range.
- No alarm/alert is generated in manual correlation.
- No reference code is generated.

Thus, by looking at all BERs (with or without alarm) occurring at box malfunction time, additional FRU(s) to be suspected can be pointed out.

Automatic FRU Correlation

- **Triggering**

The correlation is started if:

- The current BER generates an alarm by itself, and
- The current BER is related to a hardware FRU list.

- **Correlation Range**

The correlation process is done starting from the current BER, and going back up to the BERs logged during the last three minutes, or to the end of the file if needed.

- **Procedure**

The FRU correlation procedure is described in the *Service Functions* manual.

Reference Code Structure

3745 reference codes are generated by the microcode which runs in the MOSS to provide an automatic analysis of box event records (BERs). The reference code has eight significant digits (D1 to D8).

According to the combinations of the values of:

- D1
- D2-D3

the other fields may provide different kinds of information. (See Figure 11-14 on page 11-24 after the 2 examples below).

Reference code related to a hardware problem:

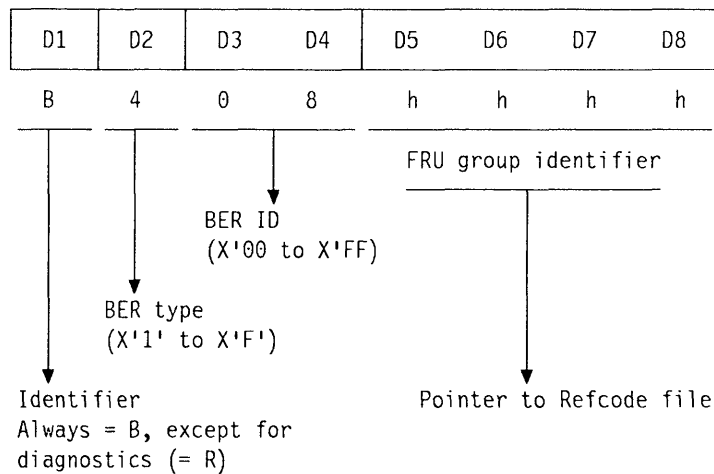


Figure 11-11. Example of a Power BER Type 4 ID 08

Reference code related to a multiple source problem:

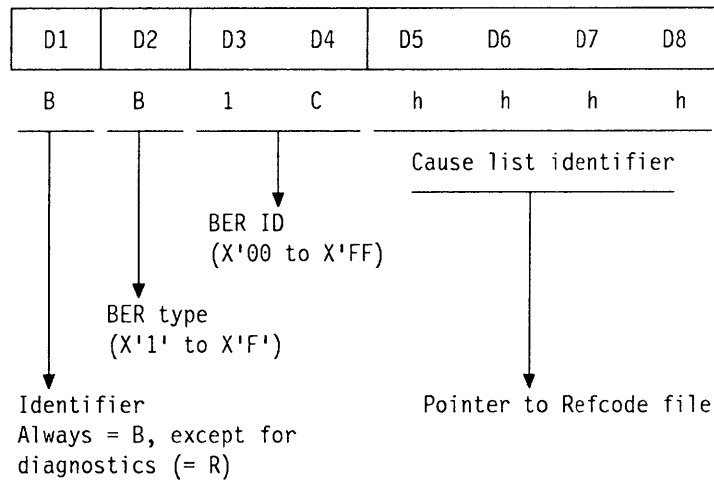


Figure 11-12. Example of a Power BER Type 11 ID 1C

Reference code related to a software/microcode problem:

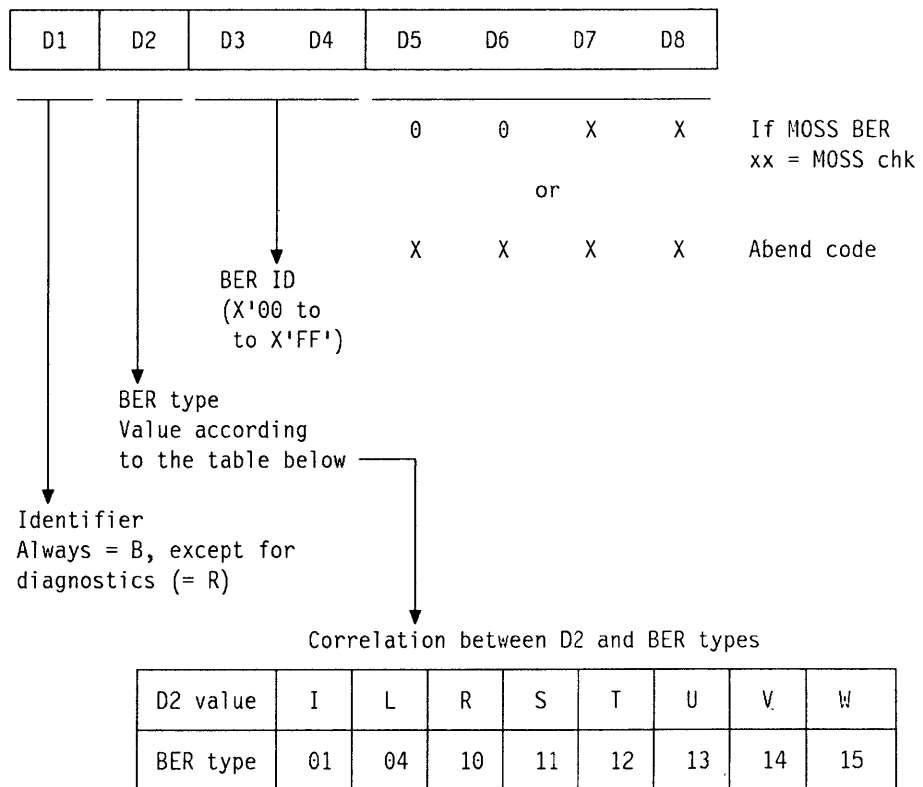


Figure 11-13. Example of a Software/Microcode Problem

Reference Codes.

| D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | |
|----|------------------------------|-----------------------------|----|--------------------------------|------------------------------|---------------------|----|---|
| B | 1, 4 A, B C, D E, F | ID | | FRU GROUP Number | | | | ← - HARDWARE FRUs pointed - MAP |
| B | G | Associated FRU indicator | | FRU GROUP Number | | | | |
| B | J | Type | ID | ADAPT Nb Note 1 | ADAPT Nb | ADAPT Nb | ← | |
| B | I, L R, S T, U V, W | ID | | ABEND CODE or MOSS Check | | | | ← SOFTWARE/ MICROCODE error |
| B | X | First FRU logical number | | | Second FRU logical number | | | ← CORRELATION |
| R | G | Associated FRUs | | FRU logical number | | | | ← DIAGNOSTICS |
| | H | Associated FRUs | | INDEX 1 (Note 2) | | INDEX 2 (Note 2) | | |
| | 3 | ID | | FRU GROUP number | | | | |
| | K | ID | | MOSS Check | | | | |
| B | Z | Type | ID | X'FOFOFO' (no error) | | | | ← DUMMY |
| | | | | X'FOFOF1' (Meaningless) | | | | |
| | | | | Program in error | | Seq. Number | | |

Figure 11-14. Reference Code Structure

Note: ADAPT Nb. is actually CA absolute number (displayable digit 0 to F).

BER Recovery Procedures

Before being logged and stored on the disk, BERs are kept in MOSS and/or CCU storage. While in this transition stage, the BERs are volatile, and are lost if a power-OFF or power-ON reset occurs.

MOSS Handling of 3745 Down

The MOSS has stored a BER in the BER stack (in MOSS storage), but could not log it on the disk. In that case, MOSS will display the error code of the MOSS BER 01 ID 00. Display the BER using the procedure given in the *Service Functions*, SY33-2069. The remaining two digits may be interpreted by referring to page 11-41.

IOC Bus and Adapters

The following three BER types can occur for failures in this area:

- BER type 10

An error is detected while the control program is involved in a transaction with a channel adapter.

- BER type 11

- An error is detected while the control program is involved in a transaction with a communication scanner **and** the control program has identified the scanner concerned.
- A specific communication scanner reports an error to the control program.

- BER type 14

An error is detected while the control program is involved in a transaction with an adapter **and** no adapter can be identified as the source of the error.

Note: A single intermittent error can be reported as BER types 10, 11, or 14, depending on the time at which the error occurred, and the control program or microcode transaction that was taking place at that time. In this case, correlation may be useful to narrow down the range of possible failing components.

Scanner Errors Without BERs

Some errors in a communication scanner may not lead to a BER, although information within the scanner is available to help in fault isolation. Use the following procedure:

1. Start an internal or external SIT. Refer to the *3745 Service Functions*.
2. When the problem occurs, stop the SIT.
3. Analyze the SIT. Use the TSS services to display the scanner storage:

Unresolved Interrupts

The control program logs BERs based on 'unresolved situations' (see "BER/Alarm/Alert/Mechanisms" page 11-13).

Unresolved Level 1 CA Adapter Error (BER 10 ID 9E)

There are two possible types of unresolved CA level 1 interrupts.

- A CA level 1 occurs and no bit is ON in the CA external register X'E'.
- There is a CA level 1 and none of the following bits is ON in the CA external register X'D':
 - 0.0 IOC bus parity error
 - 0.1 internal bus parity error
 - 0.2 CCIN card check
 - 0.4 CHIN card check
 - 0.5 address compare error
 - 1.0 output exception check
 - 1.1 PIO halt remember latch
 - 1.2 cycle steal halt remember latch
 - 1.3 bus in check interface A
 - 1.6 CADR card check interface A

The following bits are checked in X'0'. If none is ON, the control program builds a BER 10 B1:

- 0.0 (normal) initial selection interrupt
- 0.1 interface disconnect
- 0.2 selective reset
- 0.3 channel bus out check
- 0.5 stacked initial status
- 0.6 ESC status byte cleared
- 0.7 system reset.

Unresolved Level 3 CA Data/Status (BER 10 ID B2)

The following bits in are checked in X'2'. If none of these bits is set and the system reset bit in X'0' is not set (bit 0.7), the control program builds a BER 10 B2:

- 0.0 outbound data transfer sequence
- 0.1 inbound data transfer sequence
- 0.2 (final) status transfer sequence
- 0.5 channel stop/interface disconnect
- 0.6 suppress out monitor interrupt
- 1.1 data/status selective reset
- 1.3 stacked ending status.

Unresolved Level 3 CA Interrupt

If, in NCP/EP/PEP, there is no CA control block that has selected bits matching those of the interrupting CA, then a BER 10 33 is built.

Scanner AIO Unresolved Errors (BER 11 ID 92)

For the TSS, interrupts are unresolved if:

- In X'7E', bit 0.7 (IOC level 1 summary) is ON.
- In X'76', bit 0.6 (adapter-initiated operation) is ON.
- In X'75', bit 0.0 (AIO CSCW) is ON.

Then, following the IOH to read the error status, one of the following bits is ON in X'76'.

- 0.4 IOC time out.
- 0.5 IOC bus in parity error.

Scanner Adapter Unresolved Error (BER 11 ID 9A)

- In X'7E' bit 0.5 IOC adapter level 1 request.
- The error status returned an IOH read error status command = 0.

Scanner Level 2 Unresolved (BER 11 ID A1)

There are 3 types of unresolved/undefined interrupts:

- A level 2 interrupt that occurs on a non-SYSGENed line.
- A level 2 interrupt from a SYSGENed line with the SCF, SES, and LCS all zero.
- A level 2 interrupt from a SYSGENed line, but the received status does not match the expected one.

CCU Level 1 Unresolved Interrupts (BER 13 ID 91)

The following bits are checked in X'7E'. If none is set, the control program builds a BER 13 91:

- 0.0 MOSS inoperative
- 0.1 any CCU hard error
- 0.3 level 5 I/O error
- 0.4 invalid operation
- 0.5 IOC adapter level 1 request
- 1.0 address compare level 1
- 1.1 address exception I fetch
- 1.2 storage protect I fetch
- 1.3 address exception program execution
- 1.4 storage protect program execution
- 1.6 IPL level 1 request.

CCU Level 3 Unresolved Interrupt (BER 13 ID B1)

This condition occurs in three different environments:

- NCP only
- PEP
- Remote NCP (from the host standpoint)

The checks are then different.

- **NCP Only**

The following bits are checked. If none of them is set, the control program builds a BER 13 B1:

- X'77' bit 1.0 CA level 3 interrupt
- X'77' bit 1.1 CA level 3 interrupt
- X'F' bit 0.2 CA level 3 initial selection request
- X'F' bit 0.3 CA level 3 data/status request
- X'7F' bit 0.6 user interrupt request level 3
- X'7F' bit 1.5 internal timer interrupt level 3
- X'7F' bit 1.6 PCI level 3.

- **PEP**

The following bits are checked. If none of them is set, the control program builds a BER 13 B1:

- X'F' bit 0.2 CA level 3 initial selection request
- X'F' bit 0.3 CA level 3 data/status request
- X'7F' bit 0.6 user interrupt request
- X'7F' bit 1.5 internal timer level 3
- X'7F' bit 1.6 PCI level 3.

- **Remote NCP**

If X'77' bit 1.0 or bit 1.1 is set, and none of the following bits is set, the control program builds a BER 13 B1:

- X'7F' bit 0.6 user interrupt request
- X'7F' bit 1.5 internal timer level 3
- X'7F' bit 1.6 PCI level 3.

A BER 10 B7 is built if:

- X'77' bit 1.0 or bit 1.1 is reset, and
- CA is attached and installed (not defined).

Otherwise, a BER 13 32 (level 3 interrupt configuration check) is built.

CCU Unresolved Level 4 Router (BER 13 IDs C1/C2/C3)

Two conditions may be detected by the level 4 router:

- General unresolved condition
- Unresolved with respect to a PCI Level 4.
- **General Unresolved Condition**

If none of the following bits is set in the X'7F' when a level 4 interrupt occurs, the control program builds a BER 13 C1:

- X'7F' bit 0.3 MOSS request service
- X'7F' bit 0.4 MOSS response service
- X'7F' bit 0.7 PCI level 4 interrupt
- X'7F' bit 1.7 service request.

- **Unresolved Level 4 PCI**

The control program builds a:

- BER 13 C2 if X'7F' bit 0.7 is set, and no reason byte is set in the level 4 router control block.
- BER 13 C3 if the control program cannot reset the level 4 PCI latch.

Unresolved IOC Bus Errors (BER 14 IDs 91/92)

- **Unresolved Adapter Level 1 (BER 14 91)**

- In X'7E' bit 0.5, IOC adapter level 1 request, is ON.
- Following an IOH broadcast poll command to identify the board with the adapter problem, X'7E' bit 0.7, IOC level 1 summary, is ON.

- **Unresolved AIO Level 1 (BER 14 92)**

- X'7E' bit 0.7, IOC level 1 summary, is ON.
- X'76' bit 0.6, adapter initiated operation, is ON.
- X'75' is invalid. This is true when:
 - **Either**

X'76' bit 0.2, (IOC invalid CSCW) is ON
 - **Or**

X'76' bit 0.4, (IOC timeout) is ON
and IOC status (X'76' bits 0.0 to 0.3) = 2.
 (No response to TA tag or cycle steal grant.
 - **Or**

X'76' bit 0.5 (IOC bus IN parity error) is ON
and IOC status (X'76' bits 0.0 to 0.3) = B.
 (Loading the CSCW).

- **Unresolved PIO Level 1 (BER 14 93)**

- X'7E' bit 0.7 (IOC level 1 summary) is ON.
- X'76' bit 0.6 (adapter-initiated operation) is OFF.
- X'76' bits 0.4 (IOC time out) and 0.5, (IOC bus in parity error) are OFF.

MOSS Error Logging

Hexadecimal Codes

During MOSS IML, hexadecimal codes appear on the operator's panel. They are either progression codes (events), or errors.

Hexadecimal codes and BERs: The hexadecimal codes may be related to a BER. In other cases, a BER is created when the hexadecimal code is displayed.

The connection between the hexadecimal code and the BER may be done by using the time stamp (indicating when the BER was built), and by the field **hexa display** bytes 34 and 35 of MOSS BER foM0 page 11-99. For error decoding, see "MOSS Check Error Decoding" on page 11-31.

Table 11-7. Hexadecimal Codes Summary (Errors Only)

| Hex codes | Meaning | Action | Ber created | Type of info |
|-----------|---|------------------------|--------------|----------------------------|
| 001-04F | Power errors | | NO | |
| 050-17F | Error during ROS/Storage/DFA diags | | NO | |
| 180-1FE | Error during diags in RAM MOSS test | | NO | |
| 1FF | MOSS storage diag OK | | NO | |
| Axx-Bxx | IML stop on error (doesn't force re-IML) | MOSS level 0 interrupt | ID 00 | |
| Cxx | MOSS re-IML threshold reached (xx MOSS IML attempts within a given period of time) | MOSS level 0 interrupt | ID 00 | |
| D00-DFF | IML stop on disk/diskette error (doesn't force re-IML) | MOSS level 0 interrupt | ID 00 | |
| | (D00 = MOSS dump complete) | | | |
| | MOSS level 0 re-entry (re-IML) | MOSS level 0 interrupt | | |
| | MOSS level 0 re-entry while in re-IML | MOSS level 0 interrupt | | |
| F00 | Start of MOSS dump | | | |
| F01 | MOSS dump complete | | | |
| F10-F61 | IPL check | | ID 00 ERR 06 | Code to suspected FRU list |
| FEx | IML complete with error | | ID 19 | |
| FFA | Status progression steps which occur during the IPL sequence. IPL has completed but has detected a PCA1 adapter error. Local console may not be accessible. | | ID 06 ERR 03 | |
| FFE | IPL complete with error | | ID 06 ERR 03 | |
| FFF | IPL canceled after error detection | | ID 06 ERR 06 | |

Hexadecimal Codes Versus MOSS BER ID 00

When a blinking hexadecimal code is displayed, it means that the MOSS was unable to build the corresponding BER. The information concerning this BER can be found if the function DDD (dump, display, delete) is used with the address given by the parameter 'CHGHVBER', see *Service Functions*. (See "BER TYPE 01 ID 00 Error Code Description" on page 11-41 for details).

MOSS Check Error Decoding

All the MOSS check codes described in the list on Table 11-11 on page 11-41 have the following decoding.

When the faulty FRU or FRUs given by the hexadecimal code list in the 3745 MIP is exhausted and the error persists, or is transient (intermittent), it is advisable to analyze the corresponding BER, if any.

In the MOSS BER ID 00, the contents of the **MOSS check** field (see: Figure 11-14 on page 11-24) is very helpful to analyze the error. The figure below shows the information provided in this field. Alert/alarm 02 indicates that during the error, a re-IML is performed and a dump is taken.

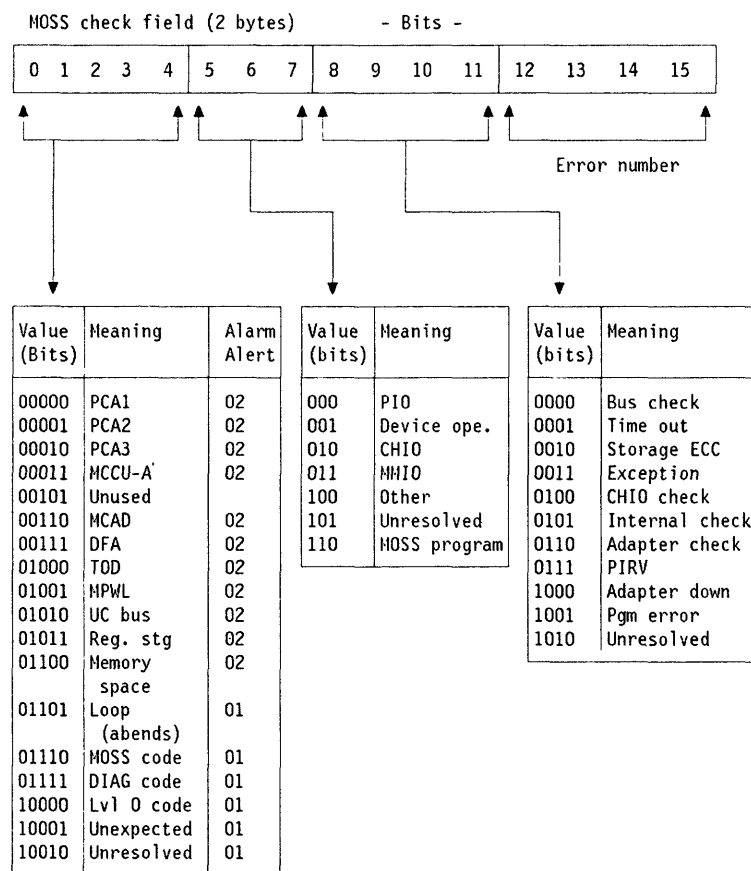


Figure 11-15. Decoding of the MOSS Check Field

Composite BER

The MOSS stacks all BERs which can be produced all along a given request, in a composite BER (type 01 ID 85) and only the last BER stacked asks for the queueing in the BER buffer pool. The composite BER is a variable-byte buffer (see page 11-104).

Scrolling over a composite ELD detail, and using the key F8 (F8: NEXT), you get only the last part of the composite BER whose description appears in the ELD list. The other parts of the BER can be displayed using the F7 key (F7: PREVIOUS).

Four cases lead to a BER reporting activity:

1. A MOSS function requests an I/O operation, and a hardware error is reported to the level 0 of the adapter code, and finally, to the task itself.

The selected command sets a pointer to the composite BER buffer, clears the data area, initializes the composite BER header and sends the I/O request. When the I/O error is reported to the level 0 of the MOSS control code, and only when that error is not recoverable, the level 0 identifies the failing adapter, and stacks the BER (Type 01 ID 00).

The level 0 control code then schedules the machine check information of the adapter. According to the kind of event or error, one of the following BERs is created:

- Moss/MCC HLIR Type 01 ID 02
- Moss/MCC CAC Type 01 ID 02
- Disk file adapter CAC Type 01 ID 03
- Keyboard display adapter ... Type 01 ID 04

The MOSS gets control back at the end of the invoked command and calls, when an error is found, a control code function which stacks a second BER according to the called function:

- Disk function Type 01 ID 10, 11, 12
- MOSS console Type 01 13
- MIOC function Type 01 14
- Mailbox interface function.. Type 01 15
- MOSS-CP interface Type 01 16
- RSF MOSS function Type 01 17

Then this function queues the composite BER in the buffer pool. The composite BER may contain a variable number of BERs, but usually, it contains three BERs.

Composite BER (Type 01, ID 85) example: If a MOSS level 0 occurs during a disk I/O operation related to a LOAD request from an application, a BER 01 85 is logged. (Assume that, for this example, it is **SEL# 233**). This BER contains:

- SEL# 233.3 BER 01 11 Disk adapter
- SEL# 233.2 BER 01 03 CAC
- SEL# 233.1 BER 01 00 Level 0

A selection number for a BER 01 85 is displayed with the event description related to the latest BER put into the BER 01 85. You may scroll from the ELD detail screen to display the other BERs contained in BER 01 85 using **F7: PREVIOUS**.

In the example above, the event description first displayed on the ELD detail screen for SEL# 233 will refer to SEL# 233.3 BER 01 11.

- Pressing 'F7: PREVIOUS' will display SEL# 233.2 BER 01 03.

- Pressing 'F7: PREVIOUS' a second time will display SEL# 233.1 BER 01 00.

If you scroll forward to SEL# 233 from SEL# 232 using 'F8: NEXT', the first detail displayed is SEL#233.3. You must then use 'F7: PREVIOUS' to display SEL# 233.2 and SEL# 233.1 as described above.

2. A MOSS function has requested an I/O operation and a hardware error is reported to the adapter code and finally to the task itself.

This case is basically identical to case 1 except for level 0 processing. In the above case, the composite BER contains two BERs.

3. No active MOSS function requests an I/O operation, but a hardware error is reported to MOSS level 0 and to the adapter code. Level 0 handles the process and uses its own composite BER buffer. The machine check microcode queues the composite BER in a buffer. In this case, the composite BER contains two BERs.

4. No active MOSS function requests an I/O operation, but a hardware error is reported to the adapter.

This case is basically identical to case 3 except for the level 0 processing. In this case, the composite BER contains one BER. The composite BER process is automatically done by the microcode.

MOSS BERs Used With the IPL Application

The following BERs are used by MOSS in connection with an IPL application:

| Table 11-8. MOSS BER Used With IPL Application | | | | |
|--|------------|------|----------------------------------|---------|
| ID | Error code | Ext. | Description | Format. |
| 06 | 03 | 01 | IPL complete + errors (1) | FoM6 |
| | 06 | 01 | IPL check | " |
| | 05 | 05 | CCU hardcheck as alert support | FoM19 |
| | 05 | 07 | Program request as alert support | " |
| | 08 | 05 | CCU hardcheck as alarm support | FoM9 |
| | 08 | 07 | Program request as alarm support | FoM19 |
| | 09 | | CLDPabend as alarm support | FoM10 |
| 20 | 01 | | IPL complete without errors | FoM21 |
| 21 | 01 | | IPL started | FoM23 |

Note: (1) Non-blocking errors.

MOSS BER Type 01 - Summary

| Table 11-9 (Page 1 of 5). MOSS BER Type 01 Summary | | | | | | |
|--|------------------|-------------|---|------------------------|----------|----------|
| BER ID | MOSS Chk code | BER Add Fld | Event Description | Recovery or PGM Action | ALERT | ALARM |
| 00 | | | See MOSS-CHECK code for software error See MOSS-CHECK code for hardware error | | 01 02 | 01 02 |
| 01 | 01 | | See MOSS 01 ID 01 field description | MOSS retry | NO | NO |
| 01 | 02 | | See MOSS 01 ID 02 field description | MOSS retry | NO | NO |
| 01 | 02 | | IOC operation error during MIOH (CCU to MOSS status A register, X'11', bit 0) | MOSS retry | NO | NO |
| 01 | 02 | | IOC operation error (limit threshold) | MOSS down | NO | 03 |
| 01 | 03 | | Adapter clock check (MCC status register 2, bit 4) | MOSS retry | NO | NO |
| 01 | 03 | | Adapter clock check (limit threshold) | MOSS down | NO | 03 |
| 01 | 04 | | CCU clock check (MCC status register 2, bit 3) | MOSS retry | NO | NO |
| 01 | 04 | | CCU clock check (limit threshold) | MOSS down | NO | 03 |
| 01 | 05 | | CCU hardcheck detected (CCU to MOSS status A register, X'11', bit 6). Upon detection of this event, MOSS will automatically start a CCU automatic re-IPL. See Specific Mechanism, page 11-13 | NCP re-IPL | | |
| 01 | 07 | | MOSS TRSS interface | | NO | NO |
| 01 | 08 | | CADS dump function | | NO | NO |
| 01 | 09 | | Address exception check in CCU (CCU to MOSS status A register, X'11', bit 5) | MOSS down | NO | 03 |
| 01 | 0A | | MOSS/MIOC operation check, CCU detected (CCU to MOSS status A register, X'11', bit 7) | MOSS down | NO | 03 |
| 02 | any | | CCU logical interface | MOSS down | NO | 03 |
| 02 | any | | CCU logical interface | MOSS fnct message | NO | NO |
| 03 | any | | Disk drive and/or adapter error CNT=10 DEVICE CODE=X'02', X'04', X'06' | MOSS inop | 07 | 07 |
| 03 | any | | Diskette file error CNT not 10 and DEVICE CODE = X'07' | MOSS inop | 06 | 06 |
| 03 | any | | Disk drive and/or adapter error CNT = 10 and DEVICE CODE = X'01' | MOSS inop | 04 | 04 |
| 03 | any | | Disk file error CNT not 10 and DEVICE CODE = X'03', X'05' | MOSS inop | 05 | 05 |
| 04 | 0A | | Local console CAC detected exception interface | Console not available | 0A | 0A |
| 04 | 0C | | Local console CAC detected error (interface) | | 0A | 0A |
| 04 | 40 | | Local console error (device) (CCA basic status register bits 4 and 5) | | 0B | 0B |
| 04 | 8A, 8C | | Remote console interface error | | 0C | 0C |
| 04 | C0 | | Remote console error (device) | | 0D | 0D |
| 05 | 00, BD, BI | | MOSS-scanner interface error. Soft re-IML OK, dump OK. Error detected by MOSS levels 1 or 4, when communicating with a scanner: <ul style="list-style-type: none"> MCC status register 1, bit 6, at level 4 CCU to MOSS status A register X'11' bit 0 | MOSS fnct message | 61 | 61 |

MOSS BER

| Table 11-9 (Page 2 of 5). MOSS BER Type 01 Summary | | | | | | |
|--|----------------------|-------------|--|------------------------|-------|-------|
| BER ID | MOSS Chk code | BER Add Fld | Event Description | Recovery or PGM Action | ALERT | ALARM |
| 05 | 00 to 03, BD, BI | | MOSS-scanner interface error. Soft re-IML OK, dump KO. Error detected by MOSS levels 1 or 4, when communicating with a scanner: <ul style="list-style-type: none"> MCC status register 1, bit 6, at level 4 CCU to MOSS status A register X'11' bit 0, and X'76' bits 0.6 or 0.7, at level 1 | MOSS funct. message | 65 | 65 |
| 05 | 00, 02 to 04, BD, BI | | MOSS-scanner interface error Soft re-IML KO, dump OK. Error detected by MOSS levels 1 or 4, when communicating with a scanner: <ul style="list-style-type: none"> MCC status register 1, bit 6, at level 4 CCU to MOSS status A register X'11' bit 0, and X'76' bits 0.6 or 0.7, at level 1 | MOSS funct. message | 62 | 62 |
| 05 | 00, BD, BI | | MOSS-scanner interface error Hard re-IML OK, dump OK. Error detected by MOSS levels 1 or 4, when communicating with a scanner: <ul style="list-style-type: none"> MCC status register 1, bit 6, at level 4 CCU to MOSS status A register X'11' bit 0, and X'76' bits 0.6 or 0.7, at level 1 | MOSS funct. message | 67 | 67 |
| 05 | 00 to 03, BD, BI | | MOSS-scanner interface error Hard re-IML OK, dump KO Error detected by MOSS levels 1 or 4, when communicating with a scanner: <ul style="list-style-type: none"> MCC status register 1, bit 6, at level 4 CCU to MOSS status A register X'11' bit 0, and X'76' bits 0.6 or 0.7, at level 1 | MOSS funct. message | 68 | 68 |
| 05 | 00, 01, BD, BI | | MOSS-scanner interface error Hard re-IML KO, dump OK. Error detected by MOSS levels 1 or 4, when communicating with a scanner: <ul style="list-style-type: none"> MCC status register 1, bit 6, at level 4 CCU to MOSS status A register X'11' bit 0, and X'76' bits 0.6 or 0.7, at level 1) | MOSS funct. message | NO | NO |
| 05 | 00, 01, BD, BI | | MOSS-scanner interface error Hard re-IML KO, dump OK. Error detected by MOSS levels 1 or 4, when communicating with a scanner: <ul style="list-style-type: none"> MCC status register 1, bit 6, at level 4 CCU to MOSS status A register X'11' bit 0, and X'76' bits 0.6 or 0.7, at level 1) | MOSS funct. message | 6B | 6B |
| 05 | 01 to 03, BD, BI | | MOSS-scanner interface error. Hard re-IML KO, dump KO. Error detected by MOSS levels 1 or 4, when communicating with a scanner: <ul style="list-style-type: none"> MCC status register 1, bit 6, at level 4 CCU to MOSS status A register X'11' bit 0. and X'76' bits 0.6 or 0.7, at level 1. | MOSS funct. message | 66 | 66 |
| 06 | 01 | | BER file deleted (via MOSS command) | File purged | NO | NO |
| 06 | 02 | | BER stack overflow in MOSS storage.(MOSS maintains a 5K-bytes buffer to stack incoming BERs, before logging on) | | NO | NO |

Table 11-9 (Page 3 of 5). MOSS BER Type 01 Summary

| BER ID | MOSS Chk code | BER Add Fld | Event Description | Recovery or PGM Action | ALERT | ALARM |
|--------|---------------|-------------|---|------------------------|-------|-------|
| 06 | 03 | 01 | <p>IPL complete with errors. Some errors do not prevent the completion of IPL:</p> <ul style="list-style-type: none"> • Scanner not IMLed successfully • Bad parameters passed by control program • Errors in CA monitoring task • Error, found on the diskette, which is not detrimental for the IPL • Console or console adapter error <p>Corresponding BERs are in the BER File. There is a message on the console.</p> | IPL completion | D1 | D1 |
| 06 | 04 | | LAXx (Lines xxxx-yyyy) IML failed | | 6A | 6A |
| 06 | 05 | 05 | <p>NCP re-IPL end and no dump MOSS creates this entry to end the re-IPL and generates the alert reporting the error which caused the re-IPL. CCU hardcheck BER as alert support (see Specific Mechanism, page 11-13)</p> | | 20 | 20 |
| 06 | 05 | 05 | <p>NCP re-IPL end and dump MOSS creates this entry to end the re-IPL and generates the alert reporting the error which caused the re-IPL. CCU hardcheck BER as alert support (see Specific Mechanism, page 11-13)</p> | | 27 | 27 |
| 06 | 05 | 07 | <p>NCP re-IPL end and no dump. MOSS creates this entry to end the re-IPL and generates the alert reporting the error which caused the re-IPL. CCU re-IPL on program request (see Specific Mechanism, page 11-13)</p> | | 46 | 46 |
| 06 | 05 | 07 | <p>NCP re-IPL end and dump, and ABENDs : 910, 911, 930, 931. MOSS creates this entry to end the re-IPL and generates the alert reporting the error which caused the re-IPL. CCU re-IPL on program request (see Specific Mechanism, page 11-13)</p> | | 41 | 41 |
| 06 | 05 | 07 | <p>NCP re-IPL end and dump and ABENDs : 912, 915 (mismatch sysgen/re-IPL). MOSS creates this entry to end the re-IPL and generates the alert reporting the error which caused the re-IPL. CCU re-IPL on program request (see Specific Mechanism, page 11-13)</p> | | 42 | 42 |
| 06 | 05 | 07 | <p>NCP re-IPL end and dump, other abends. MOSS creates this entry to end the re-IPL and generates the alert reporting the error which caused the re-IPL. CCU re-IPL on program request (see Specific Mechanism, page 11-13)</p> | | 47 | 47 |
| 06 | 05 | 07 | <p>NCP re-IPL end and dump, ABEND 7FFF. MOSS creates this entry to end the re-IPL and generates the alert reporting the error which caused the re-IPL. CCU re-IPL on program request (see Specific Mechanism, page 11-13)</p> | | 48 | 48 |

Table 11-9 (Page 4 of 5). MOSS BER Type 01 Summary

| BER ID | MOSS Chk code | BER Add Fld | Event Description | Recovery or PGM Action | ALERT | ALARM |
|--------|---------------|-------------|--|------------------------|-------|-------|
| 06 | 06 | 01 | IPL complete with check, hardware cause. The MOSS microcode action is dependent upon the kind of NCP IPL or IML error found, see hexadecimal display. IPL check Fxx | | NO | 25 |
| 06 | 06 | 01 | IPL complete with errors, dump on disk. The MOSS microcode action is dependent upon the kind of NCP IPL or IML error found, see hexadecimal display. IPL check Fxx | | NO | 44 |
| 06 | 06 | 01 | IPL complete with errors, no dump on disk. The MOSS microcode action is dependent upon the kind of NCP IPL or IML error found, see hexadecimal display. IPL check Fxx | | NO | 49 |
| 06 | 07 | | MOSS offline request by operator | MOSS offline | B7 | B7 |
| 06 | 08 | 05 | NCP re-IPL for CCU hardcheck. CCU to MOSS status A register, bit 6. See BER 01 01 05 which precedes it. This BER allows the MOSS to create an alarm. See Specific Mechanism, page 11-13 | IPL process phase 1B | NO | 24 |
| 06 | 08 | 07 | NCP re-IPL for control program abend. Control program abend, no BER in CRP (ext register X'79' bit 0.2, raising CCU to MOSS register X'11' bit 1 in MOSS). See BER 01 01 07 which precedes it. This BER allows the MOSS to create an alarm. See Specific Mechanism, page 11-13 | IPL process phase 1B | NO | 40 |
| 06 | 09 | | CLDP check. (Output X'70' with cause of check in external register X'72' bytes 0 and 1). Hex display indication at control panel. | IPL stopped | NO | D2 |
| 07 | | | TRSS MOSS BER | | NO | NO |
| 08 | | | Error on MOSS/TRSS interface | | NO | NO |
| 10 | | | DISK macro | | NO | NO |
| 11 | | | DISK macro | | NO | NO |
| 12 | | | DISK macro | | NO | NO |
| 13 | | | KBD macro | | NO | NO |
| 14 | | | MIOC function, MOSS to CCU | | NO | NC |
| 15 | | | Mailbox in request | | NO | NO |
| 16 | | | CCU buffer request | | NO | NO |
| 17 | | | RSF BER (See Specific Mechanism, page 11-13) | | NO | NO |
| 18 | | | Scanner re-IMLed successfully | | 09 | NO |
| 19 | | | MOSS IML successful or with non-blocking errors | | 0F | 0F |
| 1A | | | CHIO | | NO | NO |
| 1B | | | Power error | | NO | NO |
| 1D | | | MCAD adapter error | | NO | NO |
| 20 | 01 | | IPL completed with error | | D0 | NO |
| 21 | 01 | | IPL started | | NO | NO |
| 24 | | | Concurrent maintenance started | | C0 | C0 |
| 25 | | | Concurrent maintenance ended | | C1 | C1 |
| 26 | | | Concurrent maintenance cancelled | | C2 | C2 |
| 27 | | | Concurrent maintenance rejected due to traffic | | C3 | C3 |

Table 11-9 (Page 5 of 5). MOSS BER Type 01 Summary

| BER ID | MOSS Chk code | BER Add Fld | Event Description | Recovery or PGM Action | ALERT | ALARM |
|--------|---------------|-------------|--|------------------------|-------|-------|
| 30 | | | MOSS warning adapter(s) during IML | | NO | NO |
| 32 | | | MOSS MCAD error | | 02 | 02 |
| 36 | | | Cyclic hour notification | | NO | NO |
| 38 | | | Concurrent maintenance NCP request to cancel | | C7 | C7 |
| 39 | | | MMIO interface error | | AB | AB |
| 41 | | | Repair action started | | NO | NO |
| 42 | | | Repair action end | | NO | NO |
| 43 | | | IML data for non-blocking errors | | NO | NO |
| 44 | | | MOSS code data for problem isolation | | NO | NO |
| 50 | | | Remote console rejected | | 10 | 10 |
| 85 | | | Composite BER is handled for each BER | | NO | NO |
| 91 | | | <p>Level 1 interrupt MOSS down passed to control program by MOSS (MCC status reg 1, bit 3 giving a X'7E' input register bit 0.0 in the CCU).</p> <p>BER built by control program, and saved in the CRP. If this BER is in the diskette BER file, it means that it has been passed to the MOSS, when the MOSS was re-IMLed and set online.</p> <p>Reason for MOSS down might be found in the BER file itself, by looking at other BERs built by the MOSS, which triggered the MOSS inop bit in MCC status register.</p> | MOSS down | 03 | NO |
| B3 | | | CP/MOSS connection OUT mailbox command. Time out at level 3 in control program | MOSS down | 03 | NO |
| C1 | | | CP/MOSS connection OUT mailbox request error at level 4 in control program | MOSS down | 03 | NO |
| C2 | | | CP/MOSS connection IN mailbox command error at level 4 in control program | MOSS down | 03 | NO |

MOSS BER Type 01 ID 00 (Detailed BER Display)

BER format foM0: see page 11-99. MOSS microcode level 0 generates 3 displays. They consist in a fixed part and a part which displays the fields concerned by the type of error.

Fixed part

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:00 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                                <REF. CODE IN CHAR.> CCCCCCCC
MOSCHK:hhhh CPLLPL:hh CH:hh  NH:hh CHM:hh CHCV:hhhh CHIOP:hhhhhhhhh
MODULE:hhhhhhhhh DUMP:hh hh IA:hhhhhhhhh MS:hhhhhhhhh RS:hhhh
DIV:hhhh EIRV:hh IOIRV:hh PIRV:hh PSCI:hhhhhhhhh OP:hhhhhhhhh

REGS:hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh
      hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh hhhhhh

```

(Here are displayed the two lines of the changing part - group 1, 2 or 3- the groups are described below)

.....

Changing Part of MOSS BER Type 01 ID 00

- Errors about the PCAs (hex codes A01-A0F), the DFA or TOD (hex codes A8D, AAA, and Dxx), and MOSS BER Type 01 ID 80:

```

DFA:hh hh hh  TOD:hh
PCA1:hh hh hh hh hh PCA2:hh hh hh hh hh PCA3:hh hh hh hh hh

```

- Errors about the MCCU-A (hex codes A10 to A83):

```

MCCU A:hhhh hhhh hhhh hhhh hhhh hhhh  SWAD: 0000 (not used)

```

- Errors about the MCAD, without any register displayed (hex codes A84 to A8C, and AAB to CFF):

```

MCAD:hh hh hh hh hh hhhh hh hhhh hh
SNAP:hhhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh

```

MOSS BER Type 01 ID 00 - Field Description

| Table 11-10 (Page 1 of 2). MOSS BER Type 01 ID 00 Field Description | | |
|---|--|------------|
| Field Name | Meaning | Refer to |
| MOSS-CHECK | MOSS error code. | Page 11-41 |
| EIRV | Error interrupt request vector | Page 11-45 |
| DIV | Diagnostic information vector | Page 11-45 |
| IOIRV | I/O interrupt request vector | Page 11-45 |
| PIRV | Program interrupt request vector | Page 11-45 |
| CPLLPL | Current/last priority level | Page 11-45 |
| CM | Common mask | Page 11-45 |
| MM | Master mask | Page 11-45 |
| CHM | Channel mask | Page 11-45 |
| CHCV | Channel control vector | Page 11-46 |
| IA | Instruction address of the last level interrupted by level 0 | Page 11-46 |
| PSCI | Program status code indicator of the interrupted level | Page 11-46 |

Table 11-10 (Page 2 of 2). MOSS BER Type 01 ID 00 Field Description

| Field Name | Meaning | Refer to |
|------------|---|------------|
| LOPC | Last operation code. | Page 11-46 |
| MS | Main storage address (parity detected) | Page 11-50 |
| RS | Register storage address (parity detected in MSC) | |
| OP | Op code at error time | |
| SNAP | Snapshot dump | |
| STAT CNT | Error count for each adapter | |
| CHIO P | CHIO pointer register (current) | |
| DUMP | Dump/IML request | |
| EIRV1 | EIRV in case of MOSS level 0 re-entry. | |
| IOIRV1 | IOIRV in case of MOSS level 0 re-entry | |
| PIRV1 | PIRV in case of MOSS level 0 re-entry | |
| DIV1 | DIV in case of MOSS level 0 re-entry | |
| LOPC1 | Last operation code (level 0 re-entry) | Page 11-45 |
| PCA1 | PCA1 status registers | Page 11-47 |
| PCA2 | PCA2 status registers | Page 11-45 |
| PCA3 | PCA3 status registers | Page 11-45 |
| MCCU-A | MCCU-A status registers | Page 11-45 |
| SWAD | Not used | Page 11-49 |
| MCAD | MCAD status registers | Page 11-49 |
| DFA | DFA status registers | Page 11-49 |
| TOD | TOD status register | Page 11-50 |
| REGS | MOSS processor registers | Page 11-46 |

BER TYPE 01 ID 00 Error Code Description

The encoding of the MOSS-CHECK bytes is explained on page 11-31.

Table 11-11 (Page 1 of 4). MOSS BER Type 01 ID 00 Error Codes Description

| Field Name | Hexa Code | MOSS Check Code (Hexa) | Description |
|------------|-----------|------------------------|---|
| PCA1 | A01 | 0580 | Adapter down |
| | A02 | 0000 | PIO bus check (inbound parity) |
| | A03 | 0001 | PIO bus check (adapter not detected) |
| | A04 | 0010 | PIO time out (outbound address parity check) |
| | A05 | 0011 | PIO time out (outbound cmd/data parity check) |
| PCA2 | A06 | 0D80 | Adapter down |
| | A07 | 0800 | PIO bus check (inbound parity) |
| | A08 | 0801 | PIO bus check (adapter not detected) |
| | A09 | 0810 | PIO time out (outbound address parity check) |
| | A0A | 0811 | PIO time out (outbound cmd/data parity check) |
| PCA3 | A0B | 1580 | Adapter down |
| | A0C | 1000 | PIO bus check (inbound parity) |
| | A0D | 1001 | PIO bus check (adapter not detected) |
| | A0E | 1010 | PIO time out (outbound address parity check) |
| | A0F | 1011 | PIO time out (outbound cmd/data parity check) |

| Table 11-11 (Page 2 of 4). MOSS BER Type 01 ID 00 Error Codes Description | | | |
|---|-----------|------------------------|---|
| Field Name | Hexa Code | MOSS Check Code (Hexa) | Description |
| MCCU-A | A10 | 1D80 | Adapter down |
| | A11 | 1D81 | Adapter down (too many spurious error) |
| | A12 | 1C60 | Adapter check (bus counter parity) |
| | A13 | 1C61 | Adapter check (MIOC/CCU time out parity) |
| | A14 | 1A00 | CHIO bus check |
| | A15 | 1A10 | CHIO time out |
| | A16 | 1A20 | CHIO storage ECC (RS data parity during MS) |
| | A17 | 1A21 | CHIO storage ECC (multiple bits in DIV) |
| | A18 | 1A22 | CHIO storage ECC (no bit in DIV) |
| | A19 | 1A30 | CHIO exception address (MS data access) |
| | A1A | 1A31 | CHIO exception oper (CHCV invalid) |
| | A1B | 1A32 | CHIO exception register (CHP 0-7 not zero) |
| | A1C | 1A33 | CHIO exception spec (inv addr MS data access) |
| | A1D | 1A34 | CHIO exception (multiple bits in DIV) |
| | A1E | 1A35 | CHIO exception (no bit in DIV) |
| | A1F | 1A50 | CHIO internal check (cache parity) |
| | A20 | 1A51 | CHIO internal check (inv addr on CHP access) |
| | A21 | 1A52 | CHIO internal check (multiple bits in DIV) |
| | A22 | 1A60 | CHIO adapter check (step counter parity) |
| | A23 | 1A61 | CHIO adapter check (hw/burst counter parity) |
| | A24 | 1A62 | CHIO adapter check (CCU busy time out) |
| | A25 | 1A63 | CHIO adapter check (MIOC time out) |
| | A26 | 1A64 | CHIO adapter check (MIOC parity check in) |
| | A27 | 1A65 | CHIO adapter check (MIOC parity check out) |
| | A28 | 1A66 | CHIO adapter check (adapter failure) |
| | A29 | 1A67 | CHIO adapter check (multiple bits in STAT register) |
| | A2A | 1A68 | CHIO adapter check (no CHIO in progress in ACB) |
| | A2B | 1AA0 | CHIO (multiple bits in EIRV) |
| | A2C | 1AA1 | CHIO (no CHIO in progress in ACB) |
| | A2D | 1960 | Dev adapter check (step counter parity) |
| | A2E | 1961 | Dev adapter check (MIOC time out) |
| | A2F | 1962 | Dev adapter check (MIOC parity check in) |
| | A30 | 1963 | Dev adapter check (MIOC parity check out) |
| | A31 | 1964 | Dev adapter check (adapter failure) |
| | A32 | 1965 | Dev adapter check (multiple bits in STAT register) |
| | A33 | 1966 | Dev adapter check (no CAC running) |
| | A34 | 1800 | PIO bus check (inbound parity) |
| | A35 | 1801 | PIO bus check (adapter failure) |
| | A36 | 1802 | PIO bus check (adapter not detected) |
| | A37 | 1810 | PIO time out (invalid command) |
| | A38 | 1811 | PIO time out (outbound parity check) |
| | A39 | 1812 | PIO time out (adapter not detected) |
| | A3A | 1813 | PIO time out (adapter failure) |
| | A3B | 1814 | PIO time out (multiple bits in STAT register) |
| MCAD | A84 | 3580 | Adapter down |
| | A85 | 3000 | PIO bus check (inbound parity) |
| | A86 | 3001 | PIO bus check (adapter failure) |
| | A87 | 3002 | PIO bus check (adapter not detected) |
| | A88 | 3010 | PIO time out (invalid command) |
| | A89 | 3011 | PIO time out (outbound parity check) |
| | A8A | 3012 | PIO time out (adapter not detected) |
| | A8B | 3013 | PIO time out (adapter failure) |
| | A8C | 3013 | PIO time out (multiple bits in STAT register) |

Table 11-11 (Page 3 of 4). MOSS BER Type 01 ID 00 Error Codes Description

| Field Name | Hexa Code | MOSS Check Code (Hexa) | Description |
|------------------|-----------|------------------------|---|
| DFA | A8D | 3D80 | Adapter down |
| | A8E | 3A00 | CHIO bus check |
| | A8F | 3A10 | CHIO time out |
| | A90 | 3A20 | CHIO storage ECC (RS data parity during MS) |
| | A91 | 3A21 | CHIO storage ECC (multiple bits in DIV) |
| | A92 | 3A22 | CHIO storage ECC (no bit in DIV) |
| | A93 | 3A30 | CHIO exception (oper CHCV invalid) |
| | A94 | 3A31 | CHIO exception (register CHP 0-7 not zero) |
| | A95 | 3A32 | CHIO exception (spec inv addr MS data access) |
| | A96 | 3A33 | CHIO exception (address MS data access) |
| | A97 | 3A34 | CHIO exception (multiple bits in DIV) |
| | A98 | 3A35 | CHIO exception (no bit in DIV) |
| | A99 | 3A50 | CHIO internal check (cache parity) |
| | A9A | 3A51 | CHIO internal check (inv addr on CHP access) |
| | A9B | 3A52 | CHIO internal check (multiple bits in DIV) |
| | A9C | 3AA0 | CHIO multiple bits in EIRV |
| | A9D | 3AA1 | CHIO no CHIO in progress in ACB |
| | A9E | 3800 | PIO bus check (inbound parity) |
| | A9F | 3801 | PIO bus check (adapter failure) |
| | AA0 | 3802 | PIO bus check (adapter not detected) |
| TOD | AA1 | 3810 | PIO time out (invalid command) |
| | AA2 | 3811 | PIO time out (outbound address parity check) |
| | AA3 | 3812 | PIO time out (outbound cmd/data parity check) |
| | AA4 | 3813 | PIO time out (adapter failure) |
| | AA5 | 3814 | PIO time out (multiple bits in STAT register) |
| PCC | AA6 | 4580 | Adapter down |
| | AA7 | 4000 | PIO bus check (inbound parity) |
| | AA8 | 4001 | PIO bus check (adapter not detected) |
| | AA9 | 4010 | PIO time out (outbound address parity check) |
| UC bus | AAA | 4011 | PIO time out (outbound cmd/data parity check) |
| | AAB | 4B80 | Adapter down |
| | AAC | 4B00 | MMIO write error |
| | AAD | 4B10 | MMIO time out |
| | AAE | 4B30 | MMIO exception (address) |
| Register storage | AAF | 4B20 | MMIO read error |
| | AB0 | 4BA0 | MMIO not authorized on this level |
| Storage | AB1 | 5580 | Adapter down |
| Loop | AB2 | 5820 | PIO storage ECC (MPC data parity) |
| | AB3 | 5821 | PIO storage ECC (MSC data parity) |
| | AB4 | 5822 | PIO storage ECC (unresolved) |
| | AB5 | 5C20 | Storage ECC (during PSV swap) |
| Storage | AB6 | 6220 | CHIO storage ECC (data parity) |
| | AB7 | 6520 | Storage ECC (data parity) |
| | AB8 | 6521 | Storage ECC (I-fetch parity) |
| MOSS code | AB9 | 6DA0 | Detected |
| Diag | ABA | 7590 | Pgm error (IO address not authorized) |
| Level0 | ABB | 7C90 | Pgm error (POR/start unresolved) |
| Level0 | ABC | 8590 | Pgm error (WHO invalid in CPRET) |
| | ABD | 8591 | Pgm error (WHO invalid in PPRET) |
| | ABE | 8592 | Pgm error (WHO invalid in XPRET) |
| | ABF | 8593 | Pgm error (program state unexpected) |
| | AC0 | 8594 | Pgm error (invalid adapter ID in CHGH0BUS) |
| | AC1 | 8595 | Pgm error (RAM processor state unexpected) |
| | AC2 | 8596 | Pgm error (ROS processor state unexpected) |
| | AC3 | 8597 | Pgm error (CALL stack full) |
| | AC4 | 8598 | Pgm error (RET stack empty) |
| | AC5 | 8599 | Pgm error (error code not in BER table) |
| | AC6 | 859A | Pgm error (MOSS IMLed routine before IML) |

| Table 11-11 (Page 4 of 4). MOSS BER Type 01 ID 00 Error Codes Description | | | |
|---|-----------|------------------------|--|
| Field Name | Hexa Code | MOSS Check Code (Hexa) | Description |
| Unexpected | AC7 | 8A40 | CHIO |
| | AC8 | 8DA0 | Interrupt level 0 |
| | AC9 | 8D60 | IOIRV interrupt level 0 |
| | ACA | 8800 | PIO bus check (no last level) |
| | ACB | 8801 | PIO bus check (not IO instruction) |
| | ACC | 8802 | PIO bus check (on level 2) |
| | ACD | 8803 | PIO bus check (unexpected on level 6) |
| | ACE | 8810 | PIO time out (no last level) |
| | ACF | 8811 | PIO time out (not IO instruction) |
| | AD0 | 8812 | PIO time out (on level 2) |
| | AD1 | 8813 | PIO time out (unexpected on level 6) |
| | AD2 | 8C70 | PIRV program request |
| Unresolved | AD3 | 9530 | Exception address (I fetch) |
| | AD4 | 9531 | Exception address (MS data access) |
| | AD5 | 9532 | Exception fixed point overflow |
| | AD6 | 9533 | Exception (inv addr on non MS access) |
| | AD7 | 9534 | Exception (multiple bits in DIV) |
| | AD8 | 9535 | Exception (multiple bits in EIRV) |
| | AD9 | 9536 | Exception oper (invalid opcode) |
| | ADA | 9537 | Exception register (precision) |
| | ADB | 9538 | Exception spec (inv addr on I fetch) |
| | ADC | 9539 | Exception spec (inv addr on MS data access) |
| | ADD | 953A | Exception spec (inv addr on non GPR access) |
| | ADE | 953B | Exception spec (inv execution of ki) |
| | ADF | 953C | Exception spec (PSV bits 40-44-47 not zero) |
| | AE0 | 9550 | Internal check (cache register parity check) |
| | AE1 | 9551 | Internal check (inv address on GPR access) |
| | AE2 | 9552 | Internal check (inv address on PSV swap) |
| | AE3 | 9553 | Internal check (multiple bits in DIV) |
| | AE4 | 9554 | Internal check (multiple bits in EIRV) |
| | AE5 | 9520 | Storage ECC (multiple bits in DIV) |
| | AE6 | 9521 | Storage ECC (multiple bits in EIRV) |
| | AE7 | 9522 | Storage ECC (no bit in DIV) |
| Specific | Cxx | 76xx | PIRV (abend request) |
| | Dxx | 3Cxx | Disk adapter return code |

BER Type 01 ID 00 - Fields Details

Some of the following fields may not appear on the ELD detail display, but they are part of the BER and they are listed as they appear in the BER file. See the section 'BER Formats on Disk' page 11-99

| Table 11-12 (Page 1 of 6). BER Type 01 ID 00 Field Details | | |
|--|--|---|
| Field Name | Bit Pattern | Description |
| DIV (byte 1) | | Diagnostic information |
| | 00 1 1 0000 | Sector must be zero Error occurred during main store operation. Error occurred during a register backing store operation DMA identification must be zero |
| DIV (byte 2) | | Sector specification |
| | 1 1 1 1 1 1 1 1 1 | Exception memory subsystem detected an invalid address Error occurred during a PSV swap operation Operation exception: attempt to execute an invalid instruction A register precision occurred (result > 24 bits) Address exception: address > 'X'7FFFFF' or wrapped to zero Error occurred during an instruction fetch Fixed point overflow External error loaded in EIRV/DIV |
| EIRV | | Error interrupt request vector |
| | 1 1 1 1 1 1 1 1 0 | I/O control check Time out check Storage data/ECC check Exception (addr,op,spec.) Channel I/O check Internal control check Instruction address modifier (IA points to the beginning of the instruction) Unused (must be zero) |
| IOIRV | | I/O interrupt request vector |
| | 1 1 0 1 1 1 1 00 | MCC adapter check MCC high level interrupt or 100 ms timer interrupt Power control interrupt request MCA interrupt request MCC low level interrupt DFA interrupt request Unused (must be zero) |
| PIRV | | Programmed interrupt request vector |
| | 1 1 1 1 1 1 1 1 1 | MOSS error level 0 handler MOSS error level 0 process Power control interrupt request MOSS MCA level 3 handler MOSS MAC level 4 handler MOSS DFA level 5 handler MOSS Supervisor level 6 and task scheduler MOSS tasks level 7 programs |
| CPLLPL | | Current/last priority level |

| Table 11-12 (Page 2 of 6). BER Type 01 ID 00 Field Details | | |
|--|---|---|
| Field Name | Bit Pattern | Description |
| | 0 xxx 0 xxx | Unused (must be zero) Current priority level (000 to 111) Unused (must be zero) Last priority level (000 to 111) |
| CM | | Common mask interrupt vector |
| | 1 1 1 1 1 1 1 1 | Level 0 enabled Level 1 enabled Level 2 enabled Level 3 enabled Level 4 enabled Level 5 enabled Level 6 enabled Level 7 enabled |
| MM | | Master mask interrupt vector |
| | 0000 000 1 | Unused (must be zero) Enabled |
| CHM | | Channel mask interrupt vector |
| | 0000 000. 1 | Unused (must be zero) Enabled |
| CHCV | | Channel control vector |
| CHCV (byte 2) | 0000 0 x x x x x x x x x x x | Unused (must be zero) Channel pointer number 0 = CPR within set 12-15 1 = CPR within set 8-11 Indirect operation 0 = Mode determined by bit 1.1 1 = Indirect mode 0 = Short address 1 = Long address 0 = Write 1 = Read 0 = Indirect mode (Must be 0 if bit 0.6 is 1) 1 = Direct mode CHCV pointer number 0 = CHCV (0-6) used 1 = CHCV (0-6) not used |
| IA | | Interrupted address |
| byte 1 bytes 2-4 | 0000 0000 | Unused (must be zero) Address |
| PSCI | | Program status code indicator register space |
| byte 1 byte 2 byte 3 byte 4 | 0000 0000 0000 0 . . 0 1 . 1 1 . 1 1 xx xxxx 1 1 xx xxxx | Unused (must be zero) Unused (must be zero) Restricted address branch mode (64 K domain only) Master mode PIO and reg indirect Z indicator H indicator Secondary set number C indicator V indicator Primary set number |
| LOPC 1 | | Last operation code address |
| bytes 1-2 bytes 3-4 | hh hh hh hh | 1st part of the address 2nd part of the address |

Table 11-12 (Page 3 of 6). BER Type 01 ID 00 Field Details

| Field Name | Bit Pattern | Description |
|---------------------------------------|--|--|
| REGS | | Registers of interrupted level |
| 28-51 Prim. set 52-75 Sec. set | xxxxxx xxxxxx xxxxxx xxxxxx | |
| Dump | | MOSS dump/IML info |
| IML informa- tion (IML request) | 1 1 00 xxxx | Dump requested Re-IML requested Unused (must be zero) Re-IML count |
| DUMP status | | MOSS dump file status |
| | 0000 0000 1 | File free Enabled |
| MCCU A | | MCCU A status register 0 |
| byte 1 | 1 1 1 1 1 1 1 1 byte 2 | MOSS inoperative Step/bus counter parity MIOC/CCU counter parity HW/burst counter parity CCU busy time out MIOC time out MIOC parity check in MIOC parity check out Invalid PIO Cmd UC bus parity check Unused MIOC busy CHIO halt Equipment check Enable interrupt level 0 Interrupt level 0 (read only) |
| MCCU A | | MCCU A status register 1 |
| byte 3 | xxxx x 1 xx | Unused Enable CCU HLIR Unused |
| byte 4 | xxxx x 1 1 1 1 | Unused CCU HLIR Enable all interrupts Interrupt level 1 |
| MCCU A | | MCCU A status register 4 |
| byte 5 | xxx 1 1 1 xx | Unused Enable cycle steal end Enable CCU LLIR Enable CSP IOC1 interrupt Unused |
| byte 6 | 1 xx 1 1 1 x 1 | Programm wait Unused Cycle steal end CCU LLIR CSP IOC1 interrupt Unused Interrupt level 4 |
| MCCU A | | MCCU A MMOD register |
| byte 7 | x 1 1 1 1 1 1 1 | Unused Step 0 Step 1 Freeze MIOC direct oper mode MIOC write mode (CHIO) MIOC read mode (CHIO) DREG full |

| Table 11-12 (Page 4 of 6). BER Type 01 ID 00 Field Details | | |
|--|---|--|
| Field Name | Bit Pattern | Description |
| byte 8 | x 1 1 1 1 1 1 1 1 | Reserved for diagnostics Parity prediction diag 1 Parity prediction diag 0 MIOC diag 2 MIOC diag 1 MIOC diag 0 MOSS diag 2 MOSS diag 1 MOSS diag 0 |
| byte 9 | xxxx xxxx | MCCU A count register |
| byte 10 | xxxx xxxx | MCCU A count register |
| byte 11 | xxxx xxxx | CHCV register |
| byte 12 | xxxx xxxx | CHCV register |
| MCAD (byte 1) | | MCAD INTP1 register |
| | 1 1 xx x 1 1 1 | Invalid PIO command UC bus parity check Unused Equipment check Enable interrupt level 1 Interrupt level 1 |
| MCAD (byte 2) | | MCAD EINTP1 register |
| | 1 1 xx 1 1 xx | Enable timer Enable CADS 5-8 HLIR Unused 100 ms timer CADS 5-8 HLIR Unused |
| MCAD (byte 3) | | MCAD INTP4 register |
| | 1 1 xx 1 1 x 1 | Enable fault flags Enable CADS 5-8 LLIR Unused Fault flags CADS 5-8 LLIR Unused Interrupt level 4 |
| MCAD (byte 4) | | MCAD sense fault flags |
| | xx 1 1 xxxx | Unused Fault ENA/REST 5-6 Fault ENA/REST 7-8 Unused |
| MCAD (byte 5) | | MCAD diagnostics register |
| | 1 xxx xxxx | All CAs disabled Unused Force error |
| MCAD (byte 6) | | MCAD sense CA enable |
| | xxxx 1 1 1 1 | Unused CA 5 enabled CA 6 enabled CA 7 enabled CA 8 enabled |
| MCAD (byte 7) | | Unused |
| MCAD (byte 8) | | MCAD CAMPOR register |
| | xxxx 1 . . . | Unused CADS 5-8 nohold (reset by 'reset adapter' cmd) |

Table 11-12 (Page 5 of 6). BER Type 01 ID 00 Field Details

| Field Name | Bit Pattern | Description |
|---------------------|----------------|--|
| |X.. | Unused |
| |1. | CADS 5-8 MOSS POR (reset by 'reset adapter' cmd) |
| |1 | Unused |
| MCAD | | MCAD ENCA register |
| bytes 9-10 | xxxx xxxx | Each bit enables a CA from 5 to 8 |
| | xxxx xxxx | |
| MCAD | | MCAD CARST register |
| bytes 11-12 | xxxx xxxx | Each bit resets a CA from 5 to 8 |
| | xxxx xxxx | |
| PCA1, PCA2, or PCA3 | | PCA1, PCA2, or PCA3 basic status register |
| byte 1 | 1... .. | Input request |
| | .1... .. | Output request |
| | ..1... .. | DCE interrupt |
| | ...1... .. | Timer interrupt |
| | 1... .. | Exception |
| |1... .. | Equipment check |
| |1... .. | Enable |
| |1 | Interrupt request |
| byte 2 | | PCA1, 2, or 3 A status register |
| | 1... .. | Overrun |
| | .1... .. | Underrun |
| | ..1... .. | Receive clock running |
| | ...1... .. | SDLC invalid sequence |
| | 1... .. | SDLC flag |
| |1... .. | Invalid character |
| |1... .. | Break byte detected |
| |1 | Adapter in sync |
| byte 3 | | PCA A control register |
| | 1... .. | Receive mode |
| | .1... .. | Transmit mode |
| | ..1... .. | Inhibit zero insert |
| | ...x x... .. | Mode select |
| |xx... .. | Code length |
| |1 | NRZI/break |
| byte 4 | | PCA M status register |
| | 1... .. | Data set ready |
| | .1... .. | Clear to send |
| | ..1... .. | Receive line signal det |
| | ...1... .. | Ring indicator |
| | 1... .. | Data set ready transit |
| |0... .. | Unused (must be zero) |
| |1... .. | RLSD transition |
| |1 | Clear to send transition |
| byte 5 | | PCA M control register |
| | 1... .. | Data terminal ready |
| | .1... .. | Request to send |
| | ..1... .. | Wrap |
| | ...1... .. | Test |
| | 1... .. | Select stand by |
| |1... .. | Select half-speed |
| |1... .. | New sync |
| |1 | DCE interrupt disable |
| DFA (Byte 1) | | DFA basic status register |
| | xx... .. | Attachment status: |
| | | <ul style="list-style-type: none"> • 0 0 = idle • 0 1 = busy attention loaded • 1 0 = busy reset • 1 1 = busy CHIO |
| | ..1... .. | UC bus parity check |

| Table 11-12 (Page 6 of 6). BER Type 01 ID 00 Field Details | | |
|--|---|---|
| Field Name | Bit Pattern | Description |
| | ... 1 11..1.1 | Invalid PIO command CHIO halt Equipment check Enable Interrupt request |
| DFA (byte 2) | | DFA attention register |
| | 1111 11..00 | Command control block Command specification Sense summary block Data request bit Drive select high bit Drive select low bit Unused (must be zero) |
| DFA (byte 3) | | DFA interrupt status register |
| | 1111 11..1.1 | Termination error Invalid command Command reject Parity error Drive select high bit Drive select low bit ERP invoked Equipment check |
| TOD | | TOD status register |
| | 0000 01..1.1 | Unused (must be zero) Equipment check Enable Interrupt request |
| SNAP | | Snapshot dump (abend) |
| byte 1 | 000x xxxx | Length of snapshot |
| bytes 2-27 | xxxx xxxx | Dump |

MOSS BER Type 01 ID 01

Format foM1: see page 11-99. MOSS microcode level 1 generates the following BER:

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh  DATE:dd/dd  TIME:dd:dd  TYPE:01  ID:01
LVL1 < error description line >          <REFER.CODE IN CHAR.> CCCCCCCC
WHO-WHAT:bbbbbbb -CHECK:hh -ABEND:hh
MCCUA REGS:hhhh hhhh hhhh hhhh hhhh hhhh CMSA:bbbbbbb
X75:hhhhhh X76:hhhhhh LSR:hhhhhh CP-ABEND:hhhh TA:hhhh STATUS:bbbbbbb

MCCUB REGS:hhhh hhhh hhhh hhhh hhhh hhhh CMSA:bbbbbbb
X75:hhhhhh X76:hhhhhh LSR:hhhhhh CP-ABEND:hhhh TA:hhhh STATUS:bbbbbbb

MCAD  REGS:hh hh hh hh hh hhhh hh hhhh hhhh
CCU:hh IOC:hh NUM:hh

===>

F1:END F2:MENUE2 F3:ALARM F4:SUNHARY F5:LIST F7:PREVIOUS F8:NEXT

```

Note: All values except the fields 'WHO' and 'WHAT' are in hexadecimal notation (X'0' to X'F').

MOSS BER Type 01 ID 01 - Field Description

Table 11-13. MOSS BER Type 01 ID 01 Field Description

| Field Name | Meaning | Refer to |
|------------|--|------------|
| WHO | In binary (first part of error explanation) | Page 11-52 |
| WHAT | In binary (second part of error explanation) | Page 11-52 |
| ABEND | Level 1 abend codes: . 4E = Permanent HLIR . 4F = Too many spurious errors . FF = No abend code | |
| CMSA | CCU to MOSS status register A (X'11') | |
| CHECK | Error | Page 11-52 |
| STATUS | Level 1 status | Page 11-52 |
| X75 | X'75' - AIO CSCW byte X, byte 0, byte 1 (only used with error code 07, program request IPL) | Page 2-24 |
| X76 | X'76' - IOC level 1 interrupt request (only used with error code 07, program request IPL) | Page 2-24 |
| TA | TA register | |
| LSR | Local store register | Page 2-20 |
| MCCUA | MOSS to CCU A registers | Page 11-47 |
| MCCUB | Not used (all fields not significant) | - |
| MCAD | MOSS to CA registers | Page 11-48 |
| CCU | CCU selected for CA • hh = 01: CCUA • hh = 02: CCUB | |
| IOC | IOC selected for CA • hh = 01: IOC1 • hh = 02: IOC2 | |
| NUM | CA number | |

MOSS BER Type 01 ID 01 - Field Details

Some of the following fields may not appear on the ELD detail display, but they are part of the BER and they are listed as they appear in the BER file. See the section 'BER Formats on Disk' page 11-99

| Table 11-14. MOSS BER Type 01 ID 01 Field Details | | |
|---|--------------------------|----------------------------------|
| Field Name | Bit pattern or Hex value | Meaning |
| WHO | 0000 | Gives the origin of the error |
| | 0001 | Unresolved |
| | 0010 | CCU A |
| | 0011 | Unused |
| | 0100 | CADS1 |
| | 0101 | CADS2 |
| | 0110 | Timer |
| | 0111 | MCAD |
| | 1000 | Unused |
| | 1001 | CCU A power OFF |
| WHAT | 0000 | Unused |
| | 0001 | Under diags |
| | 0010 | CCU hardcheck |
| | 0011 | Program IPL request |
| | 0100 | Host IPL request |
| | 0101 | Multiple IPL request |
| | 0110 | I/O error alert |
| | 0111 | CCU stop |
| | 1000 | IOC operation error |
| | 1001 | Address exception |
| | 1010 | Operation check |
| | 1011 | CADS MIOH error |
| | 1100 | Timer interrupt |
| | 1101 | Unresolved |
| | 1110 | CCU power OFF |
| Check | 00 | No error on level 1 |
| | 01 | MOSS OK |
| | 02 | Adapter OK |
| | 03 | No error during CHIO |
| | 04 | Unable to reset HLIR |
| | 05 | CCU not IPLed |
| | 06 | IPL already in progress |
| | 07 | Unable to read CCU information |
| | 08 | Unable to read adapter registers |
| | 09 | Unable to read CCU registers |
| | 0A | Multiple bit in CMSA |
| | 0B | No bit in CMSA |
| | 0C | CAC not running |
| | 0D | Unexpected interrupt |
| | 0E | Unresolved interrupt |
| | 0F | No interrupt in AMAC card |
| | 10 | No interrupt in IOIRV |
| | 11 | No action for MOSS level 1 |
| Status | 20 | 218-219 Count |
| | 40 | 197-213 SCB |
| | 80 | CCUA/B X'76' |
| | | CCUA/B CMSA |
| | | MCCUA/B status Register 1 |

Note: For the list of suspected FRUs, refer to the MIP.

MOSS BER Type 01 ID 02

Format foM2: see page 11-100. The MOSS microcode generates the following BERs when an error occurs during CCU/MOSS exchanges.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh  DATE:dd/dd  TIME:dd:dd  TYPE:01  ID:02
MIOC < error description line >          <REFER.CODE IN CHAR.> CCCCCCCC
MOSS-CHECK:hh  ADNO:hh  CMD:hh  PIRV:hh  IOIRV:hh  CMSB:hh  STAC:hh
CAC-RC:hh  STAT1:hhhh  STAT4:hhhh  ADDR:hhhhhhhh
PCW:hhhhhhhh hhhhhhhh hhhhhhhh  FLAGS:hh  CA:hh

```

===>

F1:END F2:MENU2 F3:ALARM F4:SUNMARY F5:LIST F7:PREVIOUS F8:NEXT

MOSS BER Type 01 ID 02 - Field Description

Table 11-15. MOSS BER Type 01 ID 02 Field Description

| Field Name | Meaning | Refer to |
|------------|---|-------------|
| CMD | Logical command (used in the error description line) | Page 11-54 |
| MOSS-CHECK | Error code (used in the error description line) | Page 11-54 |
| CA | Channel adapter number (1 to 16) | |
| ADNO | <ul style="list-style-type: none"> CA adapter number, or Adapter CCU number (05 for CCUA, 06 for CCUB) or Switch CCU adapter on IOC1 (40). See page /LPGHRV/ Switch CCU adapter on IOC2 (C0). See page /LPGHRV/ | |
| PIRV | Programmed interrupt request vector | Page 11-45 |
| IOIRV | I/O interrupt request vector | Page 11-45 |
| CMSB | CCU to MOSS status register B (X'06') | |
| CAC-RC | CAC return code or error code | Page 11-54 |
| STAT1 | MCC status reg 1 | Page 11-47 |
| STAT4 | MCC status reg 2 | Page 11-47 |
| ADDR | PCW list address. | For PE only |
| FLAGS | Adapter control block flags | page 11-55 |
| STAC | CCU to MOSS C register | |
| PCW | Program control word. Command sent by the CCU. | For PE only |

MOSS BER Type 01 ID 02 - Field Details

Some of the following fields may not appear on the ELD detail display, but they are part of the BER and they are listed as they appear in the BER file. See the section 'BER Formats on Disk' page 11-99

| Table 11-16 (Page 1 of 2). MOSS BER Type 01 ID 02 Field Details | | |
|---|--------------------------|--|
| Field Name | Bit Pattern or Hex Value | Meaning |
| CMD | 01 | Logical command |
| | 02 | Read B register error impossible |
| | 04 | MIOC request |
| | 08 | Interrupt level 4 processing |
| | 20 | Display registers |
| | 21 | Control program buffer reading |
| | 40 | Control program buffer writing |
| | 41 | Out mailbox request |
| | 41 | Out mailbox response |
| | 80 | In mailbox request |
| | 81 | In mailbox response |
| | 90 | CHIO command |
| MOSS-CHECK | 01 | Error codes |
| | 02 | LSSD string select error |
| | 04 | Invalid PCW request |
| | 04 | Invalid out-mailbox request |
| | 08 | In-mailbox time out response |
| | 10 | Unexpected in-mailbox response from CP |
| | 20 | Unresolved interrupt |
| | 21 | C-clock stop |
| | 22 | Invalid interrupt level 4 |
| | 40 | CCU busy bit ON |
| | 41 | Devices busy bit ON |
| | 42 | CCU power down |
| | 80 | Physical error reported |
| | 86 | CHIO asynchronous error |
| | 87 | CHIO synchronous error |
| | 88 | CHIO time out |
| CAC-RC | 00 | CAC return code or error code |
| | 01 | Return code OK |
| | 01 | Adapter down |
| | 02 | LSSD string ID error |
| | 03 | LSSD residual count |
| | 04 | CCU busy bit ON |
| | 05 | Device busy bit ON |
| | 06 | IOC error |
| | 07 | Op check |
| | 08 | Exception |
| | 09 | Scanner error 1 |
| | 0A | CHIO abort |
| | 0B | Unexpected interrupt |
| | 0C | I/O interrupt cannot be reset |
| | 20 | CADS to MOSS level 1 |
| | 40 | Abend request |
| | 80 | CCU power down |
| | 81 | Invalid PCW |
| | FF | Abort |

Table 11-16 (Page 2 of 2). MOSS BER Type 01 ID 02 Field Details

| Field Name | Bit Pattern or Hex Value | Meaning |
|------------|--------------------------|-------------------------------|
| FLAGS | 80 | Adapter control block flags |
| | 40 | Adapter down |
| | 20 | Adapter checkpoint retry |
| | 10 | Adapter Xparent retry thresh. |
| | 08 | Time out on adapter |
| | 04 | Mail box in request |
| | 02 | Timer set for mail box in |
| | 01 | Moss Off line Cmd in mail box |
| | 81 | Moss On line Cmd in mail box |
| | 82 | CHIO operation in process |
| | 83 | Timer set for CHIO ope |
| | | CHIO retry has been done |

MOSS BER Type 01 ID 03

Format foM3: see page 11-100. The MOSS microcode generates the following BERs when an error occurs in the disk/diskette drive or disk drive adapter.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh  DATE:dd/dd  TIME:dd:dd  TYPE:01  ID:03
< error description line >          <REFER.CODE IN CHAR.> CCCCCCCC
MOSS-CHECK:hh  DEV:hh  FILE:hhhhhhhh  CHD:hh  REQ:hh
F:hh  CNT:hh  ARC:hh  BSTAT:hhhh  ADDR:hhhhhhhh
BCLE:hhhhhhhh  hhhhhhhh  SSB:hhhhhhhh  hhhhhhhh  hhhhhhhh

```

===>

F1:END F2:MENUE2 F3:ALARM F4:SUNMARY F5:LIST F7:PREVIOUS F8:NEXT

MOSS BER Type 01 ID 03 - Field Description

| Table 11-17. MOSS BER Type 01 ID 03 Field Description | | |
|---|---|------------|
| Field Name | Meaning | Refer to |
| CMD | Logical command | Page 11-57 |
| MOSS-CHECK | MOSS-CHECK error codes | Page 11-57 |
| DEV | Device in error | Page 11-57 |
| REQ | Function request code (reserved) | Page 11-57 |
| ARC | Adapter return code | Page 11-59 |
| BSTAT | Basic status register | Page 11-61 |
| F | Flag indicator, last BCLE executed (internal to MOSS) | Page 11-57 |
| CMD | Last BCLE command | Page 11-59 |
| CNT | BCLE-related byte count | Page 11-57 |
| ADDR | Last BCLE-related address | |
| BCLE | Last executed buffer control list element (CAC-related information) | Page 11-57 |
| SSB | Sense summary block adapter status | Page 11-58 |
| FILE | File name or load module (in EBCDIC) | |

MOSS BER Type 01 ID 03 - Field Details

Some of the following fields may not appear on the ELD detail display, but they are part of the BER and they are listed as they appear in the BER file. See the section 'BER Formats on Disk' page 11-99

| Table 11-18 (Page 1 of 2). MOSS BER Type 01 ID 03 Field Details | | |
|---|--------------------------|--|
| Field Name | Bit Pattern or Hex Value | Meaning |
| MOSS-CHECK | 01 | Bad track but no alternate track assigned. |
| | 02 | Alternate track successful assigned. |
| | 03 | Alternate track assignment failure. |
| | 04 | Disk or diskette down |
| CMD | 00 | Logical command |
| | 01 | Open |
| | 02 | Write |
| | 03 | Read |
| | 04 | Close |
| | 05 | Load |
| DEV | 01 | Direct execute |
| | 01 | Adapter failure for disk operations |
| | 02 | Adapter failure for diskette operations |
| | 03 | Disk drive |
| | 04 | Diskette drive |
| | 05 | Adapter or disk drive |
| | 06 | Adapter or diskette drive |
| REQ | 07 | Diskette media (floppy disk) |
| | 00 | Function request code |
| | 05 | Execute |
| | 07 | Read operational statistics |
| | 25 | No-op |
| | 83 | Read SCA state |
| | A3 | Open adapter |
| | AB | Open SCA |
| F (flag) | EB | Close SCA |
| | | Terminate (adapter) |
| | | CAC error record |
| BCLE byte 0 | 1 | Error code indicator |
| | . . 1 | Last record indicator |
| BCLE byte 1 | hh | Flag: hh = 00: No command chaining hh = 01: Command chaining |
| BCLE byte 2 | hh | Command field |
| BCLE bytes 3-4 | hh | Count field |
| BCLE bytes 5-7 | hh | Data address |

| Table 11-18 (Page 2 of 2). MOSS BER Type 01 ID 03 Field Details | | |
|---|--|--|
| Field Name | Bit Pattern or Hex Value | Meaning |
| SSB byte 0 | 1 1 1 1 1 x x 1 | Drive status Drive ready Seek end (HDD only) Write protected (FDD only) Write fault (HDD only) Disk change Unused Track 0 |
| SSB byte 1 | x 1 1 1 1 1 1 1 | SSB error status byte 0 CRC/ECC error x = 0: Data x = 1: ID CRC/ECC error Address mark not found Bad track Wrong cylinder Control address mark Format error ID not found |
| SSB byte 2 | x 1 1 1 xxxx | SSB error status byte 1 Unused Data adapter error Retry corrected Defective sector Unused |
| SSB bytes 3-6 | | Last data adapter ID field processed |
| SSB bytes 7-8 | | Cylinder and head location |
| SSB byte 9 | | Number of sectors corrected by ECC |
| SSB byte 10 | | Number of retries |
| SSB byte 11 | | Processor state at reset time |

Notes:

1. All values are in hexadecimal notation (X'0' to X'F'), except for the file name or module name (FILE), which is in EBCDIC.
2. The CAC will make several retries (up to 10). The retry count contains the number of retries before the disk operation was successfully terminated.
 - If RCNT is lower than 10, the last I/O operation was successful. The error was intermittent.
 - If RCNT = 10, the decision (recovery or program action) is taken by the MOSS application that activated the diskette operation. The error is permanent (solid).

Adapter Return Codes (ARC)

The error description line is built from the contents of the ARC.

| Table 11-19. MOSS BER Type 01 ID 03 Adapter Return Codes | | |
|--|--|---|
| Field Name | Hex Value | Meaning |
| ARC | | EXCEPTION/SUCCESS CLASS |
| | 22 23 30 31 | SCA ready (exception) SCA not ready (exception) SCA not ready (no error) Control record found |
| ARC | | ERROR / NOT SUCCESSFUL CLASS |
| | | SEQUENCE ERRORS |
| | 01 02 05 06 08 09 0A 0D 0E | Adapter busy-attention FRB busy. Adapter busy-CHIO Adapter busy-reset SCA 1 not open SCA 2 not open Adapter not open SCA 1 already open SCA 2 already open |
| | | PARAMETER PROBLEMS |
| | 11 12 13 | FRB program check BCL program check Invalid PIO command |
| | | HARDWARE AND EQUIPMENT CHECKS |
| | 20 28 | Undetermined equipment check (hardware error in adapter) Seek check |
| | | DATA TRANSMISSION PROBLEMS |
| | 30 32 34 37 38 39 3A 3B 3C 3E | Termination error with no specific error Sect buffer parity error Cylinder overrun HALT during a CHIO operation I/O bus parity error CCB with no active CSB Invalid command in CCB or SSB ERP invoked by thresher Internal parity error Record not found |
| | | PREEMPTIVE REQUEST CLASS |
| | 0B 0C | Preemptive request complete Preemptive request rejected |
| | | LOPERATOR INTERVENTION REQUIRED |
| | 62 6F | SCA not ready (error) Invalid diskette format |
| | | I/O MACHINE CHECK |
| | 76 F6 | PIO MCK (non-recursive) PIO MCK (recursive) |

MOSS BER Type 01 ID 04

Format foM4: see page 11-100. The MOSS microcode generates the following BER when an error occurs on the console or its adapter cards:

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh  DATE:dd/dd  TIME:dd:dd  TYPE:01  ID:04
DPLY< error description line >          <REFER.CODE IN CHAR.> CCCCCCCC
MOSS-CHECK:hh  CID:hh  BSTAT:hh  ASTAT:hh  CSTAT:hhhh  MSTAT:hh

===>

F1:END F2:MENUE2 F3:ALARM F4:SUNHARY F5:LIST F7:PREVIOUS F8:NEXT

```

MOSS BER Type 01 ID 04 - Field Description

| Table 11-20. MOSS BER Type 01 ID 04 Field Description | | |
|---|--------------------------------|------------|
| Field Name | Meaning | Refer to |
| ASTAT | Adapter error status register | Page 11-60 |
| BSTAT | CCA card basic status register | Page 11-61 |
| CMD | Logical command | Page 11-61 |
| CSTAT | Console status | Page 11-61 |
| MOSS-CHECK | Error code | Page 11-62 |
| MSTAT | Modem status register | Page 11-62 |

Note: All values are in hexadecimal notation (X'0' to X'F').

MOSS BER Type 01 ID 04 - Field Details

Some of the following fields may not appear on the ELD detail display, but they are part of the BER and they are listed as they appear in the BER file. See the section 'BER Formats on Disk' page 11-99

| Table 11-21 (Page 1 of 3). MOSS BER Type 01 ID 04 Field Details | | |
|---|-------------------------------|--|
| Field Name | Bit Number or Hex Value | Meaning |
| ASTAT | | MOSS-CHECK = X'0A' Adapter exception status |
| | X | Read/open halted |
| | . X | XMIT/RCV contention occurred |
| | . . X | BREAK character received |
| | . . . X xxxx | Unused |

Table 11-21 (Page 2 of 3). MOSS BER Type 01 ID 04 Field Details

| Field Name | Bit Number or Hex Value | Meaning |
|------------|-------------------------------|--|
| ASTAT | | MOSS-CHECK = X'0C' or '8C' |
| | X | Parity error on receive data |
| | . X | DCE error |
| | . . X | RCV line at space |
| | . . . X | RCV data buffer too short (overflow) |
| | X . . . | Unused |
| | X . . | Machine check error |
| | X . | RCV text time out |
| ASTAT | | MOSS-CHECK = X'8A' |
| | | Adapter exception status |
| | X | Parity error on received data |
| | . X | DCE error |
| | . . X | RCV line at space |
| | . . . X | RCV data line too short |
| | X . . . | Unused |
| | X . . | Machine check error |
| BSTAT | | CCA basic status register bit assignment |
| | 01 | Adapter interrupt pending |
| | 02 | Adapter enabled |
| | 04 | MCPC interrupt |
| | 08 | Exception interrupt |
| | 10 | Timer interrupt |
| | 20 | Modem interrupt |
| | 40 | CSR - output request |
| CMD | 80 | CSR - input request |
| | | Logical commands |
| | 08 | Lock keyboard |
| | 10 | Close adapter |
| | 20 | Read/write adapter |
| | 40 | Write adapter |
| CSTAT | 80 | Open CCA adapter |
| | 81 | Open console |
| | | Console status ERROR: X'40', 'C0' |
| | Bits | |
| | 0-0 | Parity bit |
| | 0-1 | Not bit 2 |
| | 0-2 | Communication buffer overrun |
| | 0-3 | Line parity error detected |
| | 0-4 | Command error detected |
| | 0-5 | Unused |
| | 0-6 | Keyboard locked |
| | 0-7 | Unused |
| | 1-0 | Parity bit |
| | 1-1 | Not bit 2 |
| | 1-2 | Block mode |
| | 1-3 | Half-duplex mode |
| | 1-4 | Unused |
| | 1-5 | Unused |
| | 1-6 | Program mode |
| | 1-7 | Unused |

| Table 11-21 (Page 3 of 3). MOSS BER Type 01 ID 04 Field Details | | |
|---|-------------------------------|---|
| Field Name | Bit Number or Hex Value | Meaning |
| MOSS-CHECK codes | 0A | CAC detected exception (local) ASTAT = adapter exception |
| | 0C | CAC detected error (local) ASTAT = adapter error |
| | 40 | Console error (local) |
| | 40 | Console error (remote) |
| | 8A | CAC detected exception ASTAT = adapter exception status (remote) |
| | 8C | CAC detected error (remote) ASTAT = adapter error |
| MSTAT | | CCA modem status register bit assignment |
| | 01 | CTS transition |
| | 02 | RLSD transitions |
| | 04 | Reserved |
| | 08 | DSR transition |
| | 10 | Ring indicator |
| | 20 | Received line signal detector (RLSD) |
| | 40 | Clear to send (CTS) |
| | 80 | Data set ready (DSR) |

Note: The correct console status is X'4030'.

MOSS BER Type 01 ID 05

Format foM5: see page 11-100 The MOSS microcode generates the following BERs when an error occurs on a scanner or on the MOSS/scanner connections.

```

                                ELD DETAIL
    < error description line >      <REFER.CODE IN CHAR.> CCCCCCCC
SEL#:hhhh FLAG:xx DATE:dd/dd TIME:dd:dd TYPE:01 ID:05
    < Error description line>
<MOSS-CHECK:04 ADDR:hh>=Unexpected interrupt received
<MOSS-CHECK:01 ADDR:hh CSCHK:hhhh>
<MOSS-CHECK:02 ADDR:hh MBST:hhhh>
<MOSS-CHECK:05 ADDR:hh TD:hhhh>

```

===>

F1:END F2:MENUE2 F3:ALARM F4:SUNHARY F5:LIST F7:PREVIOUS F8:NEXT

Table 11-22. MOSS BER Type 01 ID 05 MOSS-CHECK Details

| MOSS Check | Meaning |
|------------|-----------------------------------|
| 01 | Scanner failure during IPL |
| 02 | Mailbox contains the error status |
| 04 | Unexpected interrupt received |
| 05 | Scanner is inoperative |

MOSS BER Type 01 ID 05: Format foM5, see page 11-100. The MOSS microcode generates the following BER when an error occurs on MOSS or during IOH operations.

```

                                ELD DETAIL
    < error description line >      <REFER.CODE IN CHAR.> CCCCCCCC
SEL#:hhhh FLAG:xx DATE:dd/dd TIME:dd:dd TYPE:01 ID:05
<MOSS-CHECK:hh ADDR:hh X76:hhhhhh STATUS:hhhh>

```

===>

F1:END F2:MENUE2 F3:ALARM F4:SUNHARY F5:LIST F7:PREVIOUS F8:NEXT

Table 11-23. MOSS BER Type 01 ID 05 MOSS-CHECK Details

| MOSS Check | Detected by LVL | Meaning | Status |
|------------|-----------------|-----------------------|---------------------|
| 08 | 1 | Get error status IOH | Type 1, 2, or 3 |
| 10 | 4 | NO information | No status available |
| 20 | 4 | Mailbox status in BER | Command completion |
| 40 | 4 | Get error status IOH | Type 1, 2, or 3 |
| 80 | 1 | | No status available |

MOSS BER Type 01 ID 05: Format foM5a, see page 11-101.

ELD DETAIL

SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:01 ID:05
 < Error description line> <REFER.CODE IN CHAR.> CCCCCCCC

MOSS-CHECK:FO ADDR:hh DUIMP:hh hh ← **A**

hhhh hhhh hhhh hhhhhhhh hhhh

▲ ▲ ▲ ▲ ▲

B **C** **D** **E** **F**

hhhh hhhh hhhh hhhhhhhh hhhh

▲ ▲ ▲ ▲ ▲

G **H** **I** **J** **K**

====>

F1:END F2:MENUE2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

The field indicated by the letter **A** contains:

- The **DUMP error code** in the first byte
- The **IML error code** in the second byte, as follows:

| Table 11-24. 'A' Field Details | | |
|--------------------------------|-------|--|
| Field Name | Value | Meaning |
| Dump error code | 00 | Dump available |
| | 01 | Dump not taken (dump file already full) |
| | 02 | Dump not available (diskette error) |
| | 03 | Dump not available (hardware error MIOC/TSS) |
| | FF | Dump not taken |
| IML error code | 01 | Re-IML not successful |
| | 02 | Connect not successful, CP not answering (re-IML OK) |
| | 03 | Connect not successful (MIOC operation failed) |
| | 04 | Connect not successful, rejected by CP |
| | 05 | Threshold (no dump and no re-IML) |
| | 10 | Re-IML successful |
| | FF | Re-IML successful |

Note: All other combinations of byte values for the DUMP field are not valid
 The other fields indicated by the letters **B** to **K** have the following meaning:

| Table 11-25. 'B' to 'K' Field Details | |
|---------------------------------------|--|
| Field ID | Meaning |
| B | Last in TA for dump |
| C | Last out TA for dump |
| D | Last TD for dump |
| E | Last MB for dump. This field contains the first four bytes |
| F | Last disk ECB for dump |
| G | Last in TA for re-IML |
| H | Last out TA for re-IML |
| I | Last TD for re-IML |
| J | Last MB for re-IML. This field contains the first four bytes |
| K | Last disk ECB for re-IML |

Note: Invalid fields contain all 'F's.

MOSS BER Type 01 ID 05 - Field Description

| Table 11-26. MOSS BER Type 01 ID 05 Field Description | | |
|---|--|------------------|
| Field Name | Meaning | Refer to |
| ADDR | Scanner address as shown in "Scanner Addressing" (Hex) | MIP chapter 5 |
| X76 | X'76' (bytes X, 0, and 1 of field X76 on screen) or MOSS command completion (bytes 0 and 1; X not used) | Page 2-24 |
| STATUS | Error status, or mailbox status, depending on the error code | Page 11-63 |
| TD | Last command (DB0 and DB1 at TD time) | Chapter 8 |
| MBST | Mailbox status | Chapter 8 |
| CSCHK | Scanner status | -- |
| ADAPTER ID | IOC bus ID | -- |

Notes:

1. All values are in hexadecimal notation (X'0' to X'F').
2. For details of scanner/MOSS communication, see Chapter 8.

MOSS BER Type 01 ID 06 (Error 01 or 02)

BER format foM7: see page 11-101. The MOSS microcode generates the following BER when an error occurs in the BER file outside controller initialization.

The error description line contains information such as the CP abend code, the scanner address, or the number of BERs lost.

```
ELD DETAIL
SEL#:hhhh  FLAG:hh  DATE:dd/dd  TIME:dd:dd  TYPE:01  ID:06
APPL< error description line >          <REFER.CODE IN CHAR.> CCCCCCCC
MOSS-CHECK:hh
```

===>

F1:END F2:MENUE2 F3:ALARII F4:SUNMARY F5:LIST F7:PREVIOUS F8:NEXT

Note: For software information on BERs originated by NCP/PEP, refer to the associated product documentation.

MOSS BER Type 01 ID 06 (Error 03 or 06)

This BER corresponds to one of the following cases:

- IPL check
- IPL complete + errors

For 'IPL complete with errors' the BER is always 'normal' (in opposition to 'composite BERs').

For 'IPL check', the BER logged is a 'composite BER' for physical errors and a normal one for logical errors.

BER format foM6: see page 11-101, IPL error.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:06
APPL< error description line >          <REFER.CODE III CHAR.> CCCCCCCC
CCU:hh  REQ:hh  LVL1-REQ:hh  F2:hhhh  X71:hhhhhh  X72:hhhhhh  F1:hh
MIS:hh  hh  hh  hh  hh  hh  hh  hh  hh  hh  hh  hh  hh  hh  hh  hh  hh  hh
LA:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
   hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
   hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
   hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
CA:hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh
hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh
hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh hhhh hhhh hh

===>

F1:END F2:MENUE2 F3:ALARM F4:SUIHARY F5:LIST F7:PREVIOUS F8:NEXT

```

MOSS BER Type 01 ID 06 (Error 04)

BER format foM7a: see page 11-101. The MOSS microcode generates the following BER when an error occurs on scanner IML check failure at the end of IPL.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:06
APPL< error description line >          <REFER.CODE IN CHAR.> CCCCCCCC
MOSS-CHECK:hh
LA ADDR:hh

===>

F1:END F2:MENUE2 F3:ALARM F4:SUIHARY F5:LIST F7:PREVIOUS F8:NEXT

```

Note: For software information on BERs originated by NCP/PEP, refer to the associated product documentation.

MOSS BER Type 01 ID 06 - Field Details

Some of the following fields may not appear on the ELD detail display, but they are part of the BER and they are listed as they appear in the BER file. See the section 'BER Formats on Disk' page 11-99

According to the error type, the MIS field contents differs:

Error 03 MIS is made from the fields DISK, DISK2, IPL mode and IPLCHECK of the following table.

Error 06 As described in the field MIS (11-70) of the following table.

| Table 11-27 (Page 1 of 4). MOSS BER Type 01 ID 06 Field Details | | |
|---|---|---|
| Field Name | Bit Pattern or Hex Value | Meaning |
| MOSS-CHECK | 03 06 | MOSS error code Complete with errors Check |
| IPL info | 01 | IPL |
| CCU | 01 | Always set to 01 |
| REQ | 01 02 03 04 05 06 07 | IPL on power-ON reset CCU + scanners IPL req from KBD Unused Unused Unused Unused IPL is requested by the level 1 |
| LVL1-REQ | 02 03 04 07 | ID of CCU IPL request CCU hardcheck Program request IPL Channel request IPL CCU power drop |
| STATUS | 00 01 10 x x x1000 x | System status MOSS only MOSS disconnected System running MOSS has reached the MOSS init part 2, then normal MCPC must be used Unused Scanner not IMLed, alert sent by loop detection task IPL drive: hard disk " " : diskette When ON, no local console available |
| Abend code | xxxx xxxx xxxx xxxx | IPL abend code |
| LA byte 1 | x x x x x x x x | 32 blocks (1 per CSP) of 4 bytes, displayed as 8 hexadecimal characters LPTSS found present in CDF TRA found present in the CDF Adapter power ON Scanner/TRA is presently the scanner selected TIC1 found present in CDF TIC2 found present in CDF LA under control of the CP Scanner successfully IMLed |

Chapter 11. Error Logging 11-69

| Table 11-27 (Page 3 of 4). MOSS BER Type 01 ID 06 Field Details | | |
|---|---|--|
| Field Name | Bit Pattern or Hex Value | Meaning |
| DISK2 | x x x x x x xx | 5 bytes, same allocation as 'halfwords' above Roll in/out file LSR file CCU dump file First dump record file Last dump record file Control program load module file Unused |
| F2 byte 1 | x x x x x x x x | Bad branch trace buffer length Bad check record pool Bad control program interface table level 1 on CA during CA monitoring X71 register is not readable CLDP did a pseudoabend Loading scanner table failed (phase 3) Control info length error: MB error |
| F2 byte 2 | x x x x x x x x x x | IPL from disk length error: MB error IPL complete with port swap errors LSSD dump incorrect Adapter dump requested, not performed (bad return from CHGCDLA access function) Error during save on disk Error during load from disk Error during reset active load mode Error during dump on disk (phase 4) Error during roll-in roll-out |
| X71 | | X71 register |
| X72 | | X72 register |
| IPL mode | x x xx x xxx | IPL mode (IPLMODE) x = 0 <==> Operator x = 1 <==> Automatic Customer / maintenance (MTMENU) x = 0 <==> Customer x = 1 <==> Maintenance Unused Standalone dump status x = 0 Not requested or failed x = 1 Successfully performed Unused |
| CCU | 01 01 01 | Always set to 01 |
| MIS | | Miscellaneous. Following byte description is only for error 06 (IPL check). For error 03 MIS is made from the fields DISK, DISK2, IPL mode and IPLCHECK of this table. |
| Bytes 1-2 | | ERROR REFERENCE CODE |
| Byte 3 | x x x x x x x x | Valid field indicators IAR is valid SAR is valid LAR is valid IN70 is valid IN76 is valid IN7D is valid IN7E is valid IN7X is valid |
| Bytes 4-6 | | IAR |

Table 11-27 (Page 4 of 4). MOSS BER Type 01 ID 06 Field Details

| Field Name | Bit Pattern or Hex Value | Meaning |
|-------------|--|--|
| Bytes 7-9 | | SAR |
| Bytes 10-12 | | LAR |
| Bytes 13-14 | | INPUT X'70' |
| Bytes 15-16 | | INPUT X'76' |
| Byte 17 | X...X..X..X | IN76 IOC1 STATE LATCH (See page 2-32) Time out Bus IN parity AIO PIO |
| Byte 18 | | Unused |
| Bytes 19-20 | | INPUT X'7D' |
| Bytes 21-22 | | INPUT X'7E' |
| Bytes 23-24 | | INPUT X'7E' extension |
| F1 | X... .. .X...X.X X...X..X..X | Disk IPL facility failed PCA of local console not available PCA of remote console not available PCA of RSF console not available MCAD detected KO by MOSS diags Unused MCCUA detected KO by MOSS diags Unused |
| RC from CDF | xxxx xxxx xxxx xxxx | CDF return code from CDF access function |
| CADS byte 1 | X... .. .X...X.X X..X..X..X | 6 bytes per CA (16 CAs) MIOH failure Bad return from CHGCDCA Power OFF Verify data error Bad checkout result Chaining error Mismatch about TPS between CDF and HW Unused |
| Byte 2 | X... .. .X...X.X X...X..XX | Init error Bad return from MCAD adapter CA not found in 'CONNECTED' status during phase 1B <i>Chaining not performed due to 2 errors on the bus</i> MCAD error when enabling MCAD error when disabling Unused |
| Bytes 3-4 | xxxx xxxx xxxx xxxx | CADS checkout result |
| Byte 5 | 0000 0001 | CCU (Always set to 01) |
| Byte 6 | | Unused |
| IPLCHECK | X... .. .X...X.X X...X..X..X | Error 03 only (IPL complete with errors) Unexpected IPL option Unexpected CCU option Unexpected/undefined F key No CCU under IPL, IPL started No CCU specified for BER Unused Unexpected display request Unused |

MOSS BER Type 01 ID 06 (Errors 05/08 Ext 05/07)

BER format foM9: see page 11-102, MOSS-check: 05 EXT: 05/07 The MOSS microcode generates the following BER when a CCU hardcheck occurs. The BER fields contain information fetched from the LSSD strings and saved when the error occurs on CCU hardcheck. Then a re-IPL is started.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh  DATE:dd/dd  TIME:dd:dd  TYPE:01  ID:06
APPL< error description line >          <REFER.CODE IN CHAR.> CCCCCCCC
CCU:hh  DUHP:hh

===>

F1:END F2:MENUE2 F3:ALARII F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

```

BER format foM9a: MOSS-check 08 EXT 05, see page 11-102. The MOSS microcode generates the following BER when a CCU hardcheck occurs. The BER fields contain information fetched from the LSSD strings saved when the error occurs on CCU hardcheck. Then a re-IPL is started.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh  DATE:dd/dd  TIME:dd:dd  TYPE:01  ID:06
'3745 RE-IPL STARTED FOR CCU HARDCHECK'.  <REFER.CODE IN CHAR.> CCCCCCCC
CCU:hh
IAR:hhhhhh  LAR:hhhhhh  SAR:hhhhhh
X70:hhhhhh  X76:hhhhhh  X7D:hhhhhh  X7E:hhhhhh
HDCK:hhhh

===>

F1:END F2:MENUE2 F3:ALARII F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

```

MOSS BER Type 01 ID 06 (Errors 05/08 Ext 05/07) - Field Details

| Table 11-28. MOSS BER Type 01 ID 06 (Errors 05 or 08) Field Details | | |
|---|--------------------------------------|--|
| Field Name | Bit Pattern or Hex Value | Meaning |
| CCU | 01 | CCU (always set to 01) |
| NCP abend | xxxx xxxx xxxx xxxx | NCP abend code for alert. See page 11-37 |
| Dump status | 01 02 | Stand-alone dump status Not requested or failed Successfully performed |
| HDCK | Byte 1 xxxx xxx X | Unused Unused Level 1 error reentry |

MOSS BER Type 01 ID 06 (Error 07)

BER format foM7: see page 11-101.

```

                                ELD DETAIL
APPL< error description line >      <REFER.CODE IN CHAR.> CCCCCCCC
SEL#:hhhh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:06
MOSS OFFLINE
MOSS-CHECK:hh

====>

F1:END F2:MENU2 F3:ALARH F4:SUHMARY F5:LIST F7:PREVIOUS F8:NEXT

```

MOSS-CHECK: hh = 07: MOSS is offline.

MOSS BER Type 01 ID 06 (Error 08 Ext 07)

BER format foM19: see page 11-103. The MOSS microcode generates the following BER on CLDP abend and relatedre_IPL request.

```

                                ELD DETAIL
APPL< error description line >      <REFER.CODE IN CHAR.> CCCCCCCC
SEL#:hhhh  FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:06

CCU:hh

====>

F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

```

MOSS BER Type 01 ID 06 (Error 09)

BER format foM10: see page 11-101. The MOSS microcode generates the following BER when CLDP abends (code X'F1B'). This BER does not follow the 'composite BER' mechanism. The X72 field contains the CLDP abend code

```

                                ELD DETAIL
SEL#:hhh FLAG:hh  DATE:hh/hh TIME:hh:hh  TYPE:01  ID:06
APPL< error description line >      <REFER.CODE IN CHAR.> CCCCCCCC
CCU:hh  IAR:hhhhhh X71:hhhhhh X72:hhhhhh
WKR1:hhhhhh WKR2:hhhhhh WKR3:hhhhhh WKR4:hhhhhh WKR5:hhhhhh WKR6:hhhhhh
WKR7:hhhhhh
X7E:hhhh X7D:hhhh X76:hhhh
X6E:hhhh X6D:hhhh X50:hhhh X51:hhhh X52:hhhh X60:hhhh
LA:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
   hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh

====>

F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

```


MOSS BER 01 ID 06 (Error 09) - Field Description

| Table 11-29. MOSS BER Type 01 ID 06 (Error 09) Field Description | | |
|--|-----------------------------|----------|
| Field Name | Meaning | Refer to |
| WKR3 | For product engineering use | -- |
| WKR4 | For product engineering use | idem |
| WKR5 | For product engineering use | idem |
| WKR6 | For product engineering use | idem |
| WKR7 | For product engineering use | idem |
| LA | LA error status | idem |

Note: The other registers are described in chapter 2 of this manual.

MOSS BER Type 01 ID 06 (Err 09) - Field Details

Some of the following fields may not appear on the ELD detail display, but they are part of the BER and they are listed as they appear in the BER file. See the section 'BER Formats on Disk' page 11-99

| Table 11-30. MOSS BER Type 01 ID 06 (Err 09) Field Details | | |
|--|---|---|
| Field Name | Bit Pattern or Hex Value | Meaning |
| X71 bytes 0-1 | xxxx xxxx xxxx xxxx | CA or Link address according to IOC bus format |
| X71 byte x | xx x x x x x x x | Unused CLDPabend RPO detected Load Dump CA IPL Link IPL |
| X72 | | Contains the CLDP codes. |

MOSS BER Type 01 ID 07

Format foM29: see page 11-105. The MOSS microcode generates the following BERs when an error occurs in the MOSS/TRSS interface.

```

                                ELD DETAIL
SEL#:hhhh  FLAG 00 DATE:04/29 TIME:23:45  TYPE:01 ID:07
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC
ERROR:hh  TRA ADDR:hhhh  X76:hhhhhh
GET COMMAND COMPLETION:hhhh
MOSS  ERROR STATUS:hhhh
LEVEL1 ERROR STATUS:hhhh
LEVEL2 ERROR STATUS:
TIC1:hhhh  TIC2:hhhh
TIC CTL REGISTER
bbbbbbbb bbbbbbbb

```

==>

F1:END F2:MENU2 F3:ALARM F4:SUNMARY F5:LIST F7:PREVIOUS F8:NEXT

Table 11-31. MOSS BER Type 01 ID 07 Field Details

| Field Name | Bit Pattern or Hex Value | Meaning |
|-------------------------------------|--|---|
| ERROR | hh = 04 hh = 08 hh = 40 hh = 80 | Error description No interrupt from TRM Error detected on level 1 Error detected on level 4 Error detected on level 1 |
| TRA ADDR | hhhh | TRA address, see page 3-42. |
| GET COMMAND COMPLETION | hhhh | |
| MOSS ERROR STATUS | hhhh | See page 6-24 |
| LEVEL1 ERROR STATUS | hhhh | See page 6-20 |
| LEVEL2 ERROR STATUS TIC1 TIC2 | hhhh | See page 6-22 |
| TIC CTL REGISTER | bbbbbbbb bbbbbbbb | |

Format foM29a: see page 11-105. The MOSS microcode generates the following BERs when an error occurs on the MOSS/TRSS interface.


```
ELD DETAIL
SEL#:hhhh  FLAG 00 DATE:04/29 TIME:23:45 TYPE:01 ID:07
<ERROR DESCRIPTION> <REFER.CODE IN CHAR.> CCCCCCCC
ERROR:hh  TRA INPUT ADDR:hhhh  TRA OUTPUT ADDR:hhhh
TIC NBR:hh
2K BLOCK:  INITIAL    REQUESTED  FINAL
           hhhh      hhhh      hhhh
STOP COMMAND CNT:hh

====>

F1:END F2:MENU2 F3:ALARH F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```

| Table 11-32. MOSS BER Type 01 ID 07 Field Details | | |
|---|--------------------------------|--|
| Field Name | Bit Pattern or Hex Value | Meaning |
| ERROR | 00 FE | Error description TIC dump completed TIC set stg failure |
| TRA INPUT ADDR | hhhh | TRA input address from PCW |
| TRA OUTPUT ADDR | hhhh | TRA output address from PCW |
| TIC NBR | hh | TRP number |
| 2K BLOC: INITIAL REQUESTED FINAL | hhhh hhhh hhhh | Initial block number Requested block number Final block number |
| STOP COMMAND CNT | hh | Stop command loop count |

Format foM29b: see page 11-105. The MOSS microcode generates the following BERs when an error occurs on the MOSS/TRSS interface.

```
ELD DETAIL
SEL#:hhhh  FLAG 00 DATE:04/29 TIME:23:45 TYPE:01 ID:07
<ERROR DESCRIPTION> <REFER.CODE IN CHAR.> CCCCCCCC
ERROR:FF ERROR-EXT:hh TRA NBR:hh TIC NBR:hh
CCU:hh  TRA ADDR:hhhh

====>

F1:END F2:MENU2 F3:ALARH F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```


Table 11-33. MOSS BER Type 01 ID 07 Field Details

| Field Name | Bit Pattern or Hex Value | Meaning |
|--------------------|--------------------------------|---|
| ERROR extension | 01 02 03 04 00 | Error description Dump file full Disk error Hardware error Select TRA TIC error When the dump is available |
| TRA NBR | hh | TRA number (01-04) |
| TIC NBR | hh | TIC number (01-02) |
| CCU | hh | CCU 01 = CCUA 02 = CCUB |
| TRA ADDR | hhhh | TRA address, see page 3-42. |

MOSS BER Type 01 ID 08

Format foM16: see page 11-103. The MOSS microcode generates the following BERs when an error occurs on the MOSS/CA interface.

```

new BER not yet entered
                                ELD DETAIL
SEL#:hhhh  FLAG 00 DATE:dd/dd TIME:hh:hh  TYPE:01 ID:08
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC
DUMP:hh TRACE:hh CA:hh CCU:hh

```

===>

F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

MOSS BER Type 01 ID 08 - Field Details

Table 11-34. MOSS BER Type 01 ID 08 Field Details

| Field Name | Hex Value | Meaning |
|------------|-----------|---|
| DUMP | 00 | Dump available |
| | 01 | Dump full |
| | 02 | Disk error |
| | 03 | Threshold. |
| | | Maximum number of auto-dump (maximum value 5) |
| TRACE | 00 | Restart trace successful |
| | 01 | Restart trace failed |
| CA | xx | CA addresses, from 5 to 8 |
| CCU | 01 | CCU (always set to 01) |

MOSS BER Type 01 IDs 10 and 11

Format foM14: see page 11-103.

```

                                ELD DETAIL
SEL#:hhhh DATE:dd/dd TIME:dd:dd TYPE:01 ID:hh
< error description line >          <REFER.CODE IN CHAR.> CCCCCCCC
IORB:hhhh hhhh hhhh hhhh hh hh hh hh hhhhhhhh CCCCCCCC
      hhhhhhhh hhhhhhhh hhhhhhhh hhhh hhhh hhhh hhhh
PLIST:hhhhhhhh hhhh hhhh hhhhhhhh hhhhhhhh hhhhhhhh
OC1:CCCCCCCC OC2:CCCCCCCC CCUF:CCCCCCCC CCUB:CCCCCCCC

==>

F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

```

MOSS BER Type 01 IDs 12, 13, and 14

Format foM15: see page 11-103.

```

                                ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:01 ID:hh
< error description line >          <REFER.CODE IN CHAR.> CCCCCCCC
IORB:hhhh hhhh hhhh hhhh hh hh hh hh hhhhhhhh CCCCCCCC
      hhhhhhhh hhhhhhhh hhhhhhhh hhhh hhhh hhhh hhhh
OC1:CCCCCCCC OC2:CCCCCCCC CCUF:CCCCCCCC CCUB:CCCCCCCC

==>

F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

```

The above screen shows the details of a MOSS BER ID 12

The IORB field pattern changes according to the BER ID:

ID 13

```

      hhhh hhhh hhhhhhhh hh hh hh hh hhhhhhhh
      hhhhhhhh hhhhhhhh hhhh hhhh hh

```

ID 14

```

      hhhh hhhh hhhhhhhh hh hh hh hh hhhhhhhh

```


MOSS BER Type 01 ID 15

Format foM30: see page 11-105. MOSS-CP interface (mailbox).

```

                                ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:01 ID:15
CP< error description line >          <REFER.CODE IN CHAR.> CCCCCCCC
IORB: hhhh hhhh hhhhhhhh hh hh hh hh hhhhhhhh
MRB: hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
PLIST: hhhhhhhh hhhhhhhh hhhhhhhh
BLK4: hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh

OC1:CCCCCCCC OC2:CCCCCCCC CCUF:CCCCCCCC CCUB:CCCCCCCC

===>

F1:END F2:MENUE2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

```

MOSS BER Type 01 IDs 16 and 1A to 1D

Format foM18: see page 11-103, MOSS-CP interface.

```

                                ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:01 ID:16
CP< error description line >          <REFER.CODE IN CHAR.> CCCCCCCC

IORB: hhhh hhhh hhhhhhhh hh hh hh hh hhhhhhhh.
PLIST: hhhhhhhh hhhhhhhh hhhhhhhh

OC1:CCCCCCCC OC2:CCCCCCCC CCUF:CCCCCCCC CCUB:CCCCCCCC

===>

F1:END F2:MENUE2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

```

Note: PLIST displayed only with BER ID 16.

MOSS BER Type 01 IDs 10 to 16 and 1A to 1D - Field Description

| Table 11-35. MOSS BER Type 01 ID 10 to 16 and 1A to 1D Field Description | | |
|--|---|----------|
| Field Name | Meaning | Refer to |
| IORB | Disk input/output request block | (*) |
| MRB | Mailbox info | (*) |
| PLIST | Disk request parameter list | (*) |
| BLK4 | 4K block information | (*) |
| OC1 | Operating control transient area overlay name 8 bytes | |
| OC2 | Operating control transient area module name 8 bytes | |
| CCUF | CCU function transient area module name 8 bytes | |
| CCUB | Unused | |

(*) For information on BERs originated by NCP/PEP, refer to the associated product documentation.

F1:END F2:MENU2 F3:ALARM F4:SUNRISE F5:LIST F7:PREVIOUS F8:NEXT

Chapter 11. Error Logging 11-81

MOSS BER Type 01 ID 19

BER format foM12: see page 11-102. BER for MOSS IML complete with error.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:19
< error description line >          <REFER.CODE III CHAR.> CCCCCCCC
F:hh
PANEL NEW REQ:hh  FCN:hh  SERV:hh
PANEL OLD REQ:hh  FCN:hh  SERV:hh
HEXCODE:hhh hhh hhh hhh hhh hhh hhh hhh hhh hhh hhh hhh hhh hhh hhh
CDF-RC:hhhh
ECBDISK:hhhh MIOC  CCUA:hhhh  CCUB:hhhh
MB CCUA  CID:hh  STAT:hhhh
MB CCUB  CID:hh  STAT:hhhh

===>

F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

```

MOSS BER Type 01 ID 19 - Field Description

| Table 11-37. MOSS BER Type 01 ID 19 Field Description | | |
|---|--|-------------|
| Field Name | Meaning | Refer to |
| CCUA | CCU function transient area module name 8 bytes | |
| CCUB | Unused | |
| CDF-RC | CDF return code. Normally 0000, otherwise PE only | For PE only |
| CMD | Logical Cmd in the request function | Page 11-83 |
| ECBDISK | ECB on disk/diskette operation | Page 11-83 |
| F | Error code. Information is collected in case hexadecimal code cannot be displayed on the panel. | Page 11-86 |
| MIOC | MIOC ECB for operation on CCUA/B | Page 11-84 |
| CCUA/B | | |
| PANEL | Hexa code sequence, from the oldest to the more recent one | |
| HEXCODE | <ul style="list-style-type: none"> Bytes 1 through 16 (hex 0 thru F): mailbox request zone (in/out) (first line on the screen) Bytes 17 through 32 (hex 10 thru 1F): mailbox response zone (IN/OUT) (second line of the screen) | Page 8-13 |
| MB | | |
| PANEL NEW | Panel hex code | |
| PANEL OLD | Previous hex code | |
| REQ | Same as field 'ORIGI' in BER 01-20 | Page 11-86 |
| FCN | Selected function on control panel | Page 9-3 |
| SEV | Service mode | Page 9-3 |
| STAT | Mail box status | Page 11-85 |

MOSS BER Type 01 ID 20

Format foM21: see page 11-103. This BER corresponds to a general IPL successfully performed. Whatever the IPL trigger item is (control panel, KB/D, automatic, scheduled), this BER is logged at IPL completion.

This BER is logged for availability measurement purpose.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:20
CP< error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
ORIGI:hh  FUNCTION:hh  SERV:hh  CCU:hh
STATUS:bbbbbbb REQ:hh  LVLE-REQ:bbbbbbb
MODE:hh  DEFAULT:hh  CONF:hh

====>

F1:END F2:MENUE2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

```

MOSS BER Type 01 IDs 19 and 20 - Field Details

Some of the following fields may not appear on the ELD detail display, but they are part of the BER and they are listed as they appear in the BER file. See the section 'BER Formats on Disk' page 11-99

Table 11-38 (Page 1 of 5). MOSS BER Type 01 IDs 19 and 20 Field Details

| Field Name | Bit Pattern or Hex Value | Meaning |
|------------|--------------------------------|-------------------------------------|
| BCLE | 00 | Buffer control list element |
| | 01 | Enable request |
| | 03 | Sense adapter request |
| | 04 | Read text/HDR request |
| | 06 | BID preparation request |
| | 0C | Write SOH...ETX |
| | 10 | Write BID request |
| | 14 | Write EOT request |
| | 16 | Disable request |
| | 1E | Write STX...ETX |
| | 3C | Write STX...ETB |
| | 80 | Write disconnected request |
| CMD | | Halt request flag |
| | | Logical Cmd in the request function |
| | 80 | Open |
| | 40 | Send |
| | 20 | Send/Receive |
| | 10 | Open on PSN |
| | 08 | Close |
| | 04 | Not used |
| ECBDISK | 02 | Receive for file Xfer |
| | 01 | Line survey |
| ECBDISK | | ECB on disk/diskette operation |

| Table 11-38 (Page 2 of 5). MOSS BER Type 01 IDs 19 and 20 Field Details | | |
|---|--------------------------------|--------------------------------|
| Field Name | Bit Pattern or Hex Value | Meaning |
| Byte 1 | 00 | Normal operation |
| | 80 | CC time out |
| | 40 | CC posted |
| | 20 | CC started |
| | 10 | CC BER |
| | 08 | CC warning |
| | 04 | CC adapter down |
| | 02 | CC request rejected |
| | 01 | CC I/O exception |
| Byte 2 | 00 | Normal operation |
| | 21 | End of file |
| | 22 | Begin file |
| | 23 | File empty |
| | 25 | Diskette change |
| | 26 | Diskette not ready |
| | 41 | End of file (open output) |
| | 42 | Begin of file |
| | 43 | File empty |
| | 44 | File already open |
| | 45 | File not opened |
| | 46 | File not found |
| | 47 | Load module not found |
| | 48 | Invalid open type (open) |
| | 49 | File opened in input |
| | 4A | File opened in output |
| | 4B | Invalid load module type |
| | 4C | CRC/ECC error on data |
| | 4D | Bad track (format) |
| | 4E | Format error |
| | 4F | CRC/ECC error on ID |
| | 51 | Invalid parameter list |
| | 52 | Invalid parameter list |
| | 53 | Invalid parameter list |
| | 54 | Invalid parameter list |
| | 56 | Invalid parameter list |
| | 61 | I/O halted |
| | 62 | I/O halted |
| | 63 | I/O halted |
| | 64 | File not available |
| | 68 | File not available |
| | 6B | Write fault (hard disk) |
| | 6C | File not available |
| | 6D | Power failure on start/stop |
| | 6E | Drive not ready |
| | 6F | Write protect (FDD) |
| | 71 | Write request truncated |
| | 72 | Read request truncated |
| | 74 | Physical Rec. Log. deleted |
| | 78 | Indetermined control record |
| MIOC CCUA | | MIOC ECB for operation on CCUA |
| Byte 1 | 00 | Normal operation |
| | 80 | CC time out |
| | 40 | CC posted |
| | 20 | CC started |
| | 10 | CC BER |
| | 08 | CC warning |
| | 04 | CC adapter down |
| | 02 | CC request rejected |
| | 01 | CC I/O exception |

Table 11-38 (Page 3 of 5). MOSS BER Type 01 IDs 19 and 20 Field Details

| Field Name | Bit Pattern or Hex Value | Meaning |
|------------|--|--|
| Byte 2 | 40 41 42 43 61 62 63 64 65 66 67 68 69 6A 6B 6C 6D 6E 6F | No MCCU ID specified Invalid logical request Invalid PCW CHIO running Request truncated CCU busy bit On Abort IOC error NCP time out Mail box lock LSSD error residual count String select error No LB allowed, CCU IPL Buffer empty MIOC/adapter busy bit On MOSS address exception MOSS OP check CHIO asynchronous error CHIO time out |
| STAT | | Mail box status |
| Byte 1 | 80 40 20 10 08 04 02 01 | Accepted Rejected Not used Not used Keep buffer Free buffer Not used Not used |
| Byte 2 | 80 40 20 10 08 04 02 01 | Buffer not available Function not supported Invalid command Moss down or Off line Invalid parameters Fallback in process Not used Enable to queue SNA req. |
| MOSS-CHECK | 01 | IPL complete without errors |

| Table 11-38 (Page 4 of 5). MOSS BER Type 01 IDs 19 and 20 Field Details | | |
|---|--|--|
| Field Name | Bit Pattern or Hex Value | Meaning |
| ORIGI | x x x x x 1 . . | Origin of MOSS code activation Machine power-ON Machine reset MOSS power-ON MOSS reset MOSS automatic re-IML Forced origin The origin of the ROS code activation is forced to the previous activation (for example: machine power ON, machine reset, MOSS power ON) NOTE: this bit is meaningful when a MOSS reset occurs before all the MOSS control blocks initialization by the IML processor. x . Forced selection. This bit is set ON when the MOSS diags cannot get from the MPWL valid information defining the origin, the function or service mode. In such a case default values are Origin: MOSS power ON Function: MOSS IML from disk Service: CE mode x Unused |
| F | x x xx xxx x | Error code IML not successful Alarm indicator A0 has to be generated Unused Operation with power failed for: x Get end of IML data . x . . . Get stacked error record . x . . . Panel hex display x Unused |
| FUNCTION | 00 01 02 05 07 08 09 0A | Function selection General IPL with IML from disk MOSS IML from disk MOSS dump Remote console link test RSF console link test Local console link test Diskette mode Loop on MOSS diagnostics |
| SERV | 00 01 02 03 | Service selection Normal Customer mode Maint 1 CE mode Maint 2 By-pass MOSS diags Maint 3 First installation |
| CCU | 01 | CCU (always set to 01) |
| STATUS | x x | IPL mode (IPLMODE) x = 0 < == > Operator x = 1 < == > Automatic Customer / Maintenance (MTMENU) x = 0 < == > Customer x = 1 < == > Maintenance |
| REQ | 01 02 03 to 06 07 | IPL on power ON reset CCU + scanners IPL req from KB/D Unused IPL is requested by the level 1 |

Table 11-38 (Page 5 of 5). MOSS BER Type 01 IDs 19 and 20 Field Details

| Field Name | Bit Pattern or Hex Value | Meaning |
|------------|--------------------------------|--|
| LVLE-REQ | 0000 0010 | Identification of CCU IPL request |
| | 0000 0111 | CCU hardcheck |
| | 0000 0011 | Output 70 received |
| | 0000 0100 | Program request IPL Channel request IPL |
| CONF | 01 | Always set to 01 |
| DEFAULT | 01 | Always set to 01 |
| MODE | 01 | Always set to 01 |

MOSS BER Type 01 ID 21

Format foM23: see page 11-104 This BER is logged for availability measurement purposes. This BER corresponds to an IPL requested from the KB/D.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh  DATE:dd/dd  TIME:dd:dd  TYPE:01  ID:21
APPL < error description line >          <REFER.CODE IN CHAR.> CCCCCCCC
EVENT-EXT:hh
STATUS:bbbbbbbb  CCU:hh

===>

F1:END F2:MENU2 F3:ALARII F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

```

MOSS BER Type 01 ID 21 Field Details

Some of the following fields may not appear on the ELD detail display, but they are part of the BER and they are listed as they appear in the BER file. See the section 'BER Formats on Disk' page 11-99

| Table 11-39. MOSS BER Type 01 ID 21 Field Details | | |
|---|---|---|
| Field Name | Bit Pattern or Hex Value | Meaning |
| EVENT-EXT | 01 | IPL |
| STATUS | xxxx xx x x | Unused IPL mode (IPLMODE) x = 0 <===> Operator x = 1 <===> Automatic Customer / Maintenance (MTMENU) x = 0 <===> Customer x = 1 <===> Maintenance |
| CCU | 01 | Always set to 01 |
| CONFIG. | 01 | Always set to 01 |

MOSS BER Type 01 IDs 24 to 29, and 37

Format foM24: see page 11-104. CA concurrent maintenance BER.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:hh
APPL < error description line >          <REFER.CODE IN CHAR.> CCCCCCCC
CA:hh

```

===>

F1:END F2:MENU2 F3:ALARM F4:SUNMARY F5:LIST F7:PREVIOUS F8:NEXT

MOSS BER Type 01 ID 30

Format foM25: see page 11-104. Adapter error.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:30
APPL < error description line >          <REFER.CODE IN CHAR.> CCCCCCCC
FRU GROUP:hhhh

```

===>

F1:END F2:MENU2 F3:ALARM F4:SUNMARY F5:LIST F7:PREVIOUS F8:NEXT

MOSS BER Type 01 ID 32

Format foM27: see page 11-104. MCAD error.

```

                                ELD DETAIL
SEL#:ddd   FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:32
APPL < error description line >          <REFER.CODE IN CHAR.> CCCCCCCC
PLIST:hhhhhhhh PRB:hhhhhhhh DATA:hh  CHND:hhhh  ERR:hhhh

```

===>

F1:END F2:MENU2 F3:ALARM F4:SUNMARY F5:LIST F7:PREVIOUS F8:NEXT

MOSS BER Type 01 IDs 30, and 32 - Field Description

| Table 11-40. MOSS BER Type 01 IDs 30, 32 Field Description | | |
|--|----------------------------|-----------------------------------|
| Field Name | Meaning | Refer to |
| PLIST | Pointer to IORB list | Page 11-22 Page 11-59 (ARC) |
| PRB | Current IORB pointer value | |
| SRB | Unused | |
| FRU GROUP | Part of the reference code | |
| ERR | Return code from adapter | |
| DISC | Unused | |
| DATA | Data sent to adapter | |
| CMD | Command sent to adapter | |
| | | |

MOSS BER, Type 01 ID 36

Cyclic hour notification

```

                                ELD DETAIL
SEL#:ddd  FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:36
APPL < error description line >                <REFER.CODE IN CHAR.> CCCCCCCC

```

```

====>

```

```

F1:END F2:MENUE2 F3:ALARM F4:SUIHARY F5:LIST F7:PREVIOUS F8:NEXT

```

MOSS BER Type 01 ID 38

Format foM28: see page 11-105. CA concurrent maintenance NCP request to cancel

```

                                ELD DETAIL
SEL#:ddd  FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:38
APPL < error description line >                <REFER.CODE IN CHAR.> CCCCCCCC
ERR1:hhhh  ERR2:hhhh

```

```

====>

```

```

F1:END F2:MENUE2 F3:ALARM F4:SUIHARY F5:LIST F7:PREVIOUS F8:IIEXT

```

MOSS BER Type 01 ID 39

Format foM33: see format page 11-105 MMIO interface.

```

                                ELD DETAIL
SEL#:ddd  FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:39
APPL < error description line >                <REFER.CODE III CHAR.> CCCCCCCC
IOIRV:hh  PIRV:hh  PIC: STATUS:hh  REQ:hh

```

```

====>

```

```

F1:END F2:MENUE2 F3:ALARM F4:SUIHARY F5:LIST F7:PREVIOUS F8:NEXT

```


MOSS BER Type 01 IDs 38 and 39 - Field Description

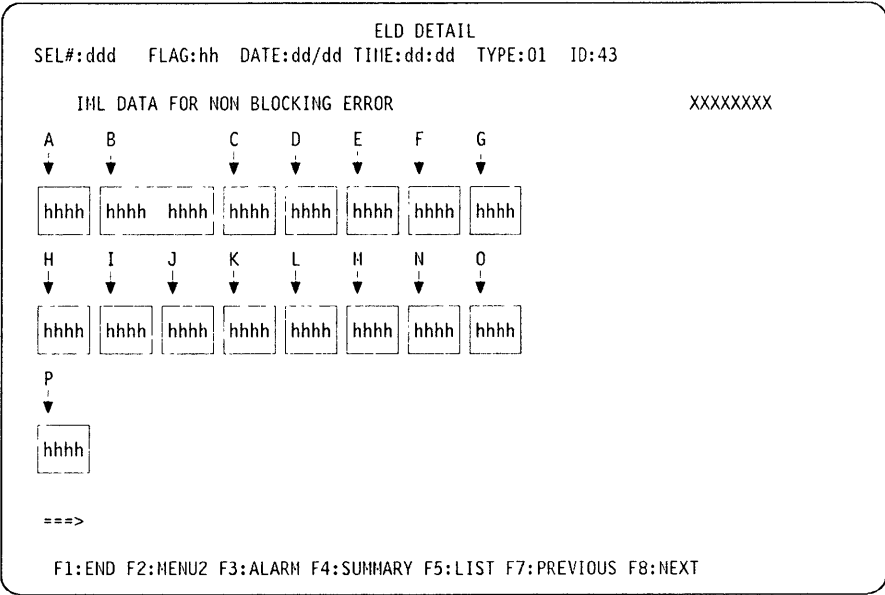
| Table 11-41. MOSS BER Type 01 IDs 38 and 39 Field Description | | |
|---|---|------------|
| Field Name | Meaning | Refer to |
| ERROR 1 | Error code 1 (contains CCU-OUTPUT X57 request from NCP) | Page 11-92 |
| ERROR 2 | Error code 2 (contains CCU-INPUT X57 return from MOSS) | Page 11-92 |
| IOIRV | I/O interrupt request vector | Page 11-45 |
| PIRV | Program interrupt request vector | Page 11-45 |
| PIC | Controller IPL type | |
| REQ | Mailbox information | |

MOSS BER Type 01 IDs 38 and 39 - Field Details

| Table 11-42. MOSS BER Type 01 ID 39 Field Details | | |
|---|--|--|
| Field Name | Bit Pattern or Hex Value | Meaning |
| CCU INPUT X57 Byte 0 | x x x x xxxx | CA 5 MOSS request pending CA 6 MOSS request pending CA 7 MOSS request pending CA 8 MOSS request pending Unused |
| Byte 1 | | Unused |
| CCU OUTPUT X57 Byte 0 | x x x x xxxx | Set/reset CA 5 MOSS request Set/reset CA 6 MOSS request Set/reset CA 7 MOSS request Set/reset CA 8 MOSS request Unused |
| Byte 1 | | Unused. |

MOSS BER Type 01 ID 43

This BER gives complementary information to BER type 01 ID 30.



Note: The representation of this BER is modified for explanatory purpose. On the MOSS display screen, only data lines (hhhh in the picture) are shown.

MOSS BER Type 01 ID 43 - Field Details

The data are displayed in hexadecimal form. The next table gives the bit correspondance of the fields referenced in the previous picture.

| Table 11-43 (Page 1 of 5). MOSS BER Type 01 ID 43 Field Details | | |
|---|--|---|
| Field Name | Bit Pattern | Meaning |
| A | | Panel and Miscellaneous Warnings |
| Byte 1 | <div>X X X X X X X X X</div> | <div>Problem suspected with hexadecimal display</div> <div>ROS 8K entry wrongly selected</div> <div>Information from panel not valid</div> <div>TOD not operative</div> <div>Single error threshold is reached</div> <div>Spare bit of MSC is used</div> <div>Spare bit test not successfull</div> <div>Display requested at end of IML</div> |
| Byte 2 | | Unused |
| B | | Test of the 3 PCAs |
| Byte 1 | <div>X X X X X . . .</div> | <div>PCAs state</div> <div>PCA1 test unsuccessfull (local)</div> <div>PCA2 test unsuccessfull (remote/alternate)</div> <div>PCA3 test unsuccessfull (RSF)</div> <div>Unused</div> |

| Table 11-43 (Page 2 of 5) MOSS BER Type 01 ID 43 Field Details | | |
|--|----------------|--|
| Field Name | Bit Pattern | Meaning |
| Byte 2 | X | PCA1 warnings |
| | . X | Hardwired values impossible in PCA1 |
| | . . X | Error in PCA1 test asynchronous |
| | . . . X . . . | Unexpected level 0 IR in PCA1 test |
| | X . . | PCA1 internal wrap asynchronous test KO |
| | XXX | Unexpected interrupt during PCA1 test |
| Byte 3 | XXX | Unused |
| | XXX | PCA2 warnings |
| | X | Hardwired values impossible in PCA2 |
| | . X | Error in PCA2 test asynchronous |
| | . . X | Unexpected level 0 IR in PCA2 test |
| | . . . X . . . | PCA2 internal wrap asynchronous test KO |
| Byte 4 | X . . | Unexpected interrupt during PCA2 test |
| | XXX | Unused |
| | X | PCA3 warnings |
| | . X | Hardwired values impossible in PCA3 |
| | . . X | Error in PCA3 test asynchronous |
| | . . . X . . . | Unexpected level 0 IR in PCA3 test |
| | X . . | PCA3 internal wrap asynchronous test KO |
| | XXX | Unexpected interrupt during PCA3 test |
| | XXX | Unused |
| C to P | | MCAC test warnings |
| C | | IPL and adapters information |
| Byte 1 | X | Unused |
| | . X | MCAD KO |
| | . . X | Unused |
| | . . . X . . . | MCCU KO |
| | XX . . | Unused |
| | X . | IPL not possible on CCU |
| Byte 2 | X | Unused |
| | X | Unused |
| | . X | MCAD usable |
| | . . X | Unused |
| | . . . X . . . | MCCU usable |
| | XXXX . | Unused |
| D | | |
| Byte 1 | X | MCAD errors |
| | . X | Valid PIO unrecognised by MCAD |
| | . . X | Valid PIO unrecognised by MCAD |
| | . . . X . . . | Unused |
| | X . . | CADS HLIR bit not expected |
| | X . | Unused |
| Byte 2 | XX | CADS LLIR bit unexpected |
| | XX | Unused |
| | X | MCAD detection information |
| | . X | Unused |
| | . . X | No error detection allowed |
| | . . . X . . . | Bad pty not found in MCAD/MOSS processor |
| | X . . | Invalid PIO command not detected |
| | X . | Unused |
| | X . | Error in MCAD not reported to MOSS processor |
| | X . | Parity error in MCAD during a write |
| | X | Parity error in MOSS processor during a read |
| E | | |

Table 11-43 (Page 3 of 5). MOSS BER Type 01 ID 43 Field Details

| Field Name | Bit Pattern | Meaning |
|------------|--|---|
| Byte 1 | X X X X xxxx | MCAD reporting MCAD IR 4 not reported to MOSS processor No CADS HLIR reporting in MCAD Unused No CADS LLIR reporting in MCAD Unused |
| Byte 2 | X X X X X X X X | CADS actions information All CA disabled, sense bit KO CADS MOSS power-ON reset bit ON Unused Validation of enable and reset CADS not possible Unused Reset of CADS not possible Nohold bit ON in CAMPOR register Force error bits ON in MCAD |
| F | | Reset CADS information |
| Byte 1 | xxxx X X X X | Unused M reset CADS 5 ON M reset CADS 6 ON M reset CADS 7 ON M reset CADS 8 ON |
| Byte 2 | | Unused |
| G | | Enable CADS possibilities |
| Byte 1 | xxxx X X X X | Unused Enable CADS 5 not possible Enable CADS 6 not possible Enable CADS 7 not possible Enable CADS 8 not possible |
| Byte 2 | | Unused |
| H | | Reset CADS possibilities |
| Byte 1 | xxxx X X X X | Unused Reset CADS 5 not possible Reset CADS 6 not possible Reset CADS 7 not possible Reset CADS 8 not possible |
| Byte 2 | | Unused |
| I | | Enable CADS information |
| Byte 1 | xxxx X X X X | Unused Enable CADS 5 ON Enable CADS 6 ON Enable CADS 7 ON Enable CADS 8 ON |
| Byte 2 | | Unused |
| J | | Sense CA enabled information |
| Byte 1 | xxxx X X X X | Unused Sense CA 5 enabled at machine power-ON or machine reset Sense CA 6 enabled at machine power-ON or machine reset Sense CA 7 enabled at machine power-ON or machine reset Sense CA 8 enabled at machine power-ON or machine reset |

| Table 11-43 (Page 4 of 5). MOSS BER Type 01 ID 43 Field Details | | |
|---|---|---|
| Field Name | Bit Pattern | Meaning |
| K | | Sense CA information |
| Byte 1 | xxxx x x x x x | Sense CA KO information Unused Sense CA enabled 5 not OK Sense CA enabled 6 not OK Sense CA enabled 7 not OK Sense CA enabled 8 not OK |
| Byte 2 | xxxx x x x x | Sense CA presence KO information Unused Sense CADS 5 presence not OK Sense CADS 6 presence not OK Sense CADS 7 presence not OK Sense CADS 8 presence not OK |
| L | | CADS interface state |
| Byte 1 | xxxx x x x x | Unused Interface with CADS 5 KO Interface with CADS 6 KO Interface with CADS 7 KO Interface with CADS 8 KO |
| Byte 2 | | Unused |
| M | | Miscellaneous MCAD errors |
| Byte 1 | xx x x xxxx | Unused M force error impossible in MCAD Unused |
| Byte 2 | | Unused |
| N | | MCCU errors |
| Byte 1 | x x x x x xxx | Valid PIO unrecognised by MCCU Valid PIO unrecognised by MCCU IOC tag reset function KO Unused IOC bus disabled by MCCU Unused MCCU error detection |
| Byte 2 | x x x x x x x x | Unused No error detection possible No CCU HLIR detection possible No CCU LLIR detection possible No CSP LLIR detection possible MIOC time out counter down Bad pty not forced in MCCU, or MOSS processor Unused |
| O | | MCCU errors |
| Byte 1 | x x x x x x x xx | MCCU error detection Unused MCCU IR 0 not reported to MOSS processor MCCU IR 1 not reported to MOSS processor MCCU IR 4 not reported to MOSS processor IR level 4 not possible in MCCU MIOC time out not detected Unused |

Table 11-43 (Page 5 of 5). MOSS BER Type 01 ID 43 Field Details

| Field Name | Bit Pattern | Meaning |
|------------|--|---|
| Byte 2 | X X X X X X X X | MCCU data transfer error Interface MCCU and CCU KO Wrap test failed on MCCU MCCU data transfer not possible No 'CYCLE STEAL END IR' possible MCCU CHIO transfer not possible Unused MOSS INOP line not operative MOSS INOP reset not OK |
| P | | MCCU miscellaneous |
| Byte 1 | X X X X X X X X | M MIOC interface sense bits KO M force errors not possible Unused M PGM WAIT signal wrong in MCCU M card ID not available for MCC M IOC tag reset function unusable M disable IOC bus not usable M watchdog mechanism KO in MCCU |
| Byte 2 | | Unused |

MOSS BER Type 01 ID 44

```

ELD DETAIL
SEL#:ddd  FLAG:hh  DATE:dd/dd  TIME:dd:dd  TYPE:01  ID:44

MOSS CODE DATA FOR PROBLEM ISOLATION
CCCCCCCC hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
hhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
hhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
hhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
hhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
hhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
hhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh

===>

F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

```

MOSS BER Type 01 ID 44 - Field Description

This BER is for PE only; no details are given about the meaning of the data displayed. It is not a failure BER or an error BER, it is an additional information for other BERs. The first 8 bytes contains the name of the control section at the origin of the BER logging. The contents of the 248 remaining bytes depends on the origin of the request. The screen displays '*****' for the unused bytes.

MOSS BER (IDs 50 to C2)

MOSS BER Type 01 ID 50

This BER is logged after three unsuccessful sign ON attempts on the remote console. There is no data in this BER. It only displays the message:

REMOTE CONSOLE REJECTED

MOSS BER Type 01 ID 80

See MOSS BER Type 01 ID 00, 11-40

MOSS BER Type 01 IDs 91, B3, C1, C2

Format foM8: see page 11-101.

The NCP/PEP program level 4 generates BERs 91, B3, C1, and C2 if a MOSS error occurs during a mailbox exchange. This BER is transferred to MOSS if MOSS successfully recovers from the MOSS error.

These BERs should always be accompanied by MOSS BER IDs 00, 01, 02, or 03. When BER ID 91 is not accompanied by one of these BERs, it only means that the MOSS has been inoperative during a period of time (MOSS re-IML, MOSS dump) and the BER ID is logged for information only.

```
                                ELD DETAIL
SEL#:ddd  FLAG:hh  DATE:dd/dd TIME:dd:dd  TYPE:01  ID:hh
CP< error description line >      <REFER.CODE IN CHAR.> CCCCCCCC
MB:hh hh  hhhh hh  hhhhhh hhhh hhhh hhhh hhhh
    hhhh hh  hhhhhh hhhh hhhhhhhh hhhhhhhh

===>

F1:END F2:MENUE2 F3:ALARH F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT
```


BER Formats on Disk

BERs Printed on Host

The length of the BERs printed from the disk on the host is not significant. When the BER detail is displayed on the console display, only the useful information is given. The remaining BER bytes, if any, printed but not displayed, have no meaning. Do not try to interpret them, they may lead to erroneous actions.

MOSS BERs Type 01 Formats

| Format: foM0 | | Format: foM1 | |
|--------------|--------------------|--------------|--------------------------------|
| ID: 00 | | ID: 01 | |
| Byte | Meaning | Byte | Meaning |
| 1-27 | Header | 1-27 | Header |
| 28-29 | TYPE-ID | 28-29 | TYPE-ID |
| 30-31 | MOSS CHECK | 30 | ABEND |
| 32-33 | Action code | 31 | Flag |
| 34-35 | Hexadecimal code | 32-33 | WHO/WHAT - CHECK |
| 36 | EIRV | 34-35 | Recovery action |
| 37-38 | DIV | 36-47 | MCCUA REGS |
| 39 | IORV | 48 | CCUA CMSA |
| 40 | PIRV | 49-51 | CCUA X75 |
| 41 | CPLLPL | 52-54 | CCUA X76 |
| 42 | CM | 55-57 | CCUA LSR |
| 43 | MM | 58 | STATUS |
| 44 | CHM | 59 | Unused |
| 45 | Unused | 60-61 | CCUA CP abend |
| 46-49 | IA | 62-63 | CCUA TA |
| 50-53 | PSCI | 64-85 | Unused |
| 54-57 | OP | 86 | STATUS |
| 58-105 | Regs interrupt LVL | 87 | Unused |
| 106-107 | CHCV | 88-89 | CCUA CP abend |
| 108-109 | Register space | 90-91 | CCUA TA |
| 110-113 | Main storage loc. | 92-103 | MCAD REGS |
| 114-117 | CHIO (current) | 104 | Map of register value |
| 118-119 | DUMP | 105 | CCU for CADS |
| 120 | MOSS dump stat | 106 | IOC for CADS |
| 121 | EIRV (1) | 107 | NUM for CADS |
| 122 | IORV (1) | 108-113 | Reentry count |
| 123 | PIRV (1) | 114-120 | Count for unexpected interrupt |
| 124-125 | DIV (1) | 121 | CHGHICAC return code |
| 130-133 | PSCI (1) | 122 | Unused |
| 134-137 | OP (1) | | |
| 138-142 | PCA1 | | |
| 143-147 | PCA2 | | |
| 148-152 | PCA3 | | |
| 153 | Unused | | |
| 154-165 | MCCUA | | |
| 166-177 | Unused | | |
| 178-181 | Unused | | |
| 182-193 | MCAD | | |
| 194-196 | DFA | | |
| 197 | TOD | | |
| 198-224 | Snapshot dump | | |
| 225-232 | Module name | | |
| 233-251 | Spurious error cnt | | |
| 252-289 | Statistics count | | |

NOTE: The fields followed by (1) give information in case of a level 0 re-entry.

Figure 11-16 (Part 1 of 7). MOSS BER Type 01 Formats

MOSS BER Formats

| Format: foM2 | |
|--------------|-------------|
| ID: 02 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | MOSS-CHECK |
| 31 | ADNO |
| 32 | CMD |
| 33 | PIRV |
| 34 | IOIRV |
| 35 | CMSB |
| 36 | STAC |
| 37 | CAC-RC |
| 38 | CA |
| 39-40 | STAT0 |
| 44-45 | STAT1 |
| 46-47 | STAT4 |
| 48-49 | Unused |
| 50-53 | ADDR |
| 54-65 | PCW |
| 66 | Flags (ACB) |

| Format: foM3 | |
|--------------|----------------|
| ID: 03 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | MOSS-CHECK |
| 31 | DEV |
| 32 | CMD (log. cmd) |
| 33 | REQ |
| 34 | Flag |
| 35 | CNT |
| 36 | Unused |
| 37 | ARC |
| 38-41 | ADDR |
| 42-43 | BSTAT |
| 44-49 | CCB |
| 50-57 | BCLC |
| 58-69 | SSB |
| 70-77 | FILE mod name |

| Format: foM4 | |
|--------------|------------|
| ID: 04 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | MOSS-CHECK |
| 31 | CMD |
| 32 | BSTAT |
| 33 | ASTAT |
| 34-35 | CSTAT |
| 36 | MSTAT |

| Format: foM5 | |
|--|------------|
| ID: 05 | |
| MOSS Check 00 01 02 04 05 08 10 20 40 80 FF | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | MOSS-CHECK |
| 31 | ADDR |
| 32-34 | X76 |
| 35-36 | STATUS |
| 37 | Adapter ID |
| 38 | IOC bus IS |

Figure 11-16 (Part 2 of 7). MOSS BER Type 01 Formats

| | | | |
|---------------|----------------|------------------|-------------------|
| Format: foM5a | | Format: foM6 | |
| ID: 05 | | ID: 06 | |
| MOSS Check F0 | | MOSS Check 03 06 | |
| Byte | Meaning | Byte | Meaning |
| 1-27 | Header | 1-27 | Header |
| 28-29 | TYPE-ID | 28-29 | TYPE-ID |
| 30 | MOSS-CHECK: F0 | 30 | MOSS-CHECK |
| 31 | ADDR | 31 | IPL information |
| 32-33 | DUMP info | 32 | CCU Id |
| 34 | Unused | 33 | REQ |
| 35-58 | Scanner dump | 34 | LVL1 REQ |
| | | 35 | System status |
| | | 36-37 | IPL check code |
| | | 38-165 | LA |
| | | 166-180 | Disk error |
| | | 181-182 | F2 |
| | | 183-185 | X71 |
| | | 186-188 | X72 |
| | | 189 | IPL mode |
| | | 190-192 | CCU configuration |
| | | 193-216 | MIS (Error 06) |
| | | 217 | F1 |
| | | 218-219 | RC from CDF |
| | | 220-315 | CADS |
| | | 316-317 | IPLCHECK |

| | | | |
|------------------|------------|------------------|------------|
| Format: foM7 | | Format: foM8 | |
| ID: 06 | | IDs: 91 B3 C1 C2 | |
| MOSS Check 01 02 | | | |
| Byte | Meaning | Byte | Meaning |
| 1-27 | Header | 1-27 | Header |
| 28-29 | TYPE-ID | 28-29 | TYPE-ID |
| 30 | MOSS-CHECK | 30 | MOSS-CHECK |
| | | 31-32 | COMMAND |
| | | 33-64 | MB |

Figure 11-16 (Part 3 of 7). MOSS BER Type 01 Formats

MOSS BER Formats

| Format: foM9 | |
|-----------------------------|------------------|
| ID: 06 | |
| EXT: 05 07 MOSS Check 05 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | MOSS-CHECK: 05 |
| 31 | EXTENSION: 05/07 |
| 32 | CCU Id |
| 33-34 | NCP abend |
| 35 | Dump status 0 |
| 36 | Unused |

| Format: foM9a | |
|--------------------------|----------------|
| ID: 06 | |
| EXT: 05 MOSS Check 08 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | MOSS-CHECK: 08 |
| 31 | EXTENSION: 05 |
| 32 | CCU Id |
| 33-35 | IAR |
| 36-38 | SAR |
| 39-41 | LAR |
| 42-44 | X70 |
| 45-47 | X76 |
| 48-50 | X7D |
| 51-53 | X7E |
| 54-55 | HDCK |

| Format: foM10 | |
|---------------|-----------------|
| ID: 06 | |
| MOSS Check 09 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | MOSS-CHECK: 09 |
| 31 | CCU |
| 32-33 | IPL-CHECK(OF1B) |
| 34-36 | X71 MSA displ. |
| 37-39 | X72 MSA displ. |
| 40-42 | IAR |
| 43-45 | WKR1 |
| 46-48 | WKR2 |
| 49-51 | WKR3 |
| 52-54 | WKR4 |
| 55-57 | WKR5 |
| 58-60 | WKR6 |
| 61-63 | WKR7 |
| 64-65 | X7E |
| 66-67 | X7D |
| 68-69 | X76 |
| 70-71 | CA XD |
| 72-73 | CA XE |
| 74-75 | X50 |
| 76-77 | X51 |
| 78-79 | X52 |
| 80-81 | X60 |
| 82-145 | LA |

| Format: foM12 | |
|---------------|-------------------|
| ID: 19 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | Flag (error C) |
| 31-32 | Alert indicator |
| 33 | Req |
| 34 | FCN |
| 35 | Serv |
| Panel old: | |
| 36 | Req |
| 37 | FCN |
| 38 | Serv |
| 39-86 | Hexadecimal codes |
| 87-88 | CDF RC |
| 89-90 | ECB DISC |
| MIOC: | |
| 91-92 | CCUA |
| 93-94 | CCUB |
| MB CCUA: | |
| 95 | CMND |
| 96-97 | STAT |
| MB CCUB: | |
| 98 | CMND |
| 99-100 | STAT |

Figure 11-16 (Part 4 of 7). MOSS BER Type 01 Formats

| Format: foM14 | |
|---------------|-----------------|
| IDs: 10 11 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30-37 | OC1 |
| 38-45 | OC2 common |
| 46-53 | CCUF |
| 54-61 | CCUB |
| 62-107 | IORB |
| 108-115 | PLIST for ID 10 |
| 108-127 | PLIST for ID 11 |

| Format: foM15 | |
|---------------|----------------|
| IDs: 12 13 14 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30-37 | OC1 |
| 38-45 | OC2 |
| 46-53 | CCUF |
| 54-61 | CCUB |
| 62-77 | IORB for ID 14 |
| 62-90 | IORB for ID 13 |
| 62-107 | IORB for ID 12 |

| Format: foM16 | |
|---------------|---------|
| ID: 08 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | DUMP |
| 31 | TRACE |
| 32 | CA |
| 33 | CCU |
| 34 | Unused |

| Format: foM18 | |
|------------------|---------|
| IDs: 16 1A 1B 1D | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30-37 | OC1 |
| 38-45 | OC2 |
| 46-53 | CCUF |
| 54-61 | CCUB |
| 62-77 | IORB |
| 82-93 | PLIST |

| Format: foM19 | |
|---------------------------|---------------|
| ID: 06 | |
| MOSS Check: 08 EXT: 07 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | MOSS-CHECK |
| 31 | EXT |
| 32 | CCU |
| 33-34 | CP abend code |

| Format: foM21 | |
|---------------|---------------|
| ID: 20 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | MOSS-check |
| 31 | ORIGI |
| 32 | Function |
| 33 | SERV |
| 34 | CCU |
| 35 | STATUS |
| 36 | REQ |
| 37 | LVL1-REQ |
| 38 | Configuration |
| 39 | CCU Default |
| 40 | 3745 mode |

Figure 11-16 (Part 5 of 7). MOSS BER Type 01 Formats

| Format: foM22 | |
|---------------|---|
| ID: 85 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 29-xx | 1st BER with its own length |
| xxx-xxx | 2nd BER with its own length |
| xxx-xxx | 3rd BER with its own length |
| | Note: There may be more than three BERs |

| Format: foM23 | |
|---------------------|-----------------|
| ID: 21 | |
| EXT: 01 02 03 04 05 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | Event-ext |
| 31 | Status |
| 32 | CCU ID |
| 33 | Configuration |
| 34 | CAC return code |
| 35 | CCU default |
| 35 | 3745 mode |

| Format: foM24 | |
|-------------------|---------|
| IDs: 24 to 29, 37 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | CA |

| Format: foM25 | |
|---------------|-----------|
| ID: 30 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30-31 | FRU GROUP |

| Format: foM27 | |
|---------------|---------|
| ID: 32 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30-33 | PLIST |
| 34-37 | PRB |
| 39 | DATA |
| 40-41 | CNND |
| 42-43 | ERR |

Figure 11-16 (Part 6 of 7). MOSS BER Type 01 Formats

| | | | |
|--------------------|--------------------|----------------|-----------------|
| Format: foM29 | | Format: foM29a | |
| ID: 07 | | ID: 07 | |
| ERROR: 04 08 40 80 | | ERROR: FE | |
| Byte | Meaning | Byte | Meaning |
| 1-27 | Header | 1-27 | Header |
| 28-29 | TYPE-ID | 28-29 | TYPE-ID |
| 30 | ERROR | 30 | ERROR= FE |
| 31-32 | TRA ADDR | 31-32 | TRA INPUT ADDR |
| 33-34 | Get CMD complete | 33-34 | TRA OUTPUT ADDR |
| | Lvl 2 err status | 35 | TIC NBR |
| 35-36 | TIC 1 Lvl 2 error | 36-37 | 2K-blk INITIAL |
| | status | 38-39 | 2K-blk REQUEST |
| 37-38 | TIC 2 | 40-41 | 2K-blk FINAL |
| 39-42 | Unused | 42 | STOP CMD CNT |
| 43-44 | MOSS error status | | |
| 45-46 | Lvl 1 error status | | |
| 47-48 | TIC CTL register | | |
| 49-51 | X'76' | | |

| | | | |
|---------------------|-------------|---------------|---------|
| Format: foM29b | | Format: foM30 | |
| ID: 07 | | ID: 15 | |
| EXT: 01 02 03 04 05 | | | |
| Byte | Meaning | Byte | Meaning |
| 1-27 | Header | 1-27 | Header |
| 28-29 | TYPE-ID | 28-29 | TYPE-ID |
| 30 | ERROR | 30-37 | OC1 |
| 31 | ERROR EXT | 38-45 | OC2 |
| 32 | TRA number | 46-53 | CCUF |
| 33-34 | TRA address | 54-61 | CCUB |
| 35 | TIC number | 62-77 | IORB |
| 36 | CCU | 78-101 | PLIST |
| | | 102-133 | BLK4T |

| | | | |
|---------------|------------|---------------|-----------------|
| Format: foM31 | | Format: foM33 | |
| ID: 17 | | ID: 39 | |
| Byte | Meaning | Byte | Meaning |
| 1-27 | Header | 1-27 | Header |
| 28-29 | TYPE-ID | 28-29 | TYPE-ID |
| 30 | MOSS-CHECK | 30 | IORV |
| 31 | BCLE | 31 | PIRV |
| 32 | CMD | 32-233 | Internal buffer |
| 33 | B STAT | 234 | Status |
| 34 | A STAT | 235 | REQ |
| 35-38 | C STAT | | |
| 39 | M STAT | | |

Figure 11-16 (Part 7 of 7). MOSS BER Type 01 Formats

Diagnostics BER Type 03

Diagnostics BER Type 03 - Summary

| Table 11-44. BER Type 03 Description | |
|--------------------------------------|---|
| BER ERROR | ID DESCRIPTION |
| 01 | Diagnostic started |
| 02 | Diagnostic completed successfully |
| 03 | Hardware error detected by diagnostic |
| 04 | Microcode error detected in a diagnostic (ABEND type 1 and 2) |
| 05 | Microcode error detected in the monitor (ABEND type 3) |

Diagnostics BER Type 03 - Detailed BER Display

Diagnostics BER Type 03 - IDs 01 and 02: Format foD1, see page 11-107

```

                                ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:03 ID:hh
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC
GROUP NBR:hh IFT/SECT:hhhh ROUTINE:hh ADT NBR:hh LINE NBR:hh

===>

F1:END F2:MENUE2 F3:ALARM F4:SUNMARY F5:LIST F7:PREVIOUS F8:NEXT

```

Diagnostics BER Type 03 - ID 03: Format foD2, see page 11-107

```

                                ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:03 ID:03
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC
ERC:hhhh RAC:hhhh
ERROR BIT:hhhh
ADT NBR:hh LINE NBR:hh MUX NBR:hh CCU ATT:hh
IFT/SECT:hhhh ROUTINE:hh

===>

F1:END F2:MENUE2 F3:ALARM F4:SUNMARY F5:LIST F7:PREVIOUS F8:NEXT

```

Diagnostics BER Type 03 - IDs 04 and 05: Format foD3, see page 11-107

```

                                ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:03 ID:hh
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC
RAC:hhhh ADT NBR:hh CCU ATT:hh IFT/SECT:hh ROUTINE:hh

===>

F1:END F2:MENUE2 F3:ALARM F4:SUNMARY F5:LIST F7:PREVIOUS F8:NEXT

```

Note: When running the diagnostics, the BR option generates the diagnostic BERs when a machine error is encountered. To suppress the generation, the command 'NBR' is used. The default option is BR. For more information see *Service Functions, SY33-2069*.

Diagnostic BERs Type 03 - Formats

Format: fo01

IDs: 01 and 02

| Byte | Meaning |
|-------|---------------------|
| 1-27 | Header |
| 28 | Group number |
| 29-31 | IFT section-routine |
| 32 | Adapter seq. number |
| 33 | Adapter line addr. |

Format: fo03

IDs: 04 and 05

| Byte | Meaning |
|--------|---------------------|
| 1-27 | Header |
| 28-29 | Type ID |
| 30-43 | Unused |
| 44-45 | RAC |
| 46-61 | Unused |
| 62 | Adapter seq. number |
| 63-64 | Unused |
| 65 | CCU attached |
| 66-189 | Unused |
| 190 | IFT |
| 191 | Section |
| 192 | Routine number |

Format: fo02

IDs: 03

| Byte | Meaning |
|--------|---------------------|
| 1-27 | Header |
| 28-29 | Type ID |
| 30-33 | Unused |
| 34-35 | Ref. error code |
| 36-37 | RAC code |
| 38-45 | Unused |
| 46-47 | Error bit |
| 48-61 | Unused |
| 62 | Adapter seq. number |
| 63 | Line address |
| 64 | MUX Id |
| 65 | CCU attached |
| 66-189 | Unused |
| 190 | IFT |
| 191 | Section |
| 192 | Routine number |

Figure 11-17. Diagnostics BER Formats

Power BER Type 04

Power Subsystem BER Type 04 - Summary

| BER ID | Description of the event | ALERT | ALARM |
|--------|---|-------|-------|
| 01 | Overcurrent fault | -- | 9C |
| 02 | PS fault | -- | 9C |
| 04 | Airflow fault | -- | A7 |
| 08 | MOSS control panel error | 08 | 08 |
| 0A | Power control mode change | -- | -- |
| 0F | Battery failure | A5 | A5 |
| 10 | Internal clock down | A6 | A6 |
| 11 | Thermal detector failure | -- | 9B |
| 12 | AC failure | A3 | A3 |
| 13 | Invalid AC failure | A4 | A4 |
| 14 | Cooling problem corrected | AD | AD |
| 15 | Remote power OFF received | -- | -- |
| 17 | Battery OK | -- | -- |
| 20 | Error on MOSS reset | AC | AC |
| 21 | Error on MMIO | AC | AC |
| 22 | Error on RPO signal | AC | AC |
| 23 | Error on CCU reset | -- | AC |
| 28 | End of IML data due to a temporary AC failure | A3 | A3 |
| 29 | End of IML data due to an unexpected event | -- | -- |
| 30 | Microcode error/Power dump | AB | AB |
| 31 | Set time of day | -- | -- |
| 35 | Battery changed | -- | -- |
| 36 | Change battery | A5 | A5 |

Figure 11-18. Power Subsystem BER Type 04 Summary

Note: The description of the events does not necessarily match the alarm messages listed in the *Problem Determination Guide*.

Power BER Type 04 (Detailed BER Display)

Power BER Type 04 - IDs 01, 02, 04, 08 and 12: Format foP1, see page 11-114.

```

ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:04 ID:hh
<ERROR DESCRIPTION> <REFER.CODE IN CHAR.> CCCCCCCC
REQ:hh RESP:hh PS ID:hh AFD ID:hh
PS TYPE:hh OLD STATUS:bbbb BUS ID:bbbbbbbb
ADAPTER1:hh ADAPTER2:hh
RPO:hh CCU:hh

```

===>

F1:END F2:MENUE2 F3:ALARM F4:SUNMARY F5:LIST F7:PREVIOUS F8:NEXT

Power BER Type 04 - ID 0A: Format foP1, see page 11-114.

```

                                ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:04 ID:0A
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC
OLD      NEW
bbbbbbbb bbbbbbbb

===>

F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

```

Power BER Type 04 - IDs 20 to 23: These BER display a single line of information, indicating the type of error, according to the next list:

ID 20 Power control detected error on MOSS reset
ID 21 Power control detected error on MMIO
ID 22 Power control detected error on RPO signal
ID 23 Power control detected error on CCU reset

One of those BER is generated when the corresponding lines is found every time clamped to the same level.

Power BER Type 04 - IDs 28, 29: Format foP2, see page 11-114.

```

                                ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:04 ID:hh
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC
IHL SOURCE:hh CAUSE:hh REASON:hh
CONTROL IODE:hh INSTAL TYPE:hh

===>

F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

```

Power BER Type 04 - ID 30: Format foP3, see page 11-114

```

                                ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:04 ID:30
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC

IOIRV:hh PIRV:hh REQ:hh RESP:hh
ERR:hh ECB:hhhh

===>

F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

```

Power BER Type 04 - ID 31: Format foP4, see page 11-114.


```

ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:04 ID:31
<ERROR DESCRIPTION> <REFER.CODE III CHAR.> CCCCCCCC
DATE:hh / hh / hh
DAY :hh
TIME:hh : hh : hh

```

```

===>

```

```

F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

```

Power BER Type 04 - Field Description

| Table 11-45. Power BER type 04 Field Description | | |
|--|--|---|
| Field name | Meaning | Refer to |
| AFD | Not used | -- |
| BUS ID | Not used | -- |
| CCU | Always set to 01 | -- |
| Control Mode | See OLD and NEW | Page 11-111 |
| ECB | Event control block | (*) |
| ERR | Microcode error | Page 11-111 |
| IML/IPL | <ul style="list-style-type: none"> • Source of IML/IPL • Cause of IML/IPL • Reason of power OFF | <ul style="list-style-type: none"> • Page 11-111 • Page 11-111 • Page 11-111 |
| Install-Type | MPW power logic card state | Page 11-111 |
| IOIRV | I/O interrupt request vector | Page 11-45 |
| LAR | Lagging address registers (input X'74') | |
| NEW | New panel info (01 = host, 02 = network, 03 = local) | -- |
| OLD | Old panel info (01 = host, 02 = network, 03 = local) | -- |
| PIRV | Program interrupt request vector | Page 11-45 |
| PS ID | Not used | -- |
| PS Type | Not used | -- |
| REQ | See request description | Page 11-112 |
| RESP | PLC response to MOSS | Page 11-113 |
| RPO | Request power OFF | Page 11-111 |

(*) For software information on BERs originated by NCP/PEP, refer to the associated product documentation.

Power BER Type 04 - Field Details

Some of the following fields may not appear on the ELD detail display, but they are part of the BER and they are listed as they appear in the BER file. See the section 'BER Formats on Disk' page 11-99

Table 11-46. BER 04 Field Details

| Field Name | Field Value | Meaning |
|-------------------|-------------|---|
| IPL/IML source | 01 | Host requested IPL |
| | 02 | Auto restart |
| | 03 | Unused |
| | 04 | Request from panel |
| | 05 | Unused |
| | 06 | Scheduled power ON |
| | 07 | Unused |
| IPL/IML cause | 01 | MOSS IML |
| | 02 | General IPL |
| | 03 | Unused |
| | 04 | MOSS check |
| Microcode error | 01 | Invalid response |
| | 02 | Request expected |
| | 03 | Response expected |
| | 04 | Invalid interrupt |
| | 05 | Invalid asynchronous event |
| | 06 | Not used |
| | 07 | Power dump requested |
| REASON | 01 | Last power OFF reason |
| | 02 | RPO from host |
| | 03 | AC failure |
| | 04 | Power OFF from NCP |
| | 05 | Power OFF from panel |
| | 06 | EPO |
| | 08 | Air flow detector failure |
| | 09 | Overcurrent problem on a power block |
| | 09 | Power supply problem on a power block |
| | 1A | MOSS power ON reset line clamped every time at the same level |
| RPO | 01 | General power OFF |
| | 02 | Remote power OFF request |
| | 03 | Requested power OFF failed |
| Install Type | 00 | Normal state |
| | 01 | First installation |
| | 02 - 03 | Unused |
| PS OLD/NEW status | | Unused |

RESP and REQ Fields

The **REQ** field may take a different meaning for identical values, depending on the event that was the cause of the BER:

- **BER caused by a power dump.**

The **RESP** field is always Dx:

- D1** The dump was possible.
- D2** The dump already existed.
- D3** The dump failed.

The **REQ** values are given in the following table.

Table 11-47 (Page 1 of 2). BER 04 REQ/RESP Table for Power Dump

| REQ | Requested by | Meaning |
|-----|--------------|---------------------------|
| 01 | PCC | Invalid power ON |
| 02 | PCC | Invalid power OFF |
| 03 | PCC | Invalid power ON reset |
| 04 | PCC | Invalid interrupt level 0 |
| 05 | PCC | Invalid interrupt level 1 |

Table 11-47 (Page 2 of 2). BER 04 REQ/RESP Table for Power Dump

| REQ | Requested by | Meaning |
|-----|--------------|---|
| 06 | PCC | Invalid interrupt level 2 |
| 81 | PCC | Invalid power ON, dump stacked |
| 82 | PCC | Invalid power OFF, dump stacked |
| 83 | PCC | Invalid power ON reset, dump stacked |
| 84 | PCC | Invalid interrupt level 0, dump stacked |
| 85 | PCC | Invalid interrupt level 1, dump stacked |
| 86 | PCC | Invalid interrupt level 2, dump stacked |
| 11 | MOSS | Power microcode error |
| 12 | MOSS | PCC ckeck bad return |
| 20 | Operator | Manual request, via power services |

• **BER caused by an event in the power area.**

RESP field meaning depends on the associated **REQ** field value.

A REQ value corresponds to 2 possible RESP:

- OK response
- KO response

according to the following table:

Note: The **REQUEST** code is valid only when the BER is issued after a MOSS request to the power control.

Table 11-48. BER 04 REQ/RESP Table

| REQ | RESP OK | RESP KO | Meaning |
|-----|---------|---------|------------------------------------|
| 01 | 42 | C2 | Start diskette |
| 02 | 43 | C3 | Stop diskette |
| 05 | N/A | N/A | MPWL reset |
| 07 | 48 | C8 | Start disk |
| 08 | 49 | C9 | Stop disk |
| 09 | 4A | CA | Set adapter |
| 0A | 4B | CB | Reset adapter |
| 0C | 4E | N/A | Check MPWL |
| 0D | 50 | N/A | Get end of IML data |
| 0E | 51 | N/A | Get stacked error record |
| 12 | 55 | N/A | Set time of day |
| 13 | 56 | D6 | Get time of day |
| 14 | 57 | N/A | Set scheduled power ON |
| 15 | 58 | N/A | Get scheduled power ON |
| 16 | 59 | N/A | Allow scheduling |
| 17 | 5A | N/A | Inhibit scheduling |
| 1B | 5E | N/A | Get scheduling state |
| 1F | 70 | F0 | Display message indicator on panel |
| 20 | 76 | F6 | Display console in use |
| 21 | 7E | FE | Display hexadecimal code on panel |
| 22 | 7F | FF | Display function code |

If the BER is issued from an error reported to the MOSS by the power control:

- The **REQUEST** field is set to 00.
- The **RESP** field takes the meaning given in the following table:

Table 11-49. BER 04 RESP Table When REQ = 00

| RESP | Meaning |
|----------|--------------------------------|
| 00 to 05 | Unused |
| 06 | Air flow fault |
| 08 | Overcurrent fault |
| 09 | PS fault |
| 0D | Local request |
| 0E | Force local |
| 0F | Battery KO |
| 11 | Power control mode change |
| 12 | Panel KO |
| 13 | AC failure |
| 14 | Invalid AC failure |
| 15 | MPWA KO |
| 16 | Remote power OFF |
| 18 | Battery OK |
| 19 | Problem on CCU reset |
| 1A | Problem detected on MOSS reset |
| 1B | MMIO errors |

Power BER Type 04 - Formats

| Format foP1 | |
|---------------------|-------------------------------|
| IDs: 01 02 04 08 12 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | REQ |
| 31 | RESP |
| 32 | PS ID |
| 33 | AFD |
| 34 | Retry indicator |
| 35 | PS type |
| 36 | |
| bbbb | Old status |
| bbbb | Address |
| 37 | BUS ID |
| 38 | Adapter 1 |
| 39 | Adapter 2 |
| 40 | RPO |
| 41 | CCU |
| ID: 0A only | |
| 42 | Old control |
| 43 | New control |
| 44 | Tower ID for airflow fault |

| Format foP2 | |
|-------------|--------------------------------|
| IDs: 28 29 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | IML source |
| 31 | CAUSE |
| 32 | POWER OFF reason |
| 33 | CTRL Mode |
| 34-173 | PCT |
| 174-180 | TOD |
| 181 | Install type |
| 182-213 | AFD status |
| 214-217 | Airflow fault on each tower |

| Format foP3 | |
|-------------|-----------|
| ID: 30 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | IORV |
| 31 | PIRV |
| 32 | REQ |
| 33 | RESP |
| 34 | ERR CODE |
| 35-37 | Unused |
| 38-41 | MPNL data |
| 42-43 | ECB |

| Format foP4 | |
|-------------|-----------------------------|
| ID: 31 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30-32 | Time (SS, MM, HH) in Hex |
| 33 | Day of week |
| 34-36 | Date (day, month, year) |

Figure 11-19. Power BER Formats

NCP CA BER Type 10

CA BER Type 10 - Summary

Table 11-50 (Page 1 of 5). CA BER Type 10 Summary

| BER ID | Abend Code (NCP) | Event Description | Recovery or PGM Action | ALERT | ALARM |
|--------|------------------|---|------------------------|-------|-------|
| 10 | 0915 | <ul style="list-style-type: none"> CADS: Invalid ESC address used (EP or NEO are the CA owner) <ul style="list-style-type: none"> Mismatch between ESC addresses range defined in NCP/PEP sysgen and in MOSS CDF for involved CA. Program error (for example, possible over-write of control blocks where ESC values are kept) if found in normal operations BCCA: ESC addresses not allowed on this type of CA. | NCP re-IPL | NO | NO |
| 14 | 0910 | Address exception (AIO) (X'76' bit 0.0 or 1.0 ON) | NCP re-IPL | NO | NO |
| 16 | 0911 | Storage protect (AIO) (X'76' bit 0.1 or 1.1 ON) | NCP re-IPL | NO | NO |
| 18 | 0912 | Invalid CA selection in control program (attempt to select a non-installed CA). Control program issuing an output X'07' with either bit 0.2 or 0.3 set and bits 0.4, 0.6 indicating select bits for a CA that is not installed. | NCP re-IPL | NO | NO |
| 1B | 0913 | Invalid IOH/IOHI input to CA (for example input to register which cannot be read) X'7E' bit 0.5 ON | NCP re-IPL | NO | NO |
| 1C | 0914 | Output sequence issued in error to CA X'0D' bit 1.0 ON | NCP re-IPL | NO | NO |
| 1E | 0913 | Invalid IOH/IOHI output to CA output X'0D', X'0E', or X'0F' | NCP re-IPL | NO | NO |
| 1F | 0913 | Invalid IOH/IOHI output to CA (hardware detected) X'7E' bit 0.5 ON | NCP re-IPL | NO | NO |
| 34 | 091F | Level 3 IPL configuration check <ul style="list-style-type: none"> Stacked status cleared by initial select for the 1st time, or transfer of final status but not on the IPLing CA. built for the non-IPLing CA PRI built for the IPLing CA | NCP re-IPL | NO | NO |
| 35 | 0 | ESC address (from host) not within range (PEP on level 3 interrupt) Mismatch between ESC addresses range defined in NCP/PEP sysgen and in MOSS CDF for involved CA. | | NO | NO |
| 80 | 0 | Autoselection error: IOH IN X'0F' failed (X'09' and X'0A' contain 'FEFE') | Retry cmd in X'0F' | | |
| 80 | 0920 | Autoselection error (limit threshold) <ul style="list-style-type: none"> X'76' bit 0.4 ON for IOC1 time out, or X'76' bits 0.0 to 0.3 contain '0010'. | NCP re-IPL | NO | NO |
| 80 | 0 | Autoselection error (limit threshold) <ul style="list-style-type: none"> X'76' bit 0.4 ON for IOC1 time out, or X'76' bits 0.0 to 0.3 contain '0101'. | CA down | 50 | 50 |
| 80 | 0920 | Autoselection error (limit threshold) <ul style="list-style-type: none"> X'76' bit 0.4 ON for IOC1 time out, or X'76' bits 0.0 to 0.3 contain '0101'. | NCP re-IPL | NO | NO |

Table 11-50 (Page 2 of 5). CA BER Type 10 Summary

| BER ID | Abend Code (NCP) | Event Description | Recovery or PGM Action | ALERT | ALARM |
|--------|-------------------|---|---|-----------|-------|
| 81 | 0 | Failure to read X'08', or more than one CA in error from the X'08'. CA dropped from the autoselection chain bit 0 in CA X'08' byte 0 | CA down | 50 | 50 |
| 81 | 0 | <ul style="list-style-type: none"> CA dropped from the autoselection chain in CA X'08' byte 0, CAs bit = 0 Non-contiguous CAs in the autoselection chain All CAs on the IOC bus are removed from the chain. | | NO | NO |
| 82 | 0 | CA cannot be selected in level 1, not possible to issue IN CA X'08 | CA down | 50 | 50 |
| 82 | | CA cannot be selected in level 1 (last CA, no INN traffic) | NCP re-IPL | NO | 40 |
| 83 | | Autoselection error, 1 CA identified | | NO | NO |
| 84 | | Autoselection error, several errors | | NO | NO |
| 85 | 917 919 91A | CA not accessible (not attached, not initialized) Unresolved AIO Unresolved adapter error PIO error on a CA | | NO | NO |
| 86 | 917 919 91A | CA not operative Unresolved AIO Unresolved adapter error PIO error on a CA | | NO | NO |
| 87 | 917 919 91A | Interrupt from a disable CA Unresolved AIO Unresolved adapter error PIO error on a CA | | NO | NO |
| 88 | 917 919 91A | Unexpected level 1 in concurrent maintenance Unresolved AIO Unresolved adapter error PIO error on a CA | | NO | NO |
| 89 | 917 919 91A | Unexpected level 1 from CA CACM disconnect or with CA install in progress AIO threshold reached Unresolved interrupt PIO threshold reached | | NO | NO |
| 90 | 0 | CADS: Invalid ESC address (PEP or NEO are not the CA owner). ESC addresses not active on the CA. BCCA: ESC addresses not allowed on this type of CA. | Invalid ESC address (PEP or NEO are not the CA owner, NCP is the owner on an ESC address compare) | NCP retry | NO |
| NO | | | | | |
| 90 | 0 | Invalid ESC address (limit threshold) | CA down | 50 | 50 |
| 90 | | Invalid ESC address (last CA, no INN) All CAs have been disabled | NCP re-IPL | NO | NO |

Table 11-50 (Page 3 of 5). CA BER Type 10 Summary

| BER ID | Abend Code (NCP) | Event Description | Recovery or PGM Action | ALERT | ALARM |
|--------|------------------|---|------------------------|-------|-------|
| 91 | 0 | AIO error <ul style="list-style-type: none"> • X'75' bit 0.0 and 1.0 OFF • X'76' bit 0.4 ON for IOC1 time out • X'76' bit 0.5 or 1.5 for IOC1 bus IN parity error • X'76' bit 0.6 in both cases (AIO) • X'76' bits 0.0, 0.1, 0.2, 0.3 contain the IOC status at the time of error | NCP retry | NO | NO |
| 91 | 0 | AIO error (limit threshold) | CA down | 50 | 50 |
| 91 | | AIO error (last CA, no INN), all CAs have been disabled | NCP re-IPL | NO | NO |
| 92 | 0922 | Level 1 from CA during recovery (interrupt from a CA which is already being disabled by error recovery procedures as a result of level 1 checks). Indicates the probable failure of the disable sequence | NCP re-IPL | NO | 40 |
| 93 | 0 | Driver/receiver check X'0D' bit 1.6 or 1.7 ON | NCP retry | NO | NO |
| 93 | 0 | Driver/receiver check (limit threshold) | CA down | 50 | 50 |
| 93 | | Driver/receiver check (last CA, no INN) All CAs have been disabled | NCP re-IPL | NO | NO |
| 94 | 0 | Level 1 from a CA not generated active X'7E' bit 0.5 or 1.5 ON | NCP retry | NO | NO |
| 94 | 0921 | Level 1 from a CA not generated active (limit threshold) | NCP re-IPL | NO | NO |
| 96 | 0 | Channel bus IN check (X'0D' bit 1.3 or 1.5 ON) | NCP retry | NO | NO |
| 96 | 0 | Channel bus IN check (limit threshold) | CA down | 50 | 50 |
| 96 | | Channel bus IN check (last CA, no INN), all CAs have been disabled | NCP re-IPL | NO | 40 |
| 97 | 0 | PIO error (Input or output IOH failed) <ul style="list-style-type: none"> • X'76' bit 0.4 ON for IOC1 time out • X'76' bit 0.5 for IOC1 bus IN parity error • X'76' bit 0.6 in both cases | NCP retry | NO | NO |
| 97 | 0 | PIO error (limit threshold) | CA down | 50 | 50 |
| 97 | 091A | PIO error (last CA, no INN), all CAs have been disabled | NCP re-IPL | NO | 40 |
| 98 | 0 | Internal adapter error: <ul style="list-style-type: none"> • X'7E' bit 0.5 or 1.5 ON • X'0E' bits to indicate CAs Control program checks the level 3 instruction that failed. <ul style="list-style-type: none"> • If it is a valid IOH/IOHI, retry the instruction in the interrupted level • If it is not a valid IOH/IOHI, attempt to disable the CA | NCP retry | NO | NO |
| 98 | 09F0 | Internal adapter error : <ul style="list-style-type: none"> • Final status transfer. Not enough information available to recover when a data/status interrupt is pending during level 1 processing | NCP re-IPL | NO | NO |

Table 11-50 (Page 4 of 5). CA BER Type 10 Summary

| BER ID | Abend Code (NCP) | Event Description | Recovery or PGM Action | ALERT | ALARM |
|--------|------------------|---|------------------------|-------|-------|
| 98 | 09F1 | Internal adapter error : <ul style="list-style-type: none"> Status byte cleared (X'00' bit 0.6) Not enough information available to recover when an Initial Selection Interrupt is pending during level 1 processing. | NCP re-IPL | NO | NO |
| 98 | 0 | Internal adapter error (limit threshold) | CA down | 50 | 50 |
| 98 | | Internal adapter error (last CA, no INN), all CAs have been disabled | NCP re-IPL | NO | NO |
| 99 | 0 | Ground fault, X'0D' bit 1.4 ON | NCP retry | NO | NO |
| 99 | 0 | Ground fault (limit threshold) | CA down | 50 | 50 |
| 9A | 0920 | IOH failed in level 1, abort AIO recovery Control program cannot get the registers needed to determine the error | NCP re-IPL | NO | NO |
| 9B | 0920 | IOH failed in level 1, abort PIO recovery <ul style="list-style-type: none"> IOH required for the recovery failed twice in level 1, or Output IOH X'07' failed twice in level 1 | NCP re-IPL | NO | 40 |
| 9B | 0 | IN CA X'08' failed in level 1 | NCP retry | NO | NO |
| 9B | 0 | IN CA X'08' failed in level 1 (limit threshold) | | NO | NO |
| 9C | 0920 | IOH failed in level 1, abort ADP recovery | NCP re-IPL | NO | NO |
| 9D | 0 | CA microcode detected error <ul style="list-style-type: none"> X'0D' bit 0.1 ON Origin found in X'60' | CA down | 51 | 51 |
| 9E | 0 | Unresolved error on CA level 1 <ul style="list-style-type: none"> CA register X'0D' did not specify any adapter error bit See Specific Mechanism, page 11-13 | NCP retry | NO | NO |
| 9E | 0 | Unresolved error on CA level 1 (limit threshold) | CA down | 50 | 50 |
| 9E | | Unresolved error on CA level 1 (last CA, no INN) All CAs have been disabled | NCP re-IPL | NO | NO |
| 9F | 0925 | ESC interrupt (PEP/NEO are not CA owner) <ul style="list-style-type: none"> X'0F' bits 0.2 or 0.3 ON ESC address in X'3' byte 0 | NCP re-IPL | NO | NO |
| B1 | 0 | Unresolved CA level 3 <ul style="list-style-type: none"> Initial select interrupt (X'0F' bit 0.2), but no bit ON in X'00'. See Specific Mechanism, page 11-13 | NCP retry | NO | NO |
| B1 | 091C | Unresolved CA level 3 initial select interrupt (limit threshold) | NCP re-IPL | NO | NO |
| B2 | 0 | Unresolved CA level 3 <ul style="list-style-type: none"> Data/status interrupt (X'0F' bit 0.3), but no bit ON in X'02', and it is not a system reset (no bit in X'00'). | NCP retry | NO | NO |
| B2 | 091D | Unresolved CA level 3 data/status interrupt (limit threshold) | NCP re-IPL | NO | NO |
| B3 | 0 | Unresolved CA level 3 interrupt <ul style="list-style-type: none"> Level 3 but no initial select nor data status | NCP retry | NO | NO |
| B3 | 091E | Unresolved CA level 3 interrupt (limit threshold) | NCP re-IPL | NO | NO |

Table 11-50 (Page 5 of 5). CA BER Type 10 Summary

| BER ID | Abend Code (NCP) | Event Description | Recovery or PGM Action | ALERT | ALARM |
|--------|------------------|---|------------------------|-------|-------|
| B5 | 0927 | NCP cannot disable CA after an error detected on the CA. NCP exhausted disable count | NCP re-IPL | NO | NO |
| B6 | 0 | Inappropriate command (neither NOP nor TIO) on stacked initial status: PEP only (X'00' bit 0.5) | NCP retry | NO | NO |
| B6 | 0926 | Inappropriate command (neither NOP nor TIO) on stacked initial status (limit threshold) | NCP re-IPL | NO | NO |
| B7 | 091E | CA level 3 interrupt from an undefined CA <ul style="list-style-type: none"> CA installed and attached but not defined in NCP CA installed and attached but the box is defined as link-attached | NCP re-IPL | NO | NO |
| B8 | 091E | CA level 3 interrupt from a CA that is neither installed nor attached to that CCU | NCP re-IPL | NO | NO |
| B9 | 0 | Unresolved CA level 3 in concurrent diag mode | | | |
| BA | 091E | CA level 3 interrupt but the CA is not operational | NCP re-IPL | NO | NO |
| BB | | CA level 3 from a CA that is CACM disconnect (MOSS cancel CACM and reset CA) | | NO | NO |
| BC | | CA level 3 from a CA with install in progress (MOSS cancel CACM and reset CA) | | NO | NO |
| BD | 091E | CA level 3 from a CA ERP inoperative | NCP re-IPL | NO | NO |
| BE | 091E | CA level 3 from a disabled CA | NCP re-IPL | NO | NO |
| BF | 0 | Unresolved adapter level 1 interrupt (CA reg X'0E' did not specify a CA with the level 1 interrupt) | NCP retry | NO | NO |
| BF | 0919 | Unresolved adapter level 1 interrupt (limit threshold) | NCP re-IPL | NO | NO |

Note: In case of abend, NCP re-IPL is performed and the Alarm/Alert is generated when IPL is completed. Alert is triggered by MOSS BER ID 06, error code 05.

CA BER Type 10 (Detailed BER Display)

CA BER Type 10 - IDs 18, 1C, 1E, 80, 97, 9B: Format foC1, see page 11-124. Program level 1 generates one of the following BERs when an error occurs during a PIO operation on a channel.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:10 ID:hh <LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb CAVT:bbbbbbbb STAT:hhhh
X7E:hhhh X76:hhhh I:hhhh LAR:hhhhhhhh X76U:hhhh ETA:hhhh ADNO:hh
SWA:hhhh IAR:hhhhhh TA:hhhh TD:hhhh X8:hhhh X9:hhhh XA:hhhh
X50:hhhh X51:hhhh X52:hhhh
CAB:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
      hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
CAC:hhhh
X0:hhhh X1:hhhh X2:hhhh X3:hhhh X4:hhhh X5:hhhh X6:hhhh X7:hhhh
XB:hhhh XC:hhhh XD:hhhh XE:hhhh XF:hhhh

===>

F1:END F2:MENUE2 F3:ALARM F4:SUIHARY F5:LIST F7:PREVIOUS F8:NEXT

```

CA BER Type 10 - IDs 14, 16, 91, 9A: Format foC2, see page 11-124. Program level 1 generates one of the following BERs when an error occurs during an AIO operation with a channel.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:10 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
X7E:hhhh X76:hhhh X75:hhhh ETA:hhhh X76U:hhhh FPR:hhhhhhhh SWA:hhhh
X50:hhhh X51:hhhh X52:hhhh
CAB:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
      hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
CAC:hhhh
X0:hhhh X1:hhhh X2:hhhh X3:hhhh X4:hhhh X5:hhhh X6:hhhh X7: hhhh
XB:hhhh XC:hhhh XD:hhhh XE:hhhh XF:hhhh

===>

F1:END F2:HENUE2 F3:ALARM F4:SUIHARY F5:LIST F7:PREVIOUS F8:NEXT

```


CA BER Type 10 IDs 10, 1F, 87, 90, 92, 96, 98, 99, 9C, 9D, 9E, 9F

: Format foC3, see page 11-125. Program level 1 generates one of these BERs when a CA reports an error on its level 1.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:10 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
X7E:hhhh X76:hhhh ADNO:hh LAR:hhhhhhhh X76U:hhhh TA:hhhh SWA :hhhh
X60:hhhh X50:hhhh X51:hhhh X52:hhhh
CAB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
      hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh CAC:hhhh
X0:hhhh X1:hhhh X2:hhhh X3:hhhh X4:hhhh X5:hhhh X6:hhhh X7: hhhh
XB:hhhh XC:hhhh XD:hhhh XE:hhhh XF:hhhh

```

====>

F1:END F2:MENUE2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

CA BER Type 10 - IDs 34, 35, B1, B2, B6, BD, BE: Format foC4, see page 11-125. Program level 3 generates one of the following BERs when a CA request at level 3 remains unresolved.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:10 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC
CAVT:bbbbbbbb
X77:hhhh X7F:hhhh X0:hhhh X1:hhhh X2:hhhh X3:hhhh X4:hhhh X5:hhhh
X6:hhhh X7:hhhh XB:hhhh XC:hhhh XF:hhhh
CAB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
      hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
CAC:hhhh TA:hh

```

====>

F1:END F2:MENUE2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

When the registers are set to 'FF', the information they contain is not valid.

CA BER Type 10 - IDs 81, 82, 83, 84: Format foC5, see page 11-125. Program level 3 generates one of the following BERs when a CA request at level 3 remains unresolved.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:10 ID:hh<LOST:ddd CP-ABEID:hhhh>
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbbb CAVT:bbbbbbbbb STAT:hhhh
X7E:hhhh X76:hhhh I:hhhh LAR:hhhhhhhhh X75:hhhh X76U:hhhh ETA:hhhhhhhhh
ADNO:hh
SWA:hhhh IAR:hhhhhhh TA:hhhh TD:hhhh X8:hhhh XE:hhhh XF:hhhh
FPR:hhhhhhhhh
CAB:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
      hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh

====>

F1:END F2:MENU2 F3:ALARH F4:SUMHARY F5:LIST F7:PREVIOUS F8:NEXT

```

CA BER Type 10 - IDs 85, 86, 88, 89, B3, B7, B8, BA, BB, BC, BF: Format foC6, see page 11-125. Program level 3 generates one of the following BERs when a CA request at level 3 remains unresolved.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:10 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC
CAVT:bbbbbbbbb
X77:hhhh X7F:hhhh
TA:hhhh STAT:hhhh CCU=INPUT-X57:hhhh CCU=OUTPUT-X57:hhhh XF:hhhh

====>

F1:END F2:MENU2 F3:ALARH F4:SUMHARY F5:LIST F7:PREVIOUS F8:NEXT

```


CA BER Type 10 - Field Description

| Table 11-51. CA BER type 10 Field Description | | |
|---|---|------------|
| Field Name | Meaning | Refer to |
| ADNO | <ul style="list-style-type: none"> field ADNO for PIO operation field XE for CA error reported at level 1 field X75 for AIO operation field XF for CA error reported at level 3. | |
| CAB | CA address (5 to 8), as used by NCP/PEP in its control blocks (not to be confused with ESC or NSC address). X'30' bytes of fields from the CAB, from CABEND up to and including CABXR6F. For PEP the fields CASEL through TERMADR are included from the PEP CHCB (X'10' bytes). The remaining space is padded with X'FF' for PEP. | (*) |
| CAC | Channel adapter contact control flags. | (*) |
| CAVT | CAVT flag | (*) |
| STAT | Auto selection chain status, input X'9'. | (*) |
| CCU | X'57' - Input CA command LS reg (same for output). | Page 11-92 |
| INPUT X57 | | |
| ETA | TA field of IOH failure in level 1. | (*) |
| F | Indicator flag byte (indicates a byte expansion follows) | (*) |
| I | First two bytes of instruction. | |
| IAR | IAR of interrupt level. | Page 2-38 |
| LAR | Lagging address register (X'74'). | Page 2-38 |
| SWA | Unused | |
| TA | IOHI image -- (TA: hhhh means data bytes 0 and 1). | Page 3-31 |
| TD | IOHI image -- TD data adapter specific bytes (TD: hhhh means data bytes 0 and 1). | Page 3-31 |
| X0-XF | Channel adapter registers | |
| XF | X'F' - CA level 3 interrupt request | Chapter 7 |
| X0 | X'0' (Initial selection) | Chapter 7 |
| X3M | CA cycle steal fixed pointer register. | Page 2-20 |
| X50 | X'50' - Adapter bus control module check register | (*) |
| X51 | X'51' - Channel A control module check register | (*) |
| X52 | X'52' - Channel B control module check register | (*) |
| X60 | X'60' - Microcode-detected error code | (*) |
| X7E | X'7E' - CCU level 1 interrupt. | Page 2-37 |
| X7F | X'7F' - Interrupt request reg - CCU level 2, 3, and 4. | Page 2-38 |
| X74 | X'74' - Cycle steal control word register. | Page 2-29 |
| X75 | X'75' - LAR bytes (see CAn). | Page 2-30 |
| X76 | X'76' - IOC error summary register. | Page 2-31 |
| X76U | X'76' - Cause of error not found (PIO to read error register failed). | Page 2-31 |
| X77 | X'77' - Interrupt request reg - adapter levels 2 and 3. | Page 2-33 |
| X79 | X'79' - Utility. | Page 2-34 |

(*) For software information on BERs originated by NCP/PEP, refer to the associated product documentation.

CA BER Type 10 - Formats

| Format f0C1 | | Format foC2 | |
|-----------------------------|--------------------|--------------------|-------------------|
| IDs: 18, 1C, 1E, 80, 97, 9B | | IDs 14, 16, 91, 9A | |
| Bytes | Meaning | Bytes | Meaning |
| 1-27 | Header | 1-27 | Header |
| 28-29 | TYPE-ID | 28-29 | TYPE-ID |
| 30 | LOST | 30 | LOST |
| 31-32 | Abend | 31-32 | Abend |
| 33-34 | X7E | 33-34 | X7E |
| 35-36 | X76 | 35-36 | X76 |
| 37-38 | I | 37-38 | X75 |
| 39-42 | LAR | 39-40 | Unused |
| 43-44 | STAT | 41-42 | ETA |
| 45-46 | X76U | 43-44 | Unused |
| 47-48 | ETA | 45-46 | X76U |
| 49 | Unused | 47-50 | FPR |
| 50 | ADNO | 51 | Flag |
| 51 | Flag | 52 | Unused |
| 52 | CAVT | 53-54 | SWA |
| 53-54 | SWA error register | 55-68 | Unused |
| 55 | Unused | 69-70 | X50 (*) |
| 56-58 | IAR int level | 71-72 | X51 (*) |
| 59-60 | TA | 73-74 | X52 (*) |
| 61-62 | TD | 75-122 | CAB (*) |
| 63-68 | Unused | 123-124 | CAC (*) |
| 63-64 | X8 ← for | 125-150 | CA regs X'0'-X'F' |
| 65-66 | X9 → ID 80/9B | | (*) |
| 67-68 | XA → | | |
| 69-70 | X50 (*) | | |
| 71-72 | X51 (*) | | |
| 73-74 | X52 (*) | | |
| 75-122 | CAB (*) | | |
| 123-124 | (CAC) | | |
| 125-150 | CA Regs X'0'-X'F' | | |

(*) means that if contents are FEF EFE...FE, data is invalid.

Figure 11-20 (Part 1 of 3). CA BER Formats

| Format f0C3 | |
|---|-------------------|
| IDs: 10 1F 87 90 92 96 98 99 9C 9D 9E 9F | |
| Bytes | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | LOST |
| 31-32 | Abend |
| 33-34 | X7E |
| 35-36 | X76 |
| 37 | ADNO |
| 38 | Unused |
| 39-42 | LAR |
| 43-44 | Unused |
| 45-46 | X76U |
| 47-48 | TA |
| 49-50 | Unused |
| 51 | Flag |
| 52 | Unused |
| 53-54 | SWA |
| 55-68 | Unused |
| 67-68 | X60 ID=9D/1F |
| 69-70 | X50 (*) |
| 71-72 | X51 (*) |
| 73-74 | X52 (*) |
| 75-76 | Unused |
| 77-124 | CAB (*) |
| 125-126 | CAC |
| 127-152 | CA Regs X'0'-X'F' |

| Format foC4 | |
|---------------------------|----------|
| IDs: 34 35 B1 B2 B6 BD BE | |
| Bytes | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | LOST |
| 31-32 | Abend |
| 33-34 | X77 |
| 35-36 | X7F |
| 37-38 | X0 |
| 39-40 | X1 |
| 41-42 | X2 |
| 43-44 | X3 |
| 45-46 | X4 |
| 47-48 | X5 |
| 49-50 | X6 |
| 51-52 | X7 |
| 53-54 | XB |
| 55-56 | XC |
| 57-58 | XF |
| 59-106 | CAB/CHCB |
| 107-108 | CAC |
| 109 | TA |
| 110 | Unused |
| 111 | Flag |

(*) means that if contents are FEF EFE...FE, data is invalid.

Figure 11-20 (Part 2 of 3). CA BER Formats

| Format f0C5 | |
|-------------------------------------|-----------------|
| IDs: 81 to 84 | |
| Bytes | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | LOST |
| 31-32 | Abend |
| 33-34 | X7E |
| 35-36 | X76 |
| 37-38 | I |
| | 0 for IDs 81/82 |
| 39-42 | LAR |
| 43-44 | X75 |
| | 0 for IDs 83/84 |
| 45-46 | X76U |
| 47-48 | ETA |
| 49 | Unused |
| 50 | ADNO |
| 51 | Flag |
| 52 | CAVT |
| 53-54 | SWA |
| 56-58 | IAR |
| | 0 for IDs 81/82 |
| 59-60 | TA |
| 61-62 | TD |
| Only for IDs 81,83 (0 for 82,84) | |
| 63-64 | X'08' |
| 65-66 | STAT |
| 67-68 | X'0E' |
| 69-70 | X'0F' |
| 71-74 | FPR |
| 75-122 | CAB |

| Format foC6 | |
|---------------------------------------|----------------|
| IDs: 85 86 88 89 B3 B7 B8 BB BC BF | |
| Bytes | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | LOST |
| 31-32 | Abend |
| 33-34 | X77 |
| 35-36 | X7F |
| 37-38 | STAT |
| 39-40 | CCU-INPUT X57 |
| 41-42 | CCU-OUTPUT X57 |
| 43 | TA |
| 44 | CAVT |
| 45-46 | X0F |

Figure 11-20 (Part 3 of 3). CA BER Formats

NCP TSS/HPTSS BER Type 11

TSS/HPTSS BER Type 11 - Summary

| Table 11-52 (Page 1 of 4). TSS/HPTSS BER Type 11 Summary | | | | | |
|--|------------------|---|---------------------------|-------|-------|
| BER ID | ABEND Code (NCP) | Event Description | Recovery or PGM Action | ALERT | ALARM |
| 14 | 0930 | Address exception (AIO) X'76' bit 0.0 or 1.0 ON | NCP re-IPL | NO | NO |
| 16 | 0931 | Storage protect (AIO) X'76' bit 0.1 or 1.0 ON | NCP re-IPL | NO | NO |
| 18 | 0 | <ul style="list-style-type: none"> IOH/IOHI issued to non operational Line Adapter (X'7E' bit 0.2 or 0.6 ON) IOC bus check in error status type 1 of CSP : bit 0.1 and 0.5 ON (X'02' bits 0.1 and 0.5) Non-operational cause is given by MCT bits bits OFF for non-attached, non-installed, non-operational or down. | | NO | NO |
| 1B | 0933 | Invalid IOH input to scanner X'7E' bit 0.2 or 0.6 ON. Origin given in error status type 1 of CSP, bit 1.7 ON | NCP re-IPL | NO | NO |
| 1C | 0 | Line command reject Error status type 3 of CSP, bit 1.0 = 1 | Line down | 43 | 43 |
| 1E | 0 | <ul style="list-style-type: none"> Invalid IOH output to scanner (pgm reset done) X'7E' bit 0.2 or 0.6 ON Undefined IOH instruction sent to the CSP Origin given in error status type 3 of CSP (bit 1.1 ON). | LSS/HSS down | 60 | 60 |
| 1E | 0 | Scanner disconnected due to 'F2' command sent by NCP. <ul style="list-style-type: none"> X'7E' bit 0.2 or 0.6 ON Error status type 3 of CSP = X'8140' | LSS/HSS down | 60 | 60 |
| 26 | | SCTL/DMA storage protect/address exception <ul style="list-style-type: none"> LCS = 'DC' ELCS bits 4,5,6 = 000 | Line down HSS down | 73 | 73 |
| 91 | 0 | Scanner AIO error <ul style="list-style-type: none"> X'75' bit 0.0 or 1.5 ON X'76' <ul style="list-style-type: none"> bit 0.4 ON for IOC1 time out bit 0.5 ON for IOC1 bus in parity error X'76' bit 0.6 ON in both cases (AIO) X'76' bits 0.0, 0.1, 0.2, 0.3 contain the IOC internal status at time of error. BER file adapter status = Error status type 2 of CSP. | TSS μ code retry | 63 | 63 |
| 92 | 0 | Scanner AIO error unresolved is generated when the CCU register X'76' = "0200" (IOC1) or "0002" (IOC2) with no indication if time-out ("uA") or bus-in parity check ("u6"). | TSS μ code retry | NO | NO |
| 92 | 0 | Scanner AIO error unresolved (limit threshold) | LSS/HSS down | 63 | 63 |
| 93 | 0 | Scanner AIO invalid CSCW <ul style="list-style-type: none"> X'75' bit 0.0 or 1.5 ON X'76' bits 0.2 and 0.6 ON | TSS μ code retry | NO | NO |
| 93 | 0 | Scanner AIO invalid CSCW (limit threshold) | LSS/HSS down | 63 | 63 |
| 94 | | DMA/cycle steal error on SET mode (LA level 1) | | 43 | 43 |

Table 11-52 (Page 2 of 4). TSS/HPTSS BER Type 11 Summary

| BER ID | ABEND Code (NCP) | Event Description | Recovery or PGM Action | ALERT | ALARM |
|--------|------------------|--|------------------------|-------|-------|
| 95 | 0 | Scanner hardstop <ul style="list-style-type: none"> • X'7E' bit 0.2 or 0.6 ON BER file adapter status = Error status type 3H of CSP, bit 0.0 = 0. | LSS/HSS down | 63 | 63 |
| 96 | 0 | TSS disconnected on manual request (following request from MOSS) <ul style="list-style-type: none"> • X'7E' bit 0.2 or 0.6 ON • Error status type 3, bit 0.7 ON • Ext register X'01' bit 5 ON | Scanner OFF line | B8 | B8 |
| 96 | 0 | HPTSS disconnected on manual request (following request from MOSS) <ul style="list-style-type: none"> • X'7E' bit 0.2 or 0.6 ON • Error status type 3, bit 0.7 ON • Ext register X'01' bit 5 ON | Scanner OFF line | BA | BA |
| 97 | 0 | Scanner PIO error-output IOH/IOHI <ul style="list-style-type: none"> • X'75' bit 0.0 or 1.5 ON • X'76' <ul style="list-style-type: none"> — bit 0.4 ON for IOC1 time out — bit 0.5 ON for IOC1 bus in parity error X'76' bit 0.6 ON in both cases BER file adapter status = Error status type 1 of CSP. | NCP retry | NO | NO |
| 97 | 0 | Scanner PIO error-output IOH/IOHI before threshold. BER file adapter status = Error status type 1 of CSP. | LSS/HSS down | 63 | 63 |
| 98 | 0 | Scanner PIO error-output IOH/IOHI (limit threshold) BER file adapter status = Error status type 1 of CSP. | LSS/HSS down | 63 | 63 |
| 99 | 0 | Scanner adapter error X'7E' bit 0.2 or 0.6 ON BER file adapter status = Error status type 3 of CSP. | LSS/HSS down | 63 | 63 |
| 9A | 0 | Scanner adapter error unresolved <ul style="list-style-type: none"> • First get error status failed but retry was succesful. • Error status has value at time of failure. | NCP retry | NO | NO |
| 9A | 0 | Get error status unresolved ON all lines. Error status filled by X'FEFE'. | | NO | NO |
| 9B | 0 | Interrupt from disconnected scanner Level 1 interrupt presented to NCP/PEP while the scanner is disconnected (X'01' bit 5 ON). X'7E' bit 0.2 or 0.6 ON | | NO | NO |
| 9B | 093A | Interrupt from disconnected scanner (limit threshold) | NCP re-IPL | NO | NO |
| 9C | 0 | Scanner PIO error input on get line ID (see BER 11 97 for general PIO errors) | NCP retry | NO | NO |
| 9C | 0937 | <ul style="list-style-type: none"> • Scanner PIO error input on get line ID (limit threshold) • Retry on get line ID failed. • Get error status unresolved on all lines. | NCP re-IPL | NO | NO |
| 9D | 0 | Scanner microcode error. BER file adapter status = status M is an error code for PE only. | LSS/HSS down | 63 | 63 |
| 9E | 0 | Get error status command failed (IOC error) during NCP LVL1 process either ON Line Adapter LVL1 or on PIO Get Line ID error. | | NO | NO |
| A1 | 0 | Unresolved level 2 interrupt. If spurious retry count (the interrupt occurred on a non-defined line) | | NO | NO |

Table 11-52 (Page 3 of 4). TSS/HPTSS BER Type 11 Summary

| BER ID | ABEND Code (NCP) | Event Description | Recovery or PGM Action | ALERT | ALARM |
|--------|------------------|--|------------------------|-------|-------|
| A1 | 0936 | Unresolved level 2 interrupt (limit threshold) See Specific Mechanism, page 11-13 | NCP re-IPL | NO | NO |
| A2 | 0 | Internal FESL error reported via level 2 <ul style="list-style-type: none"> • X'77' bit 0.1 ON • LCS = C0, C2, C4, C6, C8, D0, D2, D4, D6, D8 | Line down | 43 | 43 |
| A2 | 0 | Internal FESH error reported via level 2 <ul style="list-style-type: none"> • X'77' bit 0.1 ON • LCS = C0, C2, C4, C6, C8, D0, D2, D4, or D8 | Line down | 43 | 43 |
| A2 | 0 | Internal FESH error reported via level 2 <ul style="list-style-type: none"> • X'77' bit 0.1 ON • LCS = CE. Local clock failure. | Line down | 43 | 43 |
| A3 | 0 | Internal MUX error reported via level 2 <ul style="list-style-type: none"> • X'77' bit 0.1 ON • LCS = CA | Line down | 43 | 43 |
| A3 | 0 | Internal MUX/LIC error reported via level 2 <ul style="list-style-type: none"> • X'77' bit 0.1 ON (limit threshold) • LCS = CC. | Line down | 43 | 43 |
| A3 | 0 | Internal LIC error reported via level 2 <ul style="list-style-type: none"> • X'77' bit 0.1 ON • LIC failing or not plugged. • LCS = CE. | Line down | 43 | 43 |
| A3 | 0 | Internal LIC error reported via level 2 <ul style="list-style-type: none"> • X'77' bit 0.1 ON • Line cannot be accessed by configuration. • LCS = DE. | Line down | 43 | 43 |
| A3 | 0 | Internal FESH error reported via level 2 <ul style="list-style-type: none"> • X'77' bit 0.1 ON • Line not accessible, a line is already active LCS = 'DE' | Line down | 43 | 43 |
| A4 | 0 | Time out on any command, except F5. F5 command sent to the scanner, back up timer in NCP/PEP level 3 expired before receiving level 2 from scanner to process it. | Line down | NO | NO |
| A4 | 0 | Transient FESL error reported at level 2, ELCS bit 7 ON | TSS μ code retry | NO | NO |
| A5 | 0 | Transient MUX/LIC error reported at level 2, ELCS bit 7 OFF | TSS μ code retry | NO | NO |
| A6 | 0 | SCTL/DMA internal error, or BU LCS = 'DC' <ul style="list-style-type: none"> • ELCS bits 4,5,6 = 001 | Line down | 73 | 73 |
| A6 | 0 | SCTL/DMA internal error <ul style="list-style-type: none"> • LCS = 'DC' • ELCS bits 4,5,6 = 001 | Line down | 73 | 73 |
| A7 | 0 | SCTL/DMA interface (main bus) error <ul style="list-style-type: none"> • LCS = 'DC' • ELCS bits 4,5,6 = 010 | Line down | 73 | 73 |
| A8 | 0 | DMA reported error <ul style="list-style-type: none"> • LCS = 'DC' • ELCS bits 4,5,6 = 011 | Line down | 73 | 73 |

Table 11-52 (Page 4 of 4). TSS/HPTSS BER Type 11 Summary

| BER ID | ABEND Code (NCP) | Event Description | Recovery or PGM Action | ALERT | ALARM |
|--------|------------------|--|------------------------|-------|-------|
| A9 | 0 | DMA parity check or DMA time out <ul style="list-style-type: none"> • LCS = 'DC' • ELCS bits 4,5,6 = 100 | Line down | 73 | 73 |
| AA | 0 | FESH/DMA interface error <ul style="list-style-type: none"> • LCS = 'DC' • ELCS bits 4,5,6 = 101 | Line down | 73 | 73 |
| AB | | Internal LIC error level 2 | Line down | 43 | 43 |
| B1 | 0 | Scanner command time out on F5. Command F5 sent to the scanner, back up timer in NCP/PEP level 3 expired before receiving level 2 from scanner to process it. | Line down | 43 | 43 |

Note: In case ofabend. NCP re-IPL is performed and the Alarm/Alert is generated when IPL is completed. Alert is triggered by MOSS BER ID 06, error code 05.

TSS/HPTSS BER Type 11 (Detailed BER Display)

TSS/HPTSS BER Type 11 - ID 14, 16, 91, 92, 93: Format foT1, see page 11-136. Program level 1 generates one of the following BERs when an error occurs during an AIO operation on a scanner.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:11 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                                <REF. CODE IN CHAR.> CCCCCCCC

F:bbbbbbbb
X7E:hhhh  X76:hhhh  X75:hhhh  ETA:hhhh  LAS:hhhh  X76U:hhhh  SPR:hhhhhhhh
SWA:hhhh  LAR:hhhhhhhh

===>

F1:END F2:MENU2 F3:ALARM F4:SUNMARY F5:LIST F7:PREVIOUS F8:NEXT

```

TSS/HPTSS BER Type 11 - IDs 18, 1B, 97, 98, 9C, 9E: Format foT2, see page 11-136. Program level 1 generates one of these BERs when an error occurs during a PIO operation on a scanner.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:11 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                                <REF. CODE IN CHAR.> CCCCCCCC

F:bbbbbbbb X7E:hhhh X76:hhhh I:hhhh LAR:hhhhhhhh
LAS:hhhh  X76U:hhhh  ETA:hhhh  SWA:hhhh  IAR:hhhhhh  TA:hhhhhh  TD:hhhh
IOB/LXB:hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
          hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
CCB:hhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
          hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh
AXB:hhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhhhhh hhhhh hh
SCB:hhhh  hhhh  hhhh  hhhh  hhhh  hhhh  hhhh  hhhh  hh
PSA:hhhh  hhhh  hhhh  hhhh  hhhh  hhhh  hhhh  hhhh  hhhh  hhhh  hhhh  hhhh

===>

F1:END F2:MENU2 F3:ALARM F4:SUNMARY F5:LIST F7:PREVIOUS F8:NEXT

```


TSS/HPTSS BER Type 11 - IDs 1E, 95, 96, 99, 9A, 9B, 9D: Format foT3, see page 11-136. Program level 1 generates one of these BERs when an error is reported by a scanner on level 1.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:11 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
X7E:hhhh X76:hhhh ADH0:hh LAS:hhhh X76U:hhhh SWA:hhhh LAR:hhhhhhhh

===>

F1:END F2:MENU2 F3:ALARM F4:SUNMARY F5:LIST F7:PREVIOUS F8:NEXT

```

TSS/HPTSS BER Type 11 - ID A1: Format foT4, see page 11-137. These BERs are generated on a level 2 unresolved interrupt.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:11 ID:hh<LOST:ddd CP-ABEND:hhhh>
<Error description>                                <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
TA:hh TD:hh NW:hhhh IDR:hhhh LNVT:hhhhhhhh LCS:hh
PSA:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
CNT:hhhh

OVERRIDE FLAG WITH NEW HEXADECIMAL VALUE
===>

F1:END F2:MENU2 F3:ALARM F4:SUNMARY F5:LIST F7:PREVIOUS F8:NEXT

```

TSS/HPTSS BER Type 11 - ID B1: Format foT4, see page 11-137. These BERs are generated on a level 2 unresolved interrupt.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:11 ID:hh<LOST:ddd CP-ABEND:hhhh>
<Error description>                                <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
TA:hh TD:hh NW:hhhh IDR:hhhh LNVT:hhhhhhhh LCS:hh
PSA:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh

OVERRIDE FLAG WITH NEW HEXADECIMAL VALUE
===>

F1:END F2:MENU2 F3:ALARM F4:SUNMARY F5:LIST F7:PREVIOUS F8:NEXT

```


TSS/HPTSS BER Type 11 ID 26, A2, A3, A4, A5, A6, A7, A8, A9, AA, AB: Format foT5, see page 11-136. Program level 2 generates one of these BERs when a scanner internal error or a transient line error is detected.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:11 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbb TA:hh TD:hh NW:hhhh IDR:hhhh
PSA:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
IOB/LXB:hhhhhhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
CCB:hhhhhhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
      hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
AXB:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
SAT:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
SCB:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
CSC:hhhh CNT:hhhh

```

===>

F1:END F2:MENUE2 F3:ALARM F4:SUNHARY F5:LIST F7:PREVIOUS F8:NEXT

Note: Lost and CP abend fields are displayed when applicable.

TSS/HPTSS BER Type 11 ID 94, 1C: Format foT6, see page 11-136. Program level 1 generates this BER when a command reject is reported by a scanner on level 1 (control program error).

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:11 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbb LNVT:hhhh PSA:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
SCF:hh LSTAT:hh LAS:hhhh CR1:hh CR2:hh IAR:hhhhhhhh TA:hh TD:hh
IOB/LXB:hhhhhhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
CCB:hhhhhhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
      hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
AXB:hhhhhhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh
SCB:hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh hhhh

```

===>

F1:END F2:MENUE2 F3:ALARM F4:SUNHARY F5:LIST F7:PREVIOUS F8:NEXT

TSS/HPTSS BER Type 11 - Field Description

| Table 11-53 (Page 1 of 2). TSS/HPTSS BER Type 11 Field Description | | |
|--|--|-------------------------|
| Field Name | Meaning | Refer to |
| ADNO | CS number (decimal) in error description field. This CS number is derived from: <ul style="list-style-type: none"> field TA for PIO operation <ul style="list-style-type: none"> for CS error reported at level 2 for CA error reported at level 3. field X75 for AIO operation. field CSPA for CS error reported at level 1. <p>If no n is specified (blank CS), problem isolation by program was not possible.</p> | |
| LAS or L-STAT | LA adapter status <ul style="list-style-type: none"> LA Error status type 1: CSP error status 1 LA Error status type 2: CSP error status 1 LA Error status type 3/H: CSP error status 1 | Chapter 4 |
| CSPA | CSP address used by NCP/PEP (see CSn and LINEnn). | |
| ETA | TA field of IOH failure in level 1. | |
| IDR | Get line ID response. | Chapter 4 |
| F | Indicator flag (indicates a byte expansion follows) | (*) |
| SWA | Unused | |
| CR1 | First command sent to scanner | |
| CR2 | Second command sent to scanner | |
| LAR | Lagging address register- | Page 2-38 |
| SPR | LA shared pointer register X'3F' or X'6F'. | |
| CSC | Configuration status control flag (contains X'FFFF' for PEP, BSC/SS and BNN lines). | |
| CNT | Repetition count (BER flooding). Number of times the BER appeared. | |
| SCF | Secondary control field. | |
| I | First two bytes of instruction. | |
| IAR | IAR of interrupt level. | |
| LCS | Line control status. | Chapter 4 and page 5-31 |
| LINEnn | Line number (0 to 31) within the CS (in error description line). | |
| LNVT | Line vector table. | Chapter 4 |
| LOST | Lost record count (LRC). | (*) |
| NW | Network address (NCP) or CA number and ESC (PEP). | (*) |
| IOB/LXB | X'24' bytes of LXB (for SDLC lines) or IOB (for BSC/SS lines) control blocks. This area is padded with X'FF' for PEP. | (*) |
| CCB | X'40' bytes of data from the CCB control block. <ul style="list-style-type: none"> If PEP, the fields are CCBL2 through CCBPOLL inclusive. If PEP, the fields are CCBTROPT through CCBXPTR inclusive. | (*) |
| AXB ACB TRACE | X'E' bytes of data from the AXB control block from AXBFCTL through AXB+X'15' (ACB trace area). For PEP, this area contains the CCB extension starting at the PEP CCB + X'60'. | (*) |
| AXB PSA | X'11' bytes of data from the PSA trace area of the AXB control block (AXBASSCF through AXBTROFF). For PEP, this area contains the remaining portion of the CCB extension padded with X'F'. | (*) |
| SCB | X'19' bytes of the SCB/CUB from SCBSSCF (CUBSSCF) through SCBRTCNT (CUBRTCNT) inclusively. For BSC/SS lines and for PEP, this area is padded with X'FF's. | (*) |
| SAT | 17 bytes of PSA trace area for NCP. For PEP, this area contains the EP CCB extension. | (*) |
| SCBCSCF | Configuration station control flags (NCP only). | (*) |

Table 11-53 (Page 2 of 2). TSS/HPTSS BER Type 11 Field Description

| Field Name | Meaning | Refer to |
|------------|--|-----------|
| PSA | Parameter area (16 bytes)-status area (12 bytes). The byte contents of the PSA depend on the current command (CCMD). | Chapter 4 |
| TA | IOH/IOHI image -- TA data registers X'50', X'70' (TA: hh means TA data byte 0) (see CSn and LINEnn). | Chapter 4 |
| TD | IOH/IOHI image -- TD data adapter specific bytes (TD: hh means TD data byte 1). | Chapter 4 |
| X3F | CSP shared pointer register. | Page 2-25 |
| X74 | X'74' - LAR bytes (See CSn and LINEnn). | Page 2-25 |
| X75 | X'75' - Cycle steal control word register. | Page 2-25 |
| X76 | X'76' - IOC error summary register. | Page 2-25 |
| X76U | X'76' - Cause of error not found (PIO to read error register failed). | Page 2-25 |
| X77 | X'77' - Interrupt request register adapter levels 2 and 3 | Page 2-25 |
| X79 | X'79' - Interrupt level. | Page 2-25 |
| X7E | X'7E' - CCU level 1 interrupt. | Page 2-25 |
| X7F | X'7F' - Interrupt request register CCU levels 2, 3, and 4 | Page 2-25 |

Note: All values are in hexadecimal notation (X'0' to X'F'), except for:

- Flag bytes F and CS STAT, which are in bit format (8 or 16 bits, 0 or 1)
- The error description line with a CS number and line number, which are in decimal notation.

(*) For software information on BERs originated by NCP/PEP, refer to the associated product documentation.

TSS/HPTSS BER Type 11 - Formats

| Format: foT1 | |
|--------------------|---------|
| ID: 14 16 91 92 93 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | LOST |
| 31-32 | Abend |
| 33-34 | X7E |
| 35-36 | X76 |
| 37-38 | X75 |
| 39-40 | Unused |
| 41-42 | ETA |
| 43-44 | LAS |
| 45-46 | X76U |
| 47-50 | SPR |
| 51 | Flag |
| 52 | Unused |
| 53-54 | SWA |
| 55-58 | LAR |

| Format: foT2 | |
|------------------------|---------|
| IDs: 18 1B 97 98 9C 9E | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | LOST |
| 31-32 | Abend |
| 33-34 | X7E |
| 35-36 | X76 |
| 37-38 | I |
| 39-42 | LAR |
| 43-44 | LAS |
| 45-46 | X76U |
| 47-48 | ETA |
| 49-50 | Unused |
| 51 | Flag |
| 52 | Unused |
| 53-54 | SWA |
| 55 | Unused |
| 56-58 | IAR |
| 59-60 | TA |
| 61-62 | TD |
| 63-64 | PSA |
| 65-66 | Unused |
| 67-102 | IOB/LXB |
| 103-166 | CCB |
| 167-197 | AXB |
| 198 | Unused |
| 199-215 | SCB |
| 216 | Unused |
| 217-242 | PSA |
| + 63-64 | |

Figure 11-21 (Part 1 of 2). TSS/HPTSS BER Formats

| Format: foT3 |
|--------------|
|--------------|

| ID: 1E 95 96 99 9A 9B 9D | |
|--------------------------|----------|
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | LOST |
| 31-32 | Abend |
| 33-34 | X7E |
| 35-36 | X76 |
| 37 | ADNO |
| 38-42 | Unused |
| 43-44 | LAS |
| 45-46 | X76U |
| 47-50 | Unused |
| 51 | F |
| 52 | TSS Flag |
| 53-54 | SWA |
| 55-58 | LAR |

| Format: foT4 |
|--------------|
|--------------|

| ID: A1 B1 | |
|-----------|------------------|
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | LOST |
| 31-32 | Abend |
| 33 | F |
| 34 | Unused |
| 35-36 | IDR |
| 37-64 | PSA |
| 56 | LCS |
| 65 | TA byte 0 |
| 66 | TD byte 1 |
| 67-68 | NW |
| 69-72 | LNVT |
| 73-108 | IOB/LXB |
| 109-172 | CCB |
| 173-186 | AXB ACB Trace |
| 187-203 | AXB PSA Trace |
| 204-219 | SCB |
| 220 | SCBCSCF |
| 221-222 | Count (A1 only) |

| Format: foT5 |
|--------------|
|--------------|

| IDs: 26 A2 A3 A4 A5 A6 A7 A8 A9 AA AB | |
|--|-----------|
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | LOST |
| 31-32 | Abend |
| 33 | Flag |
| 34 | Unused |
| 35-36 | IDR |
| 37-64 | PSA |
| 65 | TA byte 0 |
| 66 | TD byte 1 |
| 67-68 | NW |
| 69-100 | IOB/LXB |
| 101-164 | CCB |
| 165-166 | AXB (IOB) |
| + | |
| 169-180 | |
| 167-168 | Unused |
| 181-197 | SAT trace |
| 198-199 | Unused |
| 215-216 | SCB |
| + | |
| 200-214 | |
| 216-217 | CSC |
| 218-219 | Count |

| Format: foT6 |
|--------------|
|--------------|

| ID: 94 1C | |
|-----------|-------------------|
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | LOST |
| 31-32 | Abend |
| 33 | F |
| 34 | Interrupt level 1 |
| 35-36 | LNVT |
| 37-52 | PSA |
| 53 | SCF |
| 54 | LSTAT |
| 55-56 | LAS |
| 57 | CR1 |
| 58 | CR2 |
| 59-62 | IAR |
| 63-64 | Unused |
| 65 | TA |
| 66 | TD |
| 67-98 | LXB/IOB |
| 99-162 | CCB |
| 163-192 | AXB |
| + 195 | |
| 193-194 | Unused |
| 196 | Unused |
| 197-213 | SCB |

Figure 11-21 (Part 2 of 2). TSS/HPTSS BER Formats

NCP/PEP BER, Type 12

NCP/PEP BER Type 12 Summary

The following BERs are software errors detected by the CCU hardware. Software errors detected by software checking mechanisms (logical errors) lead to control program abends.

| Table 11-54. NCP/PEP BER Type 12 Summary | | | | | |
|--|------------------|---|------------------------|-------|-------|
| BER ID | Abend Code (NCP) | Event Description | Recovery or PGM Action | ALERT | ALARM |
| 11 | 000A | IN/OUT or IOH/IOHI on level 5 IAR not 0, retry not possible. | NCP re-IPL | NO | NO |
| 12 | 001B | Invalid operation code • X'7E' bit 0.4 ON | NCP re-IPL | NO | NO |
| 13 | 0950 | Address exception - I fetch • X'7E' bit 1.1 ON | NCP re-IPL | NO | NO |
| 14 | 0951 | Address exception - I execution • X'7E' bit 1.3 ON | NCP re-IPL | NO | NO |
| 15 | 0952 | Storage protect - I fetch • IAR not 0 • X'7E' bit 1.2 ON | NCP re-IPL | NO | NO |
| 16 | 0953 | Storage protect - I execution • X'7E' bit 1.4 ON | NCP re-IPL | NO | NO |
| 17 | 0954 | Level 5 branch to storage location 0. IAR = 0. | NCP re-IPL | NO | NO |
| 18 | 0955 | User (non NCP code) branch to storage location 0. IAR = 0. | NCP re-IPL | NO | NO |
| 19 | 000E | Logic error (interrupt reason lost). Program check in level 1. | NCP re-IPL | NO | NO |
| 21 | 0 | Level 2 PCI. The level 2 PCI should be OFF because level 1 has reset it (X'77' bit 0.7). If it is ON (hot level 2 PCI), or if spurious retry count from a PCI level 2 interrupt. | | NO | NO |
| 21 | 0956 | Level 2 PCI (limit threshold) | NCP re-IPL | NO | NO |

Note: In case of abend, NCP re-IPL is performed and the alarm/alert is generated when IPL is completed. Alert is triggered by MOSS BER ID 06, error code 05.

NCP/PEP BER Type 12 (Detailed BER Display)

NCP/PEP BER Type 12 - IDs 11 through 19: Format foN1, see page 11-140. Program level 1 generates one of these BERs when an NCP/PEP program exception occurs.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:hh ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC

X7E:hhhh  X74:hhhhhh  X79:hh  IAR:hhhhhh  I:hhhh

===>

F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

```

NCP/PEP BER Type 12 - ID 21: Format foN2, see page 11-140. Program level 1 generates one of these BERs when a program-controlled interrupt request at level 2 remains unresolved.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:hh ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC

X7F:hhhh  IAR3:hhhhhhh  IAR4:hhhhhhh

===>

F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

```

NCP/PEP BER Type 12 - Field Description

Table 11-55. NCP/PEP BER Type 12 Field Description

| Field Name | Meaning | Refer to |
|------------|---|-----------|
| I | First two bytes of instruction. | |
| IAR | IAR of interrupt level. | -- |
| IAR3 | IAR contents of level 3. | -- |
| IAR4 | IAR contents of level 4. | -- |
| X74 | X'74' - Lagging address register. | Page 2-38 |
| X79 | X'79' - Byte 1 interrupted levels. | Page 2-25 |
| X7F | X'7F' - Interrupt request reg - CCU levels 2, 3, and 4. | Page 2-25 |

Note: All values are in hexadecimal notation (X'0' to X'F').

NCP/PEP BER Type 12 - Formats

| Format: foN1 | |
|---------------|-------------|
| IDs: 11 to 19 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | LOST |
| 31-32 | Abend |
| 33-34 | X7E |
| 35 | Unused |
| 36-38 | X74 |
| 39 | X79, byte 1 |
| 40-42 | IAR |
| 43-44 | I |

| Format: foN2 | |
|--------------|---------|
| ID: 21 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | LOST |
| 31-32 | Abend |
| 33-34 | X7F |
| 35-38 | IAR3 |
| 39-42 | IAR4 |

Figure 11-22. NCP/PEP BER Formats

NCP CCU BER Type 13

CCU BER Type 13 - Summary

| Table 11-56 (Page 1 of 2). CCU BER Type 13 Summary | | | | | |
|--|------------------|---|------------------------|-------|-------|
| BER ID | Abend Code (NCP) | Event Description | Recovery or PGM Action | ALERT | ALARM |
| 32 | 0 | Level 3 interrupt configuration check <ul style="list-style-type: none"> Invalid level 3 interrupt (for example, CA interrupt on a link-attached 3745). | | NO | NO |
| 32 | 0978 | Level 3 interrupt configuration check (limit threshold) | NCP re-IPL | NO | NO |
| 91 | 0 | Unresolved level 1 interrupt, no bit in CA register X'E'. | | NO | NO |
| 91 | 0970 | Unresolved level 1 interrupt (limit threshold) | NCP re-IPL | NO | NO |
| 92 | 0971 | Unresolved interrupted level when requested interrupt level not 2, 3, 4, 5 as per contents of X'79' bits 1.0, 1.1, 1.2, 1.3. | NCP re-IPL | NO | NO |
| 93 | 0972 | Unexpected CCU hardcheck (CCU should have stopped) <ul style="list-style-type: none"> Not possible to reset X'77', bit 0.1, or MOSS has not reset this bit after IPL. | NCP re-IPL | NO | NO |
| 94 | 0973 | Unexpected IPL request <ul style="list-style-type: none"> Not possible to reset X'77' bit 0.0, or MOSS has not reset this bit after IPL. | NCP re-IPL | NO | NO |
| 95 | 0971 | Invalid level 1 interrupted IAR (IN X'79') | NCP re-IPL | NO | NO |
| B1 | 0 | Unresolved level 3 interrupt NCP reading out X'77' does not find bit 1.0 ON (CA level 3) and X'7F' bits 0.2, 0.6, 1.5 and 1.6 ON (level 3 raised by MOSS diag, user, timer or PCI). | | NO | NO |
| B1 | 0974 | Unresolved level 3 interrupt (limit threshold) | NCP re-IPL | NO | NO |
| C1 | 0 | Unresolved level 4 interrupt NCP reading out X'7F' does not find bits 0.3, 0.4, 0.7 and 1.7 ON (Level 4 interrupt raised by MOSS request SVC, MOSS response SVC, PCI or SVC). | | NO | NO |
| C1 | 0975 | Unresolved level 4 interrupt (limit threshold) | NCP re-IPL | NO | NO |
| C2 | 0 | Unresolved level 4 PCI interrupt <ul style="list-style-type: none"> Level 4 PCI (X'7F' bit 0.7) and not wait state, but no bytes are set in level 4 control block of NCP. Mask used to set interrupt does not indicate release, slowdown, dispatcher request SVC interrupt, or mask indicates wait state plus MOSS offline, outmail box, CRP request for MOSS transfer, or MOSS request. | | NO | NO |
| C2 | 0976 | Unresolved level 4 PCI interrupt (limit threshold) | NCP re-IPL | NO | NO |
| C3 | 0 | Hot/spurious level 4 PCI Level 4 PCI latch (X'7F' bit 0.7) does not go OFF, after a reset by output X'77' bit 1.6 | | NO | NO |
| C3 | 0977 | Hot/spurious level 4 PCI (limit threshold) | NCP re-IPL | NO | NO |
| C4 | 0979 | Unresolved level 4 SVC interrupt Level 4 SVC interrupt (X'7F' bit 1.7) but CCU is in wait state. Abend if hot SVC interrupt (X'7F' bit 1.7 still ON after reset latch by Out X'77' bit 1.7). | NCP re-IPL | NO | NO |

Table 11-56 (Page 2 of 2). CCU BER Type 13 Summary

| BER ID | Abend Code (NCP) | Event Description | Recovery or PGM Action | ALERT | ALARM |
|--------|------------------|---|------------------------|-------|-------|
| C5 | 0 | Continuous/unresolved MOSS level 4 request (X'7F' bit 0.3 still ON after reset latch by Out X'77' bit 0.4). | | NO | NO |
| C5 | 097A | Continuous/unresolved MOSS level 4 request (limit threshold) | NCP re-IPL | NO | NO |
| C6 | 0 | Continuous/unresolved MOSS level 4 status (X'7F' bit 0.4 still on after reset latch by Out X'77' bit 0.5). | | NO | NO |
| C6 | 097B | Continuous/unresolved MOSS level 4 status (limit threshold) | NCP re-IPL | NO | NO |

Note: In case of abend, NCP re-IPL is performed and the Alarm/Alert is generated when IPL is completed. Alert is triggered by MOSS BER ID 06, error code 05.

CCU BER Type 13 (Detailed BER Display)

CCU BER Type 13 - IDs 32, B1: Format foU1, see page 11-144. BER generated by program level 3.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:13 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC

X77:hhhh  X7F:hhhh  X0:hhhh  X1:hhhh  X2:hhhh  X3:hhhh  X4:hhhh  X5:hhhh
X6:hhhh  X7:hhhh  X8:hhhh  XC:hhhh  XF:hhhh
XD:hhhh  XE:hhhh  X0:hhhh  X1:hhhh  X2:hhhh
X3:hhhh  X4:hhhh  X5:hhhh  X6:hhhh  X7:hhhh
XB:hhhh  XC:hhhh  XD:hhhh  XE:hhhh  XF:hhhh
TA:hhhh  CCU-INPUT-X57:hhhh  CCU-OUTPUT-X57:hhhh

====>

F1:END F2:MENUE2 F3:ALARH F4:SUNHARY F5:LIST F7:PREVIOUS F8:NEXT

```


CCU BER Type 13 - IDs 91, 92, 93, 94, and 95: Format foU2, see page 11-144. This ID indicates an unresolved level 1 interrupt.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:13 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
X7E:hhhh  X74:hhhhhh  X79:hh  IAR:hhhhhh  X7D:hhhh
CCU-INPUT-X57:hhhh  CCU-OUTPUT-X57:hhhh

====>

F1:END F2:MENUE2 F3:ALARM F4:SUNMARY F5:LIST F7:PREVIOUS F8:NEXT

```

CCU BER Type 13 - IDs C1 to C6: Format foU3, see page 11-144. This ID indicates an unresolved level 4 interrupt.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:13 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC

X77:hhhh  X7F:hhhh  RCB:hhhh hhhh hhhh hhhh

====>

F1:END F2:MENUE2 F3:ALARM F4:SUNMARY F5:LIST F7:PREVIOUS F8:NEXT

```

CCU BER Type 13 - Field Description

Table 11-57 (Page 1 of 2). CCU BER Type 13 Field Description

| Field Name | Meaning | Refer to |
|------------|---|-----------|
| IAR | IAR of interrupt level. | Chapter 7 |
| RCB | Level 4 router control block. | Chapter 7 |
| X0 | X'0' - Channel adapter initial selection register. | Chapter 7 |
| X1 | X'1' - CA CSCW and subchannel address. | Chapter 7 |
| X2 | X'2' - Data status register. | Chapter 7 |
| X3 | X'3' - CA ESC subchannel. | Chapter 7 |
| X4 | X'4' - CA IOH bytes 1 and 2. | Chapter 7 |
| X5 | X'5' - CA IOH bytes 3 and 4. | Chapter 7 |
| X6 | X'6' - CA NSC status register. | Chapter 7 |
| X7 | X'7' - CA enabled indications. | Chapter 7 |
| XB | X'B' - CA ESC TIO address and status. | Chapter 7 |
| XC | X'C' - CA AIO operations register. | Chapter 7 |
| XD | X'D' - CA error register. | Chapter 7 |
| XE | X'E' - CA level 1 interrupt requests. | Chapter 7 |
| XF | X'F' - CA level 3 interrupt request and CA number. | Chapter 7 |
| X74 | X'74' - Cycle steal control word register. | Page 2-25 |
| X77 | X'77' - Interrupt request reg - adapter levels 2 and 3. | Page 2-25 |
| X79 | X'79' - Interrupted level. | Page 2-25 |
| X7D | X'7D' - CCU hardcheck register. | Page 2-25 |
| X7E | X'7E' - CCU level 1 interrupt. | Page 2-25 |
| X7F | X'7F' - Interrupt request reg - CCU levels 2, 3, and 4. | Page 2-25 |
| TA | Tag address | -- |
| TD | Tag data | -- |

| Table 11-57 (Page 2 of 2). CCU BER Type 13 Field Description | | |
|--|----------------------------------|------------|
| Field Name | Meaning | Refer to |
| CCU INPUT X57 | X'57' - Input CA command LS reg | Page 11-92 |
| CCU OUTPUT X57 | X'57' - Output CA command LS reg | Page 11-92 |

CCU BER Type 13 - Formats

| Format foU1 | | Format foU2 | |
|-------------|--|---------------|---------------------------------|
| IDs: 32 B1 | | IDs: 91 to 95 | |
| Byte | Meaning | Byte | Meaning |
| 1-27 | Header | 1-27 | Header |
| 28-29 | TYPE-ID | 28-29 | TYPE-ID |
| 30 | LOST | 30 | LOST |
| 31-32 | Abend | 31-32 | Abend |
| 33-34 | X'77' | 33-34 | X'7E' |
| 35-36 | X'7F' | 35 | Unused |
| 37-62 | IOCI registers X'00'-X'07' and X'0B'-X'0F' | 36-38 | X74 |
| 63-88 | Unused | 39 | X79 |
| 89-90 | TA | 40-42 | IAR |
| 91-92 | CCU input X57 | 43-44 | X'70' CCU hardcheck register |
| 93-94 | CCU output X57 | 45-46 | CCU-input X57 |
| 95 | BER flag | 47-48 | CCU-output X57 |
| | | 49 | BER flag |

| Format foU3 | |
|---------------|----------|
| IDs: C1 to C6 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | LOST |
| 31-32 | CP ABEND |
| 33-34 | X'77' |
| 35-36 | X'7F' |
| 37-44 | RCB |

Figure 11-23. CCU BER Formats

NCP IOC BER Type 14

IOC BER Type 14 - Summary

| Table 11-58. IOC BER Type 14 Summary | | | | | |
|--------------------------------------|------------------|--|------------------------|-------|-------|
| BER ID | Abend Code (NCP) | Event Description | Recovery or PGM Action | ALERT | ALARM |
| 91 | 0 | Unresolved adapter level 1 | | NO | NO |
| 91 | 0990 | Unresolved adapter level 1 (limit threshold) | NCP re-IPL | NO | NO |
| 92 | 0 | Unresolved AIO level 1 Attempt to cycle steal by undefined LA or CA. X'76' = 1A, 2A, 36, or B6 X'75' = Meaningless | | NO | NO |
| 92 | 0991 | Unresolved AIO level 1 (limit threshold) | NCP re-IPL | NO | NO |
| 93 | 0 | Unresolved PIO level 1 PIO error detected by the IOC that was found unresolved (no time out or parity error, in X'76' bits 0.4 and 0.5). | | NO | NO |
| 93 | 0992 | Unresolved PIO level 1 (limit threshold) | NCP re-IPL | NO | NO |
| 96 | 0 | Read switch error register failed <ul style="list-style-type: none"> • X'76' bit 0.4 for IOC1 time out • X'76' bit 0.5 for bus IN parity error X'76' bits 0.0, 0.1, 0.2, 0.3 contain the IOC internal error status at time of error | | | |

Note: In case of abend, an NCP re-IPL is performed and the alarm/alert is generated when IPL is completed. Alert is triggered by the MOSS BER ID 06, error code 05.

IOC BER Type 14 (Detailed BER Display)

All IDs (91, 92, 93, 96): See format fol1, on page 11-146. Program level 1 generates one of these BERs when an error occurs on the IOC bus.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:10 ID:hh<LOST:ddd CP-ABEND:hhhh>
<ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
X7E:hhhh  X76:hhhh  X75:hhhh  X74:hhhhhhhh  X76U:hhhh
SWA:
CCU-INPUT-X57:hhhh  CCU-OUTPUT-X57:hhhh

```

====>

F1:END F2:MENUE2 F3:ALARM F4:SUNHARY F5:LIST F7:PREVIOUS F8:NEXT

IOC BER Type 14 - Field Description

| Table 11-59. IOC BER Type 14 Field Description | | |
|--|--|------------------|
| Field Name | Meaning | Refer to |
| CAB | CAB error register. | (*) Page 2-25 |
| F | Indicator flag byte (byte extension) | |
| X'74 | X'74' - Lagging address register (LAR) bytes. | |
| X'75 | X'75' - Cycle steal control word register. | |
| X'76 | X'76' - IOC error summary register. | |
| X'76U | X'76' - Cause of error not found (PIO to read error register failed). | Page 2-25 |
| | See page 11-14 | |
| X'7E | X'7E' - CCU level 1 interrupt. | Page 2-25 |
| SWA | Unused | Page 11-92 |
| CCU | CCU input command LS register (same for "OUTPUT") | |
| INPUT-X57 | | |

Note: All values are in hexadecimal format (X'0' to X'F'), except for the flag indicator F, which is in bit format (8 bits, 0 or 1).

(*) For software information on BERs originated by NCP/PEP, refer to the associated product documentation.

IOC BER Type 14 - Format

| Format: foI1 | |
|------------------|----------------|
| IDs: 91 92 93 96 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | Lost |
| 31-32 | Abend |
| 33-34 | X'7E |
| 35-36 | X'76 |
| 37-38 | X'75 |
| 39-42 | X'74 |
| 43-44 | Unused |
| 45-46 | X'76U |
| 47-48 | CCU input X57 |
| 49-50 | CCU output X57 |
| 51 | Flag |
| 52 | Unused |
| 53-54 | SWA |

Figure 11-24. IOC BER Format

NCP TRSS BER Type 15

TRSS BER Type 15 - Summary

| Table 11-60 (Page 1 of 3). TRSS BER Type 15 Summary | | | | |
|---|------------------|--|------------------------|--------------|
| BER ID | Abend Code (NCP) | Event Description | Recovery or PGM Action | ALARM/ ALERT |
| 14 | 0B01 | Address exception (AIO) X'76' bit 0.0 or 1.0 ON | NCP re-IPL | NO |
| 16 | 0B02 | Storage protect (AIO) X'76' bit 0.1 or 1.1 ON | NCP re-IPL | NO |
| 18 | 0 | IOH/IOHI to TRM not installed X'7E' bit 0.5 or 1.5 ON IOC bus check in error status type 1 of TRM bit 0.1 and 0.5 on (X'02 bits 0.1 and 0.5) | | 89 |
| 91 | 0 | TRM AIO error <ul style="list-style-type: none"> X'75' bit 0.0 or 1.5 ON X'76' bit 0.4 ON for IOC1 time out X'76' bit 0.5 ON for IOC bus in parity error X'76' bit 0.6 ON in both cases (AIO) <ul style="list-style-type: none"> X'76' bits 0.0, 0.1, 0.2, 0.3 contain the IOC internal status at time of error. | TIC retry | NO |
| 91 | 0 | TRM AIO error (threshold) | TRM down | 82 |
| 92 | 0 | TRM AIO error unresolved | TIC retry | NO |
| 92 | 0 | TRM AIO error unresolved (limit threshold) | TRM down | 82 |
| 93 | 0 | TRM AIO invalid CSCW <ul style="list-style-type: none"> X'75' bit 0.0 or 1.0 ON X'76' bits 0.2 and 0.6 or 1.2 and 1.6 ON | TIC retry | NO |
| 93 | 0 | TRM AIO invalid CSCW (limit threshold) | TRM down | 82 |
| 96 | 0 | TRM disconnect state (following request from MOSS) <ul style="list-style-type: none"> X'7E' bit 0.2 or 0.6 ON Error status, bit 0.7 ON Ext register X'01' bit 5 ON | TRM OFF line | B9 |
| 97 | 0 | TRM PIO error-output IOH/IOHI <ul style="list-style-type: none"> X'75' bit 0.0 or 1.0 ON X'76' bit 0.4 ON for IOC1 time out X'76' bit 0.5 for IOC bus in parity error X'76' bit 0.6 OFF in both cases Origin given in error status type 1 of TRM | NCP retry | NO |
| 97 | 0 | TRM PIO error-output IOH/IOHI (limit threshold) | TRM down | NO |
| 98 | 0 | TRM PIO error-output IOH/IOHI (over threshold) | TRM down | 82 |
| 99 | 0 | TRA adapter error (IOH bit 1.7 ON) | TRM down | 82 |
| 9A | 0 | TRM adapter error unresolved <ul style="list-style-type: none"> First get error status failed but retry was successful Error status has value at time of failure | | NO |
| 9A | 0 | TRM adapter error unresolved (limit threshold) Error status filled by X'FFFF' | TRM down | 82 |

Table 11-60 (Page 2 of 3). TRSS BER Type 15 Summary

| BER ID | Abend Code (NCP) | Event Description | Recovery or PGM Action | ALARM/ ALERT |
|--------|------------------|--|------------------------|--------------|
| 9B | 0 | Interrupt from disconnected TRM <ul style="list-style-type: none"> Level 1 interrupt presented to NCP/PEP while the TRM is disconnected (X'01' bit 5 ON) X'7E' bit 0.2 or 0.6 ON | | NO |
| 9B | 0 | Interrupt from disconnected TRM (limit threshold) | TRM down | NO |
| 9B | XXXX | Interrupt from disconnected TRM | NCP re-IPL | NO |
| 9C | 0 | TRM PIO error input on get line ID (see BER 11 97 for general PIO errors) | NCP retry | NO |
| 9C | 09x3 | TRM PIO error input on get line ID (limit threshold) Retry on get line ID failed | NCP re-IPL | NO |
| 9E | 0 | Get error status command error, after PIO (see type 15 ID 9A and 9c) | NCP re-IPL | 83 |
| A3 | 0 | Invalid level 2 interrupt | TIC down | 80 |
| A4 | 0 | DMA or interrupt vector error due to TIC interrupt level 2 <ul style="list-style-type: none"> TRM status bit 0 ON TRM status bits 4, 5 not '000' | TIC retry | NO |
| A4 | 0 | DMA or interrupt vector error due to TIC (limit threshold) | TIC down | 80 |
| A5 | 0 | DMA or interrupt vector error due to TRM Interrupt level 2 <ul style="list-style-type: none"> TRM status bit 0 ON TRM status bit 6 ON | TIC retry | NO |
| A5 | 0 | DMA or interrupt vector error due to TRM (limit threshold) | TRM down | 83 |
| A7 | 0 | PIO-MMIO error interrupt level 2 <ul style="list-style-type: none"> TRM status bit 0 ON TRM status bits 1, 2, 3 neither '000' nor '001' | TIC retry | NO |
| A7 | 0 | PIO-MMIO error (limit threshold) | TIC down | 80 |
| A8 | 0 | PIO-MMIO error (last TIC) <ul style="list-style-type: none"> TRM status bit 0 ON TRM status bits 1, 2, 3 = '001' | TRM retry | NO |
| A8 | 0 | PIO-MMIO error (last TIC) <ul style="list-style-type: none"> TRM status bit 0 ON TRM status bits 1, 2, 3 = '001' | TRM down | 83 |
| AC | 0 | TIC adapter check interrupt level 2 <ul style="list-style-type: none"> TRM status bit 0 OFF TRM status bit 3 ON | TIC down | 80 |
| AF | 0 | TIC down at open time <ul style="list-style-type: none"> Interrupt level 2 SSB open completion bit 6 ON | TIC down | 85 |
| B2 | 0 | TIC/TRM check at initialization time | TIC retry | NO |
| B2 | 0 | TIC/TRM check at initialization time (limit threshold) | TIC down | (2) |
| B3 | 0 | Back-up time out. No completion interrupt level 2 received during the back-up timer with : <ul style="list-style-type: none"> TIC control register bits 0, 1, 3 OFF IR/BR register bit interrupt request OFF | TIC down | 87 |

Table 11-60 (Page 3 of 3). TRSS BER Type 15 Summary

| BER ID | Abend Code (NCP) | Event Description | Recovery or PGM Action | ALARM/ ALERT |
|--------|------------------|--|------------------------|--------------|
| B4 | 0 | Component out of use <ul style="list-style-type: none"> 'Interrupt occurred' flag OFF when the timer elapses and no interrupt received 'Write interrupt register' with SCB | TIC down | 8B |
| B5 | 0 | Back-up time out (last TIC). No completion interrupt level 2 received during the back-up timer with : <ul style="list-style-type: none"> TIC control register bits 0, 1, 3 OFF, and IR/BR register bit interrupt request ON, or TIC control register bits 0, 1, 3 not all OFF | TRM down | 81 |
| B6 | 0 | Incomplete frame time out No interrupt level 2 received during the incomplete frame timer | TIC down | 8C |

Notes:

1. In case ofabend. NCP re-IPL is performed and the Alarm/Alert is generated when IPL is completed. Alert is triggered by MOSS BER ID 06, error code 05.
2. BER ID B2 may generate diferent alerts according to the value of the interrupt register (see alerts 8D, 84, 80).

TRSS BER Type 15 (Detailed BER Display)

TRSS BER Type 15 - IDs 14, 16, 91, 92, 93: Format foR1, see page 11-153.
Program level 1 generates one of these BERs when an error occurs during an AIO operation on a TRA.

```

                                ELD DETAIL
SEL#:ddd FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:15 ID:hh <LOST:ddd CP-ABEND:hhhh>
TRIInn TICn <ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCCCC
F:bbbbbbbbb
X7E:hhhh X76U:hhhh ETA:hhhh X3F:hhhhhhhh X75:hhhh

X76      TRII STATUS1      SWAD ERROR REG
hhhh bbbbbbbb bbbbbbbb bbbbbbbb bbbbbbbb

===>

F1:END F2:MENU2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

```


TRSS BER Type 15 - IDs 18, 97, 98, 9C: Format foR2, see page 11-153.
Program level 1 generates one of the following BERs when an error occurs during a PIO operation on a TRA.

```

                                ELD DETAIL
SEL#:ddd FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:15 ID:hh <LOST:ddd CP-ABEND:hhh>
TRMnn TICn <ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCC
F:bbbbbbb
X7E:hhh X76U:hhh ETA:hhh X74:hhhhhhh
X79:hh IAR:hhhhh I:hhh TA:hhh TD:hhh

X76      TRM STATUS1      SWAD ERROR REG
hhh bbbbbbb bbbbbbb bbbbbbb bbbbbbb

====>

F1:END F2:MENUE2 F3:ALARM F4:SUNHARY F5:LIST F7:PREVIOUS F8:NEXT

```

TRSS BER Type 15 - ID 96, 99, 9A, 9B: Format foR3, see page 11-154. Program level 1 generates one of the following BER when a TRM is disconnected by MOSS, or when an error is exported by a TRM on level 1.

```

                                ELD DETAIL
SEL#:hhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:15 ID:hh<LOST:ddd CP-ABEND:hhh>
TRMnn TICn <ERROR DESCRIPTION>                                <REFER.CODE IN CHAR.> CCCCCC
F:bbbbbbb
X7E:hhh X76U:hhh TRIA:hh
X76      TRM STATUS1      SWAD ERROR REG
hhh bbbbbbb bbbbbbb bbbbbbb bbbbbbb

====>

F1:END F2:MENUE2 F3:ALARM F4:SUNHARY F5:LIST F7:PREVIOUS F8:NEXT

```

TRSS BER Type 15 - IDs A3, A4, A5, A7, A8: Format foR4, see page 11-154. Program level 2 generates one of the following BERs when an error occurs (internal TRM/TIC error).

```

                                ELD DETAIL
SEL#:ddd FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:15 ID:hh
TRMnn TICn <ERROR DESCRIPTION>                                <REF. CODE IN CHAR.> CCCCCC
F:bbbbbbb
TA:hhh TICA:hh
TRM STATUS2
bbbbbbb bbbbbbb

====>

F1:END F2:MENUE2 F3:ALARM F4:SUNHARY F5:LIST F7:PREVIOUS F8:NEXT

```


TRSS BER Type 15 - ID AC: Format foR5, see page 11-154. Program level 2 generates the following BER when a TIC adapter check occurs on a TIC.

```

                                ELD DETAIL
SEL#:ddd FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:15 ID:hh <LOST:ddd CP-ABEND:hhh>
TRMnn TICn <ERROR DESCRIPTION>                                <REF. CODE IN CHAR.> CCCCCCCC
F:bbbbbbb
TA:hhh TICA:hh
TRM STATUS2
bbbbbbb bbbbbbb
TIC ADAPTER CHECK STATUS:
bbbbbbb bbbbbbbb hhhh hhhh hhhh

```

====>

F1:END F2:MENUE2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

TRSS BER Type 15 - ID AF: Format foR6, see page 11-154. Program level 2 generates the following BER when a TIC check occurs at open time.

```

                                ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:15 ID:hh<LOST:ddd CP-ABEND:hhh>
<ERROR DESCRIPTION>                                <REF. CODE IN CHAR.> CCCCCCCC
F:bbbbbbb
TA:hhhh TICA:hh
TRM STATUS2
bbbbbbb bbbbbbb
SSB
hhhh bbbbbbbb bbbbbbbb

```

====>

F1:END F2:MENUE2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

TRSS BER Type 15 - ID B2: Format foR7, see page 11-154. Program level 3 generates the following BER when a TIC/TRM check occurs on a command sent to a TRM.

```

                                ELD DETAIL
SEL#:hhhh FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:15 ID:hh<LOST:ddd CP-ABEND:hhh>
<ERROR DESCRIPTION>                                <REF. CODE IN CHAR.> CCCCCCCC
F:bbbbbbb
TA:hhhh TICA:hh
TRM IIR TIC CTL REGISTER
bbbbbbb bbbbbbb bbbbbbbb bbbbbbbb

```

====>

F1:END F2:MENUE2 F3:ALARM F4:SUMMARY F5:LIST F7:PREVIOUS F8:NEXT

TRSS BER Type 15 - IDs B3, B4, B5, B6: Format for 8, see page 11-154.

Program level 3 generates one of the following BERs when a time out occurs on a command sent to a TRM.

```

                                ELD DETAIL
SEL#:hhhh  FLAG:hh DATE:dd/dd TIME:dd:dd TYPE:15 ID:hh<LOST:ddd CP-ABEID:hhhh>
<ERROR DESCRIPTION>                                <REF. CODE IN CHAR.> CCCCCCCC
F:bbbbbbbb
TA:hhhh          TICA:hh
TRM IR/BR        TIC CTL REGISTER
bbbbbbbb bbbbbbbb bbbbbbbb bbbbbbbb

====>

F1:END F2:MENUE2 F3:ALARII F4:SUIHARY F5:LIST F7:PREVIOUS F8:NEXT

```

TRSS BER Type 15 - Field Description

| Table 11-61. TRSS BER Type 15 Field Description | | |
|---|--|-----------|
| Field Name | Meaning | Refer to |
| TICA | TIC internal address 00-01 (within the TRM) | Chapter 6 |
| TRM STAT2 | TRA level 2 error status | Chapter 6 |
| TRMnn | TRM number (decimal in error description field). This TRM number is derived from: <ul style="list-style-type: none"> field TA for PIO operation <ul style="list-style-type: none"> for CS error reported at level 2 for CA error reported at level 3 field X75 for AIO operation field TRM status level 1 for TRM adapter error reported at level 1 <p>If no nn is specified (blank), problem isolation by program was not possible.</p> | |
| TICn | TIC number 1-2 within the TRM | |
| TIC adapter check status | Four halfwords giving the reason of a TIC microcodeabend | Chapter 6 |
| TRM STAT1 | TRA level 1 error status | Chapter 6 |
| TRM IR/BR | Interrupt request/bus request flags | Chapter 6 |
| TIC CTL REG | TIC control register | Chapter 6 |
| TRM IIR | TIC interrupt register (initialize) | Chapter 6 |
| TA/TD | | |
| ETA | TA field of IOH failure in level 1. | |
| F | Indicator flag, indicates a byte expansion follows | |
| TRMA | TRM address | Chapter 6 |
| I | First two bytes of instruction. | |
| IAR | IAR of interrupt level. | |
| X3F | CSP shared pointer register | Chapter 4 |
| X74 | X'74' - LAR bytes | Page 2-25 |
| X75 | X'75' - Cycle steal control word register | Page 2-25 |
| X76 | X'76' - IOC error summary register | Page 2-25 |
| X76U | X'76' - Cause of error not found (PIO to read error register failed) | Page 2-25 |
| X77 | X'77' - Interrupt request reg - adapter level 2 and 3 | Page 2-25 |
| X79 | X'79' - Interrupt level | Page 2-25 |
| X7E | X'7E' - CCU level 1 interrupt | Page 2-25 |
| X7F | X'7F' - Interrupt request reg - CCU level 2, 3, and 4 | Page 2-25 |
| SSB | Sense summary block | (*) |
| SWAD | Unused | |

Note: All values are in hexadecimal format (X'0' to X'F'), except for:

1. The TIC ADPT CHECK STAT, SSB, TRM IR/BR, TIC CTL register, TRM IIR, TRM status 1, TRM status 2, which are in **bit format** (8 or 16 bits, 0 or 1)
2. The error description line with a TRM number and TIC number, which are in **decimal**.

(*) For software information on BERs originated by NCP/PEP, refer to the associated product documentation.

TRSS BER Type 15 - Formats

| Format: foR1 | | Format: foR2 | |
|---------------------|-------------|------------------|-------------|
| IDs: 14 16 91 92 93 | | IDs: 18 97 98 9C | |
| Byte | Meaning | Byte | Meaning |
| 1-27 | Header | 1-27 | Header |
| 28-29 | TYPE-ID | 28-29 | TYPE-ID |
| 30 | LOST | 30 | LOST |
| 31-32 | Abend | 31-32 | Abend |
| 33-34 | X7E | 33-34 | X7E |
| 35-36 | X76 | 35-36 | X76 |
| 37-38 | X75 | 37-38 | I |
| 39-40 | Unused | 39-42 | X74 |
| 41-42 | ETA | 43-44 | TRM STATUS1 |
| 43-44 | TRM STATUS1 | 45-46 | X76U |
| 45-46 | X76U | 47-48 | ETA |
| 47-50 | X3F | 49-50 | Unused |
| 51 | F | 51 | F |
| 52 | Unused | 52 | Unused |
| 53-54 | SWAD | 53-54 | SWAD |
| 55-72 | Unused | 55 | X79 |
| | | 56-58 | IAR |
| | | 59-60 | TA |
| | | 61-62 | TD |

Figure 11-25 (Part 1 of 2). TRSS BER Formats

| Format: foR3 | |
|------------------|----------------|
| IDs: 96 99 9A 9B | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | LOST |
| 31-32 | Abend |
| 33-34 | X7E |
| 35-36 | X76 |
| 37 | TRM address |
| 38-42 | Unused |
| 43-44 | TRM STATUS1 |
| 45-46 | X76U |
| 47-50 | Unused |
| 51 | F |
| 52 | Unused |
| 53-54 | SWAD error reg |
| 55-74 | Unused |
| 75-76 | ETA |

| Format: foR4 | |
|---------------|-------------|
| IDs: A3 to A8 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | LOST |
| 31-32 | Abend |
| 33 | F |
| 34 | TICA |
| 35-36 | TA data |
| 37-38 | TRM STATUS2 |

| Format: foR5 | |
|--------------|----------------------|
| ID: AC | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | LOST |
| 31-32 | Abend |
| 33 | F |
| 34 | TICA |
| 35-36 | TA data |
| 37-38 | TRM STATUS2 |
| 39-46 | Adapter check status |

| Format: foR6 | |
|--------------|---------------------|
| ID: AF | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | LOST |
| 31-32 | Abend |
| 33 | F |
| 34 | TICA |
| 35-36 | TA data |
| 37-38 | TRM STATUS2 |
| 39-42 | SSB open completion |

| Format: foR7 | |
|---------------|----------------------|
| IDs: B3 to B6 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | LOST |
| 31-32 | Abend |
| 33 | F |
| 34 | TICA |
| 35-36 | TA data |
| 37-38 | TRM IR/BR register |
| 39-40 | TIC control register |

| Format: foR8 | |
|--------------|-----------------------------|
| ID: B2 | |
| Byte | Meaning |
| 1-27 | Header |
| 28-29 | TYPE-ID |
| 30 | LOST |
| 31-32 | Abend |
| 33 | F |
| 34 | TICA |
| 35-36 | TA data |
| 37-38 | TIC init interrupt register |
| 39-40 | TIC control register |

Figure 11-25 (Part 2 of 2). TRSS BER Formats

List of Abbreviations

| | | | |
|---------------|--|--------------|--|
| A | ampere | CEPT | Comite Europeen des Postes et Telecommunications |
| AC | 1) alternating current 2) address compare | CLDP | controller load/dump program |
| ACK | affirmative acknowledgment (BSC) | CMSA | CCU/MOSS status register A |
| AFD | airflow detector | CMSB | CCU/MOSS status register B |
| AIO | adapter-initiated operation | CMSC | CCU/MOSS status register C |
| ASCII | American National Standard Code for Information Interchange | CNM | communication network management |
| BASA | basic board A | CO/CS | contact operate / contact sense |
| BASB | basic board B | CP | 1) communication processor 2) control program |
| BASC | basic board C | CPx | FRU name of circuit protector number x |
| BATRY | FRU name of the battery | CRP | check record pool |
| BCCA | buffer chaining channel adapter | CRU | customer replaceable unit |
| BCLE | buffer control list element | CS | cycle steal |
| BER | box event record | CSC | FRU name of the scanner for medium-/low-speed lines |
| BPC1 | FRU name of the bus propagation card to replace the CAL card | CSCW | cycle steal control word |
| BPC2 | bus propagation card to replace the TRM card | CSG | cycle steal grant |
| bps | bits per second | CSGH | cycle steal grant high |
| BSC | binary synchronous communication | CSGL | cycle steal grant low |
| BTLC | branch trace level control (register) | CSP | FRU name of the communication scanner processor associated with the FESH card for high speed lines (CSC scanner for the medium-/low-speed lines) |
| CA | channel adapter | CSR | cycle steal request |
| CAB | channel adapter board | CSRH | cycle steal request high |
| CADR | FRU name of the channel adapter driver receiver card | CSRL | cycle steal request low |
| CAL | FRU name of the channel adapter logic card | CSS | control subsystem |
| CADS | channel adapter data streaming | CTS | clear to send (signal) |
| CAMPOR | CA MOSS power-ON-reset (register) | dc | direct current |
| CARST | CA reset (register) | DCE | data circuit-terminating equipment |
| CBx | FRU name of circuit breaker number x | DCREG | FRU name of the dc regulator card |
| CCITT | Comite Consultatif International Telegraphique et Telephonique | DE | device end (channel status) |
| CCU | central control unit | DFA | FRU name of the disk file adapter card |
| CCW | channel command word | DIF | disk function |
| CD | carrier detector (signal) | DIV | diagnostic information vector |
| CDF | configuration data file | DMA | direct memory access |
| CDG | concurrent diagnostic | DMUX | FRU name of the double multiplex card |
| CDS | configuration data set (NCP/EP) | DRS | data rate select |
| CE | customer engineer | DTE | data terminal equipment |

| | | | |
|---------------|---|-------------|--|
| DTR | data terminal ready (signal) | IOH | input/output halfword (instruction) |
| EC | engineering change | IOHI | input/output halfword immediate (instruction) |
| EIA | Electronic Industries Association | IPL | initial program load |
| EINTP1 | extended interrupt 1 (register) | IR | interrupt request |
| EIRV | error interrupt request vector | IRR | interrupt request removed |
| ENCA | enable CA (register) | ISO | International Organization of Standardization |
| ENQ | enquiry (BSC) | KB | kilobyte (1024 bytes) |
| EPO | emergency power-OFF | kbps | kilobits per second |
| ERC | error reference code | kg | kilogram |
| FAN1 | FRU name of the power supply box fan | kHz | kilohertz |
| FAN2 | FRU name of the logic box fan | LA | 1) load address (instruction) 2) line adapter |
| FCC | Federal Communications Commission | LED | light-emitting diode |
| FDD | FRU name of the flexible disk drive | LIB | line interface coupler board |
| FE | field engineering | LIB1 | LIC board type 1 for LICs 1-4 (models 150 and 170) |
| FESH | FRU name of the front-end scanner (high-speed) | LIB2 | LIC board type 2 for LICs 5-6 (models 150 and 170) |
| FRU | field-replaceable unit | LIB3 | LIC board type 3 for LICs 1-4 (model 150) |
| ft | foot | LIC | line interface coupler card |
| GPT | generalized PIU trace | LICx | FRU name of line interface coupler card type x |
| GTF | generalized trace facility | LID | line interface display |
| HCS | Hardware Central Service | LLIR | low-level interrupt request |
| HDD | FRU name of the hard disk drive | LPDA | Link Problem Determination Aid |
| hex | hexadecimal | LS | local storage |
| HLIR | high-level interrupt request | LAS | line adapter status |
| HPTSS | high-performance transmission subsystem | LSAR | local storage address register |
| HSB | high-speed buffer (cache) | LSR | local storage register (CSP) |
| HSS | high-speed scanner | LSS | low-speed scanner |
| HW | hardware | LSSD | level-sensitive scan design |
| Hz | Hertz | m | meter |
| IBE | internal box error | mA | milliampere |
| ID | identifier | MB | megabyte; 1 048 576 bytes |
| IEEE | Institute of Electrical and Electronics Engineers | MCAD | MOSS/CA Adapter |
| IFT | internal function test | MCC | FRU name of the MOSS control card |
| IML | initial microcode load | MCCU | MOSS/CCU Adapter |
| in. | inch | MCF | microcode fix |
| INN | intermediate network node | MCRA | mode control register A |
| INTP1 | interrupt 1 (register) | MCT | machine configuration table |
| INTP4 | interrupt 4 (register) | | |
| IO | input/output | | |
| IOC | input/output control | | |
| IOIRV | input/output interrupt request vector | | |

| | | | |
|--------------|--|---------------|---|
| MDOR | MOSS data operand register | PS | power supply |
| MES | miscellaneous equipment specification | PCSS | power control subsystem |
| MHz | megahertz | PSTCE | product support trained CE |
| min | minute | PS1 | FRU name of power supply number 1 |
| MIO | MOSS input/output | PS2 | FRU name of power supply number 2 |
| MIOC | MOSS I/O control bus | PTCE | product-trained CE |
| MIP | Maintenance Information Procedures | PTT | Post, Telephone and Telegraph (agency) |
| mm | millimeter | PUC | FRU name of the CCU card |
| MMIO | memory mapped input/output | PV | parity valid (signal) |
| MMOD | MOSS mode (register) | RAC | repair action code |
| MOSS | maintenance and operator subsystem | RCV | receive |
| MPC | FRU name of the MOSS processor card | RD | receive data (signal) |
| MSA | machine status area | RETAIN | Remote Technical Assistance Informa- tion Network |
| MSAU | multistation access unit | RFS | ready for sending (signal) |
| MSC | FRU name of the MOSS storage card | RI | 1) register to immediate operand (instruction) 2) ring indicator (same as CI) |
| MUX | multiplex function | RIM | request initialization mode (SDLC) |
| mV | millivolt | RNIO | OS/VS VTAM IO trace |
| NAK | negative acknowledgment character (BSC) | ROS | read-only storage |
| NCCF | Network Communications Control Facility | RPO | remote power-OFF |
| NCP | Network Control Program | RSF | remote support facility |
| NCTE | network communication terminal equip- ment | RTS | request to send (signal) |
| NLDM | Network Logical Data Manager | R/W | read/write |
| NMVT | network management vector transport | SAR | storage address register |
| NPDA | Network Problem Determination Appli- cation | SCTL | FRU name of the storage control card |
| NPSI | network packet switching interface | SDLC | Synchronous Data Link Control |
| oc | overcurrent | SIM | set initialization mode (SDLC) |
| OLT | online test | SMUXA | FRU name of the single multiplex card for LIC board type 2 |
| ov | overvoltage | SMUXB | FRU name of the single multiplex card for LIC board type 2 |
| PANEL | FRU name of the control panel | SNA | Systems Network Architecture |
| PC | personal computer | SNRM | set normal response mode (SDLC) |
| PCC | FRU name of the power control card | STAT0 | status 0 register |
| PCF | primary control field (storage) | STAT1 | status 1 register |
| PKD | portable keyboard display | STAT4 | status 4 register |
| PIO | program-initiated operation | STO | FRU name of the storage (card) |
| PIRV | programmed interrupt request vector | STO4 | FRU name of the storage card 4 Mbytes |
| PNLC | FRU name of the panel card | STO8 | FRU name of the storage card 8 Mbytes |
| POR | power-ON reset | | |
| PROM | FRU name of the programmable read- only memory module | | |

| | | | |
|--------------|--|-------------|---|
| SVC | supervisor call | T1 | US service for very high speed transmissions at 1.5 million bps |
| SWx | FRU name of switch number x | UA | unnumbered acknowledgment (SDLC) |
| T | transmit (signal) | UC | universal controller |
| TA | tag address | UEPO | unit emergency power-Off |
| TCM | 1) thermally-controlled module 2) trellis coded modulation | URSF | universal remote support facility |
| TD | 1) tag data 2) transmitted data (signal) | V | volt |
| TERMD | FRU name of the DMA terminator card | VB | valid byte (signal) |
| TERMI | FRU name of the IOC terminator card | VAC | volts, alternating current |
| TI | test indicator (signal) | VDC | volts, direct current |
| TIC | token-ring interface coupler | VH | valid halfword (signal) |
| TIC1 | FRU name of the TIC card type 1 (4 Mbits only) | VTAM | Virtual Telecommunications Access Method |
| TIC2 | FRU name of the TIC card type 2 (4 and 16 Mbits) | V.24 | CCITT V.24 recommendation |
| TPS | two-processor switch | V.25 | CCITT V.25 recommendation |
| TRA | token-ring adapter | V.28 | CCITT V.28 recommendation |
| TRM | FRU name of the token-ring multiplexer card that controls up to two TICs | V.35 | CCITT V.35 recommendation |
| TRSS | token-ring subsystem | XI | X.25 SNA interconnection |
| TSS | transmission subsystem | XID | exchange identification |
| | | X.21 | CCITT X.21 recommendation |
| | | X.25 | CCITT X.25 recommendation |

Glossary

This glossary defines all new terms used in this manual. It also includes terms and definitions from the *IBM Dictionary of Computing*, GC20-1699.

adapter-initiated operation (AIO). A transfer of up to 256 bytes between an adapter (CA or LA) and the CCU storage. The transfer is initiated by an IOH/IOHI instruction, and is performed in cycle stealing via the IOC bus.

alarm. A message sent to the MOSS console. In case of an error a reference code identifies the nature of the error.

alert. A message sent to the host console. In case of an error a reference code identifies the nature of the error.

autoBER. A program to automatically analyse a BER file.

automaint. A function that uses autoBER to isolate failing FRUs.

Buffer chaining channel adapter (BCCA). A channel adapter that handles buffer chaining in write channel program and both buffer chaining and PIU chaining in read channel program. BCCA works only under NCP.

box event record (BER). Information about an event detected by the controller. It is recorded on the disk/diskette and can be displayed on the operator console for event analysis.

block multiplexer channel. A multiplexer channel that interleaves blocks of data. See also *byte multiplexer channel*. Contrast with *selector channel*.

byte multiplexer channel. A multiplexer channel that interleaves bytes of data. See also *block multiplexer channel*. Contrast with *selector channel*.

cache. A high-speed buffer storage that contains frequently accessed instructions and data; it is used to reduce access time.

central control unit (CCU). In the 3745, the controller hardware unit that contains the circuits and data flow paths needed to execute instructions and to control its storage and the attached adapters.

channel adapter (CA). A communication controller hardware unit used to attach the controller to a host processor.

clear channel. Mode of data transmission where the data passes through the DCE and network, and arrives at the receiving communication controller

unchanged from the data transmitted. The DCE or network can modify the data during transmission because of certain network restrictions, but must ensure the received data stream is the same as the transmitted data stream.

communication controller. A communication control unit that is controlled by one or more programs stored and executed in the unit. Examples are the IBM 3705, IBM 3725/3726, IBM 3720, and IBM 3745.

communication scanner processor (CSP). The processor of a scanner.

communication subsystem. The part of the controller that controls the data transfers over the transmission interface.

configuration data file (CDF). A MOSS file that contains a description of all the hardware features (presence, type, address, and characteristics).

control panel. A panel that contains switches and indicators for the use of the customer's operator and service personnel.

control program. A computer program designed to schedule and to supervise the execution of programs of the controller.

control subsystem (CSS). The part of the controller that stores and executes the control program, and monitors the data transfers over the channel and transmission interfaces.

data circuit-terminating equipment (DCE). The equipment installed at the user's premises that provides all the functions required to establish, maintain, and terminate a connection, and the signal conversion and coding between the data terminal equipment (DTE) and the line. For example, a modem is a DCE (see *modem*.)

Note: The DCE may be separate equipment or an integral part of other equipment.

data terminal equipment (DTE). That part of a data station that serves as a data source, data link, or both, and provides for the data communication control function according to protocols.

direct attachment. The attachment of a DTE to another DTE without a DCE.

high-performance transmission subsystem (HPTSS). The part of the controller that controls the data transfers over the high-speed transmission interface (speed up to 2 million bps).

high-speed scanner. Line adapter for lines up to 2 million bps, composed of a communication scanner processor (CSP) and a front-end high-speed scanner (FESH).

initial microcode load (IML). The process of loading the microcode into a scanner or into MOSS.

initial program load (IPL). The initialization procedure that causes 3745 control program to commence operation.

input/output control (IOC). The circuit that controls the input/output from/to the channel adapters and scanners via the IOC bus.

internal clock function. A LIC function that provides a transmit clock for sending data, and retrieves a receive clock from received data, when the modem does not provide those timing signals. When the terminal is connected in direct-attach mode (without modem) the ICF also provides the transmit and receive clocks to the terminal, via the LIC card.

line adapter (LA). The part of the TSS, HPTSS, or TRSS that scans and controls the transmission lines. Also called *scanner*.

For the TSS the line adapters are low-speed scanners (LSSs).

For the HPTSS the line adapters are high-speed scanners (HSSs).

For the TRSS the line adapters are token-ring adapters (TRAs).

line interface coupler (LIC). A circuit that attaches up to four transmission cables to the controller.

low-speed scanner. Line adapter for lines up to 256 kbps, composed of a CSC card.

maintenance and operator subsystem (MOSS). The part of the controller that provides operating and servicing facilities to the customer's operator and the IBM service representative.

NetView An IBM licensed program used to monitor a network, manage it, and diagnose its problems.

Network Control Program (NCP). An IBM licensed program that provides communication controller

support for single-domain, multiple-domain, and interconnected network capability.

operator console. The IBM Operator Console that is used to operate and service the communication controller (CC) through the MOSS. Optionally an alternate console may be installed up to 120 m from the CC, or a remote console may be connected to the (CC) through the switched network.

scanner. A device that scans and controls the transmission lines. Also called *line adapter*.

selector channel. An I/O channel designed to operate with only one I/O device at a time. Once the I/O device is selected, a complete record is transferred one byte at a time. Contrast with *block multiplexer channel*, *multiplexer channel*.

Systems Network Architecture (SNA). The description of the logical structure, formats, protocols, and operational sequences for transmitting information through a user application network. The structure of SNA allows the users to be independent of specific telecommunication facilities.

token-ring subsystem (TRSS). The part of the controller that controls the data transfers over an IBM Token-Ring Network

The TRSS consists of one or several token-ring adapter (TRA).

token-ring adapter (TRA). Line adapter for an IBM Token-Ring Network, composed of one token-ring multiplexer card (TRM), and two token-ring interface couplers (TICs).

transmission subsystem (TSS). The part of the controller that controls the data transfers over low- and medium-speed, switched and non switched transmission interfaces.

The TSS consists of up to six low-speed scanners (LSSs).

two-processor switch (TPS). A feature of the channel adapter that connects a second channel to the same channel adapter.

V.24,25,35. EIA/CCITT recommendations on transmission interfaces

X.20 bis, 21, 21 bis, 21 native, 25 CCITT recommendations on transmission interfaces

Bibliography

3745 Models 130, 150, and 170 Customer Documentation

| | | | |
|---|--|--|--|
| <div>Introduction</div> <div>GA33-0138</div> | Provides information for learning about and evaluating 3745 capabilities | <div>Configuration Program</div> <div>GA33-0093</div> | Provides information for configuring a 3745 |
| <div>S/370 I/O IHPP</div> <div>GC22-7064</div> | Provides information for doing physical site planning | <div>Preparing for Connection</div> <div>GA33-0140</div> | Provides information for preparing cable installation and LIC 5/6 configuration |
| <div>Principles of Operation</div> <div>SA33-0102</div> | Describes the 3745 instruction set in order to write or modify a control program | <div>Connection Integration Guide</div> <div>SA33-0141 *</div> | Provides information for installing and testing LICs and customizing the 3745 after installation |
| <div>Basic Operations Guide</div> <div>SA33-0146 *</div> | Provides procedures for carrying out daily routine operations | <div>Advanced Operations Guide</div> <div>SA33-0097 *</div> | Provides procedures for carrying out advanced operations and tests from the 3745 console |
| <div>Problem Determination Guide</div> <div>SA33-0096 *</div> | Provides procedures for performing problem determination | <div>OEMI</div> <div>SA33-0099</div> | Provides information for selecting or designing compatible interfaces for attachment to the 3745 |
| <div>Master Index</div> <div>SA33-0142 *</div> | Provides references to all 3745 models for customer documentation | <div>Console Setup Guide</div> <div>SA33-0158 *</div> | Provides information on setting consoles for the 3745 |
| <div>Remote Load./Activation Guide</div> <div>SA33-0161</div> | Provides information for loading and activating a remote controller | <div>Telecommun. Products Safety Handbook</div> <div>GA33-0126 *</div> | Recalls safety principles |

* This manual is part of the shipping group.

3745 Models 130, 150, and 170 Service Documentation

Product-Trained CE

Installation Guide

SY33-2067 *

Provides instructions
for installing or
relocating a 3745

Service Functions

SY33-2069 *

Describes the MOSS
functions used from
a 3745 console

Maintenance Information Procedures SY33-2070 *

Provides procedures
for isolating and fixing
a 3745 problem

Parts Catalog

S135-2012 *

Provides reference
information for
ordering 3745 parts

Product-Support-Trained CE

Hardware Maintenance Reference SY33-2066 *

Provides in-depth
hardware reference
information

Diagnostic Descriptions

SY33-2076 *

Describes the
3745 diagnostic
programs

External Cable References SY33-2075 *

Provides references
to console and line
cables used for
connecting a 3745

Service Master Index SY33-2079 *

Provides references
to 3745 models
130, 150, and 170
shipping group
documentation

Channel Adapter OLTs

D99-3745A

Provides procedures
to run the CA OLTs
on a 3745

* This manual is part of the shipping group.

Index

A

- A register (CCU) 2-19
- aa LIC5 FAILED 4-79
- aa LIC6 FAILED 4-90
- AC
 - detection 10-25
 - frequency 10-4
 - monitoring 10-25
- AC voltages input
 - adjustment 10-4
 - limits 10-4
- access methods 1-17
- access protocol (TRSS ring) 6-6
- actions taken during AIOs and PIOs (CCU) 2-45
- adapter check register (TIC) 6-25
- adapter interface check stop mode (CCU) 2-44
- adapter plugging rules 3-44
- adapter return codes 11-59
- adapters interconnection errors (CCU) 2-43
- adapters/CCU interconnection 3-5
- address
 - DCE, LIC type 6 4-87
- address exception
 - CCU 2-17
 - instruction fetch error (CCU) 2-43
 - program execution error (CCU) 2-43
- address register
 - LIC types 1 to 4 4-47
 - LIC types 5/6 (DTE function) 4-55
- addressing
 - CA 3-30
 - HPTSS line 3-41
 - LIC board 3-34
 - LIC1 LIC3 LIC4A and LIC4B 3-36
 - LIC5 and LIC6 3-38
 - line 3-35
 - line adapter (LSS and HSS) 3-32
 - logical adapter 3-29
 - logical, on LIC types 1 to 4 4-46
 - MOSS screen display CA 3-31
 - MOSS screen display LA 3-33
 - physical wiring 3-29
 - the lines in HSS 5-5
 - token-ring 3-43
 - token-ring adapter 3-42
 - token-ring line 3-43
 - TSS line LICs 1-4 3-37
 - TSS line LICs 5-6 3-40
- address/command tag 3-6
- aid
 - HSS microcode service aid 5-37
 - on HSS problem determination 5-37
 - on TRA problem determination 6-28

AIO

CA

- read indirect operation 3-24
- write indirect operation 3-25
- direct/indirect LA/TRA read 3-26
- direct/indirect LA/TRA write 3-27
- operation 3-18
- operation sequence
 - CSCW transfer 3-20
 - data transfer in read 3-23
 - data transfer in write 3-22
 - for CA (storage address transfer) 3-21
 - for LA (storage address transfer) 3-21
 - initialization 3-19
- TRA read direct operation 3-27

- air flow detector 10-26, 10-27
 - monitoring 10-26
 - principle 10-27
- alarm
 - tone detection, LIC type 6 4-87
- alarm/alert 11-17
- alter
 - CSP control storage 4-14
 - CSP external registers 4-14
 - CSP local storage 4-14
 - CSP ROS (read-only storage) 4-14
- alternate console 9-6
- analog
 - line analysis test 4-99
 - test from PKD 4-77
- arbitration mechanism (TRM) 6-18
- ARC 11-59
- asynchronous operation command
 - CHHITMIO input 4-29
 - FESA X'15' register 4-29
- autodiagnostics 7-21
- automatic BER analysis 11-19
- automatic FRU correlation 11-21
- automatic restart function 10-23
- autoselection (AS) 3-45
 - chain 7-11
 - error 7-12
 - mechanism 7-11

B

- background information
 - on PKD 4-75
- backup speed
 - LIC type 5 (DCE function) 4-71
- bad response
 - on PKD 4-76
- basic board DC voltages and tolerances 10-10

BCCA 7-3

BER

- alarm/alert 11-13
- composite 11-16
- detail screen 11-14
- display 11-8, 11-14
- error status 11-10
- file erasure 11-8
- format 11-6
- handling tools 11-11
- Id 11-9
- specific mechanism 11-13
- storage on disk 11-8
- structure 11-9
- type 11-9
- BER analysis 11-19
 - automatic analysis 11-19
 - automatic FRU correlation 11-21
 - CE field updating 11-20
 - correlation range 11-21
 - manual analysis 11-20
 - manual FRU correlation 11-21
- BER format on disk 11-99
- BER reference code 11-20, 11-22
- BER type description 11-9
- BER type 01 11-35, 11-40
 - summary 11-35
- BER type 01 - ID 00
 - detailed BER display 11-40
 - error code description 11-41
 - field description 11-40
 - field details 11-45
 - MOSS check codes 11-41
- BER type 01 formats 11-99
- BER type 01 ID 01
 - detailed BER display 11-51
 - field description 11-51
 - field details 11-52
- BER type 01 ID 02
 - detailed BER display 11-53
 - field description 11-53
 - field details 11-54
- BER type 01 ID 03
 - adapter return codes 11-59
 - detailed BER display 11-56
 - field description 11-56
 - field details 11-57
- BER type 01 ID 04
 - detailed BER display 11-60
 - field description 11-60
 - field details 11-60
- BER type 01 ID 05
 - detailed BER display 11-63
 - field description 11-65
- BER type 01 ID 06
 - detailed BER display 11-66
 - error 05 11-72
 - error 08 11-72

BER type 01 ID 06 (*continued*)

- error 09 11-73
- field details 11-68
- BER type 01 ID 07
 - field details 11-75
- BER type 01 ID 08 11-78
- BER type 01 ID 15 and 16 11-80
- BER type 01 ID 17 11-81
- BER type 01 ID 19 11-82
- BER type 01 ID 20 11-83
 - field details 11-85
- BER type 01 ID 21 11-88
 - field details 11-88
- BER type 01 ID 43 11-93
 - field details 11-93
- BER type 01 ID 44 11-97
- BER type 01 ID 50 11-98
- BER type 01 ID 80 11-98
- BER type 01 IDs 10 to 14 11-79
- BER type 01 IDs 16 and 1A to 1D 11-80
- BER type 01 IDs 24 to 29 and 37 11-89
- BER type 01 IDs 30 to 32 11-89
 - field description 11-90
- BER type 01 IDs 38 and 39 11-91
 - field details 11-92
- BER type 01 IDs 91, B3, C1, C2 11-98
- BER type 03
 - detailed BER display 11-106
 - formats 11-107
 - summary 11-106
- BER type 04
 - detailed BER display 11-108
 - field details 11-111
 - formats 11-114
 - RESP field 11-113
 - RESP/REQ codes 11-112
 - summary 11-108
- BER type 10
 - detailed BER display 11-120
 - field description 11-123
 - formats 11-124
 - summary 11-115
- BER type 11
 - detailed BER display 11-131
 - field description 11-134
 - formats 11-136
 - summary 11-127
- BER type 12
 - field description 11-139
 - formats 11-140
 - summary 11-138
- BER type 13
 - detailed BER display 11-142
 - field description 11-143
 - formats 11-144
 - summary 11-141
- BER type 14
 - detailed BER display 11-145

- BER type 14 (*continued*)
 - field description 11-146
 - format 11-146
 - summary 11-145
- BER type 15
 - detailed BER display 11-149
 - field description 11-152
 - formats 11-153
 - summary 11-147
- BER which are not machine errors 11-12
- bibliography xii
- BPC card plugging rules 3-44
- BPC1 3-28
- BPC2 3-28
- branch trace 8-9
- branch trace buffer 8-9
- bridges (token-ring) 6-7
- BTAM 1-17
- BTAM-ES 1-17
- buffer chaining channel adapter 7-3
- burst count checker (DMA) 5-25
- bus
 - DMA 3-9
 - interconnection control (TIC) 6-13
 - IOC 3-3
 - layout 3-4
 - main 3-3
 - propagation cards 3-28
 - signal lines summary of the TIC bus 6-17
 - summary of the IOC bus interface signal lines 6-16
 - to TIC interconnection 6-16
- bus propagation cards 3-28
- bus terminator connector pin assignment 3-55
- busy TC on
 - on PKD 4-76
- buzzer control
 - on PKD 4-78
- bypass mechanism for LAs or CAs 3-44

C

- CA
 - level 3 interrupt 7-15
- CA addressing 3-30
- CA BER
 - See ?
- CA BER formats 11-124
- CA bypass mechanism 3-44
- CA IPL detect 3-8
- CA plugging rules 3-44
- CA (channel adapter)
 - autoselection (AS) 7-11
 - initialization 7-23
 - instructions 7-8
 - interface display 7-23
 - interrupt requests 7-15
 - level 1 interrupt 7-15
 - operating environment 7-7

- CA (channel adapter) (*continued*)
 - services 7-23
 - states 7-8
 - testing and checking hardware 7-21
 - wrap plugs 7-22
- cable
 - diagrams (HSS) 5-42
 - length limitations (HSS) 5-42
 - LIC types 1 to 4 4-100
 - TSS 4-100
 - V.35
 - example of two cables connected (HSS) 5-41
 - X.21
 - example of two cables connected (HSS) 5-41
- cabling system (TRSS ring) 6-4
- cache storage (CCU) 2-16
- capacity of the 3745 1-5
- card EC level
 - LIC type 5 (DCE function) 4-71
- card replacement
 - SMUX 4-40
- carrier detector sensitivity
 - LIC type 5 (DCE function) 4-70
- CA/MOSS connection 7-14
- CCITT
 - LIC type 5 (DCE function) 4-70
 - loop 3, LIC type 5 (DCE function) 4-72
 - mode, LIC type 5 (DCE function) 4-62, 4-63
- CCU
 - cpckaging 2-3
 - cycle 2-4
 - data flow 2-3
 - detected hardware errors 2-40
 - detected not hard errors 2-40
 - diagnostics 2-40
 - environment 2-11
 - error detection 2-42
 - error handling 2-40
 - error handling summary 2-41
 - functional description 2-4
 - general description 2-3
 - hard errors 2-36
 - in 3745 data flow 2-2
 - registers 2-20
 - storage interconnection 2-16
 - storage line invalidation 2-17
 - storage read policy (CCU) 2-17
 - storage write policy 2-17
 - subsystem POR 2-12
 - timers 2-18
 - to and from adapters 2-19
 - to and from MOSS 2-39
- CCU BER
 - See BER type 13
- CCU BER formats 11-144
- CCU bus 3-3, 3-5
 - function 3-5

- CCU to MOSS communication 8-12
- CCUI logic 2-14
- CCU/adapters interconnection 3-5
- CE field updating
 - See BER analysis
- central control unit (CCU) 2-1
- channel adapter addresses 3-31
- channel adapter bypass mechanism 3-44
- channel adapter plugging rules 3-44
- channel signals used by the CA 7-10
- channel stop 7-20
- channel wrap 7-21
- characteristics
 - LIC types 1 to 4 4-9
 - LIC types 5/6 4-10
- check register decoding (TIC adapter) 6-25
- check stop mode (CCU) 2-40
- checkers 2-41
- checking the checkers (CCU) 2-41
- CLDP-HSS microcode exchange 5-9
- clear (X.21) 4-33
- clock
 - CSP 4-17
 - failure (FESH DCE) 5-21
- clocking
 - direct mode 4-51
 - external mode 4-51
 - HSS line 5-42
 - internal mode 4-50
 - 3745 mode 4-51
- CMD FROM DTE 4-79, 4-90
- CMD FROM LINE 4-79, 4-90
- command rejection
 - on PKD 4-76
- commands
 - definition 4-22
 - disk/diskette 8-17
 - in CE mode, from PKD 4-78
 - LIC type 5 configuration 4-71
 - LIC type 5 problem determination 4-71
 - mailbox 8-13
 - problem determination, LIC type 6 4-87
 - scanner 4-20
 - TSS, LIC type 6 4-87
- communication
 - CCU to MOSS 8-12
 - interfaces of HSS 5-40
 - MOSS to CCU 8-12
- communication scanner processor
 - See CSP (communication scanner processor)
- communication scanner processor (HSS) 5-10
- communication subsystem 1-7
- component location
 - primary power box 10-5
 - PS1 10-8
- composite BER 11-16, 11-31
- conditional branch trace 8-10
- CONFIG FROM HOST 4-79
- CONFIG FROM LINE 4-79
- CONFIG MISMATCH 4-79
- configuration
 - BPC1/BPC2 rules 3-28
 - CA with TPS 7-5
 - commands (LIC type 5, DCE function) 4-71
 - DSU/CSU, LIC type 6 4-88
 - from PKD 4-78
 - LIC type 5 (DCE function) 4-58, 4-67, 4-73
 - LIC type 6 4-81, 4-85, 4-90
 - LIC types 1 to 4 4-46
 - options for LIC type 6 4-82
 - options, LIC type 5 (DCE function) 4-60
 - (CA) 7-4
- configuration rules BPC1/BPC2 cards 3-28
- connection
 - DMA bus to FESH 5-10
 - FESH to CSP 5-9
 - IOC bus to CSP (HSS) 5-9
 - LIC type 6 to DDS 4-80
 - LIC type 6, limited distance 4-80
- console
 - connection 9-7
- console attachment
 - alternate 1-15
 - local 1-15
 - remote 1-15
 - RSF 1-15
- console sharing via IBM 7427 9-7
- consoles tail gate 9-7
- contact sense/operate
 - from PKD 4-78
- contingent allegiance 7-17
- control panel 9-2, 9-3
 - connection 9-5
 - operation 9-5
 - overview 9-2
 - reference card 9-4
- control program
 - See also NCP
 - generation 1-20
 - loading 1-20
 - loading from disk, automatic 1-20
 - multiple load module 1-20
- control register
 - LIC types 1 to 4 4-47
 - LIC types 5/6 (DTE function) 4-55
- control ROS parity error (CCU) 2-42
- control storage
 - CSP 4-14
- control subsystem 1-6
- controller structure 1-6
- controller-resident programs 1-19
- cpckaging
 - CCU 2-3
 - HSS 5-4
 - TRSS 6-9

- cparameters
 - for HSS customization 5-23
- cpartitioning the functions in SCTL 2-14
- CSP (communication scanner processor)
 - components 4-12
 - control storage 4-14
 - data flow 4-12
 - definition 4-12
 - error management 4-17
 - external registers 4-14
 - external registers usage 4-17
 - FES 4-6
 - FESA interconnection 4-27
 - FESA (front-end scanner adapter) 4-7
 - FESL 4-6
 - general information 4-6
 - hardstop 4-17
 - layer (HSS) 5-13
 - local storage 4-14
 - of the HSS 5-10
 - program levels 4-17
 - programmed reset PIO 4-19
 - reset 4-19
 - ROS (read-only storage) 4-14
 - scanner commands 4-20
 - scanner states 4-18
- CSP-to-IOC bus connection (HSS) 5-9
- CSS 1-6
- CSU
 - configuration, LIC type 6 4-88
 - information, LIC type 6 4-89
 - LIC type 6 4-86
- CTS state confirmation (FESH) 5-20
- customization parameters (HSS) 5-23
- cycle steal
 - grant 3-45
 - pointer allocation (CCU) 2-20
- cycle steal (CS) 7-13
 - chain 7-13
 - grant high 3-6
 - grant low 3-6
 - request high 3-6
 - request low 3-6
- D**
- D register (CCU) 2-19
- data
 - format with LIC type 6 4-82
- data bus bytes 0 and 1 3-8
- data bus parity checker (DMA) 5-25
- data encoding and modulation
 - LIC type 5 (DCE function) 4-61
- data flow
 - buses 3-2
 - CA 7-6
 - CCU 2-3
 - CCU in 3745 2-2
 - HPTSS 5-7
- data flow (*continued*)
 - HPTSS in 3745 5-3
 - IOC (CCU) 2-19
 - LIC type 5 (DCE function) 4-57
 - LIC type 6 4-80
 - power control 10-15
 - TIC 6-11
 - TRSS in 3745 6-2
 - 3745 1-4
- data management
 - HSS 5-10
 - HSS CSP layer 5-13
- data RAM
 - FESA 4-30
- data reception (HSS) 5-10
- data streaming 7-4
- data tag 3-6
- data transfer methods 7-8
- data transfer state (CA) 7-8
- data transmission (HSS) 5-10
- data value register (CCU) 2-39
- DC voltage test points
 - PS1 10-8
- DC voltages and tolerances
 - CSP, FESH cards 10-11
 - disk 10-13
 - diskette 10-13
 - PS1 10-9
 - PS2 10-12
- DCE
 - address, LIC type 5 4-69
 - address, LIC type 6 4-87
 - information (on PKD) 4-75
- DCE clock failure (FESH) 5-21
- DCE to telephone line interface
 - LIC type 5 4-63
- DDS LINE DOWN 4-90
- DDS OOS or DDS OOF 4-90
- DDS (digital data service)
 - LIC type 6 connection 4-80
 - line specifications 4-84
 - loop, LIC type 6 4-87
 - speed for LIC type 6 4-81
- debugging
 - aid for LIC types 1 to 4 4-92
 - aid for LIC types 5/6 4-95
- DEFAULT CONFIG 4-90, 4-91
- default speed
 - LIC type 5 (DCE function) 4-69
- definitions
 - DMUX (double multiplexer card) 4-7
 - FES (front end scanner) 4-22
 - FESA (front-end scanner adapter) 4-26
 - LIC board 4-7
 - LIC (line interface coupler) 4-9
 - LSS (low-speed scanner) 4-6
 - MUX (multiplexer card) 4-7
 - SMUX (single multiplexer card) 4-8

definitions (*continued*)

- TSS (transmission subsystem) 4-5
- description
 - FESA 4-28
- description of the BER type 11-9
- diagnostic BER
 - See BER type 03
- diagnostic BER formats 11-107
- diagnostic section TA0A warning 6-19, 6-28
- diagnostics
 - CCU 2-40
 - facilities (HSS) 5-37
- digital test
 - from PKD 4-77
- direct memory access
 - CCU 2-13
- direct memory access operation (TRA) 6-17
- direct mode (clocking)
 - See 3745 mode (clocking)
- disable
 - LIC types 1 to 4 line 4-44
 - LIC types 5/6 (DTE function) line 4-55
- disabled
 - LIC 4-31
- disabled state (CA) 7-9
- disconnected 4-18
 - disconnected-go 4-19
- disconnected-go 4-19
- disconnected-stop 4-19
- disk drive (HDD) 9-9
- diskette drive 9-10
 - description 9-10
 - part number 9-10
 - removal and replacement procedure 9-10
- disk/diskette commands 8-17
- disk/diskette drive 9-9
- disk/diskette drive ON/OFF control 10-13
- display
 - CSP control storage 4-14
 - CSP external registers 4-14
 - CSP local storage 4-14
 - CSP ROS (read-only storage) 4-14
- DMA
 - burst count checker 5-25
 - bus 3-9
 - bus during read operation 3-12
 - bus during write operation 3-13
 - bus interconnection layout 3-10
 - bus physical interconnection 3-9
 - bus to FESH connection 5-10
 - data bus parity checker 5-25
 - DMA bus errors reported by FESH 5-27
 - errors reporting 5-26
 - HSS DMA manager layer 5-13
 - interconnection errors detected by FESH 5-25
 - logic (CCU) 2-14
 - operation (TRA) 6-17
 - size 5-23

DMA (*continued*)

- tag sequence 5-25
- time out 5-25
- DMA-to-SCTL bus line function 3-10
- DMUX (double multiplexer card)
 - definition 4-7
 - functional description 4-37
 - functions 4-35
 - reset 4-37
- double multiplexer card
 - See DMUX (double multiplexer card)
- DSR 4-32
 - confirmation (FESH) 5-19
 - integration timer (HSS) 5-23
- DSU
 - configuration, LIC type 6 4-88
 - information, LIC type 6 4-89
 - LIC type 6 4-86
- DTE clocking
 - LIC types 1 to 4 4-9
 - LIC types 5/6 4-10
- DTE function
 - LIC types 5/6 4-54
- D1/D2 register parity errors (two errors) (CCU) 2-42

E

- ECC and MCTL (CCU) 2-14
- effect of selective reset on CA 7-19
- effect of system reset on CA 7-18
- ELCS (initial status = B'110') for HSS 5-35
- enable
 - LIC types 1 to 4 line 4-44
 - LIC types 5/6 (DTE function) line 4-55
- enable clock mode
 - LIC types 1 to 4 4-47
- enabled
 - LIC leads 4-31
- end of chain 3-7
- ending status
 - normal tagged status 7-17
 - tagged DE status 7-17
 - untagged asynchronous status 7-18
- environment system for HSS 5-4
- EP 1-19
- error
 - adapter interface check stop mode (CCU) 2-44
 - adapters interconnection errors (CCU) 2-43
 - address exception instruction fetch error (CCU) 2-43
 - address exception program execution error (CCU) 2-43
 - CCU detected hardware errors 2-40
 - CCU detected not hard errors 2-40
 - CCU hard errors 2-36
 - control ROS parity error (CCU) 2-42
 - detected by TRM (format 1) 6-22
 - detection and reporting
 - HSS 5-23
 - TRM 6-20

error (*continued*)

- detection (CCU) 2-42
- DMA bus errors reported by FESH 5-27
- DMA interconnection errors detected by FESH 5-25
- DMA/SCTL reporting 5-26
 - during MOSS AIOs (CCU) 2-44
 - during program AIOs (CCU) 2-44
- D1/D2 register parity errors (two errors) (CCU) 2-42
- handling summary (CCU) 2-41
- handling (CCU) 2-40
- hard stop error status (detected by CSP hardware), (HSS) 5-30
- hardware error detection and reporting (HSS) 5-24
- hardware errors (CCU) 2-42
- internal box error (IBE) reporting (HSS) 5-24
- level 5 I/O error (CCU) 2-43
- local storage parity error (CCU) 2-42
- MIOC parity error (CCU) 2-42
- MOSS address exception error 2-45
- MOSS data operand register (MDOR) parity error (CCU) 2-42
- MOSS interconnection type errors 2-45
- MOSS OP error 2-45
- POP parity error (CCU) 2-42
- program errors (CCU) 2-43
- program/hardware (HSS) 5-23
- SAR parity error (CCU) 2-42
- SCTL card detected errors reported by FESH 5-26
- sequence (HSS) 5-23
- status register (level 2) (TRM) 6-22
- status register (MOSS) (TRA) 6-24
- status (HSS) 5-29
- storage protect instruction fetch error (CCU) 2-43
- storage protect program execution error (CCU) 2-43
 - with MOSS user (MIOH) (CCU) 2-44
 - with program user (IOH, IOHI) (CCU) 2-44
- Z register parity error (CCU) 2-42
- error alert
 - from CP 7-20
 - from MOSS 7-20
- error count 11-5
- error management
 - CSP 4-17
- error status 11-10
- ESC mode 7-7
- exchange time out 8-11
- extended LCS (ELCS) for HSS 5-35
- external mode (clocking) 4-51
- external registers
 - CCU 2-20
 - CSP 4-14
 - FESA X'13' 4-29
 - FESA X'15' 4-29
 - line interface address 4-29

external wrap facility (HSS) 5-38

F

- fan stacked faults 10-27
 - faults logging 10-27
- FDD ON/OFF command 10-13
- features
 - CA 7-4
- FES (front end scanner)
 - data flow 4-22
 - function 4-6
 - power ON reset 4-25
 - programmed reset 4-25
 - RAM A 4-23
 - RAM B 4-23
 - RAM C 4-23
 - storages 4-23
 - storages display 4-23
- FESA (front-end scanner adapter) 4-7
 - CSP interconnection 4-27
 - data flow 4-26
 - data RAM 4-30
 - definition 4-26
 - description 4-28
 - external register X'13' 4-29
 - external register X'15' 4-29
 - inbound and outbound control RAM 4-29
 - inbound/outbound RAM addressing 4-29
 - inbound/outbound RAM layout 4-29
 - local store 6 4-29
 - RAM organization 4-28
 - serial link interconnection 4-27
- FESH
 - card 5-11
 - CTS state confirmation 5-20
 - DCE clock failure 5-21
 - DCE interface 5-40
 - DMA bus connection 5-10
 - DMA bus errors reported by FESH 5-27
 - DSR confirmation 5-19
 - end of receive 5-17
 - flush command 5-18
 - flush end of frame command 5-18
 - hardware functions 5-14, 5-16
 - interconnection to CSP 5-9
 - internal checkers 5-28
 - microcode 5-9
 - modem interface management 5-19
 - modem retrain 5-21
 - modem-in management 5-19
 - modem-out management 5-21
 - receive
 - command 5-16
 - continue command 5-17
 - flow 5-17
 - operation for I-frame 5-17
 - reset 5-14
 - SCTL card detected errors reported by FESH 5-26

FESH (continued)

- stop receive command 5-18
- FESL 4-6
 - reset 4-24
- fields analysis 11-19
- final status field (FSF)
 - bit definition 5-33
- flush command (FESH) 5-18
- flush end of frame command (FESH) 5-18
- format fol1 11-146
- format of a BER 11-6
- format 1 (error detected by TRM) 6-22
- format 2 (interrupt request by the TIC) 6-23
- formats foCxx 11-124
- formats foDxx 11-107
- formats foMxx 11-99
- formats foNxx 11-140
- formats foPxx 11-114
- formats foRxx 11-153
- formats foTxx 11-136
- formats foUxx 11-144
- frame
 - in serial link 4-34
 - slots 4-34
- frame format (token-ring) 6-6
- frequency (AC) 10-4
- front-end scanner
 - See FES (front end scanner)
- front-end scanner adapter (FESA)
 - See FESA (front-end scanner adapter)
- front-end scanner high-speed (FESH) card 5-11
- FRU correlation
 - See BER analysis
- FRU list 11-10
- FSF 5-33
- function partitioning in SCTL card 2-14
- functional description
 - CCU 2-4

G

- general description
 - bus 3-3
 - CCU 2-3
 - channel adapter (CA) 7-3
 - control panel 9-2
 - diskette drive 9-10
 - hard disk drive 9-9
 - MOSS 8-3
 - operator consoles 9-6
- general information 1-1
- generation of line ID (TRA) 6-23

H

- halt 3-7
- hard disk drive 9-9
 - description 9-9
 - part number 9-9

hard disk drive (continued)

- removal and replacement procedures 9-9
- hard stop error status (detected by CSP hardware), (HSS) 5-30
- hard stop transmit command (HSS) 5-16
- hardstop
 - CSP 4-18
- hardware error status (initial status = B'111') 5-36
- hardware error status (initial status = B'111') for HSS 5-36
- hardware errors
 - CCU detected 2-40, 2-42
 - detection and reporting (HSS) 5-24
- hardware functions (FESH) 5-16
- hardware registers (CCU) 2-38
- HDD 9-9
- HDD ON/OFF command 10-13
- hexadecimal codes 11-30
- hexadecimal codes versus mosscheck code 11-30
- high and low resolution timer (CCU) 2-18
- high performance transmission subsystem (HPTSS)
 - introduction 5-3
- high-performance transmission subsystem 1-11
- host support
 - LIC type 5 (DCE function) 4-71
 - LIC type 6 4-87
- host-resident programs 1-17
- HPTSS 1-11
 - data flow 5-7
 - in 3745 data flow 5-3
- HPTSS line addressing 3-41
- HSS 5-22
 - commands NCP 5-6
 - communication interfaces 5-40
 - cpckaging 5-4
 - CSP 5-10
 - CSP layer 5-13
 - CSP-to-IOC bus connection 5-9
 - customization parameters 5-23
 - data reception 5-10
 - data transmission 5-10
 - diagnostic facilities 5-37
 - DMA manager layer 5-13
 - ELCS (initial status = B'110') 5-35
 - error status 5-29
 - hard stop transmit command 5-16
 - hardware error status (initial status = B'111') 5-36
 - IBE (initial status = B'110') 5-34
 - in system environment 5-4
 - interface FESH-DCE 5-40
 - interface types 5-6
 - internal interconnections 5-9
 - introduction 5-4
 - line addressing 5-5
 - line interface check 5-29
 - microcode
 - functions 5-14, 5-16
 - service aid 5-37

HSS (*continued*)

- modem and data management 5-10
- problem determination aid 5-37
- receive
 - operation 5-16
- soft stop transmit command 5-16
- time out values used 5-22
- transmit
 - command 5-15
 - initial command 5-14
 - operation 5-14

HSS CSP

- data management layer 5-13
- interconnection errors 5-27
- microcode
 - differences between HSS and LSS 5-8
 - summary 5-7
- modem-in layer 5-12
- modem-out layer 5-12
- receive layers 5-12
- transmit layers 5-12

I

- I-frame receive operation (FESH) 5-17
- IACK operation (TRM) 6-17
- IBE HSS (initial status = B'110') 5-34
- IBM Token-Ring network 6-3
- ICF (internal clock function) 4-11, 4-50
 - LIC types 1 to 4 4-50
- identification of the 3745 1-5
- IML
 - status of the HSS scanner after IML 5-13
- implicit allegiance 7-17
- in mailbox 8-12
- inbound/outbound RAM
 - addressing (FESA) 4-29
 - control (FESA) 4-29
 - external registers 4-29
 - layout (FESA) 4-29
- initial selection state (CA) 7-8
- initial status field (ISF) bit definition 5-32
- initial status = B'110' (internal box error HSS) 5-34
- initialized 4-18
- inoperative 4-18
- input and output X'7x' register bits (CCU) 2-27
- input instructions
 - details (CCU) 2-24
- input instructions (CCU) 2-22
- input/output 3-6
- input/output X'7x' instructions (CCU) 2-24
- instantaneous allegiance 7-17
- instruction
 - address register (CCU) 2-20, 2-38
- instruction set (CCU) 2-9
- interconnection
 - adapter's interconnection errors (CCU) 2-43
 - bus control (TIC) 6-13
 - CCU-to-storage 2-16

interconnection (*continued*)

- DMA bus to FESH 5-10
- errors (DMA) detected by FESH 5-25
- errors (HSS CSP) 5-27
- FESA-CSP 4-27
- FESA-serial link 4-27
- FESH to CSP 5-9
- HSS internal interconnections 5-9
- MOSS type errors 2-45
- PCC 10-16
- PCC card to MOSS 10-17
- PCC card to control panel 10-18
- PCC card to power supply signal 10-18
- SCTL-to-CCU cache 2-15
- TIC to bus 6-16
- TRA IOC bus 6-15

interface

- check stop mode (adapter) (CCU) 2-44
- check (HSS line) 5-29
- communication interfaces of HSS 5-40
- DCE to telephone line (LIC type 5) 4-63
- FESH-DCE 5-40
- LIC types 1 to 4 4-100
- LIC types 1 to 4 lines 4-43
- types (HSS) 5-6
- X.21 (HSS) 5-41
- interface coupler (TIC) card 6-7
- interface disconnect 7-20
- internal box error status HSS (initial status = B'110') 5-34
- internal box error (IBE)
 - IBE reporting (HSS) 5-24
- internal checkers (FESH) 5-28
- internal clock function
 - See ICF (internal clock function)
- internal mode (clocking) 4-50
- interrupt
 - CA 7-9
 - IACK operation (TRM) 6-17
 - request by the TIC (format 2) 6-23
- interrupt request removed 3-6
- interrupts
 - level 1 interrupt reporting (CCU) 2-19
 - level 1 (CCU) 2-7
 - level 2 and level 3 interrupt reporting (CCU) 2-19
 - level 2 (CCU) 2-7
 - level 3 (CCU) 2-7
 - level 4 (CCU) 2-7
 - level 5 (CCU) 2-7
 - mechanism (CCU) 2-6
 - request determination (CCU) 2-6
 - request sources (CCU) 2-7
 - setting/resetting interrupt requests (CCU) 2-6
- interrupts (CCU) 2-5
- introduction
 - power control subsystem 10-14
 - power subsystem 10-3
 - to HSS 5-4

- INV PATTERN RCV 4-90
- invalid OP-code (CCU) 2-43
- IOC
 - bus interconnection (TRA) 6-15
 - bus-to-CSP interconnection (HSS) 5-9
 - control logic (CCU) 2-19
 - data flow (CCU) 2-19
- IOC BER
 - See BER type 14
- IOC BER format 11-146
- IOC bus 3-3
 - physical interconnection 3-8
 - protocol 3-3
 - scoping routine 3-49
 - adapter selection 3-50
 - ERC meaning 3-52
 - error bit 3-52
 - examples 3-53
 - how to start 3-49
 - parameter description 3-50
 - RAC meaning 3-51
 - RACs generated 3-51
 - terminator connector pin assignment 3-55
- IOC bus and adapter errors 11-25
- IOCDS 7-7
- IPL
 - automatic 1-20
- IPL automatic 1-20
- IPL BER 11-34
- IPL error 11-67
- ISF bit definition 5-32
- I/O
 - configuration data set (IOCDS) 7-7
 - error alert from CP 7-20
 - error alert from MOSS 7-20

K

- KEY n STUCK 4-79, 4-90
- keying procedures
 - on PKD 4-76

L

- LA bypass mechanism 3-44
- LA plugging rules 3-44
- lagging address register (CCU) 2-38
- lamp test
 - PKD 4-75
- LCS 5-31
- LD
 - LIC type 6 4-86
- LDM LINE DOWN 4-90
- lead state confirmation
 - on V.35 modem-in leads (FESH) 5-19
 - on X.21 modem-in leads (FESH) 5-20
- level 1
 - error status register (TRM) 6-20
 - interrupt reporting (CCU) 2-19

- level 1 (*continued*)
 - interrupt request (CA) 7-15
- level 2
 - error status registers (TRM) 6-22
 - interrupt reporting (CCU) 2-19
- level 3
 - interrupt reporting (CCU) 2-19
- level 3 interrupt request (CA) 7-15
- level 5
 - I/O error (CCU) 2-43
- library for service 1-21
- LIB1/LIB2/LIB3 4-7
- LIC board 1-9
 - definition 4-7
- LIC board addressing 3-34
- LIC boards 01L-A1 and 01L-A2 DC voltages and tolerances 10-11
- LIC boards 01M-A1 and 01M-A2 DC voltages and tolerances 10-11
- LIC type 4
 - personalization 4-48
- LIC type 5
 - configuration from PKD 4-78
 - multipoint 4-59
 - panel 4-65
 - point-to-point 4-58
 - PT2/3 connection 4-79
 - to LIC type 5 connection point-to-point 4-58
 - to LICs type 5 connection multipoint 4-59
 - to one tailed 586X connection multipoint 4-60
 - to tailed 586X connection 4-59
 - point-to-point 4-59
 - to 586X or 786X connection 4-58
 - to 586Xs connection 4-59
- LIC type 5 (DCE function)
 - alarm tone detection 4-73
 - backup speed 4-71
 - card EC level 4-71
 - carrier detector sensitivity 4-70
 - CCITT 4-70
 - CCITT mode 4-62, 4-63
 - configuration 4-73
 - configuration commands 4-71
 - configuration options 4-60
 - configurations 4-58
 - data encoding and modulation 4-61
 - data flow 4-57
 - DCE address 4-69
 - DCE to telephone line interface 4-63
 - default speed 4-69
 - host support 4-71
 - line quality threshold 4-70
 - line specifications 4-65
 - line spectrum 4-65
 - LPDA-2 hit count threshold 4-70
 - LPDA-2 enabled 4-70
 - maintenance approach 4-57
 - manual tests 4-72

\ LIC type 5 (DCE function) *(continued)*

- microcode EC level 4-71
- multipoint - LIC type 5 to LICs type 5 4-59
- multipoint - LIC type 5 to one tailed 586X 4-60
- multipoint - LIC type 5 to 586Xs 4-59
- native mode 4-62, 4-63
- options and configurations 4-67
- point-to-point - LIC type 5 to LIC type 5 4-58
- point-to-point - LIC type 5 to tailed 586X 4-59
- point-to-point - LIC type 5 to 586X or 786X 4-58
- point-to-point/multipoint 4-69
- problem determination commands 4-71
- receive level threshold 4-70
- RFS delay 4-64
- speed setting 4-58
- speeds 4-57
- surge protection 4-64
- tone characteristics 4-73
- transit time 4-64
- transmit clock control 4-70
- transmit level 4-70
- TSS commands 4-72

LIC type 6

- plugging limitations 4-10

LIC type 6 (DSU/CSU function)

- alarm tone detection 4-87
- configuration 4-90
- configuration options 4-82
- configurations 4-81
- connection to US DDS 4-80
- data flow 4-80
- data format 4-82
- DCE address 4-87
- DDS loop 4-87
- DSU/CSU configuration 4-88
- DSU/CSU information 4-89
- DSU/CSU to line interface 4-82
- DSU/CSU/LD 4-86
- host support 4-87
- limited distance connection 4-80
- line specifications 4-84
- local loop back 4-89
- maintenance 4-80
- manual tests 4-91
- modulation 4-82
- network services 4-86
- options and configurations 4-85
- panel 4-84
- PKD command rejection 4-89
- PKD use 4-88
- point-to-point/multipoint 4-86
- POR bring-up information 4-89
- problem determination commands 4-87
- PT2/3 4-91
- RFS delay 4-83
- speed change 4-89
- speed control 4-87
- speed setting 4-81

LIC type 6 (DSU/CSU function) *(continued)*

- speeds 4-81
- surge protection 4-83
- timing sources 4-86
- tone characteristics 4-88
- tone reception 4-88
- transit time 4-83
- TSS commands 4-87
- unsolicited messages 4-90

LIC types 1 to 4

- address register 4-47
- cards 4-43
- characteristics 4-9
- control register 4-47
- DTE clocking 4-9
- enable clock mode 4-47
- interface lines 4-43
- interfaces and cables 4-100
- Internal clock function (ICF) 4-50
- line enable/disable 4-44
- line interface 4-9
- logical addressing 4-46
- loop 1 on V.24 4-51
- loop 1 on V.25 4-52
- loop 1 on X.21 4-52
- loop 3 on V.24 4-52
- loop 3 on X.21 4-52
- protocols 4-9
- reset 4-44
- RTS 4-48
- selective scanning 4-45
- swap 4-46
- transfer mode 4-9
- transmission speed 4-9
- transmit/receive mechanism 4-44
- wraps 4-51

LIC types 1 to 4 clocking

- direct mode 4-51
- external mode 4-51
- internal mode 4-50
- 3745 mode 4-51

LIC types 1, 2 and 3

- transmit clock gating by RFS 4-48

LIC types 5/6

- characteristics 4-10
- DTE clocking 4-10
- line interface 4-10
- protocols 4-10
- transfer mode 4-10
- transmission speed 4-10

LIC types 5/6 DTE function

- address register 4-55
- control register 4-55
- LIC reset 4-55
- line enable/disable 4-55
- loop 3 on V.24 4-56
- selective scanning 4-55
- swap 4-55

- LIC types 5/6 DTE function (*continued*)
 - transmit/receive mechanism 4-54
 - wraps 4-55
- LIC (line interface coupler)
 - definition 4-9
 - disabled 4-31
 - enabled leads 4-31
 - LIC line analysis procedures 4-100
 - line weight 4-10
 - modem-in process for non X.21 lines 4-48
 - modem-in process for X.21 lines 4-48
 - reset 4-38, 4-42
 - serial link connection to LICs5/6 4-34
 - swap 4-46
- LIC1 LIC3 LIC4A and LIC4B addressing 3-36
- LIC5 and LIC6 addressing 3-38
- limited distance
 - LIC type 6 connection 4-80
 - line specifications 4-84
 - speed for LIC type 6 4-81
- line adapter addressing (LSS and HSS) 3-32
- line adapter bypass mechanism 3-44
- line adapter plugging rules 3-44
- line addressing 3-35
- line characteristics
 - France 4-67
 - Japan 4-67
 - M.1020 4-66
 - M.1025 4-66
 - UK 4-67
 - 3002 channel (US) 4-66
- line clocking (HSS) 5-42
- line communication status (LCS) 5-31
- line enable/disable
 - LIC types 5/6 (DTE function) 4-55
- line function 3-5
 - address/command tag 3-6
 - CA IPL detect 3-8
 - cycle steal grant high 3-6
 - cycle steal grant low 3-6
 - cycle steal request high 3-6
 - cycle steal request low 3-6
 - data bus bytes 0 and 1 3-8
 - data tag 3-6
 - DMA-to-SCTL bus 3-10
 - halt 3-7
 - input/output 3-6
 - interrupt request removed 3-6
 - modifier 3-7
 - out (R/W) 3-7
 - parity valid 3-7
 - reset 3-8
 - scanner interrupt 3-8
 - valid byte 3-7
 - valid halfword 3-7
- line identification (line ID) generation (TRA) 6-23
- line interface
 - LIC types 1 to 4 4-9
- line interface (*continued*)
 - LIC types 5/6 4-10
- line interface address
 - asynchronous operation command 4-29
 - FESA X'13' register 4-29
- line interface check (HSS) 5-29
- line interface coupler
 - See LIC (line interface coupler)
- line interface couplers 1-10
- line quality threshold
 - LIC type 5 (DCE function) 4-70
- line specifications
 - LIC type 5 (DCE function) 4-65
 - LIC type 6 4-84
- line spectrum
 - LIC type 5 (DCE function) 4-65
 - native 4-65
 - V.27 bis 4-65
 - V.29 4-65
 - V.33 4-66
- line weight
 - LIC 4-10
- Link Problem Determination Aid
- LLAP
 - See LIC (line interface coupler), LIC line analysis procedures
- local
 - attachment (HSS) 5-42
 - status 4-98
- local console 9-6
- local loop
 - from PKD 4-77
- local self-test
 - LIC type 5 4-96
 - LIC type 6 4-97
- local storage
 - CSP 4-14
- local storage parity error (CCU) 2-42
- logical adapter address 3-29
- logical addressing
 - LIC types 1 to 4 4-46
- long-term allegiance 7-17
- loop
 - DDS, LIC type 6 4-87
 - (local) from PKD 4-77
- loop back
 - local, LIC type 6 4-89
- loop or wrap tests for HSS V.35 and X.21 5-39
- loop 1
 - on V.24 (LIC types 1 to 4) 4-51
 - on V.25 (LIC types 1 to 4) 4-52
 - on X.21 (LIC types 1 to 4) 4-52
- loop 2
 - remote loop back (LIC 5/6) 4-96
- loop 3
 - LIC type 6 4-87
 - local loop back (LIC 5/6) 4-96
 - on V.24 (LIC types 1 to 4) 4-52

- loop 3 (*continued*)
 - on V.24, LIC types 5/6 (DTE function) 4-56
 - on X.21 (LIC types 1 to 4) 4-52
- loosely coupled 7-16
- low-speed scanner 1-8
 - See *also* LSS (low-speed scanner)
- LPDA-2
 - enabled (LIC type 5) 4-70
 - hit count threshold (LIC type 5) 4-70
- LSS (low-speed scanner)
 - definition 4-6
- LSSD
 - data flow 8-15
 - operation 8-15
 - testing circuit 8-15

M

- mailbox 8-11, 8-12
- mailbox commands 8-13
- main line survey 10-25
- main storage protection state (CCU) 2-17
- main storage (CCU) 2-12
- mains voltage
 - adjustment 10-4
 - limits 10-4
- maintenance 1-23
 - aids 1-23
 - console 9-8
 - LIC type 5 (DCE function) 4-57
 - LIC type 6 4-80
 - philosophy 1-23
 - tools and test equipment 1-23
- maintenance and operator subsystem 1-13
- maintenance temporary address register (MTAR) (CCU) 2-39
- maintenance temporary data register (MTDR) (CCU) 2-39
- Manchester encoding
 - description 4-35
 - SMUX 4-39
- MAND DDS LOOP 4-91
- manual BER file correlation
 - See BER analysis
- manual test
 - from PKD (LIC types 5/6) 4-95
 - LIC type 5 (DCE function) 4-72
- manual versus scheduled power ON 10-23
- manual V.35/X.21 wrap or loop tests 5-39
- MCTL and ECC (CCU) 2-14
- messages
 - unsolicited (PKD), LIC type 6 4-90
- microcode
 - differences between HSS and LSS 5-8
 - exchange between CLDP-HSS 5-9
 - exchange between NCP-HSS 5-9
 - functions (HSS) 5-14, 5-16
 - of the FESH 5-9
 - service aid (HSS) 5-37
- microcode EC level
 - LIC type 5 (DCE function) 4-71
- MIOC interconnection (CCU) 2-11
- MIOC parity error (CCU) 2-42
- MMIO operation (TRA) 6-17
- modem and data management (HSS) 5-10
- modem interface management (FESH) 5-19
- modem retrain (FESH) 5-21
- modem-in 4-32
 - layer (HSS CSP) 5-12
 - lead state confirmation
 - on V.35 (FESH) 5-19
 - on X.21 (FESH) 5-20
 - management (FESH) 5-19
- modem-out 4-33
 - layer (HSS CSP) 5-12
 - management (FESH) 5-21
- modes of operation
 - CA 7-7
- modifier 3-7
- modulation
 - LIC type 6 4-82
- MOSS 1-13
 - address exception error 2-45
 - changes of state 8-7
 - data operand register (MDOR) parity error (CCU) 2-42
 - error status register (TRA) 6-24
 - functions 8-6
 - interconnection type errors 2-45
 - OP error 2-45
 - packaging 8-3
 - processor 8-3
 - reset 8-4
 - screen address display CA 3-31
 - screen address display LA 3-33
 - states 8-7
 - to and from CCU 2-39
- MOSS BER 11-9
 - See *also* BER type 01
- MOSS BER formats 11-99
- MOSS board DC voltages and tolerances 10-9
- MOSS check 11-31
- MOSS check codes 11-41
- MOSS ID 06 formats 11-34
- MOSS-to-CCU communication 8-12
- MOSS/disk/diskette drive interaction 8-17
- MOSS/operator console connections 8-18
- MSAU (TRSS) 6-5
- multi-floor wiring example 6-8
- multipoint
 - LIC type 5 to LICs type 5 connection 4-59
 - LIC type 5 to one tailed 586X 4-60
 - LIC type 5 to 586Xs connection 4-59
 - LIC type 5 (DCE function) 4-69
 - LIC type 6 4-86
- multistation access unit, (TRSS) 6-5

MUX (multiplexer card)
 data flow 4-36
 definition 4-7
M.1020 line characteristics 4-66
M.1025 line characteristics 4-66

N

native mode
 LIC type 5 (DCE function) 4-62, 4-63
NCP 1-19, 1-20
 buffer handling logic checker 5-28
 buffer prefix validity checking in receive (HSS) 5-37
 commands (HSS) 5-6
 to HSS microcode exchange 5-9
NCP definition facility
 See NDF
NCP/PEP BER
 See BER type 12
NCP/PEP BER formats 11-140
NDF 1-20
NEF 1-20
NetView*
 facilities 1-18
 Performance Monitor (NPM) 1-18
network
 management 1-18
Network Control Program 1-19
Network Extension Facility, IBM
 See NEF
Network Routing Facility
 See NRF
network services
 LIC type 6 4-86
Network Terminal Option
 See NTO
no response
 on PKD 4-76
nodes (TRSS) 6-7
non X.21 lines
 modem-in process 4-48
Non-SNA Interconnection, IBM
 See NSI
normal tagged status 7-17
not executed
 PKD command 4-76
NPSI 1-19
NRF 1-19
NSC mode 7-7
NSI 1-20
NTO 1-19
numbering (CA) 7-4

O

on site service 1-22
operating systems 1-17

operation register (CCU) 2-38
operator address register (CCU) 2-39
operator consoles 1-15
 alternate console 9-6
 console sharing via IBM 7427 9-7
 highlights 9-6
 local console 9-6
 remote console 9-6
 remote support facility 9-7
operator function select value register (CCU) 2-39
OPT DDS LOOP 4-91
options
 LIC type 5 (DCE function) 4-67
 LIC type 6 4-85
opto-coupler device output 10-26
out mailbox 8-12
out (R/W) 3-7
output instructions
 CCU 2-23
 details (CCU) 2-25

P

packaging
 CA 7-3
 MOSS 8-3
Packet Switching Interface, NCP
 See NPSI
panel
 LIC type 5 4-65
 LIC type 6 4-84
parity valid 3-7
path POR
PEP 1-19
performance test points 2-46
personalization
 LIC type 4 4-48
physical address wiring 3-29
physical interconnection
 DMA bus 3-9
 IOC bus 3-8
pin assignment (bus terminator) 3-55
ping/pong buffers 4-17
 clocks 4-17
PIO
 operation sequence 3-14
 data transfer 3-16
 initialization 3-15
 read (halfword adapter) 3-17
 write (halfword adapter) 3-17
PKD (portable keypad display)
 analog test 4-77
 background information 4-75
 background information (LIC type 6) 4-88
 bad response 4-76
 busy TC on 4-76
 buzzer control 4-78
 command not executed 4-76
 command rejection 4-76

- PKD (portable keypad display) *(continued)*
 - commands in CE mode 4-78
 - contact sense/operate 4-78
 - DCE information 4-75
 - description 4-74
 - digital test 4-77
 - keying procedures 4-76
 - lamp test 4-75
 - LIC type 5 configuration 4-73, 4-78
 - local loop 4-77
 - manual tests LIC type 5 (DCE function) 4-72
 - no response 4-76
 - POR bring-up information 4-76
 - self-tests 4-77
 - speed change 4-77
 - status display 4-77
 - unsolicited messages 4-79
- plugging limitations
 - LIC type 6 4-10
- plugging rules for LAs or CAs 3-44
- point-to-point
 - LIC type 5 to LIC type 5 4-58
 - LIC type 5 to tailed 586X 4-59
 - LIC type 5 to 586X or 786X 4-58
 - LIC type 5 (DCE function) 4-69
 - LIC type 6 4-86
- POP parity error (CCU) 2-42
- POR
 - CCU subsystem 2-12
 - MOSS 8-4
 - path 10-29
 - pin location 10-29
 - principle 10-28
 - storage control (CCU) 2-12
- POR - bring-up
 - information (on PKD) 4-76
 - information, LIC type 6 4-89
- POR (power ON reset)
 - CSP 4-20
 - FES 4-25
- portable keypad display
 - See PKD (portable keypad display)
- power reset function 10-24
- power BER
 - See BER type 04
- power BER formats 11-114
- power control subsystem 10-14
 - data flow 10-15
 - introduction 10-14
- power input limitation
 - adjustment 10-4
 - limits 10-4
- power mode of operation 10-19
 - host mode 10-19
 - local mode 10-19
 - network mode 10-19
 - switching from one mode to another. 10-20

- power OFF sequence. 10-22
- power ON
 - reset (TRA) 6-19
- power ON reset 4-20
- power ON retry
 - function 10-23
 - sequence 10-23
- power ON sequence 10-21
- power ON/OFF 1-16
- power stacked faults 10-27
 - faults logging 10-27
- power status monitoring 10-24
- power subsystem
 - introduction 10-3
- presentation of status 7-18
- preventive maintenance 1-23
- primary power box
 - component location 10-5
 - distribution 10-6
- problem determination
 - aid for LIC types 1 to 4 4-92
 - aid for LIC types 5/6 4-95
 - aid on HSS 5-37
 - aid on TRA 6-28
 - CCITT loop 3 4-87
 - commands, LIC type 5 (DCE function) 4-71
 - commands, LIC type 6 4-87
 - programming support (HSS) 5-37
 - self-test 4-87
- problem isolation and network management (HSS) 5-38
- processor unit (CCU) 2-3
- program display register 1 (CCU) 2-39
- program display register 2 (CCU) 2-39
- program errors (CCU) 2-43
- program levels
 - level 1 (CCU) 2-4
 - level 2 (CCU) 2-4
 - level 3 (CCU) 2-5
 - level 4 (CCU) 2-5
 - level 5 (CCU) 2-5
 - masking priorities (CCU) 2-5
 - priorities (CCU) 2-4
- programmed reset
 - FES 4-25
 - TRA 6-19
- programming support
 - coexistence/migration 1-20
 - for problem determination (HSS) 5-37
 - in controller 1-17
 - in network 1-18
- program/hardware errors (HSS) 5-23
- protocol
 - LIC types 1 to 4 4-9
 - LIC types 5/6 4-10
 - of the token-ring access 6-6
- protocol of IOC buses 3-3

- PS1
 - component locations 10-8
 - connection layout 10-7
 - DC voltage test points 10-8
 - DC voltages and tolerances 10-9
- PS2
 - connection layout 10-12
 - DC voltages and tolerances 10-12
- PT2/3
 - connection to LIC type 5 4-79
 - LIC type 6 4-91
- PUC 2-3
 - oscillator interconnection (CCU) 2-11

R

- RAM A 4-23
- RAM B 4-23
- RAM C 4-23
- RAM organization
 - FESA 4-28
- read PIO example 3-3
- ready state (CA) 7-8
- read/write operations 8-18
- receive
 - command FESH 5-16
 - continue command (FESH) 5-17
 - end of receive (FESH) 5-17
 - flow (FESH) 5-17
 - layers (HSS CSP) 5-12
 - level threshold for LIC type 5 (DCE function) 4-70
 - operation for I-frame (FESH) 5-17
 - operation HSS 5-16
 - operation (TRA) 6-13
- reception of data (HSS) 5-10
- reference code 11-10, 11-19, 11-22
- reference code generation 11-17
- register
 - A (CCU) 2-19
 - adapter check (TIC) 6-25
 - CCU 2-20
 - D (CCU) 2-19
 - data value register (CCU) 2-39
 - external (CCU) 2-20
 - general (CCU) 2-20
 - hardware registers (CCU) 2-38
 - instruction address (CCU) 2-20, 2-38
 - lagging address register (CCU) 2-38
 - maintenance temporary address register (MTAR) (CCU) 2-39
 - maintenance temporary data register (MTDR) (CCU) 2-39
 - operation (CCU) 2-38
 - operator address (CCU) 2-39
 - operator function select value register (CCU) 2-39
 - program display register 1 (CCU) 2-39
 - program display register 2 (CCU) 2-39
 - storage address (CCU) 2-39

- registers (CA) 7-9
- REM DSU/CSU FAILED 4-90
- REM MODEM FAILED 4-79
- REM PWR LOSS 4-79, 4-90
- remote
 - self-test 4-97
 - status 4-98
- remote console 9-6
- remote service 1-21
- Remote Support Facilities (RSF) 8-18
- remote support facility 1-15, 9-7
- removing CA from CS chain 7-13
- reporting DMA errors 5-26
- reset 3-8
 - AIO (CCU) 2-20
 - CSP 4-19
 - DMUX 4-37
 - FESH 5-14
 - FESL 4-24
 - LIC 4-38, 4-42
 - LIC types 1 to 4 4-44
 - LIC types 5/6 (DTE function) 4-55
 - power ON and tag reset (TRA) 6-19
 - programmed reset PIO 4-19
 - programmed (TRA) 6-19
 - SMUX 4-42
 - TIC 6-19
- reset and set the bypass CCU check stop mode 2-40
- resetting interrupt requests (CCU) 2-6
- RESP field in power BER 11-113
- RESP/REQ in power BER 11-112
- RFS 4-32
 - delay, LIC type 5 (DCE function) 4-64
 - delay, LIC type 6 4-83
 - transmit clock gating 4-48
- RI 4-32
- ring
 - access protocol (TRSS) 6-6
- RLSD 4-32
- ROS (read-only storage)
 - CSP 4-14
- RSF 1-15, 9-7
- RTAM 1-17
- RTS
 - LIC types 1 to 4 4-48
- rules of configuration BPC1/BPC2 cards 3-28

S

- safety,
 - general iv
 - inspection procedure iv
 - notices iv
- SAR parity error (CCU) 2-42
- scanner errors with no BER 11-25
- scanner interrupt 3-8
- scanner states
 - connected 4-18
 - disconnected 4-18

- scanner states (*continued*)
 - disconnected-stop 4-19
 - initialized 4-18
 - inoperative 4-18
 - running 4-19
 - stopped 4-19
- scanner status after IML (HSS) 5-13
- SCF bit definition 5-31
- scheduled power ON function 10-22
- scoping routine for IOC bus 3-49
- SCTL 2-13
 - function partitioning 2-14
- SCTL card detected errors reported by FESH 5-26
- SCTL-to-CCU cache interconnection 2-15
- SCTL-to-DMA bus line function 3-10
 - byte select 3-11
 - data bus 3-11
 - errors 3-11
 - FESH clock 3-11
 - grant 3-11
 - ready 3-11
 - read/write 3-11
 - request 3-11
 - SCTL clock 3-11
 - turnaround 3-11
 - valid 3-11
- secondary status field (SES) bit definition 5-31
- selective reset on CA 7-19
- selective scanning
 - configuration 4-46
 - LIC types 1 to 4 4-45
 - LIC types 5/6 (DTE function) 4-55
- SELF TEST FAILED 4-79, 4-91
- SELF TEST OK 4-79, 4-91
- self-test
 - LIC type 5 (DCE function) 4-72
 - LIC type 6 4-87
 - local (LIC type 5) 4-96
 - local (LIC type 6) 4-97
 - PKD 4-77
 - remote 4-97
- sensitivity
 - carrier detector (LIC type 5) 4-70
- serial link 4-12
 - connection to LICs 5/6 4-34
 - FESA interconnection 4-27
 - frames 4-34
- service aid
 - HSS microcode 5-37
- service personnel definitions xi
- SES bit definition 5-31
- set and reset the bypass CCU check stop mode 2-40
- set and reset the level 1 adapter mask (CCU) 2-40
- setting interrupt requests (CCU) 2-6
- setup of the console 9-8
- short hold mode/multiple port sharing 1-19
- signals used by CA 7-10
- single multiplexer card
 - See SMUX (single multiplexer card)
- slot
 - control slots 4-35
 - data slots 4-35
 - in serial link 4-34
- SMUX (single multiplexer card)
 - card replacement 4-40
 - data flow 4-41
 - definition 4-8
 - functional description 4-42
 - functions 4-39
 - reset 4-42
 - transmit level 4-40
- SNA Interconnection (XI), X.25 1-19
- soft stop transmit command (HSS) 5-16
- specific mechanism 11-13
- speed
 - change from PKD 4-77
 - change, LIC type 6 4-89
 - control, LIC type 6 4-87
 - LIC type 5 (DCE function) 4-57
 - LIC type 6 4-81
 - setting, LIC type 5 (DCE function) 4-58
 - setting, LIC type 6 4-81
- SP/AE
 - address exception key (CCU) 2-18
 - address exception (CCU) 2-18
 - instructions (CCU) 2-18
 - key locations (CCU) 2-18
 - keys (CCU) 2-18
 - read only key (CCU) 2-18
 - storage protection key (CCU) 2-18
 - storage protection (CCU) 2-18
 - user key (CCU) 2-18
- SSP 1-17
- state
 - CA 7-8
- state confirmation
 - on CTS lead (FESH) 5-20
 - on X.21 modem-in lead (FESH) 5-20
- status
 - display on PKD 4-77
 - local 4-98
 - remote 4-98
- status control field (SCF) bit definition 5-31
- status fields SCF, SES, LCS 5-31
- status of the HSS scanner after IML 5-13
- status transfer state (CA) 7-9
- stop 2-20
 - AIO (CCU) 2-20
 - receive command (FESH) 5-18
- storage
 - address exception (CCU) 2-18
 - address register (CCU) 2-39
 - basic card (CCU) 2-3
 - CACHE (CCU) 2-16
 - CCU 2-12

- storage (*continued*)
 - control card (SCTL) (CCU) 2-3
 - control interconnection (CCU) 2-11
 - control mode (CCU) 2-15
 - control (CCU) 2-13
 - environment (CCU) 2-13
 - instructions (CCU) 2-18
 - line invalidation (CCU) 2-17
 - protect (CCU) 2-18
 - protection state (CCU) 2-17
 - protection (CCU) 2-17
 - read policy (CCU) 2-17
 - word (CCU) 2-12
 - write policy (CCU) 2-17
- storage protect
 - and address exception instructions (CCU) 2-18
 - instruction fetch error (CCU) 2-43
 - program execution error (CCU) 2-43
- summary of the IOC bus interface signal lines 6-16
- surge protection
 - LIC type 5 4-64
 - LIC type 6 4-83
- swap
 - LIC types 1 to 4 4-46
 - LIC types 5/6 (DTE function) 4-55
- switches setting
 - SMUX 4-40
- system components (TRSS) 6-7
- system environment (HSS) 5-4
- system reset on CA 7-18
- system support programs 1-17

T

- tag reset (TRA) 6-19
- tag sequence (DMA) 5-25
- tagged DE status 7-17
- tail gate for consoles 9-7
- test
 - analog line analysis 4-99
 - digital (xmit/rcve) LIC type 5 4-99
 - digital (xmit/rcve) LIC type 6 4-99
 - manual from PKD (LIC types 5/6) 4-95
 - manual, LIC type 6 4-91
 - PKD 4-77
- TEST FAILED 4-79, 4-91
- TEST FROM HOST 4-79, 4-90
- TEST OK 4-79, 4-91
- TEST OK NOWRP 4-79, 4-91
- TEST OK WRAP 4-79, 4-91
- test points for performance 2-46
- thresholds 11-5
- TI 4-33
- TIC 6-7
- TIC (token-ring interface coupler)
 - adapter check register 6-25
 - bus interconnection 6-16
 - bus interconnection control 6-13
 - bus signal lines summary 6-17

- TIC (token-ring interface coupler) (*continued*)
 - card 6-11
 - data flow 6-11
 - reset 6-19
- time out
 - DMA 5-25
 - values used by the HSS 5-22
- timers (CCU) 2-18
- timing
 - LIC type 6 4-86
- token-ring
 - access control protocol 6-6
 - adapter addressing 3-42
 - adapter (TRA) 6-4, 6-9
 - address 3-43
 - bridges 6-7
 - cabling system 6-4
 - frame format 6-6
 - interconnection function, (NCP) 1-19
 - interface coupler (TIC) card 6-7, 6-11
 - line addressing 3-43
 - multiplexor (TRM) card 6-15
 - network 6-3
 - wrap tests (TRA) 6-28
- token-ring subsystem 1-12
- token-ring subsystem (TRSS) 6-1
- tone
 - alarm tone detection (LIC type 5, DCE function) 4-73
 - characteristics (LIC type 5, DCE function) 4-73
 - characteristics, LIC type 6 4-88
 - reception, LIC type 6 4-88
- tone detection
 - alarm, LIC type 6 4-87
- tools and test equipment 1-23
- TPF 1-20
- TPS
 - alternate path 7-16
 - contingent allegiance 7-17
 - implicit allegiance 7-17
 - instantaneous allegiance 7-17
 - long-term allegiance 7-17
 - neutral 7-17
 - states of allegiance 7-17
 - switched 7-17
- TPS/TCS mode 7-16
- TRA (token-ring adapter)
 - functions 6-4
 - in the 3745 6-9
 - IOC bus interconnection 6-15
 - receive operation 6-13
 - resets 6-19
 - transmit operation 6-14
- Transaction Processing Facility, IBM
 - See TPF
- transfer mode
 - LIC types 1 to 4 4-9
 - LIC types 5/6 4-10

- transit time
 - LIC type 5 (DCE function) 4-64
 - LIC type 6 4-83
- transmission of data (HSS) 5-10
- transmission speed
 - LIC types 1 to 4 4-9
 - LIC types 5/6 4-10
- transmission subsystem 1-8
 - See also TSS (transmission subsystem)
- transmit
 - command (HSS) 5-15
 - initial command (HSS) 5-14
 - operation
 - TRA 6-14
 - operation (HSS) 5-14
- transmit clock control
 - LIC type 5 (DCE function) 4-70
- transmit level
 - LIC type 5 (DCE function) 4-70
 - SMUX 4-40
 - switches setting 4-40
- transmit/receive
 - LIC types 1 to 4 4-44
- TRM (token-ring multiplexor)
 - arbitration mechanism 6-18
 - card 6-15
 - error detected by TRM (format 1) 6-22
 - error status
 - register (level 1) 6-20
 - register (level 2) 6-22
- TRSS 1-12
 - cabling system 6-4
 - cpckaging (TRSS) 6-9
 - in 3745 data flow 6-2
 - major system components 6-7
 - nodes 6-7
 - ring 6-4
 - ring access protocol 6-6
- TRSS BER
 - See BER type 15
- TRSS BER formats 11-153
- TSS 1-8
 - interface cables 4-100
- TSS commands
 - CCITT loop 3 4-72
 - LIC type 5 (DCE function) 4-72
 - LIC type 6 4-87
 - self-test 4-72
- TSS line addressing 3-37
- TSS (transmission subsystem)
 - definition 4-5
- TSS/HPTSS BER
 - See BER type 11
- TSS/HPTSS BER formats 11-136
- two-processor switch (TPS) 7-16

U

- UCW 7-7
- unit control word (UCW) 7-7
- unresolved error on:
 - IOC bus 11-29
 - scanner adapter 11-27
 - scanner AIO 11-27
- unresolved interrupts on:
 - CA adapter error 11-26
 - CA data/status 11-26
 - CCU level 1 11-27
 - CCU level 3 11-28
 - CCU level 4 router 11-28
 - level 1 CA 11-26
 - level 2, scanner 11-27
 - level 3 11-26, 11-27
 - PCI 11-29
 - scanner level 2 11-27
- untagged asynchronous status 7-18

V

- valid byte 3-7
- valid halfword 3-7
- VTAM* 1-17
- V.24
 - loop 1 (LIC types 1 to 4) 4-51
 - loop 3 (LIC types 1 to 4) 4-52
 - loop 3, LIC types 5/6 (DTE function) 4-56
- V.25
 - loop 1 (LIC types 1 to 4) 4-52
- V.35
 - and X.21 example of cables connected (HSS) 5-41
 - and X.21 wrap or loop tests (HSS) 5-39
 - example of two cables connected (HSS) 5-41
 - modem-in lead state confirmation (FESH) 5-19

W

- wrap
 - external facility (HSS) 5-38
 - LIC types 1 to 4 4-51
 - LIC types 5/6 (DTE function) 4-55
 - mode at DCE level (HSS) 5-38
 - or loop tests (HSS) 5-39
 - token-ring wrap tests (TRA) 6-28
- wrap plugs 7-22
- wrap tests
 - controlled from host 4-93, 4-95
 - LIC types 1 to 4 4-93
 - LIC types 5/6 4-95
 - controlled from MOSS 4-94, 4-95
 - LIC types 1 to 4 4-94
 - LIC types 5/6 4-95
- WRONG SLOT 4-79, 4-90

X

- X'13' register
 - FESA line interface address 4-29
- X'15' register
 - FESA asynchronous operation command 4-29
- xmit/rcve
 - digital test, LIC type 5 4-99
 - digital test, LIC type 6 4-99
- X 21
 - clear 4-33
 - example of two cables connected (HSS) 5-41
 - interface (HSS) 5-41
 - loop 1 (LIC types 1 to 4) 4-52
 - loop 3 (LIC types 1 to 4) 4-52
 - modem-in lead state confirmation (FESH) 5-20
- X.21 lines
 - ICF data flow 4-50
 - modem-in process 4-48
- X.21 SH/MPS 1-19
- X.25 SNA Interconnection (XI) 1-19

Z

- Z register parity error (CCU) 2-42

Numerics

- 100 ms interval timer (CCU) 2-18
- 2701 1-19
- 2702 1-19
- 2703 1-19
- 3002 channel (US) characteristics 4-66
- 3161 console 3727 console key conversion 9-8
- 3727 console 3161 console key conversion 9-8
 - maintenance 9-8
 - setup 9-8
- 3745
 - capacity 1-5
 - data flow 1-4
 - identification 1-5
 - model 130 1-5
 - model 150 1-5
 - model 170 1-5
 - power ON/OFF 1-16
- 3745 down 11-25
- 3745 mode (clocking) 4-51

IBM 3745 Communication Controller
Models 130, 150, and 170
Hardware Maintenance Reference (HMR)
Order No. SY33-2066-2

**READER'S
COMMENT
FORM**

Please write your comments concerning this manual in the space reserved below. We will greatly appreciate them and will consider them for later releases of the present manual.

In advance, thank you.

Note: Staples can cause problems with automated mail sorting equipment.
Please use pressure sensitive or other gummed tape to seal this form.

Reader's Comment Form

Fold and tape

Please Do Not Staple

Fold and tape

Stamp

IBM France
Centre d'Etudes et Recherches
Service 0762 - BP 79
06610 - La Gaude
France

Fold and tape

Please Do Not Staple

Fold and tape

If you would like a reply, please print:

Your Name _____

Company Name _____ *Department* _____

Address _____

IBM Branch Office serving you _____

IBM

D

D

D

D

D



Part Number
03F5010

Printed in U.S.A.

SY33-2066-2

