7095 DATA PROCESSING SYSTEM
FUNCTIONAL OBJECTIVES

1. DESCRIPTION

1.1 The 7095 is a new Data Processing System which extends the 7090/7094/7094-II line by means of new technology and new systems organization.

1.2 The system will operate in either the 7094-Compatible Mode or the 7095 Mode.

1.2.1 In the Compatible Mode all instructions which do not refer to input-output will be executed as in the 7094 or 7094-II. Those instructions which refer to input-output will cause a trap to a fixed location where they will be simulated in 7095 Mode.

1.2.2 In the 7095 Mode the system utilizes a new instruction format and a modified instruction set.

1.3 The 7095 allows for the attachment of NPL input/output devices by means of NPL control units. The 7095 Data Channel will be designed to meet the NPL Interface of these control units.

1.4 Bulk Storage (LCM) will be attached to the system by means of a parallel transmit channel which will control the transfer of data between high speed storage and bulk storage.

1.5 A modified 7095 Data Channel designed to meet a parallel interface enables attachment of some non-NPL Interface devices to the 7095.

1. DESCRIPTION (Continued)

1.6 Storage Protection and a Real Time Clock System will be standard equipment on the 7095.

1.7 The system will also be able to operate in a Problem Program Mode. When operating in this mode the program is prevented from executing certain instructions such as those affecting storage protection and all input-output instructions. If the system is not in the Problem Program Mode it is said to be in the Monitor Mode.

2. GENERAL CHARACTERISTICS

2.1 The system will normally operate in the 7095 Mode. In its reset status it will be in the 7095 Mode (not in Compatible Mode) and in the Monitor Mode (not in Problem Program Mode). All traps will return the system to the 7095 and Monitor Mode.

2.2 When in the 7095 Mode, all instructions will have the following format:

S - 8	9	10-13	14-17	18-35
Operation	Flag	Tag 1	Tag 2	Address Field
O	F	T1	T2	Y

2.2.1 Tag 1 specifies the index register in those operations involving an index register. In other operations Tag 1 specifies an index register by which the address is modified.

2. GENERAL CHARACTERISTICS (Continued)

2.2.2 Tag 2 always specifies an index register by which the address is modified.

2.2.3 The flag field (F) specifies indirect addressing.

2.2.4 There will be 15 index registers of 18 bits each.

2.2.5 The 18 bit address field allows for directly addressing 262,144 words of core storage.

2.2.6 Those 7094 instructions which contain a decrement field have been replaced by equivalent instructions in the new format. (See Table 1, Section 3.4)

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR

3.1 Addressing

3.1.1 The program counter, index registers, the index adder and all address paths are 18 bits and address arithmetic is performed modulo 262,144.

3.1.2 Indexing is subtractive. For those instructions which allow double indexing the effective address is obtained by subtracting the contents of the index registers specified by Tag 1 and Tag 2 from Y, the address field of the instruction. In those instructions which allow only single indexing, the effective address is obtained by subtracting the contents of the index register specified by Tag 2 from Y.

CHANGES TO 7095 DATA PROCESSING SYSTEM
FUNCTIONAL OBJECTIVES
REVISION #1 dated 3/17/64

1. Section 3.1.3 should read as follows:

"Indirect Addressing is possible on all instructions. Specifying indirect addressing does not change the function of the Tag fields in the instruction as defined in Section 3.1.2. The word containing the direct address is fetched from the location specified by the effective address of the instruction; $[Y - (T_1) - (T_2)]$ for those instructions which allow double indexing and $[Y - (T_2)]$ for those instructions which do not allow double indexing. The format of the word fetched by the indirect address is as follows:

S, 1-8 Not Used	9 Flag F^1	10-13 Tag 2 $T2^1$	14-17 Tag 2 $T2^1$	18-35 Address Field Y^1

When F^1 is zero this word contains the direct address. When F^1 is one this word contains another indirect address. In both cases, independent of the instruction being executed, the effective address is obtained by subtracting the index registers specified by $T1^1$ and $T2^1$ from Y^1. Any number of levels of indirect addressing is possible. After the last level the use of the effective address depends on the instruction being executed and may represent the location of a data fetch or an immediate quantity. Using indirect addressing on a Load Index from Address instruction may be used to compute the effective address of an instruction and load it into an index register."

is one, this word contains another indirect address which is computed in the same manner as a direct address. Any number of levels of indirect addressing is possible.

3.2 Storage Protection

3.2.1 Storage Protection is provided by means of a ten bit High Protect Register and a ten bit Low Protect Register.

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR (Continued)

3.2.1 (Continued)

Whenever an attempt is made to store a word in the high speed memory a comparison is made between the ten high order bits of the address and the High and Low Protect Registers. If these ten bits of the address are greater than the High Protect Register or less than the Low Protect Register then there is a potential storage protect violation. A potential storage protect violation becomes an actual storage protect violation if either of the two following conditions is met:

a) The request for the store cycle came from the CPU and the CPU is in the Problem Program Mode.

b) The request for the store cycle came from a Data Channel and storage protect is not inhibited by the channel.

3.2.3 The channel will inhibit storage protection throughout any operation resulting from an I/O instruction which was given in the Monitor Mode unless the instruction specified that it was to be protected.

3.2.4 A CPU storage protect violation is never possible when the system is in the Monitor Mode.

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR (Continued)

3.3 Problem Program Mode

3.3.1 When operating in the Monitor Mode any instruction may be executed by the CPU. When operating in the Problem Program Mode there are certain instructions which are illegal. An attempt to execute one of these instructions causes a trap to a fixed location. The restricted instructions are as follows:

a) Set Storage Protection

b) Inhibit Channel Traps

c) Set Channel Assignment Register

d) Start Channel

e) Channel Test

f) Store Channel

g) Halt Channel

h) Restore Channel Trap

i) Set CPU Status instruction

3.3.2 The Channel Assignment Register is comprised of one bit per channel including the transmit channel for bulk storage. If a particular bit position contains a zero, then no I/O instructions may be executed for that channel when the system is in the Problem Program Mode. If a particular bit position contains a one, then instructions d, e, f, g and h (in Section 3.3.1) may be executed for

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR (Continued)

3.3.2 (Continued)

that channel when the system is in the Problem Program Mode. Use of this register allows the Monitor to assign "Private Channels" to the Problem Program Mode.

3.3.3 Storage Protection is always in effect for I/O instructions issued in the Problem Program Mode.

3.4 Data Channel Traps (also see 7095 Data Channel Functional Objectives)

3.4.1 All data channel traps store the CPU location counters and the CPU mode status in a fixed location, place the system in the 7095, Monitor and No Transfer Trap Mode and transfer control to one of twenty-four fixed locations.

3.4.2 Further I/O traps are prevented until a Return from Channel Trap instruction is executed.

3.4.3 The Return from Channel Trap instruction restores the system to its status prior to the trap by setting the mode under control of the bits (positions S, 1-17) in the CPU status location (see Section 3.4.1) and returning control to the location specified in positions 18-35 of this status word. The Return from Channel Trap instruction also allows other traps to occur by returning control to that set by the last Inhibit Channel Trap instruction.

2. In Section 3.4.3 the following sentence should be added at the end of the section:

"After restoring the system this instruction also places zero in the contents of the CPU Status word."

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR (Continued)

3.5 CPU Traps

3.5.1 CPU traps are caused by any of the following conditions:

a) Floating Point Trap or Divide Check Trap.

b) CPU Storage Protect Violation or Illegal Operation in Problem Program Mode.

c) Attempt to execute an I/O instruction in the 7094 Compatible Mode.

d) Transfer Trap (Successful transfer while in Transfer Trap Mode).

e) Monitor Call Instruction.

3.5.2 All CPU traps store the mode status and the program location counter in one of two fixed locations, place the system in 7095, Monitor and No Transfer Trap Modes, store any status information required to further define the trap in one of the three fixed locations and then transfer control to one of five fixed locations. (See Table I)

3.5.3 The Set CPU Status instruction places the system in the mode specified in S, 1-17 of the word fetched from location Y. By making Y the address of one of the mode status words described in Section 3.5.2 this instruction can be used to return from a CPU trap. With other values of Y the instruction can be used as an enter or leave mode instruction.

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR (Continued)

3.6 New 7095 Instructions

3.6.1 Add to Exponent

Positions 27-35 of Y are added to positions P, 1-8 of C(AC). If a floating point overflow or underflow occurs, the operation is subject to floating point trap. Positions 27-35 are considered as a two's complement number for subtraction.

3.6.2 Load Left Half Word into Accumulator

Positions S, 1-17 of C(Y) replace positions 18-35 of C(AC). Positions P, Q, S and 1-17 of AC are set to zero. C(Y) are unchanged.

3.6.3 Load Right Half Word into Accumulator

Positions 18-35 of C(Y) replace positions 18-35 of C(AC). Positions P, Q, S and 1-17 of AC are set to zero. C(Y) are unchanged.

3.6.4 Store Accumulator into Left Half Word

Positions 18-35 of C(AC) replace positions S, 1-17 of C(Y). Positions 18-35 of C(Y) and the C(AC) are unchanged.

3.6.5 Store Accumulator into Right Half Word

Positions 18-35 of C(AC) replace positions 18-35 of C(Y). Positions S, 1-17 of C(Y) and the C(AC) are unchanged.

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR (Continued)

3.6.6 Double Logical Load

The C(Y) replaces P, 1-35 of C(AC) and C (Y+1) replaces C(MQ). Positions Q and S are set to zero. C(Y) and C(Y+1) are unchanged.

3.6.7 Double Logical Store

Positions P, 1-35 of C(AC) replace the C(Y) and the C(MQ) replace the C(Y+1). The AC and MQ are unchanged.

3.6.8 Store Magnitude

Positions 1-35 of C(AC) replace positions 1-35 of C(Y). The sign of C(Y) is set plus.

3.6.9 Store Negative

Positions 1-35 of C(AC) replace positions 1-35 of C(Y). The sign of C(Y) is set to the inverse of the sign of the accumulator.

3.6.10 Load Accumulator Under Control of the Mask

Each bit of C(Y) is matched with the corresponding bit of C(SI) and the result is set into positions P, 1-35 of the accumulator. A resulting bit is a one only if both the SI and the AC contained a one bit in the same position. The C(SI) and the C(Y) are unchanged.

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR (Continued)

3.6.11 Store Accumulator Under Control of the Mask

Positions P, 1-35 of AC are matched with the corresponding bits of C(SI) and the result is stored into C(Y). A resulting bit is a one only if both the SI and the AC contained a one bit in the same position. The C(SI) and the C(AC) are unchanged.

3.6.12 Insert Accumulator Into Storage Under Control of Mask

Positions P, 1-35 of AC are matched with the corresponding bits of the C(SI). If a position of C(SI) contains a one, the corresponding bit of the C(AC) is stored into the corresponding bit of the C(Y). All other positions of C(Y) are unchanged. The C(SI) and C(AC) are unchanged.

3.6.13 Transfer on Zero or Minus (TZM)

If the sign position of the AC is minus or if the C(AC) is zero, the next instruction is taken from location Y. Otherwise, the next sequential instruction follows.

3.6.14 Transfer on Zero or Plus (TZP)

If the sign position of the AC is plus or if the C(AC) is zero, the next instruction is taken from Y. Otherwise, the next sequential instruction follows.

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR (Continued)

3.6.15 Compare Accumulator with Storage Under Control of the Mask

The C(AC) positions P and 1-35 are compared with C(Y). The only positions to be considered in the comparison are those for which the corresponding position of the C(SI) is a one bit. The comparison is always logical. If the factors compared are equal the next instruction is skipped and the program proceeds from there. If the factor from the C(AC) is less than the factor from the C(Y) the next two instructions are skipped and the program proceeds from there. If the factor from the C(AC) is greater than the factor from the C(Y) the program takes the next sequential instruction.

3.6.16 Load Index from Left Half Storage Word

Positions S and 1-17 of C(Y) replace the C(XR) specified by T1. The C(Y) are unchanged.

3.6.17 Store Index into Left Half Storage Word

The C(XR) specified by T1 replace positions S and 1-17 of C(Y). The C(XR) and positions 18-35 of C(Y) are unchanged.

3.6.18 Add to Index Direct (ADXD)

The C(XR) specified by T1 are replaced by C(XR) plus positions 18-35 of C(Y). The arithmetic is performed modulo 262,144 and no indication is given when an overflow

10. The following condition applies to Section 3.6.18, 3.6.19, 3.6.20 and 3.6.21.

When performing an Add or Subtract from Index one of the three Index Compare Indicators is always set based on a comparison with zero. If the result of the operation is zero, the Equal Indicator is set. If an add operation causes the result to pass thru zero, the High Indicator is set. If a subtract operation causes the result to pass thru zero, the Low Indicator is set.

11. The following instructions should be deleted:

3.6.22 Skip on No Index Direct
3.6.23 Skip on No Index Immediate
3.6.24 Skip on Index Direct
3.6.25 Skip on Index Immediate
3.6.26 Skip on Index Low or Equal Direct
3.6.27 Skip on Index Low or Equal Immediate
3.6.28 Skip on Index High Direct
3.6.29 Skip on Index High Immediate
3.6.30 Skip on Index Equal Direct
3.6.31 Skip on Index Equal Immediate

Note: These deletions are also reflected in TABLE II on page 28 of the Functional Objectives.

Y. The arithmetic is performed modulo 262,144 and no indication is given when an overflow occurs. With T1 equal to zero, no operation results.

3.6.22 Skip on No Index Direct (SNXD)

If the C(XR) specified by T1 are greater than positions 18-35 of C(Y), the number in the index register is reduced by positions 18-35 of C(Y) and the next sequential instruction is taken. If the C(XR) specified by T1 are

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR (Continued)

3.6.22 (Continued)

less than or equal to positions 18-35 of C(Y), the contents of the index register are unchanged and the computer skips the next sequential instruction. With T1 equal to zero, the skip occurs.

3.6.23 Skip on No Index Immediate (SNXI)

If the C(XR) specified by T1 are greater than Y, the number in the index register is reduced by Y and the next sequential instruction is taken. If the C(XR) specified by T1 are less than or equal to Y, the contents of the index register are unchanged and the computer skips the next sequential instruction. With T1 equal to zero, the skip occurs.

3.6.24 Skip on Index Direct (SIXD)

If the C(XR) specified by T1 are equal to or less than positions 18-35 of the C(Y), the C(XR) are unchanged and the computer takes the next sequential instruction. If C(XR) specified by T1 are greater than positions 18-35 of C(Y), the C(XR) are reduced by positions 18-35 of C(Y) and the computer skips the next sequential instruction. With T1 equal to zero, no skip occurs.

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR (Continued)

3.6.25 Skip on Index Immediate (SIXI)

If the C(XR) specified by T1 are equal to or less than Y, the C(XR) are unchanged and the computer takes the next sequential instruction. If C(XR) specified by T1 are greater than Y, the C(XR) are reduced by Y and the computer skips the next sequential instruction. With T1 equal to zero, no skip occurs.

3.6.26 Skip on Index Low or Equal Direct (SXLD)

If the C(XR) specified by T1 are greater than positions 18-35 of C(Y), the computer takes the next sequential instruction. If the C(XR) specified by T1 are equal to or less than positions 18-35 of the C(Y), the computer skips the next sequential instruction. With T1 equal to zero, a skip does occur.

3.6.27 Skip on Index Low or Equal Immediate (SXLI)

If the C(XR) specified by T1 are greater than Y, the computer takes the next sequential instruction. If the C(XR) specified by T1 are equal to or less than Y, the computer skips the next sequential instruction. With T1 equal to zero, a skip does occur.

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR (Continued)

3.6.28 Skip on Index High Direct (SXHD)

If the C(XR) specified by T1 are less than or equal to positions 18-35 of C(Y), the computer takes the next sequential instruction. If the C(XR) specified by T1 are greater than positions 18-35 of C(Y), the computer skips the next sequential instruction. With T1 equal to zero, a skip does not occur.

3.6.29 Skip on Index High Immediate (SXHI)

If the C(XR) specified by T1 are less than or equal to Y, the computer skips the next sequential instruction. If the C(XR) specified by T1 are greater than Y, the computer skips the next sequential instruction. With T1 equal to zero, a skip does not occur.

3.6.30 Skip on Index Equal Direct (SXED)

If the C(XR) specified by T1 are not equal to positions 18-35 of C(Y), then the computer takes the next sequential instruction. If the C(XR) are equal to positions 18-35 of C(Y), the computer skips the next sequential instruction. With T1 equal to zero, a skip does not occur.

3.6.31 Skip on Index Equal Immediate (SXEI)

If the C(XR) specified by T1 are not equal to Y, then the computer takes the next sequential instruction. If the

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR (Continued)

3.6.31 (Continued)

C(XR) are equal to Y, the computer skips the next sequential instruction. With T1 equal to zero, a skip does not occur.

3.6.32 Close Loop Forward

The contents of XR2 are added to the C(XR) specified by T1 and the sum replaces the C(XR) specified by T1. The C(XR) specified by T1 is then compared with C(XR1). If C(XR-T1) are less than or equal to C(XR1), the next instruction is taken from location Y. If C(XR-T1) are greater than C(XR1), the next sequential instruction is taken. Use of XR1 and XR2 is implied by the instruction.

3.6.33 Close Loop Reverse

The contents of XR2 are to the C(XR) specified by T1 and the sum replaces the C(XR) specified by T1. The C(XR) specified by T1 is then compared with C(XR1). If C(XR-T1) are greater than or equal to C(XR1), the next instruction is taken from location Y. If C(XR-T1) are less than C(XR1), the next sequential instruction is taken. Use of XR1 and XR2 is implied by the instruction.

3.6.34 Exclusive OR to Storage (ERS)

The C(Y) are replaced by the result obtained by matching bits of C(AC), positions P and 1-35, with the corresponding

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR (Continued)

3.6.34 (Continued)

bits of C(Y), positions S and 1-35. The result will be a one bit if one and only one of the two bits matched is a one bit. Otherwise, the result is a zero bit. The C(AC) are unchanged.

3.6.35 OR Indicators to Storage (OIS)

The C(Y) are replaced by the result obtained by matching bits of C(SI), positions 0-35, with the corresponding bits of C(Y), positions S and 1-35. A resulting bit will be a one if either or both of the two bits matched is a one bit. The result will be a zero only if both of the bits matched are zeros. The C(SI) are unchanged.

3.6.36 Place Characteristics in Index Register (PCHX)

This instruction places the C(AC) 1-8 into the specified $XR_{(10-17)}$ and clears the remaining bits of the XR.

3. Section 3.6.37 Save CPU (SCPU) should be changed to the following:

"The C(AC) positions S and 1-35 are stored in location Y. The overflow trigger, the accumulator P and Q bits, and the three index register compare indicators (High, Low, and Equal) are stored in the left half of location Y + 1. Tag 1 specifies the index registers which are to be stored. Index register 1 is stored in the right half of location Y + 1. Pairs of index registers, beginning with XR2 and XR3 are stored in successive locations beginning with Y + 2. If Tag 1 contains an even number the right half of the storage location will be set to zero."

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR (Continued)

3.6.38 Restore CPU (RCPU)

Positions S and 1-35 of the accumulator are replaced by positions S and 1-35 of location Y. Positions S and 1-17

4. Section 3.6.38 Restore CPU (RCPU) should be changed to the following:

"Positions S and 1-35 of the accumulator are replaced by positions S and 1-35 of location Y. The overflow trigger, the P and Q bits, and the index register compare indicators (High, Low, and Equal) are set from bits in the left half of location Y + 1. Index register 1 is replaced by positions 18-35 of Y + 1. The number of XR's to be loaded is contained in Tag 1. Pairs of XR's beginning with XR2 and XR3 are loaded from successive locations beginning with Y + 1. Tag 1 may contain an even number."

5. Section 3.6.39 Block Index Store (SXR) should be changed to the following:

"XR1 is stored in positions 18-35 of Y. Tag 1 specifies the total number of XR's to be stored. Pairs of XR's beginning with XR2 and XR3 are stored in consecutive locations beginning with Y +1. If T1 is an even number the right half of that storage word is set to zero."

6. Section 3.6.40 Block Index Load (LXR) should be changed to the following:

"Tag 1 specifies the number of XR's to be loaded. XR1 is loaded from positions 18-35 of location Y. Pairs of XR's beginning with XR2 and XR3 are loaded from consecutive locations beginning with Y + 1."

7. Section 3.6.41 Integer Multiply should be changed to the following:

"At the beginning of the operation the multiplier must be in the accumulator. The multiplicand is in location Y. The contents of Y are multiplied by the contents of the accumulator. A 35 bit product plus sign is developed and placed in the accumulator. The sign is set according to the normal rules for multiply. If the resulting product is greater than 35 bits in length the overflow trigger is set and the high order bits are stored in the MQ register."

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR (Continued)

3.6.42 Floating Reciprocal Divide

The C(Y) are divided by the C(AC). The quotient appears in the accumulator and the remainder in the MQ. The sign of the AC is set according to normal rules of division. The sign of the MQ is set to the sign of Y. The C(Y) are not changed. The rules for divide check and trap are the same as for Floating Divide.

3.6.43 Convert Fixed Point to Floating Point (FLT)

The C(Y) is treated as a fixed point binary integer and converted to a normalized floating point binary number. The result is obtained in the C(AC), and the C(Y) are unchanged.

3.6.44 Convert Floating Point to Fixed Point (FIX)

The C(Y) is treated as a floating point binary number and converted to a fixed point binary number. The integer portion of the converted number is obtained in the AC, and the functional remainder is in the MQ. If the $C(Y) > 2^{35}$, a floating point trap will occur.

3.6.45 Transfer and Store Instruction Counter (TSL)

The location of the TSL instruction, plus one, is stored in positions 18-35 of C(Y). Positions S, 1-19 of C(Y) are unchanged. The computer takes its next instruction from location Y + 1.

8. Section 3.6.46 should be changed as follows:

"Shift MQ to Index Register
The C (MQ) position S and 1-35 are shifted left into the XR specified by Tag 1. The number of positions to be shifted is designated by Y modified by the XR specified by T2. Bits shifted out of the XR are lost."

9. Section 3.6.47 should be changed as follows:

"Shift Index Register to Accumulator
The right most n bits of the XR specified by Tag 1 (positions 19 minus n thru position 18) replace positions 36 minus n thru position 35 of the accumulator. The number of bits to be shifted, n, is designated by Y modified by the XR specified by T2. The remaining positions of AC are set to zero. The contents of the XR specified by T1 are unchanged.

cumulator. The number of bits to be shifted, n, is designated by Y modified by the XR's specified by T1 and T2. The remaining positions of AC are set to zero. The contents of XR1 are unchanged.

3.6.48 Shift MQ to Index Register One and Skip

Position's S and 1-35 of the MQ are shifted left into XR1 after XR1 has been reset to zero. The address of the instruction, Y, modified by the contents of the XR specified by T2, is used as a count value, C. C is compared with the contents of the XR specified by T1. The smaller of the two numbers determines the number of positions to be shifted. If the C(XR) specified by T1 is greater than C, the next instruction is skipped. Otherwise, the next sequential instruction is taken.

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR (Continued)

3.6.48 (Continued)

The C(XR) specified by T1 is always decreased by C. If this subtraction reduces the value in the XR below zero, the result will be left in two's complement form.

3.6.49 Shift Index Register One to Accumulator and Skip

Positions P and 1-35 of the Accumulator are shifted left the number of places specified by the count C Y - C (XR specified by T2) or by the contents of the XR specified by T1, whichever is smaller. If the contents of the XR specified by T1 is greater than C, the contents of the XR are logically ORed with the contents of the Accumulator and the result is placed in the Accumulator. The next instruction is skipped.

If the XR specified by T1 is less than or equal to C, XR1 is shifted right C minus the contents of XR1 positions. The remaining contents of the XR1 are ORed with the Accumulator, the result is placed in the accumulator and the next sequential instruction is taken.

The contents of the XR specified by T1 is always decremented by C. If the result is less than zero it remains in two's complement form.

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR (Continued)

3.6.49 (Continued)

The contents of XR1 are unchanged. They are restored to their value at the beginning of the instruction.

3.6.50 Double Precision Floating Point Reciprocal Divide

This instruction execution is the same as Double Precision Floating Point except that the initial factors are reversed. The contents of Y and Y + 1 are divided by the contents of the AC and the MQ. The quotient is placed in the AC and the remainder in the MQ.

3.6.51 Set Memory Protection

The Low Protect Register is set from positions S and 1-9 of location Y and the High Protect Register is set from positions 18-27 of location Y.

3.6.52 Convert BCD to Binary (CDEC)

(To Be Defined)

3.6.53 Convert Binary to BCD (CBIN)

(To Be Defined)

3.6.54 Set Interval Timer

(To Be Defined)

3.6.55 Store Interval Timer

(To Be Defined)

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR (Continued)

3.6.56 Set Real Time Clock

(To Be Defined)

3.6.57 Store Real Time Clock

(To Be Defined)

3.6.58 Restore Channel Trap

The mode is set under control of the bits in positions S, 1-17 of the CPU status location. The next instruction is taken from the location specified by positions 18-35 of the CPU status location. The CPU status location is a fixed word in storage.(See Sections 3.4.1 - 3.4.3)

3.6.59 Set CPU Status (Restore CPU Trap)

The mode is set under control of the bits in positions S, 1-17 of Y. The next instruction is taken from the location specified by positions 18-35 of Y. This instruction may not be executed in the Problem Program Mode. (See Sections 3.5.1 - 3.5.3)

3.6.60 Set Channel Assignment Register

The channel assignment register (one bit for each channel) is set according to the contents of the word fetched from location Y. (See Section 3.3.2)

3.6.61 All 7095 I/O instructions are described in the 7095 Data Channel Functional Objectives.

12. The following instructions should be added:

3.6.62 Transfer on Accumulator Greater Than Zero

If the accumulator is positive and non zero, the next instruction is taken from Y. Otherwise the next sequential instruction follows.

3.6.63 Transfer on Accumulator Less Than Zero

If the accumulator is negative and non zero, the next instruction is taken from Y. Otherwise the next sequential instruction follows.

3.6.64 Double Load Negative

The C(Y) positions 1-35 replace the C(AC) positions 1-35. The C(Y + 1) positions 1-35 replace the C(MQ) positions 1-35. The sign of AC and MQ is set to the opposite of the sign of Y. C(Y) and C(Y + 1) are unchanged.

3.6.65 Double Store Negative

Positions 1-35 of C(AC) replace positions 1-35 of C(Y). Positions 1-35 of C(MQ) replace positions 1-35 of C(Y + 1). The signs of Y and Y + 1 are set to the opposite of the sign of the AC. The C(AC) and C(MQ) are unchanged.

3.6.66 Add One to Storage

The C(Y) are incremented by one. If an overflow occurs no indication is given but the contents of Y positions 1-35 will be zero.

3.6.67 Compare Index Direct

The C(XR) specified by T1 are compared with positions 18-35 of C(Y). If C(XR) are greater than positions 18-35 of C(Y) the Index High Indicator is set. If they are equal the Index Equal Indicator is set. Otherwise the index low indicator is set.

3.6.68 Compare Index Immediate

The C(XR) specified by T1 are compared with Y, positions 18-35 of the instruction. If C(XR) are greater than Y, the Index High Indicator is set. If they are equal, the Index Equal Indicator is set. Otherwise the index low indicator is set.

3.6.69 Transfer Index High

3.6.70 Transfer Index Not High
3.6.71 Transfer Index Low
3.6.72 Transfer Index Not Low
3.6.73 Transfer Index Equal
3.6.74 Transfer Index Not Equal

In the above six instructions, if the transfer condition matches the setting of the Index Compare Indicators, the next instruction is taken from Y. Otherwise, the next sequential instruction is taken.

3.6.75 Test Index and Transfer

The C(XR) specified by T1 is decremented by one. If the result is not zero the next instruction is taken from location Y. If the result is zero, the next sequential instruction follows.

3.6.76 Load Index Signed

The C(XR) specified by T1 is loaded from positions 18-35 of C(Y). If the sign of C(Y) is positive positions 18-35 of C(Y) are loaded directly. If the sign of C(Y) is negative the two's complement of positions 18-35 of C(Y) are loaded into the XR.

3.6.77 Add to Index Signed

If the C(Y) is positive, positions 18-35 of C(Y) are added to C(XR) specified by T1. If the sign is negative, the two's complement of positions 18-35 of C(Y) are added to C(XR) specified by T1.

3.6.78 Subtract from Index Signed

If the C(Y) is positive, positions 18-35 of C(Y) are subtracted from C(XR) specified by T1. If the sign is negative, the two's complement of positions 18-35 of C(Y) are subtracted from C(XR) specified by T1.

3.6.79 Compare Index Signed

The C(XR) specified by T1 are compared with positions 18-35 of C(Y) if the sign of Y is positive, and with the two's complement of positions 18-35 of C(Y) if the sign of Y is negative. The result of the comparison sets the Index High, Low, or Equal Indicator.

3.6.80 Integer Divide or Trap

The C(AC) are divided by C(Y). At the completion of the operation the quotient is in the accumulator and the remainder is in the MQ. If the divisor, C(Y), contains zero a trap occurs. The sign of the accumulator is set according to the normal rules for division. The sign of the MQ is set to the original sign of the accumulator which contained the dividend.

JJWebster/am
4/8/64

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR (Continued)

3.7 7094 Instructions Not Included in New Instruction Format for 7095 Mode

3.7.1 Store Prefix - The function of this instruction is replaced by "Store Accumulator Under Control of the Mask" in Expanded Memory Mode.

3.7.2 Store Decrement - The decrement field is not applicable to the Expanded Memory Mode.

3.7.3 Store Tag - In the Expanded Memory Mode there are two tag fields either of which can be stored by "Store Accumulator Under Control of Mask".

3.7.4 Store Address - The function of this instruction is replaced by "Store Accumulator into Right Half Word".

3.7.5 Transfer on MQ Overflow

3.7.6 Enter Multiple Tag Mode

3.7.7 Leave Multiple Tag Mode

3.7.8 Transfer with Index Incremented - See Table 1 for the instructions which can replace this instruction.

3.7.9 Transfer on Index High - See Table 1.

3.7.10 Transfer on Index Low or Equal - See Table 1.

3.7.11 Transfer on Index - See Table 1.

3.7.12 Transfer on No Index - See Table 1.

3. OPERATIONAL CHARACTERISTICS OF CENTRAL PROCESSOR (Continued)

3.7.13 Variable Length Multiply (VLM)

3.7.14 Divide or Proceed (DVP)

3.7.15 Variable Length Divide or Halt (VDH)

3.7.16 Variable Length Divide or Proceed (VDP)

3.7.17 Floating Divide or Proceed (FDP)

3.7.18 Double-Precision Floating-Point Divide and Proceed (DFDP)

3.7.19 Convert by Replacement from the AC (CVR)

3.7.20 Convert by Replacement from the MQ (CRQ)

3.7.21 Convert by Addition from the MQ (CAQ)

3.7.22 All 7094 I/O instructions have been dropped in the 7095 Mode. The new I/O instructions are described in the 7095 Data Channel Functional Objectives.

3.8 Instruction Execution Changes (Relative to 7094)

3.8.1 All fixed point and floating point divide instructions cause a trap if a divide check occurs. Thus, the Divide or Halt instruction becomes Divide or Trap, etc. (See Section 3.5 for CPU Trap)

3.8.2 Compare Accumulator with Storage

In the 7095 a plus zero is equal to a minus zero when executing the Compare instruction.

CPU TRAP LOCATIONS

Type of Trap	Transfer Address	Modes & Return Addr	Other Conditions
Floating Point or Divide Check	$\mathcal{X}$6	$\mathcal{X}$4	$\mathcal{X}$1 (Spill Code)
Protect Violation or Illegal Operation	$\mathcal{X}$7	$\mathcal{X}$5	$\mathcal{X}$2 (Spill Code)
I/O in Compatible Mode	$\mathcal{X}$8	$\mathcal{X}$5	$\mathcal{X}$2 (Op.Code) $\mathcal{X}$3 (Effective Addr)
Transfer Trap	$\mathcal{X}$9	$\mathcal{X}$5 (Instruction Address)	
Monitor Call	$\mathcal{X}$10	$\mathcal{X}$5	$\mathcal{X}$2 (Effective Addr)

TABLE I

	7095 Instruction	Replacement Instructions
3.7.8	TXI	Add to Index Direct Immediate Transfer
3.7.9	TXH	Skip on Index High Direct/Immediate;
3.7.10	TXL	Skip on Index Low or Equal Direct/Immediate; Skip on Index Equal Direct/Immediate
3.7.11	TIX	Skip on No Index Direc/Immediate Transfer
3.7.12	TNX	Skip on Index Direct/Immediate Transfer

Note: Also see Sections 3.6.32 and 3.6.33 for the Generalized Loop Close instructions.

TABLE II

WORD TRANSMISSION INSTRUCTIONS

	Name	Mnemonic	Notes	7090 Code
1.	Clear and Add	CLA		240
2.	Clear and Add Logical	CAL		-240
3.	Clear and Subtract	CLS		242
4.	Load Left Accumulator	LLA	2	
5.	Load Right Accumulator	LRA	2	
6.	Load MQ Register	LDQ		270
7.	Double Load	DLD		223
8.	Double Logical Load	DLLD	2,4	
9.	Double Load Negative	DLDN	4	301
10.	Store Accumulator	STO		302
11.	Store Logical Word	SLW	4	
12.	Store Accumulator Left	STAL	2	
13.	Store Accumulator Right	STAR	2	
~~14.~~	~~Store Accumulator Magnitude~~	~~STAM~~	~~2~~	
15.	Store Accumulator Negative	STAN	2	
16.	Store Prefix	STP	1	-
17.	Store Decrement	STD	1	-
18.	Store Tag	STT	1	-
19.	Store Address	STA	1	-
20.	Store MQ Register	STQ		-300
21.	Store Left MQ	SLQ		-310
22.	Double Store	DST		-303
23.	Double Logical Store	DLST	4	
24.	Double Store Negative	DSTN	2	300
25.	Store Zeros	STZ		-315
26.	Store Instruction Counter	STL		051
27.	Exchange AC and MQ	XCA		-051
28.	Exchange Logical AC and MQ	XCL	4	370...4
29.	Enter Keys	ENK		
30.	Save Central Processor	SCPU	2	
31.	Restore Central Processor	RCPU	2	

FIXED POINT OPERATIONS

32.	Add	ADD		200
33.	Add Magnitude	ADM		201
34.	Add and Carry Logical	ACL		171
35.	Subtract	SUB		202
36.	Subtract Magnitude	SBM		-200
37.	Multiply	MPY		100
38.	Multiply and Round	MPR		-100
39.	Integer Multiply	IMP	2	

FIXED POINT OPERATIONS (Continued)

	Name	Mnemonic	Notes	7094 Code
40.	Variable Length Multiply	VLM	7	104
41.	Round	RND		370...10
42.	Divide and Proceed	DVP	1	-
43.	Divide or Halt	DVH	1	-
44.	Divide or Trap	DVT	2, 6	111
45.	Integer Divide or Trap	IDV	2	
46.	Variable Divide and Proceed	VDP	1	-
47.	Variable Divide or Halt	VDH	1	-
48.	Variable Divide or Trap	VDT	2, 6, 7	115

FLOATING POINT OPERATIONS

49.	Floating Add	FAD		140
50.	Floating Add Magnitude	FAM		144
51.	Unnormalized Floating Add	UFA		-140
52.	Unnormalized Floating Add Magnitude	UAM		-144
53.	Floating Subtract	FSB		142
54.	Floating Subtract Magnitude	FSM		146
55.	Unnormalized Floating Subtract	UFS		-142
56.	Unnormalized Floating Subtract Magnitude	USM		-146
57.	Floating Multiply	FMP		130
58.	Unnormalized Floating Multiply	UFM		-130
59.	Floating Round	FRN		370..11
60.	Floating Divide and Proceed	FDP		121
61.	Floating Divide or Halt	FDH		120
62.	Floating Divide or Trap	FDT	2, 6	121
63.	Floating Reciprocal Divide or Trap	FRD	2	
64.	Add to Exponent	ADXP	2	
65.	Double Floating Add	DFAD		141
66.	Double Floating Add Magnitude	DFAM		145
67.	Double Unnormalized Floating Add	DUFA		-141
68.	Double Unnormalized Floating Add Magnitude	DUAM		-145
69.	Double Floating Subtract	DFSB		143
70.	Double Floating Subtract Magnitude	DFSM		147
71.	Double Unnormalized Floating Subtract	DUFS		-143
72.	Double Unnormalized Floating Subtract Magnitude	DUSM		-147
73.	Double Floating Multiply	DFMP		131
74.	Double Unnormalized Floating Multiply	DUFM		-131
75.	Double Floating Divide and Proceed	DFDP	1	-
76.	Double Floating Divide or Halt	DFDH	1	-
77.	Double Floating Divide or Trap	DFDT	2, 6	-121
78.	Double Floating Reciprocal Divide or Trap	DFRD	2	

SHIFTING OPERATIONS

	Name	Mnemonic	Notes	7094 Code
79.	Accumulator Left Shift	ALS		377
80.	Accumulator Right Shift	ARS		-377
81.	Long Left Shift	LLS		373
82.	Long Right Shift	LRS		375
83.	Logical Left Shift	LGL		-373
84.	Logical Right Shift	LGR		-375
85.	Rotate MQ Left	RQL		-372

CONTROL OPERATIONS

86.	No Operation	NOP		371
87.	Halt and Proceed	HPR		210
88.	Halt and Transfer	HTR		000
89.	Execute	XEC		252
90.	Transfer	TRA		010
91.	Trap Transfer	TTR		011
92.	Transfer on Zero	TZE		040
93.	Transfer on No Zero	TNZ		-040
94.	Transfer on Plus	TPL		050
95.	Transfer on Minus	TMI		-050
96.	Transfer on Zero or Minus	TZM	2	
97.	Transfer on Zero or Plus	TZP	2	
98.	Transfer Greater than Zero	TGZ	2	
99.	Transfer Less than Zero	TLZ	2	
100.	Transfer on Overflow	TOV		060
101.	Transfer on No Overflow	TNO		-060
102.	Transfer on MQ Plus	TQP		072
103.	Transfer on Low MQ	TLQ		020
104.	Plus Sense	PSE		370
105.	Minus Sense	MSE		-370
106.	P Bit Test	PBT	4	-370...1
107.	Low Order Bit Test	LBT		370...1
108.	Divide Check Test	DCT	1	370..12
109.	Storage Zero Test	ZET		250
110.	Storage Not Zero Test	NZT		-250
111.	Compare Accumulator with Storage	CAS		160
112.	Logical Compare Accumulator with Storage	LAS		-160
113.	Transfer and Store Location	TSL		
114.	Set Memory Protect	SMP	2	
115.	Enter Trapping Mode	ETM		370...7

CONTROL OPERATIONS (Continued)

	Name	Mnemonic	Notes	7095 Code
116.	Leave Trapping Mode	LTM		-370...7
117.	Enter Multiple Tag Mode	EMTM		-370..16
118.	Leave Multiple Tag Mode	LMTM		370..16
119.	Load Interval Timer	LTMR	2	
120.	Store Interval Timer	STMR	2	
121.	Load Real Time Clock	LRTC	2	
122.	Store Real Time Clock	SRTC	2	
123.	Channel Trap Return	CTR	2	
124.	Processor Trap Return	PTR	2	
125.	Set Channel Assignment Return	SCAR	2	
126.	Call Monitor	CMON	2	

INDEX REGISTER OPERATIONS

127.	Address to Index True	AXT	3	374
128.	Address to Index Complemented	AXC	3	-374
129.	Place Address in Index	PAX, PRX	3	354
130.	Place Complement of Address in Index	PAC, PRC	3	357
131.	Place Index in Address	PXA, PXR	3	364
132.	Place Index in Decrement	PXD, PXL	3	-364
133.	Place Complement of Decrement in Index	PDC, PLC	3	-357
134.	Place Complement of Index in Decrement	PCD, PCL	3	-366
135.	Place Complement of Index in Address	PCA, PCR	3	366
136.	Store Index in Address	SXA, SXR	3	314
137.	Store Index in Decrement	SXD, SXL	3	-314
138.	Store Complement of Index in Address	SCA, SCR	3	316
139.	Store Complement of Index in Decrement	SCD, SCL	3	-316
140.	Load Index from Address	LXA, LXR	3	254
141.	Load Index from Decrement	LXD, LXL	3	-254
142.	Load Complement of Address in Index	LAC, LRC	3	255
143.	Load Complement of Decrement in Index	LDC, LLC	3	-255
144.	Add to Index Signed	ADXS	2	
145.	Add to Index Direct	ADXD	2	
146.	Add to Index Immediate	ADXI	2	
147.	Subtract from Index Signed	SBXS	2	
148.	Subtract from Index Direct	SBXD	2	
149.	Subtract from Index Immediate	SBXI	2	
150.	Place Characteristic in Index	PCHX	2	
151.	Transfer and Set Index	TSX		041
152.	Transfer on Index Incremented	TXI	1	-
153.	Transfer on Index High	TXH	1	-
154.	Transfer on Index Low or Equal	TXL	1	-
155.	Transfer on Index	TIX	1	-

INDEX REGISTER OPERATIONS (Continued)

	Name	Mnemonic	Notes	7095 Code
156.	Transfer on No Index	TNX	1	-
157.	Test Index and Transfer	TXT	2	
158.	Transfer Index High	TXRH	2	
159.	Transfer Index Not High	TXNH	2	
160.	Transfer Index Low	TXRL	2	
161.	Transfer Index Not Low	TXNL	2	
162.	Transfer Index Equal	TXRE	2	
163.	Transfer Index Not Equal	TXNE	2	
164.	Load Index Signed	LXS	2	
~~165.~~	~~Store Index Signed~~	~~SXS~~	~~2~~	
166.	Compare Index Signed	CXS	2	
167.	Compare Index Direct	CXD	2	
168.	Compare Index Immediate	CXI	2	
169.	Close Loop Forward	XLF	2	
170.	Close Loop Backward	XLB	2	
171.	Store Multiple Index	SMX	2	
172.	Load Multiple Index	LMX	2	

LOGICAL OPERATIONS

173.	OR to Accumulator	ORA		-241
174.	OR to Storage	ORS		-302
175.	AND to Accumulator	ANA		-150
176.	AND to Storage	ANS		150
177.	Exclusive OR to Accumulator	ERA		152
178.	Exclusive OR to Storage	ERS	2	
179.	Complement Magnitude	COM		370...6
180.	Clear Magnitude	CLM		370...0
181.	Change Sign	CHS		370...2
182.	Set Sign Plus	SSP		370...3
183.	Set Sign Minus	SSM		-370...3
184.	Add One to Storage	ADOS	2	

SENSE INDICATOR OPERATIONS

185.	Load Indicators	LDI		221
186.	Store Indicators	STI		304
187.	Place Accumulator in Indicators	PAI		024
188.	Place Indicators in Accumulator	PIA		-026
189.	OR Accumulator to Indicators	OAI		023
190.	OR Storage to Indicators	OSI		222

SENSE INDICATOR OPERATIONS (Continued)

	Name	Mnemonic	Notes	7095 Code
191.	OR Indicators to Storage	OIS	2	
192.	Reset Indicators Left	RIL		-037
193.	Reset Indicators Right	RIR		037
194.	Set Indicators Left	SIL		-035
195.	Set Indicators Right	SIR		035
196.	Reset Indicators from Accumulator	RLA		-022
197.	Reset Indicators from Storage	RIS		225
198.	Invert Indicators from Accumulator	IIA		021
199.	Invert Indicators from Storage	IIS		220
200.	Invert Indicators Left	IIL		-031
201.	Invert Indicators Right	IIR		031
202.	Off Test for Indicators	OFT		224
203.	On Test for Indicators	ONT		226
204.	Right Off Test for Indicators	RFT		034
205.	Right On Test for Indicators	RNT		036
206.	Left Off Test for Indicators	LFT		-034
207.	Left On Test for Indicators	LNT		-036
208.	Load Accumulator Under Control of Indicators	LACI	2	
209.	Store Accumulator Under Control of Indicators	SACI	2	
210.	Insert Accumulator Under Control of Indicators	IASI	2	
211.	Compare Accumulator Under Control of Indicators	CASI	2	

SPECIAL PURPOSE OPERATIONS

212.	Convert Fixed to Floating Point	FLT	2	
213.	Convert Floating to Fixed Point	FIX	2	
214.	Convert BCD to Binary	CDEC	2	
215.	Convert Binary to BCD	CBIN	2	
216.	Convert by Addition from MQ	CAQ	1	-
217.	Convert by Replacement from MQ	CRQ	1	-
218.	Convert by Replacement from Accumulator	CVR	1	-
219.	Shift MQ to Index Left	SQXL	2	
220.	Shift Index to Accumulator Right	SXAR	2	
221.	Shift MQ to Index and Test	SQXT	2	
222.	Shift Index to Accumulator and Test	SXAT	2	
223.	Channel Test or Start	CTS	2	
224.	Channel Test	CHT	2	
225.	Store Channel	SCHX	2	
226.	Halt Channel	HCHX	2	
227.	Inhibit Channel Traps	ICT	2	
228.	Set Bulk Storage Protect	SBP	2	

NOTES

1. Applicable only in 7094 mode. 7094 codes apply.

2. Applicable only in 7095 mode.

3. Redefined in 7095 mode. Reference to "decrement" becomes left half word, "address" becomes right half word.

4. Dependant upon definition of "P" bit.

5. None

6. Divide and proceed codes are used in 7095 mode for Divide and Trap operation.

7. Count specified by T_1 field.

7095 DATA CHANNEL
FUNCTIONAL OBJECTIVES

1 DESCRIPTION

1.1 The 7095 Data Channel provides the input-output paths and control flexibility essential to the 7095 Data Processing System. Effective channel operation is attained by a streamlined instruction-command set and a comprehensive trap system.

1.2 The Data Channel attaches NPL input-output devices to the system via the NPL Interface.

2 GENERAL CHARACTERISTICS

2.1 The 7095 Data Channel is a stored program channel providing seven basic commands:

1) Read
2) Write
3) Sense
4) Control (including Control Immediate)
5) Read Backward
6) Transfer in Channel
7) Execute

Operations that require data transmission will fetch a Data Control Word (DCW) which contains Word Count and Starting Address of the data, along with flags for indirect addressing; non-transmission; and chaining to another DCW.

2.2 When a trap condition occurs which has been previously enabled, the channel will generate a trap. If the condition occurs but is not enabled, it will never generate a trap.

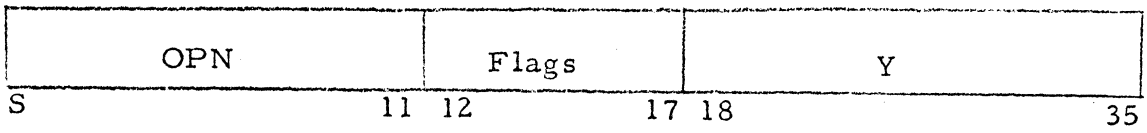
When a channel trap occurs, all subsequent channel traps are automatically inhibited until restored by the main program. Traps may also be inhibited selectively by channel under main program control. Whenever a channel is inhibited it will save all trap conditions that are enabled until the inhibit is removed, at which time a trap will be generated.

A channel trap will store address and status information in three fixed core locations. The channel will then cause the CPU to execute one of three fixed locations; one each per channel for end, unusual end, and attention.

3 OPERATIONAL CHARACTERISTICS

3.1 Channel Commands

All channel commands have the following format



Pos. S-11 - Operation -

The format required by the NPL Control Units will be used. Positions S, 1, 2 equal to 7 octal cause the channel to decode 3-11 as operation code, and if position 3 is zero then 4-11 are sent to the control unit.

3.1 Channel Commands (continued)

S	1	2	3	4	5	6	7	8	9	10	11	
1	1	1	0	M	M	M	M	0	1	0	0	Sense
1	1	1	0	M	M	M	M	1	1	0	0	Read Backward
1	1	1	0	M	M	M	M	M	M	0	1	Write
1	1	1	0	M	M	M	M	M	M	1	0	Read
1	1	1	0	M	M	M	M	M	M	1	1	Control
1	1	1	1	0	0	0	0	0	0	0	0	Transfer in Channel
1	1	1	1	0	0	0	0	0	0	0	1	Execute

M - Modifier Bit - Interpreted by the Control Unit.

Pos 12-17 - Command Flags -

Pos 12 - Spare

Pos 13 - 6 Bit Mode

The channel normally operates in 8-bit mode. This position flags 6-bit operation.

Pos 14 - BCD Mode

The channel normally operates in Binary mode. This position flags BCD operation.

Pos 15 - Advance/Disconnect

*Advance - The channel advances to the next sequential command upon completion of the current operation.

Disconnect - The channel is disconnected upon completion of the current operation.

*While advancing the channel ignores Data Control words, and continues to advance until a command is interpreted.

3.1 Channel Commands (continued)

Pos 16 - Indirect Addressing -

Those operations which refer to Y, may be indirectly addressed.

Pos 17 - Immediate -

1) Indicates a Control operation which does not require a Data Control Word.

2) Indicates an immediate address.

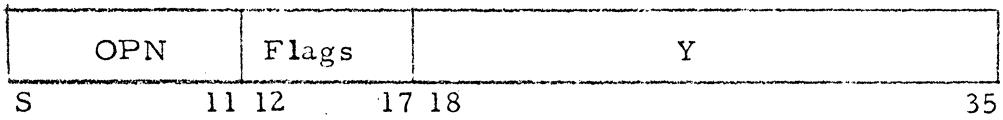
Pos 18-35 - Address -

The address will contain:

1) The Transfer Address of a TCH.

2) The operand of an Execute.

Command Operations



Control Unit Operations

Operation	Opn Code	Applicable Flags
Write	7001	A/D, 6/8, BCD
Read	7002	A/D, 6/8, BCD
*Control	7003	A/D, IMM, I/A
Sense	7004	A/D
Read Backward	7014	A/D, 6/8, BCD

All Control Unit Operations require a Data Control Word except Control Immediate.

*Control Immediate - The control information is contained in Pos 4-9 of the control command.

3.1 Channel Commands (continued)

Sequence Operations

Operation	Opn Code	Applicable Flags
TCH, Y	7400	A/D, I/A
XEC, Y	7401	A/D, I/A

Description

TRANSFER CHAN - TCH, Y

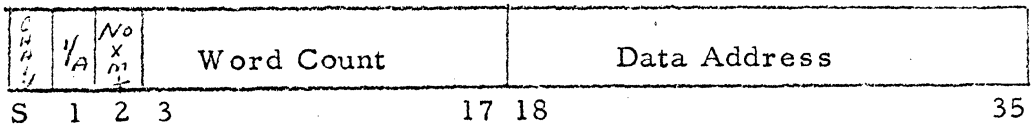
The channel transfers to location Y, for its next command or data control word.

EXECUTE - XEC, Y

The channel executes the command or control word at location Y. When that command has been completed, the channel returns to the location of the XEC command plus one for its next command.

3.2 Data Control Word

The following format will be used for the Data Control Word:



Pos S - DCW Chaining -

Data transmission may be controlled as follows:

1. With the chain bit on:

   a. When the word counter is equal to 0 the channel proceeds to the next sequential DCW, and Data transmission continues under the current command.

3.2 Data Control Word (continued)

b. When an End Signal is received from the control unit, data transmission is terminated. At this time the Option to disconnect the channel, or advance to a new command is determined by the status of the Advance/Disconnect bit in the current command.

2. With the chain bit off:

Data transmission is terminated when either the Word Counter is equal to zero or an End signal is received from the control unit, whichever occurs first. The Advance or Disconnect option is again determined by the status of the Advance/Disconnect bit in the current command.

Pos 1 - Indirect Addressing -

Permits indirect addressing of the Data Address. If sign bit is on in indirect word, the channel will interpret pos 13-35 as the data address.

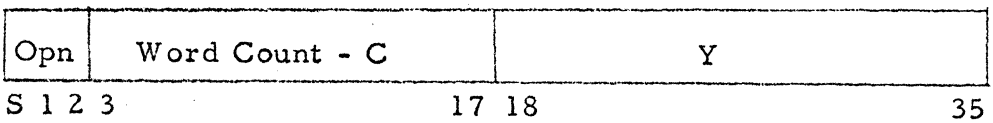
Pos 2 - No Transmission -

The transmission of Data to memory may be inhibited for (N) words under control of the word counter.

Pos 3-17 - Word Count

Pos 18-35 - Data Address

Data Control Word Operations



3.2 Data Control Word (continued)

Positions S, 1 and 2 are coded to provide the following Data Control Word operations:

Operation		Octal Opn Code
TCW	(Terminate Control Word)	0
TCW*	(Terminate Control Word IA)	2
CCW	(Chain Control Word)	4
CCWN	(Chain Control Word Non-Transmit)	5
CCW*	(Chain Control Word IA)	6

Description

Terminate Control Word - TCW, Y, C

The chan. terminates transmission under the current command when the word counter is equal to zero or an end is received from the control unit whichever occurs first.

Terminate Control Word I/A - TCW*, Y, C

Positions 18-35 of location Y, replace the contents of the address counter. Transmission then proceeds under TCW control.

Chain Control Word - CCW, Y, C

The chan. terminates transmission under the current command when an End signal is received from the control unit. If the word counter is equal to zero, and an End signal has not been received from the control unit, the chan. proceeds to the next sequential location. A new DCW may be brought into continue Data Transmission under the current command.

3.2 Data Control Word (continued)

Chain Control Word Non-Transmit - CCWN, Y, C

Data transmission is suppressed for C-words. The chan then proceeds under CCW control.

Chain Control Word I/A - CCW*, Y, C

Positions 18-35 of location Y, replace the contents of the address counter. Transmission then proceeds under CCW control.

3.3 Channel Trap

Each channel may be enabled to trap one of three locations. The Trap location is determined by the type of trap that occurs; End, Unusual End or Attention.

The conditions which may cause each type of trap are listed as follows:

1. End Trap - The Trap will occur if the chan. is free of any error, or unusual conditions at the completion of a command which does not have the advance bit on.
2. Unusual End Trap - Will cause a trap when one of the following unusual conditions appear at the completion of a command:
   a. Data Error
   b. Exceptional Condition (End of File, etc.)
   c. Intervention Required
   d. Incorrect Length

Enable Trap bits required - Unusual End (a, b, c)

Incorrect Length (d)

3.3 Channel Trap (continued)

If the channel advance bit is on in the current command, the channel will be disconnected only if an unusual end occurs.

3. Attention Trap - 1) Will cause a trap when an attention or unit freed signal is received from the Control Unit.

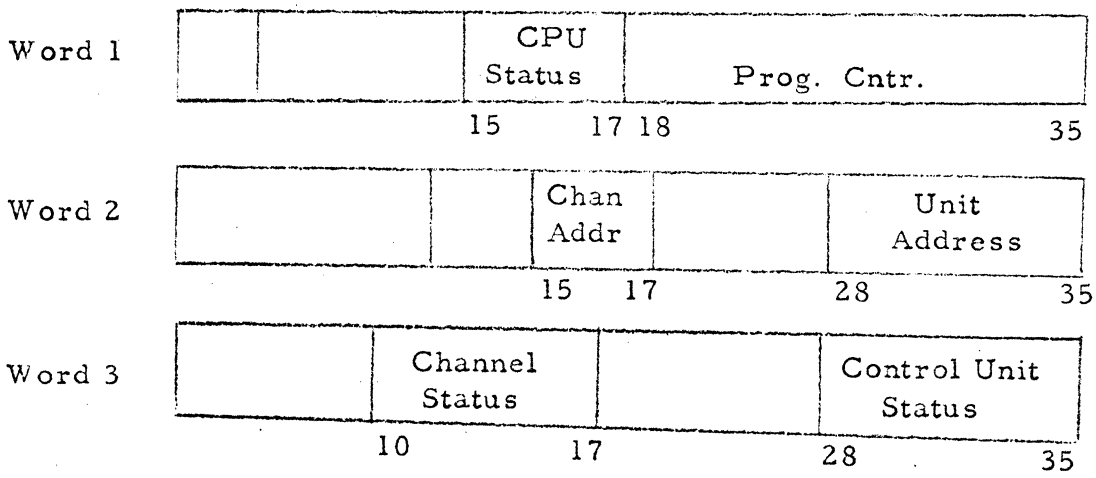
a) Enabled Attention Immediate - The trap will occur as soon as attention is received from the Control Unit.

b) Enabled Attention Not in Use - The trap will occur as soon as the channel is not in use after an attention has been received.

2) Will cause a trap when chaining between Data Control Words.

Enable Trap Bit required - Chain Trap.

Each channel trap will perform a three word store. The format is as follows:

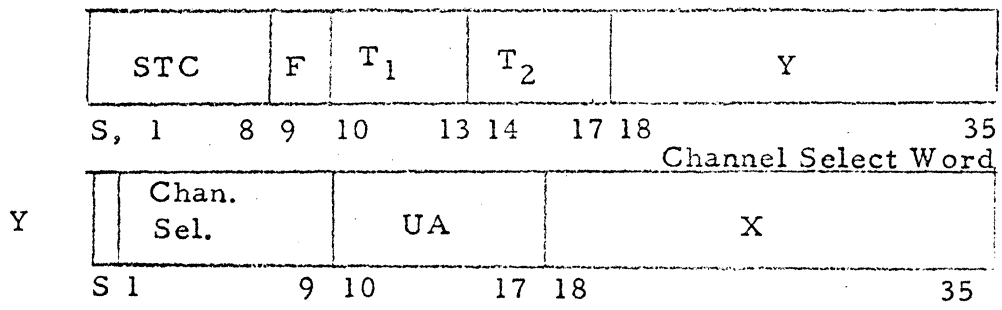


3.4 I/O Instructions

3.4.1 STC Start Channel (Skip Type)

All I/O Instructions, except Restore Channel Traps require a Channel Select Word (CSW). The format for the CSW is as follows:

Pos.	I/O Instruction	Function
S	STC, CHT, SCH	Ignore Memory Protect
1	ALL	Special Chan. Sel.
2	ALL	Sel Chan A
3	ALL	Sel Chan B
4	ALL	Sel Chan C
5	ALL	Sel Chan D
6	ALL	Sel Chan E
7	ALL	Sel Chan F
8	ALL	Sel Chan G
9	ALL	Sel Chan H
10-17	STC, CHT	Unit Address, 0-256
18-35	STC, CHT, SCH	Memory Address
30-35	ENB	Trap Mask



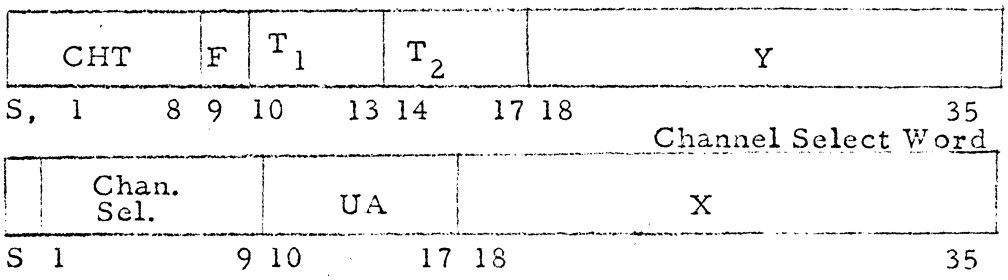
3.4 I/O Instructions (continued)

The STC instruction specifies the location (Y) of a Channel Select Word (CSW). The CSW contains the address of the channel and unit to be selected and the location (X) of the first channel command.

If the selected channel is not busy it clears previous status, accepts the unit address and loads its first command from X. The CPU then skips the next sequential instructions.

If the selected channel is busy, no action is taken and the CPU proceeds to its next sequential instruction. Only one channel may be specified in the CSW.

3.4.2 CHT Channel Test Instruction (Skip Type)

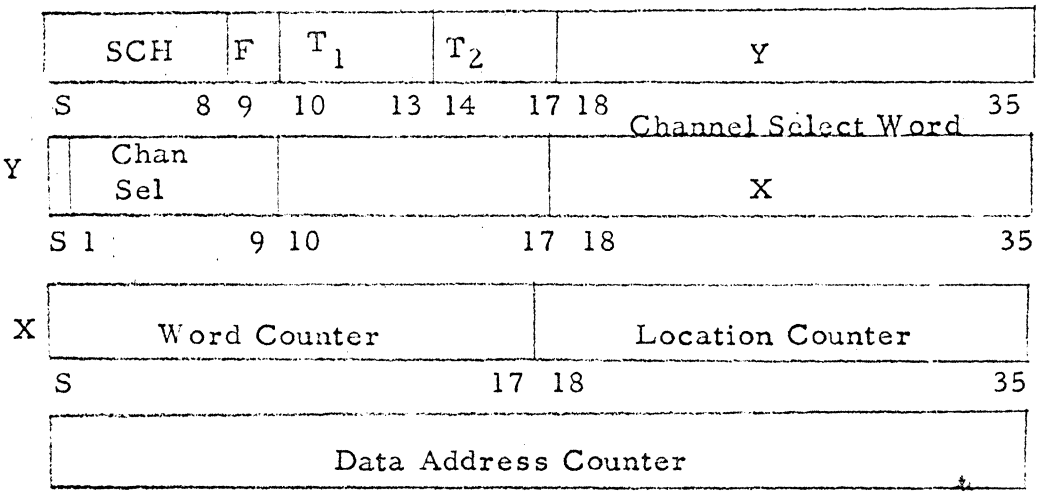


The CHT instruction specifies the location (Y) of a Channel Select Word (CSW). The CSW contains the address of the channel and unit to be tested and the location (X) in which status will be stored. If the channel and device is available, the CPU skips the next sequential instruction. If the channel and/or device are not available, the CPU proceeds to the next

3.4 I/O Instructions (continued)

sequential instruction. In either case channel stores status at location X. Only one chan. may be specified in the CSW.

3.4.3 SCH Store Channel

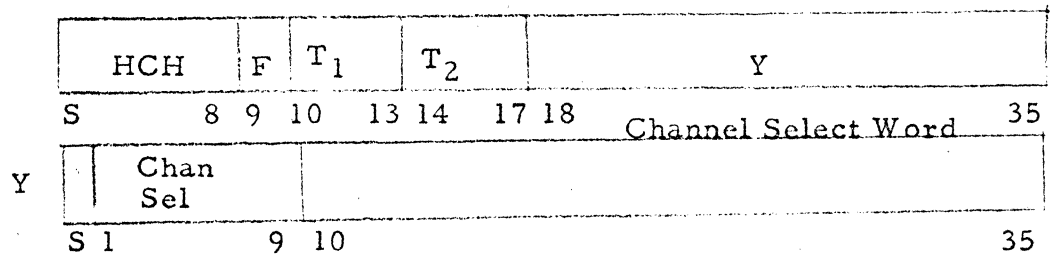


The SCH instruction specifies the location (Y) of a Channel Select Word (CSW).

The CSW specifies the channel whose counters are to be stored. The address (X) specifies the locations (X and X + 1) into which the Location Counter, Word Counter and Data Address Counter are stored.

Only one channel may be specified in the CSW.

3.4.4 HCH Halt Channel

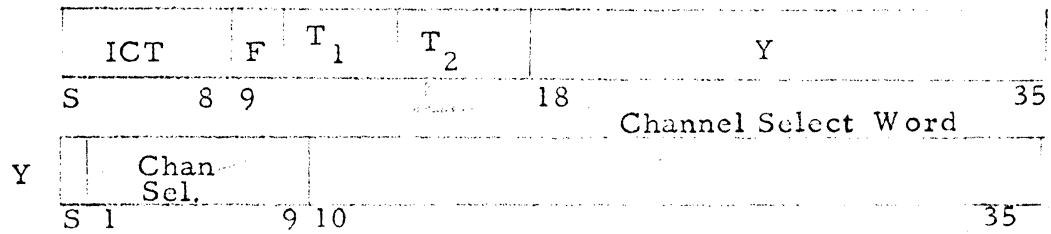


3.4 I/O Instructions (continued)

The HCH instruction specifies the location (Y) of a Channel Select Word (CSW). The CSW specifies the channels to be halted. This instruction causes the specified channel to come to an orderly halt at the end of its current command.

Up to eight channels may be specified in the CSW.

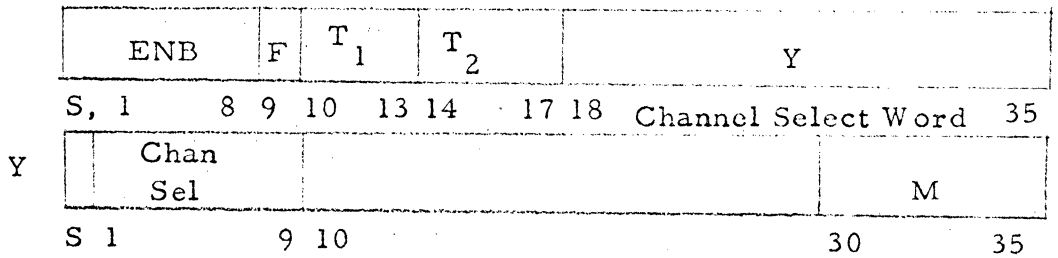
3.4.5 ICT Inhibit Channel Traps



The ICT instructions specifies the location (Y) of a Channel Select Word (CSW). The CSW selectively inhibits channels from trapping. If a channel trap has been enabled, and this channel is inhibited, the trap will wait in the channel until the inhibit is removed.

Up to eight channels may be specified in the CSW.

3.4.6 ENB Enable Channel Traps



3.4 I/O Instructions (continued)

The ENB instruction specifies the location (Y) of a Channel Select Word (CSW). The CSW specifies the channels to be enabled, and the enable mask (M). The enable mask will be interpreted by the specified channels as follows:

Pos 30 - Chain Trap

Pos 31 - Attention Immediate

Pos 32 - Attention Not in Use

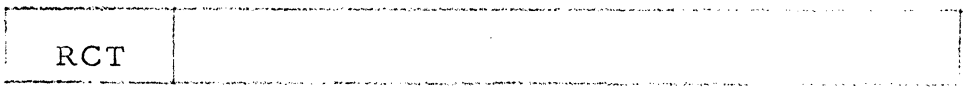
Pos 33 - End

Pos 34 - Unusual End

Pos 35 - Incorrect Length.

Channels not specified are not affected.

3.4.7 RCT Restore Channel Traps



After a channel trap has occurred, all further channel traps are automatically inhibited. The RCT instruction allows channel traps subject to the mask set by the most recent ICT.