IBM CONFIDENTIAL

EVALUATION of 7095 FUNCTIONAL OBJECTIVES

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I. INTRODUCTION

This study report contains the results of an evaluation, by CSC, of the 7095 data processing system, as described in the following IBM Documents:

1. 7095 DATA PROCESSING SYSTEM, FUNCTIONAL OBJECTIVES; Revision 2, dated April 7, 1964.
2. 7095 DATA CHANNEL, FUNCTIONAL OBJECTIVES; dated April 10, 1964.

Section II presents the instruction set recommended by CSC as a result of this evaluation.

Section III summarizes specific alterations proposed by CSC.

Sections IV and V contain clarification of certain portions of the above-mentioned IBM documents.

II. RECOMMENDED 7095 INSTRUCTION SET

Table A lists the proposed 7095 instruction set. CSC additions to this set are denoted by an asterisk.

TABLE A. RECOMMENDED 7095 INSTRUCTION SET

1. MEMORY/AC-MQ

LDA	Load AC
LDN	Load AC negative
LLW	Load logical word
LMW	Load masked word
LMP	*Load masked positions of AC
LLH	Load AC from left half word
LRH	Load AC from right half word
STO	Store AC
STN	Store AC negative
SLW	Store logical word
SMW	Store masked word
SMP	Store masked positions of AC
SLH	Store AC in left half word
SRH	Store AC in right half word
LDQ	Load MQ
STQ	Store MQ
DLD	Double load
DLN	Double load negative
DLL	Double load logical
DST	Double store
DSN	Double store negative
DSL	Double store logical

2. MEMORY/INDEX REGISTERS

LXS	Load index from signed word
LXL	Load index with left half word
LXR	Load index with right half word
LXI	Load index immediate
LCS	*Load index with complement from signed word
LCL	Load index with complement left half
LCR	Load index with complement right half
LCI	Load index with complement immediate
SXL	Store index in left half word
SXR	Store index in right half word
SXS	*Store index in full word
SCL	Store index complement in left half word
SCR	Store index complement in right half word
SCS	*Store index complement in full word

BXL	Block index load
BXS	Block index store
DXL	*Double index load
DXS	*Double index store

3. AC/INDEX REGISTERS

PAX	Place accumulator in index
PCX	Place complement accumulator in index
PCHX	Place characteristic in index
PXA	Place index in accumulator
PCA	Place index complement in accumulator

4. AC, MQ/INDEX REGISTERS

QXS	Shift MQ to index
QXT	Shift MQ to index and test
XAS	Shift index to accumulator
XAT	Shift index to accumulator and test

5. INDEX ARITHMETIC AND TESTING

ASX	Add signed word to index
ALX	*Add left half word to index
ARX	Add right half word to index
AIX	Add immediate to index
SSX	Subtract signed word from index
SLX	*Subtract left half word from index
SRX	Subtract right half word from index
SIX	Subtract immediate from index
CXS	Compare index to signed word
CXL	*Compare index to left half word
CXR	Compare index to right half word
CXI	Compare index to immediate

6. AC MODIFICATION

SSP	Set sign plus
SSM	Set sign minus
CHS	Change sign
CLM	Clear magnitude
COM	Complement magnitude
XCA	Exchange AC with MQ
XCL	Exchange logical AC with MQ

7. FIXED POINT ARITHMETIC

ADD	Add
ADM	Add magnitude
SUB	Subtract
SBM	Subtract magnitude
MPY	Multiply
MPR	Multiply and round
VLM	Variable length multiply
IMP	Integer multiply
RND	Round
DIV	Divide or trap
VLD	Variable length divide or trap
IDV	Integer divide or trap
ACL	Add and carry logical
ADC	Add to characteristic
AOS	Add one to storage
SOS	*Subtract one from storage

8. FLOATING POINT ARITHMETIC

FAD	Add
FAM	Add magnitude
FSB	Subtract
FSM	Subtract magnitude
FMP	Multiply
FRN	Round
FDV	Divide or trap
FRD	Reciprocal divide or trap

9. UN-NORMALIZED FLOATING POINT

UAD	Add
UAM	Add magnitude
USB	Subtract
USM	Subtract magnitude
UMP	Multiply

10. DOUBLE-PRECISION FLOATING POINT

DFAD	Add
DFAM	Add magnitude
DFSB	Subtract
DFSM	Subtract magnitude

DFMP	Multiply
DFDV	Divide or trap
DFRD	Reciprocal divide or trap

11. UN-NORMALIZED DOUBLE-PRECISION FLOATING POINT

DUAD	Add
DUAM	Add magnitude
DUSB	Subtract
DUSM	Subtract magnitude
DUFM	Multiply

12. SHIFTING OPERATIONS

ALS	Accumulator left shift
ARS	Accumulator right shift
LLS	Long left shift
LRS	Long right shift
LGL	Logical left shift
LGR	Logical right shift
RQL	Rotate MQ left
RQR	*Rotate MQ right
XLS	Index left shift
XRS	Index right shift

13. CONDITIONAL TRANSFER OF CONTROL

TGT	Transfer if greater than comparison
TEQ	Transfer if equal comparison
TLT	Transfer if less than comparison
TLE	Transfer if less than or equal comparison
TNE	Transfer if not equal comparison
TGE	Transfer if greater than or equal comparison
TZE	Transfer if zero
TZP	Transfer if zero or plus
TZM	Transfer if zero or minus
TPL	Transfer if plus
TNZ	Transfer if not zero
TLZ	Transfer if not zero or plus (less than zero)
TGZ	Transfer if not zero or minus (greater than zero)
TMI	Transfer if minus
TLQ	Transfer if less than MQ
TQP	Transfer if MQ positive
TOV	Transfer if overflow
TNV	Transfer if no overflow

TIO	Transfer when indicators on
TIF	Transfer when indicators off
TXLE	Transfer on index less than or equal
TXGE	Transfer on index greater than or equal
TIX	Transfer on index (decrement = 1)
TNX	*Transfer on no index (decrement = 1)

14. UNCONDITIONAL TRANSFER OF CONTROL

TRA	Transfer
TSX	Transfer and set index
TSL	Transfer and store location counter
TTR	Trap transfer

15. MULTIPLE SKIP TESTS

CAS	Compare accumulator to storage
LAS	Compare logical accumulator to storage
CMW	Compare marked word

16. SINGLE SKIP TESTS

PBT	P bit on test
LBT	Low bit on test
ZET	Storage zero test
NZT	Storage non-zero
PLT	*Storage plus test
MIT	*Storage minus test
SLT	Sense light test
SWT	Sense switch test
LNT	Left indicators on test
RNT	Right indicators on test
LFT	Left indicators off test
RFT	Right indicators off test
ONT	Indicators on test
OFT	Indicators off test

17. LOGICAL OPERATIONS

ORA	OR to accumulator
ORS	OR to storage
ANA	AND to accumulator
ANS	AND to storage
ERA	Exclusive OR to accumulator
ERS	Exclusive OR to storage

18. SENSE INDICATOR OPERATIONS

LDI	Load indicators
STI	Store indicators
PAI	Place accumulator in indicators
PIA	Place indicators in accumulator
OAI	OR accumulator to indicators
OSI	OR storage to indicators
OIS	OR indicators to storage
SIL	Set indicators of left half
SIR	Set indicators of right half
RIA	Reset indicators from accumulator
RIS	Reset indicators from storage
RIL	Reset indicators of left half
RIR	Reset indicators of right half
IIA	Invert indicators from accumulator
IIS	Invert indicators from storage
IIL	Invert indicators of left half
IIR	Invert indicators of right half

19. MISCELLANEOUS

SCPU	Save CPU
RCPU	Restore CPU
FLT	Convert fixed point to floating point
FIX	Convert floating point to fixed point
CDB	Convert BCD to binary
CBD	Convert binary to BCD
SMP	Set memory protection
SBP	Set bulk memory protection
LTMR	Load interval timer
STMR	Store interval timer
LRTC	Load real time clock
SRTC	Store real time clock
STZ	Store zero
STL	Store location counter
ENK	Enter keys

20. DATA CHANNEL INSTRUCTIONS

CST	Channel start or test
CHT	Channel test
SCH	Store channel
HCH	Halt channel
ICH	Inhibit channel traps

SCA	Set channel assignment register
ECH	Enable channel traps

21. SPECIAL CONTROL

NOP	No operation
XEC	Execute
MTR	Call monitor
HTR	Halt and transfer
HPR	Halt and proceed
ETM	Enter trapping mode
LTM	Leave trapping mode
CTR	Channel trap return
PTR	Processor trap return

In Table B are listed four instructions; CSC recommends the deletion of of these from the 7095 Instruction Set.

TABLE B. RECOMMENDED DELETIONS FROM 7095 INSTRUCTION SET

21	SLQ	Store left MQ
132	PXD	Place index in decrement
133	PDC	Place complement of decrement in index
134	PCD	Place complement of index in decrement

III. OPERATIONAL RECOMMENDATIONS

CSC's recommendations, and the relevant factors leading to those recommendations, are as follows:

1. CHARACTER ORIENTATION

1.1 It is strongly recommended that the 7095 Data Channel permit a six-bit internal character representation.

a. An eight-bit representation would entail drastic degradation of performance; for example:

b. The parasite system would require one-third more disk space; a 132-character print image would require thirty words, rather than twenty-two. In turn (assuming a 920 word track and 165 ms average access), the access time per print image would rise from 4.6 ms, for six-bit characters, to 6.1 ms, for eight-bit characters.

c. In some cases, particularly the FORTRAN compiler, the software would have to be converted from eight-bit to six-bit characters, to achieve the table-packing densities required.

d. A character scan that cannot be word-oriented is necessarily more complex, and, hence, slower.

1.2 The recommended code is the existing 7094 six-bit representation, expanded to a 63-character set.

a. While a six-bit subset of EBCDIC would suffice, it would require a programmed translation to and from 7094 code, when running the 7095 in the 7094-Compatible mode.

1.3 Character-oriented unit record operations will require reciprocal translation between the six-bit internal representation and any eight-bit representation -- the Extended BCD Interchange Code, say. Channels with this facility can operate a 2821 Mod 3 Control Unit. CSC recommends that the 2201 Mod 3 Printer be specified as standard equipment for the IBM 7095. This would not only give improved performance; it would also allow software development to utilize the recommended extended character set.

1.4 For the majority of potential 7095 users, compatibility with 729-produced tapes will be important; thus, the seven-track option must be available, if 2400-series tapes are to be used.

1.5 The six-bit/eight-bit translation discussed in Paragraph 1.3 will suffice for communication external to the computer, but will not be satisfactory for internal storage, since the transfer rate is necessarily slower.

1.6 Two distinct modes of operation with 9-track tapes are identifiable: working with multiples of 36 bits, and working with multiples of eight-bits; the former is, of course, the normal case for the 7095. The latter is required only if interchange of tapes between the 7095 and SYSTEM/360 is required, for which the six-bit/eight-bit translation is inadequate (e.g., for binary information or for character sets with more than 64 characters). These two modes may be selected by single bit -- say, bit 12 -- of a channel command. This bit should specify that, if word byte boundaries do not match, the channel will either stop transmission at a natural boundary of the transmitting equipment, and fill with zeros to the natural boundary of the equipment; or it will stop transmission at the natural

boundary of the receiving equpment, and truncate the information coming from the transmitting equipment. Thus, when processing information expressed in multiples of 36 bits, standard procedure would be to fill during output, and truncate during input; conversely, when processing information expressed in multiples of eight bits, standard procedure would be to truncate during output and fill during input. In this latter instance, any SYSTEM/360 tape could be properly read by the 7095, and a 7095 tape could be read by SYSTEM/360. It would not be possible to produce an arbitrary number of bytes on a 7095 output tape, because a record written from N words is necessarily $\left\lceil \frac{36N}{8} \right\rceil$ bytes long. There is probably little need to produce an arbitrary SYSTEM/360 tape; the attendant hardware complications and cost would undoubtedly be excessive.

Disk and drum equipment may be treated in the same manner as tape, in regard to word-byte manipulation. The read-fill/write-truncate mode (8-bit orientation) would be unnecessary, unless shared-file and disk-pack or data-cell interchangeability are major criteria.

2. 7094 COMPATIBILITY

2.1 It is recommended that, when the 7095 is operating in the 7094 mode, the program counter start at (actual) 0100000. Thus the effective memory in 7094 mode is the second bank of core storage.

2.2 If this scheme were not adopted, any trapping in either mode could destroy received code generated for use in the opposite mode. With the adoption of this feature, any 7094 program, whether written in IBSYS or not, would run.

2.3 Input/Output operations would trap to lower core.

2.4 CPU traps in the 7094-compatible mode should also trap to lower core, with the three-word store; this is the recommended approach, but traps relative to 0100000 (in normal 7094 fashion) would be only slightly less desirable.

3. CPU TRAP LOCATIONS

3.1 It is felt that the CPU trap locations can be simplified, as indicated in paragraph 3.5.5 on page 19.

3.2 The effective address should always be computed and stored.

3.3 It would be useful if the Monitor Call location were the last "special" cell, as it should get the most traffic.

4. MODE STATUS

4.1 Monitor coding is simplified if the mode switches are set as indicated:

a. Monitor Mode - off
b. 7095 Mode - off
c. Non-trapping Mode - off

5. BULK CORE CHANNELS

5.1 Bulk core channels are not yet described

6. WORD FORMAT

6.1 The instruction word format has been altered, inserting the OP field between T2 and Y. Thus an indirect address word can address twenty-seven bit addresses in bulk core.

7. DATA CHANNEL MEMORY PROTECT VIOLATION

7.1 When a memory protect violation occurs while storing, during a data channel read, a data channel trap must occur.

7.2 This is an Unusual End Trap, and is always enabled.

7.3 A bit has been added to the Channel Status field of the third word, in which this violation can be flagged.

8. CPU INSTRUCTION SET

8.1 Several instructions have been recommended for the 7095 to complete the symmetry of the instruction set. Symmetry generally simplifies programming, and, to some extent, increases performance; additionally -- and, perhaps most important, when instructions are generated by a compiler, the performance of the compiler can be upgraded, and its complexity reduced, if the instruction set used for generation is symmetrical.

8.2 Since integer usage in programming systems is now generally full-word, it is recommended that the instructions corresponding to the 7094 instructions PDX, PDC, PCD, and PXD be omitted from the 7095 set.

8.3 Because the instruction SLQ is a remnant from the 701, and can be of little value in 7095 operations, its retention is not recommended for the 7095 set.

8.4 The utility of the instructions SPT (Storage Plus Test) and SMT (Storage Minus Test) has been demonstrated on the 7040/44 computers; their inclusion in the 7095 set is, therefore, strongly recommended.

8.5 Since one of the more important uses of the 7095 will be as an information processing machine, inclusion of the instructions ALX, SLX, and CLX is recommended, to provide the symmetry necessary for efficient list processing.

8.6 It is recommended that the use of the instructions HTR and HPR be prohibited in Problem Program Mode, and that all unassigned operation codes cause a Prohibited Instruction Trap, whether in Problem Program Mode, or in Monitor Mode.

8.7 The inclusion in the 7095 Instruction Set of the instructions XLS (Index Left Shift) and XRS (Index Right Shift) is recommended to enhance the utility of the QXS, QXT, XAS, XAT instructions and to improve the table-searching capability of the 7095.

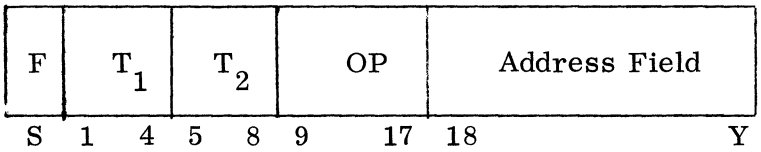
IV. ADDITIONS TO "7095 FUNCTIONAL OBJECTIVES"

The following additional passages, if inserted according to their paragraph numbers into "7095 FUNCTIONAL OBJECTIVES" (dated 3/17/64, Revision 1, as modified by Revision 2, dated 4/7/64) will clarify the text of this document appreciably.

In all cases, instruction names and mnemonics should conform to the 7095 instruction set specifications.

Insert Paragraph 2.2

The word format should be changed to the following:



This permits indirect addressing of addresses of twenty-seven bits each. This format change applies to all instruction diagrams in this report.

Insert Paragraph 3.2.5

If a storage protect violation occurs during transmission from a data channel, the channel traps to the Unusual End position, and an indicator is set, marking the memory protect violation; the channel then disconnects. Thus, an SCH instruction will show the specific violation.

Insert Paragraph 3.3.1

The Restricted Instruction Lists are as follows:

1. Always restricted to Monitor Mode operation:
   - a. SMP Set Memory Protect
   - b. IHC Inhibit Channel Traps
   - c. PTR Processor Trap Return

d. SCA Set Channel Assignment Register

e. ECH Enable Channel Traps

f. HTR Halt and Trap

g. HPR Halt and Proceed

2. Permitted in Problem Program Mode only on channels marked (see 3.3.2) as non-restricted:

a. CST Channel Start or Test

b. CHT Channel Test

c. SCH Store Channel

d. HCH Halt Channel

e. CTR Channel Trap Return

Insert Paragraph 3.5.2

All CPU traps store the Program Location Counter + 1 in fixed cell X1; the effective address in fixed cell X2; and status information (spill, mode, 7094 Input/Output Operation code) in fixed cell X3. Control is then transferred to one of five fixed locations.

Insert Paragraph 3.5.4

The mode status contains three bits:

1. Monitor Mode Off, Problem Program Mode On

2. 7095 Mode Off, 7094 Mode On

3. Non-trapping Mode Off, ETM On

This state of the switches facilitates Monitor coding.

Insert Paragraph 3.5.5

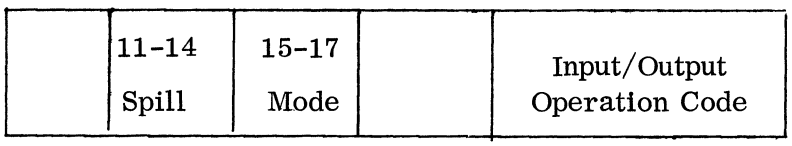
CPU TRAP LOCATIONS

Type of Trap	Transfer Address	Return Address	Effective Address	Status
Floating Point or Divide Check	X4	X1	X2	X3
Protect Violation or Restricted Operation or STR (in 7094 Mode)	X5	X1	X2	X3
Input/Output in Compatibility Mode	X6	X1	X2	X3
Transfer Trap	X7	X1	X2	X3
Monitor Call	X8	X1	X2	X3

Return Address

Effective Address

Status



Insert Paragraph 3.5A

7094-7095 Compatibility

3.5A.1 The computer enters 7094 Compatible Mode when the Processor Trap Return instruction refers to a mode word with the 7094 bit set. When in this mode, the Program Counter refers to the second bank of core; thus the second bank of 7095 core acts like a 7094, in the 7094-Compatible Mode.

3.5A.2 Any 7094 Input/Output instructions trap to lower core, and then enter Monitor Mode.

3.5A.3 7094 CPU traps (STR, for example) trap to lower core with the 7095 word store, and then change to Monitor Mode.

Insert Paragraph 3.6.17A (Modifies Paragraphs 3.6.18, 3.6.19, 3.6.20, 3.6.21, i.e., No. 10 of Revision 2)

When performing an Add or Subtract from Index, one of the three comparison indicators is always set based on a comparison with zero. If the result of the operation is zero, the "Equal" indicator is set; if the operation causes overflow (or underflow), the "Less Than" indicator is set; otherwise the "Greater Than" indicator is set.

Insert Paragraph 3.6.75 (Change)

Transfer on Index (TIX)

If the X(T1) are greater than 1, the X(T1) are replaced by X(T1) - 1, and the next instruction is taken from location Y. If the X(T1) are less than, or equal to, 1, the X(T1) are unchanged, and the next sequential instruction follows.

Insert Paragraph 3.6.81

Double Index Load (DXL)

Positions 0-17 of C(Y) replace (T1) and positions 18-35 of C(Y) replace X(T1+1).

Insert Paragraph 3.6.82

Double Index Store (DXS)

X(T1) replaces positions 0-17 of C(Y); X(T1+1) replaces positions 18-35 of C(Y).

Insert Paragraph 3.6.83

Load Masked Positions (LMP)

The positions of the logical AC for which the corresponding position of C(SI) is one are replaced by the corresponding positions of C(Y); Q and S are unchanged.

Insert Paragraph 3.6.84

Add Left Half-Word to Index (ALX)

X(T1) are replaced by X(T1) + $C(Y)_{0-17}$. If the result is zero, the EQUAL comparison indicator is set; if overflow occurs, the LESS THAN comparison indicator is set; otherwise the GREATER THAN comparison indicator is set. Arithmetic is performed modulo 262, 144. If T1 is zero, X(T1) is assumed to be zero, also.

Insert Paragraph 3.6.85

Subtract Left Half-Word From Index (SLX)

X(T1) are replaced by X(T1) - $C(Y)_{0-17}$. If the result is zero, the EQUAL comparison indicator is set; if underflow occurs, the LESS THAN comparison indicator is set; otherwise, the GREATER THAN comparison indicator is set. Arithmetic is performed modulo 262, 144. If T1 is zero, X(T1) is assumed to be zero.

Insert Paragraph 3.6.86

Storage Plus Test (SPT)

If the sign position of the C(Y) is zero, the next sequential instruction is skipped; otherwise, the next sequential instruction follows.

Insert Paragraph 3.6.87

Storage Minus Test (SMT)

If the sign position of the C(Y) is one, the next sequential instruction is skipped; otherwise the next sequential instruction follows.

Insert Paragraph 3.6.88

Compare Index to Left Half-Word (CXL)

The contents of the index register designated by T1 is compared with positions 0-17 of C(Y), and the GREATER THAN, EQUAL, or LESS THAN indicators are set, or not set, accordingly.

Insert Paragraph 3.6.45 (Change)

Transfer and Store Location (TSL)

The contents of the location counter plus one (LC + 1) replace positions 18-35 of C(Y); positions 0-17 of C(Y) are set to zero, and the next instruction is taken from location Y + 1.

Insert Paragraph 3.6.89

Rotate MQ Right (RQR)

The contents of the MQ are rotated right Y positions; bits shifted out of position 35 re-enter in position 0.

Insert Paragraph 3.6.90

Store Index in Full Word (SXS)

X(T1) replace $C(Y)_{18-35}$, and $C(Y)_{0-17}$ are set to zero. If T1 is zero, $C(Y)_{18-35}$ are set to zero.

Insert Paragraph 3.6.91

Store Index Complement in Full Word (SCS)

The complement of X(T1) replaces $C(Y)_{18-35}$, and $C(Y)_{0-17}$ are set to zero. If T1 is zero, $C(Y)_{18-35}$ are set to zero.

Insert Paragraph 3.6.92

Subtract One from Storage (SOS)

The C(Y) are replaced by the C(Y) -1. No overflow indication is given.

Insert Paragraph 3.6.93

Transfer on No Index (TNX)

If the X(T1) are greater than 1, the X(T1) are replaced by X(T1) - 1 and the next sequential instruction follows. If the X(T1) are less than, or equal to, 1, the X(T1) are unchanged, and the next instruction is taken from location Y.

Insert Paragraph 3.6.94

Index Left Shift (XLS)

The X(T1) are shifted left Y positions. Bits shifted out of the index register are lost. Zeroes are introduced in the Y-vacated positions.

Insert Paragraph 3.6.95

Index Right Shift (XRS)

The X(T1) are shifted right Y positions. Bits shifted out of the index register are lost. Zeroes are introduced in the Y-vacated positions.

Insert Paragraph 3.6.96

Call Monitor (MTR)

Mode status and program location counter are stored in trap locations. The system is placed in 7095, Monitor, and No Transfer Trap Mode, and the effective address of Y is stored in a trap location.

Insert Paragraph 3.6.97

Transfer, Store Location, Zeroed (TSS)

Control goes to location Y + 1. The location counter plus one is stored in bits 18-35 of Y. Positions S, 1-17 of Y are set to zero.

Delete Paragraph 3.7.13

Delete Paragraph 3.7.15

Insert Paragraph 3.7.23

Store Location and Trap (STR)

Insert Paragraph 3.8.3

7095 Multiplication and Division Instructions operate differently from their 7094 counter parts. All 7095 Multiplication Instructions assume that the multiplier is to be in the AC, rather than in the MQ, and all Division Instructions place the quotient in the AC, and the remainder in the MQ -- rather than vice-versa, as in the 7094.

V. ADDITIONS TO 7095 DATA CHANNEL FUNCTIONAL OBJECTIVES

The following passages are to be inserted, according to paragraph number, into "7095 DATA CHANNEL FUNCTIONAL OBJECTIVES", Revision 3, dated April 10, 1964. This insertion will clarify the document's contents appreciably.

Insert Paragraph 3.1

Channel Commands

Pos 12 (replace)

On 7095 Orientation

Off System/360 Orientation

Pos 15 (insert)

When a channel disconnects, either by this control or by an unusual End trap, the following registers are preserved:

a. Command Counter

b. Word Counter

c. Data Address Register

Insert Before the Operations Summary

Mode Flags, bits 12, 13, 14

The 7095 is a thirty-six-bit word machine, and is oriented to a six-bit character. NPL equipment is oriented to an eight-bit character. To provide the necessary communication, these situations are recognized:

000 Input--nine-track operation, eight-bit orientation. Where eight-bit frames do not fill the last word, it is filled with zeros.

Output--nine-track operation, eight-bit orientation. Where specified words do not satisfy eight-bit frame requirements, information is lost. In other words, the external medium governs.

001 Nine-track operation, character translation. (Six-bit internal characters mapped into eight-bit external representation, thus permitting 64 characters in the set normally used by the 7095.)

010 Seven-track operation, binary information.

011 Seven-track operation, BCD translation. This provides for 729 tapes, etc.

100 Input--nine-track operation, 36-bit orientation. Where eight bit frames do not fill the last word, the last frame is truncated. Output--nine-track operation, 36-bit orientation. Where 36 bit words do not fill eight bit frames, the last frame is filled with zeros. This will be the normal mode for processing binary information.

NOTE: Control Unit Operations

Control cannot have the indirect address flag.

The description of Command Operations is to be augmented by the following:

WRITE	Modifier bits are interpreted by the Control Unit; this must have a DCW following.
READ	Modifier bits are interpreted by the Control Unit; this must have a DCW following.
READ BACKWARD	Modifier bits are interpreted by the Control Unit; this must have a DCW following.
SENSE	SENSE, M A/D Modifier bits M are interpreted by the Control Unit and refer to specific NPL equipment.

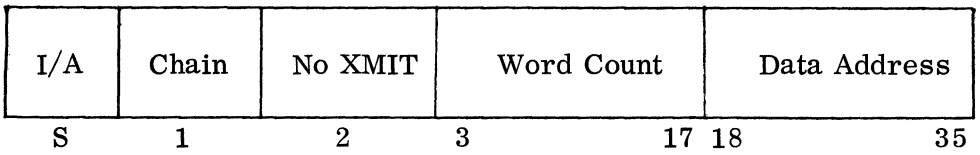
CONTROL - CNTL M. A/D,IMM

Modifier bits M are interpreted by the Control Unit, and refer to specific NPL equipment. If IMM is specified, the control information is in bits 4-9 of the control command. If IMM is not specified, a DCW is required. This command passes to auxiliary equipment such commands as SEEK (1301, two words), EJECT, REWIND.

Insert Paragraph 3.2

Data Control Word

The format is to be changed to place the I/A flag in position S.



Insert Under Data Control Word Operations

Data control words follow their respective commands--i.e., they are under the same program counter. Where the external medium is such that some DCW's are not used on return to an ADVANCE command--on a short record, for example--the Incorrect Length trap is taken, and the channel is disconnected, if this action has been enabled.

Positions S, 1 and 2 are coded to provide the following Data Control Word operations:

Mnemonic Code	Operation	Octal Operation Code
TCW	Terminate control word	0
TCWN	Terminate control word non-transmit	1
TCW*	Terminate control word I/A	4
CCW	Chain control word	2
CCWN	Chain control word non-transmit	3
CCW*	Chain control word I/A	6

Insert into Description

Terminate Control Word Non-Transmit TCWN, Y, C

Data transmission is suppressed for C-words, unless an END is received from the Control Unit. It then terminates.

Insert Paragraph 3.3

Channel Trap

(Replace conditions 1 and 2.)

1. End Trap--A trap will occur if the channel is free of any error, or is free of unusual conditions at the completion of a command which does not have the Channel Advance bit On.
2. Unusual End Trap--A trap will be caused when one of the following unusual conditions appears at the completion of a command:
   a. Data Error
   b. Exceptional Condition (End of File, etc.)
   c. Intervention Required
   d. Incorrect Length
   e. Memory Protect Violation

   Enable trap bits required - Unusual End (a, b, c)
   Incorrect Length (d)

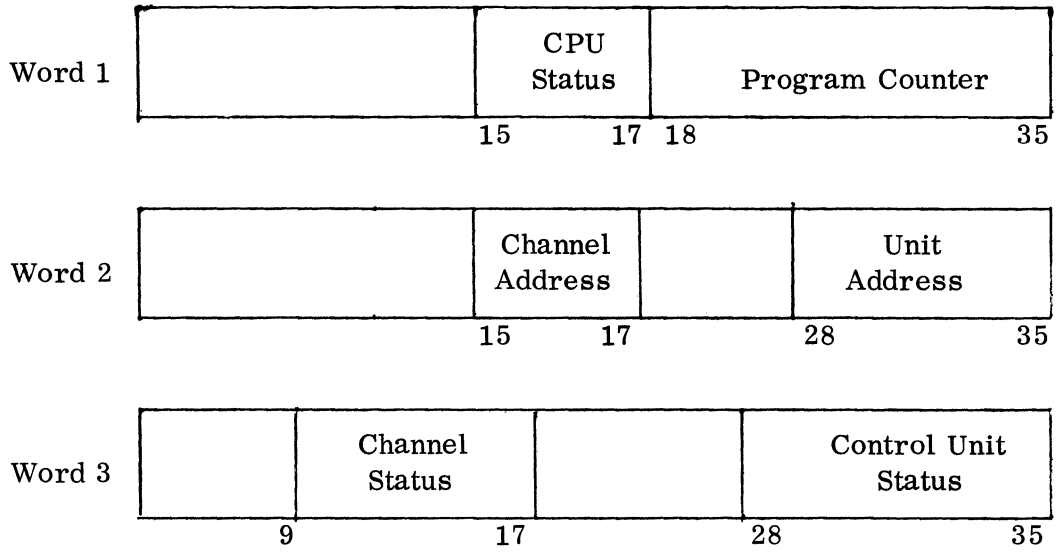
If the Channel Advance bit is On in the current command, the channel will be disconnected only if an Unusual End occurs.

Attention Trap 2 - Chain Trap

The trap occurs when the current DCW chain bit is on, and the word count has reached zero causing access of the next DCW.

Insert Paragraph 3.4.6

Each channel trap will perform a three-word store. The format is as follows:



Entries in Word 1.

CPU Status

a) Monitor Mode - Problem Program

b) 7094-7095

c) Non-trapping mode - trapping mode

Program Counter - CPU

Entries in Word 2.

Channel Address

Unit Address

Entries in Word 3

Channel Status - 9 bits; the type of trap is indicated, and can be one of the following three types:

a) Normal end

b) Unusual end--one of the following types:

1) Data error

2) Exceptional condition

3) Intervention Required

4) Incorrect Length

5) Memory Protect

c) Attention Trap--one of the following types:

1) Immediate

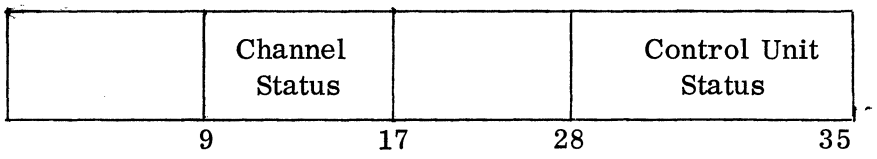
2) Not in Use

3) Chain

Control Unit Status

Insert Paragraph 3.4.1

An STC Instruction, issued in Problem Program Mode, the inhibit bit (S of the CSW) will be set Off.

Insert Paragraph 3.4.2

The format of the status in X is the third word of a Data Channel trap: