SATURN V

Simplex Models

Laboratory Maintenance Instructions for LVDC

Volume II

Maintenance Data

Space Guidance Center, Owego, New York IBM

VOLUME II OF II

Laboratory Maintenance Instructions

SATURN V
LAUNCH VEHICLE DIGITAL COMPUTER

Simplex Models

NASA Part No. 50M35010

IBM Part No. 6109030

(International Business Machines Corporation)

Contract NAS 8-11561

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3-2. Figure 3-1 shows the connector interface by function and the direction of signal flow relative to the computer. Figure 3-2 lists the computer interface signal names and functions alphabetically by connector number. Figure 3-3 is a functional block diagram which shows the interconnection of groups of similar signals between the computer and the data adapter. Figure 3-4 shows the interconnection of groups of similar signals between the computer and the LVDC-ME. Figure 3-5 shows the interconnection of groups of similar signals between the computer and the ATOM.

NOTE

All the channel reference designations (A1 through A3) have been left off the functional signal names in all diagrams in this section.

3-3. ADJUSTMENTS

3-4. No adjustments are made on the computer.

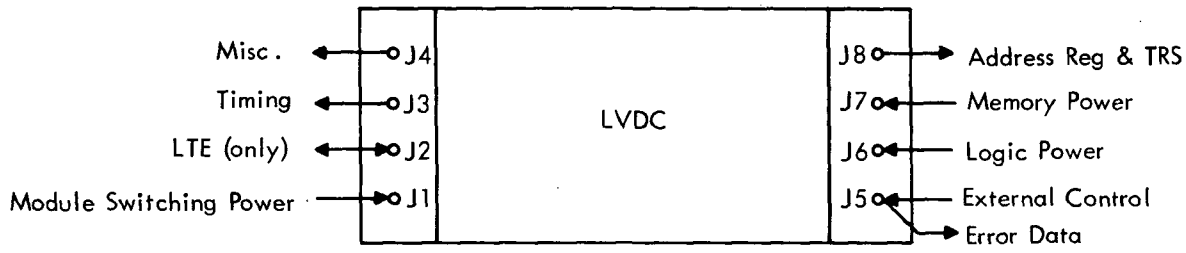


Figure 3-1. Computer Connectors By Signal Function

NAME	CONNECTOR	PIN	FUNCTION
*A1V4M1	J1	HH	CHANNEL 1, 6 VDC, MODULE 1 SWITCHING
*A2V4M1	J1	J	CHANNEL 2, 6 VDC, MODULE 1 SWITCHING
*A3V4M1	J1	FF	CHANNEL 3, 6 VDC, MODULE 1 SWITCHING
*A1V4M2	J1	BB	CHANNEL 1, 6 VDC, MODULE 2 SWITCHING
*A2V4M2	J1	¤E	CHANNEL 2, 6 VDC, MODULE 2 SWITCHING
*A3V4M2	J1	¤W	CHANNEL 3, 6 VDC, MODULE 2 SWITCHING
*A1V4M3	J1	AA	CHANNEL 1, 6 VDC, MODULE 3 SWITCHING
*A2V4M3	J1	¤F	CHANNEL 2, 6 VDC, MODULE 3 SWITCHING
*A3V4M3	J1	¤I	CHANNEL 3, 6 VDC, MODULE 3 SWITCHING
*A1V4M4	J1	CC	CHANNEL 1, 6 VDC, MODULE 4 SWITCHING
*A2V4M4	J1	¤G	CHANNEL 2, 6 VDC, MODULE 4 SWITCHING
*A3V4M4	J1	EE	CHANNEL 3, 6 VDC, MODULE 4 SWITCHING
*A1V4M5	J1	¤Q	CHANNEL 1, 6 VDC, MODULE 5 SWITCHING
*A2V4M5	J1	¤D	CHANNEL 2, 6 VDC, MODULE 5 SWITCHING
*A3V4M5	J1	¤V	CHANNEL 3, 6 VDC, MODULE 5 SWITCHING
*A1V4M6	J1	GG	CHANNEL 1, 6 VDC, MODULE 6 SWITCHING
*A2V4M6	J1	K	CHANNEL 2, 6 VDC, MODULE 6 SWITCHING
*A3V4M6	J1	¤U	CHANNEL 3, 6 VDC, MODULE 6 SWITCHING
*A1V4M7	J1	¤Y	CHANNEL 1, 6 VDC, MODULE 7 SWITCHING
*A2V4M7	J1	¤Y	CHANNEL 2, 6 VDC, MODULE 7 SWITCHING
*A3V4M7	J1	DD	CHANNEL 3, 6 VDC, MODULE 7 SWITCHING
*A1V5M1	J1	Y	CHANNEL 1, 12 VDC, MODULE 1 SWITCHING
*A2V5M1	J1	¤T	CHANNEL 2, 12 VDC, MODULE 1 SWITCHING
*A3V5M1	J1	¤P	CHANNEL 3, 12 VDC, MODULE 1 SWITCHING
*A1V5M2	J1	¤R	CHANNEL 1, 12 VDC, MODULE 2 SWITCHING
*A2V5M2	J1	G	CHANNEL 2, 12 VDC, MODULE 2 SWITCHING
*A3V5M2	J1	V	CHANNEL 3, 12 VDC, MODULE 2 SWITCHING
*A1V5M3	J1	C	CHANNEL 1, 12 VDC, MODULE 3 SWITCHING
*A2V5M3	J1	¤C	CHANNEL 2, 12 VDC, MODULE 3 SWITCHING
*A3V5M3	J1	W	CHANNEL 3, 12 VDC, MODULE 3 SWITCHING
*A1V5M4	J1	H	CHANNEL 1, 12 VDC, MODULE 4 SWITCHING
*A2V5M4	J1	H	CHANNEL 2, 12 VDC, MODULE 4 SWITCHING
*A3V5M4	J1	A	CHANNEL 3, 12 VDC, MODULE 4 SWITCHING
*A1V5M5	J1	¤S	CHANNEL 1, 12 VDC, MODULE 5 SWITCHING
*A2V5M5	J1	¤A	CHANNEL 2, 12 VDC, MODULE 5 SWITCHING
*A3V5M5	J1	¤N	CHANNEL 3, 12 VDC, MODULE 5 SWITCHING
*A1V5M6	J1	D	CHANNEL 1, 12 VDC, MODULE 6 SWITCHING
*A2V5M6	J1	F	CHANNEL 2, 12 VDC, MODULE 6 SWITCHING
*A3V5M6	J1	T	CHANNEL 3, 12 VDC, MODULE 6 SWITCHING
*A1V5M7	J1	Z	CHANNEL 1, 12 VDC, MODULE 7 SWITCHING
*A2V5M7	J1	¤B	CHANNEL 2, 12 VDC, MODULE 7 SWITCHING
*A3V5M7	J1	U	CHANNEL 3, 12 VDC, MODULE 7 SWITCHING
INTRLK	J1	N	LTE INTERLOCK FOR LTE USE ONLY
INTRLK	J1	P	LTE INTERLOCK FOR LTE USE ONLY
SR01	J1	E	SIGNAL RETURN, LINE 01 A2V5M1-A2V5M7
SR02	J1	M	SIGNAL RETURN, LINE 02 A2V4M1-A2V4M7
SR03	J1	X	SIGNAL RETURN, LINE 03 A1V5M1-A1V5M7
SR04	J1	¤M	SIGNAL RETURN, LINE 04 A3V5M1-A3V5M7
SR05	J1	¤X	SIGNAL RETURN, LINE 05 A3V4M1-A3V4M7
SR06	J1	¤Z	SIGNAL RETURN, LINE 06 A1V4M1-A1V4M7
SPARE	J1	R	
SPARE	J1	S	
SPARE	J1	¤H	
SPARE	J1	¤J	
SPARE	J1	¤K	

NOTE *DENOTES INPUTS TO COMPUTER, ¤INDICATES LOWER CASE LETTER

Figure 3-2. Computer Interface Signals (Sheet 1 of 8)

NAME	CONNECTOR	PIN	FUNCTION
*A1CSTN	J2	□K	CHANNEL 1, SINGLE STEP CONTROL
*A2CSTN	J2	E	CHANNEL 2, SINGLE STEP CONTROL
*A3CSTN	J2	K	CHANNEL 3, SINGLE STEP CONTROL
*A1DIN	J2	□M	CHANNEL 1, MEMORY LOAD
*A2DIN	J2	□A	CHANNEL 2, MEMORY LOAD
*A3DIN	J2	L	CHANNEL 3, MEMORY LOAD
A1HOPC1V	J2	R	CHANNEL 1, HOP CONSTANT
A2HOPC1V	J2	HH	CHANNEL 2, HOP CONSTANT
A3HOPC1V	J2	□I	CHANNEL 3, HOP CONSTANT
*A1MCL	J2	□C	CHANNEL 1, MARGINAL CHECK LATE, STROBE CONTROL
*A2MCL	J2	D	CHANNEL 2, MARGINAL CHECK STROBE CONTROL
*A1MCN	J2	U	CHANNEL 1, MARGINAL CHECK STROBE CONTROL
*A2MCN	J2	CC	CHANNEL 2, MARGINAL CHECK STROBE CONTROL
A1MD7V	J2	□H	CHANNEL 1, MULTIPLICAND DIVISOR REGISTER LATCH 7
A2MD7V	J2	N	CHANNEL 2, MULTIPLICAND DIVISOR REGISTER LATCH 7
A3MD7V	J2	M	CHANNEL 3, MULTIPLICAND DIVISOR REGISTER LATCH 7
A1MR1V	J2	F	CHANNEL 1, MULTIPLIER REGISTER LATCH
A2MR1V	J2	□T	CHANNEL 2, MULTIPLIER REGISTER LATCH
A3MR1V	J2	□U	CHANNEL 3, MULTIPLIER REGISTER LATCH
A1OP1V	J2	J	CHANNEL 1, OPERATION CODE REGISTER LATCH 1
A2OP1V	J2	H	CHANNEL 2, OPERATION CODE REGISTER LATCH 1
A3OP1V	J2	G	CHANNEL 3, OPERATION CODE REGISTER LATCH 1
A1OP2V	J2	B	CHANNEL 1, OPERATION CODE REGISTER LATCH 2
A2OP2V	J2	C	CHANNEL 2, OPERATION CODE REGISTER LATCH 2
A3OP2V	J2	A	CHANNEL 3, OPERATION CODE REGISTER LATCH 2
A1OP3V	J2	□P	CHANNEL 1, OPERATION CODE REGISTER LATCH 3
A2OP3V	J2	Z	CHANNEL 2, OPERATION CODE REGISTER LATCH 3
A3OP3V	J2	□X	CHANNEL 3, OPERATION CODE REGISTER LATCH 3
A1OP4	J2	S	CHANNEL 1, OPERATION CODE REGISTER LATCH 4
A2OP4V	J2	□S	CHANNEL 2, OPERATION CODE REGISTER LATCH 4
A3OP4V	J2	□G	CHANNEL 3, OPERATION CODE REGISTER LATCH 4
A1PROV	J2	□D	CHANNEL 1, PRODUCT REMAINDER LATCH
A2PROV	J2	□V	CHANNEL 2, PRODUCT REMAINDER LATCH
A3PROV	J2	EE	CHANNEL 3, PRODUCT REMAINDER LATCH
*A1TER	J2	W	CHANNEL 1, RESET MEMORY ERROR INDICATION
*A2TER	J2	□E	CHANNEL 2, RESET MEMORY ERROR INDICATION
*A3TER	J2	□W	CHANNEL 3, RESETS MEMORY ERROR INDICATION
BRA14P	J2	DD	BUFFER REGISTER A, PARITY BIT
BRB14P	J2	□B	BUFFER REGISTER B PARITY BIT
INTRLK	J2	□Y	LTE INTERLOCK FOR LTE USE ONLY
INTRLK	J2	□Z	LTE INTERLOCK FOR LTE USE ONLY
SIGRET	J2	P	SIGNAL RETURN, DC REGULATED
SIGRET	J2	X	SIGNAL RETURN, DC REGULATED
SIGRET	J2	Y	SIGNAL RETURN, DC REGULATED
SIGRET	J2	BB	SIGNAL RETURN, REGULATED DC
SIGRET	J2	FF	SIGNAL RETURN, REGULATED DC
SPARE	J2	T	
SPARE	J2	V	
SPARE	J2	□F	
SPARE	J2	□J	
SPARE	J2	□N	
SPARE	J2	□Q	
SPARE	J2	□R	
SPARE	J2	AA	
SPARE	J2	GG	

NOTE *DENOTES INPUTS TO COMPUTER, □INDICATES LOWER CASE LETTER

Figure 3-2. Computer Interface Signals (Sheet 2)

NAME	CONNECTOR	PIN	FUNCTION
A1G5VN	J3	C	CHANNEL 1, TIMING SYNC FOR DATA ADAPTER
A2G5VN	J3	¤Y	CHANNEL 2, TIMING SYNC FOR DATA ADAPTER
A3G5VN	J3	¤P	CHANNEL 3, TIMING SYNC FOR DATA ADAPTER
A1PBVN	J3	¤S	CHANNEL 1, TIMING SYNC FOR DATA ADAPTER
A2PBVN	J3	¤A	CHANNEL 2, TIMING SYNC FOR DATA ADAPTER
A3PBVN	J3	R	CHANNEL 3, TIMING SYNC FOR DATA ADAPTER
A1WDA	J3	¤B	CHANNEL 1, TIMING SYNC FOR DATA ADAPTER
A2WDA	J3	K	CHANNEL 2, TIMING SYNC FOR DATA ADAPTER
A3WDA	J3	N	CHANNEL 3, TIMING SYNC FOR DATA ADAPTER
A1XDA	J3	F	CHANNEL 1, TIMING SYNC FOR DATA ADAPTER
A2XDA	J3	J	CHANNEL 2, TIMING SYNC FOR DATA ADAPTER
A3XDA	J3	HH	CHANNEL 3, TIMING SYNC FOR DATA ADAPTER
A1YDA	J3	H	CHANNEL 1, TIMING SYNC FOR DATA ADAPTER
A2YDA	J3	¤H	CHANNEL 2, TIMING SYNC FOR DATA ADAPTER
A3YDA	J3	¤K	CHANNEL 3, TIMING SYNC FOR DATA ADAPTER
A1ZDA	J3	G	CHANNEL 1, TIMING SYNC FOR DATA ADAPTER
A2ZDA	J3	M	CHANNEL 2, TIMING SYNC FOR DATA ADAPTER
A3ZDA	J3	¤J	CHANNEL 3, TIMING SYNC FOR DATA ADAPTER
BO1N	J3	DD	2.048 MC TIMING
BO2N	J3	¤F	2.048 MC TIMING
BO3N	J3	¤V	2.048 MC TIMING
INTRLK	J3	W	LTE INTERLOCK FOR LTE USE ONLY
INTRLK	J3	X	LTE INTERLOCK FOR LTE USE ONLY
SR07	J3	E	SIGNAL RETURN, LINE 07-A1XDA
SR08	J3	L	SIGNAL RETURN, LINE 08-A2WDA
SR09	J3	P	SIGNAL RETURN, LINE 09-A3PBVN
SR10	J3	S	SIGNAL RETURN, LINE 10-A3YDA
SR11	J3	Z	SIGNAL RETURN, LINE 11-A2PBVN
SR12	J3	¤C	SIGNAL RETURN, LINE 12-A1ZDA
SR13	J3	¤D	SIGNAL RETURN, LINE 13-A1YDA
SR14	J3	¤E	SIGNAL RETURN, LINE 14-A2XDA
SR15	J3	¤G	SIGNAL RETURN, LINE 15-A2ZDA
SR16	J3	¤I	SIGNAL RETURN, LINE 16-A3WDA
SR17	J3	¤N	SIGNAL RETURN, LINE 17-A3G5VN
SR18	J3	¤R	SIGNAL RETURN, LINE 18-A1G5N
SR19	J3	¤T	SIGNAL RETURN, LINE 19-A1WDA
SR20	J3	¤U	SIGNAL RETURN, LINE 20-BO1N
SR21	J3	¤W	SIGNAL RETURN, LINE 21-BO2N
SR22	J3	¤X	SIGNAL RETURN, LINE 22-A2YDA
SR23	J3	¤Z	SIGNAL RETURN, LINE 23-A3ZDA
SR24	J3	CC	SIGNAL RETURN, LINE 24-A3XDA
SR25	J3	EE	SIGNAL RETURN, LINE 25-BO3N
SR26	J3	FF	SIGNAL RETURN, LINE 26-A3XDA
SR27	J3	GG	SIGNAL RETURN, LINE 27-A2G5VN
SPARE	J3	A	
SPARE	J3	B	
SPARE	J3	D	
SPARE	J3	T	
SPARE	J3	U	
SPARE	J3	V	
SPARE	J3	Y	
SPARE	J3	¤M	
SPARE	J3	¤Q	
SPARE	J3	AA	
SPARE	J3	BB	

NOTE *DENOTES INPUTS TO COMPUTER, ¤INDICATES LOWER CASE LETTER

Figure 3-2. Computer Interface Signals (Sheet 3)

NAME	CONNECTOR	PIN	FUNCTION
A1AI3V	J4	¤M	CHANNEL 1, ACCUMULATOR THIRD DELAY LATCH
A2AI3V	J4	¤Z	CHANNEL 2, ACCUMULATOR THIRD DELAY LATCH
A3AI3V	J4	¤Q	CHANNEL 3, ACCUMULATOR THIRD DELAY LATCH
A1PIOV	J4	GG	CHANNEL 1, PROCESS INPUT-OUTPUT
A2PIOV	J4	U	CHANNEL 2, PROCESS INPUT-OUTPUT
A3PIOV	J4	U	CHANNEL 3, PROCESS INPUT-OUTPUT
EP01	J4	W	ERROR SIGNAL 01
EP02	J4	¤R	ERROR SIGNAL 02
EP03	J4	T	ERROR SIGNAL 03
EP04	J4	AA	ERROR SIGNAL 04
EP06	J4	V	ERROR SIGNAL 06
EP07	J4	¤N	ERROR SIGNAL 07
INTRLK	J4	¤G	LTE INTERLOCK FOR LTE USE ONLY
INTRLK	J4	¤H	LTE INTERLOCK FOR LTE USE ONLY
SR28	J4	A	SIGNAL RETURN, LINE 28-EP06
SR29	J4	B	SIGNAL RETURN, LINE 29-A1PIOV,A3PIOV
SR30	J4	P	SIGNAL RETURN, LINE 30-A2AI3
SR31	J4	S	SIGNAL RETURN, LINE 31-EP03
SR32	J4	X	SIGNAL RETURN, LINE 32-EP01
SR33	J4	Z	SIGNAL RETURN, LINE 33-THERM 1, THERM 2,
SR34	J4	¤P	SIGNAL RETURN, LINE 34-EP07
SR35	J4	¤S	SIGNAL RETURN, LINE 35-EP02
SR36	J4	BB	SIGNAL RETURN, LINE 36-EP04
SR37	J4	CC	SIGNAL RETURN, LINE 37-A3AI3V
SR38	J4	HH	SIGNAL RETURN, LINE 38-A1AI3V
THERM1	J4	Y	THERMISTOR 1 LEAD 1
THERM2	J4	D	THERMISTOR 1 LEAD 2
SPARE	J4	E	
SPARE	J4	F	
SPARE	J4	G	
SPARE	J4	H	
SPARE	J4	J	
SPARE	J4	K	
SPARE	J4	L	
SPARE	J4	M	
SPARE	J4	N	
SPARE	J4	R	
SPARE	J4	¤A	
SPARE	J4	¤B	
SPARE	J4	¤C	
SPARE	J4	¤D	
SPARE	J4	¤E	
SPARE	J4	¤F	
SPARE	J4	¤I	
SPARE	J4	¤J	
SPARE	J4	¤K	
SPARE	J4	¤T	
SPARE	J4	¤U	
SPARE	J4	¤V	
SPARE	J4	¤W	
SPARE	J4	¤X	
SPARE	J4	¤Y	
SPARE	J4	DD	
SPARE	J4	EE	
SPARE	J4	FF	

NOTE *DENOTES INPUTS TO COMPUTER, ¤INDICATES LOWER CASE LETTER

Figure 3-2. Computer Interface Signals (Sheet 4)

NAME	CONNECTOR	PIN	FUNCTION
A1EAMV	J5	¤P	CHANNEL 1, EVEN MEMORY ERROR
A2EAMV	J5	¤Z	CHANNEL 2, EVEN MEMORY ERROR
A3EAMV	J5	AA	CHANNEL 3, EVEN MEMORY ERROR
A1EBMV	J5	U	CHANNEL 1, ODD MEMORY ERROR
A2EBMV	J5	¤J	CHANNEL 2, ODD MEMORY ERROR
A3EBMV	J5	¤K	CHANNEL 3, ODD MEMORY ERROR
*A1DATAV	J5	R	CHANNEL 1, COMPUTER DATA INPUT
*A2DATAV	J5	GG	CHANNEL 2, COMPUTER DATA INPUT
*A3DATAV	J5	¤B	CHANNEL 3, COMPUTER DATA INPUT
*A1HALTV	J5	P	CHANNEL 1, HALT SIGNAL
*A2HALTV	J5	A	CHANNEL 2, HALT SIGNAL
*A3HALTV	J5	G	CHANNEL 3, HALT SIGNAL
*A1INTCV	J5	N	CHANNEL 1, INTERRUPT COMPUTER
*A2INTCV	J5	FF	CHANNEL 2, INTERRUPT COMPUTER
*A3INTCV	J5	¤C	CHANNEL 3, INTERRUPT COMPUTER
A1TLCV	J5	T	CHANNEL 1, SIMULTANEOUS MEMORY ERROR
A2TLCV	J5	S	CHANNEL 2, SIMULTANEOUS MEMORY ERROR
A3TLCV	J5	¤I	CHANNEL 3, SIMULTANEOUS MEMORY ERROR
EP05	J5	H	ERROR SIGNAL 05
EP08	J5	Z	ERROR SIGNAL 08
EP09	J5	¤N	ERROR SIGNAL 09
EP10	J5	V	ERROR SIGNAL 10
EP11	J5	E	ERROR SIGNAL 11
EP12	J5	¤Q	ERROR SIGNAL 12
EP13	J5	BB	ERROR SIGNAL 13
INTRLK	J5	K	LTE INTERLOCK FOR LTE USE ONLY
INTRLK	J5	L	LTE INTERLOCK FOR LTE USE ONLY
SR39	J5	B	SIGNAL RETURN, LINE 39-EP10
SR40	J5	C	SIGNAL RETURN, LINE 40-THERM3,THERM4
SR41	J5	W	SIGNAL RETURN, LINE 41-EP09
SR42	J5	¤A	SIGNAL RETURN, LINE 42-EP11
SR43	J5	¤D	SIGNAL RETURN, LINE 43-EP05
SR44	J5	¤H	SIGNAL RETURN 44-INTC, HALT, TLC, EAM AND EBM
SR45	J5	¤S	SIGNAL RETURN LINE 45-EP08
SR46	J5	¤X	SIGNAL RETURN, LINE 46-DATAV FOR CHANNELS 1, 2, 3
SR47	J5	CC	SIGNAL RETURN, LINE 47-EP13
SR90	J5	¤R	SIGNAL RETURN LINE 90-EP12
THERM4	J5	D	THERMISTOR 2 LEAD 2
THERM3	J5	Y	THERMISTOR 2 LEAD 1
SPARE	J5	F	
SPARE	J5	J	
SPARE	J5	M	
SPARE	J5	X	
SPARE	J5	¤E	
SPARE	J5	¤F	
SPARE	J5	¤G	
SPARE	J5	¤M	
SPARE	J5	¤T	
SPARE	J5	¤U	
SPARE	J5	¤V	
SPARE	J5	¤W	
SPARE	J5	¤Y	
SPARE	J5	DD	
SPARE	J5	EE	
SPARE	J5	HH	

NOTE *DENOTES INPUTS TO COMPUTER, ¤INDICATES LOWER CASE LETTER

Figure 3-2. Computer Interface Signals (Sheet 5)

NAME	CONNECTOR	PIN	FUNCTION
INTRLK	J6	K	LTE INTERLOCK FOR LTE USE ONLY
INTRLK	J6	L	LTE INTERLOCK FOR LTE USE ONLY
SR48	J6	H	SIGNAL RETURN, LINE 48-V1 05
SR49	J6	N	SIGNAL RETURN, LINE 49-V1 21
SR50	J6	P	SIGNAL RETURN, LINE 50-V1 15
SR51	J6	R	SIGNAL RETURN, LINE 51-V1 07
SR52	J6	¤C	SIGNAL RETURN, LINE 52-V1 04
SR53	J6	¤D	SIGNAL RETURN, LINE 53-V1 13
SR54	J6	¤E	SIGNAL RETURN, LINE 54-V1 14
SR55	J6	¤F	SIGNAL RETURN, LINE 55-V1 20
SR56	J6	¤G	SIGNAL RETURN, LINE 56-V1 24
SR57	J6	J	SIGNAL RETURN, LINE 57-V1 06
SR58	J6	¤H	SIGNAL RETURN, LINE 58-V1 23
SR59	J6	¤I	SIGNAL RETURN, LINE 59-V1 22
SR60	J6	¤J	SIGNAL RETURN, LINE 60-V1 16
SR61	J6	¤K	SIGNAL RETURN, LINE 61-V1 08
SR62	J6	¤M	SIGNAL RETURN, LINE 62-V1 01
SR63	J6	¤U	SIGNAL RETURN, LINE 63-V1 12
SR64	J6	¤V	SIGNAL RETURN, LINE 64-V1 19
SR65	J6	¤W	SIGNAL RETURN, LINE 65-V1 18
SR66	J6	¤X	SIGNAL RETURN, LINE 66-V1 17
SR67	J6	¤Y	SIGNAL RETURN, LINE 67-V1 09
SR68	J6	EE	SIGNAL RETURN, LINE 68-V1 17
SR69	J6	FF	SIGNAL RETURN, LINE 69-V1 10
SR70	J6	GG	SIGNAL RETURN, LINE 70-V1 02
SR71	J6	HH	SIGNAL RETURN, LINE 71-V1 03
*V1 01	J6	A	6 VDC, LINE 1
*V1 02	J6	B	6 VDC, LINE 2
*V1 03	J6	C	6 VDC, LINE 3
*V1 04	J6	D	6 VDC, LINE 4
*V1 05	J6	E	6 VDC, LINE 5
*V1 06	J6	F	6 VDC, LINE 6
*V1 07	J6	T	6 VDC, LINE 07
*V1 08	J6	U	6 VDC, LINE 08
*V1 09	J6	V	6 VDC, LINE 09
*V1 10	J6	W	6 VDC, LINE 10
*V1 11	J6	X	6 VDC, LINE 11
*V1 12	J6	Y	6 VDC, LINE 12
*V1 13	J6	Z	6 VDC, LINE 13
*V1 14	J6	¤A	6 VDC, LINE 14
*V1 15	J6	S	6 VDC, LINE 15
*V1 16	J6	¤N	6 VDC, LINE 16
*V1 17	J6	¤P	6 VDC, LINE 17
*V1 18	J6	¤Q	6 VDC, LINE 18
*V1 19	J6	¤R	6 VDC, LINE 19
*V1 20	J6	¤S	6 VDC, LINE 20
*V1 21	J6	¤Z	6 VDC, LINE 21
*V1 22	J6	AA	6 VDC, LINE 22
*V1 23	J6	BB	6 VDC, LINE 23
*V1 24	J6	CC	6 VDC, LINE 24
SPARE	J6	G	
SPARE	J6	M	
SPARE	J6	¤B	
SPARE	J6	¤T	
SPARE	J6	DD	

NOTE *DENOTES INPUTS TO COMPUTER, ¤INDICATES LOWER CASE LETTER

Figure 3-2. Computer Interface Signals (Sheet 6)

NAME	CONNECTOR	PIN	FUNCTION
*ETI-1	J7	E	ELAPSED TIME INDICATOR 1
*ETI-2	J7	F	ELAPSED TIME INDICATOR 2
INTRLK	J7	GG	LTE INTERLOCK FOR LTE USE ONLY
INTRLK	J7	HH	LTE INTERLOCK FOR LTE USE ONLY
SRMEM01	J7	A	MEMORY SIGNAL RETURN, LINE 01-V20BM1
SRMEM02	J7	B	MEMORY SIGNAL RETURN, LINE 02-V3MEM1
SRMEM03	J7	C	MEMORY SIGNAL RETURN, LINE 03-V1MEM1
SRMEM04	J7	D	MEMORY SIGNAL RETURN, LINE 04-V20AM1
SRMEM05	J7	U	MEMORY SIGNAL RETURN, LINE 05-V20BM2
SRMEM06	J7	V	MEMORY SIGNAL RETURN, LINE 06-V3MEM2
SRMEM07	J7	Y	MEMORY SIGNAL RETURN, LINE 07-V5MEM1
SRMEM08	J7	¤B	MEMORY SIGNAL RETURN, LINE 0-V5MEM2
SRMEM09	J7	G	MEMORY SIGNAL RETURN, LINE 09-V20AM2
SRMEM10	J7	¤Q	MEMORY SIGNAL RETURN LINE 10-V1MEM3
SRMEM11	J7	AA	MEMORY SIGNAL RETURN, LINE 11-V1MEM2
SRMEM12	J7	H	
SR73	J7	¤D	SIGNAL RETURN, LINE 73-V5 02
SR75	J7	J	SIGNAL RETURN, LINE 75-V5 01
SR76	J7	M	SIGNAL RETURN, LINE 76-V20 01
SR77	J7	¤G	SIGNAL RETURN, LINE 77-V20 02
SR78	J7	¤I	SIGNAL RETURN, LINE 78-V3 01, V3 02
SR79	J7	¤J	SIGNAL RETURN, LINE 79-V3 03, V3 04
SR80	J7	¤M	SIGNAL RETURN, LINE 80-V3 05, V3 08
SR82	J7	¤X	SIGNAL RETURN, LINE 82-V3 09
SR83	J7	¤Z	SIGNAL RETURN, LINE 83-V3 07,V3 10
SR85	J7	EE	SIGNAL RETURN, LINE 85-V3 06
*V1MEM1	J7	¤R	6 VDC, LINE 01, MEMORY
*V1MEM2	J7	BB	6 VDC, LINE 02, MEMORY
*V1MEM3	J7	CC	6 VDC, LINE 03, MEMORY
*V20AM1	J7	¤A	20 VDC, LINE 1, EVEN MEMORY
*V20BM2	J7	¤N	20 VDC, LINE 02, ODD MEMORY
*V20BM1	J7	W	20 VDC LINE 01 ODD MEMORY
*V20AM2	J7	¤T	20 VDC, LINE 2, EVEN MEMORY
*V20 01	J7	L	20 VDC, LINE 01
*V20 02	J7	¤F	20 VDC, LINE 02
*V3MEM1	J7	X	-3 VDC, LINE 01 MEMORY
*V3MEM2	J7	¤P	-3 VDC, LINE 02, MEMORY
*V3 01	J7	¤H	-3 VDC, LINE 01
*V3 02	J7	N	-3 VDC, LINE 02
*V3 03	J7	P	-3 VDC, LINE 03
*V3 04	J7	R	-3 VDC, LINE 04
*V3 05	J7	S	-3 VDC, LINE 05
*V3 06	J7	¤V	-3 VDC, LINE 06
*V3 07	J7	¤Y	-3 VDC, LINE 07
*V3 08	J7	¤H	-3 VDC, LINE 08
*V3 09	J7	¤W	-3 VDC, LINE 09
*V3 10	J7	FF	-3 VDC, LINE 10
*V5MEM1	J7	Z	12 VDC, LINE 01, MEMORY
*V5MEM2	J7	¤S	12 VDC, LINE 02, MEMORY
*V5 01	J7	K	12 VDC, LINE 01
*V5 02	J7	¤E	12 VDC, LINE 02
SPARE	J7	T	
SPARE	J7	¤C	
SPARE	J7	¤U	
SPARE	J7	DD	

NOTE *DENOTES INPUTS TO COMPUTER, ¤INDICATES LOWER CASE LETTER

Figure 3-2. Computer Interface Signals (Sheet 7)

NAME	CONNECTOR	PIN	FUNCTION
A1A1V	J8	T	CHANNEL 1, OPERAND ADDRESS BIT 1
A2A1V	J8	¤M	CHANNEL 2, OPERAND ADDRESS BIT 1
A3A1V	J8	¤P	CHANNEL 3, OPERAND ADDRESS BIT 1
A1A2V	J8	DD	CHANNEL 1, OPERAND ADDRESS BIT 2
A2A2V	J8	BB	CHANNEL 2, OPERAND ADDRESS BIT 2
A3A2V	J8	AA	CHANNEL 3, OPERAND ADDRESS BIT 2
A1A3V	J8	¤N	CHANNEL 1, OPERAND ADDRESS BIT 3
A2A3V	J8	CC	CHANNEL 2, OPERAND ADDRESS BIT 3
A3A3V	J8	¤Q	CHANNEL 3, OPERAND ADDRESS BIT 3
A1A4V	J8	FF	CHANNEL 1, OPERAND ADDRESS BIT 4
A2A4V	J8	GG	CHANNEL 2, OPERAND ADDRESS BIT 4
A3A4V	J8	¤Z	CHANNEL 3, OPERAND ADDRESS BIT 4
A1A5V	J8	R	CHANNEL 1, OPERAND ADDRESS BIT 5
A2A5V	J8	¤W	CHANNEL 2, OPERAND ADDRESS BIT 5
A3A5V	J8	¤J	CHANNEL 3, OPERAND ADDRESS BIT 5
A1A6V	J8	¤V	CHANNEL 1, OPERAND ADDRESS BIT 6
A2A6V	J8	¤Y	CHANNEL 2, OPERAND ADDRESS BIT 6
A3A6V	J8	¤K	CHANNEL 3, OPERAND ADDRESS BIT 6
A1A7V	J8	A	CHANNEL 1, OPERAND ADDRESS BIT 7
A2A7V	J8	X	CHANNEL 2, OPERAND ADDRESS BIT 7
A3A7V	J8	¤R	CHANNEL 3, OPERAND ADDRESS BIT 7
A1A8V	J8	EE	CHANNEL 1, OPERAND ADDRESS BIT 8
A2A8V	J8	HH	CHANNEL 2, OPERAND ADDRESS BIT 8
A3A8V	J8	S	CHANNEL 3, OPERAND ADDRESS BIT 8
A1A9V	J8	Y	CHANNEL 1, OPERAND ADDRESS BIT 9
A2A9V	J8	C	CHANNEL 2, OPERAND ADDRESS BIT 9
A3A9V	J8	W	CHANNEL 3, OPERAND ADDRESS BIT 9
A1TRSV	J8	F	CHANNEL 1, TRANSFER REGISTER OUTPUT
A2TRSV	J8	E	CHANNEL 2, TRANSFER REGISTER OUTPUT
A3TRSV	J8	D	CHANNEL 3, TRANSFER REGISTER OUTPUT
INTRLK	J8	K	LTE INTERLOCK FOR LTE USE ONLY
INTRLK	J8	L	LTE INTERLOCK FOR LTE USE ONLY
SR86	J8	V	SIGNAL RETURN, LINE 86 OPERAND ADDRESS BITS A1,A2, A3,A7, AND A9 FOR CHANNELS 1,2,AND3
SR87	J8	Z	SIGNAL RETURN, LINE 87 TRSV, CHANNELS 1,2, AND 3
SR88	J8	¤I	SIGNAL RETURN, LINE 88 OPERAND ADDRESS BITS A4,A5, A6, AND A8 FOR CHANNELS 1,2, AND 3
SPARE	J8	B	
SPARE	J8	G	
SPARE	J8	H	
SPARE	J8	J	
SPARE	J8	M	
SPARE	J8	N	
SPARE	J8	P	
SPARE	J8	U	
SPARE	J8	¤A	
SPARE	J8	¤B	
SPARE	J8	¤C	
SPARE	J8	¤D	
SPARE	J8	¤E	
SPARE	J8	¤F	
SPARE	J8	¤G	
SPARE	J8	¤H	
SPARE	J8	¤S	
SPARE	J8	¤T	
SPARE	J8	¤U	
SPARE	J8	¤X	

NOTE *DENOTES INPUTS TO COMPUTER, ¤INDICATES LOWER CASE LETTER

Figure 3-2. Computer Interface Signals (Sheet 8)

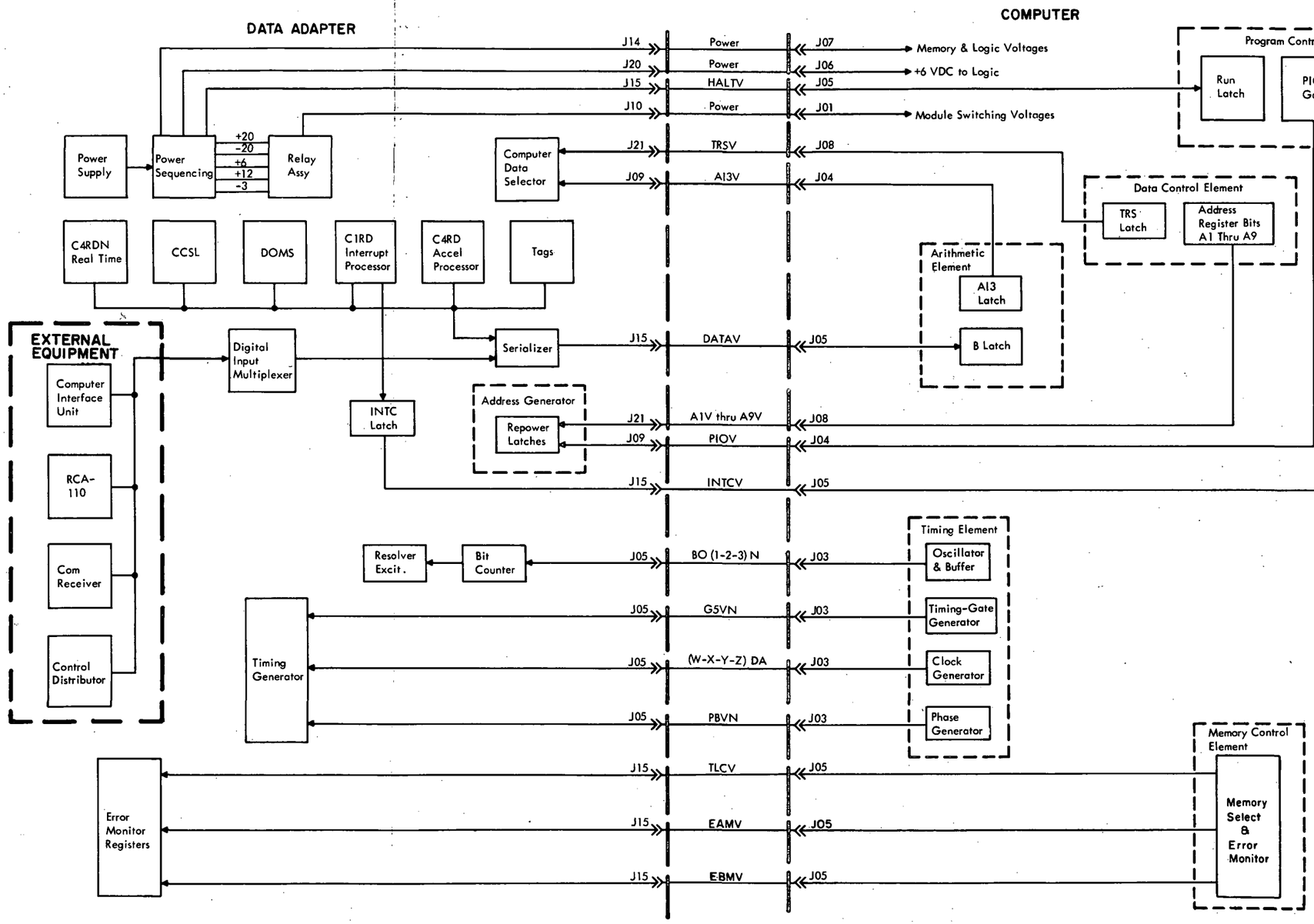


Figure 3-3. Computer - Data Adapter Interconnection Block Diagram

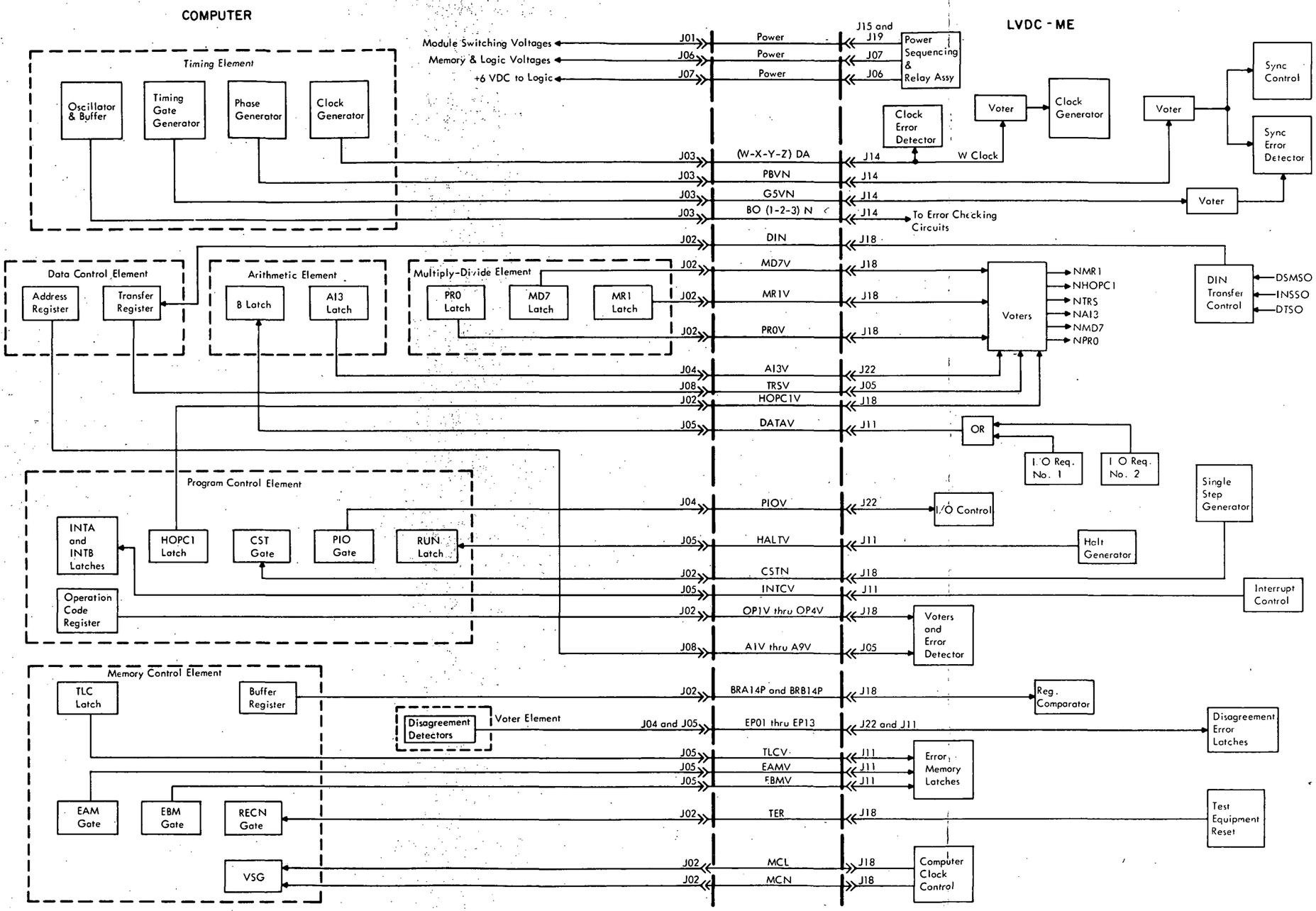


Figure 3-4. Computer and LVDC-ME Interconnection Block Diagram

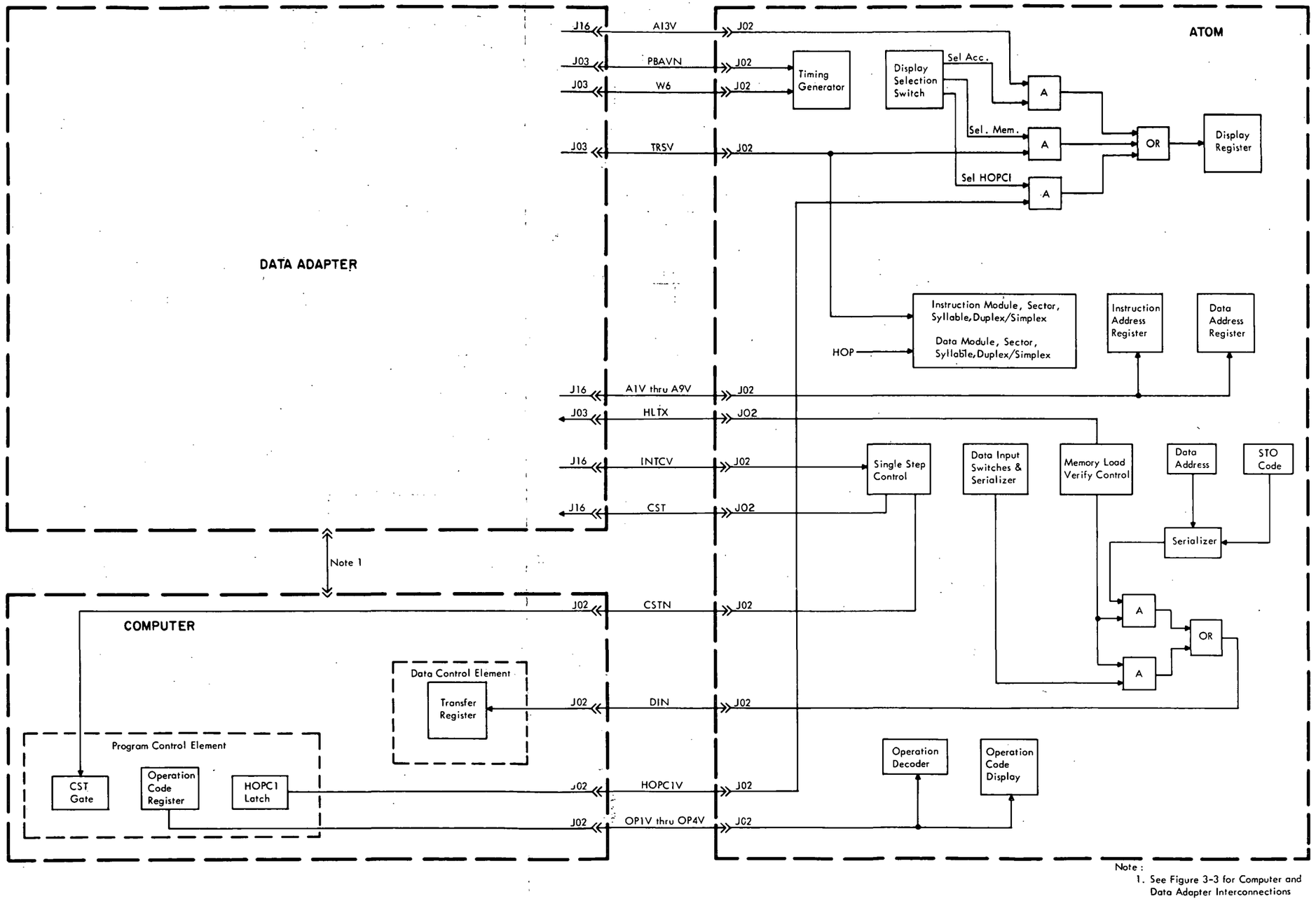


Figure 3-5. Computer - ATOM Interconnection Block Diagram

SECTION IV

TEST EQUIPMENT AND SPECIAL TOOLS.

4-1. TEST EQUIPMENT.

4-2. STANDARD TEST EQUIPMENT.

4-3. The standard test equipment recommended to maintain the computer is listed in figure 4-1.

4-4. SPECIAL TEST EQUIPMENT.

4-5. The special test equipment required to maintain the computer is listed in figure 4-2.

4-6. SPECIAL TOOLS.

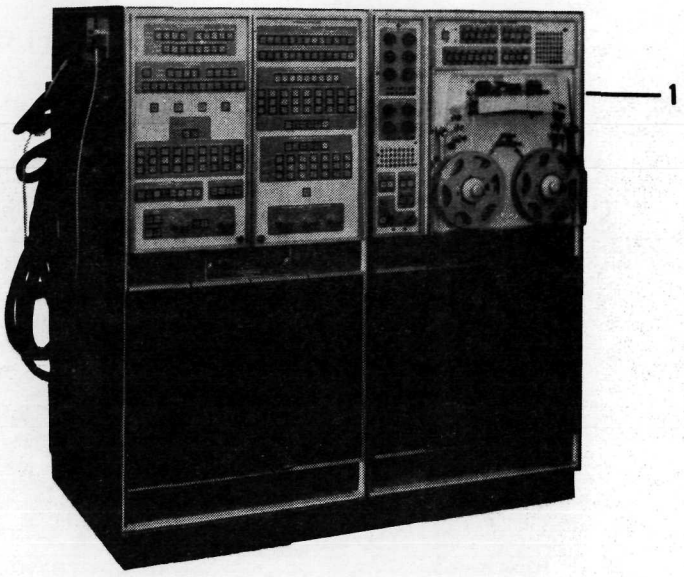
4-7. The special tools recommended to maintain the computer are listed in figure 4-4.

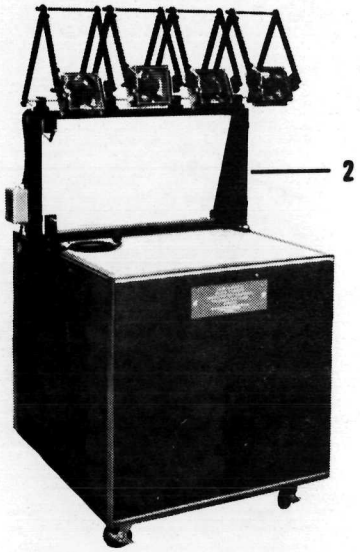
Name	Model or Type	Vendor
Differential Voltmeter	803-B	John Fluke Mfg. Co., Inc.
Volt-Ohm-Ammeter	630-A	Triplett Electrical Instrument Co.
Oscilloscope	585A	Tektronix, Inc.
Oscilloscope Adapter	81	Tektronix, Inc.
Oscilloscope Plug-In Unit	M	Tektronix, Inc.

Figure 4-1. Standard Test Equipment Table

Name	Manufacturer's Designation	Index No. (Figure 4-3)	Description
Book Cart	IBM 6900039	3	Movable book case, used for storage of prime and test equipment manuals and logic diagrams.
Equipment Test Stand	IBM 6940100	2	Supports the computer and provides cooling air during test.
Launch Vehicle Digital Computer-Manual Exerciser	IBM 6902000 MD1	1	Used to test and evaluate computer operation.
Test Program Tape	IBM 6001225		Contains a program which, when loaded into the computer memory, permits the Launch Vehicle Digital Computer-Manual Exerciser to check each functional part of the computer that can be exercised by a program.

Figure 4-2. Special Test Equipment Table





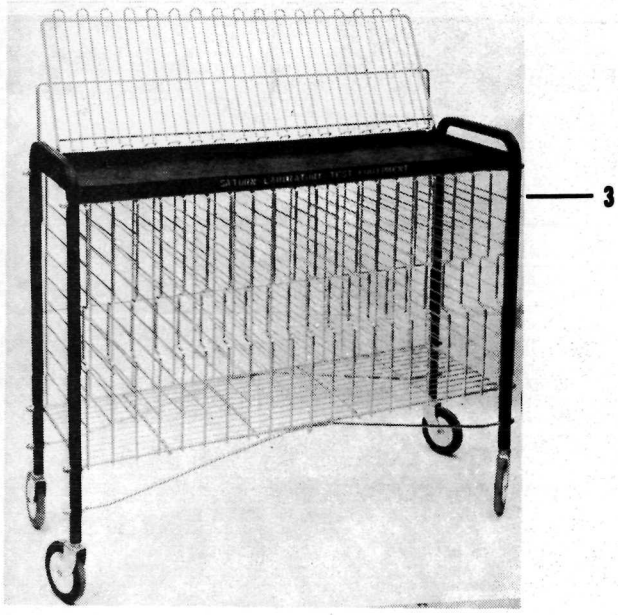


Figure 4-3. Special Test Equipment

Name	Manufacturer's Designation	Index No. (Figure 4-5)	Description
Handling Dolly	IBM 658042		Supports computer while being maintained.
Lift Handles	IBM D-656101	3	Provide a means for handling and lifting the computer during general handling activity.
Memory Handle	IBM 658044	2	Used to disengage memory from its mating receptacle. Also recommended for general handling of memory.
Page Extractor	IBM 657922	1	Used to mechanically engage or disengage the page connector from its mating receptacle.
Test Point Adapter	Number to be supplied.		Use to provide access to test points on page assemblies.
Torque Tool Kit	Number to be supplied.		Contains special torque tools required for torquing those items replaced during laboratory maintenance.

Figure 4-4. Special Tools Table

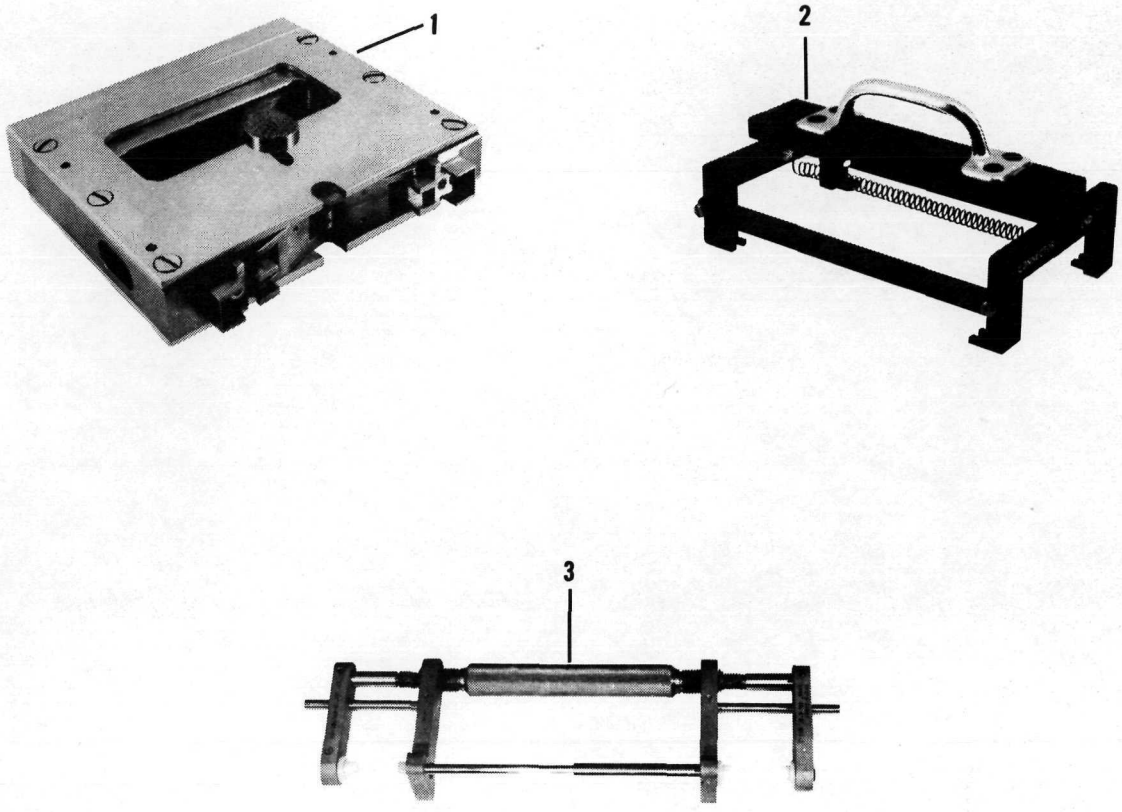


Figure 4-5. Special Tools

SECTION V

PREPARATION FOR USE, STORAGE AND SHIPMENT

5-1. PREPARATION FOR USE.

5-2. The computer is shipped in a reuseable shipping container (part number 6019994, figure 5-1). Included in the container, although not shown in figure 5-1, is a shock recorder (part number 6019637). To remove the computer from the container, proceed as follows:

a. Turn pressure equalizer screw (on shipping container) two turns counterclockwise.

b. Unlatch and remove container cover.

c. Remove the four mounting bolts securing the computer to the container frame.

WARNING

The computer shall be lifted by at least two persons. Otherwise, a person may be injured or the computer damaged.

d. Attach the lift handles to the computer, as described in paragraph 5-8; remove the computer from the container and place on a handling dolly or test stand. (Refer to section IV.)

e. Reinstall the mounting bolts for safekeeping.

f. Remove the shock recorder after removing the four socket head screws which attach it to its bracket; then replace socket head screws in bracket for safekeeping.

g. Open the shock recorder.

g1. Remove the spool that contains the recorded portion of chart paper (figure 5-2).

CAUTION

When removing chart paper, handle chart paper carefully. Cut (do not tear) the chart paper to detach recorded portion. The paper is pressure sensitive, and data may be obliterated by rough or excessive handling.

g2. Cut the chart paper, remove it from the spool, and replace the spool in the recorder.

Figure 5-1. Reuseable Shipping Container

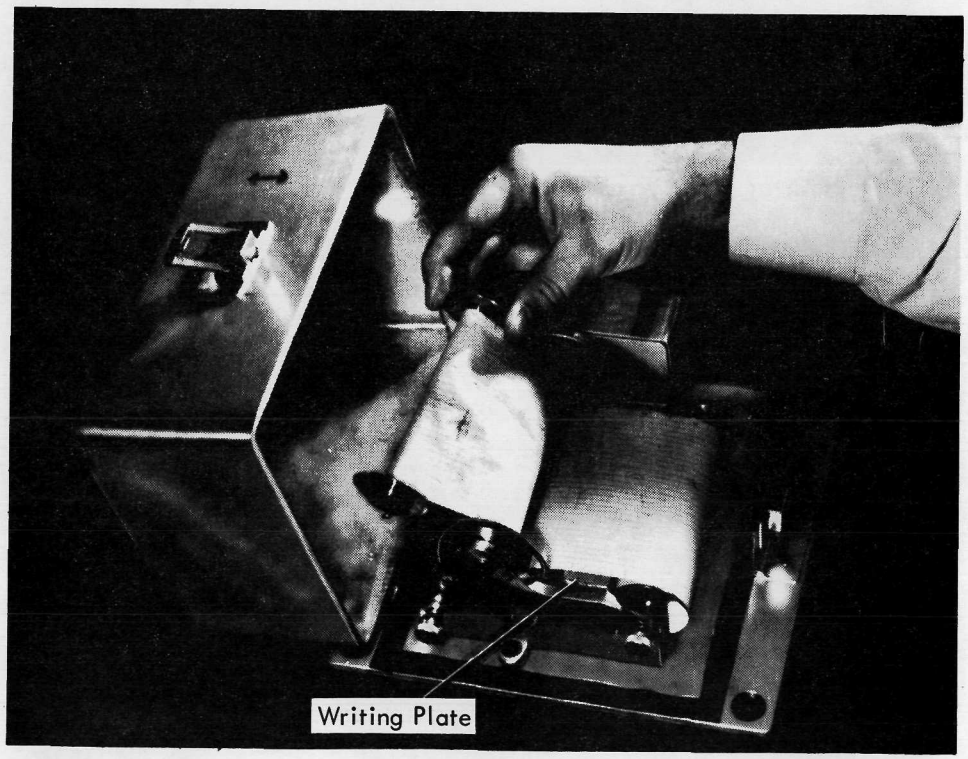


Figure 5-2. Removing Roll Chart From Shock Recorder

NOTE

The recorder clock mechanism will operate until its spring mechanism has unwound. If the recorder is not to be used immediately, do not rethread the chart paper. Instead, tape the loose end of the chart paper to the writing plate. (See figure 5-2.) This procedure saves paper and protects the styluses which would otherwise rest on the hard surface of the plate.

g3. Rethread the chart paper onto the takeup spool (figure 5-3), or tape the paper to the writing plate.

g4. Close and latch the shock recorder.

g5. Reinstall the shock recorder (handle side up) in the shipping container.

g6. On a blank portion of the removed section of chart paper, record the

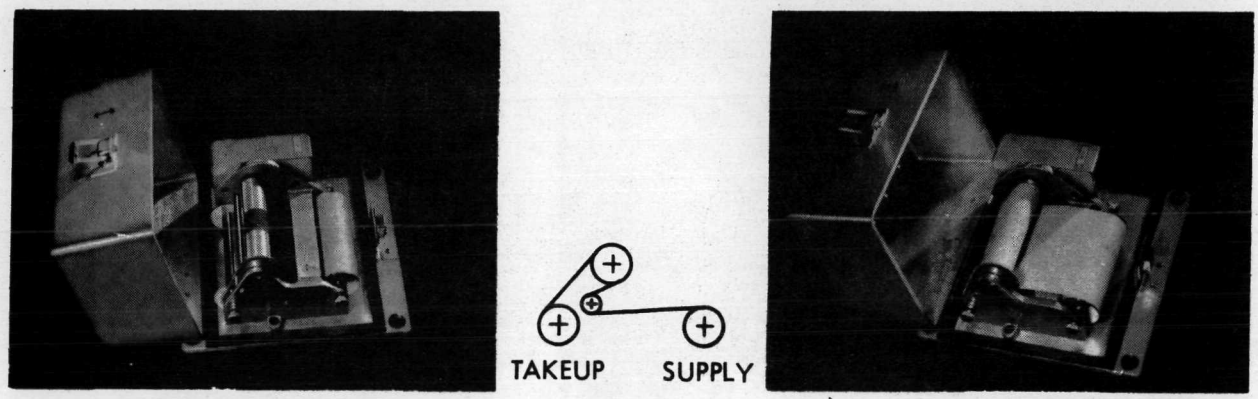
Government Bill of Lading Number

Receiving Location and Receiving Individual's Signature

Unit Name, Part Number, and Serial Number

Container Serial Number and Recorder Serial Number

Data and Local Time recorder was opened.



(B) FEED DIAGRAM

(A) ROLL CHART PARTIALLY INSTALLED

(C) ROLL CHART COMPLETELY INSTALLED

Figure 5-3. Installing Roll Chart in Shock Recorder

h. Ship removed section of chart paper to:

Saturn Programs Office, Department 839

IBM Space Guidance Center

Owego, New York, 13827

h1. Use a vacuum cleaner to clean the interior of container if foreign material or debris is in the shipping container.

i. Secure cover on shipping container; then store container for reuse.

5-2A. INSPECTION AND TEST.

5-2B. After the computer has been unpacked, proceed as follows:

a. Examine the exterior of the computer for mechanical damage, noting any evidence of impact or other severe mechanical stress. Check for loose screws and broken or missing connector dust covers. If extensive abnormalities are noted, remove covers and inspect interior of the computer. (Refer to Section IX for disassembly instructions.)

b. Remove and store connector dust covers.

c. Perform an electrical checkout of the computer. (Refer to Technical Manual, Checkout Procedures for Saturn LVDC and LVDA.)

5-3. PREPARATION FOR STORAGE.

5-4. The computer is stored in a reuseable shipping container (part number 6019994, figure 5-1). The computer is prepared for storage as follows:

a. Install dust covers (part number 6036037) on the eight computer connector jacks.

a1. Unlatch and remove shipping container cover.

a2. Use a vacuum cleaner to clean interior of container if foreign material or debris is in the shipping container.

b. Remove mounting bolts from computer shipping container.

b1. Attach lift handles to computer as described in paragraph 5-8.

WARNING

The computer shall be lifted by at least two persons. Otherwise, a person may be injured or the computer damaged.

c. Place computer on container mounting frame and secure with mounting bolts. Tighten mounting bolts with a torque of 250 inch-pounds.

d. Place 17 units of desiccant in receptacle provided.

NOTE

The 17 units of desiccant are packaged in three bags. The package part number, units of desiccant per package, and the quantity of each part number used are as follows:

IBM Part Number	No. of Units	Quantity Used
6019623	8	2
6019653	1	1

e. Secure cover on shipping container.

f. Turn pressure equalizer screw fully clockwise.

NOTE

During storage, the container humidity indicator should be checked at least once a week (more often if high humidity conditions prevail). If the "40" sector of the humidity indicator turns pink, the container dessicant should be replaced.

5-5. PREPARATION FOR SHIPMENT.

5-6. The computer is shipped in a reuseable shipping container (part number 6019994, figure 5-1). Included in the container is a shock recorder (part number 6019637). The computer is prepared for shipment as follows:

a. Install dust covers (part number 6036037) on the eight computer connector jacks.

a1. Unlatch and remove container cover.

b. Remove mounting bolts from computer shipping container.

WARNING

The computer shall be lifted by at least two persons. Otherwise, a person may be injured or the equipment damaged.

c. Place computer on container mounting frame and secure with mounting bolts. Tighten mounting bolts with a torque of 250 inch-pounds.

CAUTION

Verify that shock recorder styluses are marked "100 g". Otherwise, recorder will not be capable of recording excessive shock with accuracy.

c1. Remove the shock recorder after removing the four socket head screws which attach the recorder to its bracket. Replace socket head screws in bracket for safekeeping.

c2. Open the shock recorder and check for damage.

d. Thread roll chart onto takeup spool of shock recorder. (See figure 5-3.)

d1. Close cover and strike recorder sharply against floor. Open cover and verify that all three styluses have made a discernable impression on the chart paper.

NOTE

A full roll of chart paper is long enough to record shock for a period of 60 half days (30 days). The numbers on the left-hand margin indicate the number of half days remaining on the roll. The mechanism is capable of running for eight days (16 half days). Verify that the number on the left-hand margin is 16 or greater at the point where recording starts. Reorder chart paper from the following address:

Electrical Standards, Dept. 331
Attention: Manager
IBM Space Guidance Center
Owego, New York, 13827

d2. On the chart paper record the

Government Bill of Lading Number

Sending Location and Sending Individual's Signature

Unit Name, Part Number and Serial Number

Container Serial Number and Recorder Serial Number

Date and Local Time recorder was started

NOTE

The chart paper is calibrated in A.M. and P.M. hours, but it is not necessary to align the paper with the local time. Simply write the local time at the point where the recorder was started.

d3. Wind the shock recorder, and verify that the paper is moving and that all three styluses are tracking.

d4. Close and latch the shock recorder, but do not lock the latch.

e. Remove socket head screws from shock recorder mounting bracket.

f. Install shock recorder on bracket, using socket head screws previously removed.

g. Place 17 units of desiccant in receptacle provided.

NOTE

The 17 units of desiccant are packaged in three bags. The package part number, units of desiccant per package, and the quantity of each part number used are as follows:

IBM Part Number	No. of Units	Quantity Used
6019623	8	2
6019653	1	1

h. Secure cover on shipping container.

i. Turn pressure equalizer screw fully clockwise.

5-7. GENERAL COMPUTER HANDLING.

5-8. Computer lift handles (IBM Tool Number D-656101) are used for general handling of the computer. Two computer lift handles are needed for computer handling; one handle is mounted on the left side of the computer and the other handle is mounted on the right side of the computer. Mount the computer lift handles as shown in figure 5-4.

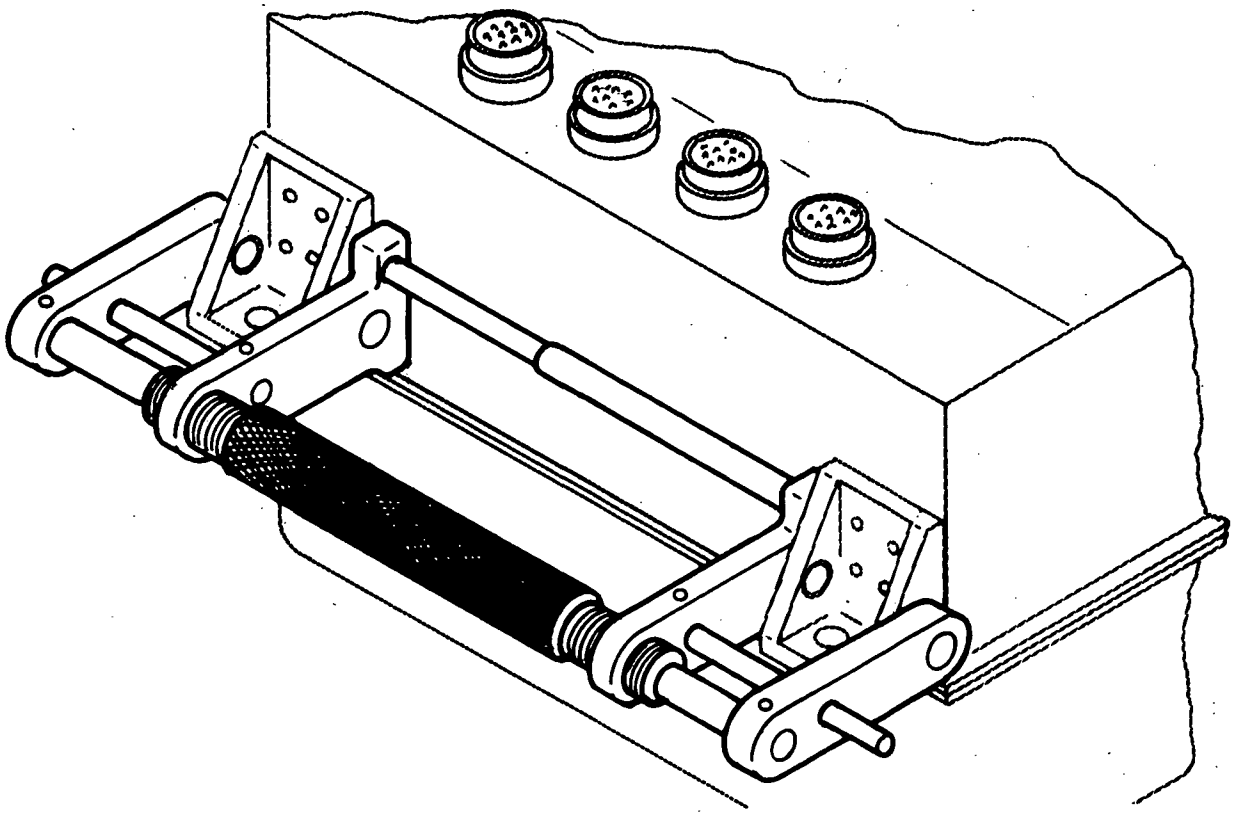


Figure 5-4. Computer Lift Handle, Mounted

SECTION VI

PREVENTIVE MAINTENANCE

No preventive maintenance is performed on the breadboard models.

SECTION VII

CHECKOUT

7-1. OPERATING TEST PROCEDURES.

7-2. Instructions for testing the computer are located in the Saturn V Launch Vehicle Digital Computer and Data Adapter Checkout Procedures Laboratory Maintenance Instructions.

SECTION VIII

TROUBLE ISOLATION

This section is not applicable
for breadboard equipments.

SECTION IX

REPAIR

9-1. REPAIR.

9-2. Laboratory repair of the computer is limited to replacing page assemblies and toroid memory assemblies. Laboratory replaceable assemblies are listed in figure 9-1. The methods for replacing such assemblies are described in this section. The computer is mounted on an equipment test stand (IBM part number 6940100) during repair.

9-3. PAGE ASSEMBLY REPLACEMENT. (See figure 9-2.) The page assemblies are accessable after removing the computer logic cover. To replace a page assembly proceed as follows:

a. Remove the logic cover by removing and storing the 14 mounting screws and washers located around the outer edge of the cover.

b. Locate the page assembly to be replaced. (Refer to figure 9-3.)

NOTE

Do not remove page assembly captive mounting screws from page assembly until after the page assembly is removed from computer.

Assembly	Location
6110211	A4A11
6110212	A4A12
6110213	A1A3, A2A3, A3A3
6110214	A1A7
6110215	A1A8
6110216	A1A9
6110217	A1A10
6110218	A1A5
6110219	A1A11
6110230	A1A12
6110231	A1A13
6110232	A1A14
6110233	A1A15
6110234	A1A16
6110235	A1A17
6110236	A1A18
6110237	A1A19

Assembly	Location
6110238	A1A20
6110239	A5A9, A5A10
6110240	A5A11
6110251	A1A4, A2A4, A3A4, A4A4
6110252	A5A3
6111500	A6A2, A6A3
6125408	A5A5
6125409	A5A6
6125420	A4A5, A4A6, A4A7, A4A8, A4A9, A4A13, A4A14
6125423	A5A7, A5A8
6125424	A5A12
6125425	A5A13
6125426	A5A14
6125427	A5A15

Figure 9-1. Laboratory Replaceable Assemblies

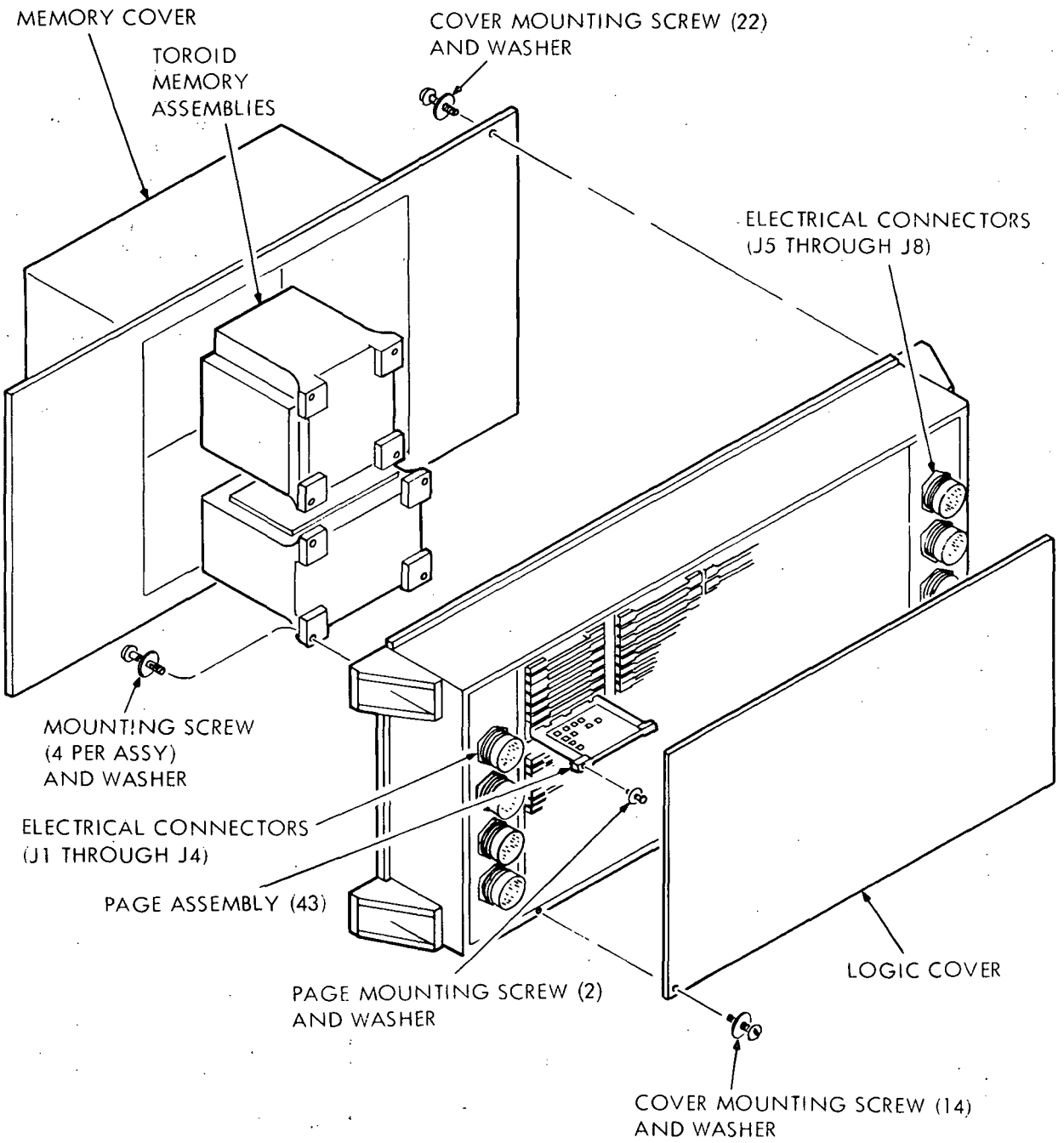


Figure 9-2. Computer, Partially Disassembled

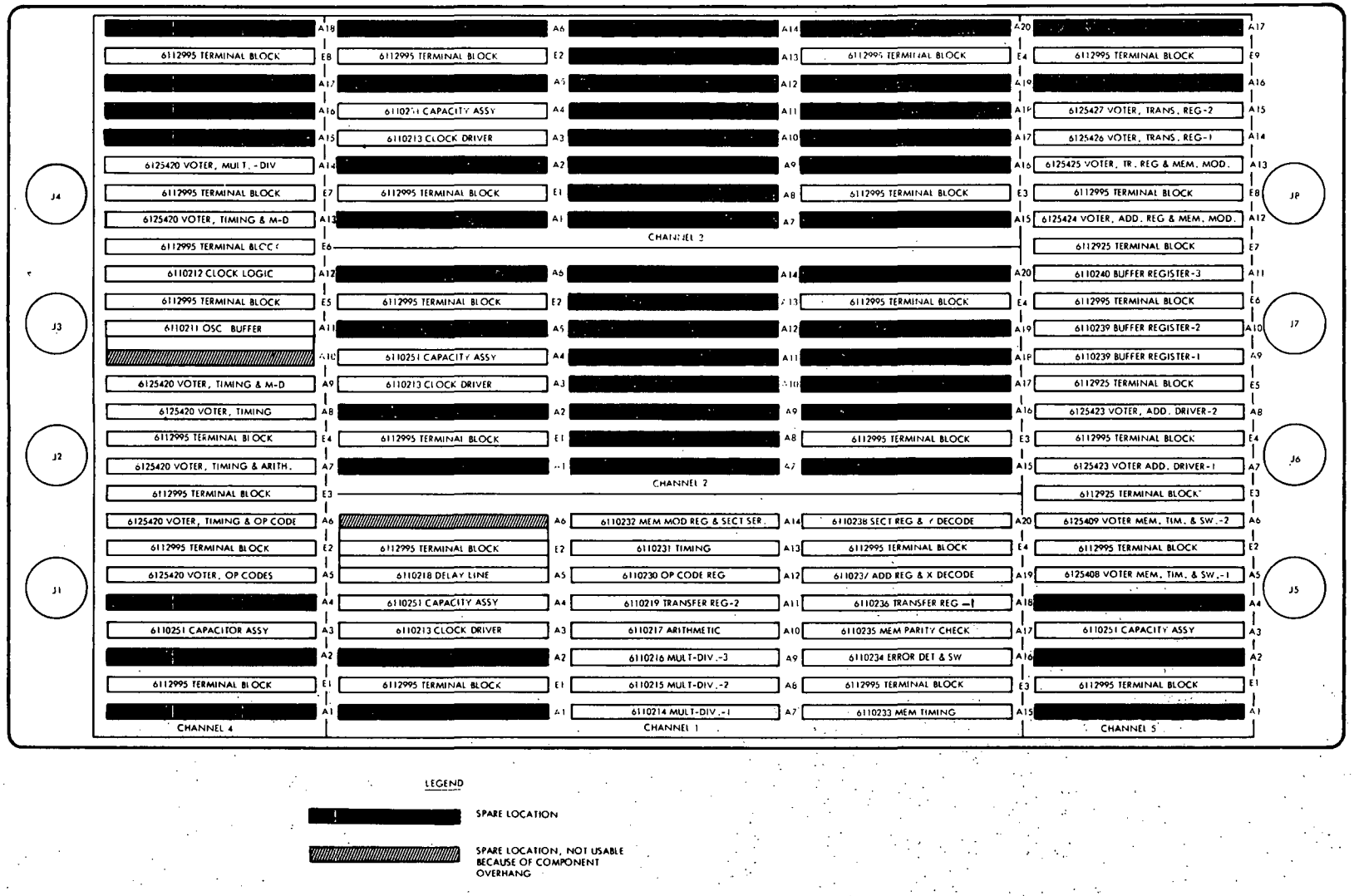


Figure 9-3. Page Assembly Location Guide

c. Unscrew the two page assembly captive mounting screws until free of mounting holes.

NOTE

Remove page assemblies with a page insertion-extraction tool (figure 4-4), hereafter referred to as extractor tool.

d. Place extractor tool over top of page assembly; then push locking knob toward page assembly, thus locking tool to assembly.

e. Squeeze extractor tool handle to its limit (disengaging page assembly connector); then pull page assembly straight out.

CAUTION

Hold page assembly firmly to safeguard dropping when releasing extractor tool.

f. Release page assembly from extractor tool by pushing in the locking knob and moving knob away from page assembly.

g. Remove and store mounting screws and associated fiber washers from page assembly.

NOTE

Page assembly removal is now complete. To install the replacement page assembly proceed with step h.

h. Install previously removed page assembly mounting screws and fiber washers (IBM part numbers 6110636 and 6113634) in replacement page assembly.

i. Place extractor tool over top of replacement page assembly; then push locking knob toward page assembly, thus locking tool to assembly.

CAUTION

Verify that A side of page assembly faces downward when inserting page assembly into computer. Otherwise connector pins will not mate with receptacle.

j. Insert page assembly into proper computer logic channel location.

k. Push in extractor tool locking knob; then move knob away from page assembly, thus releasing tool from page assembly.

l. Turn in the two page assembly mounting screws; then torque screws to 15 inch-pounds.

m. Secure computer logic cover by turning in cover mounting screws and washers (IBM part numbers 6072520 and 6048641); then, using the cross-over method, torque cover mounting screws to 10 inch-pounds.

9-4. TOROID MEMORY ASSEMBLY REPLACEMENT. (See figure 9-2.) The toroid memory is accessable after removal of the computer memory cover. To replace a toroid memory assembly proceed as follows:

a. Remove the memory cover by removing and storing the 22 mounting screws and washers located around cover edge.

NOTE

Memory assembly connectors mate with connectors J2 and J3 of memory mounting plate assembly.

NOTE

The replacement of the toroid memory assembly is simplified by the use of the memory handle. (Refer to figure 4-4.)

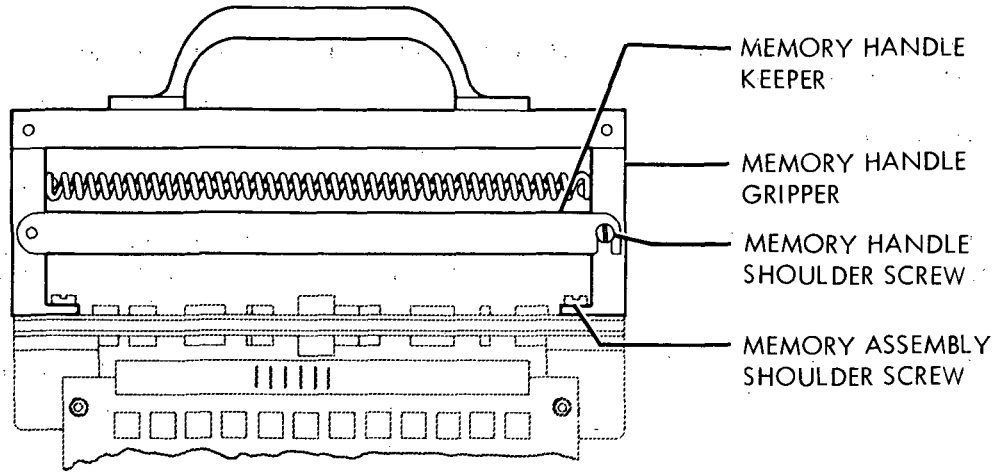
When attaching memory handle to memory assembly, attach gripper marked CONNECTOR END to shoulder screws at connector end of memory assembly.

b. Slide memory handle grippers under four shoulder screws on top of memory assembly; then place tool keeper over memory handle shoulder screw, thus securing tool to assembly. (See figure 9-4.)

CAUTION

Hold memory handle firmly to safeguard dropping memory assembly during removal of memory assembly mounting screws.

c. Remove and store the four memory assembly mounting screws and associated washers.



NOTE: PHANTOM AREA INDICATES MEMORY ASSEMBLY

Figure 9-4. Memory Handle Secured to Memory Assembly

NOTE

The memory assembly connector is a rack-and-panel type and will disengage from its mating receptacle on the memory distribution board as the memory assembly is lifted out.

d. Pull on memory handle just enough to disengage memory assembly connector; then offset assembly enough to clear adjacent memory assembly and pull assembly straight out.

e. Remove memory handle from memory assembly.

NOTE

Toroid memory assembly removal is now complete. To install a replacement memory assembly proceed with step f.

NOTE

When attaching memory handle to memory assembly, attach gripper marked CONNECTOR END to shoulder screws at connector end of memory assembly.

f. Slide memory handle grippers under four shoulder screws on top of replacement memory assembly; then place tool keeper over memory handle shoulder screw, thus securing tool to assembly. (See figure 9-4.)

CAUTION

Hold memory assembly and memory handle
firmly to safeguard dropping during installation.

g. Insert replacement memory assembly into proper memory distribution board location; then verify that connector and receptacle are properly mated.

h. Turn in memory assembly mounting screws with associated washers (IBM part numbers 6035770 and 6113635); then torque screws to 15 foot-pounds.

i. Install memory cover and turn in mounting screws with associated washers (IBM part numbers 6076307 and 6048641); then using the cross-over method torque screws to 10 inch-pounds.

SECTION X

DIAGRAMS

10-1. DIAGRAMS.

10-2. The diagrams included in this section are the drawings required to maintain the computer. The drawings consist of the following:

Figure 10-1. Clock Drivers Logic Diagram (4 Sheets)
Figure 10-2. Decoupling Capacitors (Channel 1) Logic Diagram (4 Sheets)
Figure 10-3. Delay Lines Logic Diagram (2 Sheets)
Figure 10-4. Multiply-Divide Element Logic Diagram (12 Sheets)
Figure 10-5. Add-Subtract Element Logic Diagram (4 Sheets)

Figure 10-6. Transfer Register Bits 10-TRS and Control Logic Diagram (2 Sheets)
Figure 10-7. Memory Buffer Control and Parity Counter Logic Diagram (2 Sheets)
Figure 10-8. Operation Code Register Logic Diagram (4 Sheets)
Figure 10-9. Timing Gate Generator Logic Diagram (2 Sheets)
Figure 10-10. Phase Generator Logic Diagram (2 Sheets)

Figure 10-11. Memory Module Registers Logic Diagram (2 Sheets)
Figure 10-12. HOP Constant Serializer and Memory Read Latches Logic Diagram (2 Sheets)
Figure 10-13. Memory Timing Logic Diagram (4 Sheets)
Figure 10-14. Memory Error Detector Logic Diagram (8 Sheets)

Figure 10-15. Transfer Register Bits 1-9 Logic Diagram (4 Sheets)
Figure 10-16. Address Register and Memory Address Decoder Logic Diagram (4 Sheets)
Figure 10-17. Memory Sector Registers Logic Diagram (2 Sheets)
Figure 10-18. Hi-Y Memory Address Decoder Logic Diagram (2 Sheets)
Figure 10-19. Decoupling Capacitors (Channel 4) Logic Diagram (4 Sheets)

Figure 10-20. Operation Code Voters Logic Diagram (4 Sheets)
Figure 10-21. Timing Gate and Operation Code Voters Logic Diagram (4 Sheets)
Figure 10-22. Timing and Add-Subtract Voters Logic Diagram (4 Sheets)
Figure 10-23. Timing Voters Logic Diagram (4 Sheets)
Figure 10-24. Timing and Multiply-Divide Voters Logic Diagram (4 Sheets)

Figure 10-25. Oscillator and Buffer Logic Diagram (2 Sheets)
Figure 10-26. Clock Generator Timing Logic, Logic Diagram (4 Sheets)
Figure 10-27. Timing and Multiply-Divide Voters Logic Diagram (4 Sheets)
Figure 10-28. Multiply-Divide Voters, Logic Diagram (4 Sheets)
Figure 10-29. Decoupling Capacitors (Channel 5) Logic Diagram (4 Sheets)

Figure 10-30. Memory Timing Voters Logic Diagram (8 Sheets)
Figure 10-31. Memory Address Decoder Voters Logic Diagram (8 Sheets)
Figure 10-32. Memory Buffer Registers Logic Diagram (12 Sheets)
Figure 10-33. Address Register and Memory Module Register Voters Logic Diagram (4 Sheets)

10-3. SIGNAL TRACING.

10-4. Signals may be categorized into two groups:

- Signals that appear at the input-output connectors.
- Signals that originate in, and are used solely by, the computer.

Locating these two types of signals and finding points in the computer where they may be observed requires two different procedures.

10-5. TRACING INPUT-OUTPUT SIGNALS. These signals may be located by referring to the interface listing, figure 3-2. The signals may be checked by probing the A4 and A5 back panels at terminal blocks A4J1 through A4J4, and A5J5 through A5J8. (See figure 10-50.)

NOTE

The A5J7 terminal block has the same pin layout as A4J4, with a different orientation.

The terminal blocks are directly wired to the input-output connectors and the terminal block pins have the same corresponding designation as the connector pins. To trace an input-output signal into the logic, refer to the interconnection back panel listings, figures 10-47 through 10-49. The signal can be found under the "Net Name" column.

NOTE

Signals originating outside the back panel (listing) being used, may require the reference designator prefix that is automatically assigned to all signals. Thus, if a signal cannot be found under the alphabetic portion of the listing, be sure to look under the portion of the listing which contains reference designator prefixes.

Once the signal is found in the listing, all the pin locations, by reference designator, are listed under the "Page-Pin" and "Bib-Pin" columns. The reference designator can then be used to find the signal in the logic. (See figures 10-1 through 10-35.)

NOTE

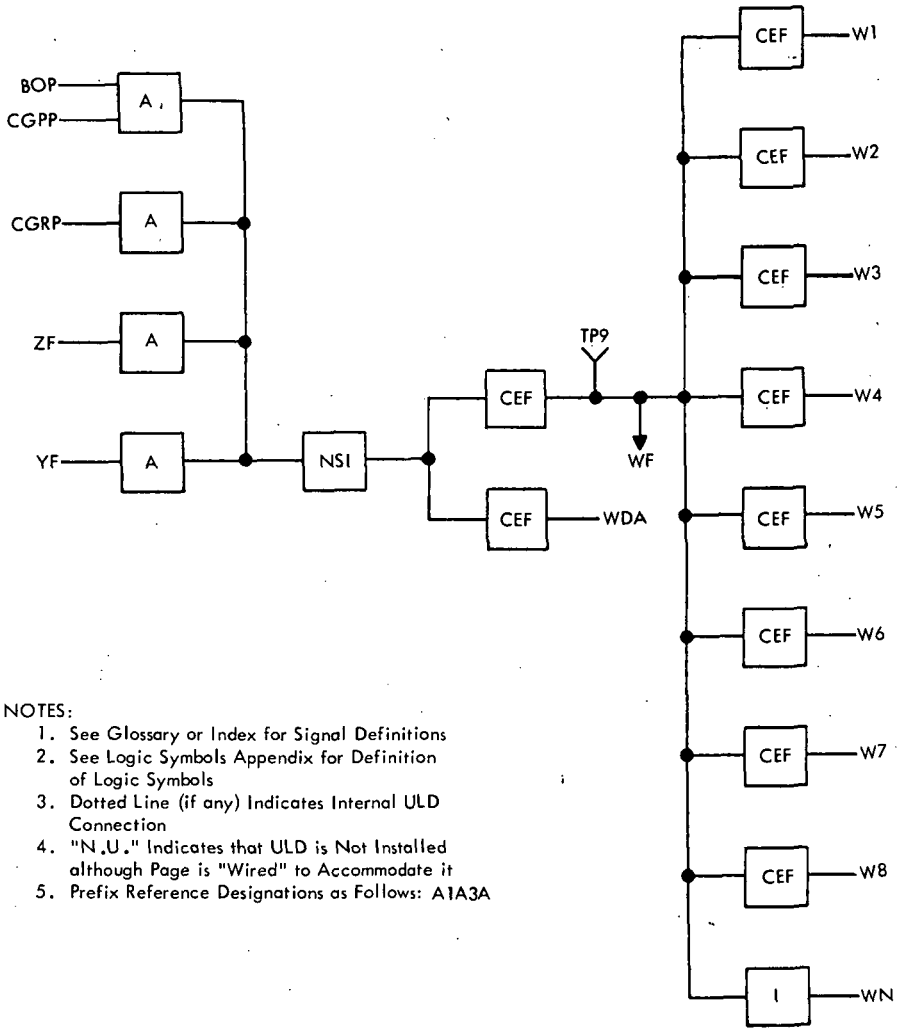
The reference designator for each MIB-logic diagram is located on the right hand margin, white symbols on a black background.

10-6. TRACING INTERNALLY GENERATED SIGNALS. These signals may be located by referring to the Signal-Origin List, figure 10-46. The signal-origin list refers the reader to the appropriate MIB-logic diagram by reference designator. (See figures 10-1 through 10-41.) On the MIB-logic diagram are references to test point locations on the logic page. If a signal is to be checked for which a test point is not provided, then one of the terminal blocks on the A4 or A5 back panels may make the desired signal available. (In addition, most of the channel 4 page pins are available from the rear of the A4 back panel.) Look up the signal name in the appropriate interconnection back panel listing and determine whether or not the signal goes to a terminal block. If the signal is used on both panels A1 (A2 and A3 also apply for redundant circuits) and A4, the listing will show a reference to a terminal block, reference designator A1EX or A4EX. (See figure 10-51 to identify pin locations.)

NOTE

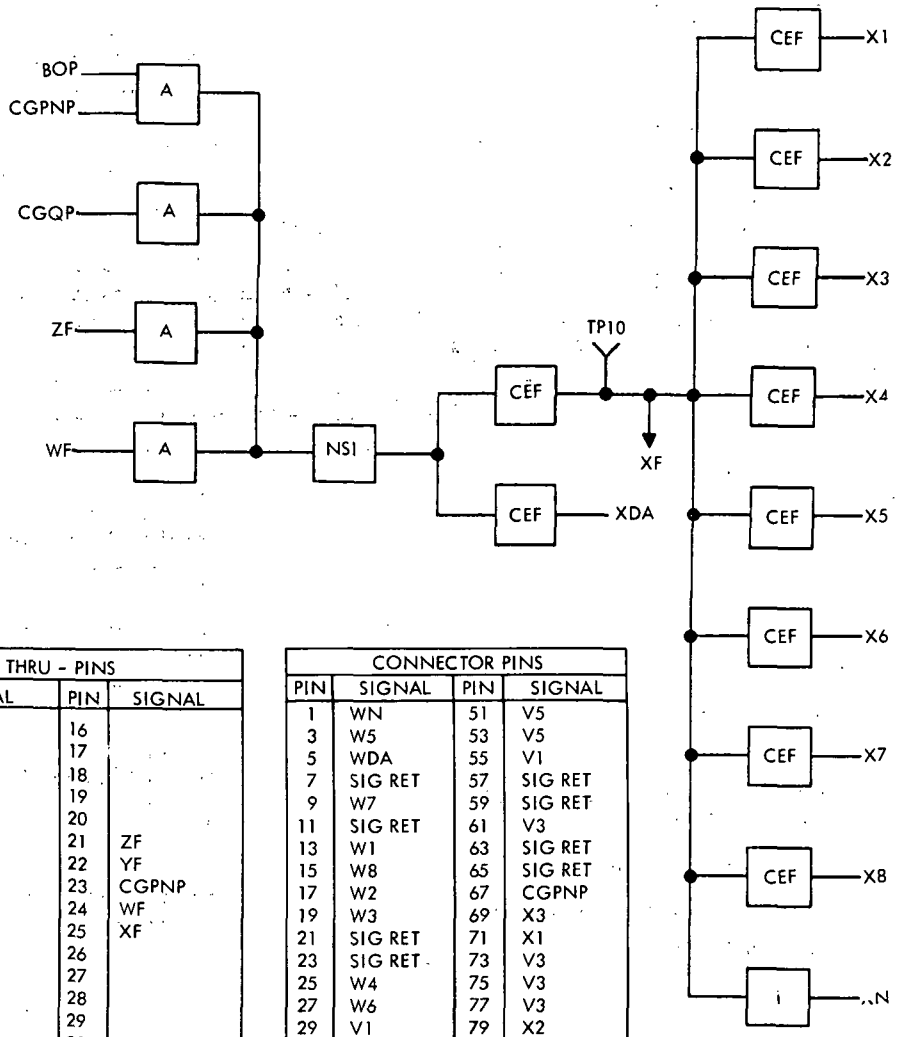
A one-to-one correspondence exists between pins on the A4 and A1 terminal blocks due to the printed circuit cables interconnecting the terminal blocks. (See figure 1-2.)

If the signal goes to a memory module from a location in channel 5, a reference to terminal blocks A5E3, A5E5, or A5E7 will occur. Some of these locations are available for probing. (See figure 10-51 to identify pin locations. Only the upper pins, rows A and B, are available for probing.) The points where signals appear on the memory module and memory distribution panel are illustrated in figures 10-44 and 10-45. These points are not available for probing.



NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate it
5. Prefix Reference Designations as Follows: A1A3A

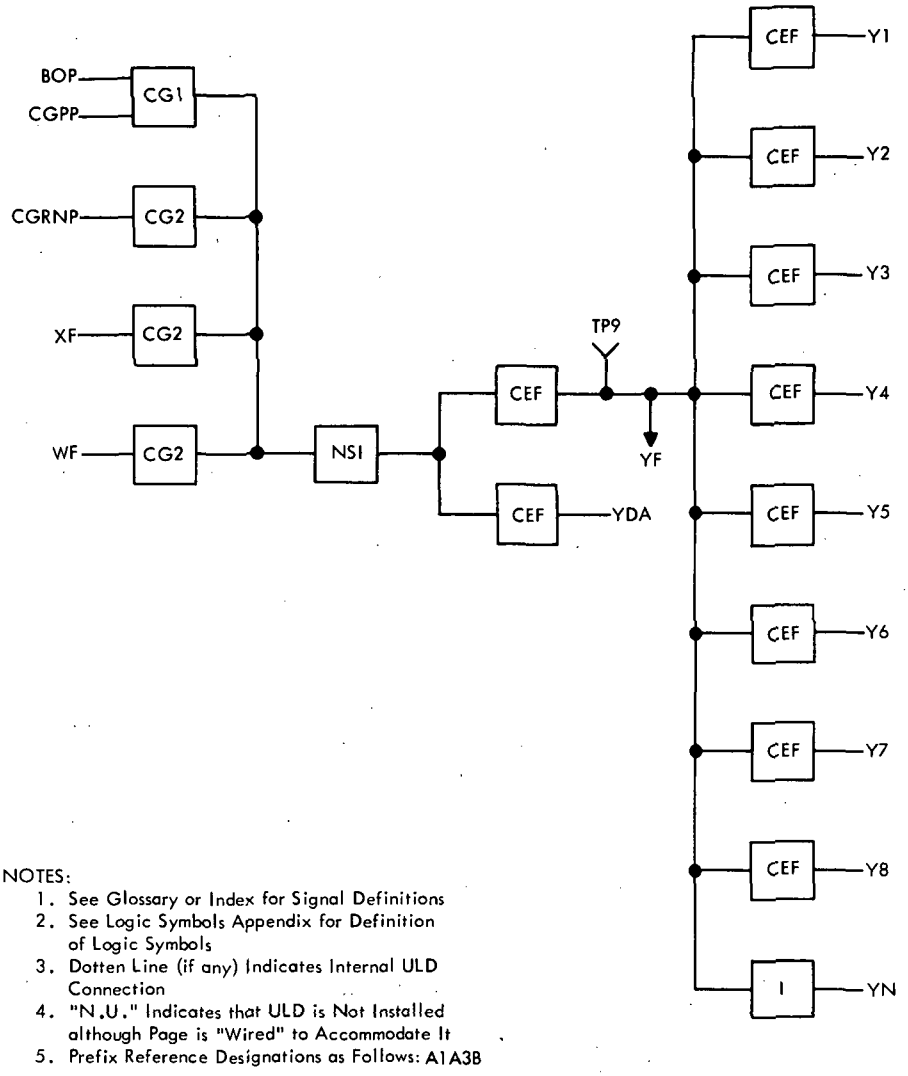
Figure 10-1. Clock Drivers, Logic Diagram (Sheet 1 of 4)



THRU - PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2		17	
3		18	
4		19	
5		20	
6		21	ZF
7		22	YF
8	CGPP	23	CGPNP
9		24	WF
10		25	XF
11		26	
12		27	
13		28	
14		29	
15		30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	WN	51	V5
3	W5	53	V5
5	WDA	55	V1
7	SIG RET	57	SIG RET
9	W7	59	SIG RET
11	SIG RET	61	V3
13	W1	63	SIG RET
15	W8	65	SIG RET
17	W2	67	CGPNP
19	W3	69	X3
21	SIG RET	71	X1
23	SIG RET	73	V3
25	W4	75	V3
27	W6	77	V3
29	V1	79	X2
31	V1	81	X4
33	CGRP	83	X6
35	SIG RET	85	X5
37	V3	87	SIG RET
39	BOP	89	XN
41	CGQP	91	SIG RET
43	V1	93	X8
45	CGPP	95	X7
47	V5	97	XDA
49	V5		

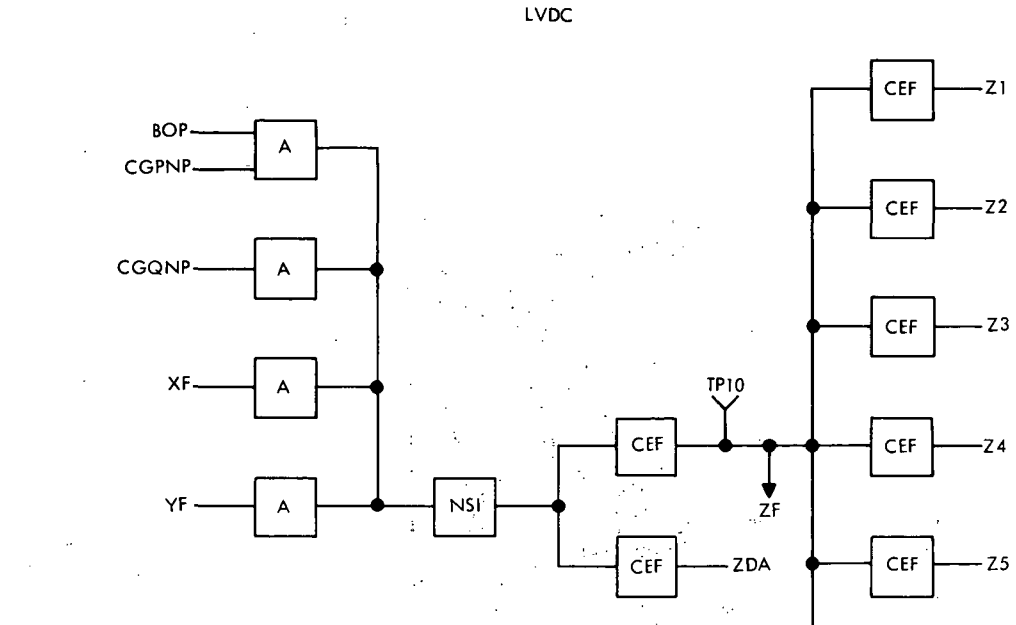
Figure 10-1. Clock Drivers, Logic Diagram (Sheet 2)



NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotten Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A3B

Figure 10-1. Clock Drivers, Logic Diagram (Sheet 3)



THRU - PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2		17	
3		18	
4		19	
5		20	
6		21	ZF
7		22	YF
8	CGPP	23	CGPNP
9		24	WF
10		25	XF
11		26	
12		27	
13		28	
14		29	
15		30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	ZDA	52	V5
4	Z7	54	CGPP
6	Z8	56	V1
8	SIG RET	58	CGQNP
10	ZN	60	BOP
12	SIG RET	62	V3
14	Z5	64	SIG RET
16	Z6	66	CGRNP
18	Z4	68	V1
20	Z2	70	V1
22	V3	72	Y6
24	V3	74	Y4
26	V3	76	SIG RET
28	Z1	78	SIG RET
30	Z3	80	Y3
32	CGPNP	82	Y2
34	SIG RET	84	Y8
36	SIG RET	86	Y1
38	V3	88	SIG RET
40	SIG RET	90	Y7
42	SIG RET	92	SIG RET
44	V1	94	YDA
46	V5	96	Y5
48	V5	98	YN
50	V5		

Figure 10-1. Clock Drivers, Logic Diagram (Sheet 4)

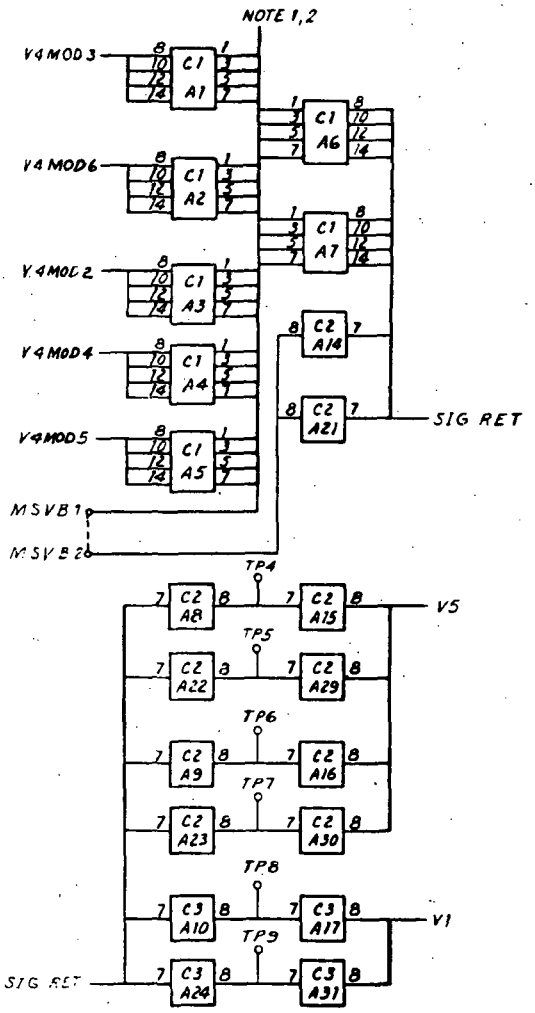
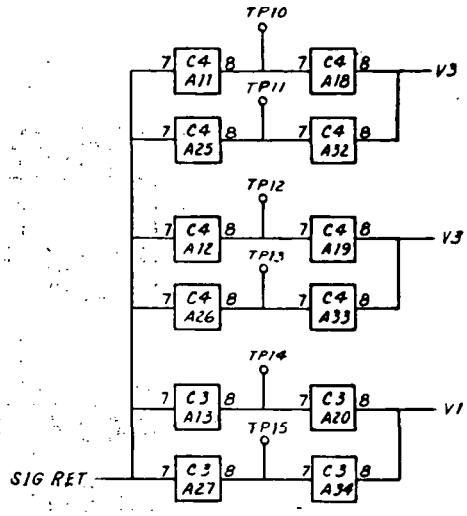


Figure 10-2. Decoupling Capacitors (Channel 1), Logic Diagram (Sheet 1 of 4)

A1A4A



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	MSVB1	51	SIG RET
3	MSVB1	53	SIG RET
5	SIG RET	55	SIG RET
7	SIG RET	57	SIG RET
9	V4MOD3	59	SIG RET
11	V3	61	SIG RET
13	V3	63	V3
15	V3	65	V3
17	V3	67	V3
19	V4MOD6	69	V3
21	V5	71	SIG RET
23		73	V1
25		75	V1
27		77	V1
29	V4MOD2	79	V1
31	V1	81	SIG RET
33	V1	83	SIG RET
35	V1	85	SIG RET
37	V1	87	SIG RET
39	V4MOD4	89	SIG RET
41	SIG RET	91	SIG RET
43	SIG RET	93	SIG RET
45	SIG RET	95	MSVB2
47	SIG RET	97	MSVB2
49	V4MOD5		

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A4A

Figure 10-2. Decoupling Capacitors (Channel 1), Logic Diagram (Sheet 2)

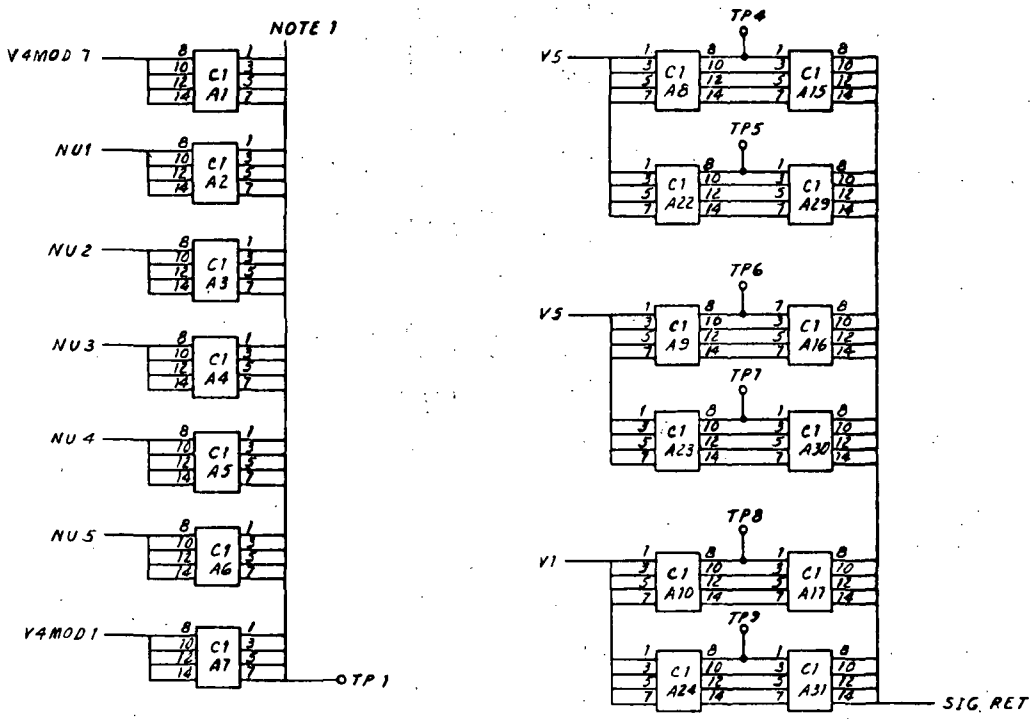
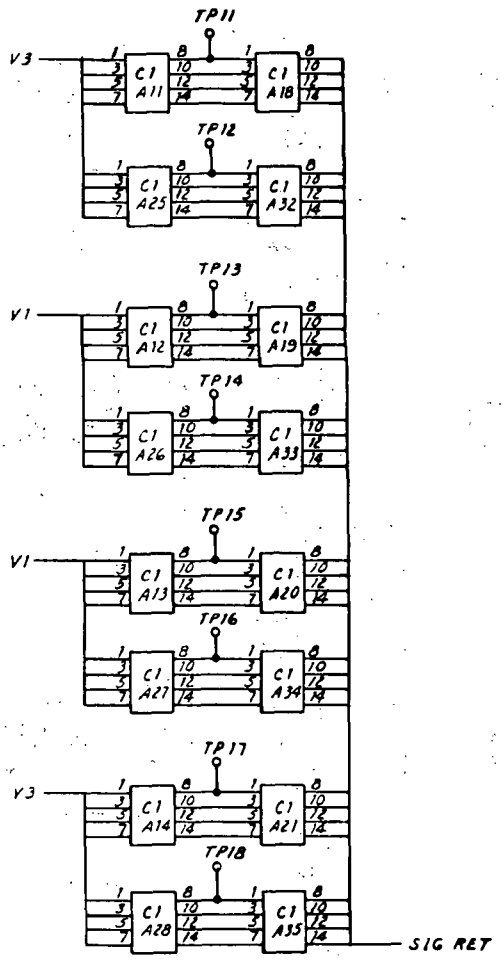


Figure 10-2. Decoupling Capacitors (Channel 1), Logic Diagram (Sheet 3)

A1A4B



CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	V3	52	V3
4		54	
6		56	
8		58	NU3
10	V4 MOD1	60	V1
12	V1	62	
14		64	
16		66	
18		68	SIG RET
20	SIG RET	70	
22		72	
24		74	
26		76	
28		78	NU2
30	V1	80	V5
32		82	
34		84	
36		86	
38	NU5	88	NU1
40	SIG RET	90	V5
42		92	
44		94	
46		96	
48	NU4	98	V4 MOD7
50	V3		

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A4B

Figure 10-2. Decoupling Capacitors (Channel 1), Logic Diagram (Sheet 4)

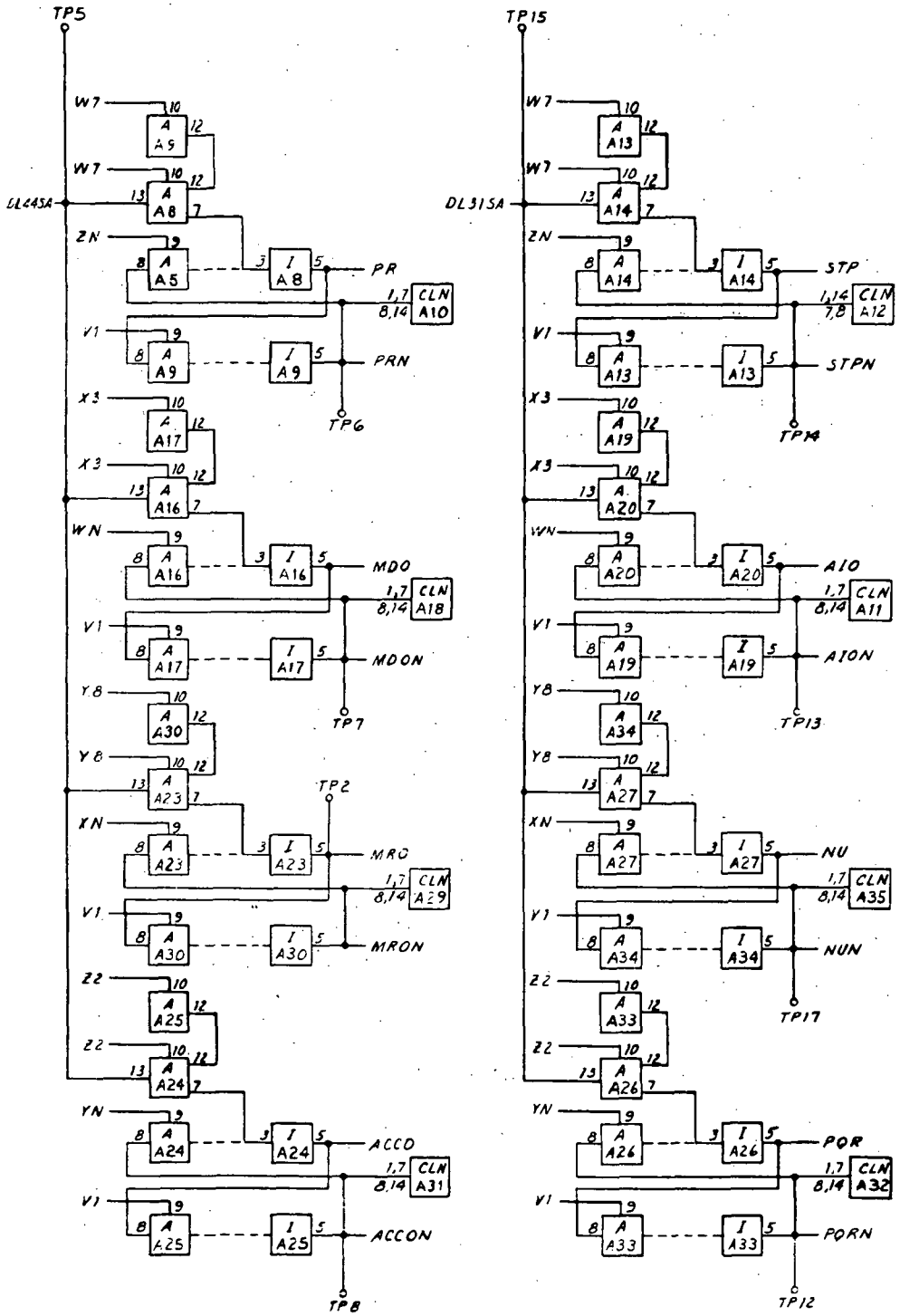
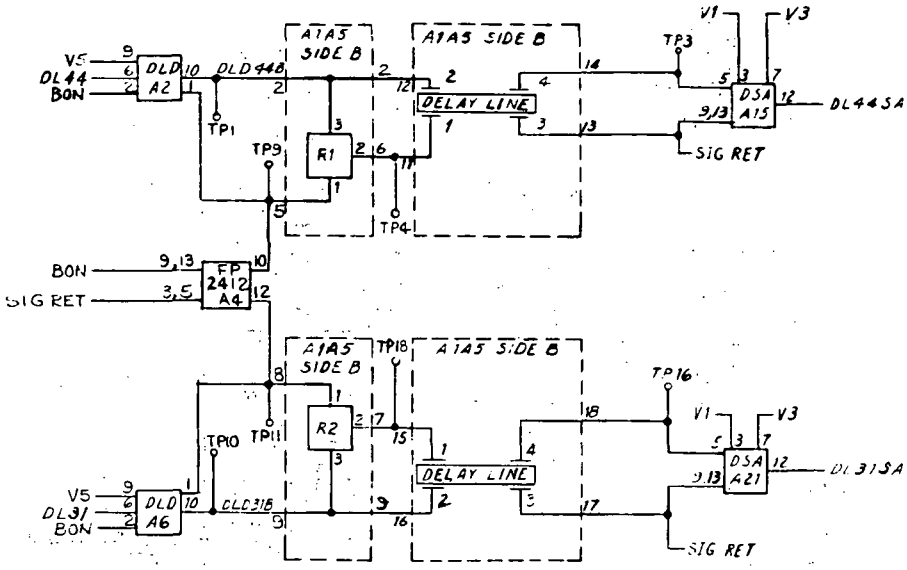


Figure 10-3. Delay Lines, Logic Diagram (Sheet 1 of 2)

A1A5A



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	WN	51	ZN
3	SIG RET	53	PR
5	MRON	55	NU
7	MRO	57	A10N
9		59	XN
11		61	NUN
13	V3	63	
15		65	Z2
17	ACCON	67	Y8
19	YN	69	X3
21		71	A10
23	PQR	73	W7
25		75	
27	ACCO	77	
29	MDON	79	
31	V1	81	
33	STP	83	MDO
35		85	STPN
37		87	DL31
39	PQRN	89	DL44
41	PRN	91	
43		93	
45		95	BON
47		97	V5
49			

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A5A

Figure 10-3. Delay Lines, Logic Diagram (Sheet 2)

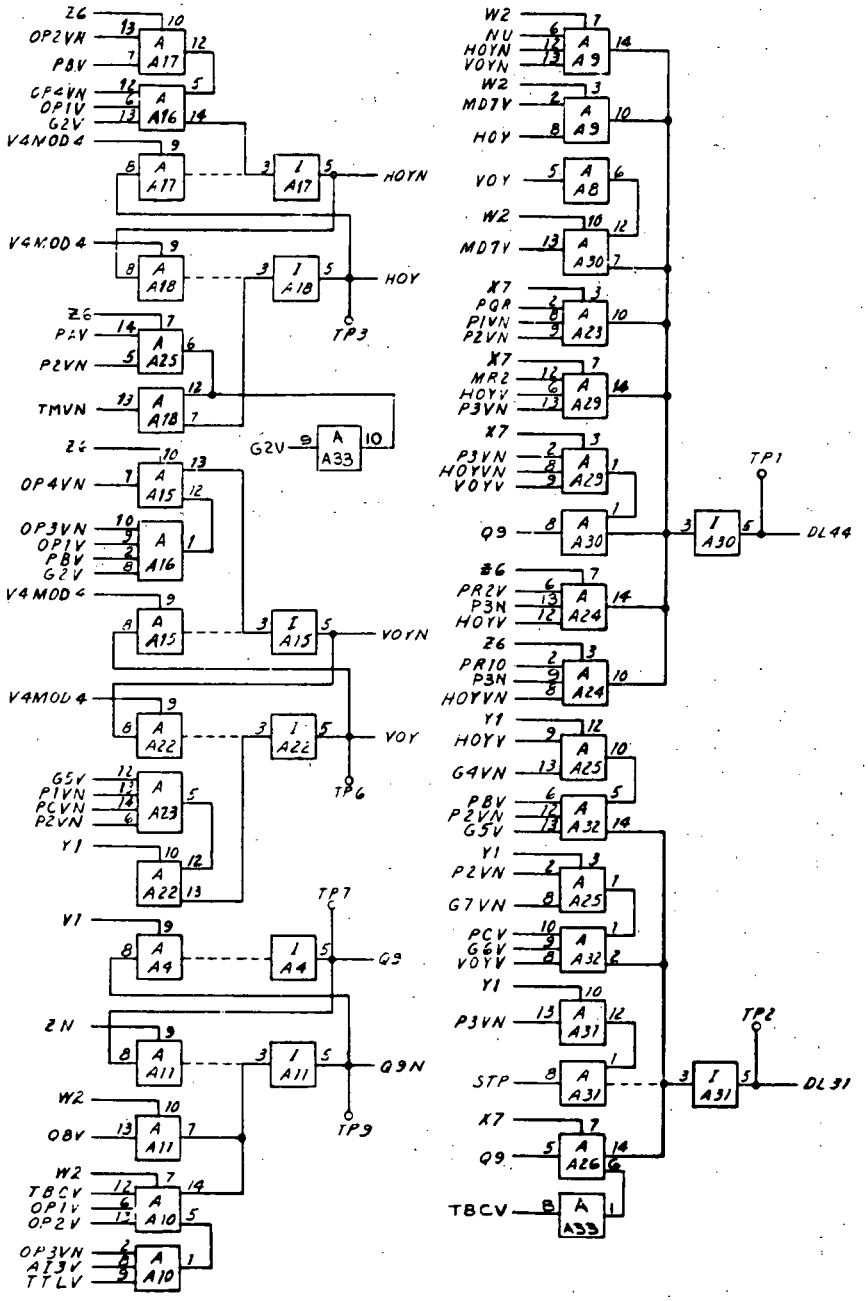
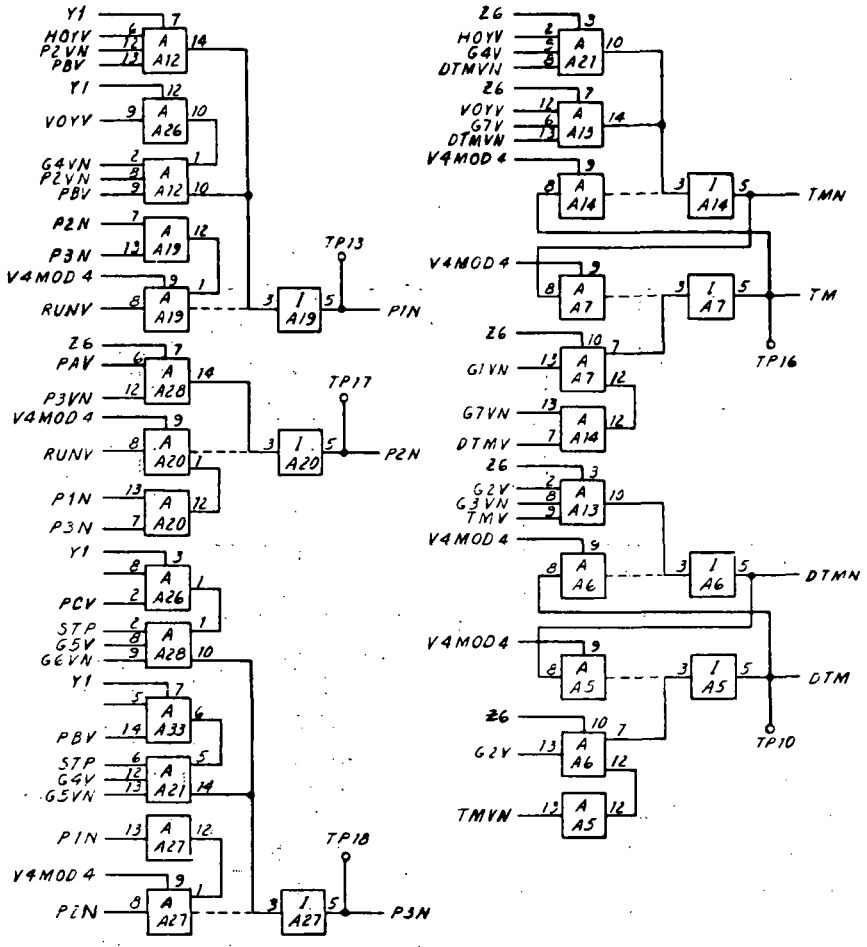


Figure 10-4. Multiply-Divide Element, Logic Diagram (Sheet 1 of 12)



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	OP1V	51	G7VN
3	P1VN	53	Q8V
5	PCVN	55	DTMN
7	VOYN	57	RUNV
9	VOY	59	VOYV
11	MR2	61	PBV
13	V1	63	G4VN
15	OP4VN	65	P3N
17	DL44	67	TMVN
19	G2V	69	DTM
21	PR10	71	TMV
23	PQR	73	G3VN
25	MD7V	75	P2N
27	TTLV	77	P1N
29	A13V	79	G7V
31	DL31	81	G1VN
33	STP	83	TM
35	PR2V	85	PAV
37	HOY	87	G6VN
39	OP3VN	89	G4V
41	OP2VN	91	DTMVN
43	HOYN	93	DTMV
45	G6V	95	TMN
47	PCV	97	G5VN
49	ZN		

THRU PINS			
Pin	Signal	Pin	Signal
1	SIG RET	16	V3
2	HOYVN	17	G5V
3	W2	18	NU
4	OP2V	19	
5		20	V1
6	TBCV	21	V4MOD4
7		22	
8		23	P3VN
9	P2VN	24	G4VN
10	DTMVN	25	HOYV
11	G2V	26	
12		27	G3VN
13		28	TMVN
14		29	Z6
15	G7VN	30	X7

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A7A

Figure 10-4. Multiply-Divide Element, Logic Diagram (Sheet 2)

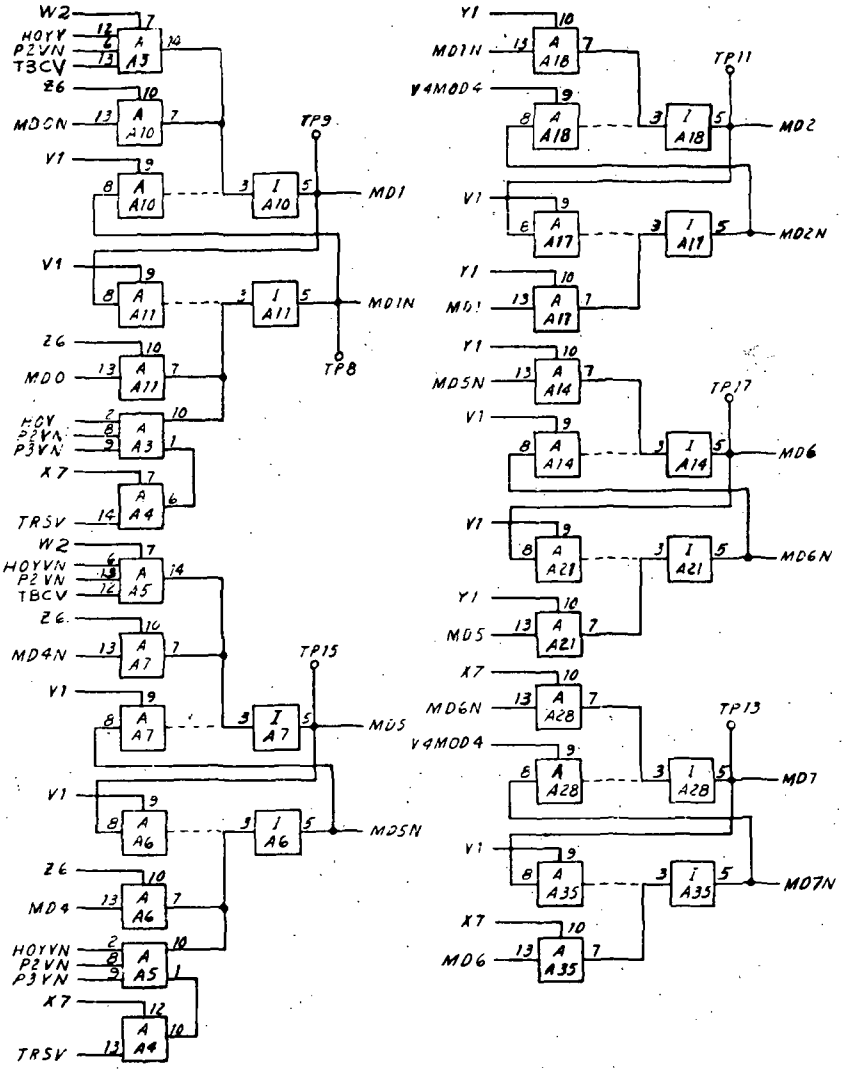
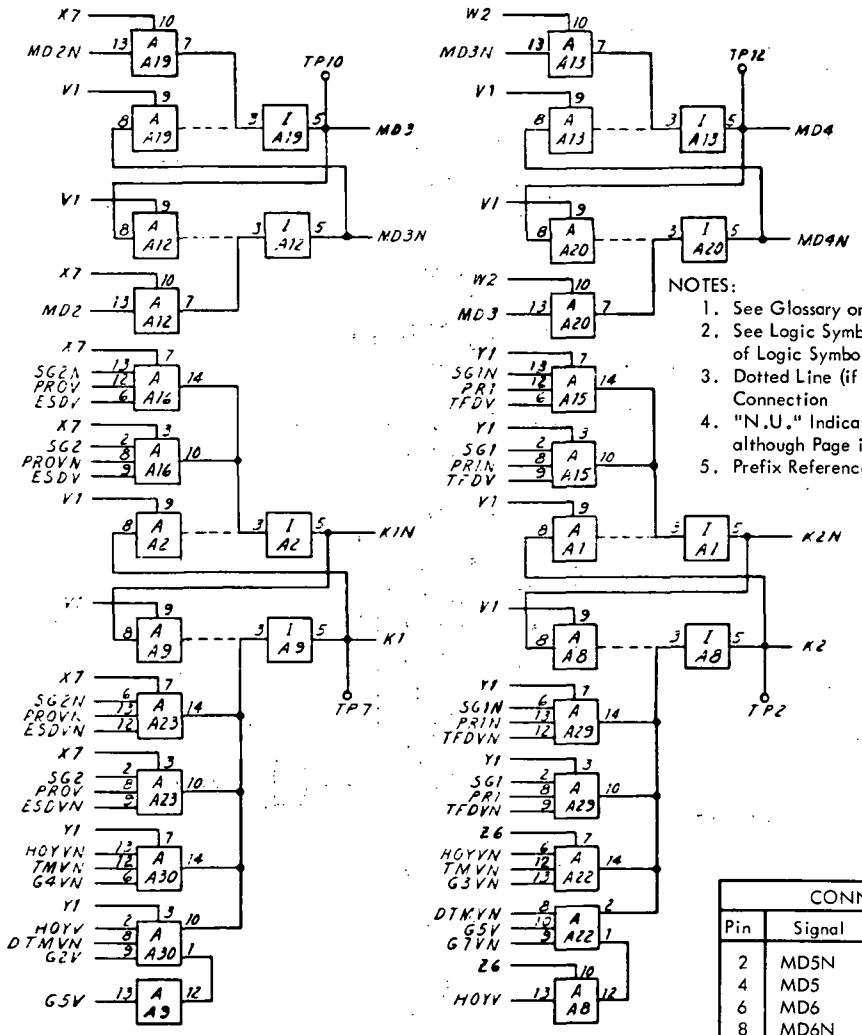


Figure 10-4. Multiply-Divide Element, Logic Diagram (Sheet 3)



A1A7B

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A7B

THRU PINS			
Pin	Signal	Pin	Signal
1	SIG RET	16	V3
2	HOYVN	17	G5V
3	W2	18	NU
4	OP2V	19	
5		20	V1
6	TBCV	21	V4MOD4
7		22	
8		23	P3VN
9	P2VN	24	G4VN
10	DTMVN	25	HOYV
11	G2V	26	
12		27	G3VN
13		28	TMVN
14		29	Z6
15	G7VN	30	X7

CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	MD5N	52	Z6
4	MD5	54	MD2N
6	MD6	56	TBCV
8	MD6N	58	MDON
10	MD7N	60	K1
12	X7	62	K1N
14	MD7	64	K2N
16	MD4N	66	P2VN
18	MD3	68	P3VN
20	V4MOD4	70	K2
22	V3	72	HOYVN
24	SIG RET	74	SG2N
26	NU	76	SG2
28		78	HOYV
30	MD4	80	PROVN
32	MD2	82	PROV
34	W2	84	ESDV
36		86	ESDVN
38	OP2V	88	SG1N
40	MD3N	90	PR1N
42	TRSV	92	TFDVN
44	MD0	94	PR1
46	V1	96	SG1
48	V1	98	TFDV
50	G5V		

Figure 10-4. Multiply-Divide Element, Logic Diagram (Sheet 4)

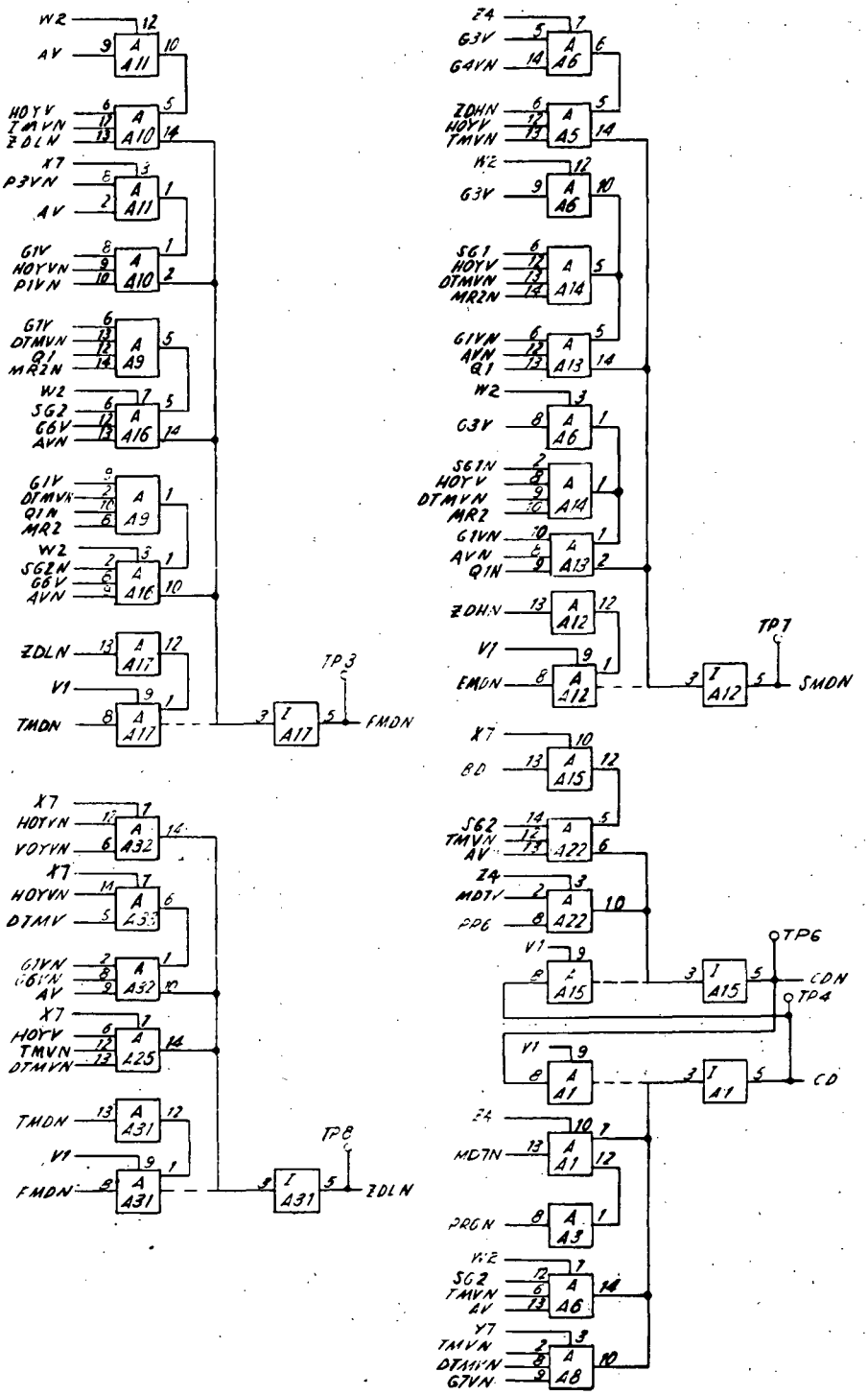


Figure 10-4. Multiply-Divide Element; Logic Diagram (Sheet 5)

A1A8A

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U. Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A8A

CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	MR2N	51	
3	MD7N	53	
5	PR6	55	X7
7	G6V	57	W2
9	Y7	59	
11	MR2	61	
13	VOYVN	63	G3V
15	HOYV	65	Z4
17	AV	67	TMVN
19	G2V	69	P3VN
21		71	
23	G7VN	73	HOYVN
25	MD7V	75	G4V
27	SG2N	77	G1V
29	SG2	79	G1V
31	Q1	81	G1VN
33	PR6N	83	AVN
35	P1VN	85	Q1N
37		87	G6VN
39		89	G4VN
41		91	DTMVN
43		93	DTMV
45		95	SG1
47		97	SG1N
49			

THRU PINS			
Pin	Signal	Pin	Signal
1	SIG RET	16	V3
2		17	ZDHN
3	EMDN	18	VOYV
4	SMDN	19	PR6
5	FMDN	20	ZDLN
6	HOYVN	21	TMDN
7	G2VN	22	G1YN
8	CDN	23	G7V
9	G6VN	24	G7VN
10	HOYV	25	G2V
11	TMVN	26	DTMVN
12	CD	27	DTMV
13	G6V	28	V1
14	PR6N	29	Y7
15	G5V	30	G1V

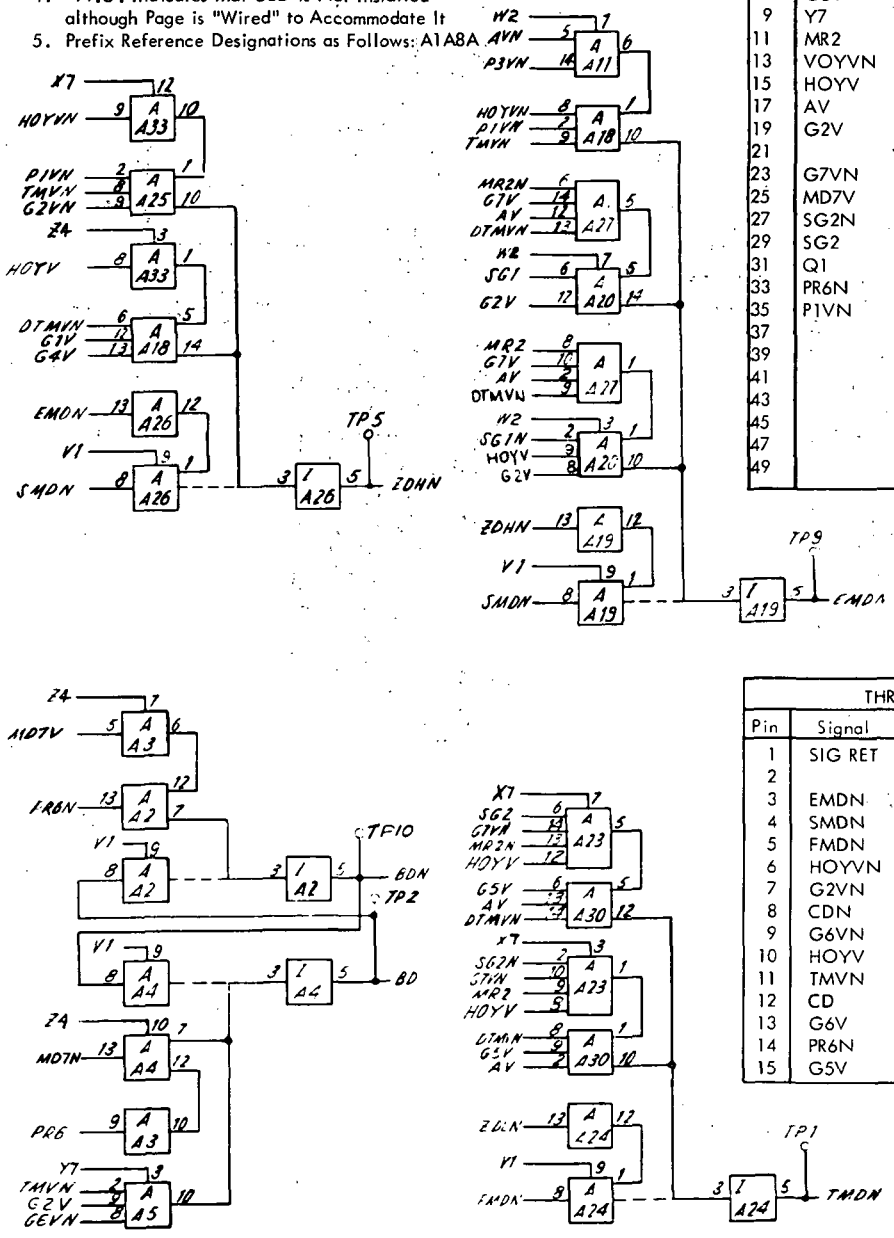


Figure 10-4. Multiply-Divide Element, Logic Diagram (Sheet 6)

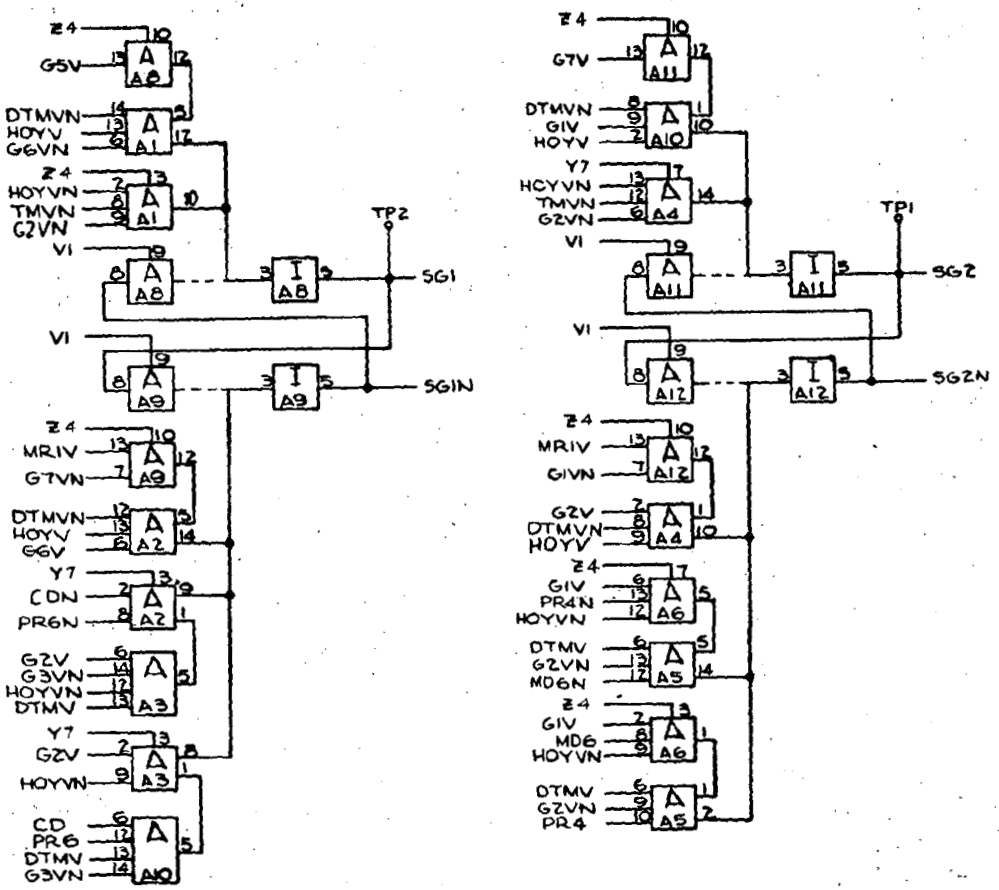
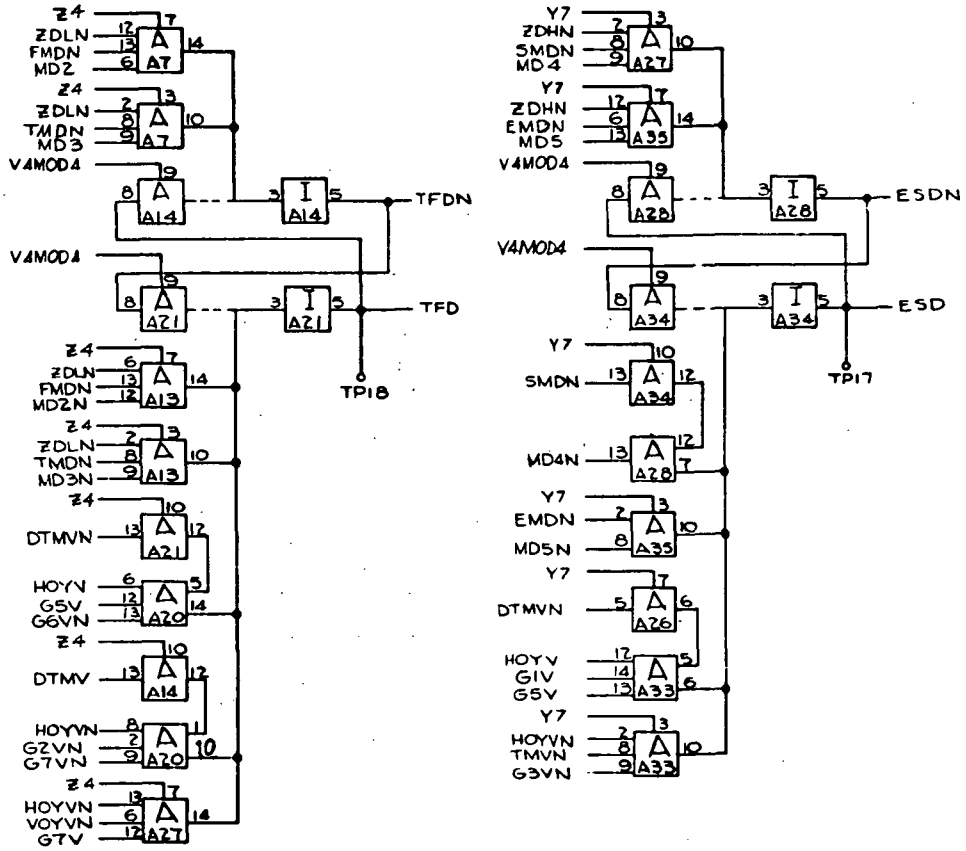


Figure 10-4. Multiply-Divide Element, Logic Diagram (Sheet 7)



CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	TFD	50	G5V
4	MD4N	52	MR1V
6	MD5	54	
8		56	MD6N
10	MD5N	58	PR4
12	TFDN	60	
14	MD2	62	
16	ESD	64	
18	MD3	66	
20	V4MOD4	68	
22	V3	70	
24	PR4N	72	
26	ESDN	74	SG2N
28	SIG RET	76	SG2
30	MD4	78	
32		80	
34		82	Z4
36		84	
38	MD2N	86	
40	MD3N	88	SG1N
42	MD6	90	
44		92	
46	G3VN	94	
48	V1	96	SG1
		98	G2VN

THRU PINS			
Pin	Signal	Pin	Signal
1	SIG RET	16	V3
2		17	ZDHN
3	EMDN	18	VOYVN
4	SMDN	19	PR6
5	FMDN	20	ZDLN
6	HOYVN	21	TMDN
7	G2VN	22	G1VN
8	CDN	23	G7V
9	GGVN	24	G7VN
10	HOYV	25	G2V
11	TMVN	26	DTMVN
12	CD	27	DTMV
13	G6V	28	V1
14	PR6N	29	Y7
15	G5V	30	G1V

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A8B

Figure 10-4. Multiply-Divide Element, Logic Diagram (Sheet 8)

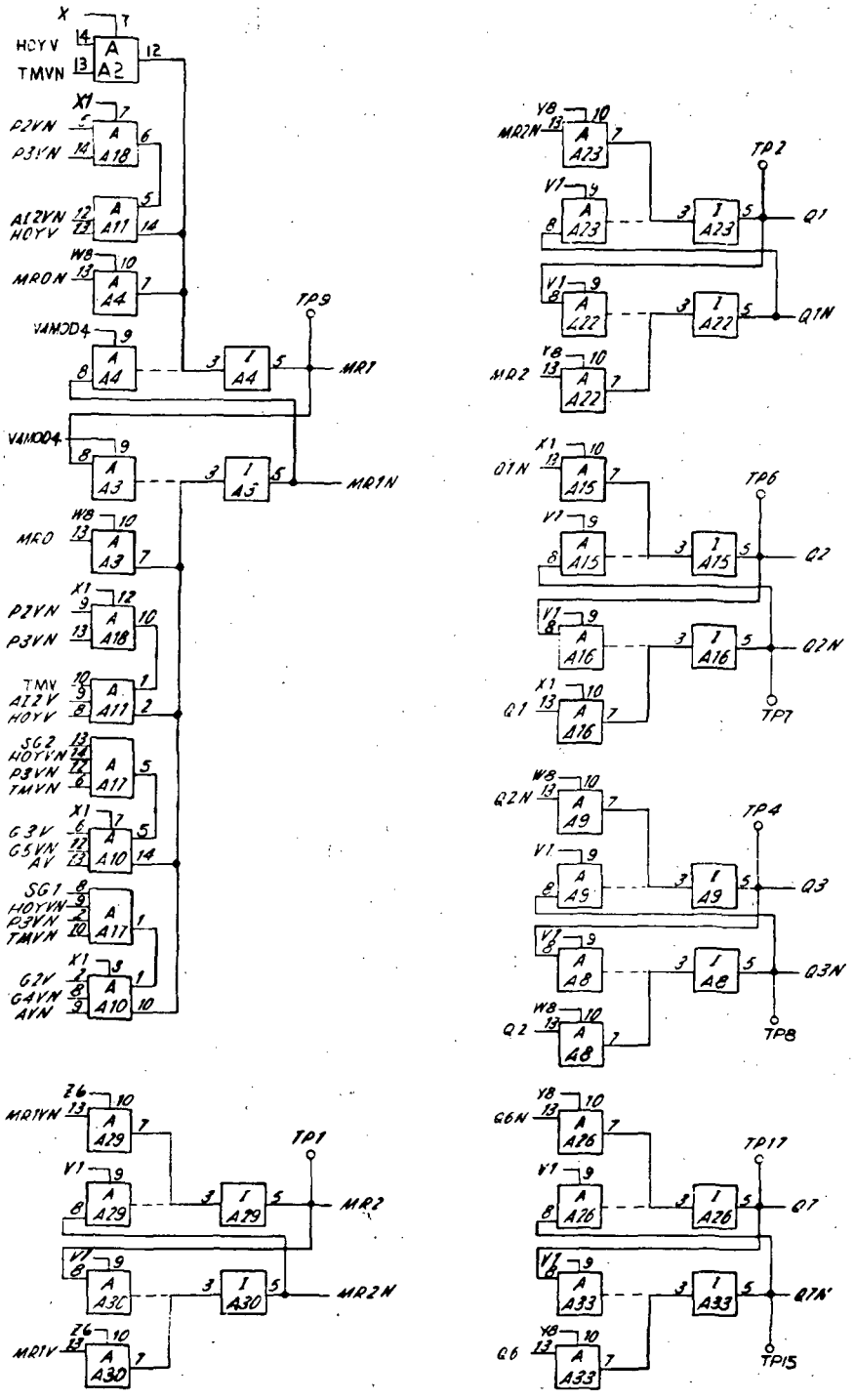
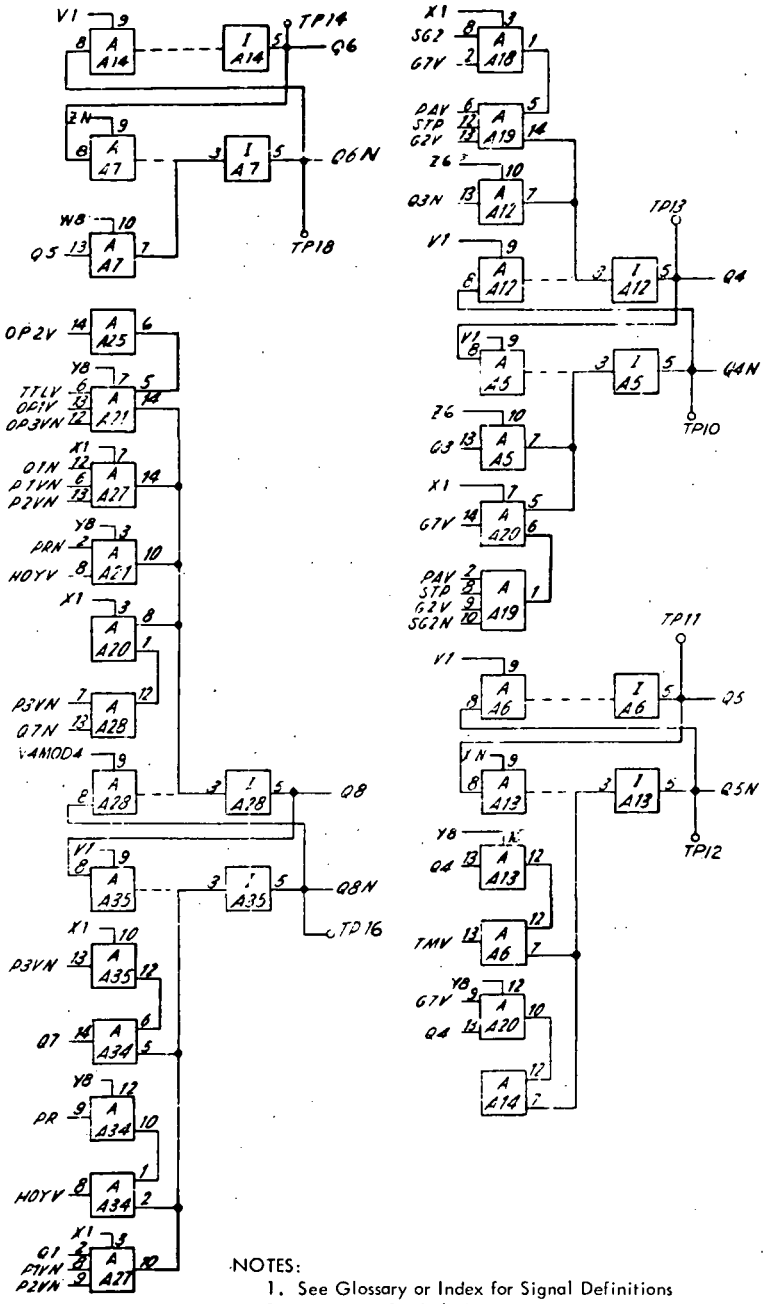


Figure 10-4. Multiply-Divide Element, Logic Diagram (Sheet 9)



THRU PINS			
Pin	Signal	Pin	Signal
1	HOYVN	16	TMVN
2		17	G4VN
3	Z6	18	W8
4	Y8	19	
5	X1	20	
6	P2VN	21	
7		22	V4MOD4
8	ZN	23	SIG RET
9	V1	24	V3
10		25	P3VN
11		26	
12		27	
13		28	
14		29	PR
15	PRN	30	TMV

CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	MR1	51	MR1V
3	MR2N	53	G7V
5	MRO	55	
7	MRON	57	PAV
9	AI2V	59	MR1N
11	MR2	61	XN
13	MR1VN	63	
15	HOYV	65	
17		67	
19		69	
21	V3	71	
23	SIG RET	73	SG2N
25	AI2VN	75	
27	TTLV	77	AVN
29	SG2	79	Q1N
31	Q1	81	V4MOD4
33	STP	83	Q8
35	AV	85	OP1V
37		87	G5VN
39	OP3VN	89	G3V
41	P1VN	91	
43		93	
45		95	SG1
47	V1	97	G2V
49	OP2V		

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate it
5. Prefix Reference Designations as Follows: A1A9A

Figure 10-4. Multiply-Divide Element, Logic Diagram (Sheet 10)

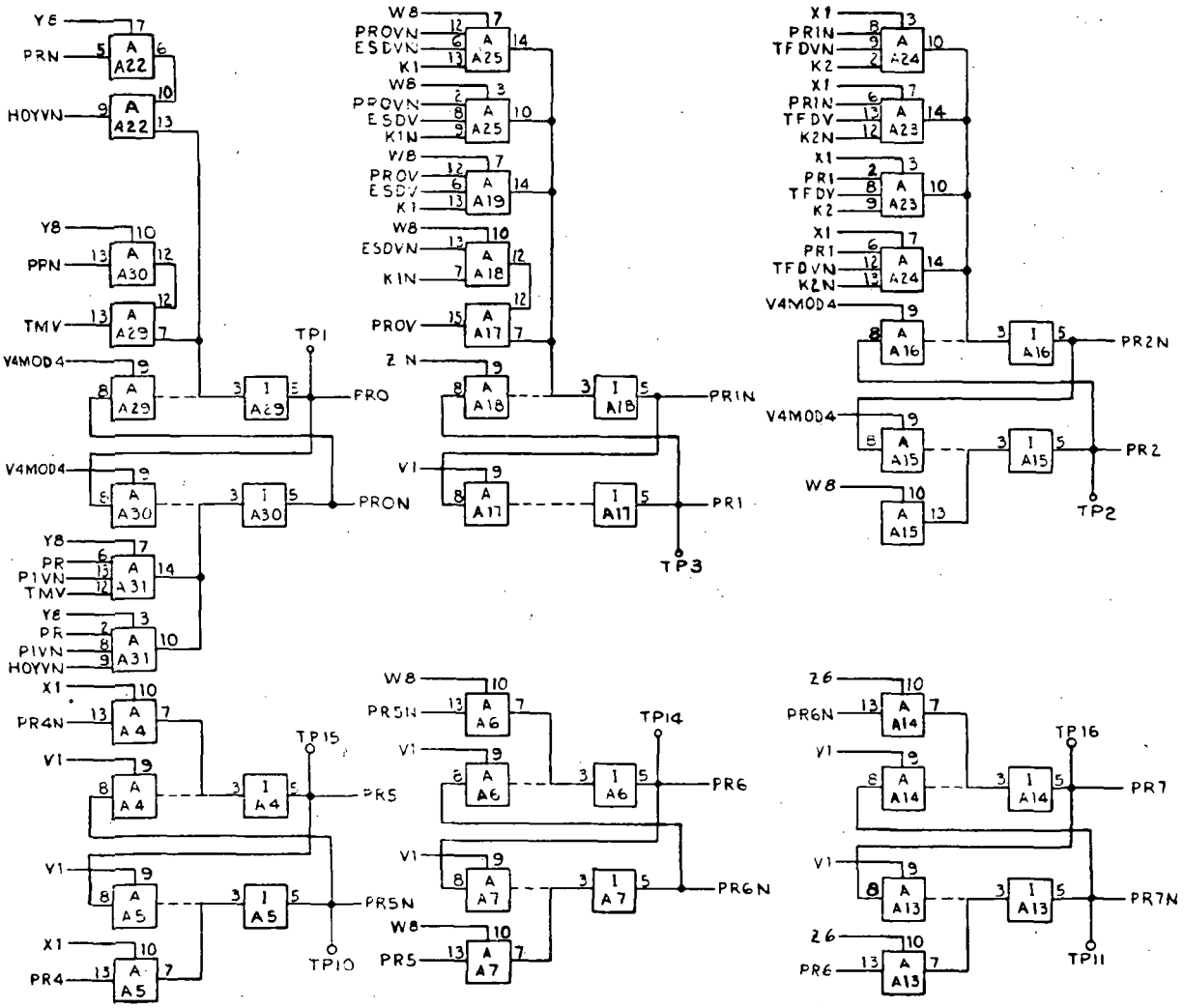
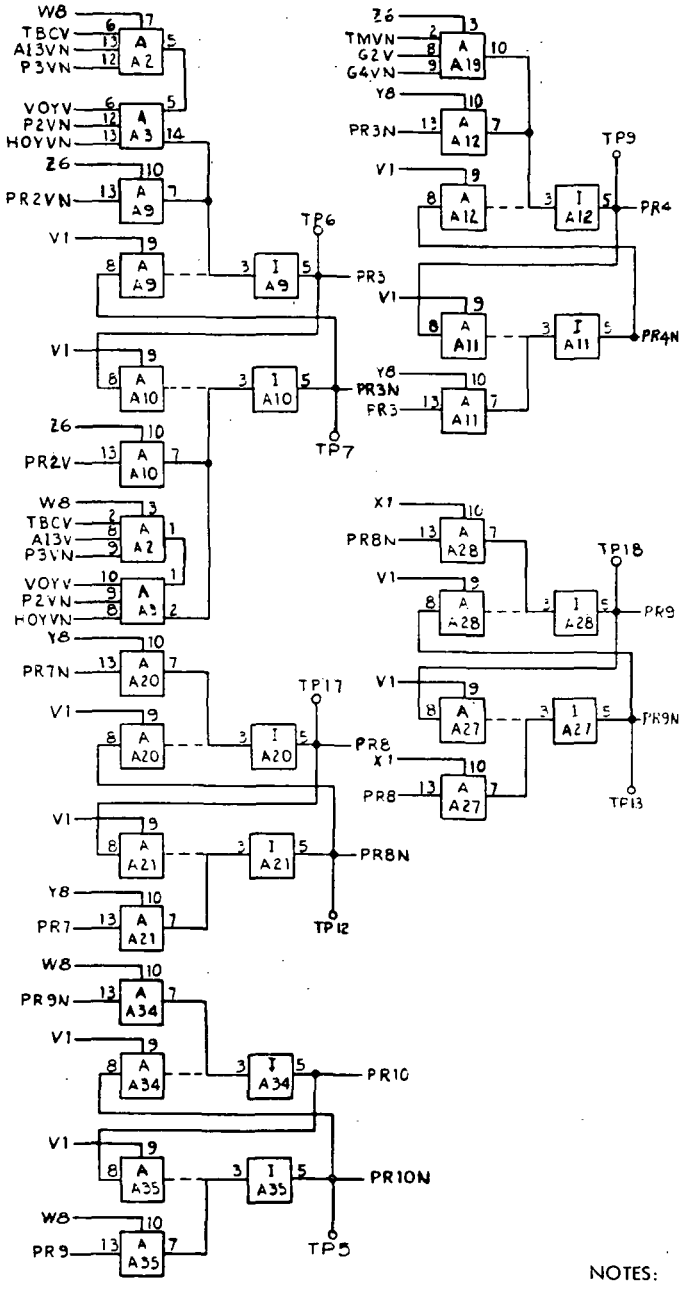


Figure 10-4. Multiply-Divide Element, Logic Diagram (Sheet 11)

A1A9B



THRU PINS			
Pin	Signal	Pin	Signal
1	HOYVN	16	TMVN
2		17	G4VN
3	Z6	18	W8
4	Y8	19	
5	X1	20	
6	P2VN	21	
7		22	V4MOD4
8	ZN	23	SIG RET
9	V1	24	V3
10		25	P3VN
11		26	
12		27	
13		28	
14		29	PR
15	PRN	30	TMV

CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	Z6	52	VOYV
4	Y8	54	PR
6	PR6	56	TBCV
8		58	P1VN
10		60	K1
12		62	K1N
14	PR10	64	K2N
16	X1	66	P2VN
18	PR6N	68	P3VN
20		70	K2
22	PR4N	72	HOYVN
24		74	PRN
26	PR4	76	PRO
28		78	A13V
30		80	PROVN
32	PR1N	82	PROV
34	W8	84	ESDV
36	PR2	86	ESDVN
38	PR1	88	TMV
40	G2V	90	PR2V
42	TMVN	92	TFDVN
44	G4VN	94	PR2VN
46	ZN	96	A13VN
48	PR2N	98	TFDV
50	PRON		

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotten Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A9B

Figure 10-4. Multiply-Divide Element, Logic Diagram (Sheet 12)

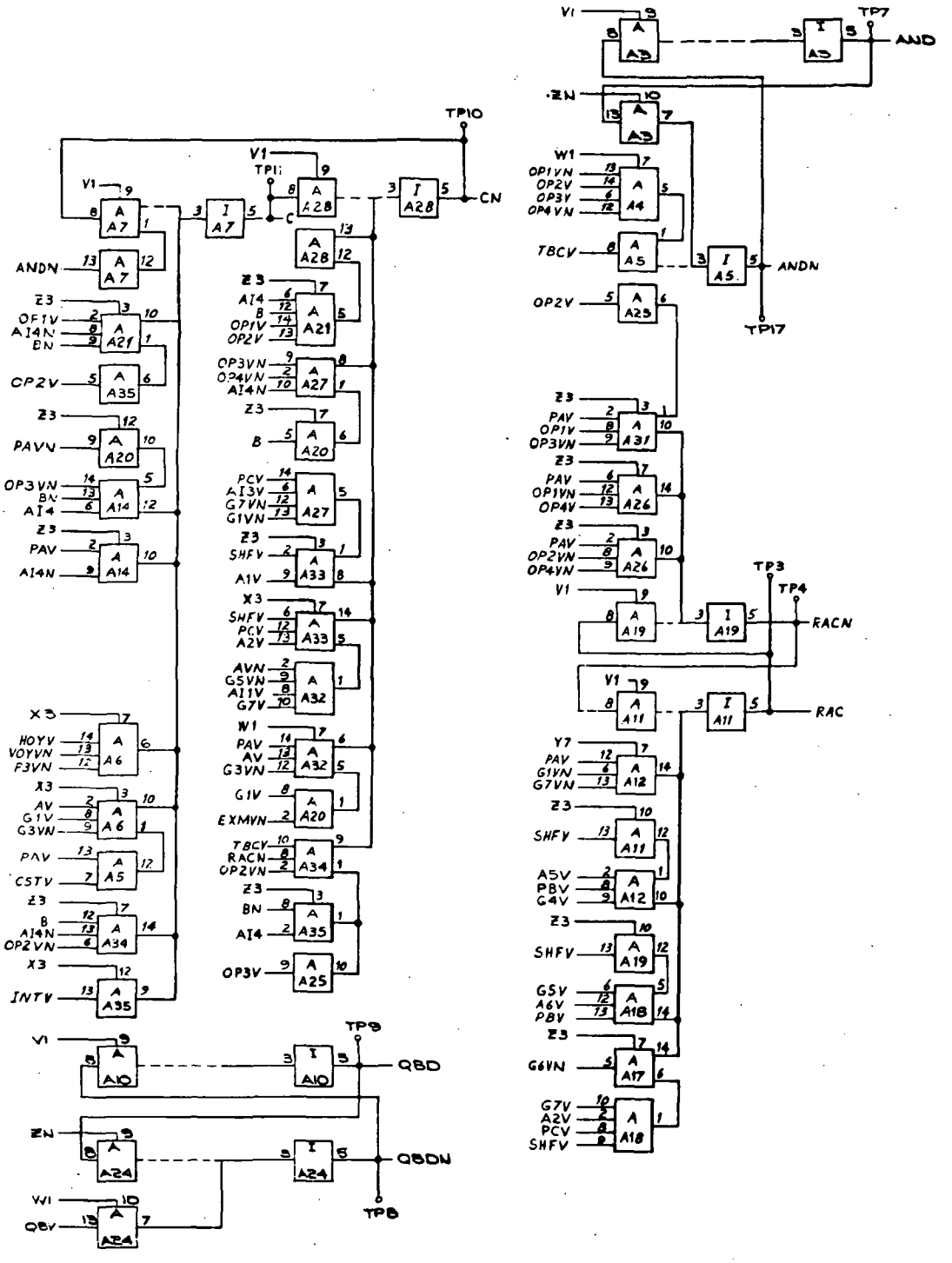
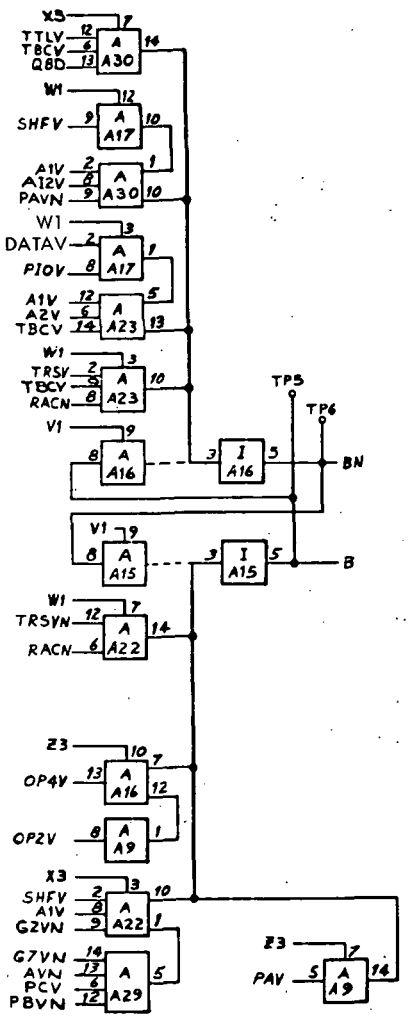
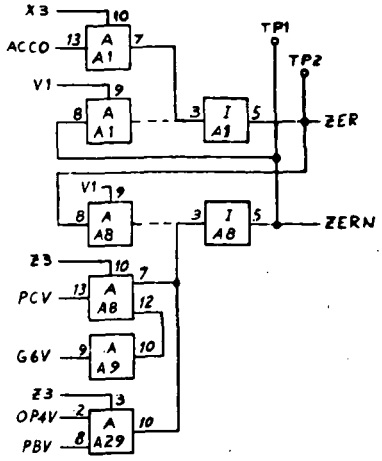


Figure 10-5. Add-Subtract Element, Logic Diagram (Sheet 1 of 4)



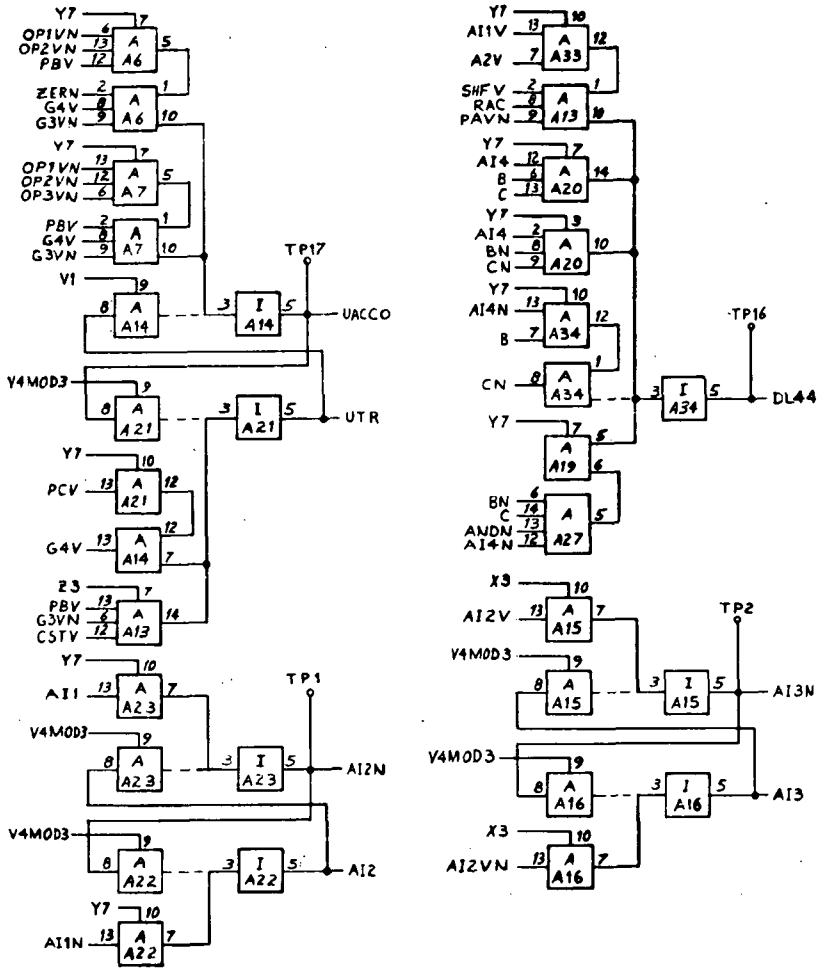


CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	SIG RET	51	PBVN
3	V3	53	OP3V
5	PBV	55	CSTV
7	AVN	57	G4V$_2$
9	TRSVN	59	A5V
11	G6V	61	SHFV
13	TRSV	63	A6V
15	A2V	65	Z3
17	A12V	67	G7VN
19	TBCV	69	PCV
21	TTLV	71	OP4VN
23	Q8V	73	G5V
25	OP4V	75	V7
27	IOREG	77	INTV
29	PIOV	79	G1VN
31	G2VN	81	P3VN
33	W1	83	AV
35	G1V	85	HOYV
37	G6VN	87	VOYVN
39	X3	89	EXMVN
41	V1	91	OP1V
43	ZN	93	
45	G5VN	95	OP3VN
47	G7V	97	G3VN
49	PAV		

THRU PINS			
Pin	Signal	Pin	Signal
1	ZERN	16	ACCO
2	A1V	17	G6VN
3	A11V	18	RAC
4	G4V	19	PAVN
5		20	OP1VN
6	OP2VN	21	
7	CSTV	22	OP2V
8	ANDN	23	A13V
9	A14N	24	C
10	A14	25	CN
11	OP4V	26	OP3VN
12	PCV	27	B
13	BN	28	G3VN
14	TBCV	29	
15		30	G5VN

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A10A

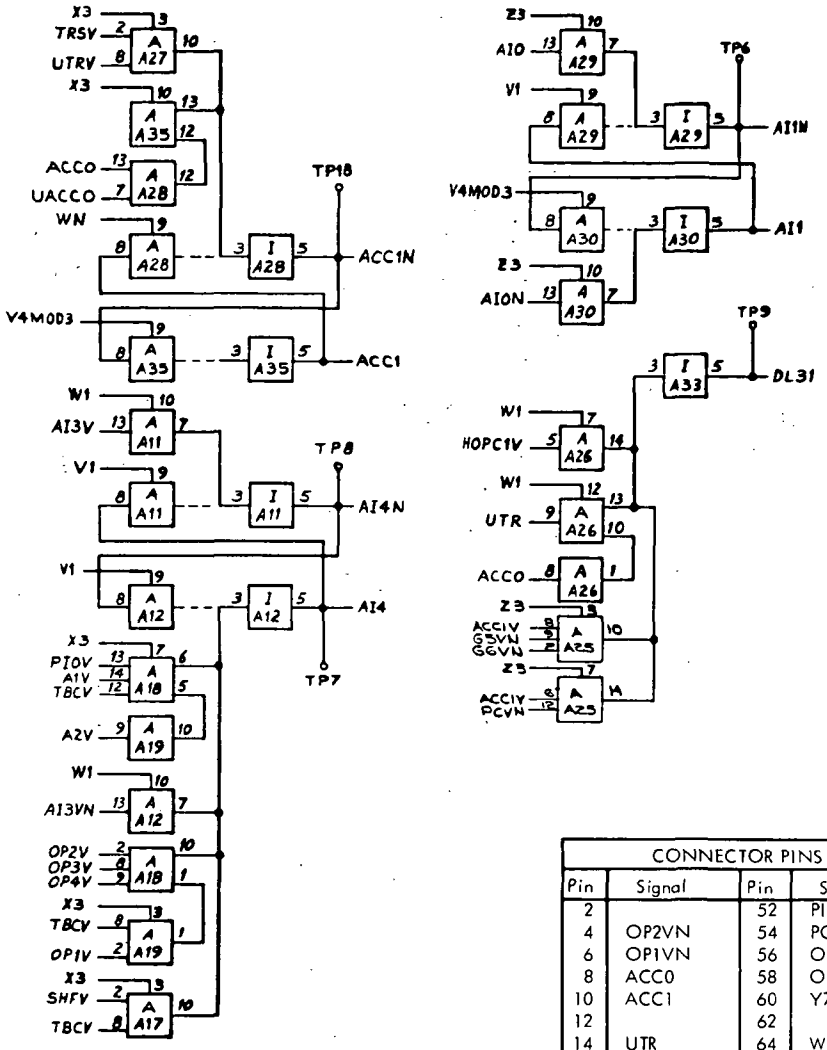
Figure 10-5. Add-Subtract Element, Logic Diagram (Sheet 2)



NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A10B

Figure 10-5. Add-Subtract Element, Logic Diagram (Sheet 3)



THRU PINS			
Pin	Signal	Pin	Signal
1	ZERN	16	ACC0
2	A1V	17	G6VN
3	AI1V	18	RAC
4	G4V	19	PAVN
5		20	OP1VN
6	OP2VN	21	
7	CSTV	22	OP2V
8	ANDN	23	A13V
9	AI4N	24	C
10	AI4	25	CN
11	OP4V	26	OP3VN
12	PCV	27	B
13	BN	28	G3VN
14	TBCV	29	
15		30	G5VN

CONNECTOR PINS			
Pin	Signal	Pin	Signal
2		52	PIOV
4	OP2VN	54	PCVN
6	OP1VN	56	OP2V
8	ACC0	58	OP3V
10	ACC1	60	Y7
12		62	
14	UTR	64	W1
16	DL44	66	
18	PBV	68	V1
20	SHFV	70	X3
22	AI4N	72	AI0N
24	TRSV	74	Z3
26		76	V4MOD3
28	PAVN	78	AI2VN
30	AI1V	80	AI1N
32	UTRV	82	AI2
34	HOPC1V	84	AI3N
36	DL31	86	AI2N
38	ACC1V	88	AI0
40	WN	90	AI2V
42	A1V	92	AI3
44	A2V	94	AI1
46	AI3VN	96	SIG RET
48	OP1V	98	-3VDC (V3)
50	AI3V		

Figure 10-5. Add-Subtract Element, Logic Diagram (Sheet 4)

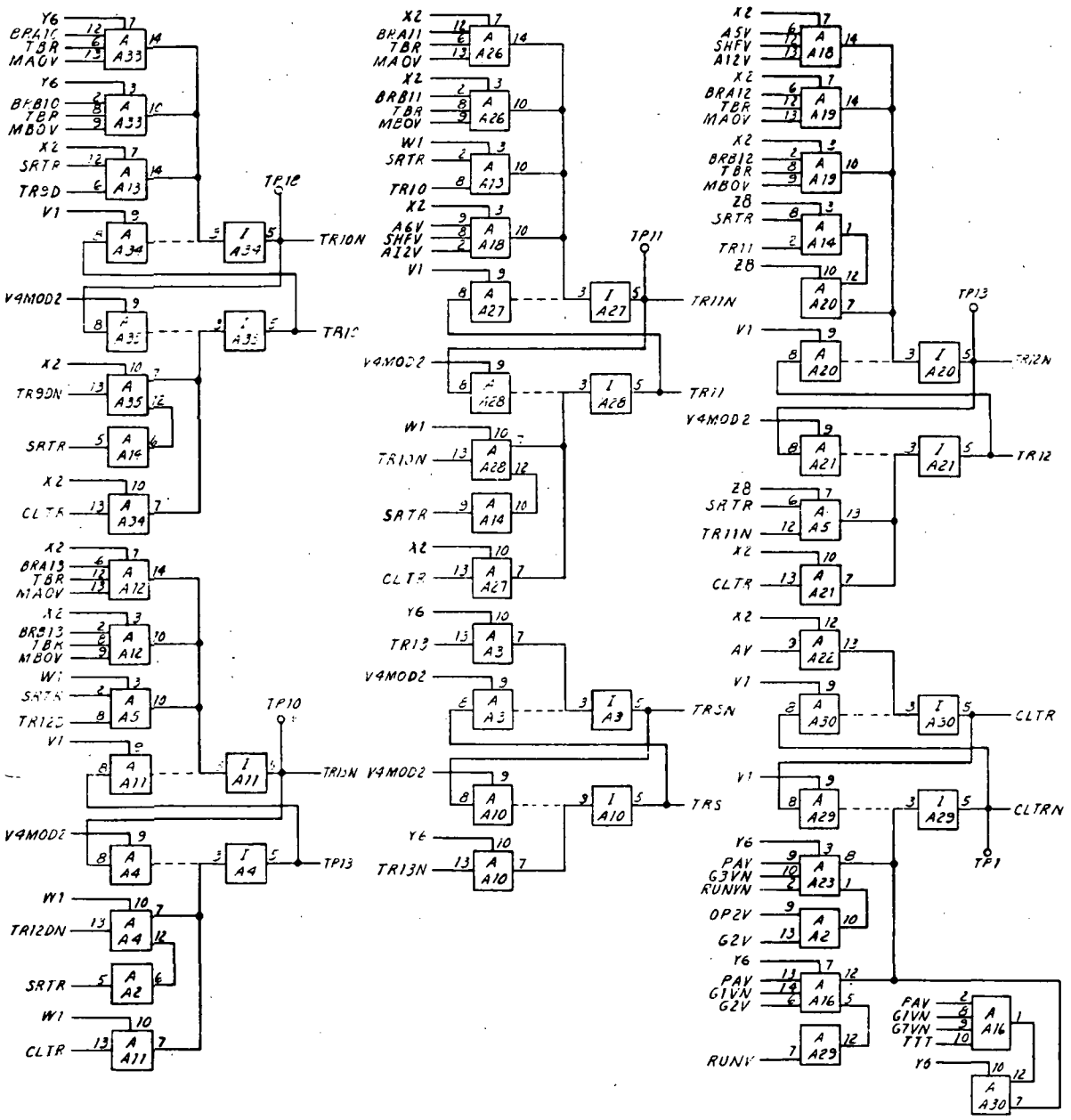


Figure 10-6. Transfer Register Bits 10-TRS and Control, Logic Diagram (Sheet 1 of 2)

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A11A

A1A11A

CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	G3V	51	A12V
3	RUNV	53	BRB11
5	RUNVN	55	A5V
7	G3VN	57	BRB13
9		59	MBOV
11	Y6	61	BRB10
13		63	BRA10
15	OP2V	65	BRA11
17		67	MAOV
19		69	BRA13
21		71	
23	EXMVN	73	TR10
25		75	BRB12
27	CLTR	77	BRA12
29	G2VN	79	TR12
31	TRSN	81	TR9D
33	HOPV	83	
35		85	
37		87	
39	TRS	89	X2
41	SHFV	91	TR9DN
43		93	TR11
45		95	
47	TR13	97	
49	A6V		

THRU PINS			
Pin	Signal	Pin	Signal
1	SIG RET	16	V3
2	AV	17	G5V
3	G7V	18	TTT
4		19	PBV
5	PAV	20	G7VN
6	G1V	21	STO
7	G1VN	22	G2V
8	PCVN	23	V1
9	SRTR	24	X2
10	TBR	25	V4MOD2
11	W1	26	Z8
12		27	PCV
13		28	CDS
14		29	G6VN
15		30	

Figure 10-6. Transfer Register Bits 10-TRS and Control, Logic Diagram (Sheet 2)

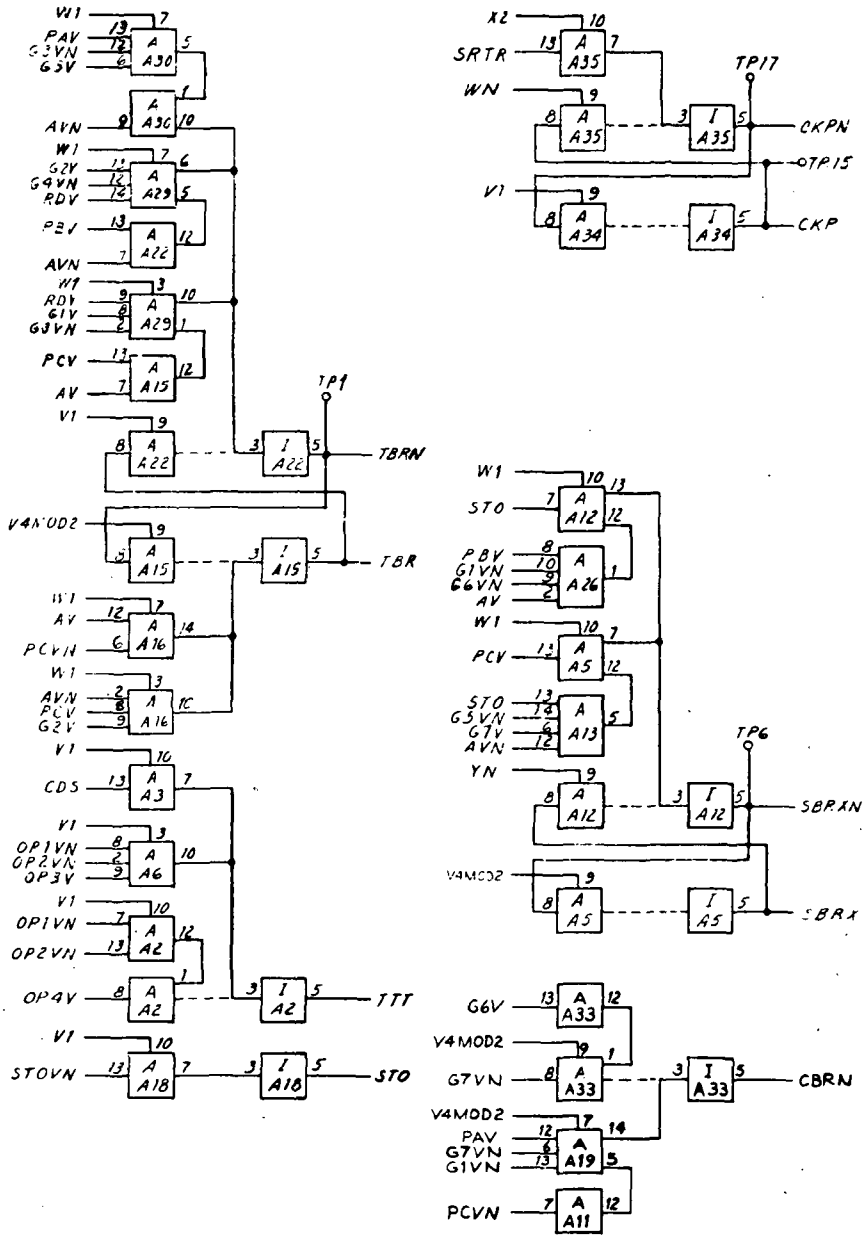
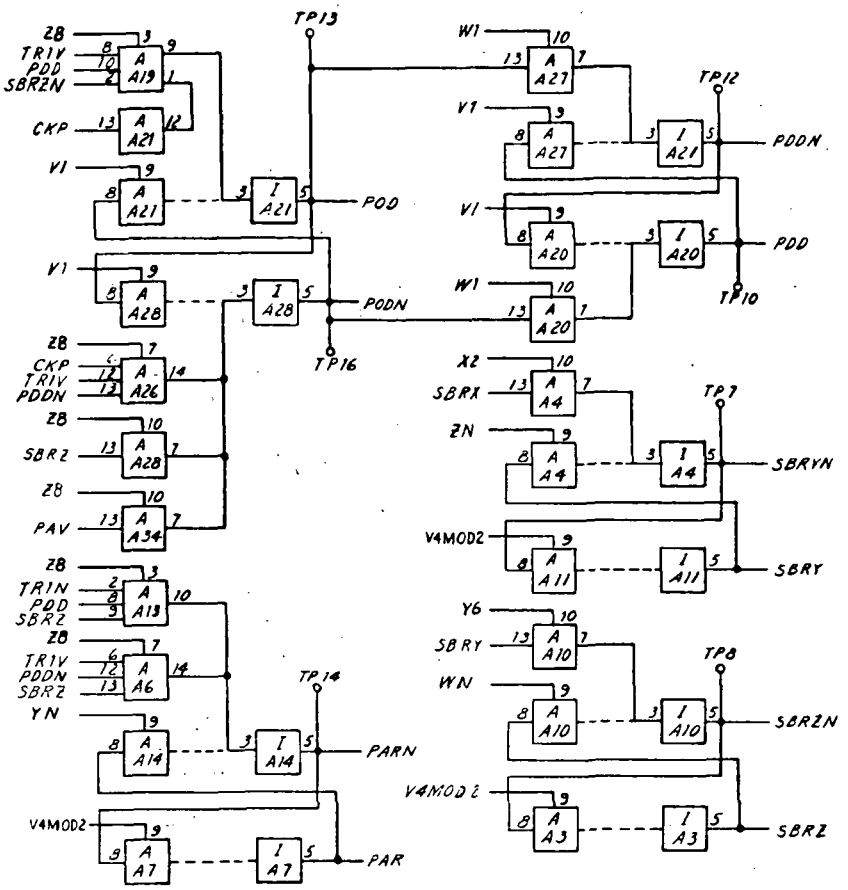


Figure 10-7. Memory Buffer Control and Parity Counter, Logic Diagram (Sheet 1 of 2)



CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	OP2VN	52	V1
4	OP1VN	54	ZN
6	SRTR	56	TTT
8	SBRZ	58	SBRY
10	PAR	60	STO
12	TR1N	62	CDS
14	OP3V	64	
16	G7V	66	Y6
18	PAV	68	W1
20	V3	70	G5V
22	SIG RET	72	PCVN
24	Z8	74	OP4V
26	YN	76	G2V
28	G5VN	78	
30	G1VN	80	
32	G6V	82	AVN
34	CBRN	84	PBV
36	V4MOD2	86	RDV
38	TR1V	88	G4VN
40	G7VN	90	G3VN
42	AV	92	
44	STOVN	94	TBR
46	G6VN	96	G1V
48	SBRX	98	PCV
50	WN		

THRU PINS			
Pin	Signal	Pin	Signal
1	SIG RET	16	V3
2	AV	17	G5V
3	G7V	18	TTT
4		19	PBV
5	PAV	20	G7VN
6	G1V	21	STO
7	G1VN	22	G2V
8	PCVN	23	V1
9	SRTR	24	X2
10	TBR	25	V4MOD2
11	W1	26	Z8
12		27	PCV
13		28	CDS
14		29	G6VN
15		30	

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A11B

Figure 10-7. Memory Buffer Control and Parity Counter, Logic Diagram (Sheet 2)

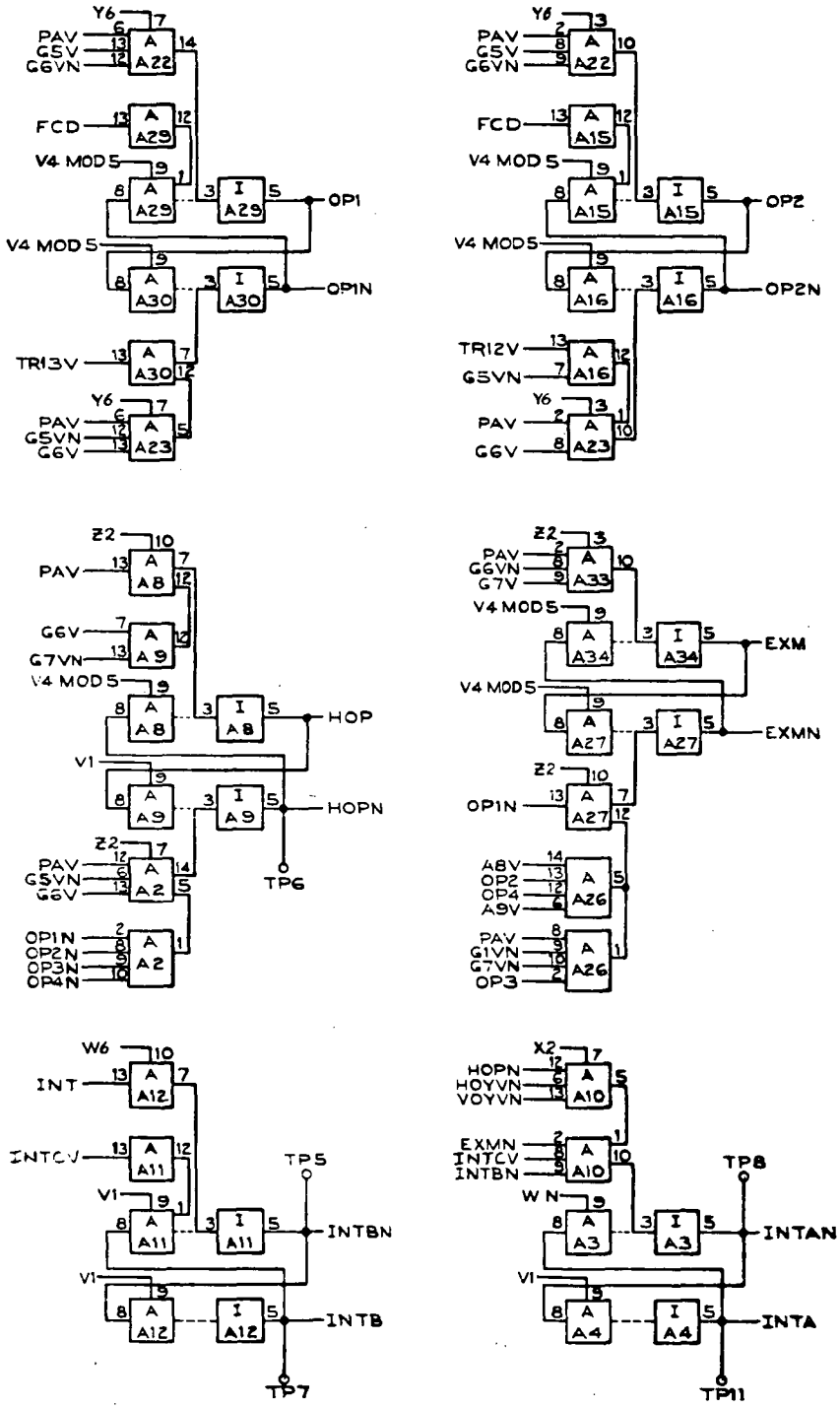
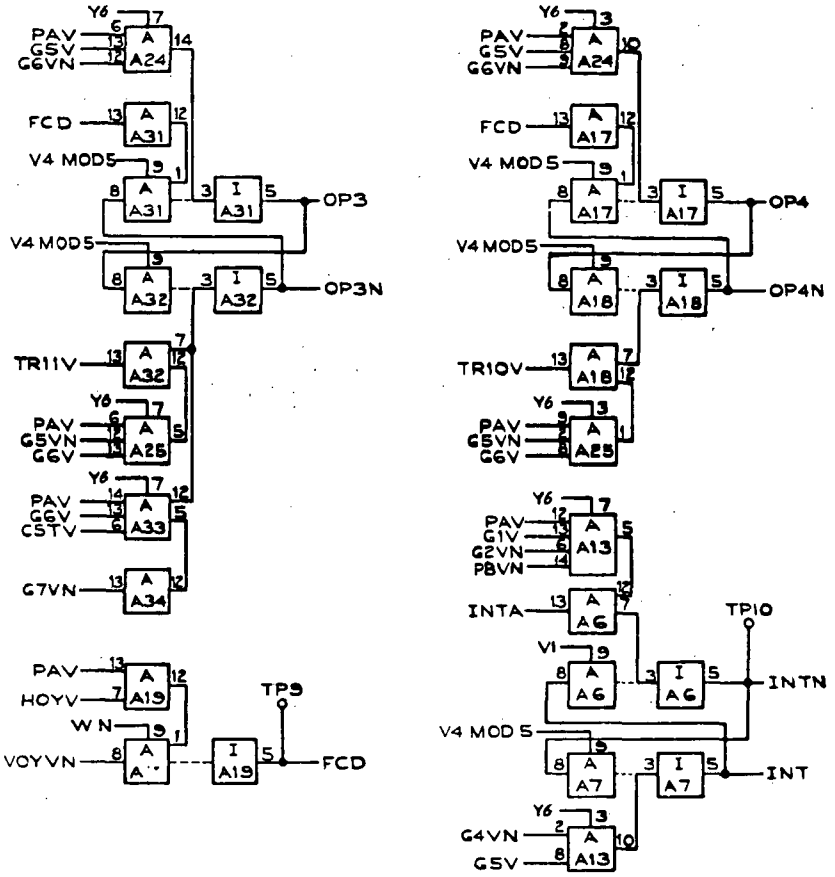


Figure 10-8. Operation Code Register, Logic Diagram (Sheet 1 of 4)



THRU PINS			
Pin	Signal	Pin	Signal
1	OP3N	16	FCD
2	OP1	17	PAV
3		18	G6V
4		19	
5		20	
6		21	G5V
7		22	G6VN
8		23	
9		24	A9V
10		25	A8V
11		26	
12		27	
13		28	G5VN
14		29	OP1N
15		30	

CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	HOP	51	OP4
3	OP2N	53	Y6
5	OP1N	55	TR11V
7	HOYVN	57	OP2
9	SIG RET	59	TR10V
11	V3	61	Z2
13	V1	63	G1V
15		65	VOYVN
17	TR12V	67	G2VN
19	V4MOD5	69	CSTV
21	OP1	71	HOYV
23	G1VN	73	EXMN
25	G4VN	75	
27	TR13V	77	
29	G7V	79	
31	WN	81	
33	OP3N	83	
35	W6	85	
37	X2	87	
39	OP3	89	
41	OP4N	91	EXM
43	INTCV	93	
45	G7VN	95	PBVN
47		97	INT
49			

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A12A

Figure 10-8. Operation Code Register, Logic Diagram (Sheet 2)

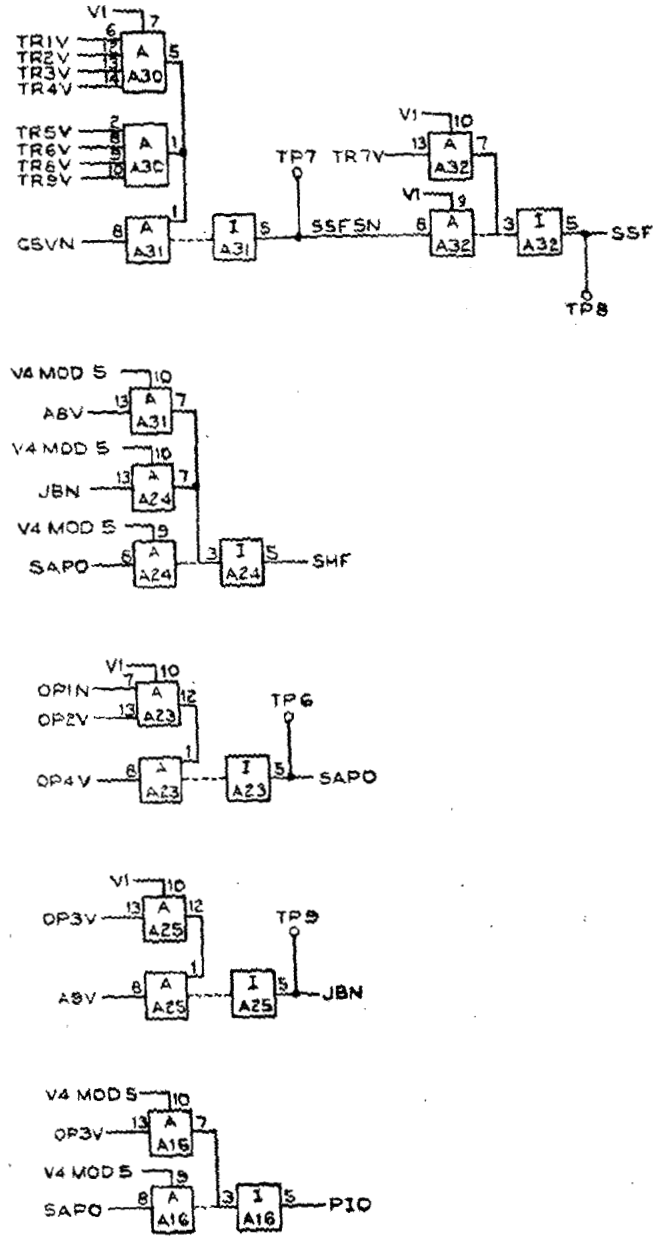
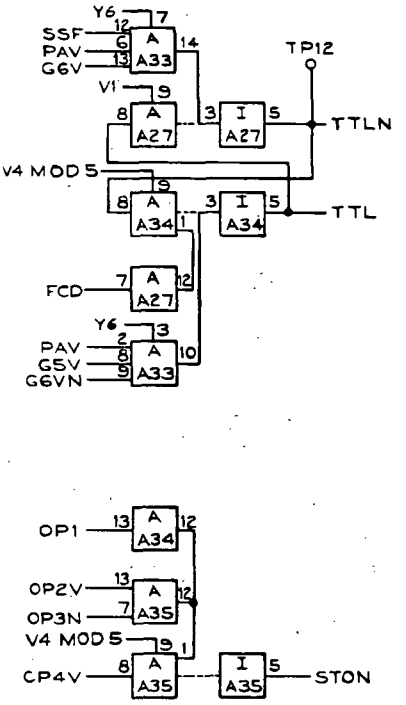


Figure 10-8. Operation Code Register, Logic Diagram (Sheet 3)

A1A12B



CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	STON	52	
4	OP2V	54	Y6
6	A8V	56	A9V
8	OP4V	58	
10	SIG RET	60	TR5V
12	V3	62	
14	V1	64	
16	PAV	66	TR1V
18	TTL	68	SHF
20	V4MOD5	70	TR6V
22	G5VN	72	
24	TR8V	74	
26		76	
28	G5V	78	
30		80	TR2V
32		82	TR7V
34	G6V	84	G6VN
36		86	
38		88	
40	TR9V	90	
42	OP3V	92	PIO
44	TR4V	94	
46	TR3V	96	
48		98	
50			

THRU PINS			
Pin	Signal	Pin	Signal
1	OP3N	16	FCD
2	OP1	17	PAV
3		18	G6V
4		19	
5		20	
6		21	G5V
7		22	G6VN
8		23	
9		24	A9V
10		25	A8V
11		26	
12		27	
13		28	G5VN
14		29	OP1N
15		30	

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U. Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A12B

Figure 10-8. Operation Code Register, Logic Diagram (Sheet 4)

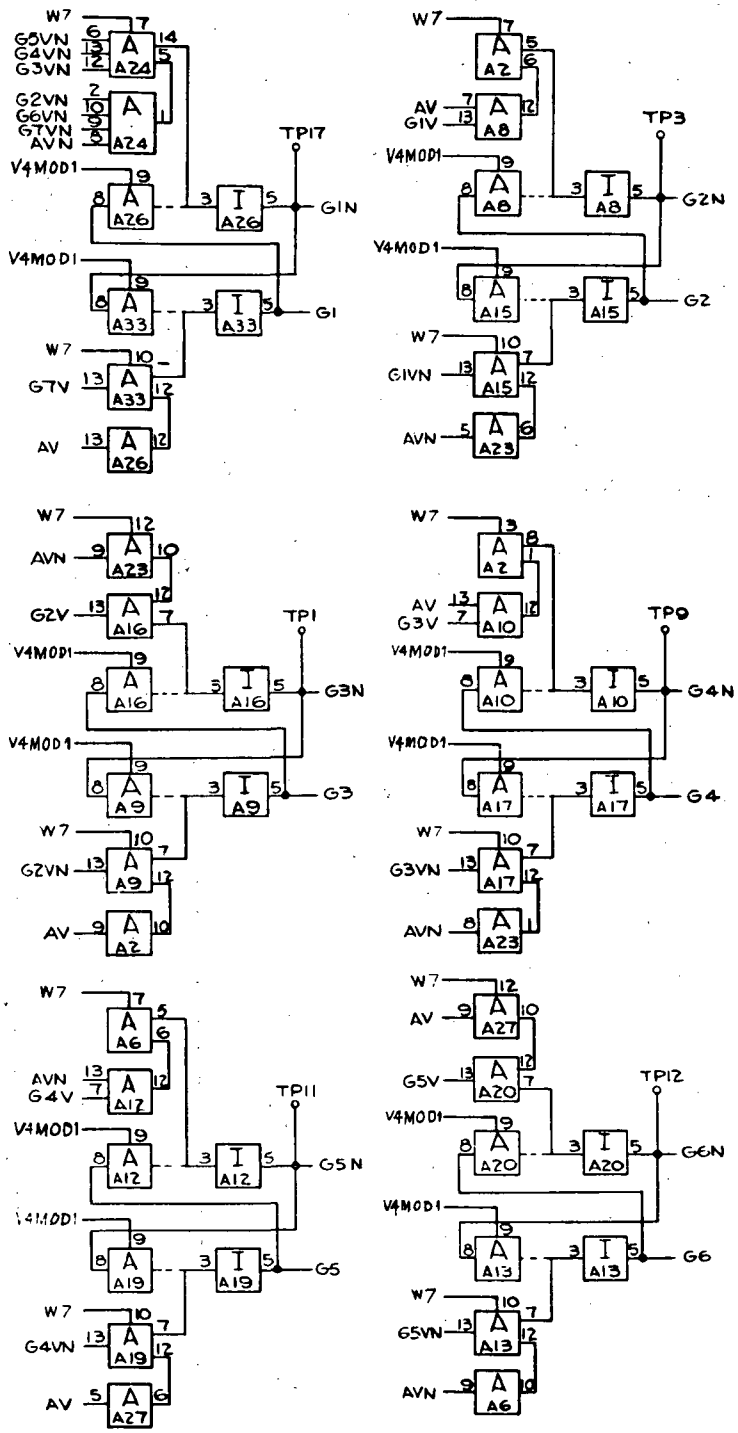
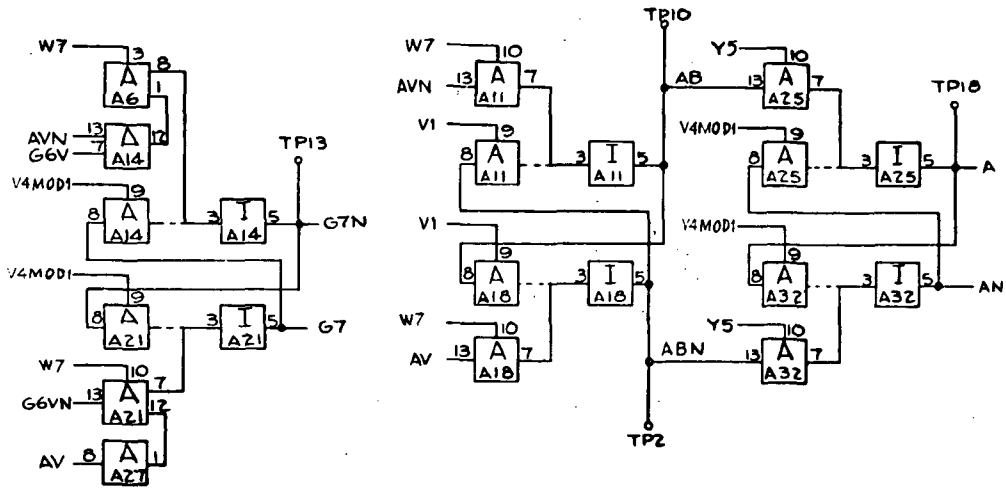


Figure 10-9. Timing Gate Generator, Logic Diagram (Sheet 1 of 2)

A1A13A



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1		51	
3	G2	53	
5	G2N	55	AN
7		57	G5N
9		59	
11	G1VN	61	G1N
13		63	
15	G3N	65	G7V
17	G3	67	G1
19		69	G5
21		71	G4V
23		73	G6
25		75	
27	G2V	77	
29	G4N	79	AV
31	G3VN	81	G5V
33		83	G6N
35		85	G7N
37	G6VN	87	
39	G4	89	
41	G4VN	91	
43	G5VN	93	
45	A	95	G7
47		97	G6V
49			

THRU PINS			
Pin	Signal	Pin	Signal
1	G1V	16	G2VN
2	G7VN	17	G3V
3		18	AVN
4		19	
5		20	
6		21	V1
7		22	W7
8		23	
9		24	
10	V3	25	V4MOD1
11		26	
12		27	SIG RET
13		28	
14		29	
15		30	Y5

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A13A

Figure 10-9. Timing Gate Generator, Logic Diagram (Sheet 2)

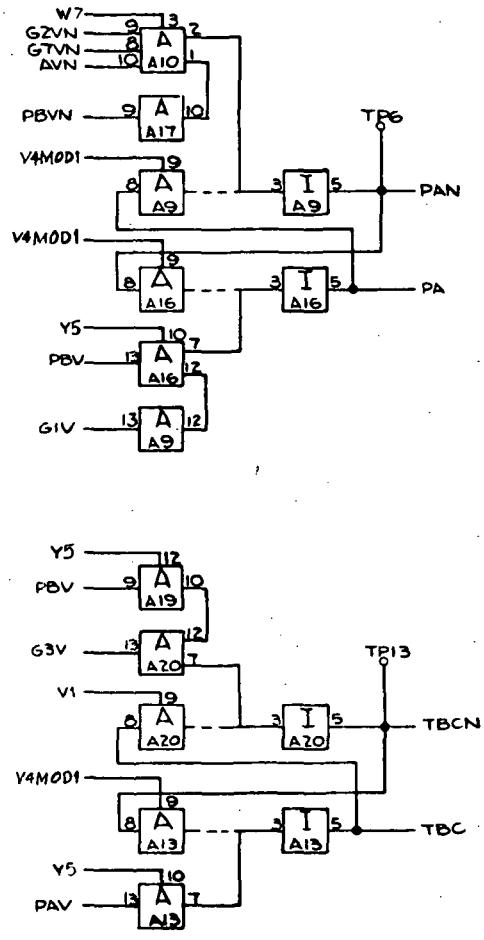
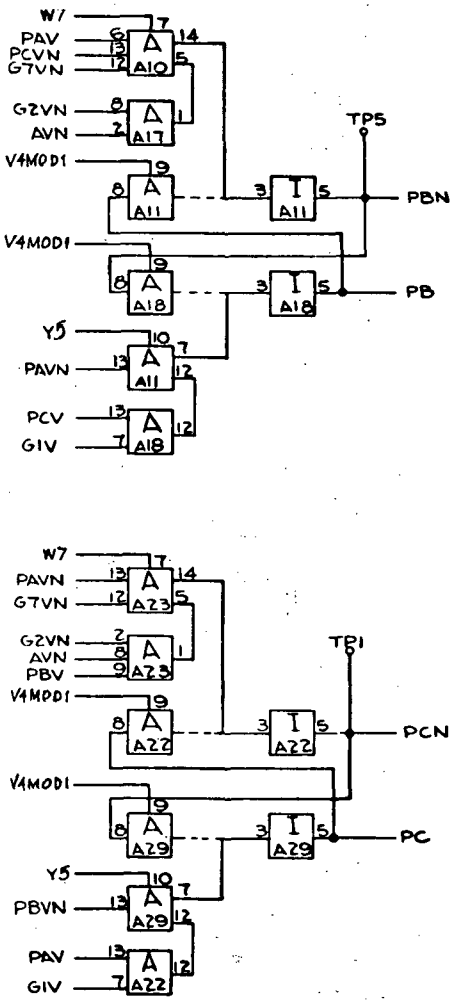


Figure 10-10. Phase Generator, Logic Diagram (Sheet 1 of 2)



CONNECTOR PINS			
Pin	Signal	Pin	Signal
2		52	
4		54	V1
6		56	PBN
8		58	PCVN
10		60	
12		62	
14	W7	64	
16	PAV	66	
18	G3V	68	
20		70	PA
22		72	G2VN
24		74	G7VN
26		76	
28		78	V3
30	TBC	80	SIG RET
32		82	AVN
34		84	PBV
36		86	PAN
38		88	G1V
40		90	PBVN
42	PAVN	92	Y5
44	PB	94	PCN
46	PCV	96	V4MOD1
48		98	PC
50			

A1A13B

THRU PINS			
Pin	Signal	Pin	Signal
1	G1V	16	G2VN
2	G7VN	17	G3V
3		18	AVN
4		19	
5		20	
6		21	V1
7		22	W7
8		23	
9		24	
10	V3	25	V4MOD1
11		26	
12		27	SIG RET
13		28	
14		29	
15		30	Y5

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate it
5. Prefix Reference Designations as Follows: A1A13B

Figure 10-10. Phase Generator, Logic Diagram (Sheet 2)

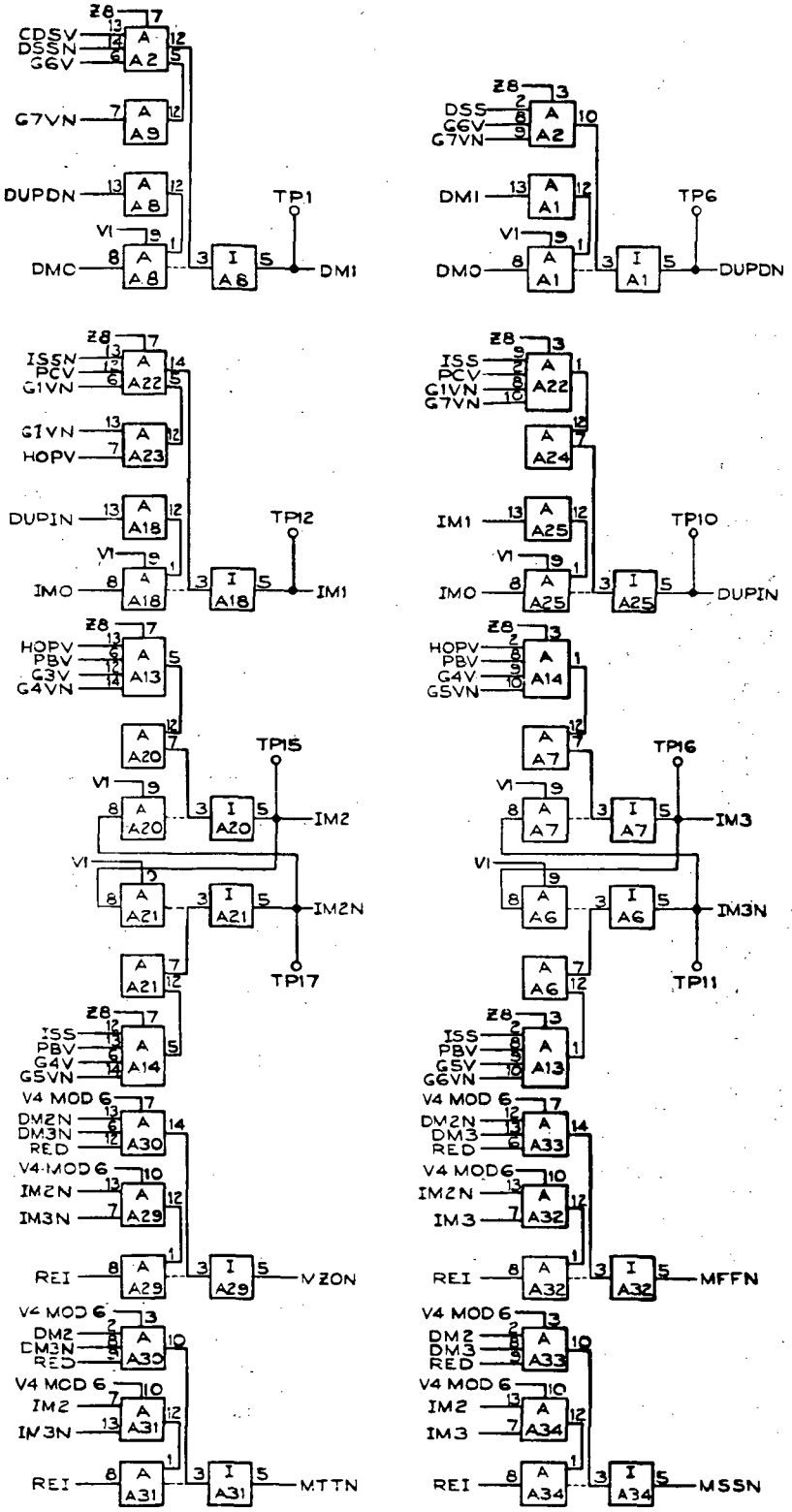
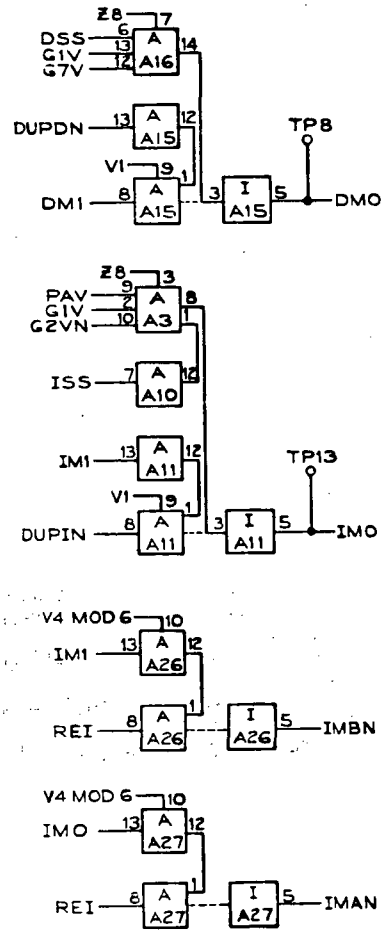
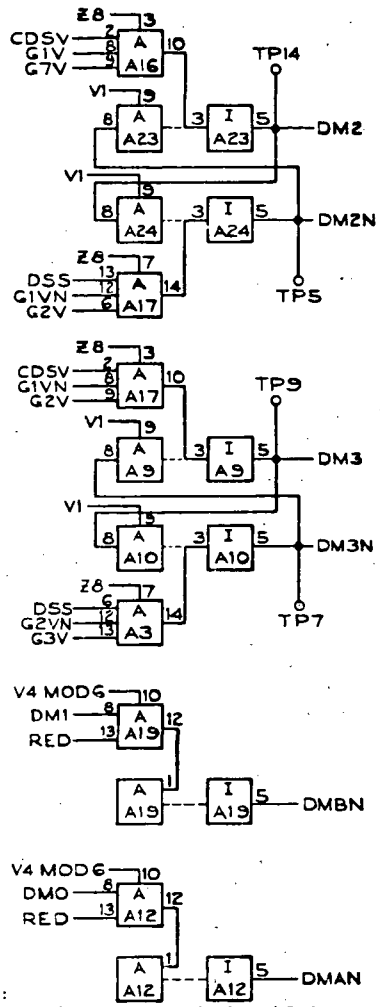


Figure 10-11. Memory Module Registers, Logic Diagram (Sheet 1 of 2)



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	ISS	51	SIG RET
3	G1VN	53	
5	G7VN	55	MFFN
7	HOPV	57	DMAN
9	MZON	59	DMBN
11	PCV	61	Z8
13	ISSN	63	
15		65	
17		67	
19	V4MOD6	69	IMBN
21		71	
23		73	
25		75	G5V
27		77	
29	G7V	79	
31		81	MSSN
33	G6V	83	G6VN
35	DSSN	85	G3V
37	CDSV	87	G4VN
39	G1V	89	V3
41	DSS	91	IMAN
43	G2V	93	G4V
45	MTTN	95	PBV
47	G2VN	97	G5VN
49	V1		



A1A14A

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotten Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A14A

THRU PINS			
Pin	Signal	Pin	Signal
1	DUPDN	16	DM0
2	G6V	17	DM1
3	G1VN	18	PCV
4	G7VN	19	DM2
5	G1V	20	DM3
6	PAV	21	G7V
7	G2V	22	G2VN
8	G3V	23	
9	RED	24	REI
10	IM2	25	IM0
11	G5V	26	IM1
12	G4V	27	G6VN
13	PBV	28	G4VN
14		29	DUPIN
15	IM3	30	G5VN

Figure 10-11. Memory Module Registers, Logic Diagram (Sheet 2)

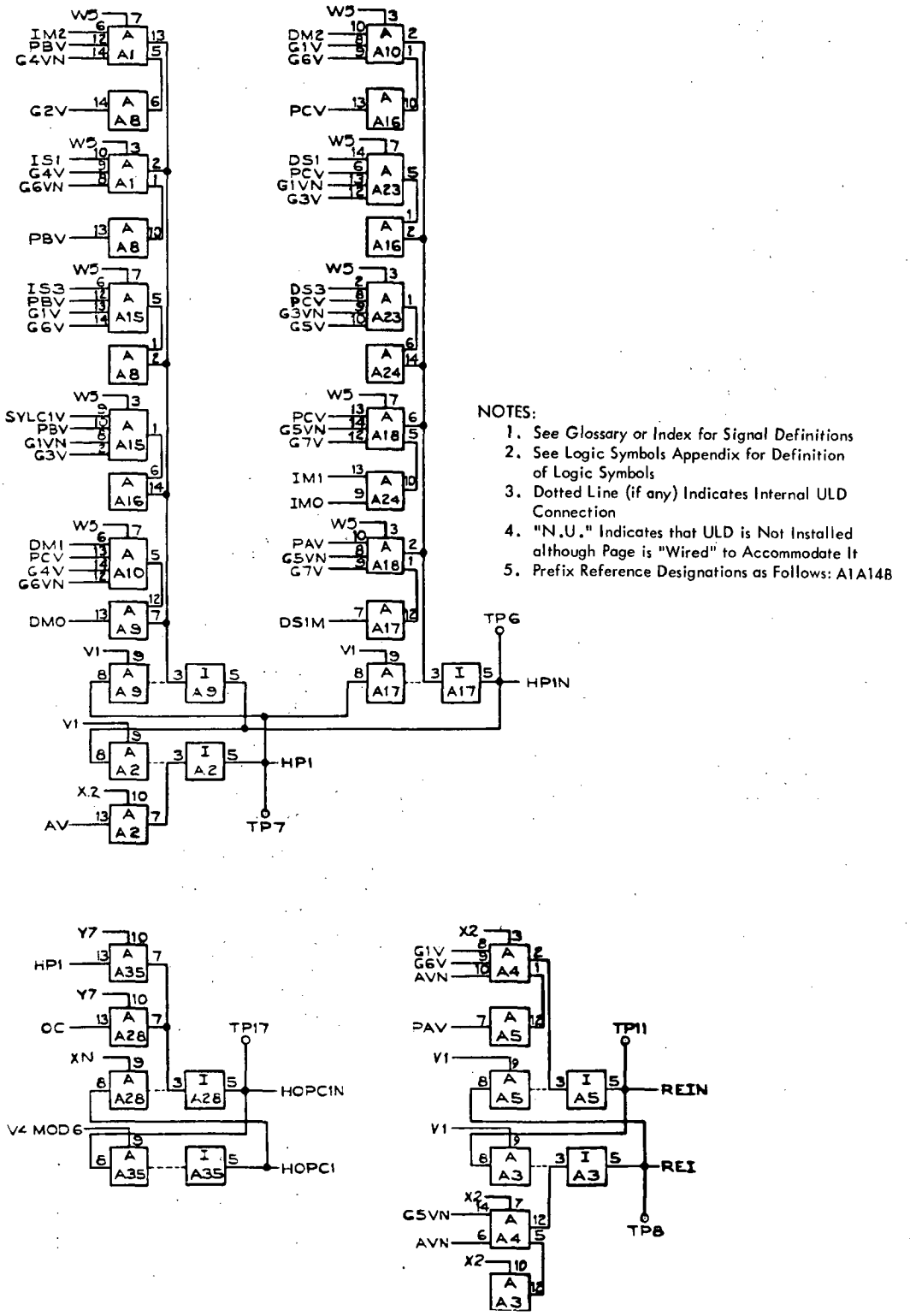
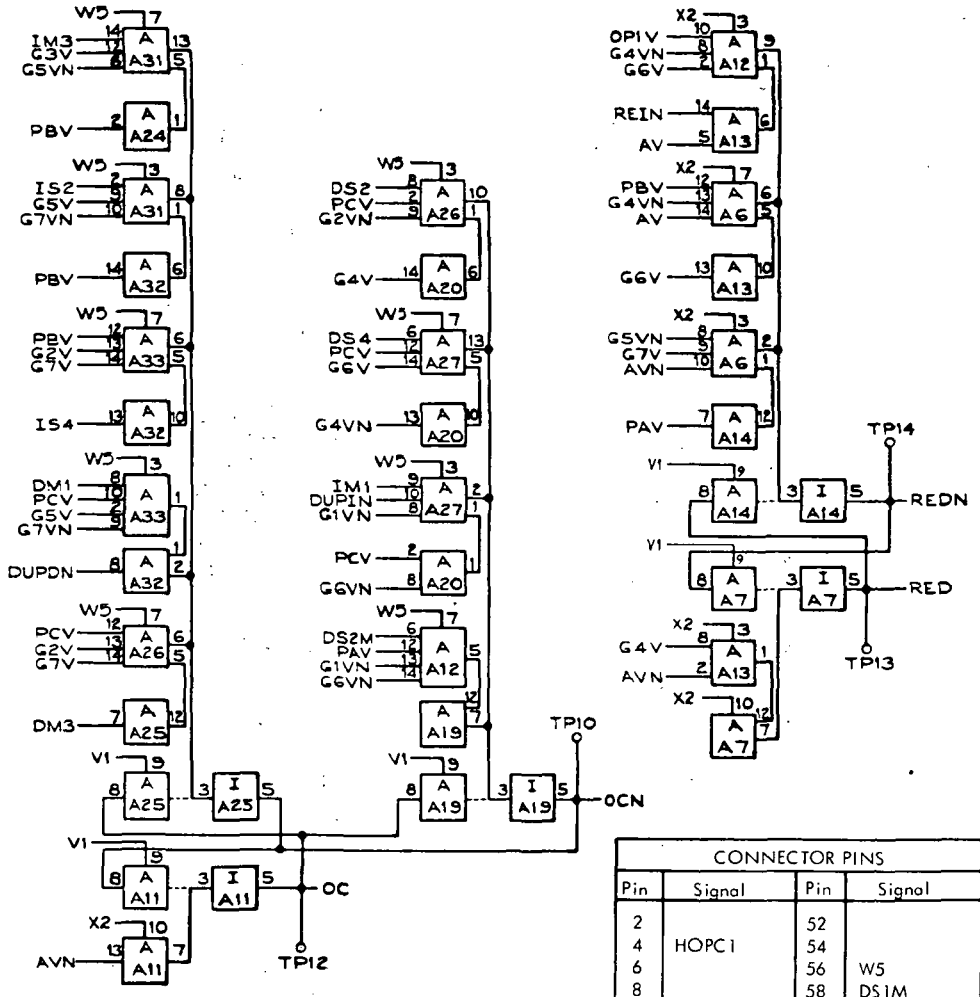


Figure 10-12. HOP Constant Serializer and Memory Read Latches, Logic Diagram (Sheet 1 of 2)

A1A14B



THRU PINS			
Pin	Signal	Pin	Signal
1	DUPDN	16	DM0
2	G6V	17	DM1
3	G1VN	18	PCV
4	G7VN	19	DM2
5	G1V	20	DM3
6	PAV	21	G7V
7	G2V	22	G2VN
8	G3V	23	
9	RED	24	REI
10	IM2	25	IM0
11	G5V	26	IM1
12	G4V	27	G6VN
13	PBV	28	G4VN
14		29	DUPIN
15	IM3	30	G5VN

CONNECTOR PINS			
Pin	Signal	Pin	Signal
2		52	
4	HOPC1	54	
6		56	W5
8		58	DS1M
10		60	
12		62	
14	Y7	64	IS2
16	PAV	66	
18	AV	68	
20	V4MOD6	70	DS1
22	XN	72	
24	AVN	74	V1
26	DS2M	76	
28	OP1V	78	DS3
30	DS4	80	G3VN
32		82	
34		84	
36		86	SYLC1V
38	X2	88	
40		90	
42	DS2	92	IS1
44		94	IS3
46	IS4	96	SIG RET
48		98	V3
50			

Figure 10-12. HOP Constant Serializer and Memory Read Latches, Logic Diagram (Sheet 2)

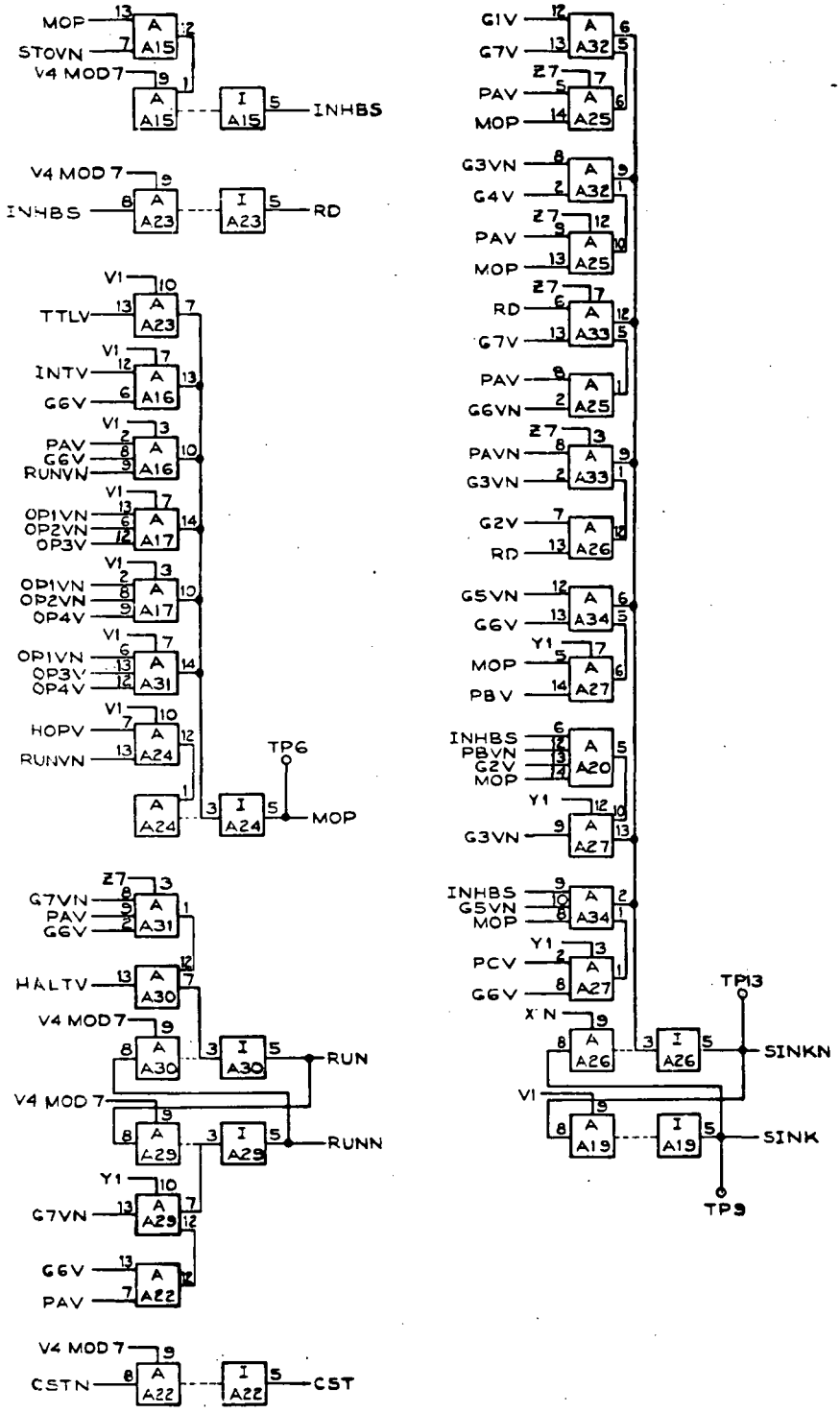
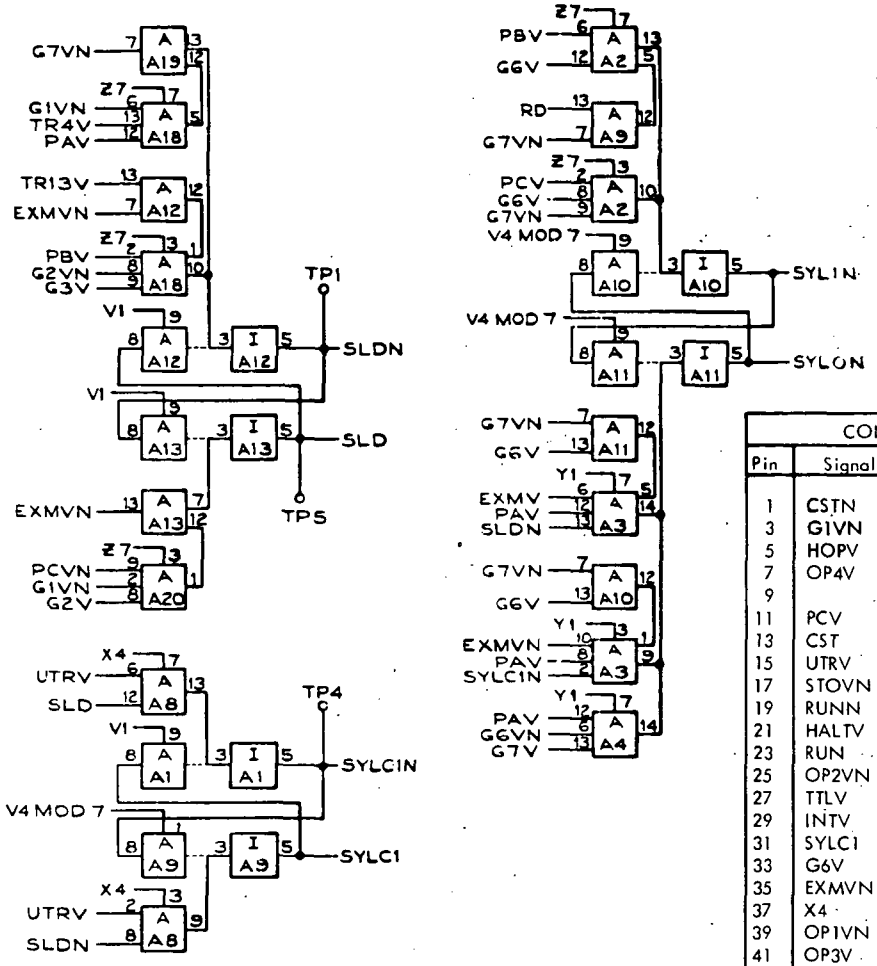


Figure 10-13. Memory Timing, Logic Diagram (Sheet 1 of 4)



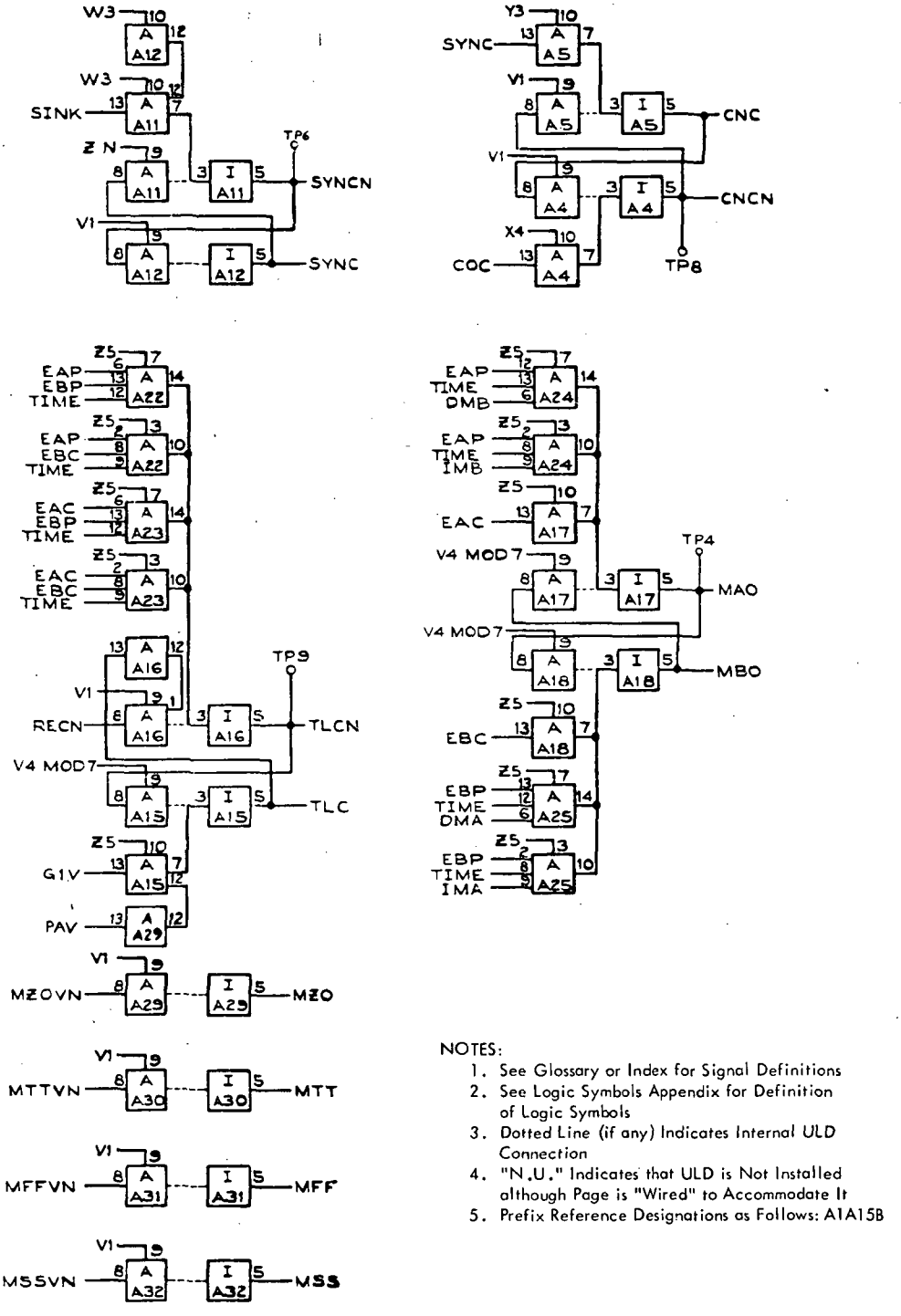
CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	CSTN	51	
3	G1VN	53	Y1
5	HOPV	55	SYLON
7	OP4V	57	PAVN
9		59	SYLIN
11	PCV	61	Z7
13	CST	63	PBVN
15	UTRV	65	RD
17	STOVN	67	G2VN
19	RUNN	69	INHBS
21	HALTV	71	
23	RUN	73	
25	OP2VN	75	
27	TTLV	77	PBV
29	INTV	79	PCVN
31	SYLC1	81	TR13V
33	G6V	83	
35	EXMVN	85	G3V
37	X4	87	
39	OP1VN	89	XN
41	OP3V	91	
43	TR4V	93	
45	G7VN	95	EXMV
47	RUNVN	97	G5VN
49			

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A15A

THRU PINS			
Pin	Signal	Pin	Signal
1	PAV	16	PCV
2	PBV	17	G3VN
3	RD	18	G1V
4	G7V	19	SINK
5		20	
6	G2V	21	G4V
7		22	
8	G2VN	23	PAVN
9		24	XN
10	V1	25	V3
11		26	
12	SIG RET	27	
13		28	G6VN
14		29	
15		30	V4MOD7

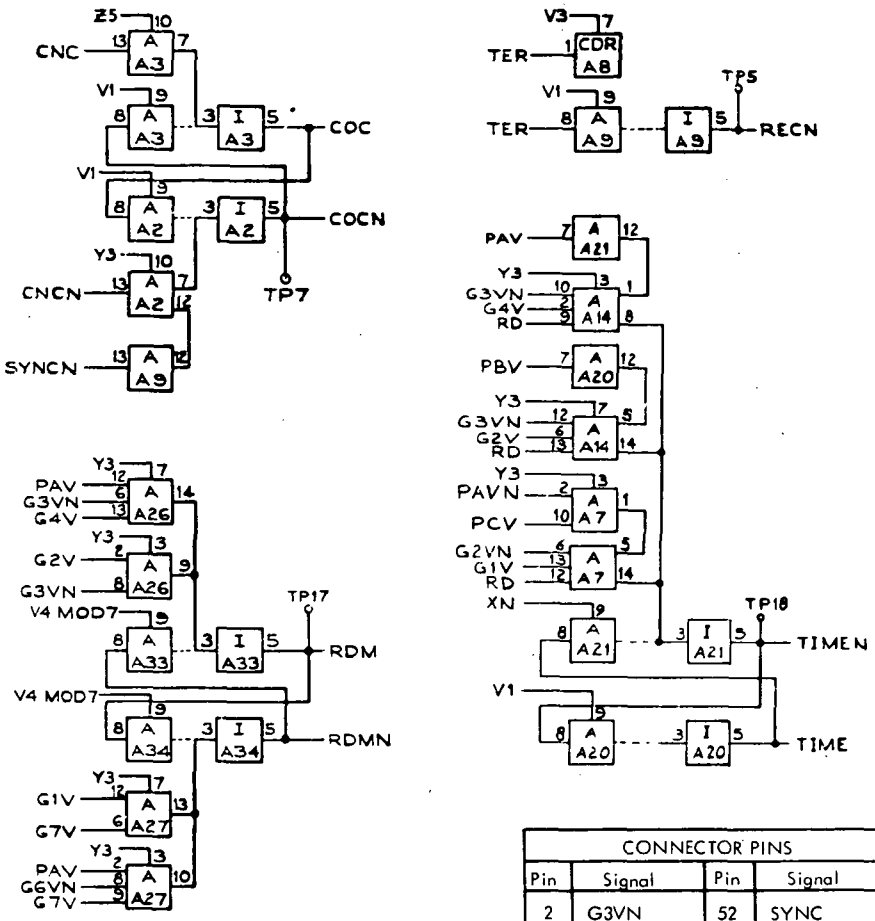
Figure 10-13. Memory Timing, Logic Diagram (Sheet 2)



NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A15B

Figure 10-13. Memory Timing, Logic Diagram (Sheet 3)

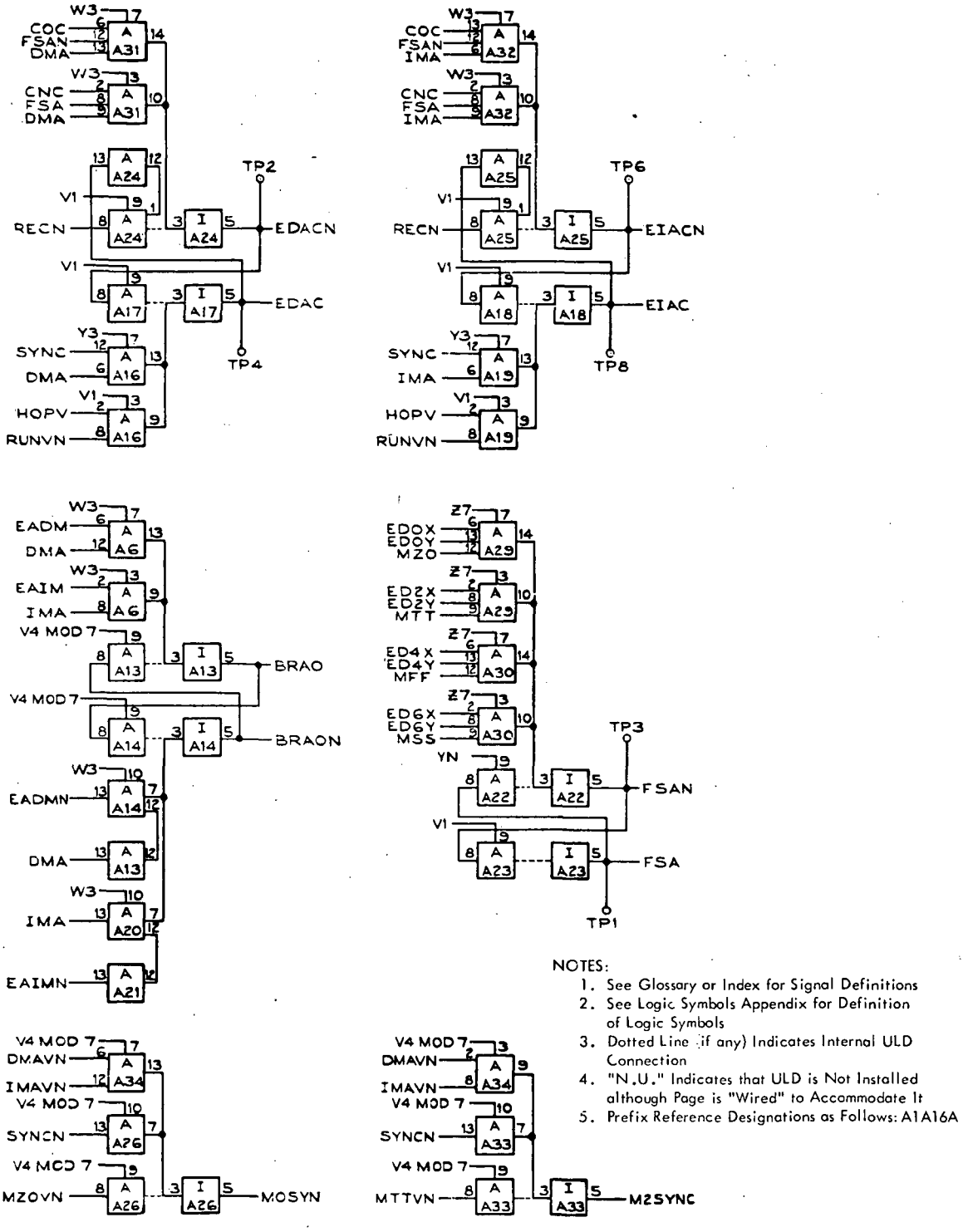


A1A15B

THRU PINS			
Pin	Signal	Pin	Signal
1	PAV	16	PCV
2	PBV	17	G3VN
3	RD	18	G1V
4	G7V	19	SINK
5		20	
6	G2V	21	G4V
7		22	
8	G2VN	23	PAVN
9		24	XN
10	V1	25	V3
11		26	
12	SIG RET	27	
13		28	G6VN
14		29	
15		30	V4MOD7

CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	G3VN	52	SYNC
4		54	Y3
6	DMA	56	EAC
8	CNC	58	MTT
10		60	MTTVN
12	V3	62	Z5
14	V1	64	G1V
16	PAV	66	MSSVN
18	RDM	68	TER
20		70	G2V
22	RDMN	72	EBC
24	IMA	74	IMB
26	MSS	76	G4V
28	MBO	78	SYNCN
30	G7V	80	EBP
32	MFF	82	TLC
34	MAO	84	G6VN
36	W3	86	MFFVN
38	X4	88	ZN
40		90	SIG RET
42		92	MZOVN
44	EAP	94	DMB
46	TIME	96	V4MOD7
48	RECN	98	MZO
50	COC		

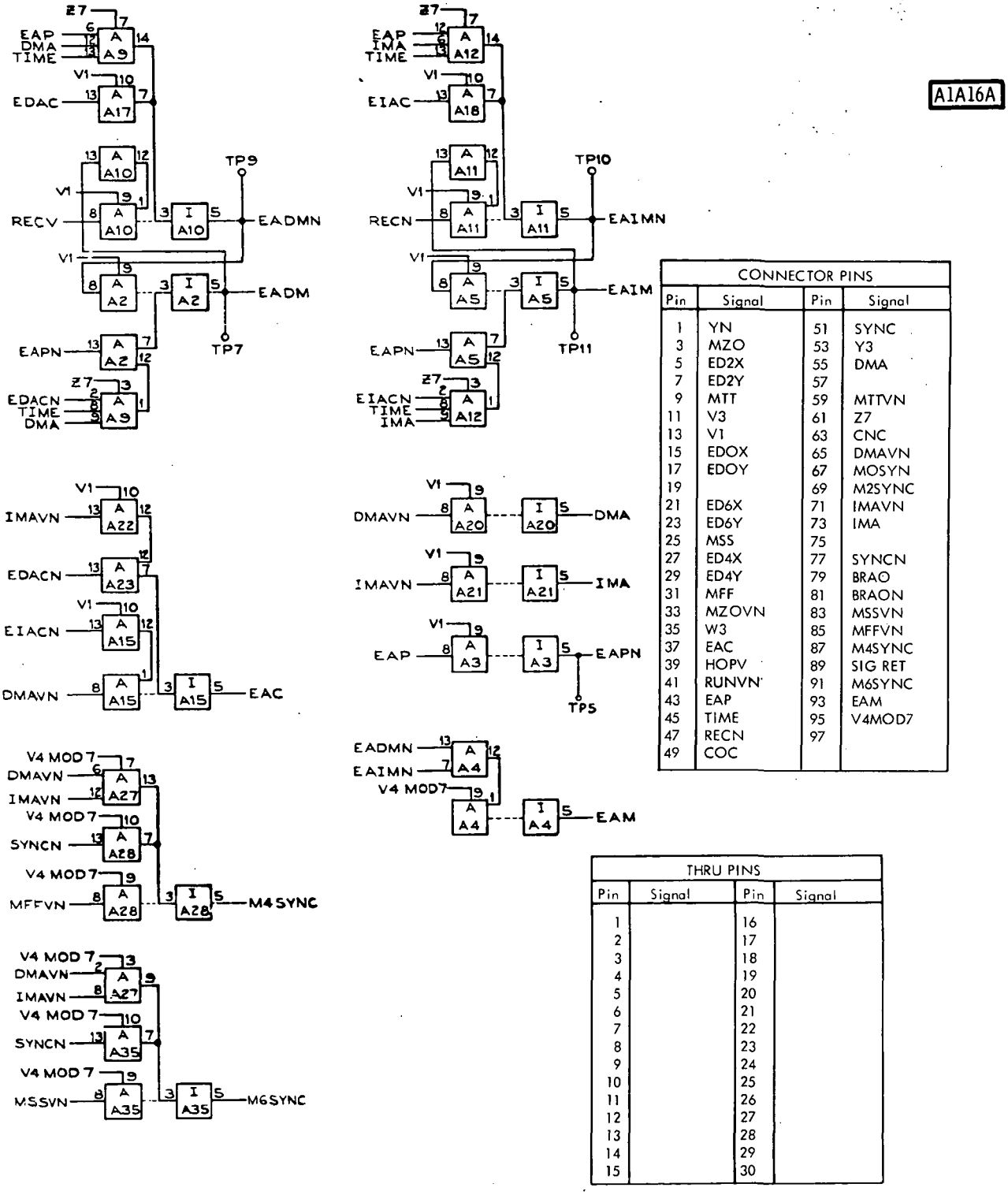
Figure 10-13. Memory Timing, Logic Diagram (Sheet 4)



NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A16A

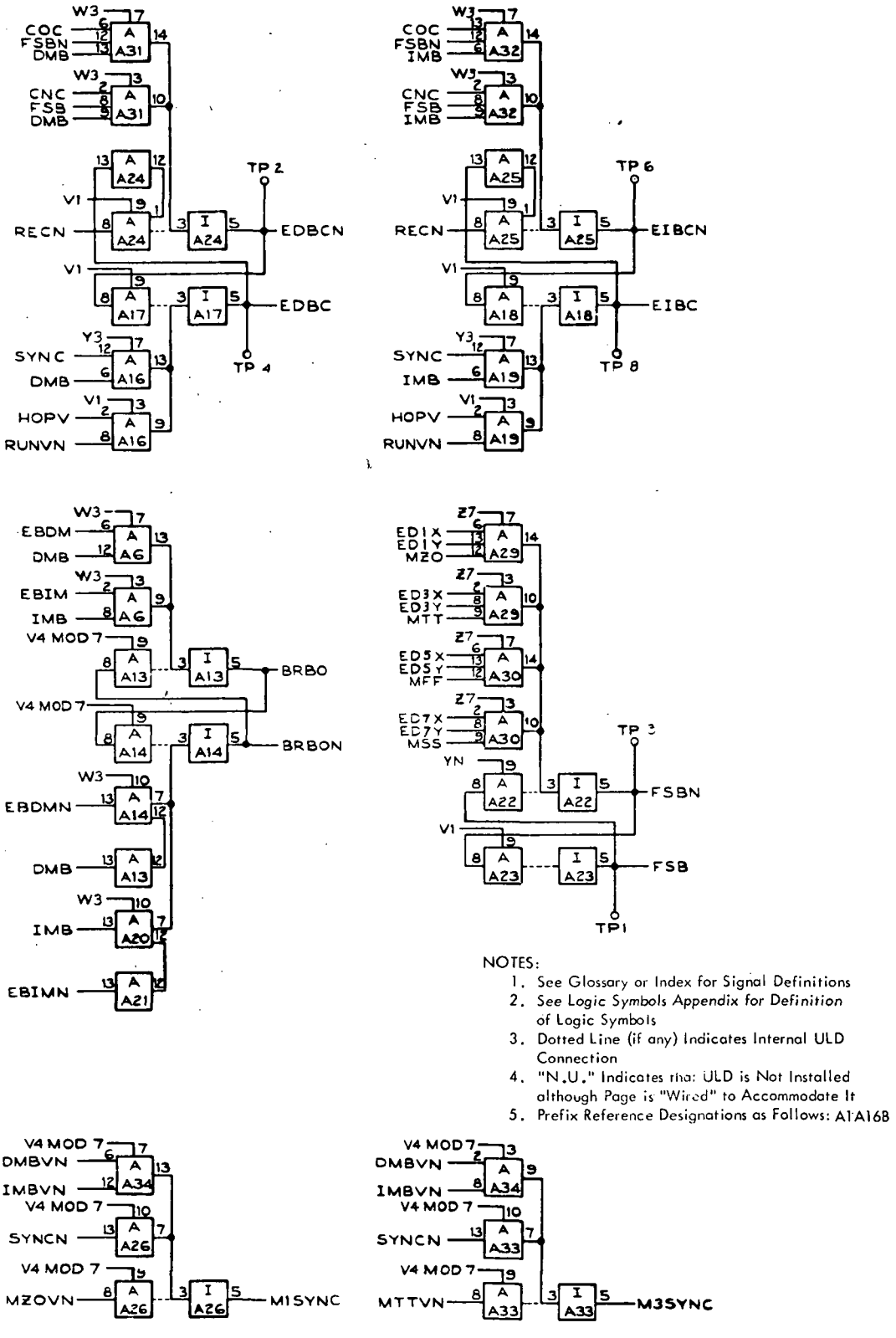
Figure 10-14. Memory Error Detector, Logic Diagram (Sheet 1 of 8)



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	YN	51	SYNC
3	MZO	53	Y3
5	ED2X	55	DMA
7	ED2Y	57	
9	MTT	59	MTTVN
11	V3	61	Z7
13	V1	63	CNC
15	EDOX	65	DMAVN
17	EDOY	67	MOSYN
19		69	M2SYNC
21	ED6X	71	IMAVN
23	ED6Y	73	IMA
25	MSS	75	
27	ED4X	77	SYNCN
29	ED4Y	79	BRAO
31	MFF	81	BRAON
33	MZOVN	83	MSSVN
35	W3	85	MFFVN
37	EAC	87	M4SYNC
39	HOPV	89	SIG RET
41	RUNVN	91	M6SYNC
43	EAP	93	EAM
45	TIME	95	V4MOD7
47	RECN	97	
49	COC		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2		17	
3		18	
4		19	
5		20	
6		21	
7		22	
8		23	
9		24	
10		25	
11		26	
12		27	
13		28	
14		29	
15		30	

Figure 10-14. Memory Error Detector, Logic Diagram (Sheet 2)

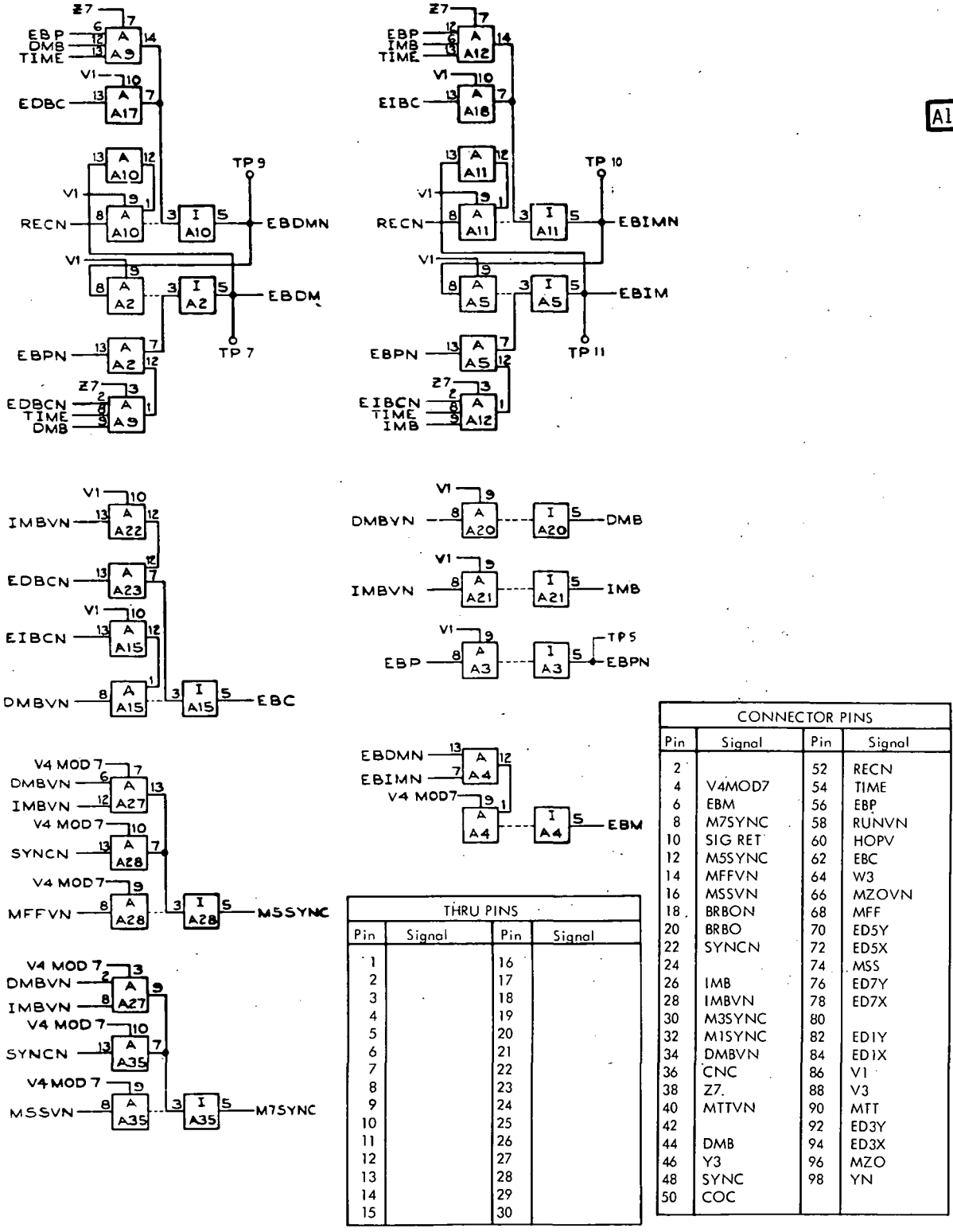


NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1-A168

Figure 10-14. Memory Error Detector, Logic Diagram (Sheet 3)

A1A16B



CONNECTOR PINS			
Pin	Signal	Pin	Signal
2		52	RECN
4	V4MOD7	54	TIME
6	EBM	56	EBP
8	M7SYNC	58	RUNVN
10	SIG RET	60	HOPV
12	M5SYNC	62	EBC
14	MFFVN	64	W3
16	MSSVN	66	MZOVN
18	BRBON	68	MFF
20	BRBO	70	ED5Y
22	SYNCN	72	ED5X
24		74	MSS
26	IMB	76	ED7Y
28	IMBVN	78	ED7X
30	M3SYNC	80	
32	M1SYNC	82	ED1Y
34	DMBVN	84	ED1X
36	CNC	86	V1
38	Z7	88	V3
40	MTTVN	90	MTT
42		92	ED3Y
44	DMB	94	ED3X
46	Y3	96	MZO
48	SYNC	98	YN
50	COC		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2		17	
3		18	
4		19	
5		20	
6		21	
7		22	
8		23	
9		24	
10		25	
11		26	
12		27	
13		28	
14		29	
15		30	

Figure 10-14. Memory Error Detector, Logic Diagram (Sheet 4)

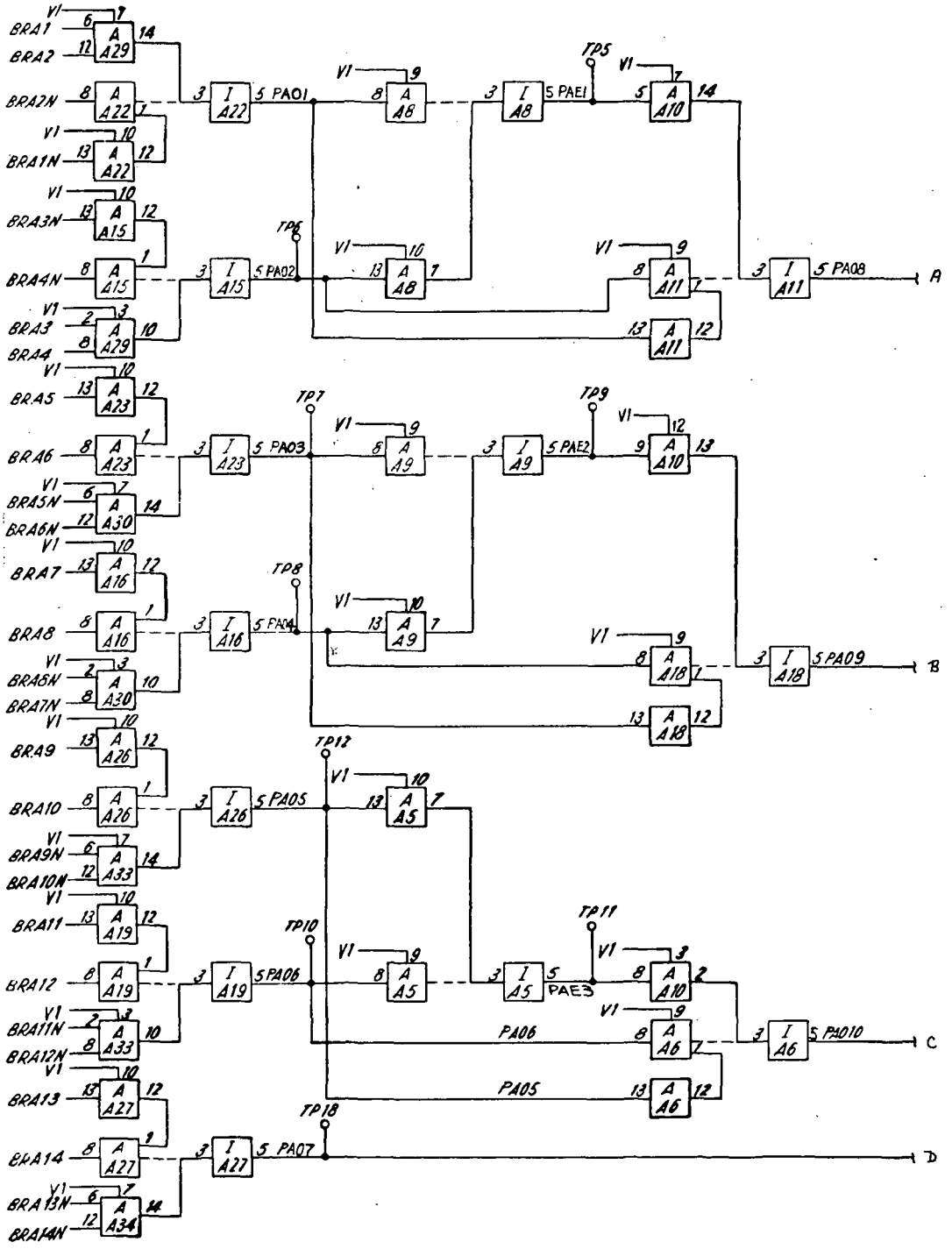


Figure 10-14. Memory Error Detector, Logic Diagram (Sheet 5)

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U. Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A17A

A1A17A

CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	BRA4N	51	
3	BRA2N	53	BRA12
5	BRA3	55	BRA10
7	BRA4	57	PAO1
9	BRA1	59	BRA12N
11	BRA2	61	BRA11N
13	BRA8	63	BRA10N
15	BRA1N	65	BRA9N
17	BRA3N	67	
19	BRA6	69	BRA9
21	BRA8N	71	BRA11
23	BRA6N	73	BRA14
25	BRA5N	75	
27	BRA7N	77	BRA14N
29	BRA5	79	BRA13N
31	BRA7	81	
33	SIG RET	83	BRA13
35	V3	85	
37		87	
39		89	
41	V1	91	
43		93	
45		95	
47		97	EAP
49			

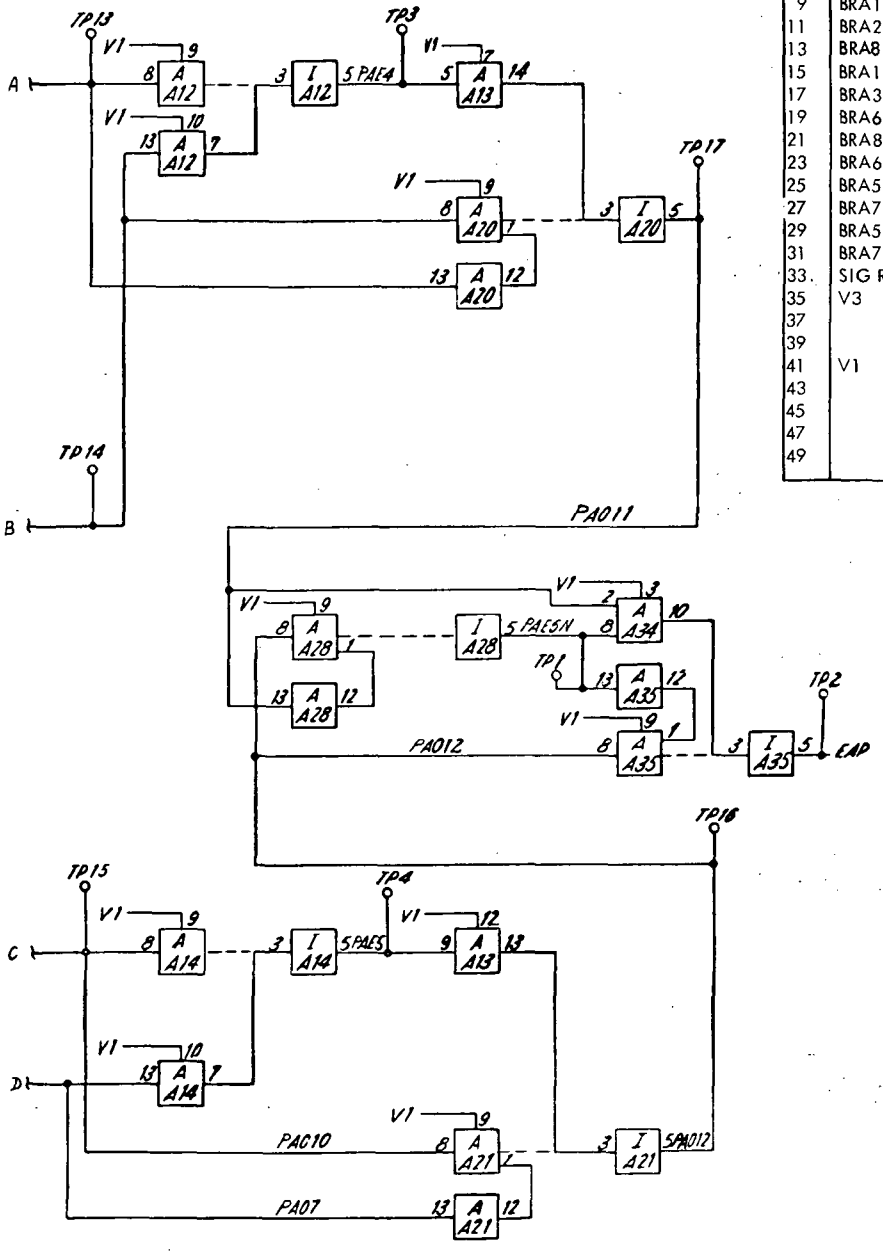


Figure 10-14. Memory Error Detector, Logic Diagram (Sheet 6)

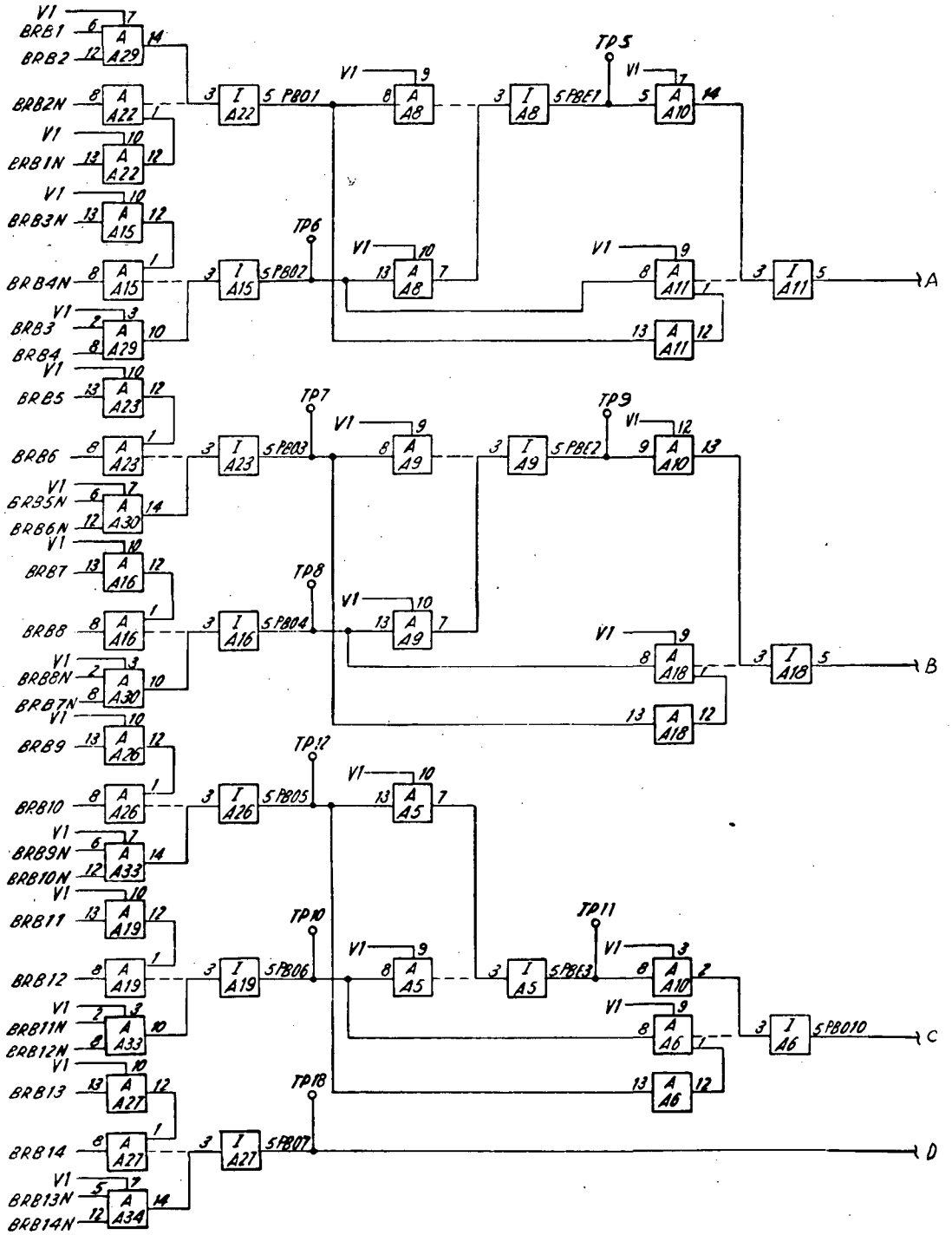


Figure 10-14. Memory Error Detector, Logic Diagram (Sheet 7)

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A17B

A1A17B

CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	EBP	52	
4		54	
6		56	
8		58	V1
10		60	
12		62	
14		64	V3
16	BRB13	66	SIG RET
18		68	BRB7
20	BRB13N	70	BRB5
22	BRB14N	72	BRB7N
24		74	BRB5N
26	BRB14	76	BRB6N
28	BRB11	78	BRB8N
30	BRB9	80	BRB6
32		82	BRB3N
34	BRB9N	84	BRB1N
36	BRB10N	86	BRB8
38	BRB11N	88	BRB2
40	BRB12N	90	BRB1
42	PB01	92	BRB4
44	BRB10	94	BRB3
46	BRB12	96	BRB2N
48		98	BRB4N
50			

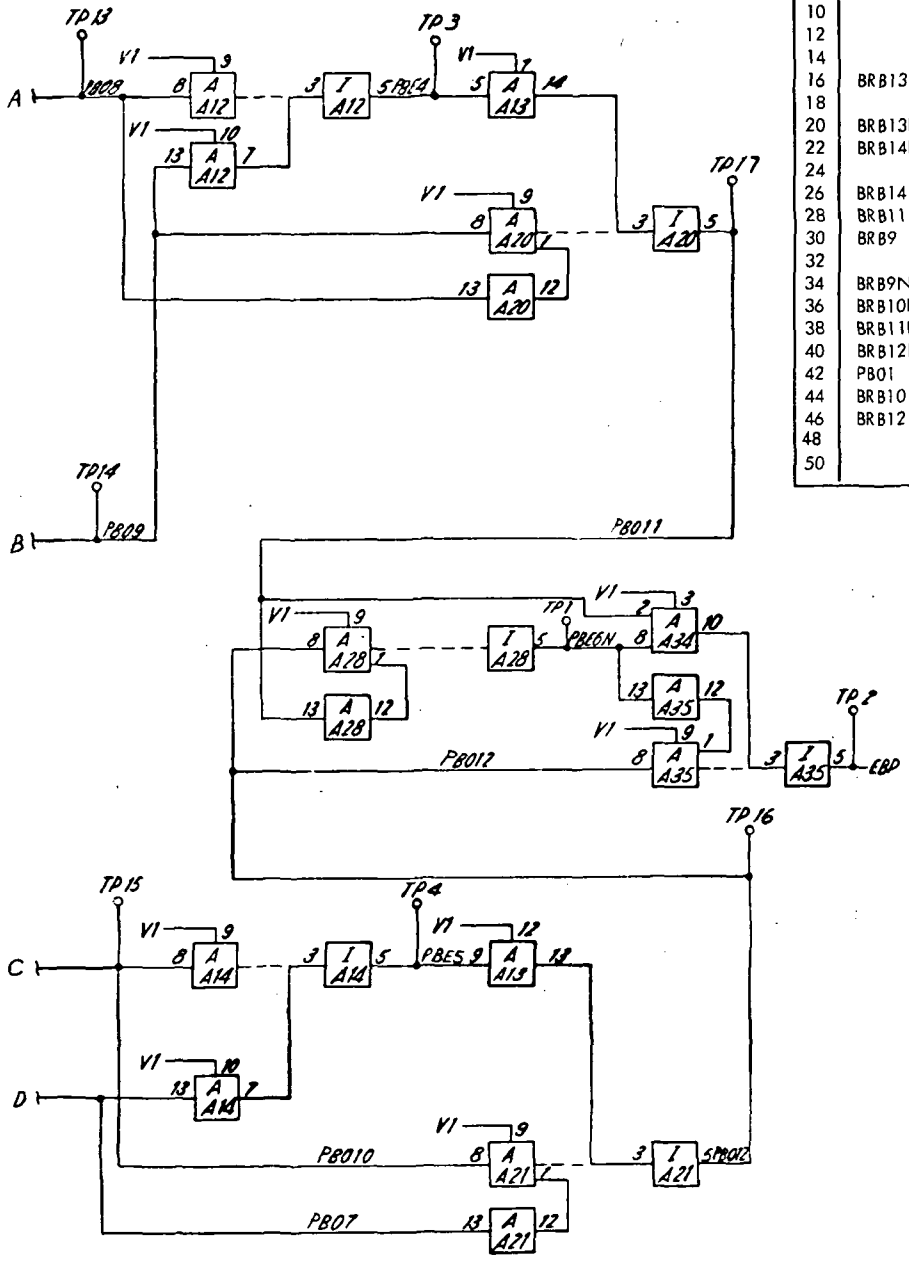


Figure 10-14. Memory Error Detector, Logic Diagram (Sheet 8)

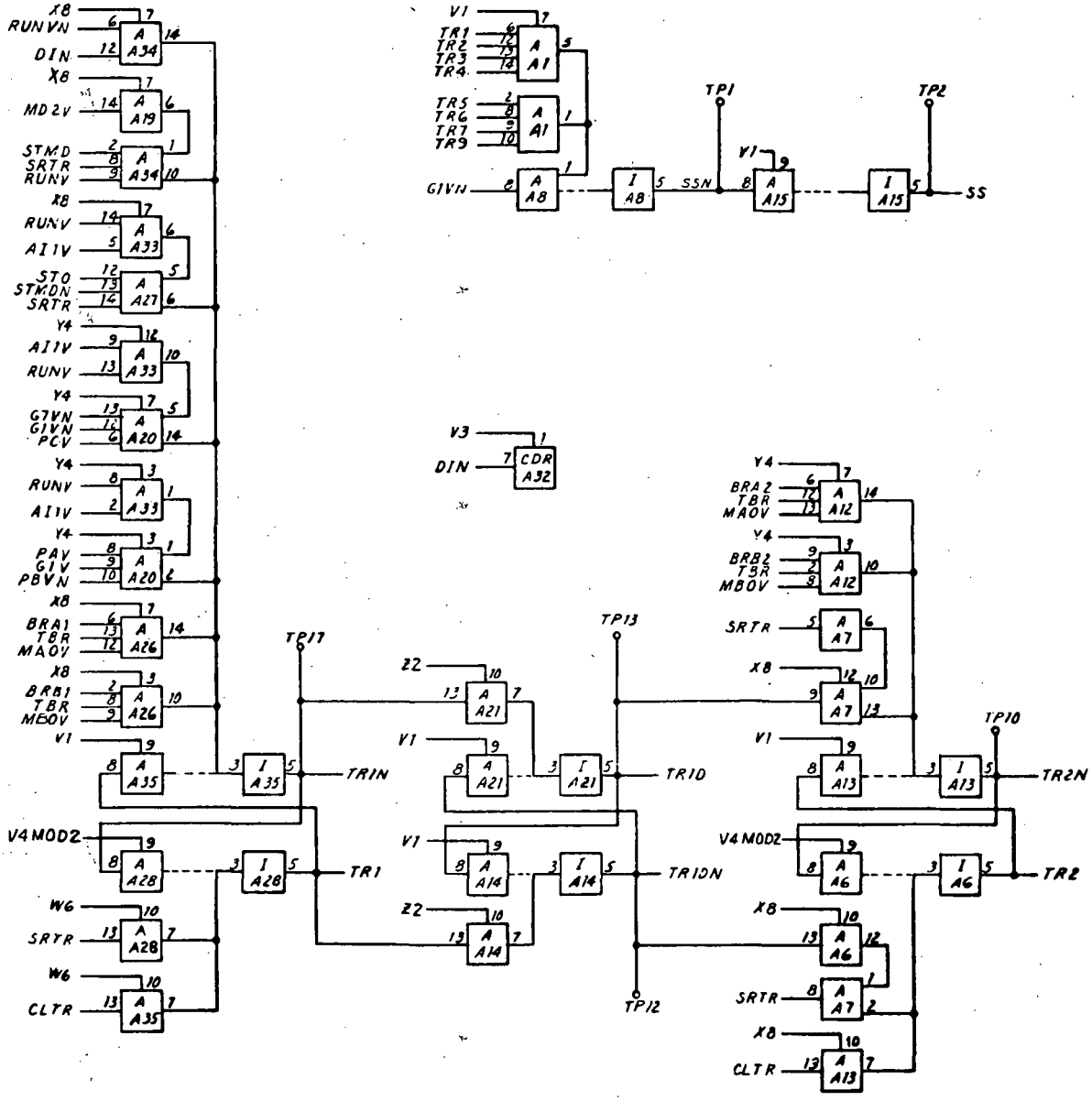
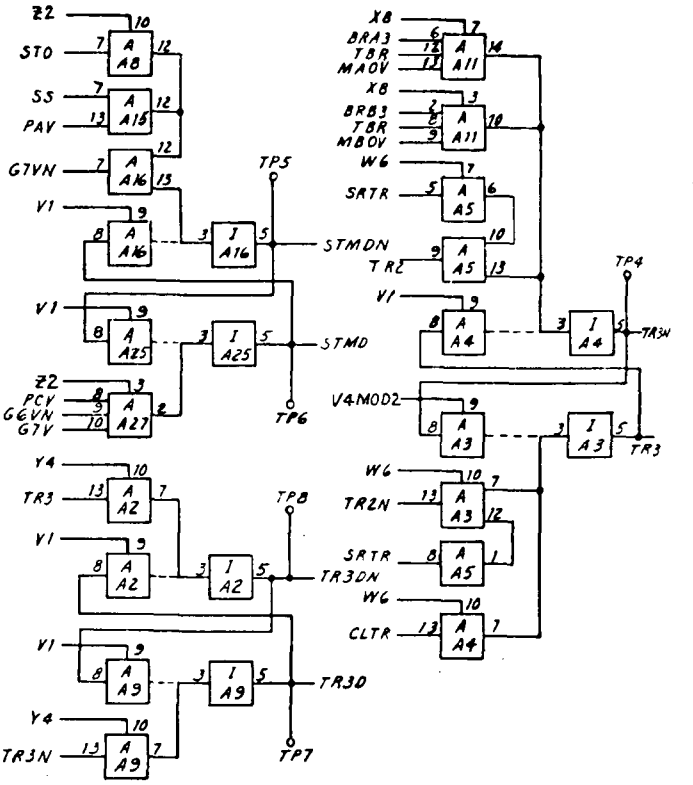


Figure 10-15. Transfer Register Bits 1-9, Logic Diagram (Sheet 1 of 4)



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	SIG RET	51	
3		53	BRB1
5		55	BRA1
7		57	AI1V
9		59	
11		61	G6VN
13		63	RUNV
15		65	G7V
17		67	TR1N
19		69	MD2V
21		71	G1V
23		73	SRTR
25		75	PAV
27	TR3	77	DIN
29		79	RUNVN
31		81	PBVN
33		83	PCV
35		85	G1VN
37	V1	87	G7VN
39	BRB2	89	V4MOD2
41	BRA3	91	TR1
43		93	TR2
45	BRA2	95	W6
47	BRB3	97	STO
49			

THRU PINS			
Pin	Signal	Pin	Signal
1	SIG RET	16	TR3DN
2	TR3D	17	-3VDC(V3)
3	TR7	18	Y4
4	TR5	19	X8
5	TR4	20	
6	TR9	21	V1
7	V4	22	
8	TR6	23	
9		24	CLTR
10		25	TBR
11		26	MBOV
12		27	SRTR
13		28	Z2
14		29	MAOV
15		30	

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate it
5. Prefix Reference Designations as Follows: A1A18A

Figure 10-15. Transfer Register Bits 1-9, Logic Diagram (Sheet 2)

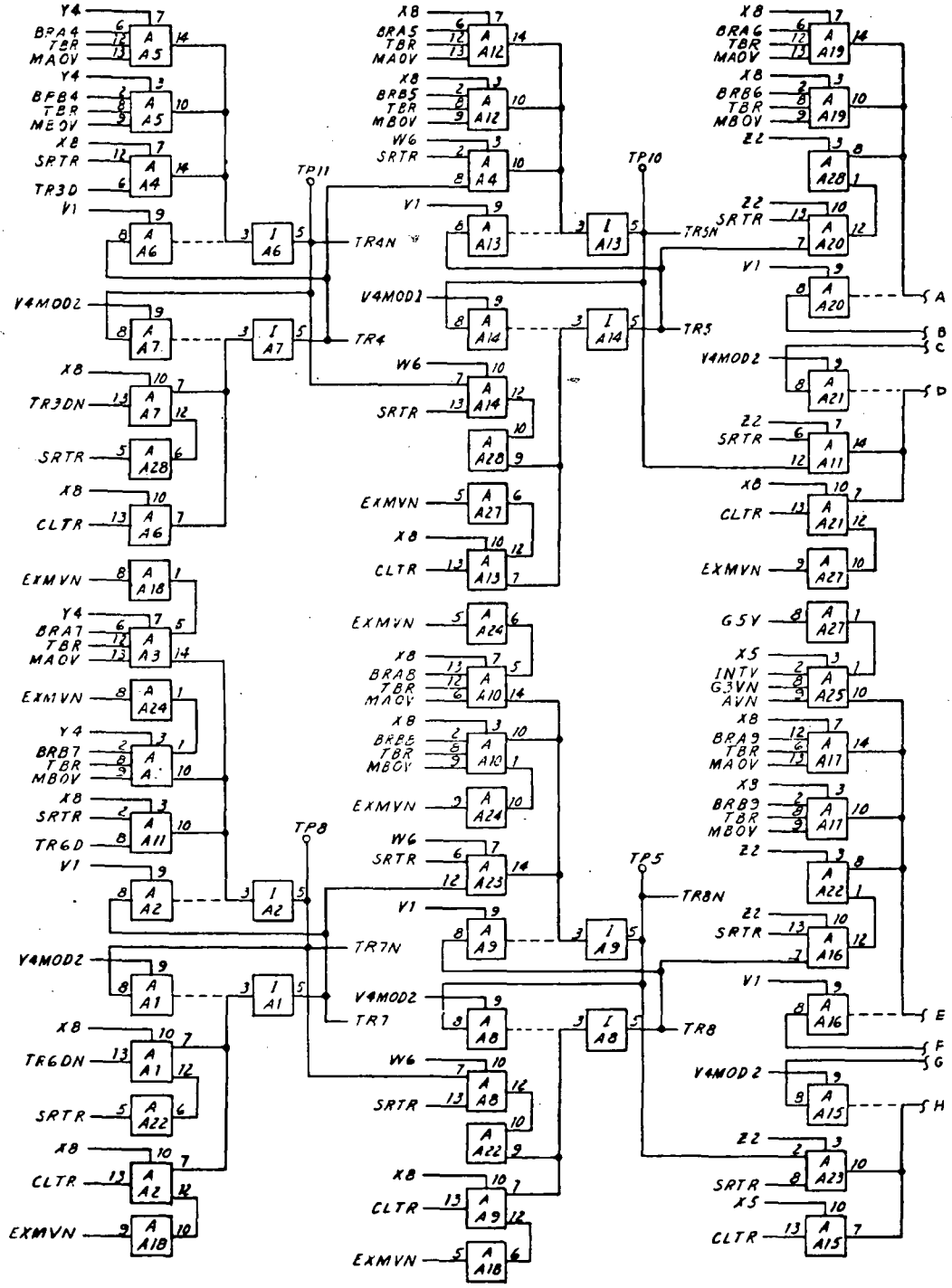
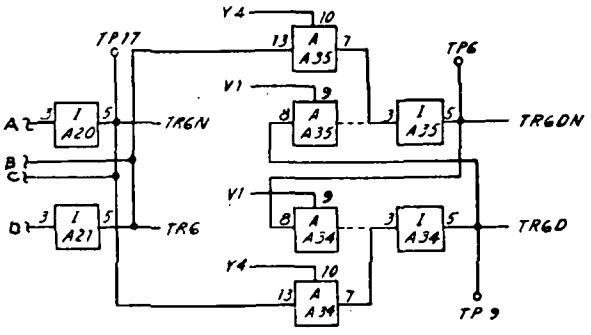


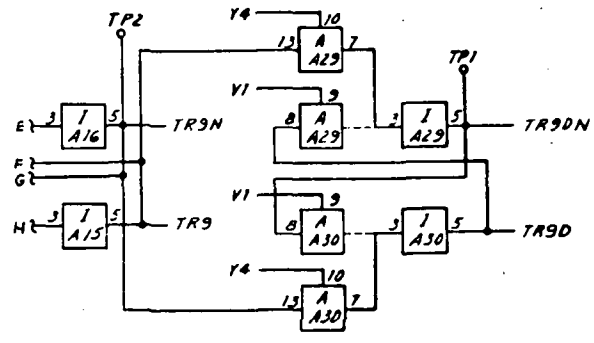
Figure 10-15. Transfer Register Bits 1-9, Logic Diagram (Sheet 3)



NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotten Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A18B

CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	TR6	52	Y4
4	TR4	54	BRA7
6	SRTR	56	BRA8
8		58	BRA9
10		60	BRB9
12		62	AVN
14		64	EXMVN
16	TR5	66	X5
18		68	TBR
20		70	BRB7
22		72	BRB8
24	X8	74	TR8
26	BRA4	76	
28	BRA5	78	
30	MAOV	80	TR7
32	BRB5	82	TR9DN
34	BRA6	84	
36	G5V	86	TR9
38		88	
40	CLTR	90	
42	BRB6	92	
44	MBOV	94	TR9D
46	BRB4	96	W6
48	INTV	98	Z2
50	G3VN		



THRU PINS			
Pin	Signal	Pin	Signal
1	SIG RET	16	TR3DN
2	TR3D	17	V3
3	TR7	18	V4
4	TR5	19	X8
5	TR4	20	
6	TR9	21	V1
7	V4MOD2	22	
8	TR6	23	
9		24	CLTR
10		25	TBR
11		26	MBOV
12		27	SRTR
13		28	Z2
14		29	MAOV
15		30	

Figure 10-15. Transfer Register Bits 1-9, Logic Diagram (Sheet 4)

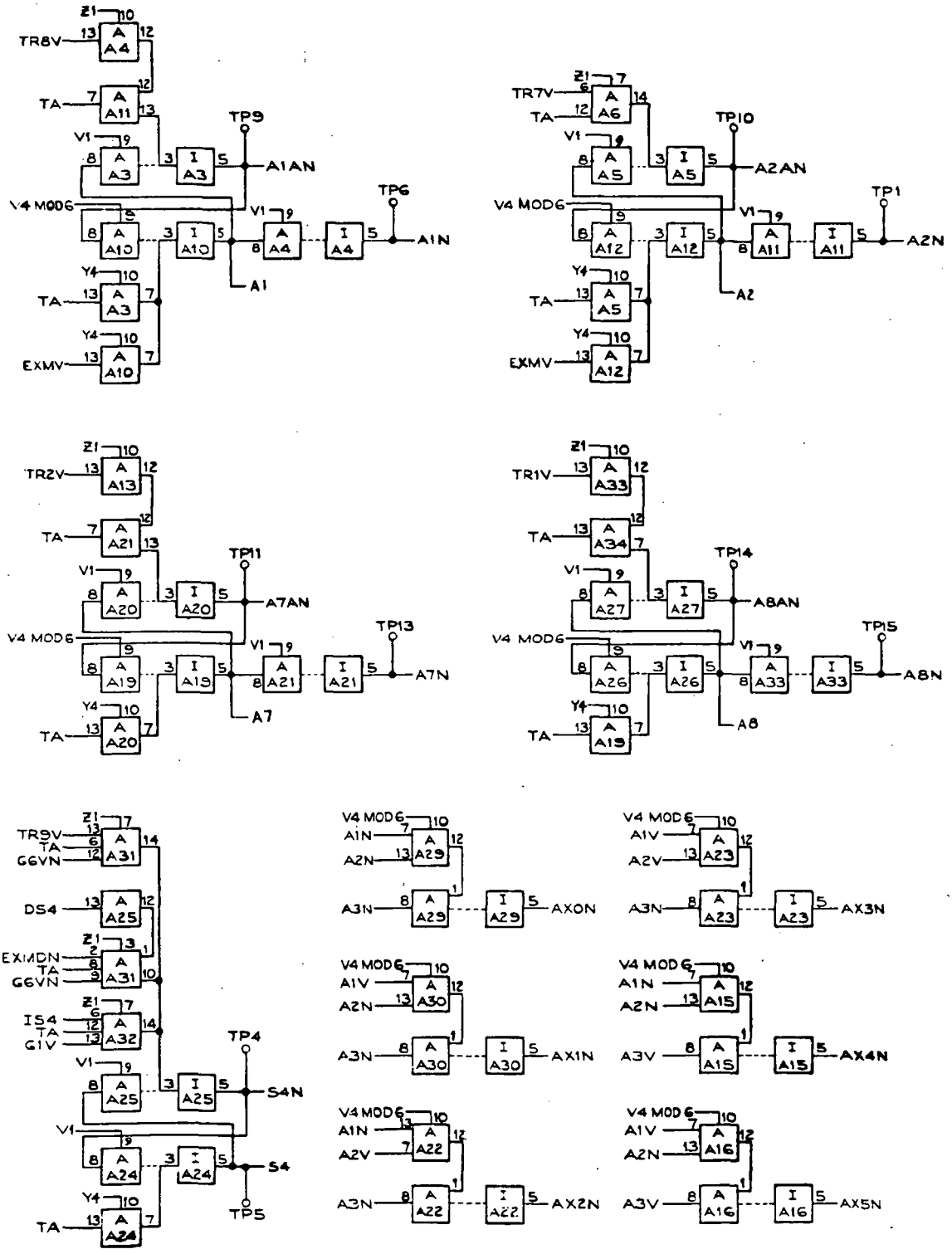
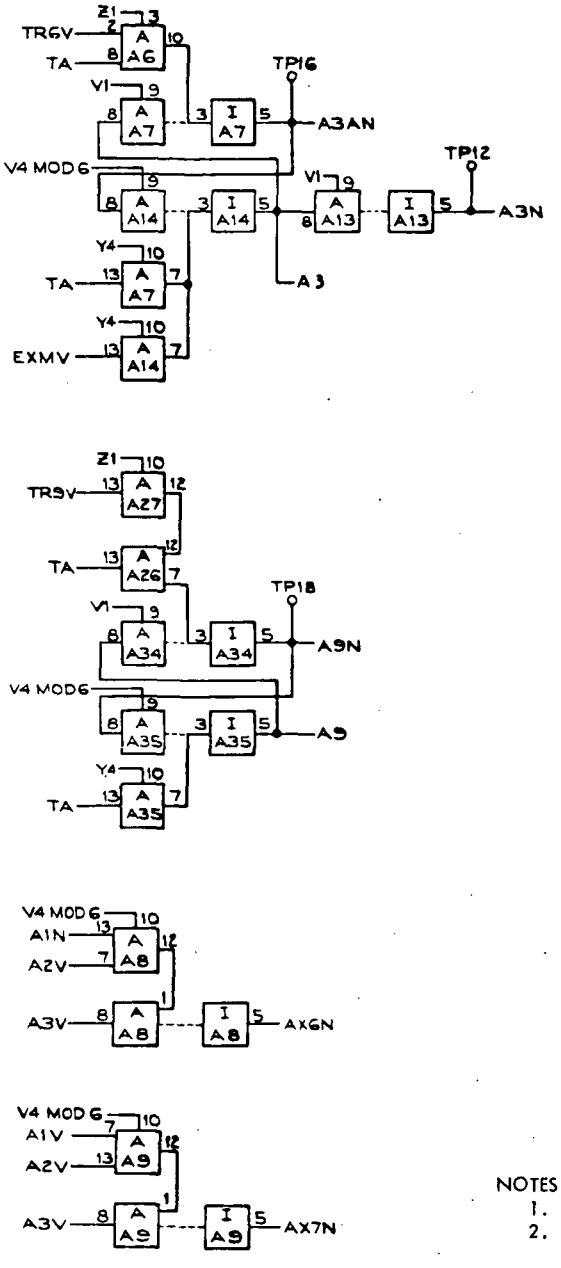


Figure 10-16. Address Register and Memory Address Decoder, Logic Diagram (Sheet 1 of 4)



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	AX6N	51	
3	AX4N	53	Y4
5	A3V	55	DS4
7		57	A8
9	SIG RET	59	IS4
11	V3	61	Z1
13	AX2N	63	
15		65	TR1V
17	AX7N	67	
19	V4MOD6	69	TR6V
21	AX3N	71	A3
23	TR8V	73	A9
25	AX1N	75	
27	A2V	77	
29	A1V	79	TR2V
31	AX5N	81	TR7V
33	EXMDN	83	G6VN
35	AXON	85	A7
37		87	
39	TR9V	89	
41	EXMV	91	
43	A1	93	
45	A2	95	
47	V1	97	
49			

A1A19A

THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2		17	S4
3		18	
4		19	
5		20	
6		21	TA
7		22	
8		23	S4N
9		24	G1V
10		25	A7N
11		26	EXMV
12		27	
13		28	
14		29	A8N
15		30	

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A19A

Figure 10-16. Address Register and Memory Address Decoder, Logic Diagram (Sheet 2)

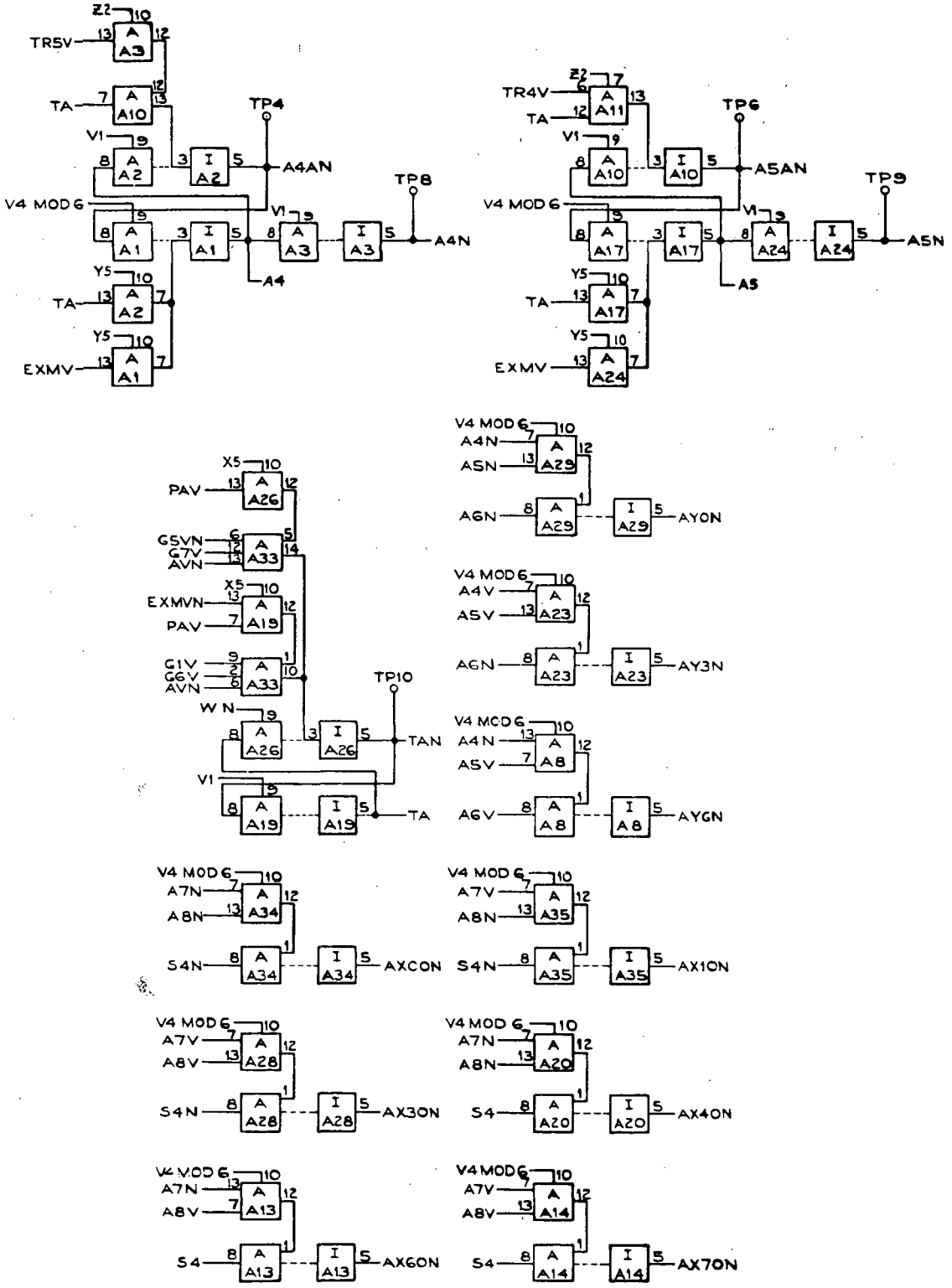
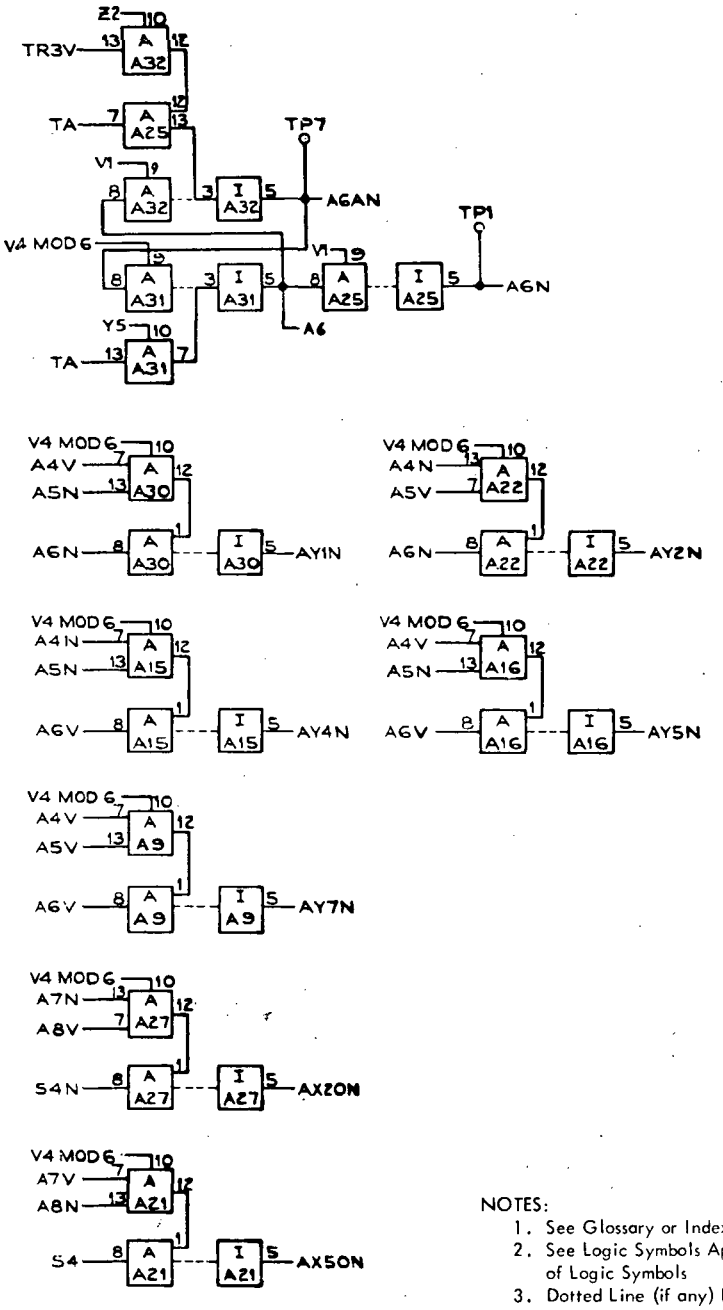


Figure 10-16. Address Register and Memory Address Decoder, Logic Diagram (Sheet 3)

A1A19B



CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	AX7ON	52	
4	A7V	54	Y5
6	A8V	56	A6
8	AX1ON	58	
10	AX5ON	60	TR5V
12	V1	62	Z2
14	SIG RET	64	G1V
16	PAV	66	AY7N
18	AXOON	68	A5
20	V4MOD6	70	
22	AX4ON	72	A4V
24	AX6ON	74	AY5N
26	TA	76	AY4N
28	AX2ON	78	AY3N
30	G7V	80	AY1N
32	WN	82	A5V
34	G6V	84	AYON
36	EXMVN	86	V3
38	X5	88	
40	AVN	90	
42	AX3ON	92	AY2N
44	TR4V	94	A6V
46	TR3V	96	A4
48	G5VN	98	AY6N
50			

THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2		17	S4
3		18	
4		19	
5		20	
6		21	TA
7		22	
8		23	S4N
9		24	G1V
10		25	A7N
11		26	EXMV
12		27	
13		28	
14		29	A8N
15		30	

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A19B

Figure 10-16. Address Register and Memory Address Decoder, Logic Diagram (Sheet 4)

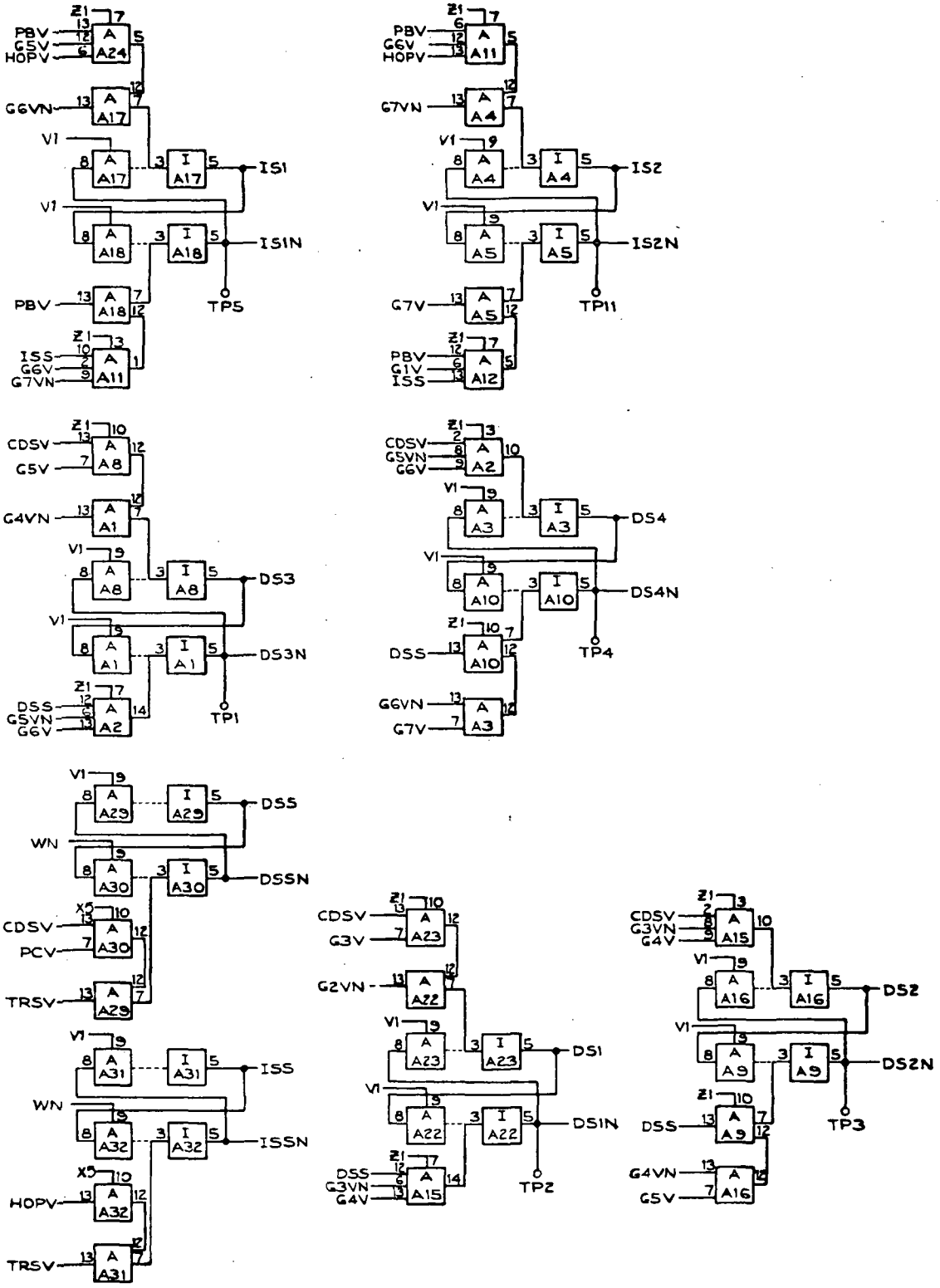
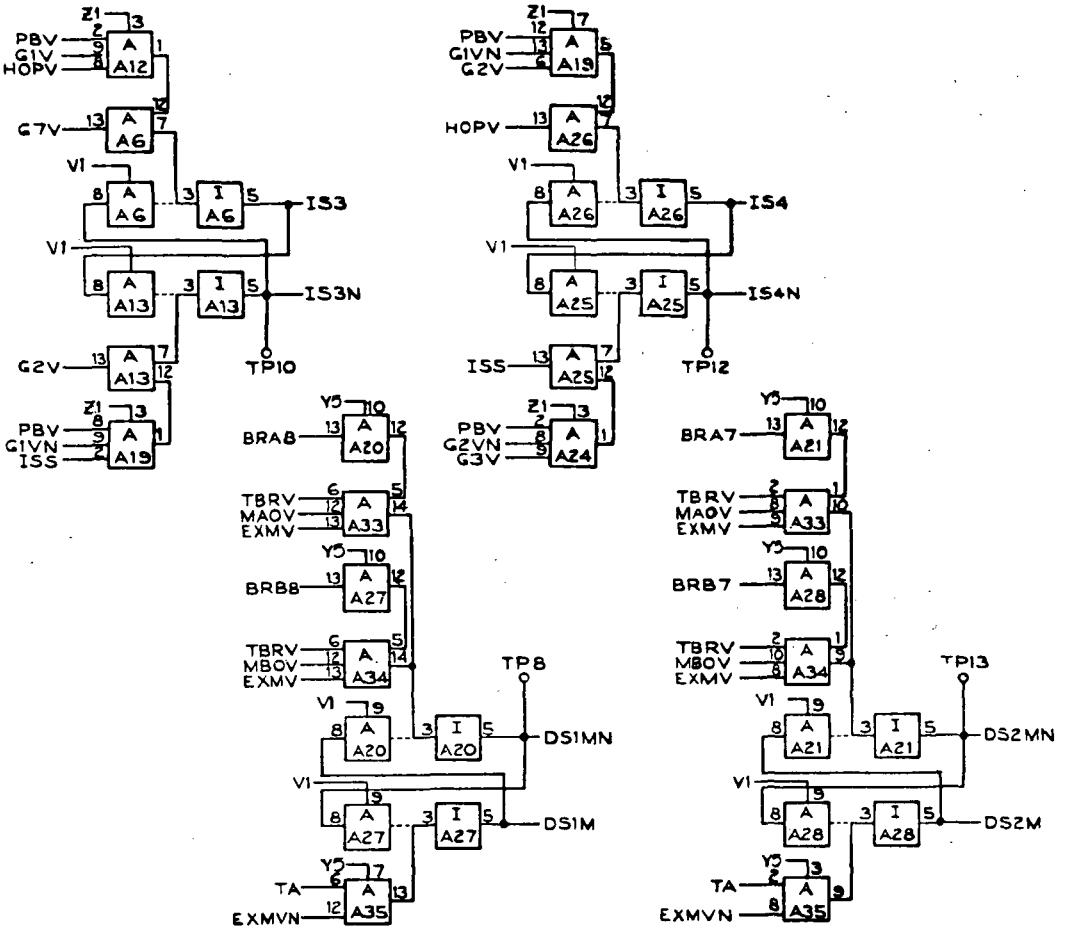


Figure 10-17. Memory Sector Registers, Logic Diagram (Sheet 1 of 2)



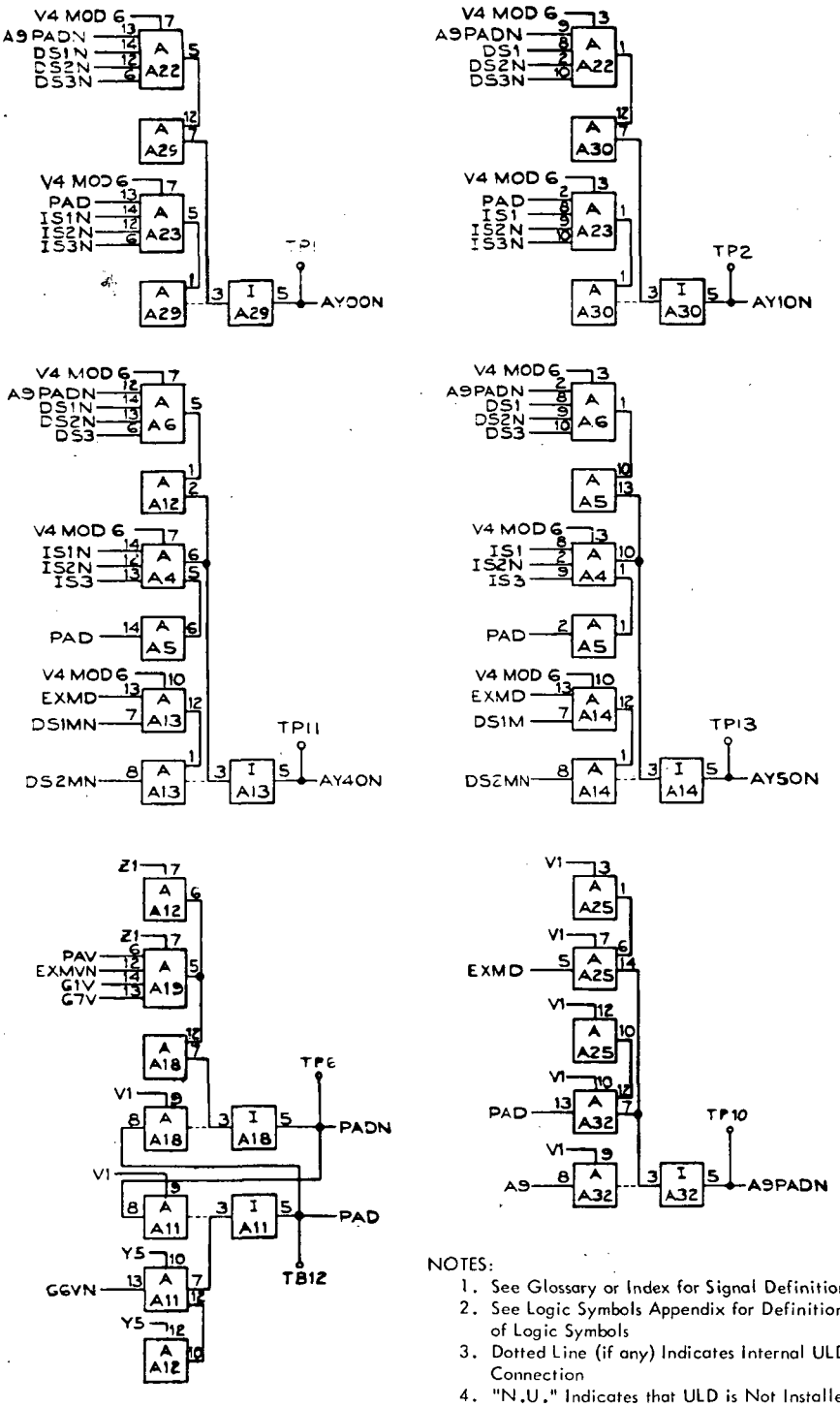
CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	PCV	51	
3	G4V	53	Y5
5	G3VN	55	DS4
7	DSSN	57	HOPV
9	V3	59	IS4
11	SIG RET	61	Z1
13	V1	63	G1V
15	G2VN	65	MAOV
17	G3V	67	G1VN
19	DSS	69	G2V
21	G5VN	71	TBRV
23	CDSV	73	
25	G4VN	75	
27	G5V	77	MBOV
29	G7V	79	BRB8
31	WN	81	BRA8
33	G6V	83	G6VN
35	ISSN	85	
37	X5	87	
39	PBV	89	
41	TRSV	91	
43	ISS	93	BRB7
45	G7VN	95	BRA7
47		97	
49			

THRU PINS			
Pin	Signal	Pin	Signal
1	DS2M	16	DS2MN
2	EXMV	17	DS1
3	DS1MN	18	EXMVN
4	TA	19	DS1N
5	DS1M	20	DS3
6		21	DS2N
7		22	IS3
8	IS1N	23	IS2
9		24	IS1
10		25	IS2N
11		26	DS2
12		27	
13		28	DS3N
14		29	IS3N
15		30	

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A20A

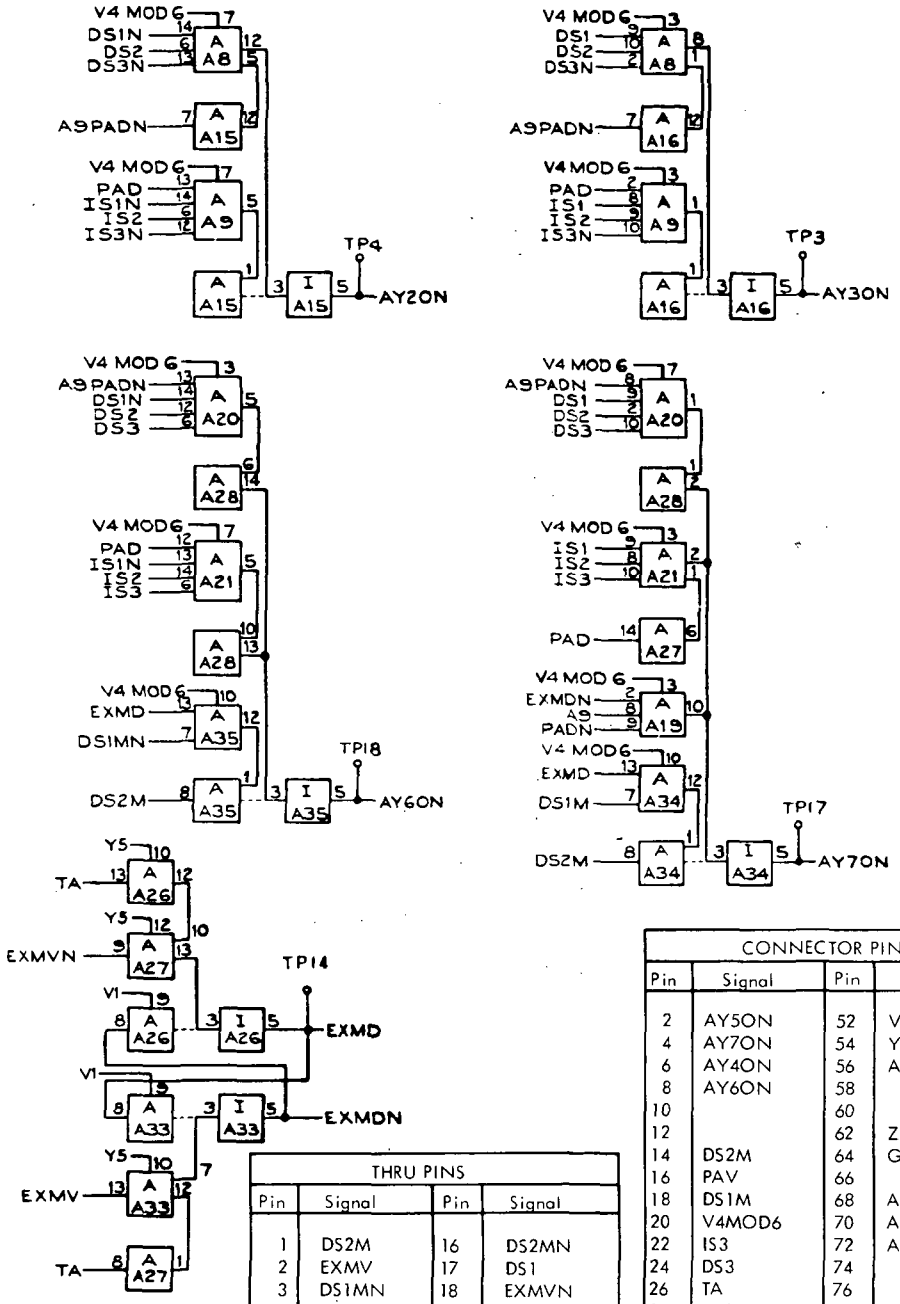
Figure 10-17. Memory Sector Registers, Logic Diagram (Sheet 2)



NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A1A20B

Figure 10-18. Hi-Y Memory Address Decoder, Logic Diagram (Sheet 1 of 2)



THRU PINS			
Pin	Signal	Pin	Signal
1	DS2M	16	DS2MN
2	EXMV	17	DS1
3	DS1MN	18	EXMVN
4	TA	19	DS1N
5	DS1M	20	DS3
6		21	DS2N
7		22	IS3
8	IS1N	23	IS2
9		24	IS1
10		25	IS2N
11		26	DS2
12		27	
13		28	DS3N
14		29	IS3N
15		30	

CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	AY5ON	52	V1
4	AY7ON	54	Y5
6	AY4ON	56	A9
8	AY6ON	58	
10		60	
12		62	Z1
14	DS2M	64	G1V
16	PAV	66	
18	DS1M	68	AY2ON
20	V4MOD6	70	AY1ON
22	IS3	72	AY3ON
24	DS3	74	
26	TA	76	
28	DS2	78	
30	G7V	80	AY0ON
32		82	IS1
34	EXMDN	84	G6VN
36	EXMVN	86	
38		88	V3
40	EXMD	90	SIG RET
42	EXMV	92	
44	IS2	94	
46		96	
48		98	DS1
50			

Figure 10-18. Hi-Y Memory Address Decoder, Logic Diagram (Sheet 2)

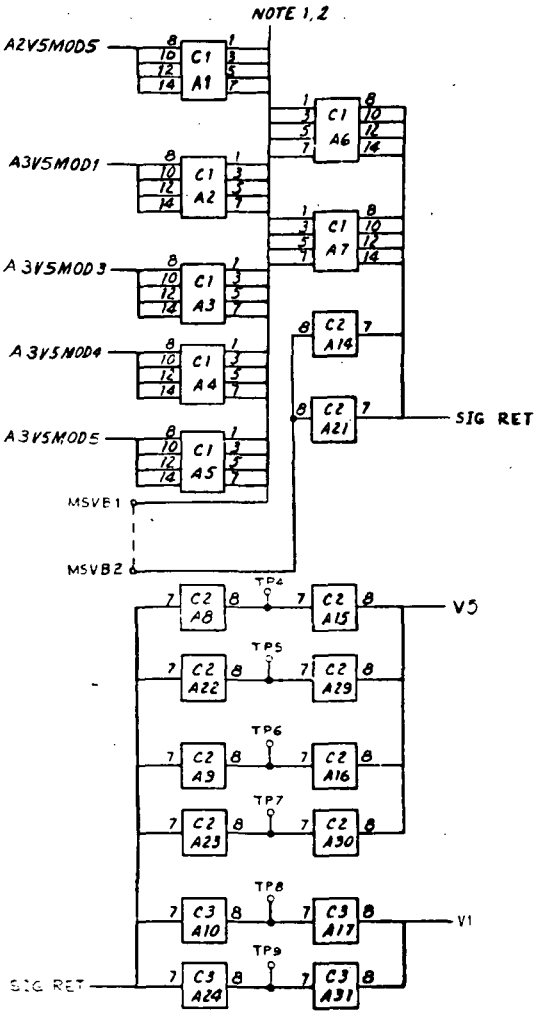
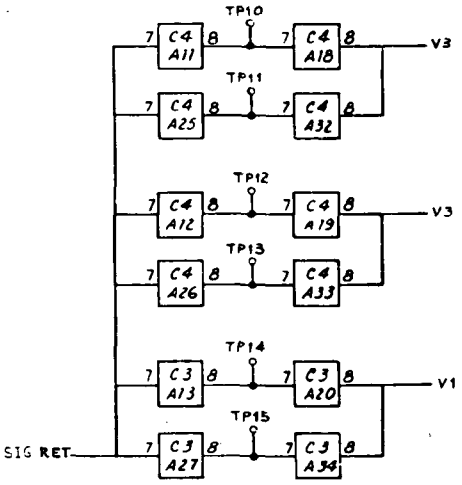


Figure 10-19. Decoupling Capacitors (Channel 4), Logic Diagram (Sheet 1 of 4)

A4A3A



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	MSVB1	51	SIG RET
3	MSVB1	53	SIG RET
5	SIG RET	55	SIG RET
7	SIG RET	57	SIG RET
9	A2V5MOD5	59	SIG RET
11	V3	61	SIG RET
13	V3	63	V3
15	V3	65	V3
17	V3	67	V3
19	A3V5MOD1	69	V3
21	V5	71	SIG RET
23	V5	73	V1
25	V5	75	V1
27	V5	77	V1
29	A3V5MOD3	79	V1
31	V1	81	SIG RET
33	V1	83	SIG RET
35	V1	85	SIG RET
37	V1	87	SIG RET
39	A3V5MOD4	89	SIG RET
41	SIG RET	91	SIG RET
43	SIG RET	93	SIG RET
45	SIG RET	95	MSVB2
47	SIG RET	97	MSVB2
49	A3V5MOD5		

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A4A3A

Figure 10-19. Decoupling Capacitors (Channel 4), Logic Diagram (Sheet 2)

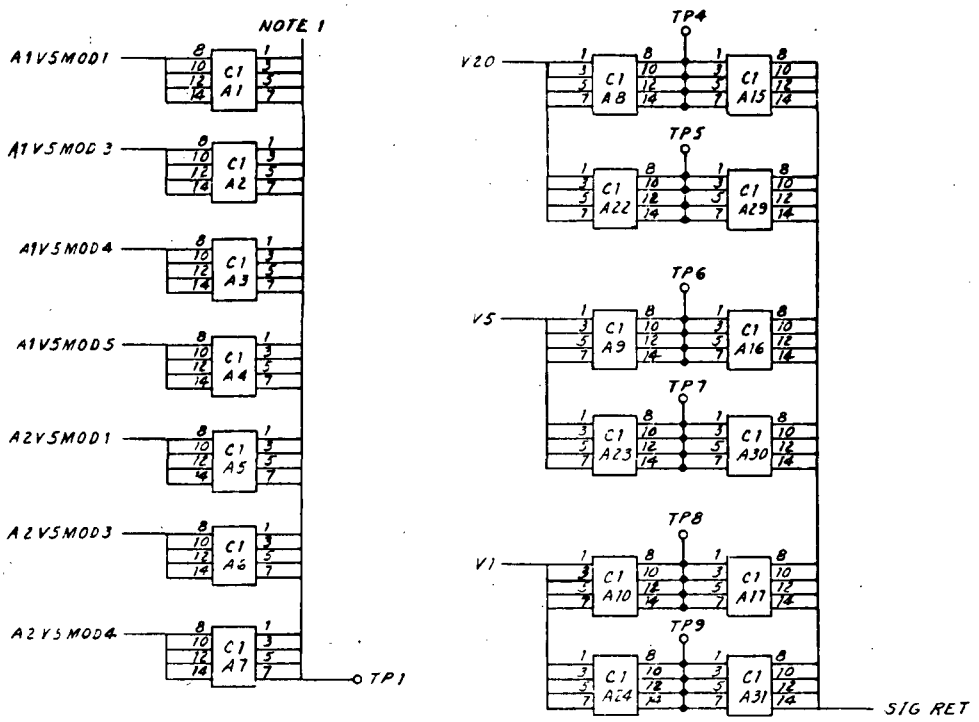
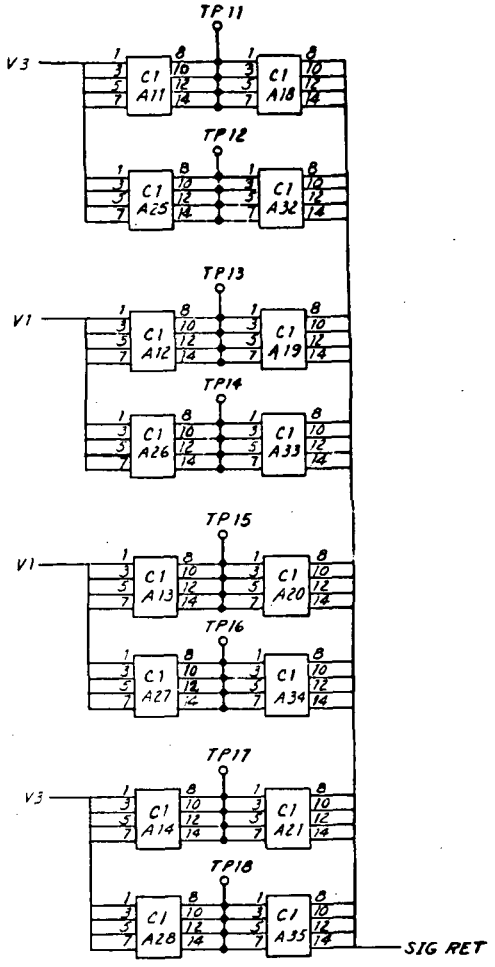


Figure 10-19. Decoupling Capacitors (Channel 4), Logic Diagram (Sheet 3)

A4A3B



CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	V3	52	V3
4	V3	54	V3
6	V3	56	V3
8	V3	58	A1V5MOD5
10	A2V5MOD4	60	V1
12	V1	62	V1
14	V1	64	V1
16	V1	66	V1
18	V1	68	SIG RET
20	SIG RET	70	SIG RET
22	SIG RET	72	SIG RET
24	SIG RET	74	SIG RET
26	SIG RET	76	SIG RET
28	SIG RET	78	A1V5MOD4
30	V1	80	V5
32	V1	82	V5
34	V1	84	V5
36	V1	86	V5
38	A2V5MOD3	88	A1V5MOD3
40	SIG RET	90	V20
42	SIG RET	92	V20
44	SIG RET	94	V20
46	SIG RET	96	V20
48	A2V5MOD1	98	A1V5MOD1
50	V3		

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U. Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A4A3B

Figure 10-19. Decoupling Capacitors (Channel 4), Logic Diagram (Sheet 4)

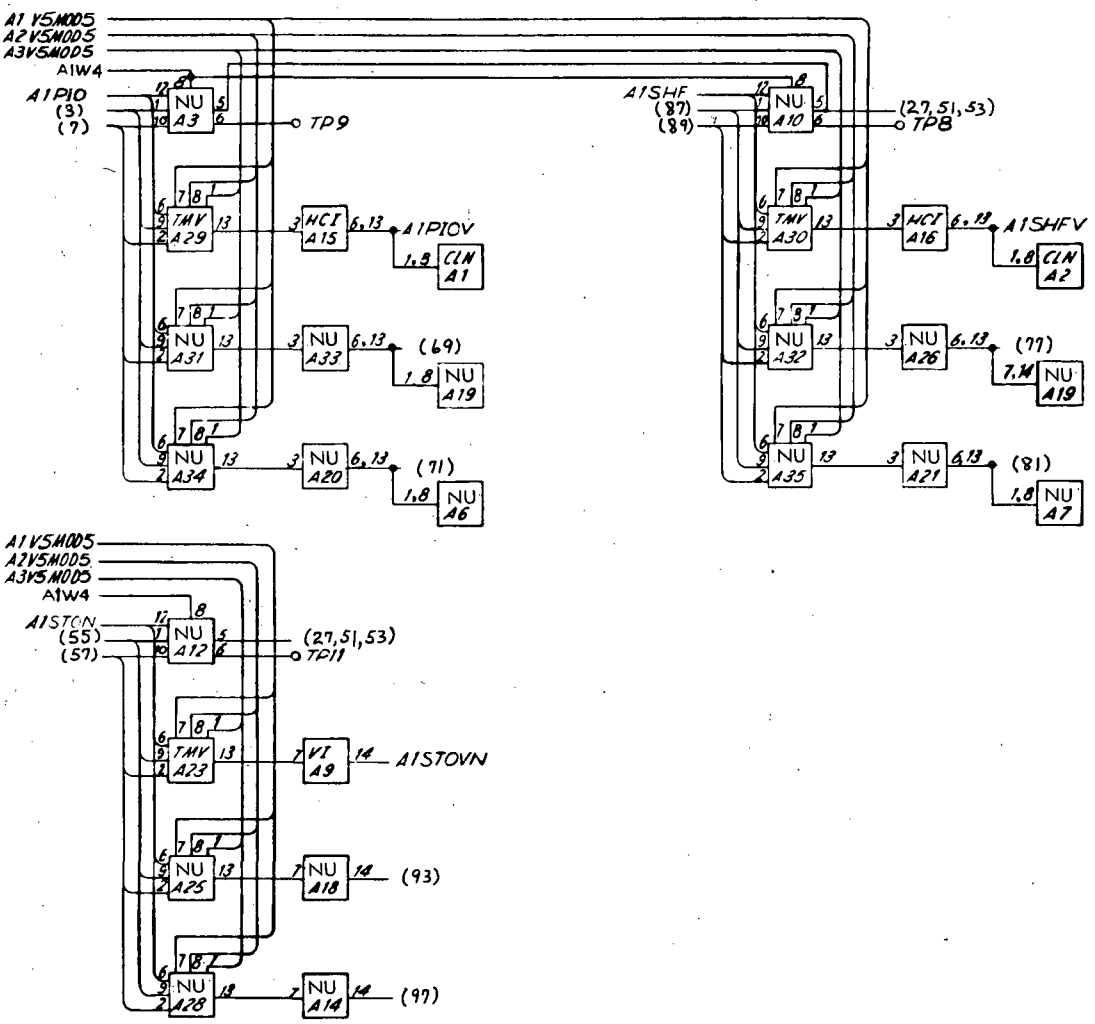
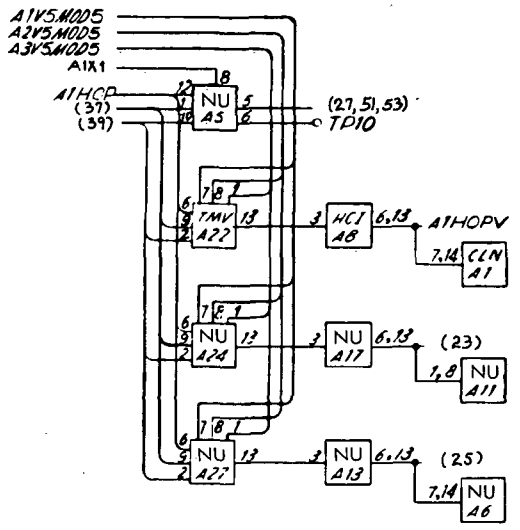


Figure 10-20. Operation Code Voters, Logic Diagram (Sheet 1 of 4)

A4A5A



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	A3V4M0D5	51	
3		53	
5	A2V5M0D5	55	
7		57	
9	A1PI0	59	A1ST0N
11	A1V5M0D5	61	V3
13	V3	63	V1
15	V1	65	SIG RET
17	SIG RET	67	A1PI0V
19		69	
21	A1H0PV	71	
23		73	V3
25		75	V1
27		77	
29	A3V5M0D5	79	A1SHFV
31	A2V5M0D5	81	
33	A1V5M0D5	83	A1W4
35	A1X1	85	SIG RET
37		87	
39		89	
41	A1H0P	91	A1SHF
43	A3V5M0D5	93	
45	A2V5M0D5	95	A1ST0VN
47	A1V5M0D5	97	
49	A1W4		

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A4A5A

THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2	SIG RET	17	
3	V1	18	
4	V3	19	
5		20	
6		21	
7		22	
8	SIG RET	23	
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	

Figure 10-20. Operation Code Voters, Logic Diagram (Sheet 2)

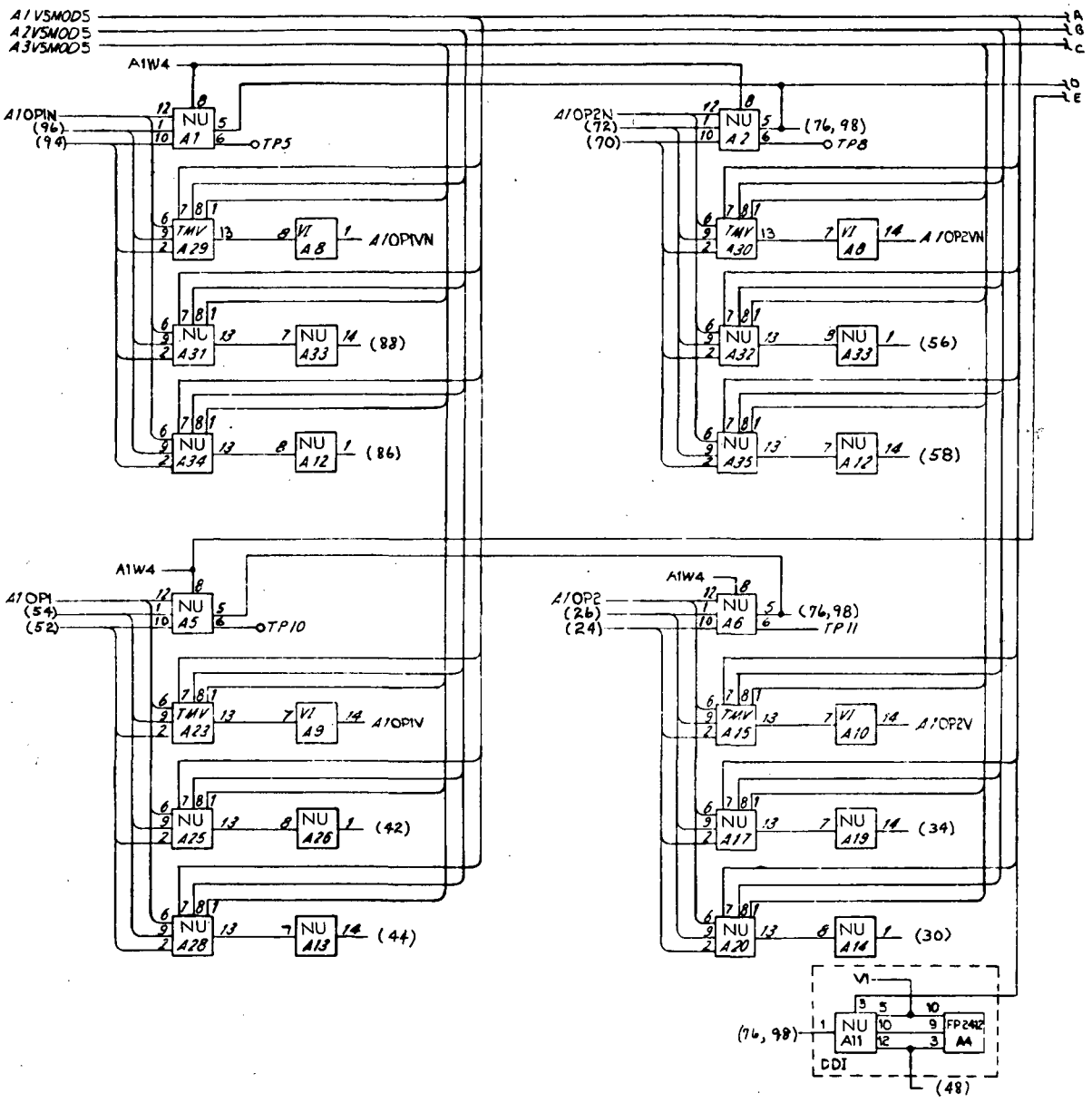
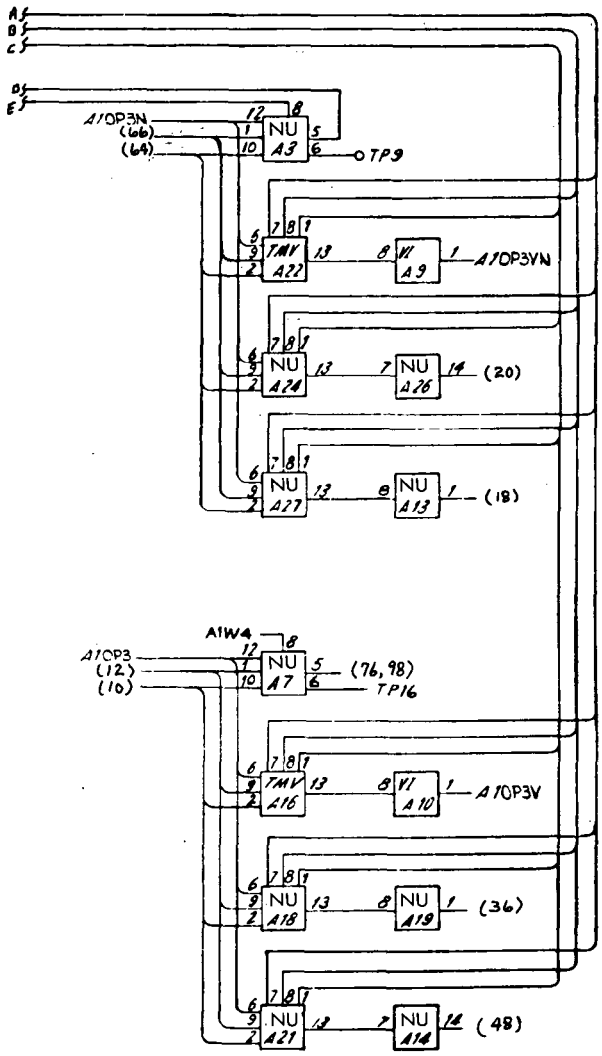


Figure 10-20. Operation Code Voters, Logic Diagram (Sheet 3)



A4A5B

CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	NU1	52	
4	NU2	54	
6	NU3	56	
8	A10P3	58	
10		60	A10P2VN
12		62	A10P3N
14	A1W4	64	
16	A10P3VN	66	
18		68	A10P2N
20		70	
22	A10P2	72	
24		74	A1W4
26		76	
28	A1W4	78	A1W4
30		80	A1V5M0D5
32	A10P2V	82	A2V5M0D5
34		84	A3V5M0D5
36		86	
38		88	
40	A10P3V	90	A10P1VN
42		92	A10P1N
44		94	
46	A10P1V	96	
48		98	
50	A10P1		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	A3V5M0D5
2	SIG RET	17	NU1
3	V1	18	NU2
4	V3	19	NU3
5		20	
6		21	
7		22	
8	SIG RET	23	A2V5M0D5
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	A1V5M0D5

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate it
5. Prefix Reference Designations as Follows: A4A5B

Figure 10-20. Operation Code Voters, Logic Diagram (Sheet 4)

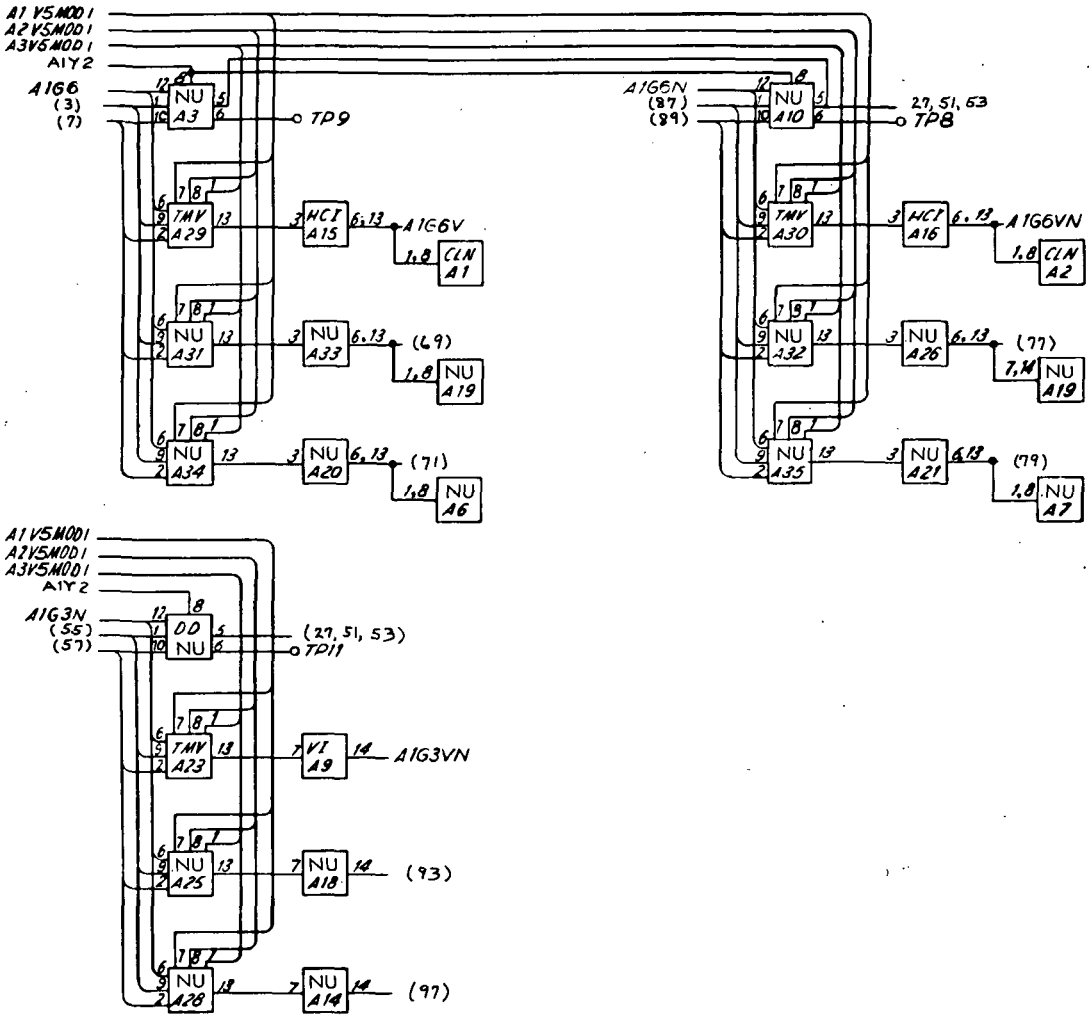
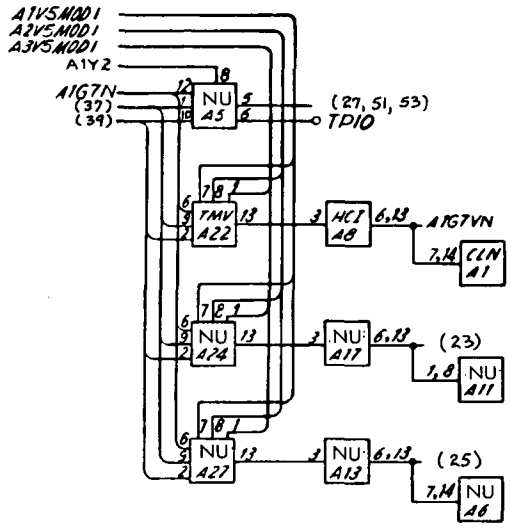


Figure 10-21. Timing Gate and Operation Code Voters, Logic Diagram (Sheet 1 of 4)

A4A6A



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	A3V5M0D1	51	
3		53	
5	A2V5M0D1	55	
7		57	
9	A1G6	59	A1G3N
11	A1V5M0D1	61	V3
13	V3	63	V1
15	V1	65	SIG RET
17	SIG RET	67	A1G6V
19		69	
21	A1G7VN	71	
23		73	V3
25		75	V1
27		77	
29	A3V5M0D1	79	A1G6VN
31	A2V5M0D1	81	
33	A1V5M0D1	83	A1Y2
35	A1Y2	85	SIG RET
37		87	
39		89	
41	A1G7N	91	A1G6N
43	A3V5M0D1	93	
45	A2V5M0D1	95	A1G3VN
47	A1V5M0D1	97	
49	A1Y2		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2	SIG RET	17	
3	V1	18	
4	V3	19	
5		20	
6		21	
7		22	
8	SIG RET	23	
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotten Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A4A6A

Figure 10-21. Timing Gate and Operation Code Voters, Logic Diagram (Sheet 2)

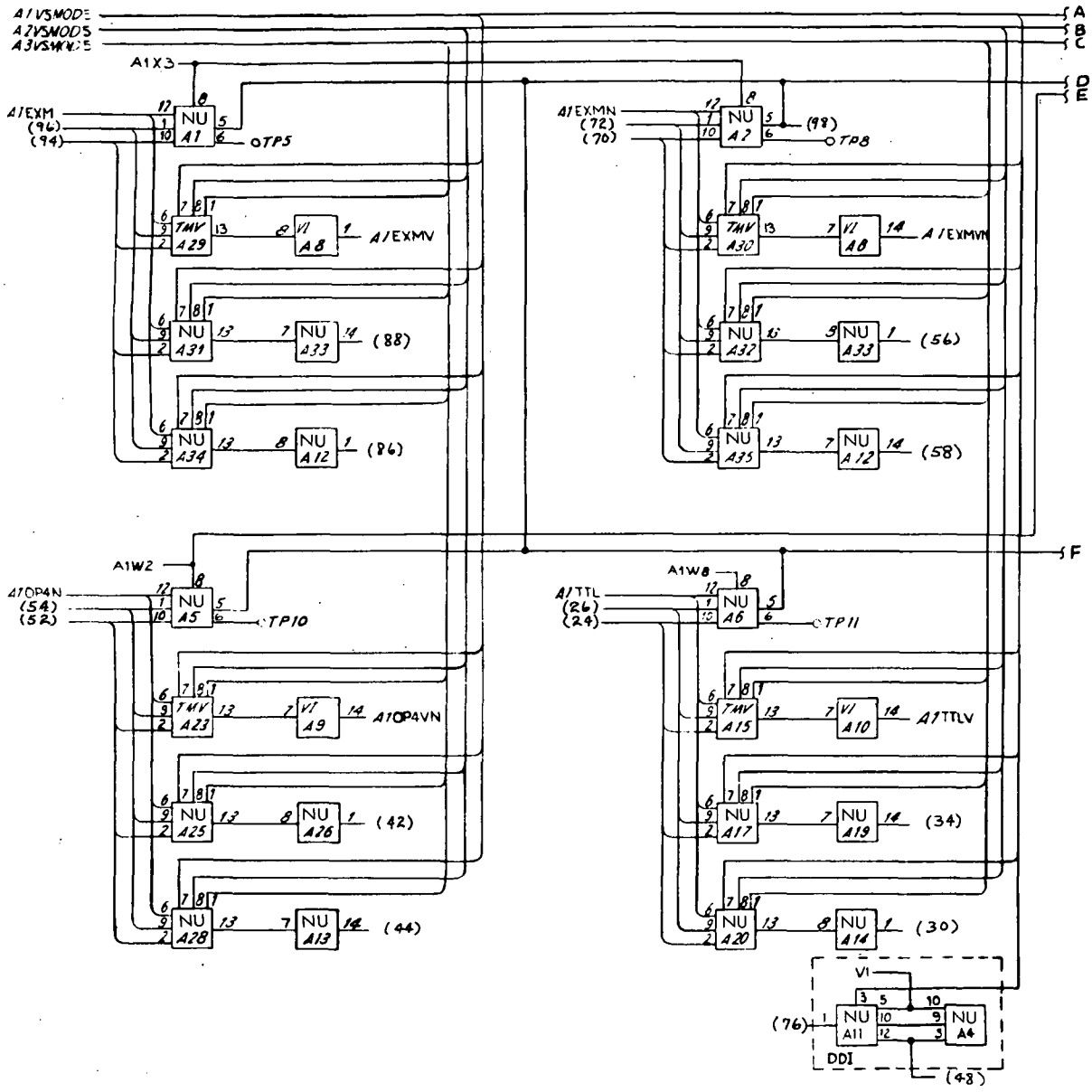
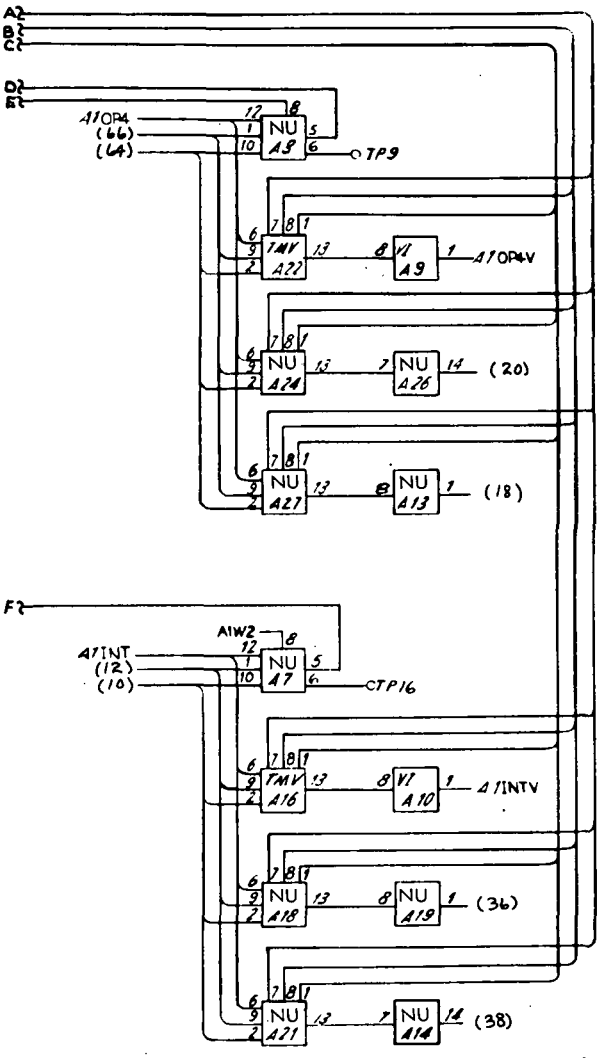


Figure 10-21. Timing Gate and Operation Code Voters, Logic Diagram (Sheet 3)



A4A6B

CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	NU1	52	
4	NU2	54	
6	NU3	56	
8	A1INT	58	
10		60	A1EXMVN
12		62	A10P4
14	A1W2	64	
16	A10P4V	66	
18		68	A1EXMN
20		70	
22	A1TTL	72	
24		74	A1W2
26		76	
28	A1W8	78	A1X3
30		80	A1V5M0D5
32	A1TTLV	82	A2V5M0D5
34		84	A3V5M0D5
36		86	
38		88	
40	A1INTV	90	A1EXMV
42		92	A1EXM
44		94	
46	A10P4VN	96	
48		98	
50	A10P41		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	A3V5M0D5
2	SIG RET	17	NU1
3	V1	18	NU2
4	V3	19	NU3
5		20	
6		21	
7		22	
8	SIG RET	23	A2V5M0D5
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	A1V5M0D5

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A4A6B

Figure 10-21. Timing Gate and Operation Code Voters, Logic Diagram (Sheet 4)

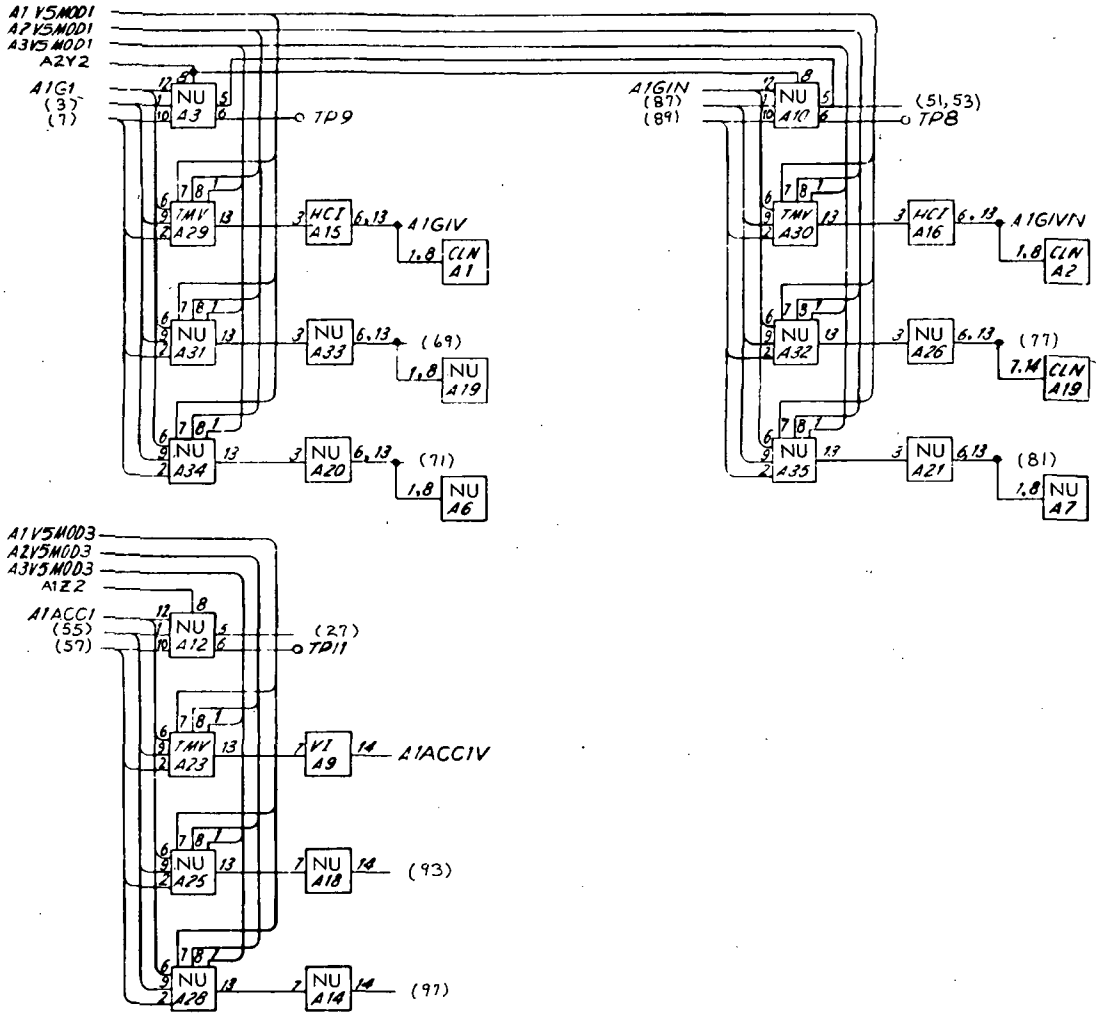
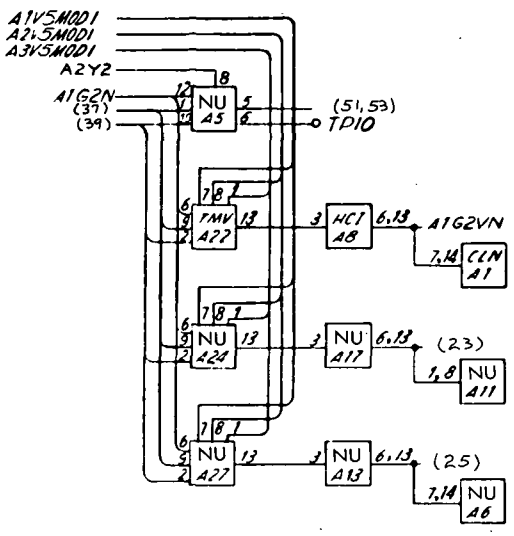


Figure 10-22. Timing and Add-Subtract Voters, Logic Diagram (Sheet 1 of 4)

A4A7A



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	A3V5MOD1	51	
3		53	
5	A2V5MOD1	55	
7		57	
9	A1G1	59	A1ACC1
11	A1V5MOD1	61	V3
13	V3	63	V1
15	V1	65	SIG RET
17	SIG RET	67	A1G1V
19		69	
21	A1G2VN	71	
23		73	V3
25		75	V1
27		77	
29	A3V5MOD1	79	A1G1VN
31	A2V5MOD1	81	
33	A1V5MOD1	83	A1Z2
35	A2Y2	85	SIG RET
37		87	
39		89	
41	A1G2N	91	A1G1N
43	A3V5MOD3	93	
45	A2V5MOD3	95	A1ACC1V
47	A1V5MOD3	97	
49	A2Y2		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2	SIG RET	17	
3	V1	18	
4	V3	19	
5		20	
6		21	
7		22	
8	SIG RET	23	
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A4A7A

Figure 10-22. Timing and Add-Subtract Voters, Logic Diagram (Sheet 2)

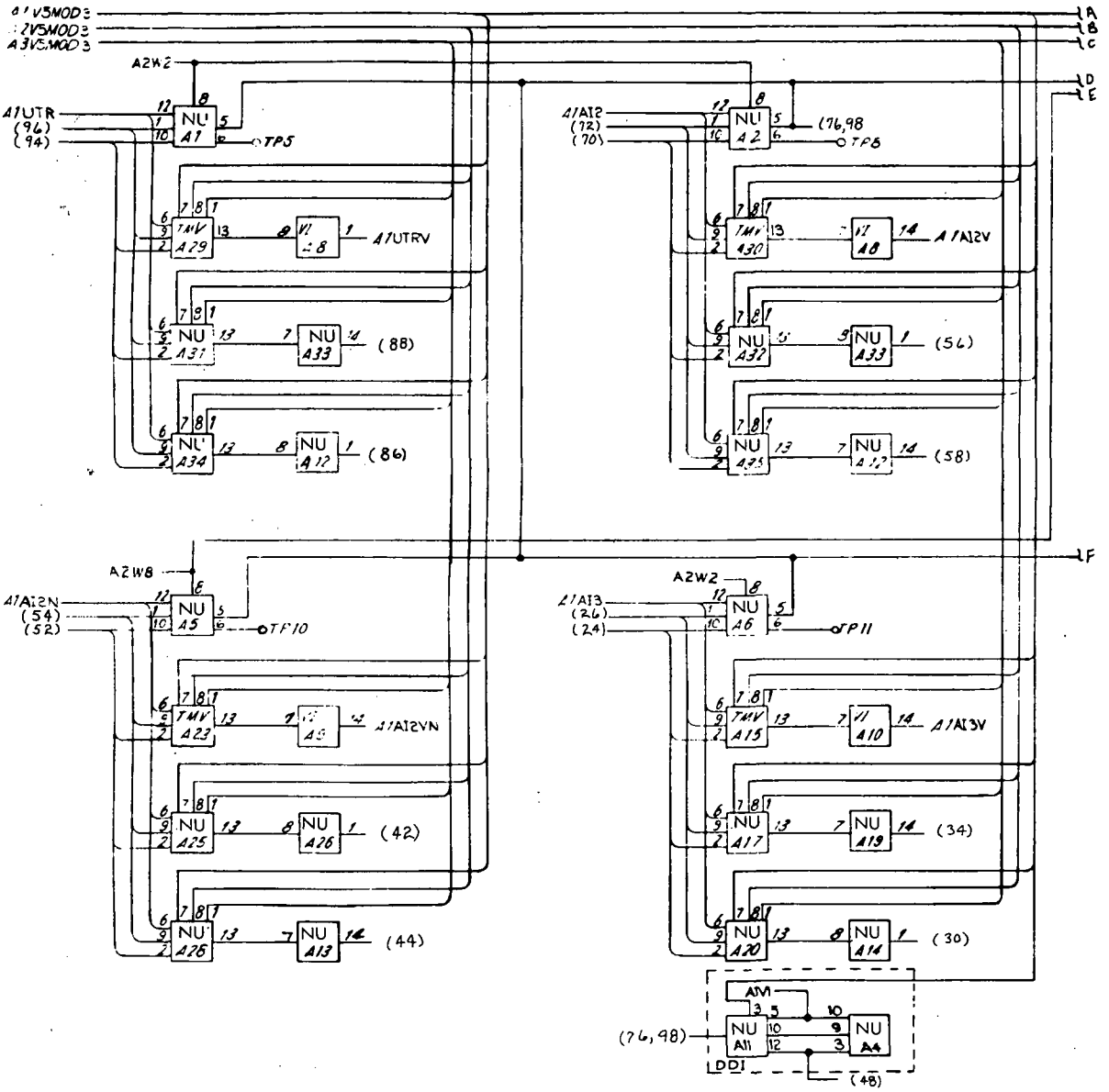
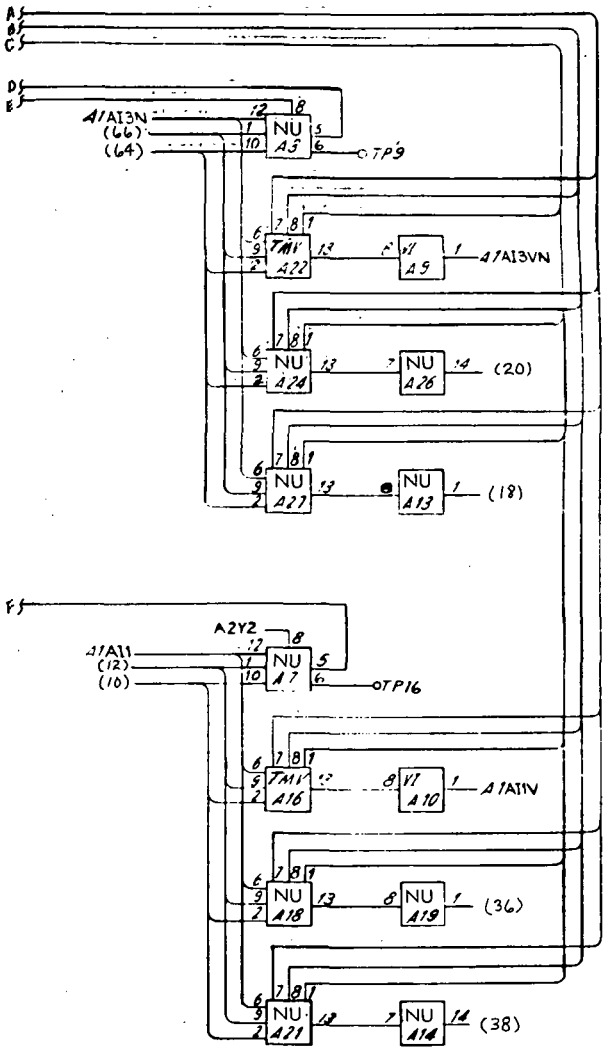


Figure 10-22. Timing and Add-Subtract Voters, Logic Diagram (Sheet 3)

A4A7,B



CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	NU1	52	
4	NU2	54	
6	NU3	56	
8	A1AI1	58	
10		60	A1AI2V
12		62	A1AI3N
14	A2Y2	64	
16	A1AI3VN	66	
18		68	A1AI2
20		70	
22	A1AI3	72	
24		74	A2W8
26		76	
28	A2W2	78	A2W2
30		80	A1V5MOD3
32	A1AI3V	82	A2V5MOD3
34		84	A3V5MOD3
36		86	
38		88	
40	A1AI1V	90	A1UTRV
42		92	A1UTR
44		94	
46	A1AI2VN	96	
48		98	
50	A1AI2N		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	A3V5MOD3
2	SIG RET	17	NU1
3	V1	18	NU2
4	V3	19	NU3
5		20	
6		21	
7		22	
8	SIG RET	23	A2V5MOD3
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	A1V5MOD3

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A4A7B

Figure 10-22. Timing and Add-Subtract Voters, Logic Diagram (Sheet 4)

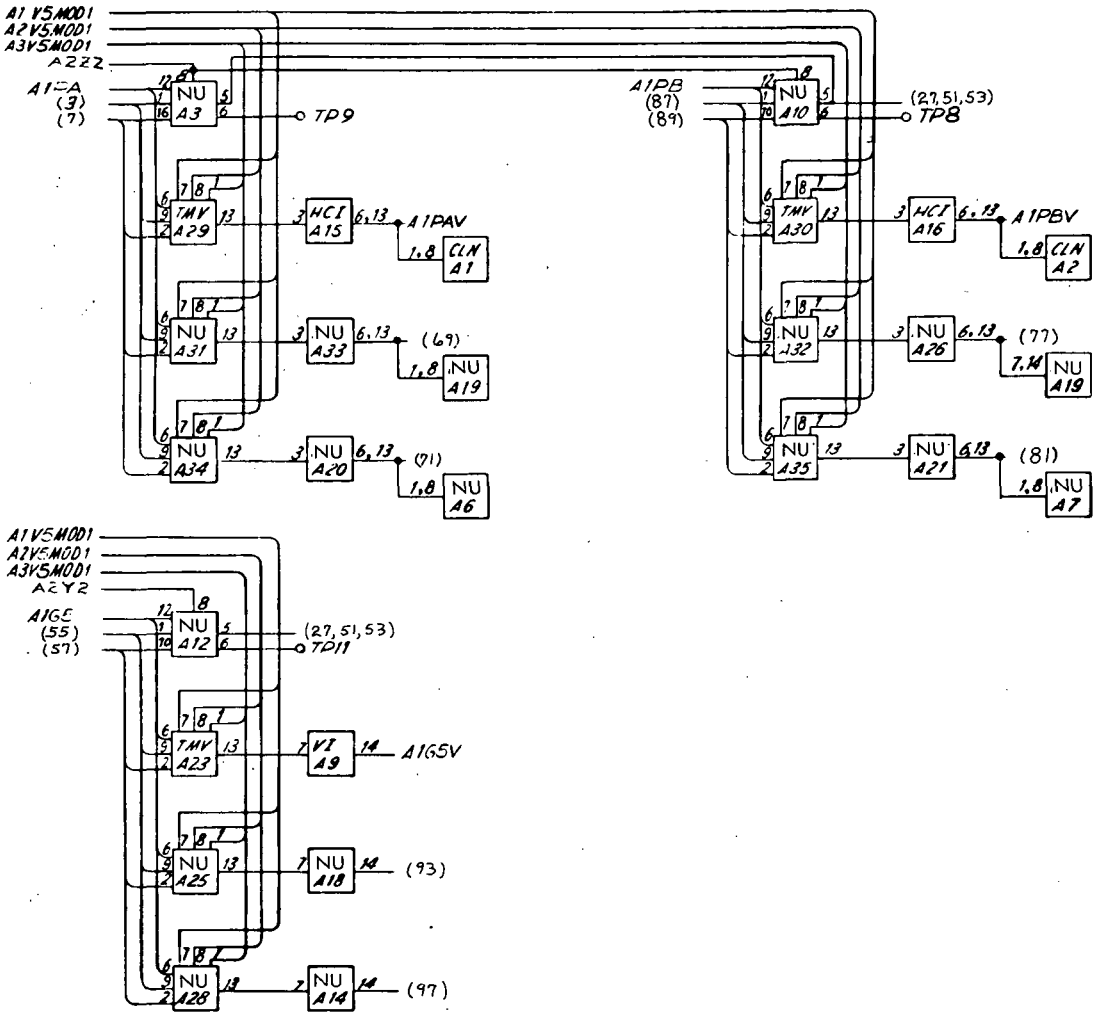
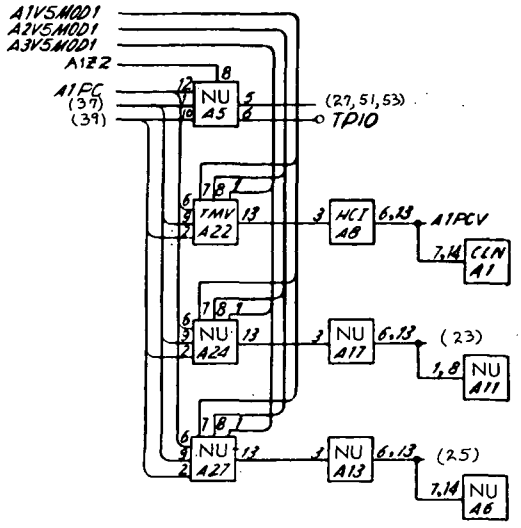


Figure 10-23. Timing Voters, Logic Diagram (Sheet 1 of 4)

A4A8A



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	A3V5MOD1	51	
3		53	
5	A2V5MOD1	55	
7		57	
9	A1PA	59	A1G5
11	A1V5MOD1	61	V3
13	V3	63	V1
15	V1	65	SIG RET
17	SIG RET	67	A1PAV
19		69	
21	A1PCV	71	
23		73	V3
25		75	V1
27		77	
29	A3V5MOD1	79	A1PBV
31	A2V5MOD1	81	
33	A1V5MOD1	83	A2Y2
35	A1Z2	85	SIG RET
37		87	
39		89	
41	A1PC	91	A1PB
43	A3V5MOD1	93	
45	A2V5MOD1	95	A1G5V
47	A1V5MOD1	97	
49	A2Z2		

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A4A8A

THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2	SIG RET	17	
3	V1	18	
4	V3	19	
5		20	
6		21	
7		22	
8	SIG RET	23	
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	

Figure 10-23. Timing Voters, Logic Diagram (Sheet 2)

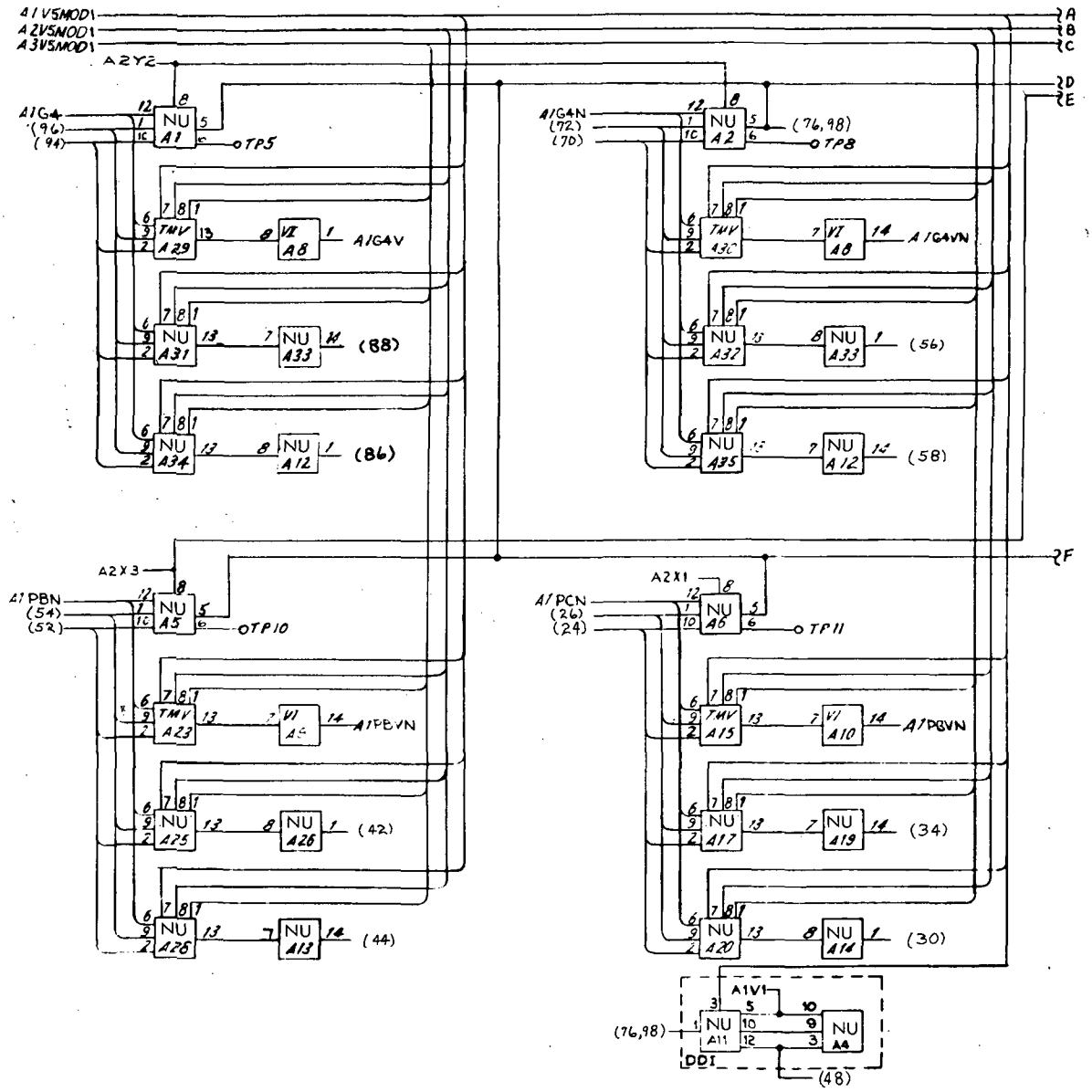
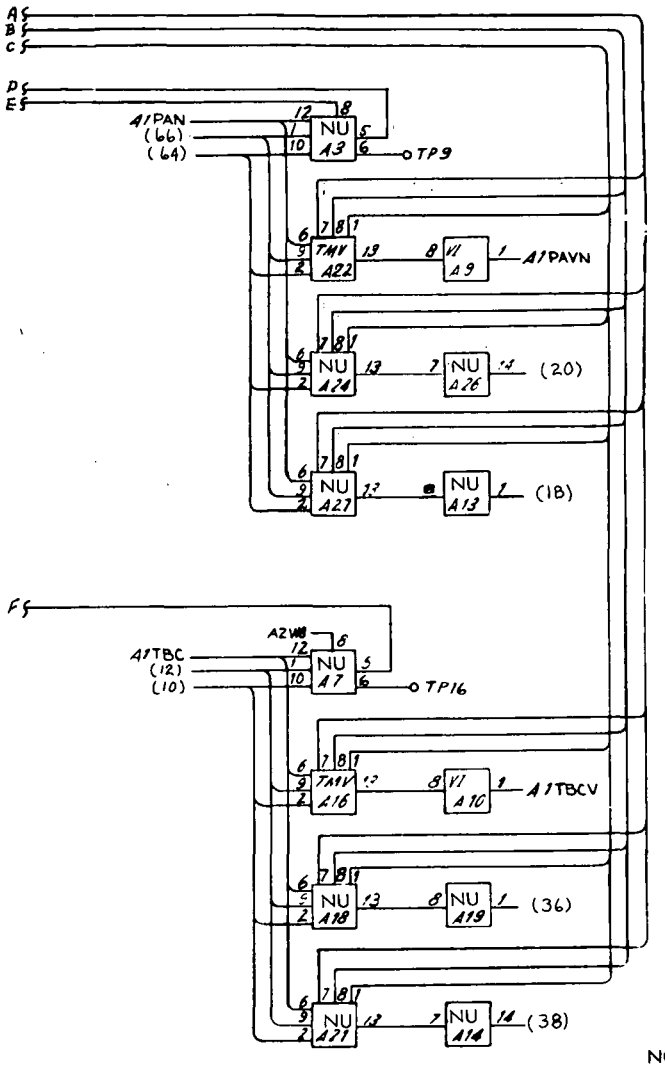


Figure 10-23. Timing Voters, Logic Diagram (Sheet 3)

A4A8B



THRU PINS			
Pin	Signal	Pin	Signal
1		16	A3V5MOD1
2	SIG RET	17	NU1
3	V1	18	NU2
4	V3	19	NU3
5		20	
6		21	
7		22	
8	SIG RET	23	A2V5MOD1
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	A1V5MOD1

CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	NU1	52	
4	NU2	54	
6	NU3	56	
8	A1TBC	58	
10		60	A1G4VN
12		62	A1PAN
14	A2W8	64	
16	A1PAVN	66	
18		68	A1G4N
20		70	
22	A1PCN	72	
24		74	A2X3
26		76	
28	A2X1	78	A2Y2
30		80	A1V5MOD1
32	A1PCVN	82	A2V5MOD1
34		84	A3V5MOD1
36		86	
38		88	
40	A1TBCV	90	A1G4V
42		92	A1G4
44		94	
46	A1PBVN	96	
48		98	
50	A1PBN		

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A4A8B

Figure 10-23. Timing Voters, Logic Diagram (Sheet 4)

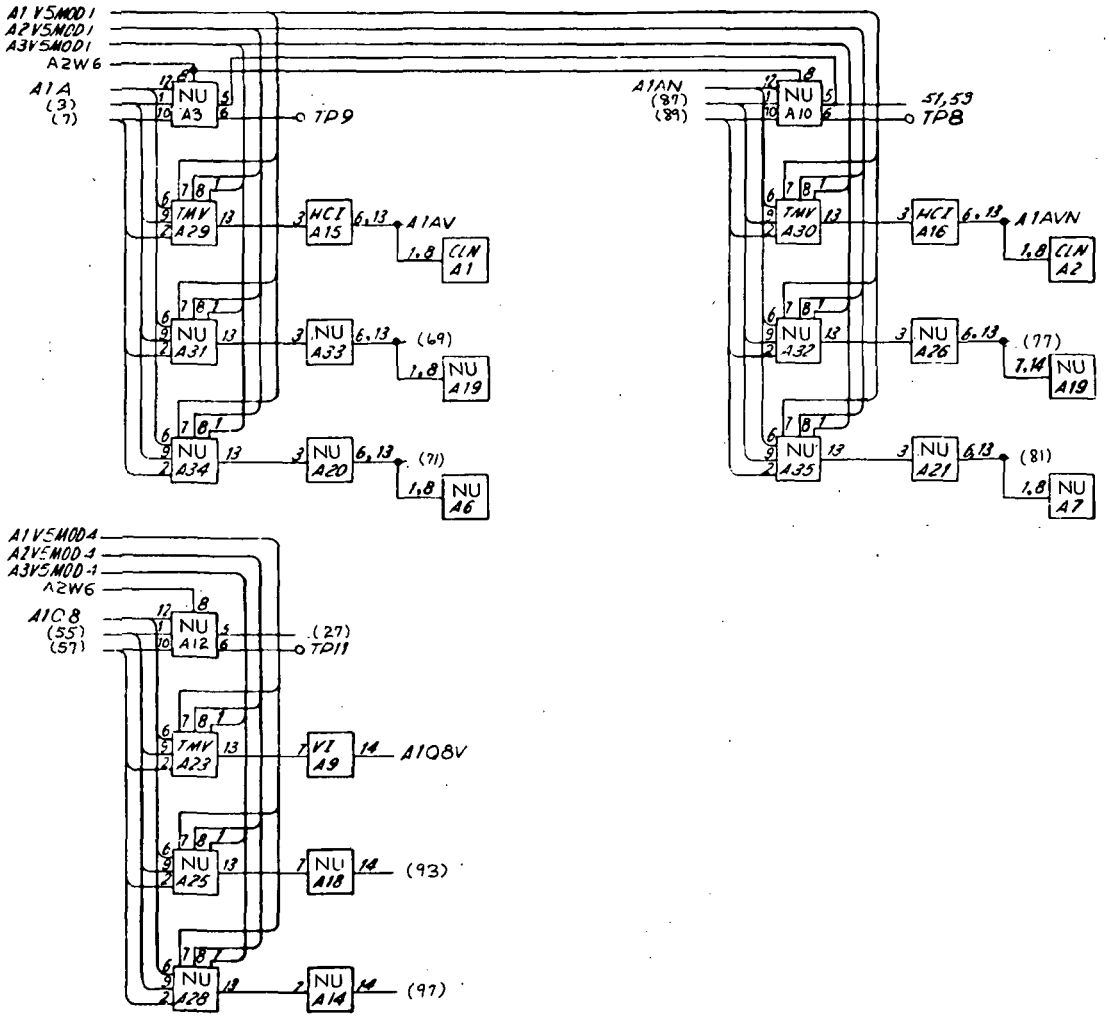
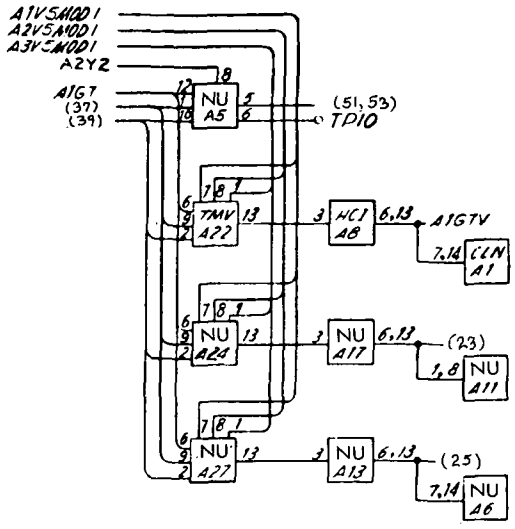


Figure 10-24. Timing and Multiply-Divide Voters, Logic Diagram (Sheet 1 of 4)

A4A9A



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	A3V5M0D1	51	
3		53	
5	A2V5M0D1	55	
7		57	
9	A1A	59	A1Q8
11	A1V5M0D1	61	V3
13	V3	63	V1
15	V1	65	SIG RET
17	SIG RET	67	A1AV
19		69	
21	A1G7V	71	
23		73	V3
25		75	V1
27		77	
29	A3V5M0D1	79	A1AVN
31	A2V5M0D1	81	
33	A1V5M0D1	83	A2W6
35	A2Y2	85	SIG RET
37		87	
39		89	
41	A1G7	91	A1AN
43	A3V5M0D4	93	
45	A2V5M0D4	95	A1Q8V
47	A1V5M0D4	97	
49	A2W6		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2	SIG RET	17	
3	V1	18	
4	V3	19	
5		20	
6		21	
7		22	
8	SIG RET	23	
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U. Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A4A9A

Figure 10-24. Timing and Multiply-Divide Voters, Logic Diagram (Sheet 2)

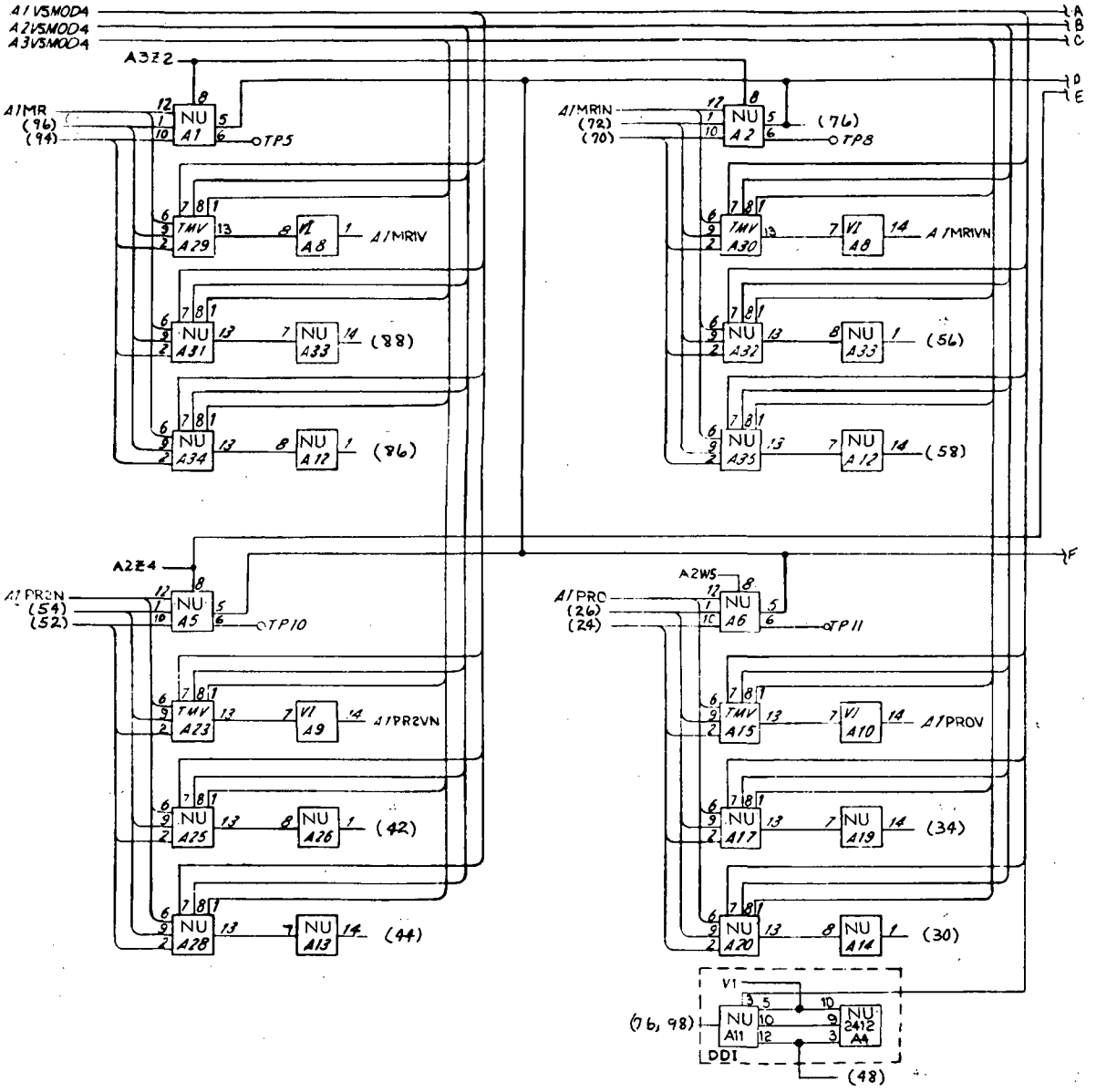
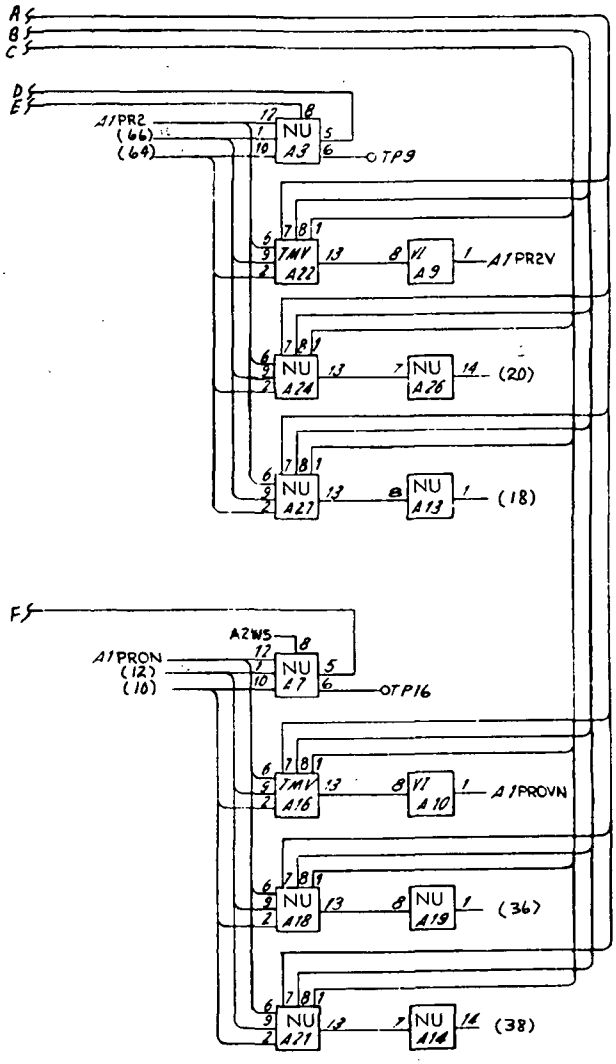


Figure 10-24. Timing and Multiply-Divide Voters, Logic Diagram (Sheet 3)

A4A9B



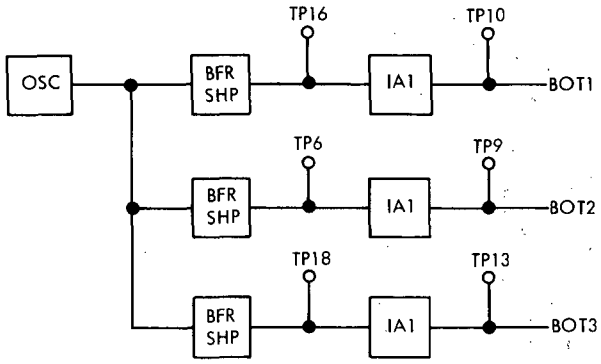
CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	NU1	52	
4	NU2	54	
6	NU3	56	
8	A1PR0N	58	
10		60	A1MR1VN
12		62	A1PR2
14	A2W5	64	
16	A1PR2V	66	
18		68	A1MR1N
20		70	
22	A1PR0	72	
24		74	A2Z4
26		76	
28	A2W5	78	A3Z2
30		80	A1V5M0D4
32	A1PR0V	82	A2V5M0D4
34		84	A3V5M0D4
36		86	
38		88	
40	A1PR0VN	90	A1MR1V
42		92	A1MR1
44		94	
46	A1PR2VN	96	
48		98	
50	A1PR2N		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	A3V5V0D4
2	SIG RET	17	NU1
3	V1	18	NU2
4	V3	19	NU3
5		20	
6		21	
7		22	
8	SIG RET	23	A2V5M0D4
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	A1V5M0D4

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. *Dotted Line (if any) Indicates Internal ULD Connection*
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A4A9B

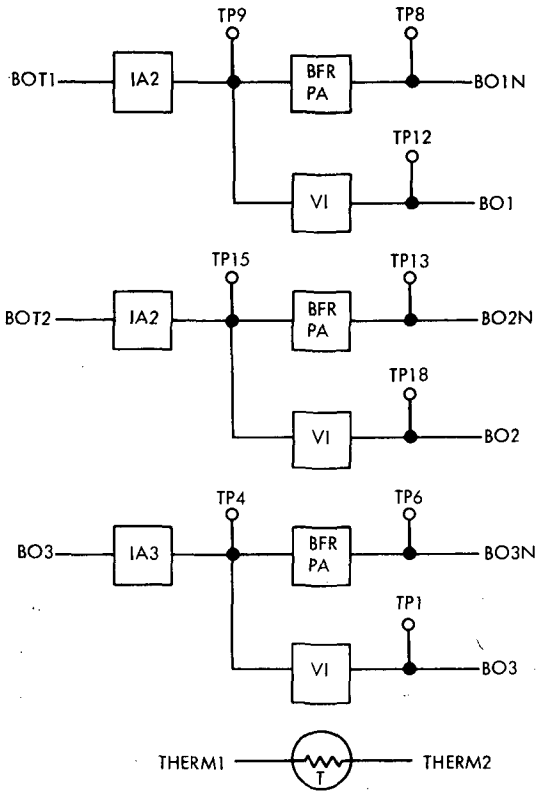
Figure 10-24. Timing and Multiply-Divide Voters, Logic Diagram (Sheet 4)



NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A4A11A (left page), A4A11B (right page)

Figure 10-25. Oscillator and Buffer, Logic Diagram (Sheet 1 of 2)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	SIG RET	51	SIG RET
3	SIG RET	53	SIG RET
5	SIG RET	55	V1
7	SIG RET	57	V1
9	SIG RET	59	V3
11	V20	61	V3
13	V20	63	V20
15	V5	65	V20
17	V5	67	SIG RET
19	V1	69	SIG RET
21	V1	71	SIG RET
23	SIG RET	73	SIG RET
25	SIG RET	75	SIG RET
27	SIG RET	77	V5
29	SIG RET	79	V5
31	SIG RET	81	V1
33	V3	83	V1
35	V3	85	V3
37	V20	87	V3
39	V20	89	SIG RET
41	V5	91	SIG RET
43	V5	93	SIG RET
45	SIG RET	95	SIG RET
47	SIG RET	97	SIG RET
49	SIG RET		

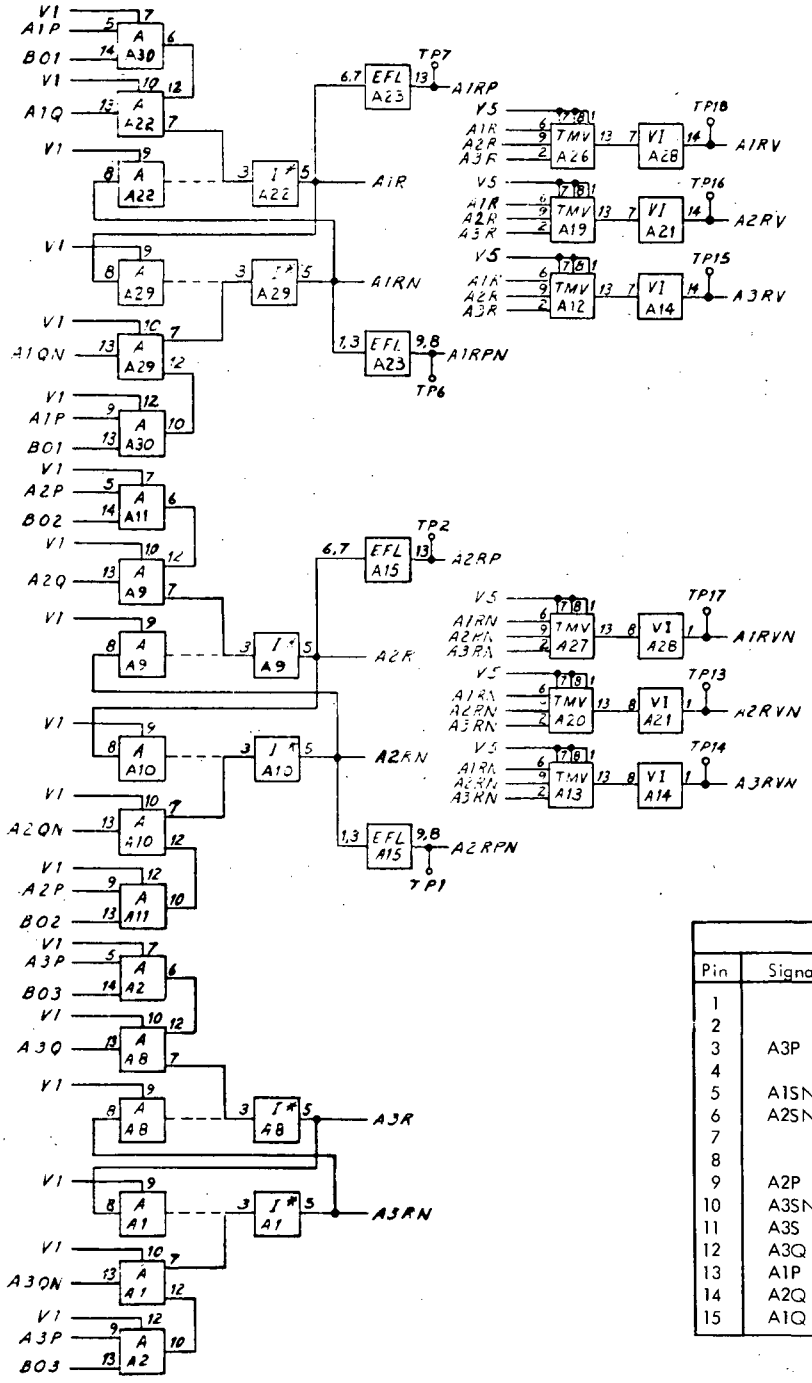
A4A11A

A4A11B

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	V5	52	V5
4	|	54	V5
6	⊥	56	BO1N
8	V1	58	SIG RET
10	V1	60	|
12	BO2	62	⊥
14	SIG RET	64	V1
16	|	66	|
18	⊥	68	|
20	V3	70	⊥
22	V3	72	SIG RET
24	BO2N	74	SIG RET
26	SIG RET	76	V3,
28	|	78	V3
30	|	80	BO3N
32	⊥	82	SIG RET
34	V3	84	|
36	V3	86	⊥
38	SIG RET	88	BO3
40	SIG RET	90	V1
42	THERM1	92	V1
44	V1	94	V5
46	V1	96	|
48	BO1	98	⊥
50	THERM2		

THRU - PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2		17	
3		18	BOT2
4		19	
5		20	
6		21	
7		22	
8		23	BOT1
9		24	
10		25	
11		26	
12		27	
13		28	BOT3
14		29	
15		30	

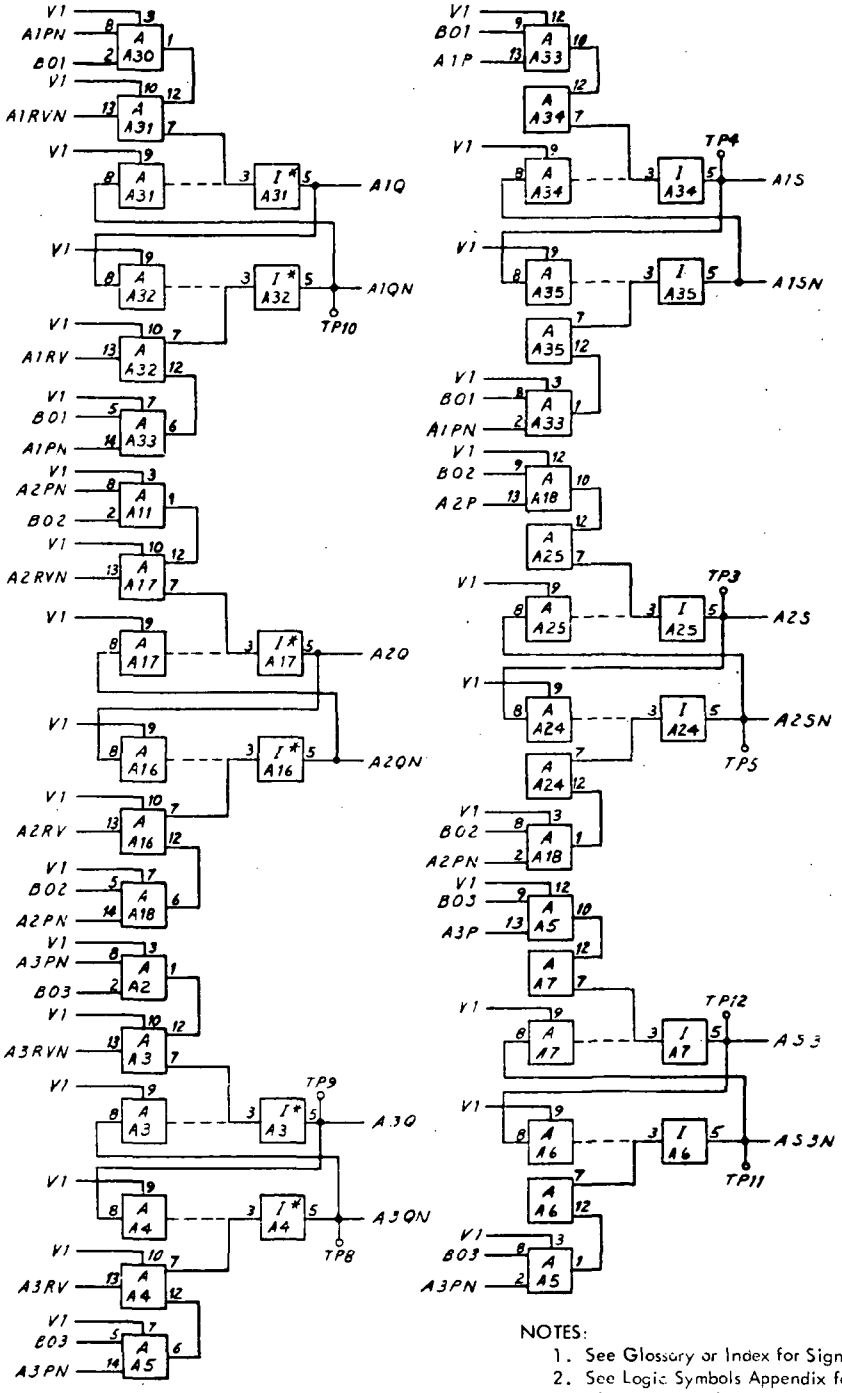
Figure 10-25. Oscillator and Buffer, Logic Diagram (Sheet 2)



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	A2RPN	51	V5
3	V1	53	V5
5	A2RP	55	SIG RET
7	V1	57	
9	⊥	59	
11		61	
13	A1RPN	63	
15	V1	65	
17	A1RP	67	
19	V1	69	
21	BO3	71	
23	V3	73	
25	BO1	75	
27	V3	77	
29	⊥	79	
31		81	
33	SIG RET	83	V3
35	⊥	85	⊥
37		87	
39		89	
41	BO2	91	V1
43	SIG RET	93	⊥
45	SIG RET	95	
47	V5	97	
49	V5		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	BO3
2		17	
3	A3P	18	A3PN
4		19	A1S
5	A1SN	20	A2S
6	A2SN	21	
7		22	A3R
8		23	A3RN
9	A2P	24	BO2
10	A3SN	25	A2PN
11	A3S	26	BO1
12	A3Q	27	A3QN
13	A1P	28	A1PN
14	A2Q	29	A2QN
15	A1Q	30	A1QN

Figure 10-26. Clock Generator Timing Logic, Logic Diagram (Sheet 1 of 4)



NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A4A12A
6. Asterisk indicates load resistor not connected.

Figure 10-26. Clock Generator Timing Logic, Logic Diagram (Sheet 2)

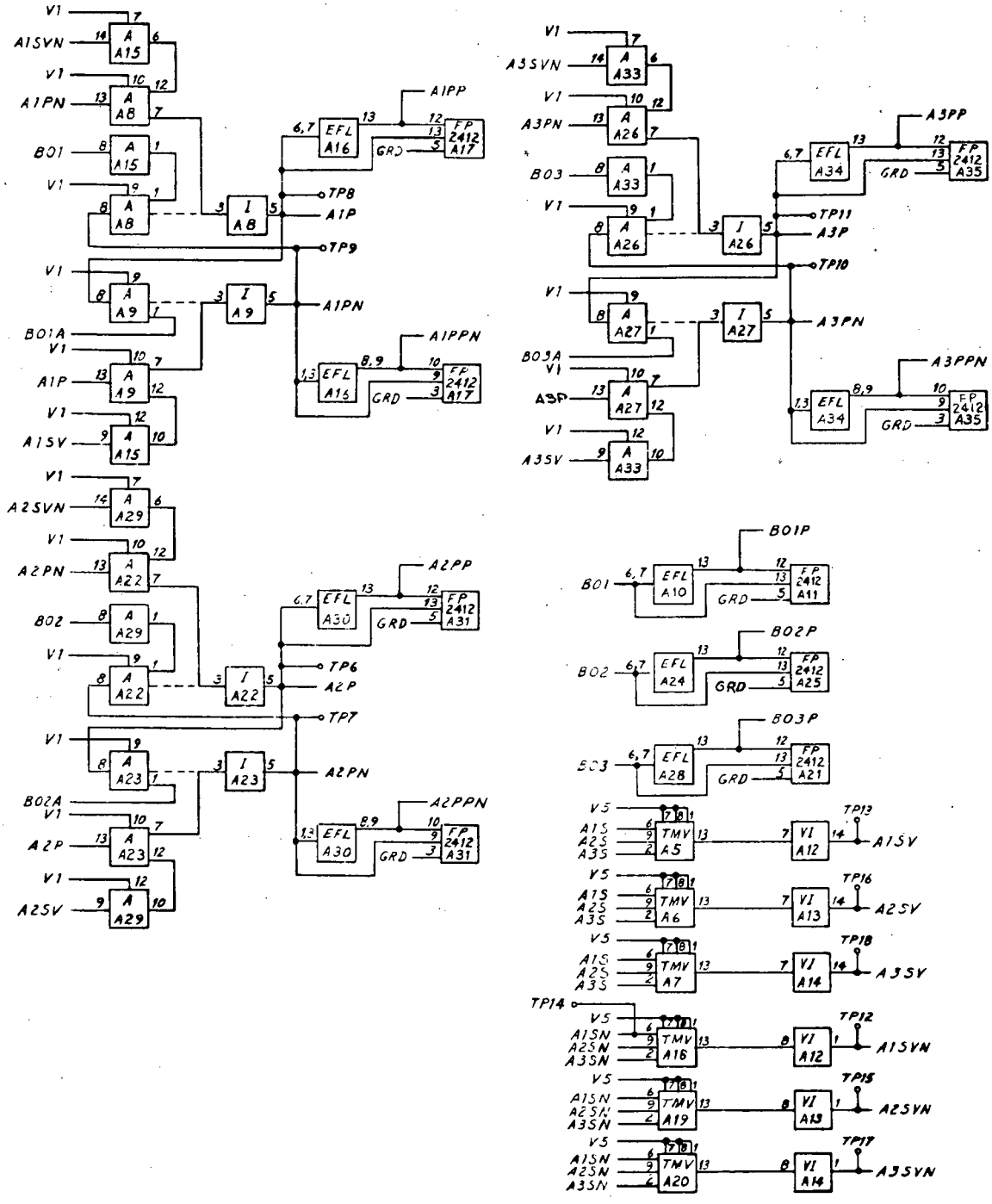
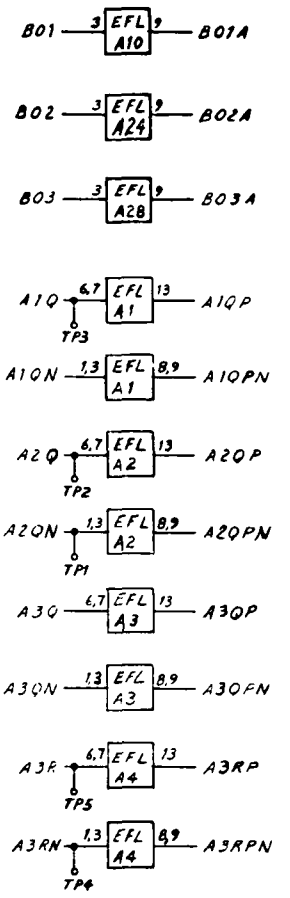


Figure 10-26. Clock Generator Timing Logic, Logic Diagram (Sheet 3)



CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	V1	52	V5
4	BO3P	54	A3RPN
6	V3	56	A2QP
8	V3	58	BO1P
10	A3PP	60	BO2P
12	V3	62	SIG RET
14	V1	64	SIG RET
16		66	A2PPN
18		68	A3QPN
20	SIG RET	70	A2QP
22		72	A1PP
24		74	A2PP
26		76	V1
28		78	
30	A3PPN	80	
32	SIG RET	82	A1PPN
34		84	A2QPN
36		86	A1QP
38		88	SIG RET
40		90	V3
42		92	
44	A3RP	94	
46	SIG RET	96	A1QPN
48	V5	98	V1
50	V5		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	BO3
2		17	
3	A3P	18	A3PN
4		19	A1S
5	A1SN	20	A2S
6	A2SN	21	
7		22	A3R
8		23	A3RN
9	A2P	24	BO2
10	A3SN	25	A2PN
11	A3S	26	BO1
12	A3Q	27	A3QN
13	A1P	28	A1PN
14	A2Q	29	A2QN
15	A1Q	30	A1QN

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate it
5. Prefix Reference Designations as Follows: A4A12B

Figure 10-26. Clock Generator Timing Logic, Logic Diagram (Sheet 4)

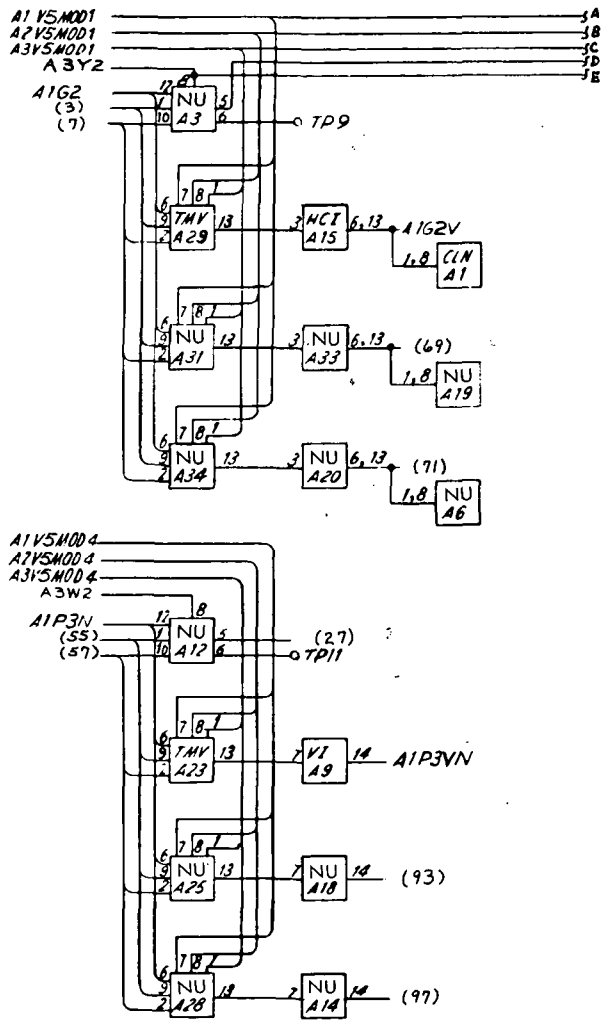
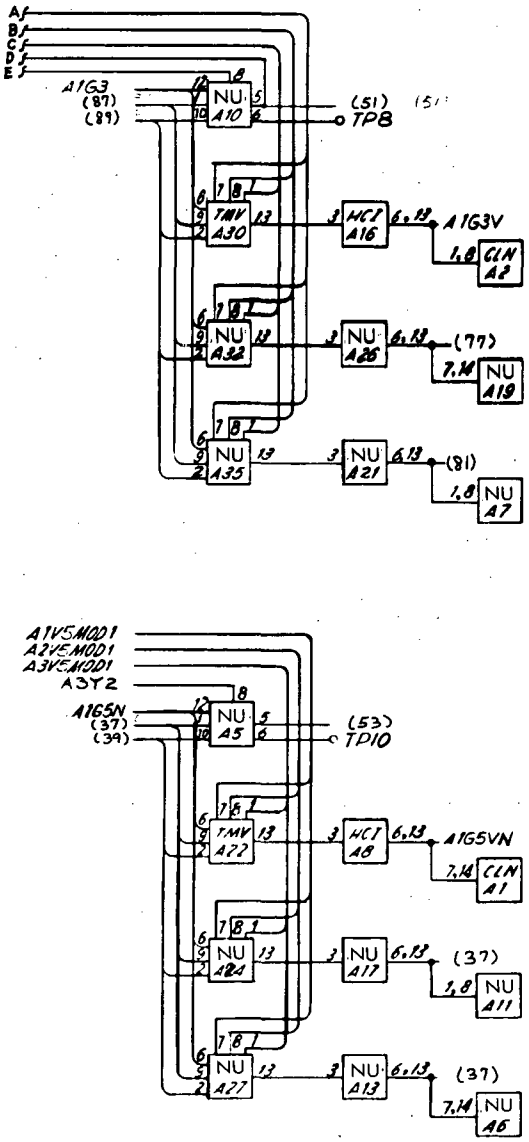


Figure 10-27. Timing and Multiply-Divide Voters, Logic Diagram (Sheet 1 of 4)



A4A13A

THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2	SIG RET	17	
3	V1	18	
4	V3	19	
5		20	
6		21	
7		22	
8	SIG RET	23	
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	

CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	A3V5M0D1	51	
3		53	
5	A2V5M0D1	55	
7		57	
9	A1G2	59	A1P3N
11	A1V5M0D1	61	V3
13	V3	63	V1
15	V1	65	SIG RET
17	SIG RET	67	A1G2V
19		69	
21	A1G5VN	71	
23		73	V3
25		75	V1
27		77	
29	A3V5M0D1	79	A1G3V
31	A2V5M0D1	81	
33	A1V5M0D1	83	A3W2
35	A3Y2	85	SIG RET
37		87	
39		89	
41	A1G5N	91	A1G3
43	A3V5M0D4	93	
45	A2V5M0D4	95	A1P3VN
47	A1V5M0D4	97	
49	A3Y2		

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotten Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A4A13A

Figure 10-27. Timing and Multiply-Divide Voters, Logic Diagram (Sheet 2)

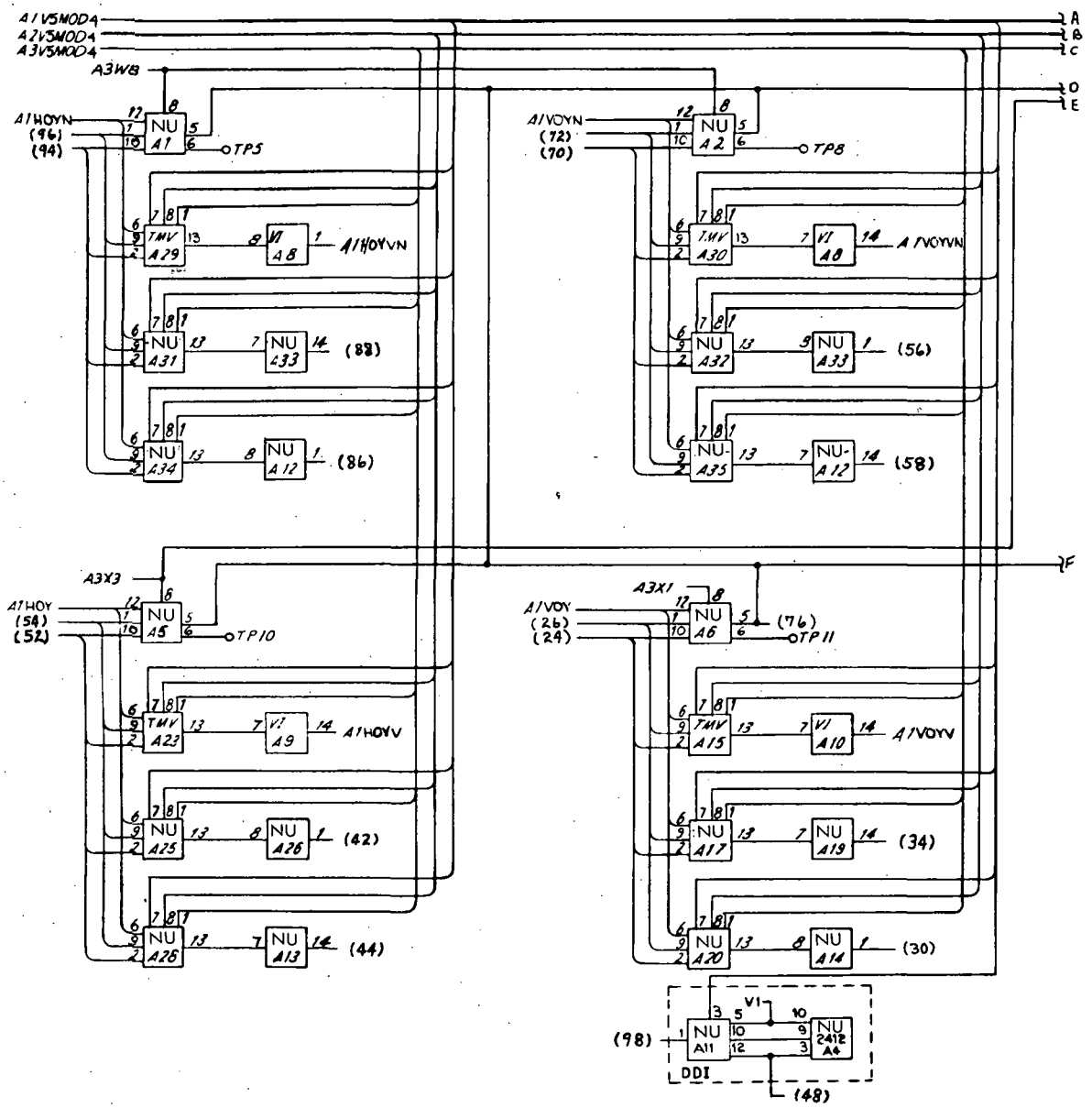
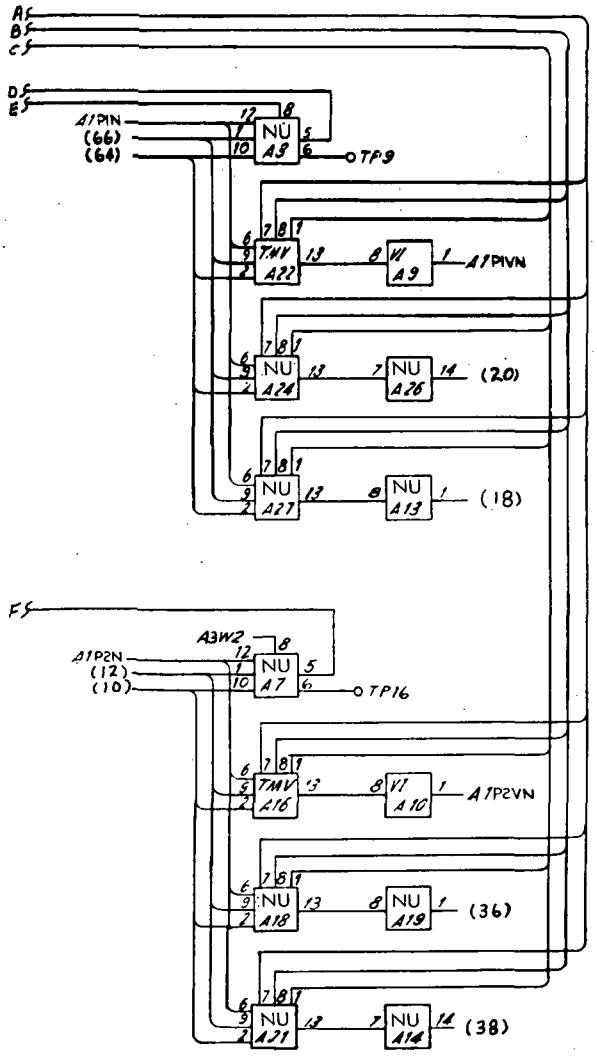


Figure 10-27. Timing and Multiply-Divide Voters, Logic Diagram (Sheet 3)

A4A13B



CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	NU1	52	
4	NU2	54	
6	NU3	56	
8	A1P2N	58	
10		60	A1VOYVN
12		62	A1P1N
14	A3W2	64	
16	A1P1VN	66	
18		68	A1VOYN
20		70	
22	A1VOY	72	
24		74	A3X3
26		76	
28	A3X1	78	A3W8
30		80	A1V5MOD4
32	A1VOYV	82	A2V5MOD4
34		84	A3V5MOD4
36		86	
38		88	
40	A1P2VN	90	A1HOYVN
42		92	A1HOYN
44		94	
46	A1HOYV	96	
48		98	
50	A1HOY		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	A3V5MOD4
2	SIG RET	17	NU1
3	V1	18	NU2
4	V3	19	NU3
5		20	
6		21	
7		22	
8	SIG RET	23	A2V5MOD4
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	A1V5MOD4

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. *Dotted Line (if any) Indicates Internal ULD* Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A4A13B

Figure 10-27. Timing and Multiply-Divide Voters, Logic Diagram (Sheet 4)

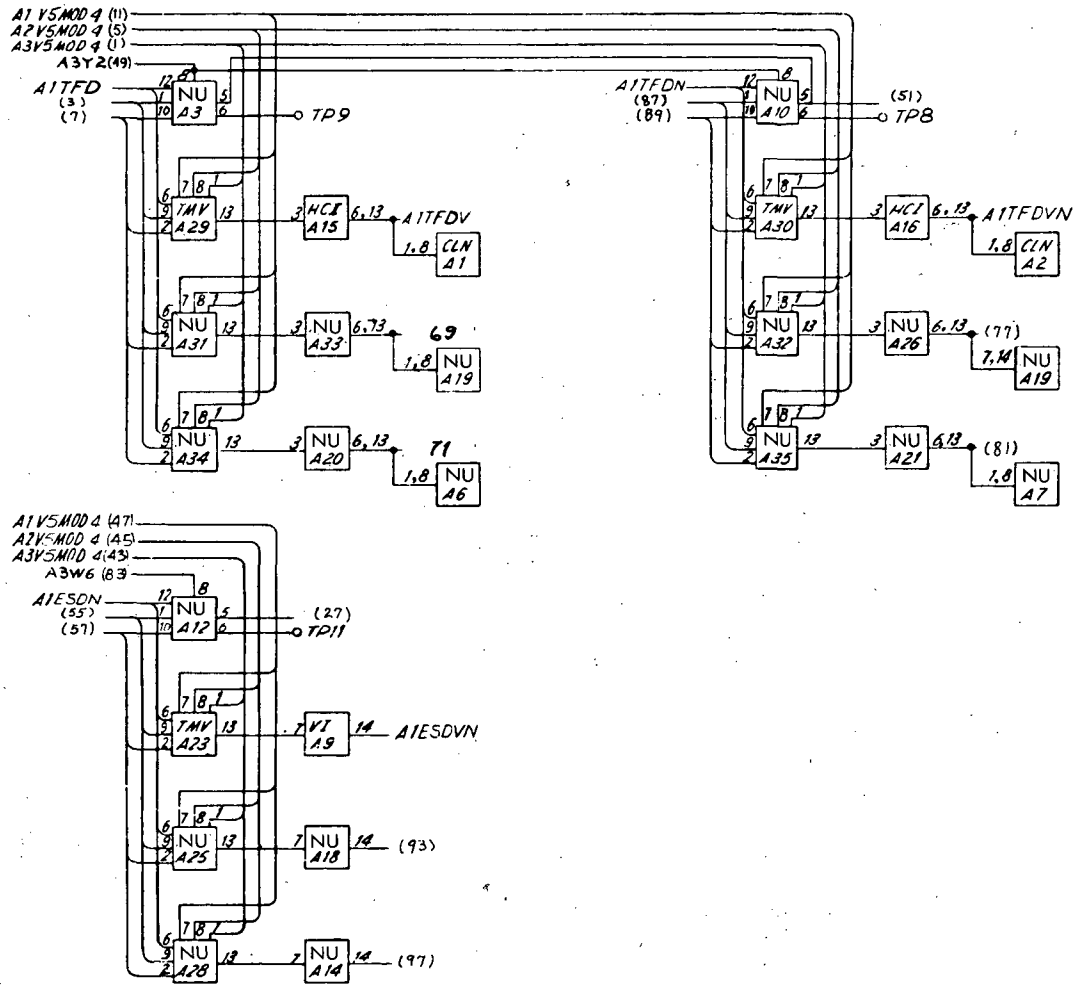
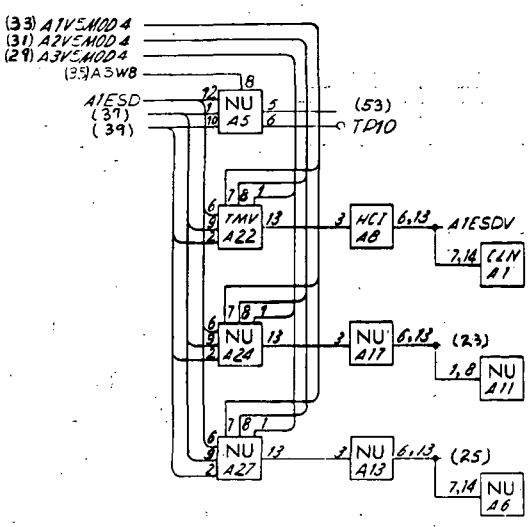


Figure 10-28. Multiply-Divide Voters, Logic Diagram (Sheet 1 of 4)

A4A14A



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	A3V5MOD4	51	
3		53	
5	A2V5MOD4	55	
7		57	
9	A1TFD	59	A1ESDN
11	A1V5MOD4	61	V3
13	V3	63	V1
15	V1	65	SIG RET
17	SIG RET	67	A1TFDV
19		69	
21	A1ESDV	71	
23		73	V3
25		75	V1
27		77	
29	A3V5MOD4	79	A1TFDVN
31	A2V5MOD4	81	
33	A1V5MOD4	83	A3W6
35	A3W8	85	SIG RET
37		87	
39		89	
41	A1ESD	91	A1TFDN
43	A3V5MOD4	93	
45	A2V5MOD4	95	A1ESDVN
47	A1V5MOD4	97	
49	A3Y2		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2	SIG RET	17	
3	V1	18	
4	V3	19	
5		20	
6		21	
7		22	
8	SIG RET	23	
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A4A14A

Figure 10-28. Multiply-Divide Voters, Logic Diagram (Sheet 2)

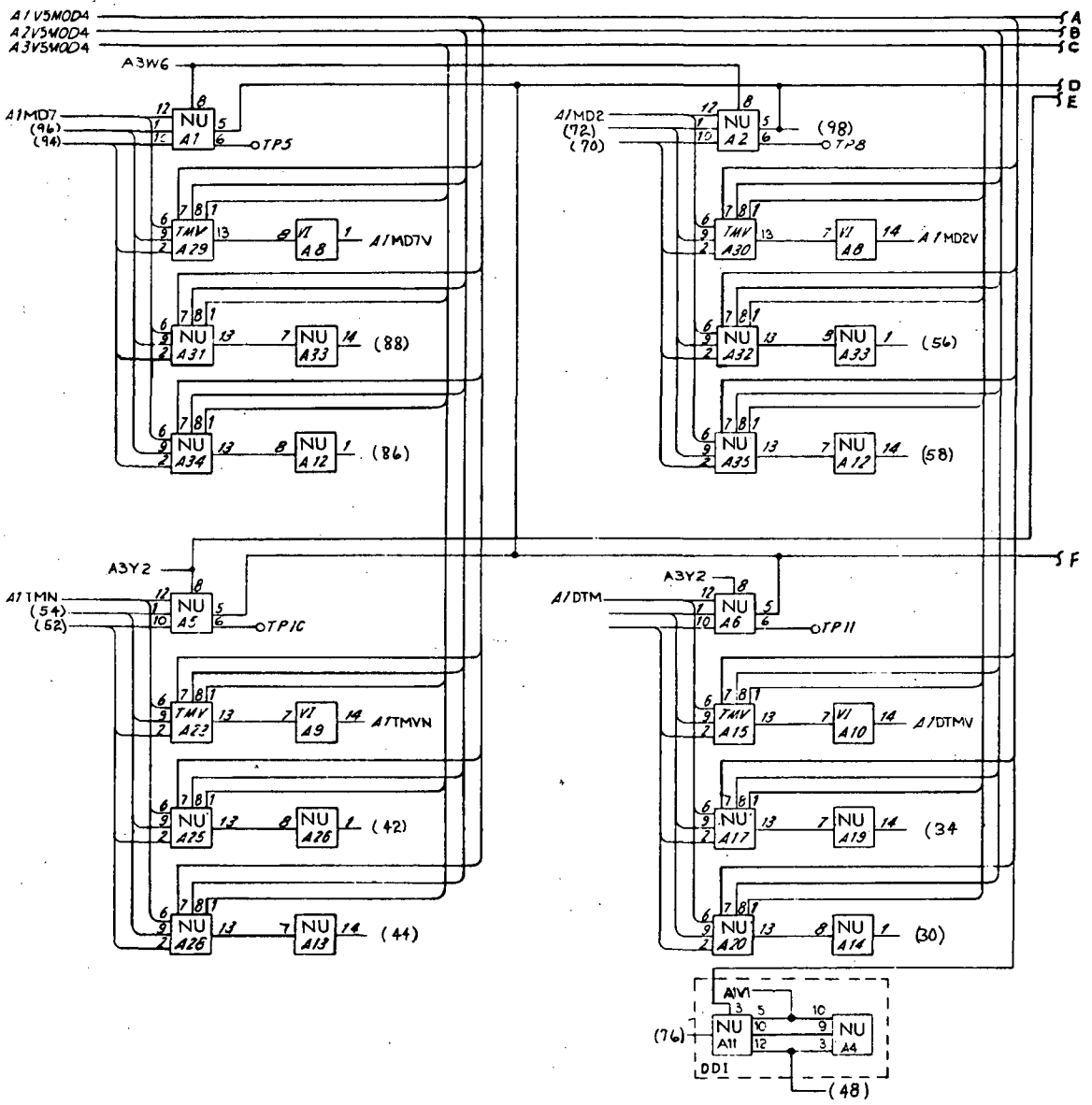
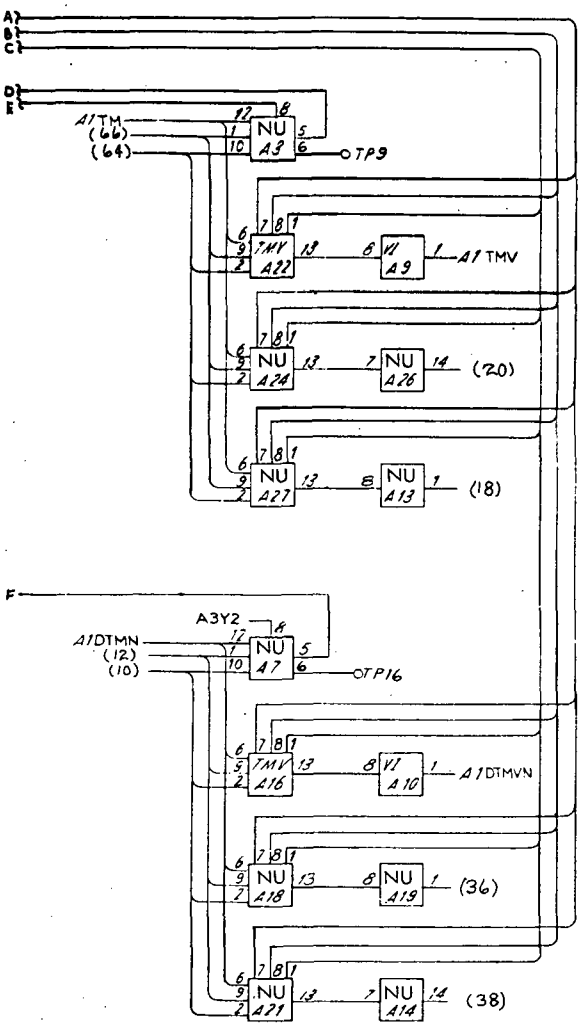


Figure 10-28. Multiply-Divide Voters, Logic Diagram (Sheet 3)



A4A14B

CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	NU1	52	
4	NU2	54	
6	NU3	56	
8	A1DTMN	58	
10		60	A1MD2V
12		62	A1TM
14	A3Y2	64	
16	A1TMV	66	
18		68	A1MD2
20		70	
22	A1DTM	72	
24		74	A3Y2
26		76	
28	A3Y2	78	A3W6
30		80	A1V5MOD4
32	A1DTMV	82	A2V5MOD4
34		84	A3V5MOD4
36		86	
38		88	
40	A1DTMVN	90	A1MD7V
42		92	A1MD7
44		94	
46	A1TMVN	96	
48		98	
50	A1TMN		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	A3V5MOD4
2	SIG RET	17	NU1
3	V1	18	NU2
4	V3	19	NU3
5		20	
6		21	
7		22	
8	SIG RET	23	A2V5MOD4
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	A1V5MOD4

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A4A14B

Figure 10-28. Multiply-Divide Voters, Logic Diagram (Sheet 4)

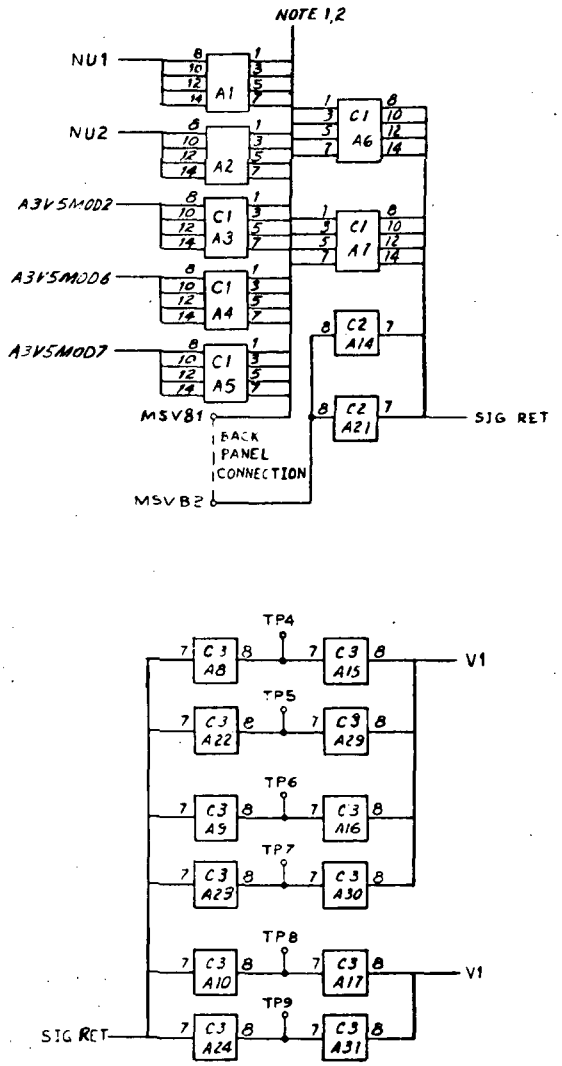
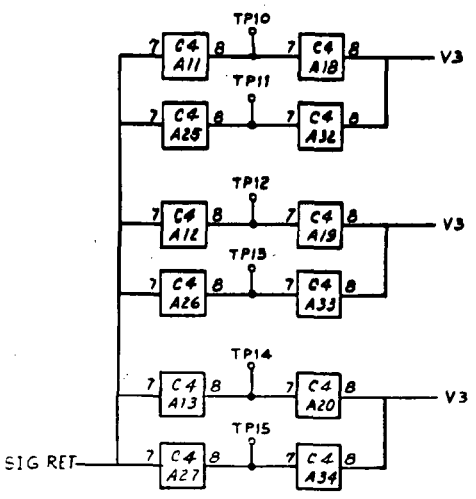


Figure 10-29. Decoupling Capacitors (Channel 5), Logic Diagram (Sheet 1 of 4)



A5A3A

CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	MSVB1	51	SIG RET
3	MSVB1	53	SIG RET
5	SIG RET	55	SIG RET
7	SIG RET	57	SIG RET
9	NU1	59	SIG RET
11	V3	61	SIG RET
13	V3	63	V3
15	V3	65	V3
17	V3	67	V3
19	NU2	69	V3
21	V1	71	SIG RET
23	V1	73	V3
25	V1	75	V3
27	V1	77	V3
29	A3V5MOD2	79	V3
31	V1	81	SIG RET
33	V1	83	SIG RET
35	V1	85	SIG RET
37	V1	87	SIG RET
39	A3V5MOD6	89	SIG RET
41	SIG RET	91	SIG RET
43	SIG RET	93	SIG RET
45	SIG RET	95	MSVB2
47	SIG RET	97	MSVB2
49	A3V5MOD7		

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A5A3A

Figure 10-29. Decoupling Capacitors (Channel 5), Logic Diagram (Sheet 2)

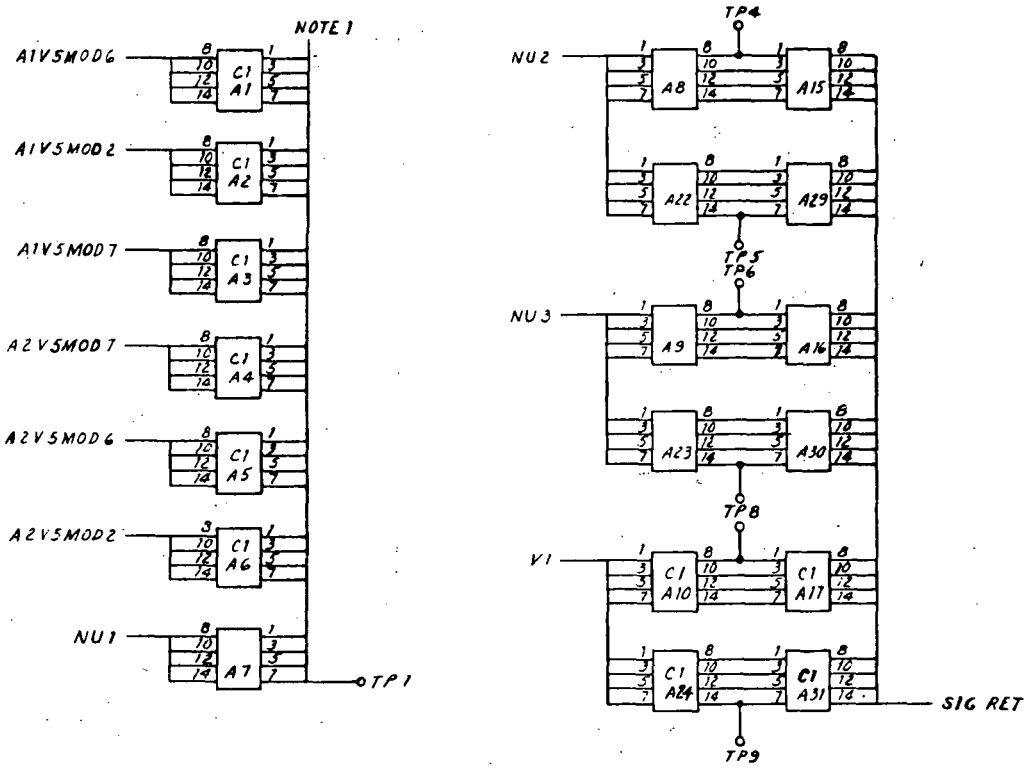
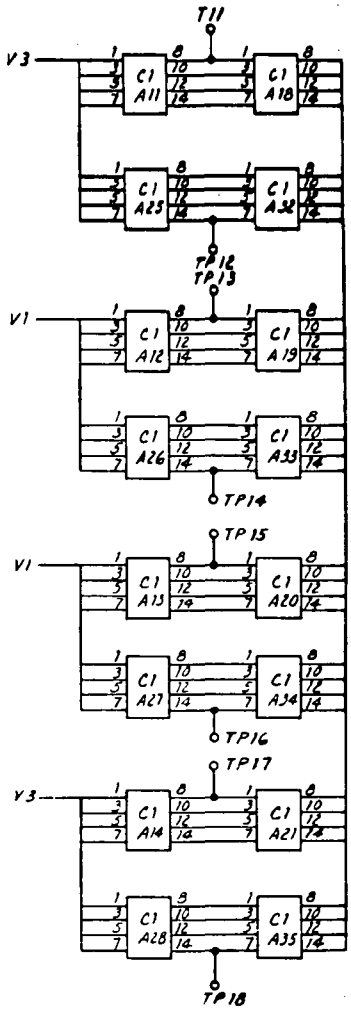


Figure 10-29. Decoupling Capacitors (Channel 5), Logic Diagram (Sheet 3)

A5A3B

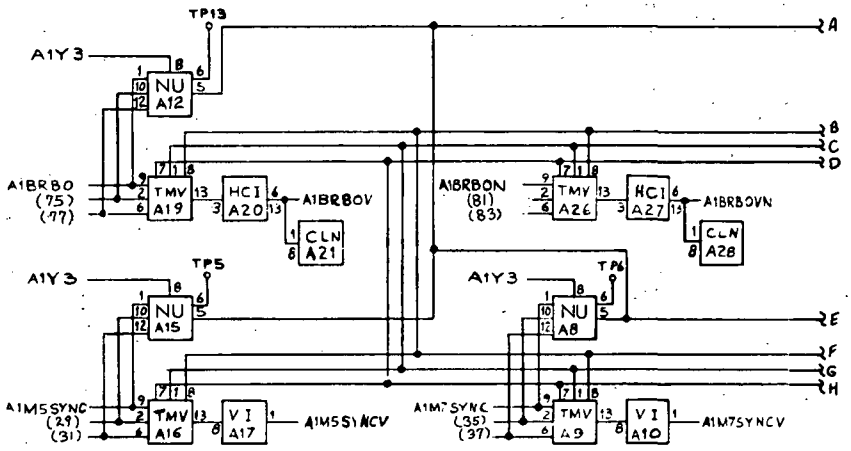


CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	V3	52	V3
4		54	
6		56	
8		58	A2V5MOD7
10	NU1	60	V1
12	V1	62	
14		64	
16		66	
18		68	SIG RET
20	SIG RET	70	
22		72	
24		74	
26		76	
28		78	A1V5MOD7
30	V1	80	NU3
32		82	
34		84	
36		86	
38	A2V5MOD2	88	A1V5MOD2
40	SIG RET	90	NU2
42		92	
44		94	
46		96	
48	A2V5MOD6	98	A1V5MOD6
50	V3		

NOTES.

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U. indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A5A3B

Figure 10-29. Decoupling Capacitors (Channel 5), Logic Diagram (Sheet 4)

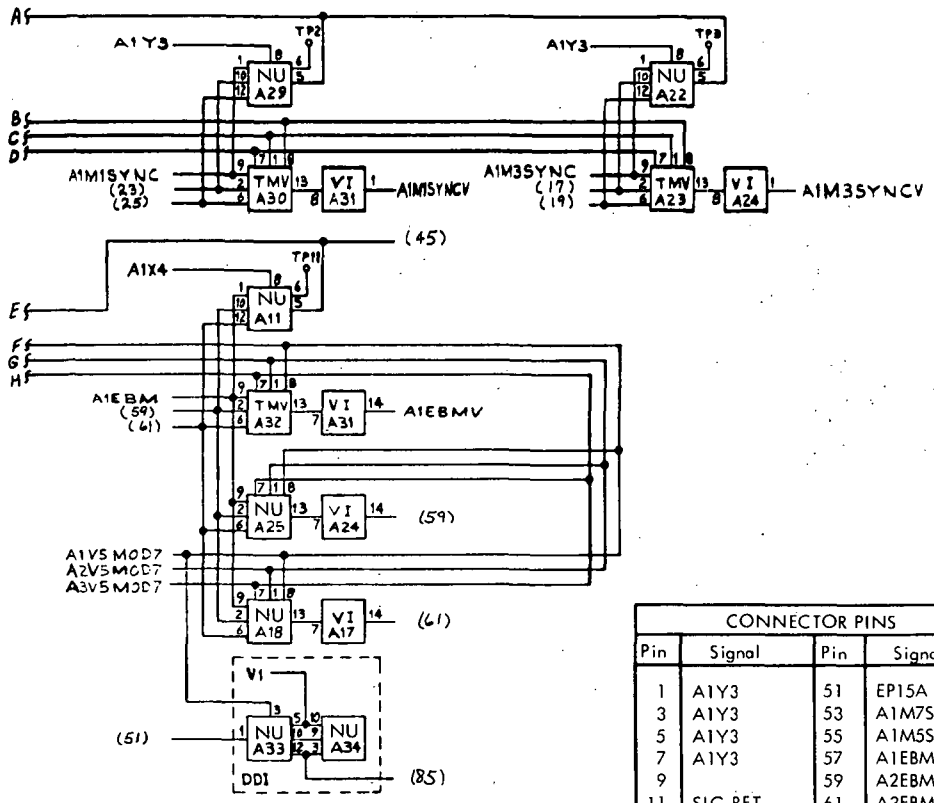


NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate it
5. Prefix Reference Designations as Follows: A5A5A

Figure 10-30. Memory Timing Voters, Logic Diagram (Sheet 1 of 8)

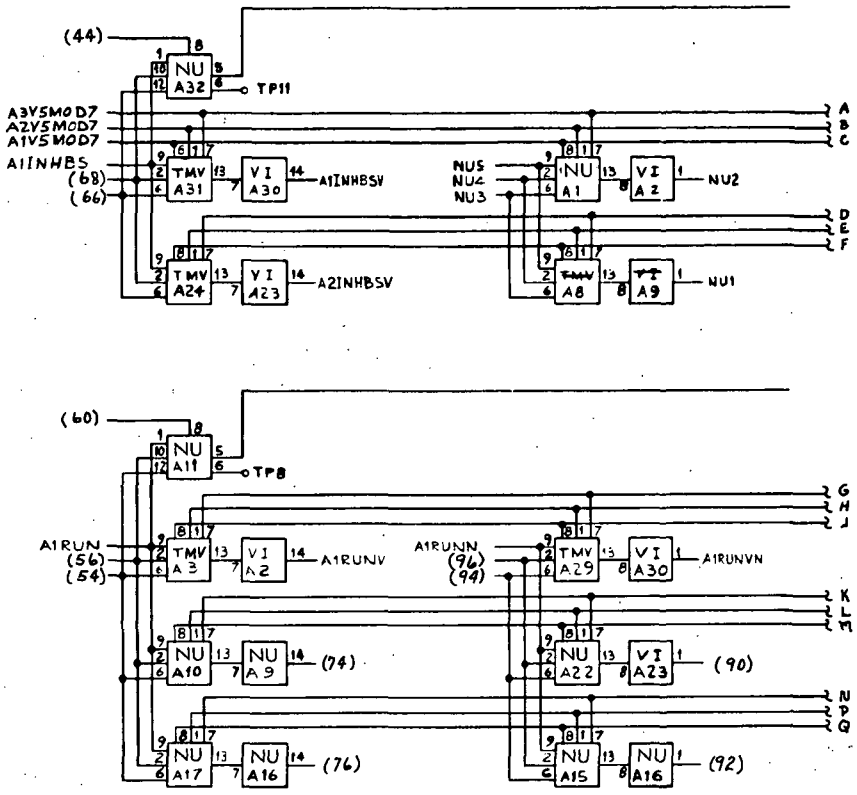
A5A5A



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	A1Y3	51	EP15A
3	A1Y3	53	A1M7SYNCV
5	A1Y3	55	A1M5SYNCV
7	A1Y3	57	A1EBM
9		59	A2EBM
11	SIG RET	61	A3EBM
13	SIG RET	63	A1M3SYNCV
15	A1M3SYNC	65	A1M1SYNCV
17	A2M3SYNC	67	A3V5MOD7
19	A3M3SYNC	69	A2V5MOD7
21	A1M1SYNC	71	A1V5MOD7
23	A2M1SYNC	73	A1BRB0
25	A3M1SYNC	75	A2BRB0
27	A1M5SYNC	77	A3BRB0
29	A2M5SYNC	79	A1BRB0N
31	A3M5SYNC	81	A2BRB0N
33	A1M7SYNC	83	A3BRB0N
35	A2M7SYNC	85	EP15
37	A3M7SYNC	87	V3
39	A1EBMV	89	V3
41	A2EBMV	91	A1X4
43	A3EBMV	93	A1Y3
45	EP16A	95	A1BRB0V
47	V1	97	A1BRB0VN
49	V1		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2	SIG RET	17	
3	V1	18	
4	V3	19	
5		20	
6		21	
7		22	
8	SIG RET	23	
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	

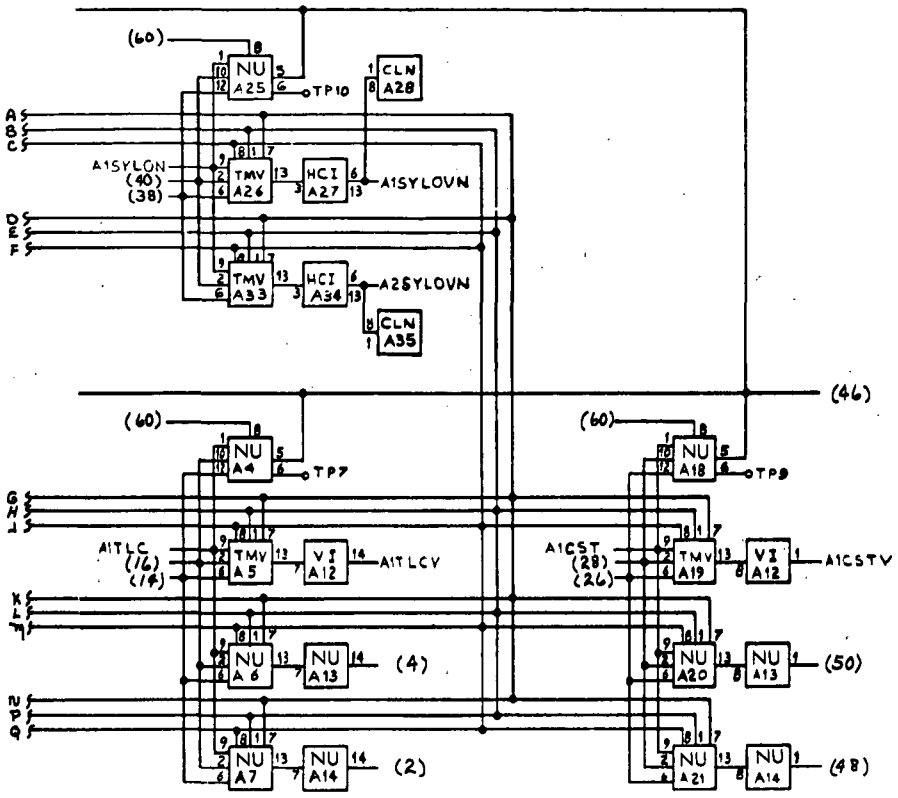
Figure 10-30. Memory Timing Voters, Logic Diagram (Sheet 2)



NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotten Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A5A5B

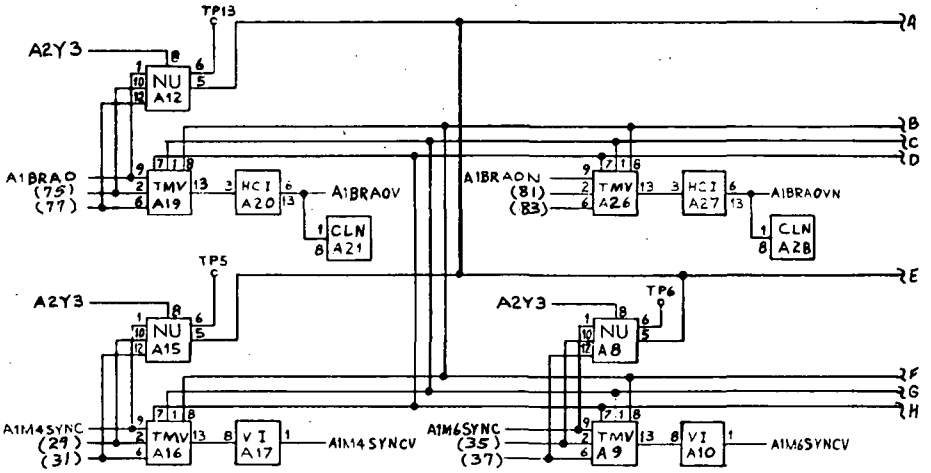
Figure 10-30. Memory Timing Voters, Logic Diagram (Sheet 3)



CONNECTOR PINS			
Pin	Signal	Pin	Signal
2		52	A1CSTV
4		54	
6	A1TLCV	56	
8		58	A1RUN
10	A1SYLOVN	60	A1X4
12	A2SYLOVN	62	A2INHBSV
14		64	A1INHBSV
16		66	
18	A1TLC	68	
20	A1X4	70	A1INHBS
22	A1X4	72	A1RUNV
24	A1X4	74	
26		76	
28		78	NU1
30	A1CST	80	NU2
32	A3V5MOD7	82	NU3
34	A2V5MOD7	84	NU4
36	A1V5MOD7	86	NU5
38		88	A1RUNVN
40		90	
42	A1SYLON	92	
44	A1Z5	94	
46		96	
48		98	A1RUNN
50			

THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2	SIG RET	17	
3	V1	18	
4	V3	19	
5		20	
6		21	
7		22	
8	SIG RET	23	
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	

Figure 10-30. Memory Timing Voters, Logic Diagram (Sheet 4)

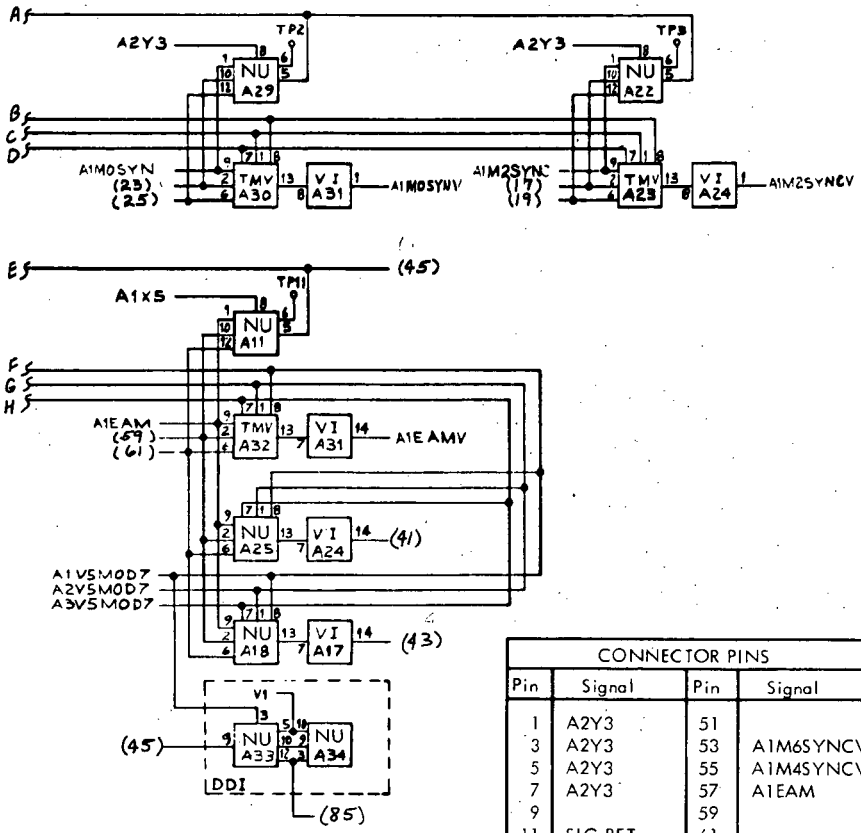


NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A5A6A

Figure 10-30. Memory Timing Voters, Logic Diagram (Sheet 5)

A5A6A



THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2	SIG RET	17	
3	V1	18	
4	V3	19	
5		20	
6		21	
7		22	
8	SIG RET	23	
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	

CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	A2Y3	51	
3	A2Y3	53	A1M6SYNCV
5	A2Y3	55	A1M4SYNCV
7	A2Y3	57	A1EAM
9		59	
11	SIG RET	61	
13	SIG RET	63	A1M2SYNCV
15	A1M2SYNC	65	A1MOSYNV
17		67	A3V5MOD7
19		69	A2V5MOD7
21	A1MOSYN	71	A1V5MOD7
23		73	A1BRAO
25		75	
27	A1M4SYNC	77	
29		79	A1BRAON
31		81	
33	A1M6SYNC	83	
35		85	
37		87	V3
39	A1EAMV	89	V3
41		91	A1X5
43		93	A2Y3
45		95	A1BRAOV
47	V1	97	A1BRAOVN
49	V1		

Figure 10-30. Memory Timing Voters, Logic Diagram (Sheet 6)

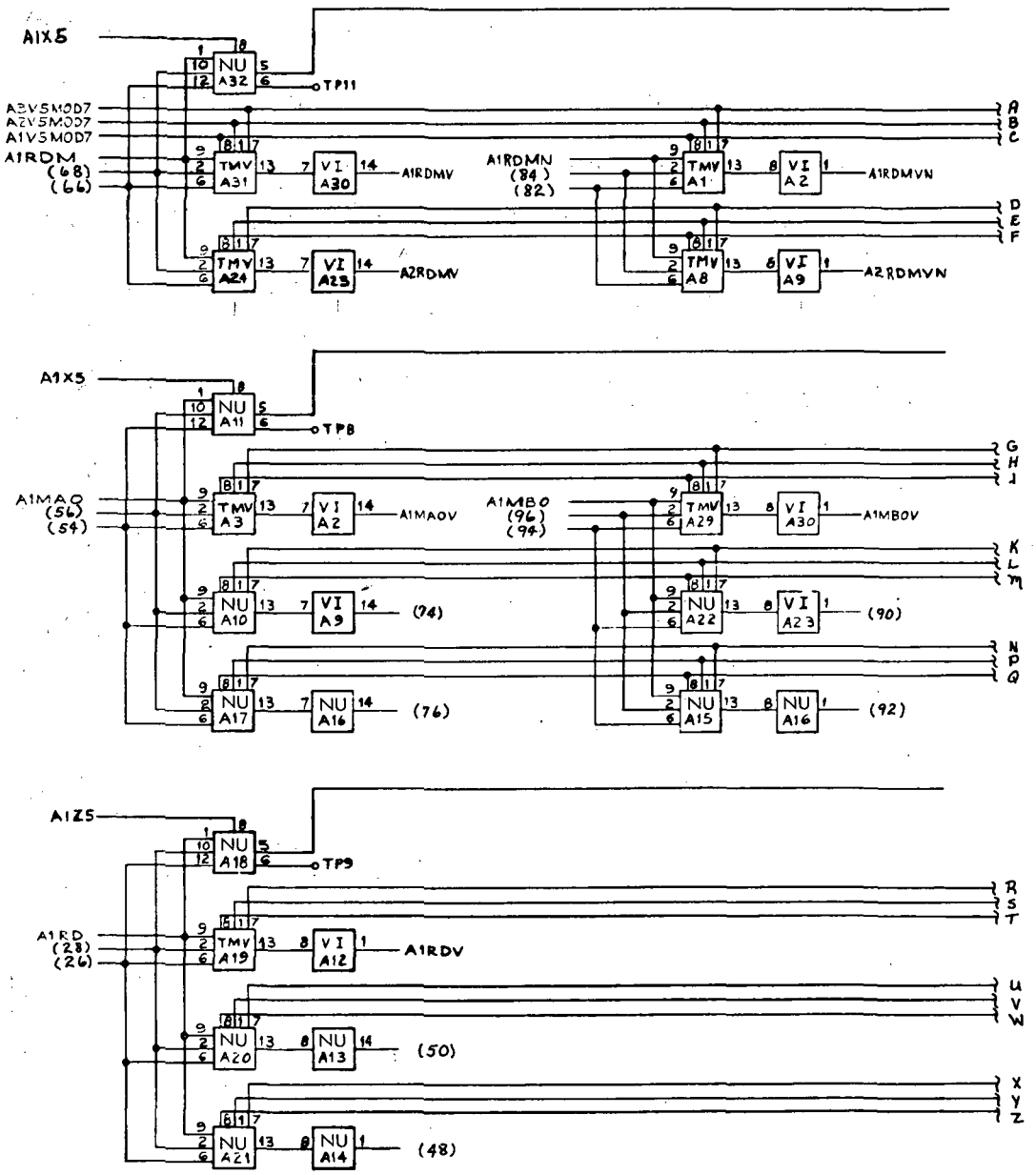
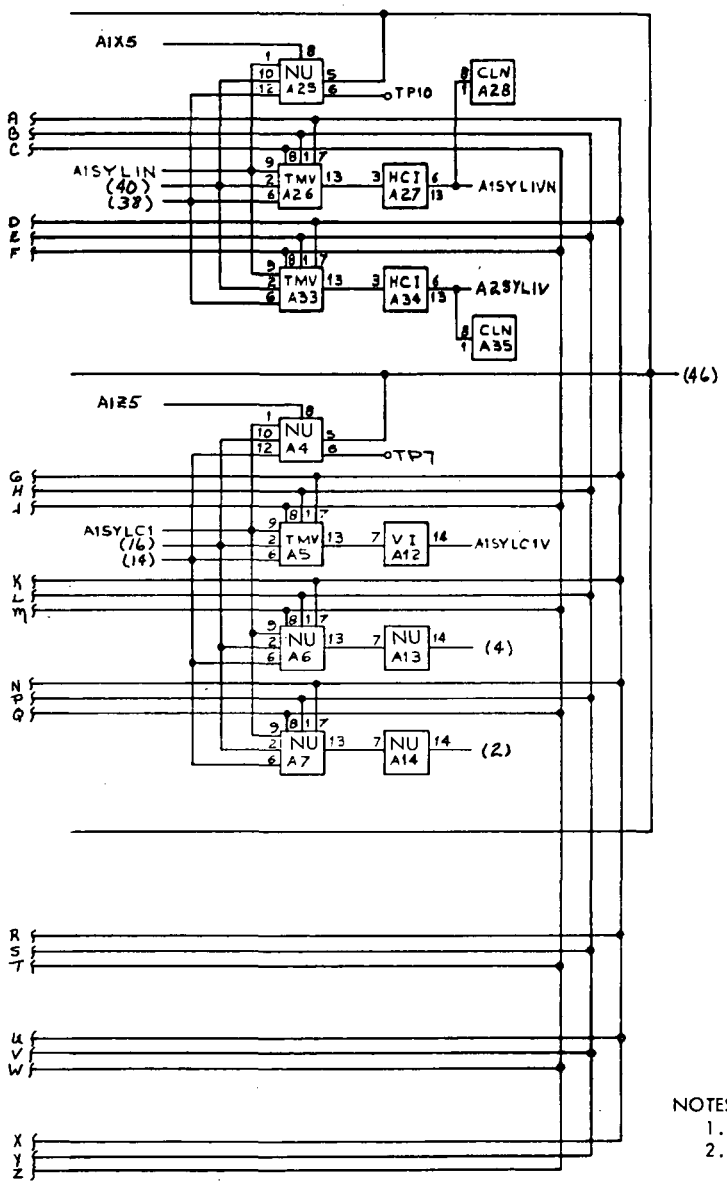


Figure 10-30. Memory Timing Voters, Logic Diagram (Sheet 7)

A5A6B



CONNECTOR PINS			
Pin	Signal	Pin	Signal
2		52	A1RDV
4		54	
6	A1SYLC1V	56	
8		58	A1MAO
10	A1SYLIVN	60	A1Z5
12		62	A2RDMV
14		64	A1RDMV
16		66	
18	A1SYLC1	68	
20	A1X5	70	A1RDM
22	A1Z5	72	A1MAOV
24	A1X5	74	
26		76	
28		78	A2RDMVN
30	A1RD	80	A1RDMVN
32	A3V5MOD7	82	
34	A2V5MOD7	84	
36	A1V5MOD7	86	A1RDMN
38		88	A1MBOV
40		90	
42	A1SYLIN	92	
44	A1X5	94	
46		96	
48		98	A1MBO
50			

THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2	SIG RET	17	
3	V1	18	
4	V3	19	
5		20	
6		21	
7		22	
8	SIG RET	23	
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A5A6B

Figure 10-30. Memory Timing Voters, Logic Diagram (Sheet 8)

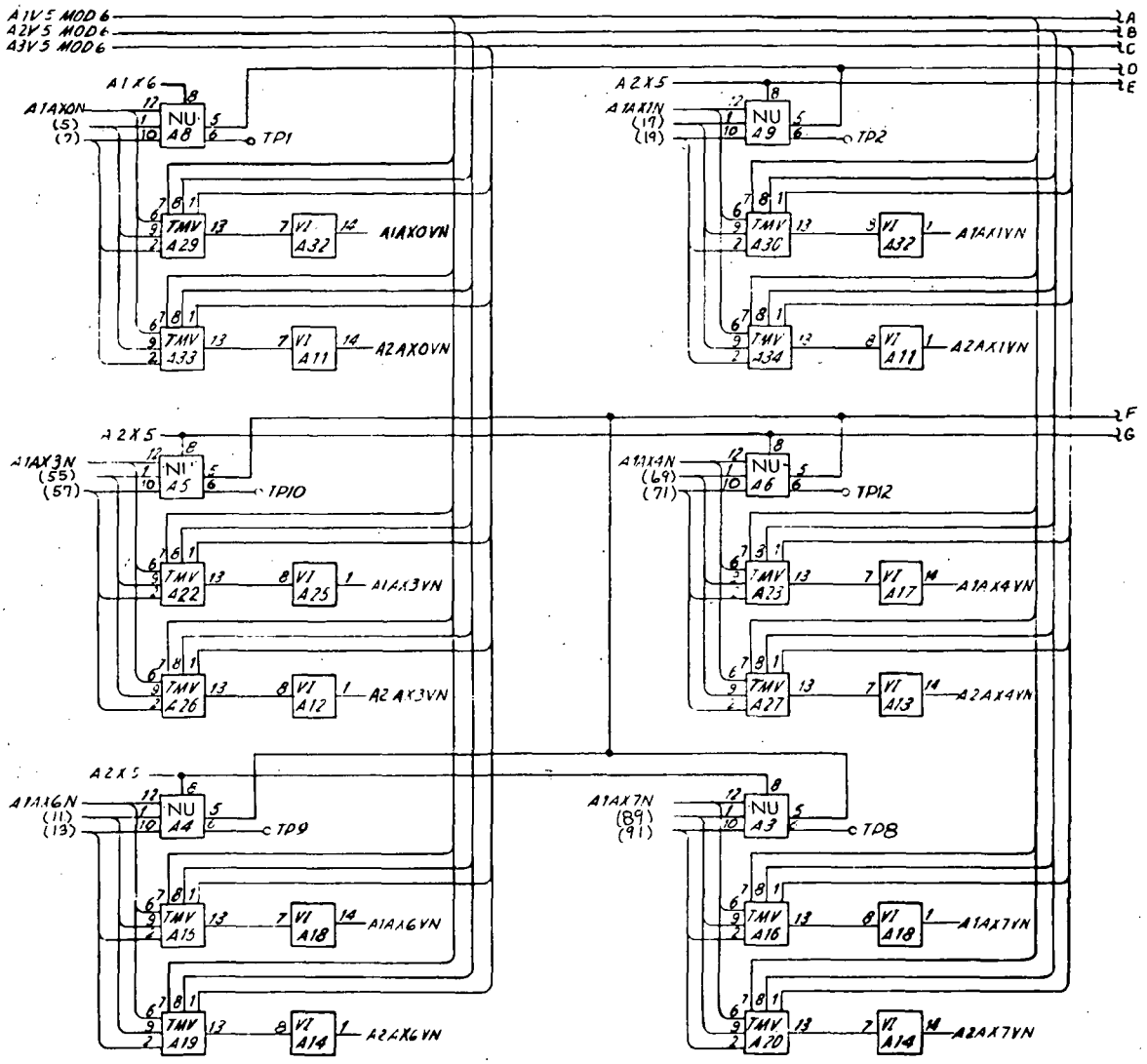
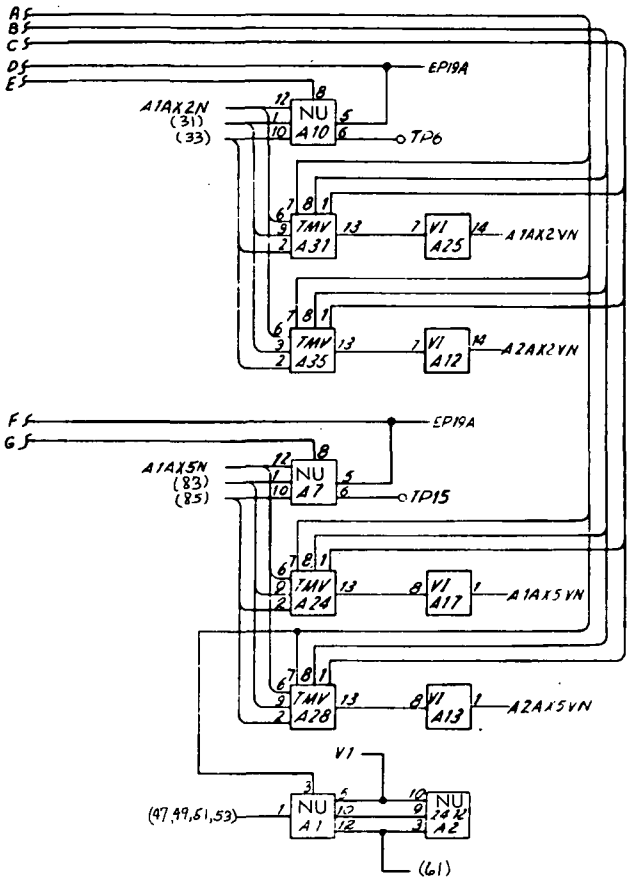


Figure 10-31. Memory Address Decoder Voters, Logic Diagram (Sheet 1 of 8)

A5A7A



NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A5A7A

CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	A1AX3VN	51	
3	A2AX3VN	53	
5		55	
7		57	
9	A1AX0N	59	A1AX3N
11		61	
13		63	A2AX1VN
15	A1AX6N	65	A1AX1VN
17		67	A1AX4N
19		69	
21	A1AX1N	71	
23	A2AX4VN	73	A2X5
25	A1AX4VN	75	A2X5
27	A1AX2VN	77	A1X6
29	A2AX2VN	79	A1AX5VN
31		81	A2AX5VN
33		83	
35	A1AX2N	85	
37	A2AX7VN	87	A1AX5N
39	A1AX7VN	89	
41	A2X5	91	
43	A1AX0VN	93	A1AX7N
45	A2AX0VN	95	A2AX6VN
47		97	A1AX6VN
49			

THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2	SIG RET	17	A1X6
3	V3	18	
4	V1	19	(47,49,51, 53)
5			
6		20	
7		21	
8		22	
9		23	
10		24	A2V5MOD6
11		25	A3V5MOD6
12	SIG RET	26	A1V5MOD6
13	V3	27	
14	V1	28	
15		29	
		30	

Figure 10-31. Memory Address Decoder Voters, Logic Diagram (Sheet 2)

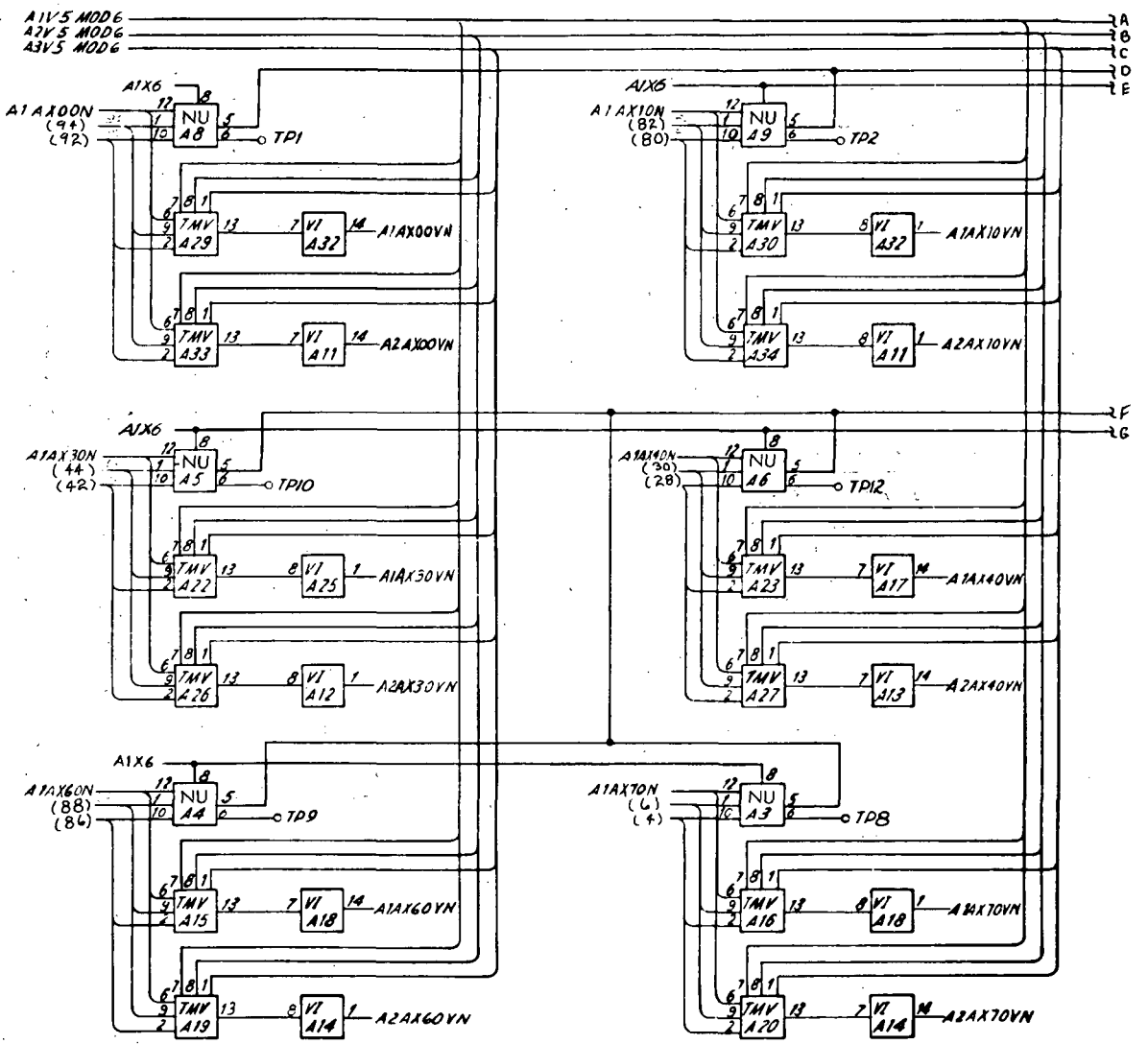
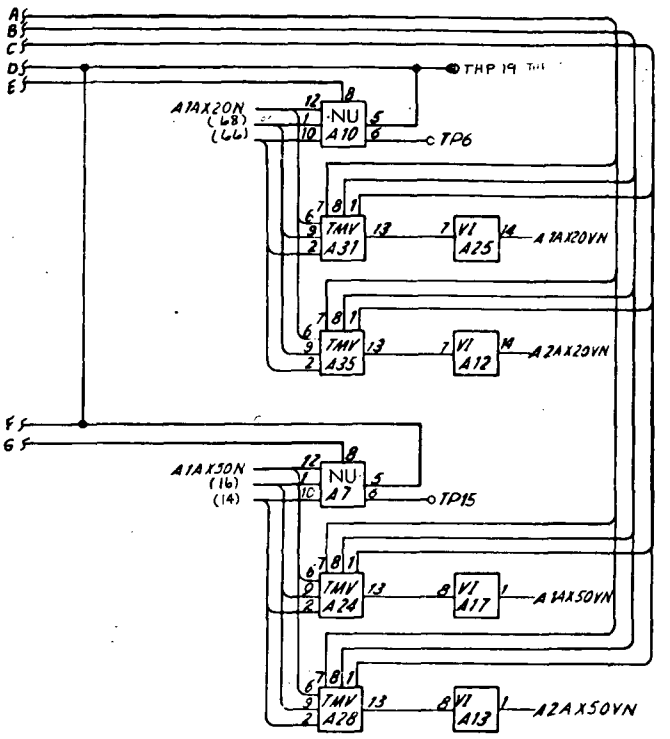


Figure 10-31. Memory Address Decoder Voters, Logic Diagram (Sheet 3)

A5A7B



CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	A1AX70N	52	A1AX00VN
4		54	A2AX00VN
6		56	SIG RET
8	A2AX60VN	58	V3
10	A1AX60VN	60	A1AX70VN
12	A1AX50N	62	A2AX70VN
14		64	A1AX20N
16		66	
18	SIG RET	68	
20	A2AX40VN	70	A2AX50VN
22	A1AX40VN	72	A1AX50VN
24	V3	74	V1
26	A1AX40N	76	A1V5MOD6
28		78	A1AX10N
30		80	
32	A2AX20VN	82	
34	A1AX20VN	84	A1AX60N
36	A2AX10VN	86	
38	A1AX10VN	88	
40	A1AX30N	90	A1AX00N
42		92	
44		94	
46	V1	96	A2V5MOD6
48	A2AX30VN	98	A3V5MOD6
50	A1AX30VN		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2	SIG RET	17	A1X6
3	V3	18	
4	V1	19	
5		20	
6		21	
7		22	
8		23	
9		24	A2V5MOD6
10		25	A3V5MOD6
11		26	A1V5MOD6
12	SIG RET	27	
13	V3	28	
14	V1	29	
15		30	

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A5A7B

Figure 10-31. Memory Address Decoder Voters, Logic Diagram (Sheet 4)

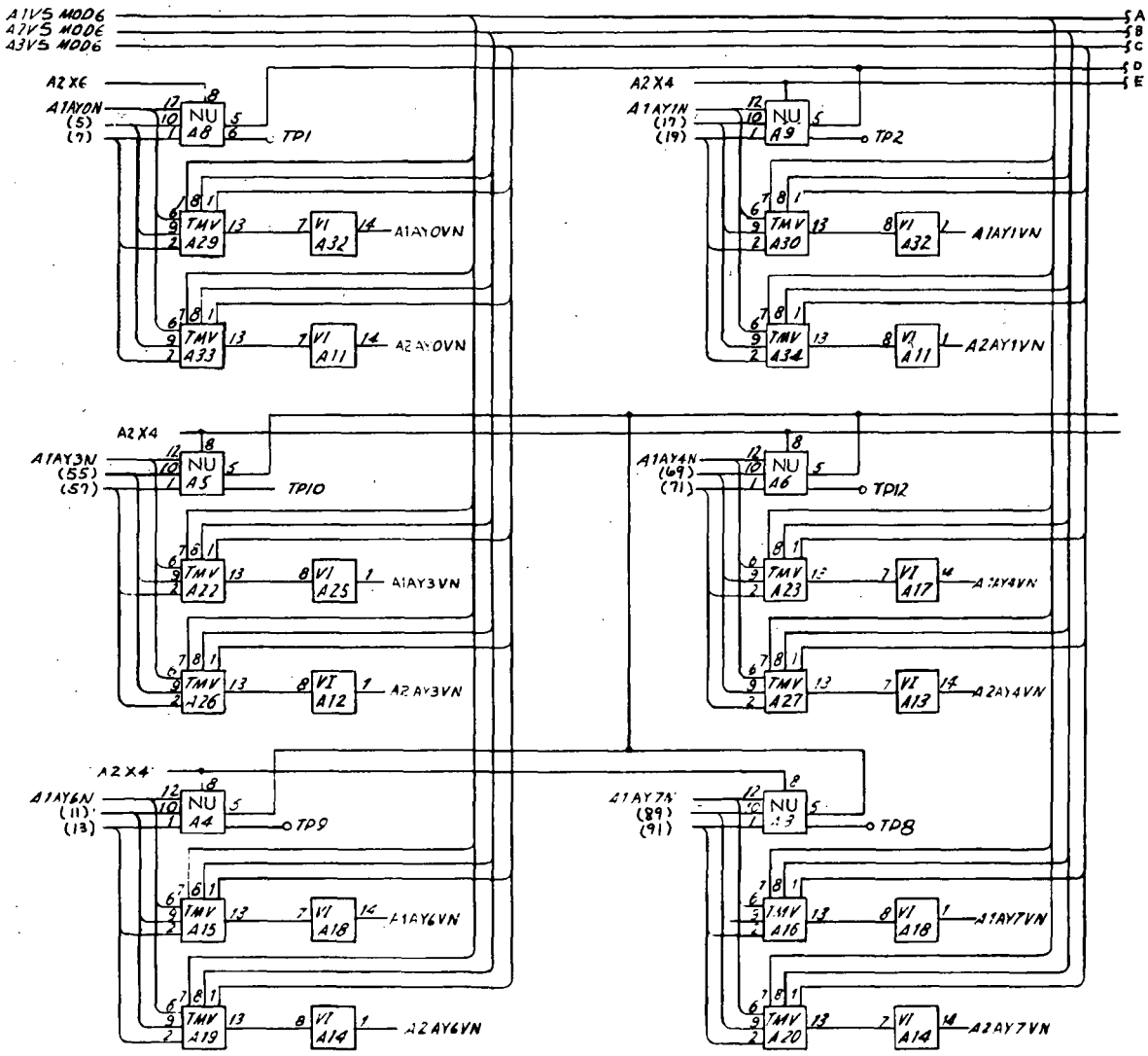
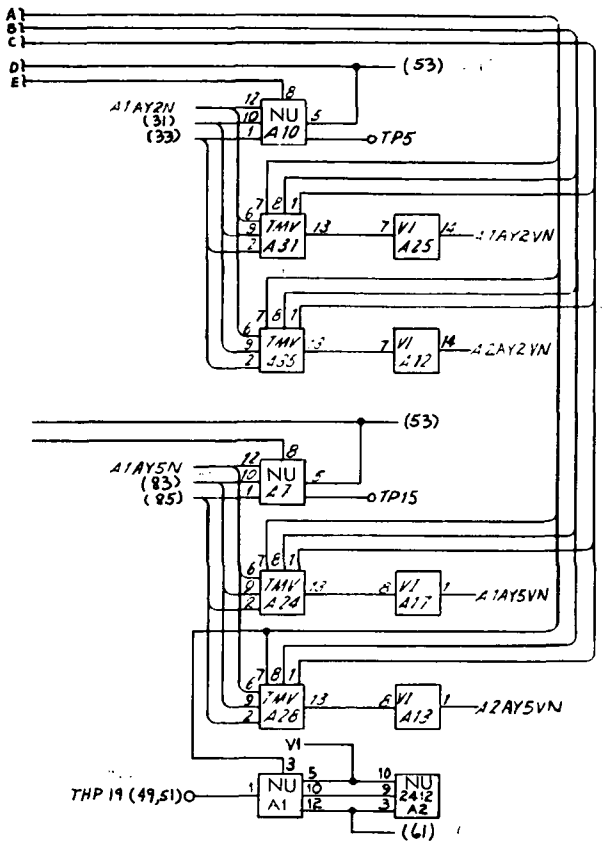


Figure 10-31. Memory Address Decoder Voters, Logic Diagram (Sheet 5)

A5A8A



NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A5A8A

CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	A1AY3VN	51	
3	A2AY3VN	53	
5		55	
7		57	
9	A1AY0N	59	A1AY3N
11		61	
13		63	A2AY1VN
15	A1AY6N	65	A1AY1VN
17		67	A1AY4N
19		69	
21	A1AY1N	71	
23	A2AY4VN	73	A2X4
25	A1AY4VN	75	A2X4
27	A1AY2VN	77	A2X6
29	A2AY2VN	79	A1AY5VN
31		81	A2AY5VN
33		83	
35	A1AY2N	85	
37	A2AY7VN	87	A1AY5N
39	A1AY7VN	89	
41	A2X4	91	
43	A1AY0VN	93	A1AY7N
45	A2AY0VN	95	A2AY6VN
47		97	A1AY6VN
49			

THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2	SIG RET	17	A2X6
3	V3	18	
4	V1	19	
5		20	
6		21	
7		22	
8		23	
9		24	A2V5M0D6
10		25	A3V5M0D6
11		26	A1V5M0D6
12	SIG RET	27	
13	V3	28	
14	V1	29	
15		30	

Figure 10-31. Memory Address Decoder Voters, Logic Diagram (Sheet 6)

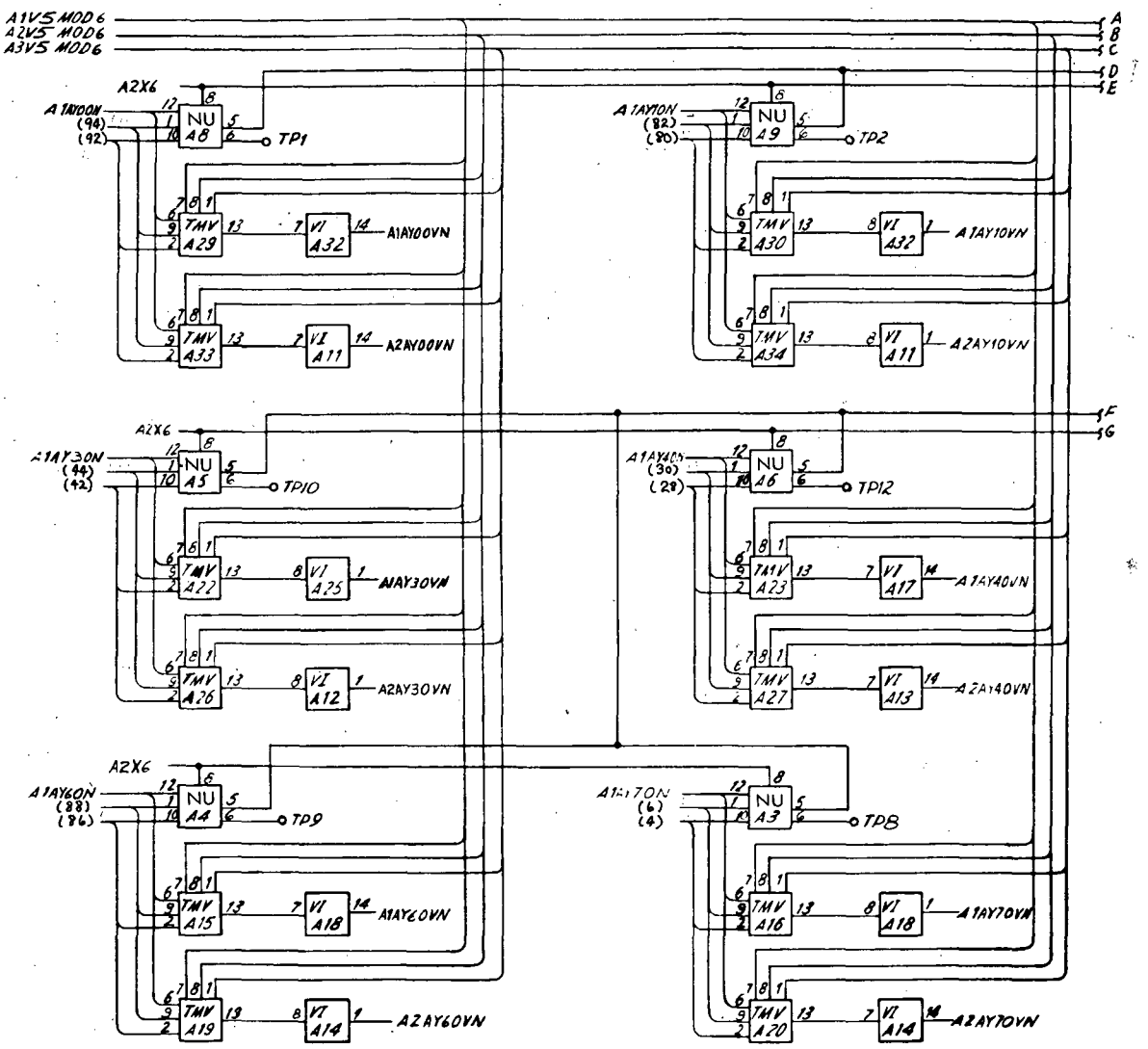
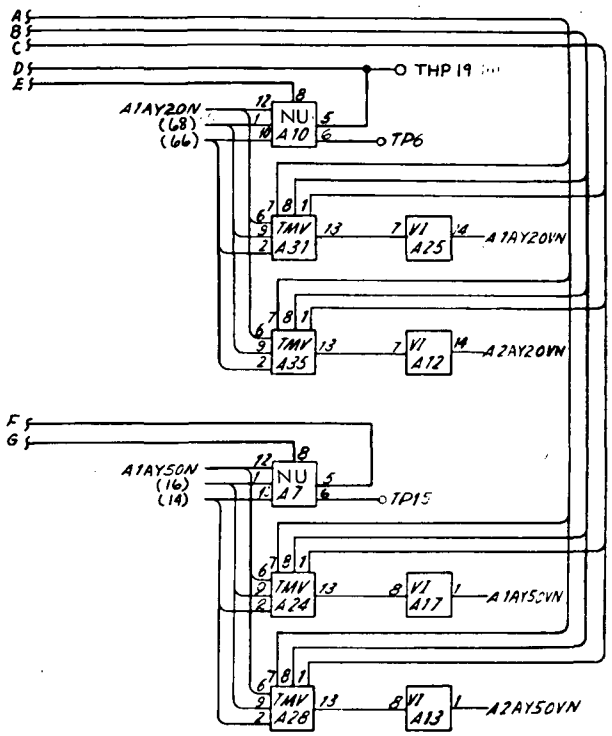


Figure 10-31. Memory Address Decoder Voters, Logic Diagram (Sheet 7)

A5A8B



CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	A1AY70N	52	A1AY00VN
4		54	A2AY00VN
6		56	SIG RET
8	A2AY60VN	58	V3
10	A1AY60VN	60	A1AY70VN
12	A1AY50N	62	A2AY70VN
14		64	A1AY20N
16		66	
18	SIG RET	68	
20	A2AY40VN	70	A2AY50VN
22	A1AY40VN	72	A1AY50VN
24	V3	74	V1
26	A1AY40N	76	A1V5M0D6
28		78	A1AY10N
30		80	
32	A2AY20VN	82	
34	A1AY20VN	84	A1AY60N
36	A2AY10VN	86	
38	A1AY10VN	88	
40	A1AY30N	90	A1AY00N
42		92	
44		94	
46	V1	96	A2V5M0D6
48	A2AY30VN	98	A3V5M0D6
50	A1AY30VN		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2	SIG RET	17	A2X6
3	V3	18	
4	V1	19	
5		20	
6		21	
7		22	
8		23	
9		24	A2V5M0D6
10		25	A3V5M0D6
11		26	A1V5M0D6
12	SIG RET	27	
13	V3	28	
14	V1	29	
15		30	

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U. Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A5A8B

Figure 10-31. Memory Address Decoder Voters, Logic Diagram (Sheet 8)

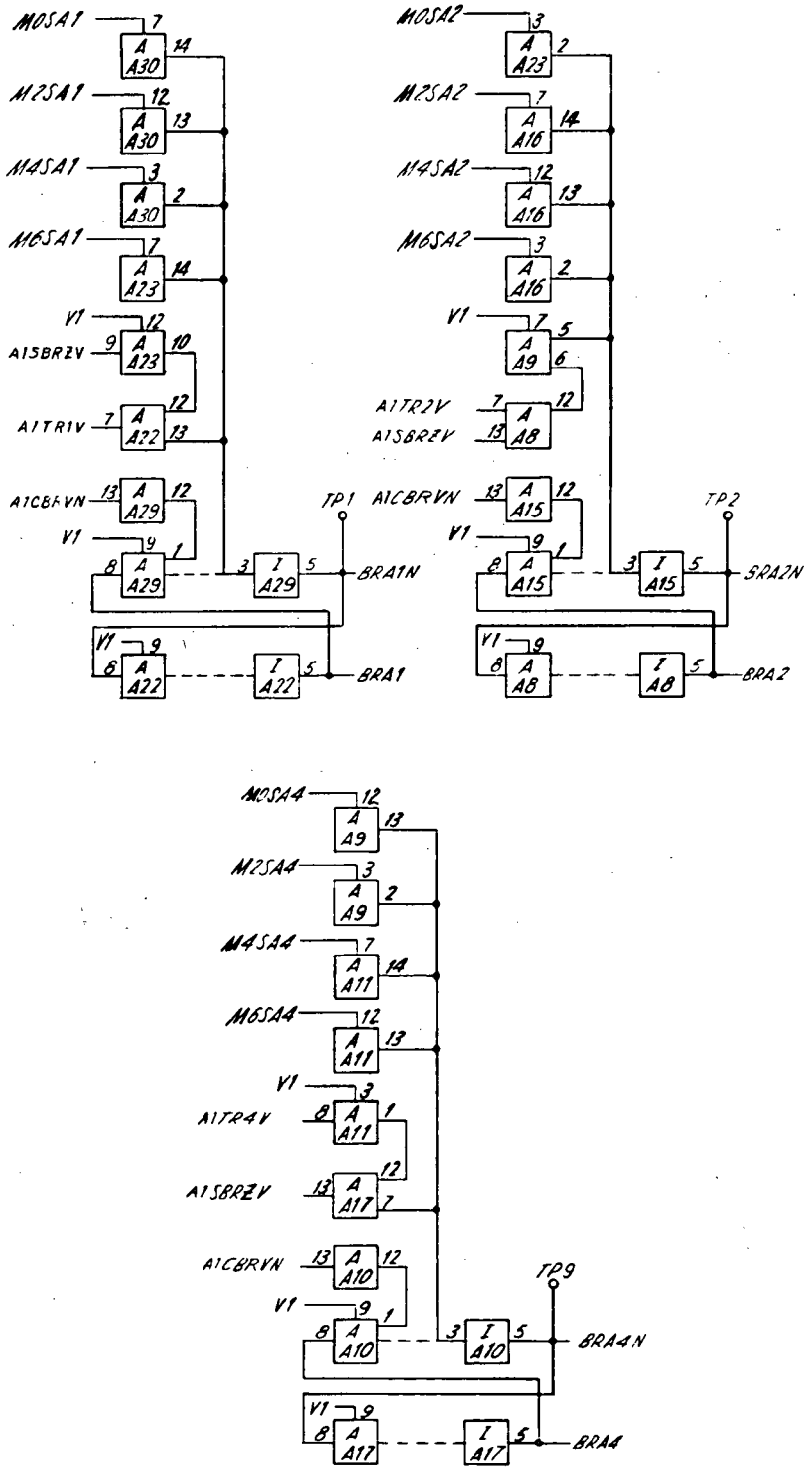
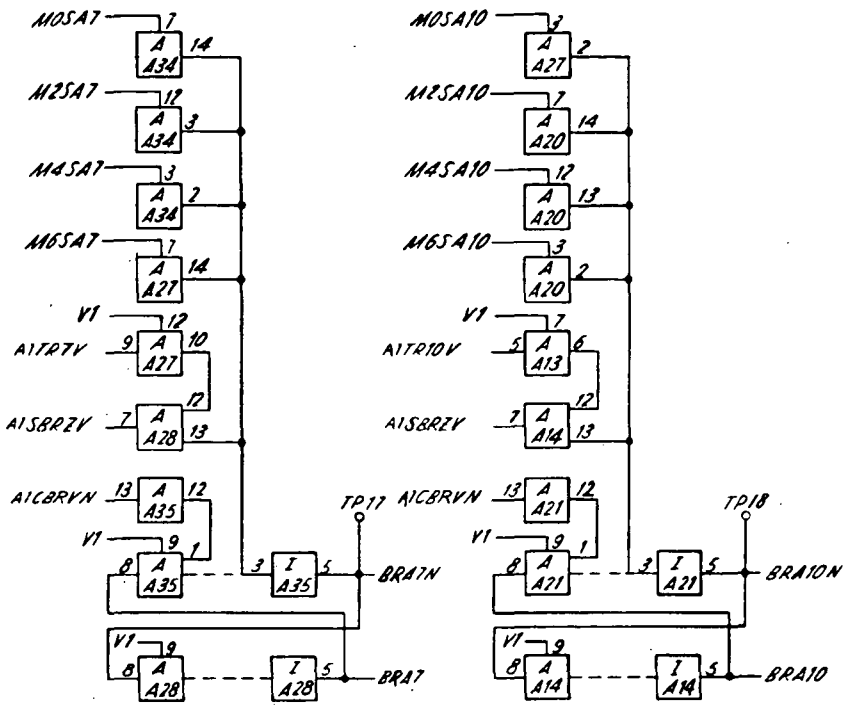


Figure 10-32. Memory Buffer Registers, Logic Diagram (Sheet 1 of 12)



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	BRA2N	51	
3	BRA2	53	A1TR4V
5	BRA1N	55	M6SA4
7	BRA1	57	M4SA4
9	M2SA4	59	
11	M6SA2	61	
13	A1CERVN	63	M0SA10
15	A1TR1V	65	A1TR7V
17	M4SA1	67	
19	M0SA4	69	M4SA7
21	A1SBRZV	71	M6SA10
23	M4SA2	73	
25	M2SA2	75	M4SA10
27	M2SA1	77	M2SA7
29	M0SA10	79	M2SA10
31	M6SA1	81	M0SA7
33	M0SA2	83	M6SA7
35	BRA4N	85	BRA7
37	A1TR2V	87	A1TR10V
39	SIG RET	89	BRA10
41	V1	91	
43	BRA4	93	BRA7N
45	V3	95	BRA10N
47		97	
49			

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A5A9A

Figure 10-32. Memory Buffer Registers, Logic Diagram (Sheet 2)

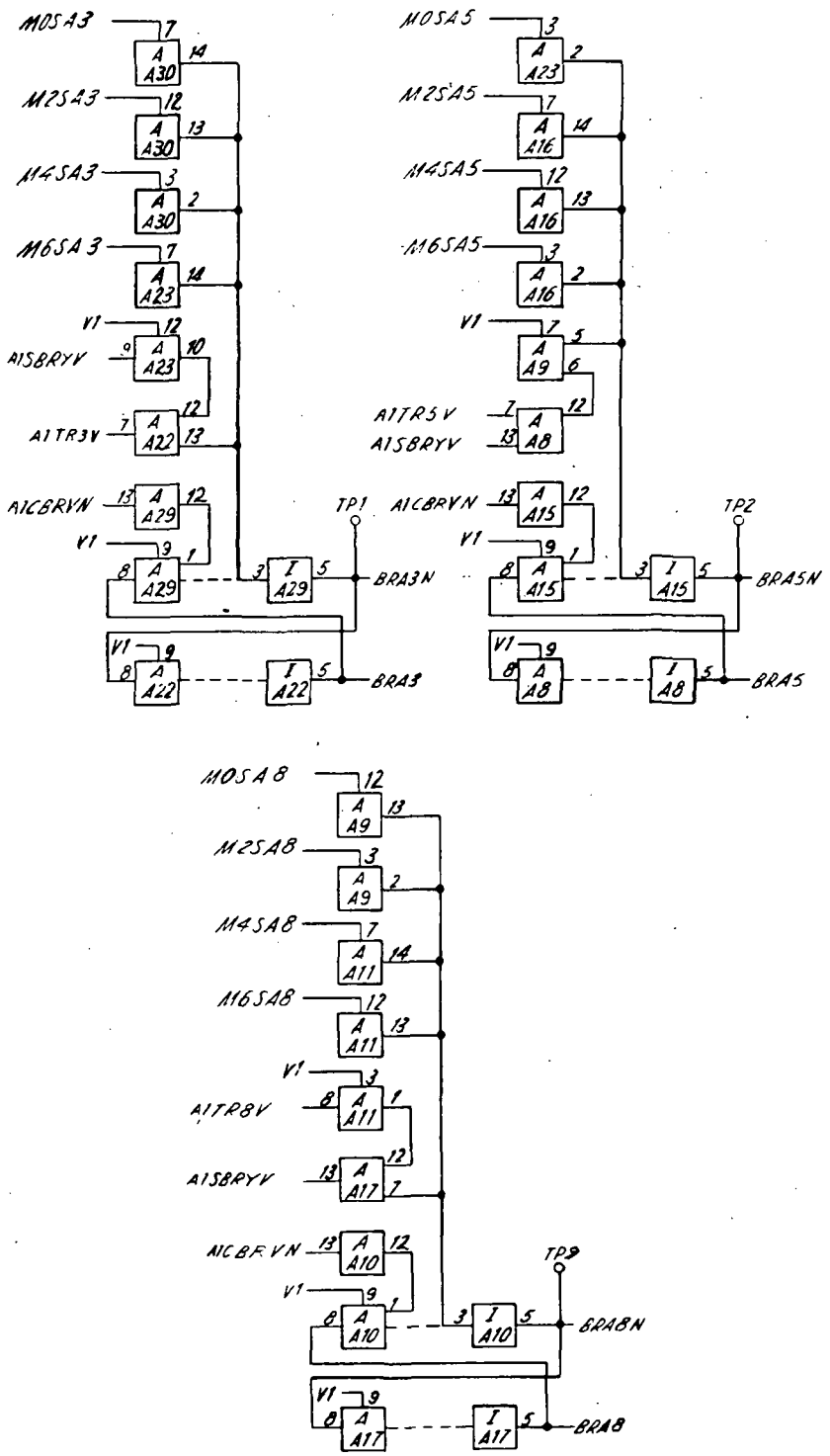
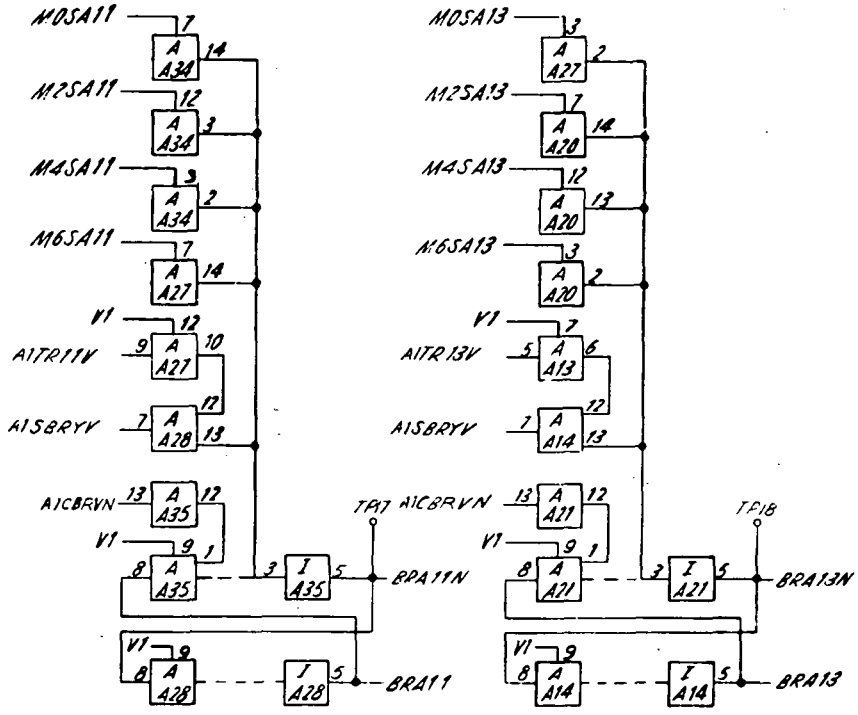


Figure 10-32. Memory Buffer Registers, Logic Diagram (Sheet 3)

A5A9B



CONNECTOR PINS			
Pin	Signal	Pin	Signal
2		52	
4	BRA13N	54	V3
6	BRA11N	56	BRA8
8		58	V1
10	BRA13	60	SIG RET
12	A1TR13V	62	A1TR5V
14	BRA11	64	BRA8N
16	M6SA11	66	M0SA5
18	M0SA11	68	M6SA3
20	M2SA13	70	M0SA3
22	M2SA11	72	M2SA3
24	M4SA13	74	M2SA5
26		76	M4SA5
28	M6SA13	78	A1SBRYV
30	M4SA11	80	M0SA8
32		82	M4SA3
34	A1TR11V	84	A1TR3V
36	M0SA13	86	A1CBRVN
38		88	M6SA5
40		90	M2SA8
42	M4SA8	92	BRA3
44	M6SA8	94	BRA3N
46	A1TR8V	96	BRA5
48		98	BRA5N
50			

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate it
5. Prefix Reference Designations as Follows: A5A9B

Figure 10-32. Memory Buffer Registers, Logic Diagram (Sheet 4)

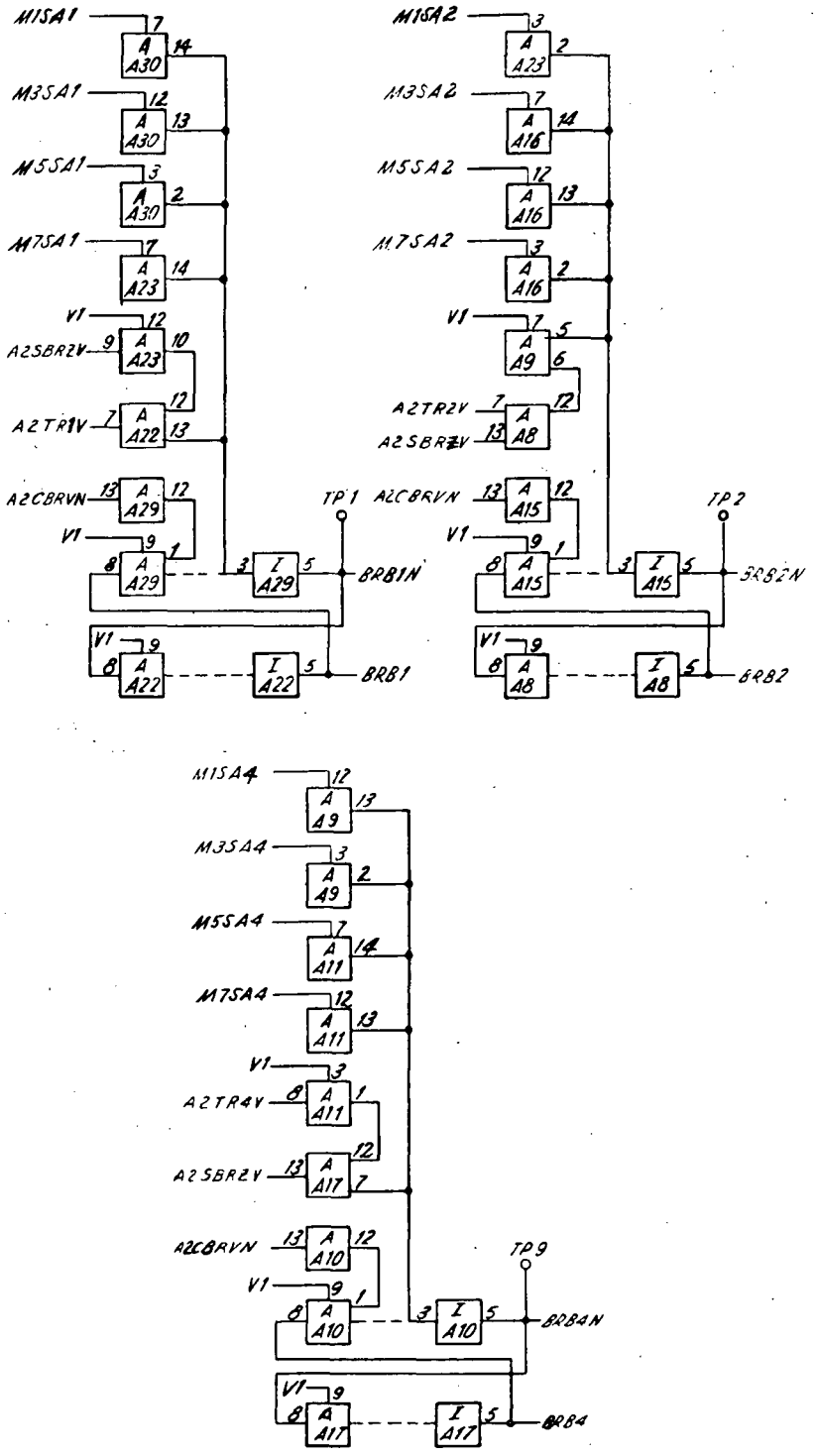
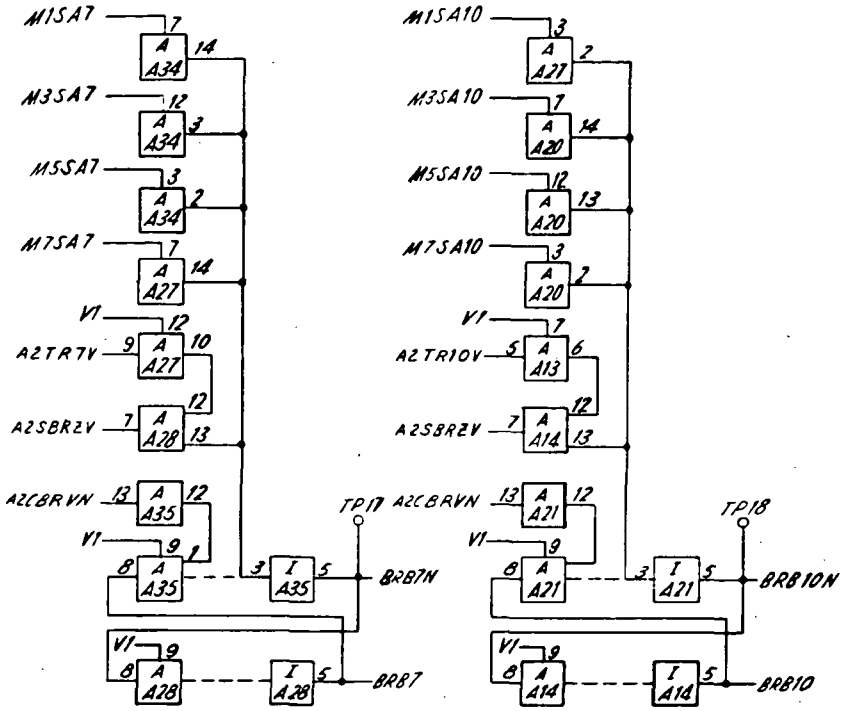


Figure 10-32. Memory Buffer Registers, Logic Diagram (Sheet 5)

A5A10A



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	BRB2N	51	
3	BRB2	53	A2TR4V
5	BRB1N	55	M7SA4
7	BRB1	57	M5SA4
9	M3SA4	59	
11	M7SA2	61	
13	A2CBRVN	63	M1SA10
15	A2TR1V	65	A2TR7V
17	M5SA1	67	
19	M1SA4	69	M5SA7
21	A2BRZV	71	M7SA10
23	M5SA2	73	
25	M3SA2	75	M5SA10
27	M3SA1	77	M3SA7
29	M1SA1	79	M3SA10
31	M7SA1	81	M1SA7
33	M1SA2	83	M7SA7
35	BRB4N	85	BRB7
37	A2TR2V	87	A2TR10V
39	SIG RET	89	BRB10
41	V1	91	
43	BRB4	93	BRB7N
45	V3	95	BRB10N
47		97	
49			

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotten Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A5A10A

Figure 10-32. Memory Buffer Registers, Logic Diagram (Sheet 6)

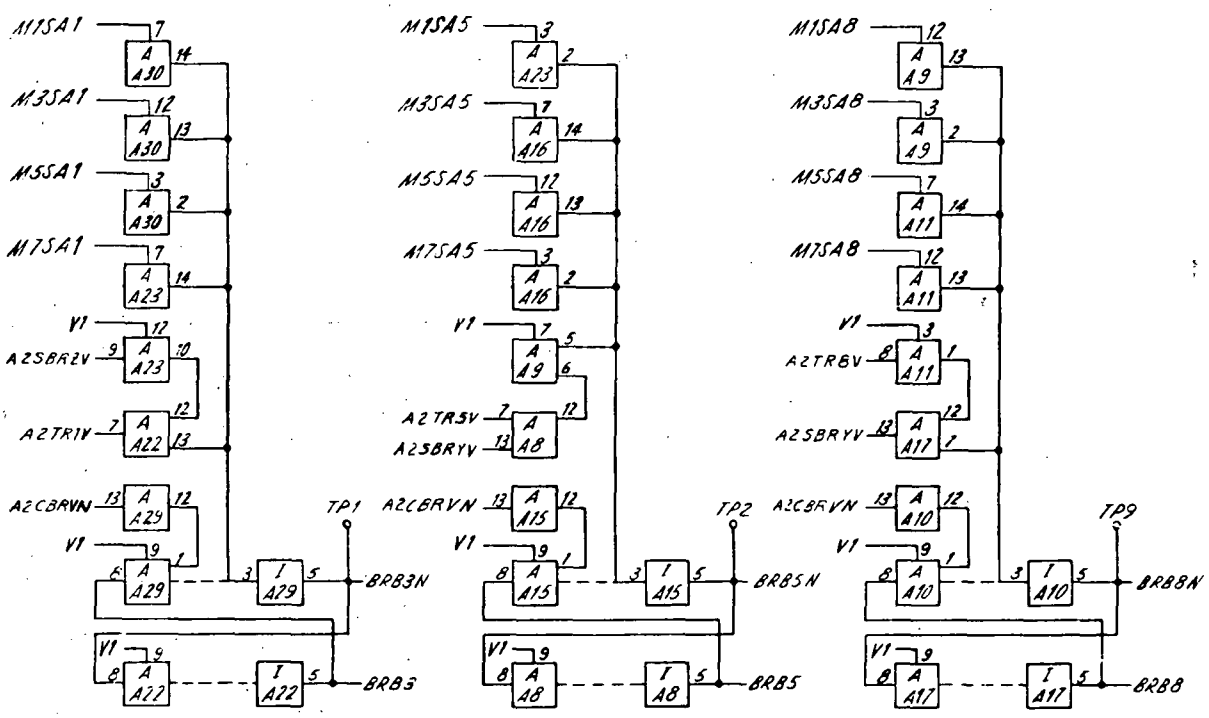
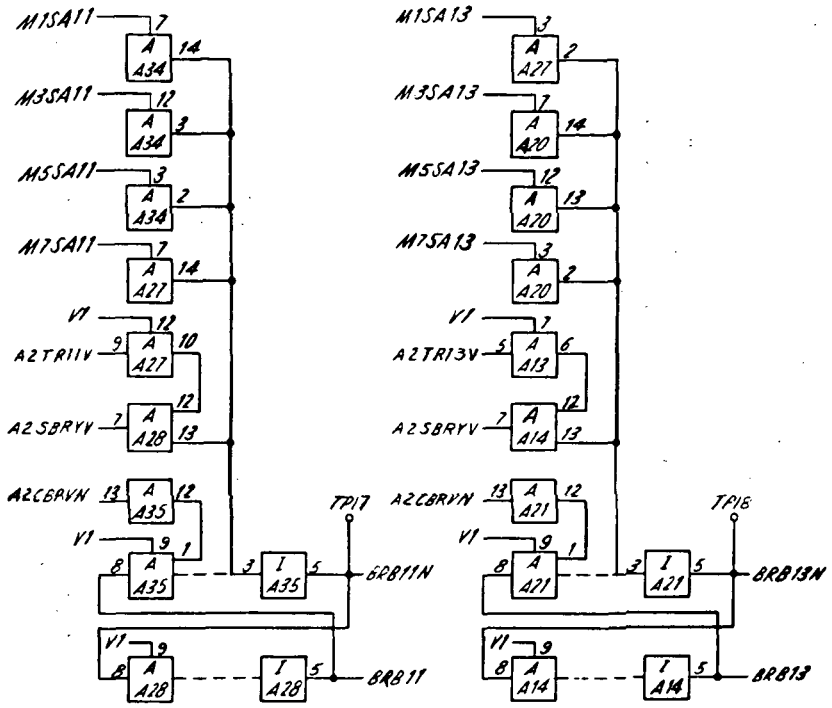


Figure 10-32. Memory Buffer Registers, Logic Diagram (Sheet 7)



CONNECTOR PINS			
Pin	Signal	Pin	Signal
2		52	
4	BRB13N	54	V3
6	BRB11N	56	BRB8
8		58	V1
10	BRB13	60	SIG RET
12	A2TR13V	62	A2TR5V
14	BRB11	64	BRB8N
16	M7SA11	66	M1SA5
18	M1SA11	68	M7SA3
20	M3SA13	70	M1SA3
22	M3SA11	72	M3SA3
24	M5SA13	74	M3SA5
26		76	M5SA5
28	M7SA13	78	A2SBRYV
30	M5SA11	80	M1SA8
32		82	M5SA3
34	A2TR1V	84	A2TR3V
36	M1SA13	86	A2CBRVN
38		88	M7SA5
40		90	M3SA8
42	M5SA8	92	BRB3
44	M7SA8	94	BRB3N
46	A2TR8V	96	BRB5
48		98	BRB5N
50			

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A5A10B

Figure 10-32. Memory Buffer Registers, Logic Diagram (Sheet 8)

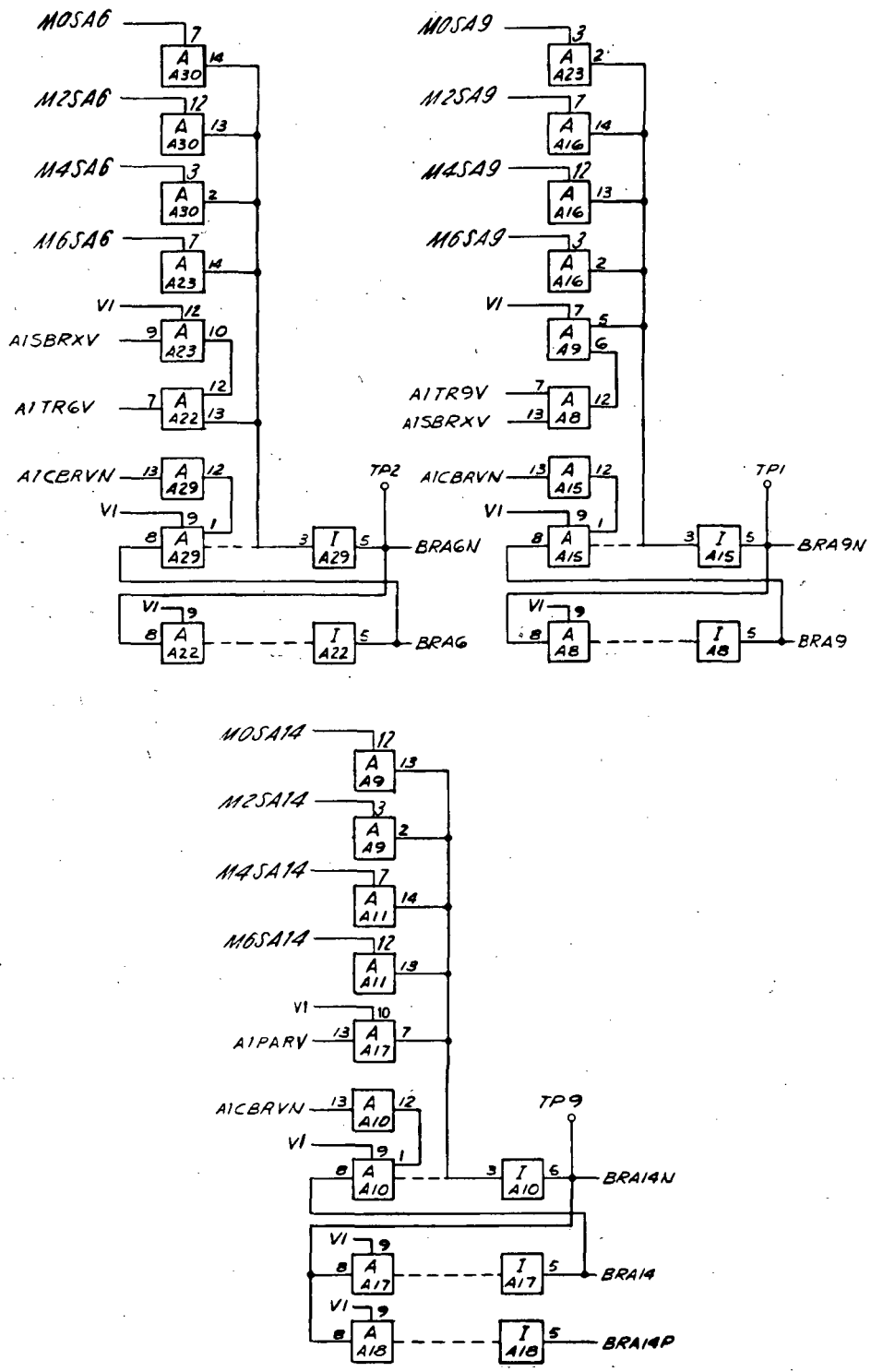
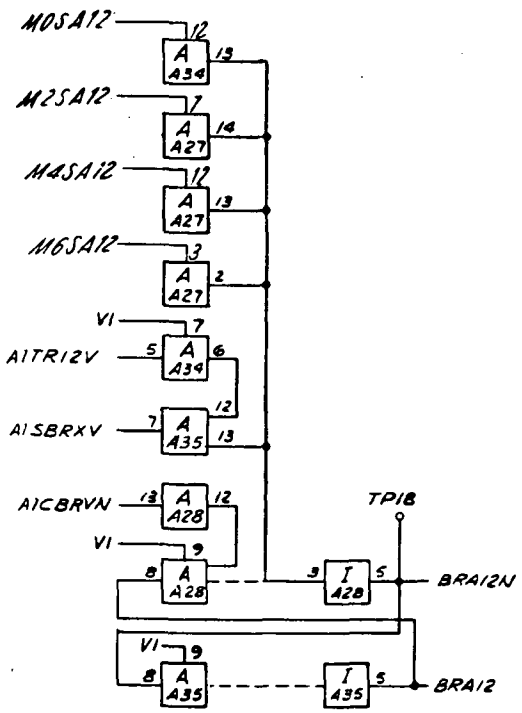


Figure 10-32. Memory Buffer Registers, Logic Diagram (Sheet 9)

A5A11A



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	BRA9	51	
3	BRA6N	53	
5	BRA6	55	M6SA14
7	A1TR6V	57	M4SA14
9	BRA9N	59	
11	M2SA14	61	
13	M0SA14	63	
15	A1TR9V	65	
17	M0SA6	67	
19	M4SA6	69	M6SA12
21	M2SA6	71	
23	M0SA6	73	
25	M6SA6	75	
27	M4SA9	77	M0SA12
29		79	A1TR12V
31	M2SA9	81	M4SA12
33	M6SA9	83	M2SA12
35	BRA14N	85	BRA12N
37	V3	87	
39	V1	89	
41	BRA14	91	
43	A1PARV	93	
45	A10BRVN	95	A1SBRXV
47	SIG RET	97	BRA12
49	BRA14P		

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A5A11A

Figure 10-32. Memory Buffer Registers, Logic Diagram (Sheet 10)

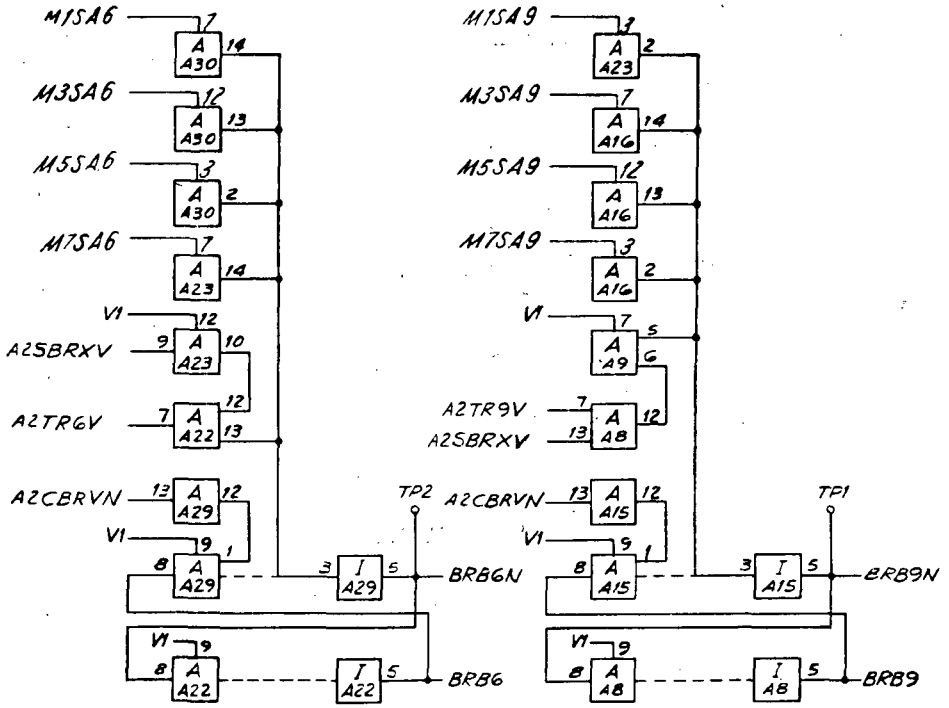
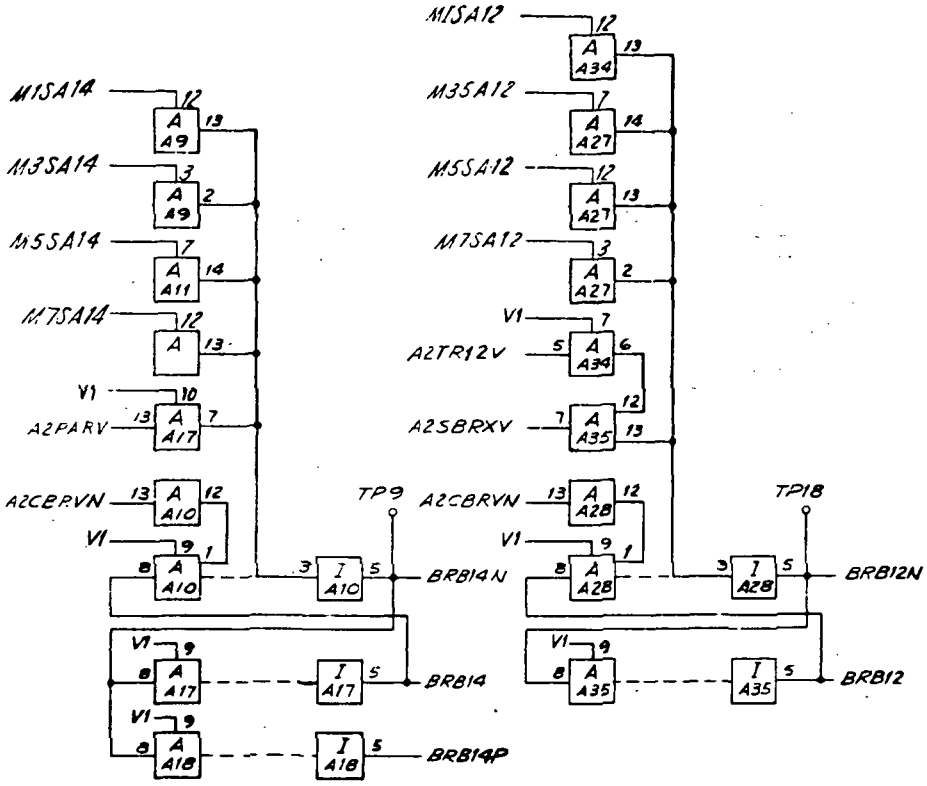


Figure 10-32. Memory Buffer Registers, Logic Diagram (Sheet 11)

A5A11B



CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	BRB12	52	SIG RET
4	A2SBRXV	54	A2CBRVN
6		56	A2PARV
8		58	BRB14
10		60	V1
12		62	V3
14	BRB12N	64	BRB14N
16	M3SA12	66	M7SA9
18	M5SA12	68	M3SA9
20	A2TR12V	70	
22	M1SA12	72	M5SA9
24		74	M7SA6
26		76	M1SA6
28		78	M3SA6
30	M7SA12	80	M5SA6
32		82	M1SA9
34		84	A2TR9V
36		86	M1SA14
38		88	M3SA14
40		90	BRB9N
42	M5SA14	92	A2TR6V
44	M7SA14	94	BRB6
46		96	BRB6N
48		98	BRB9
50	BRB14P		

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A5A11B

Figure 10-32. Memory Buffer Registers, Logic Diagram (Sheet 12)

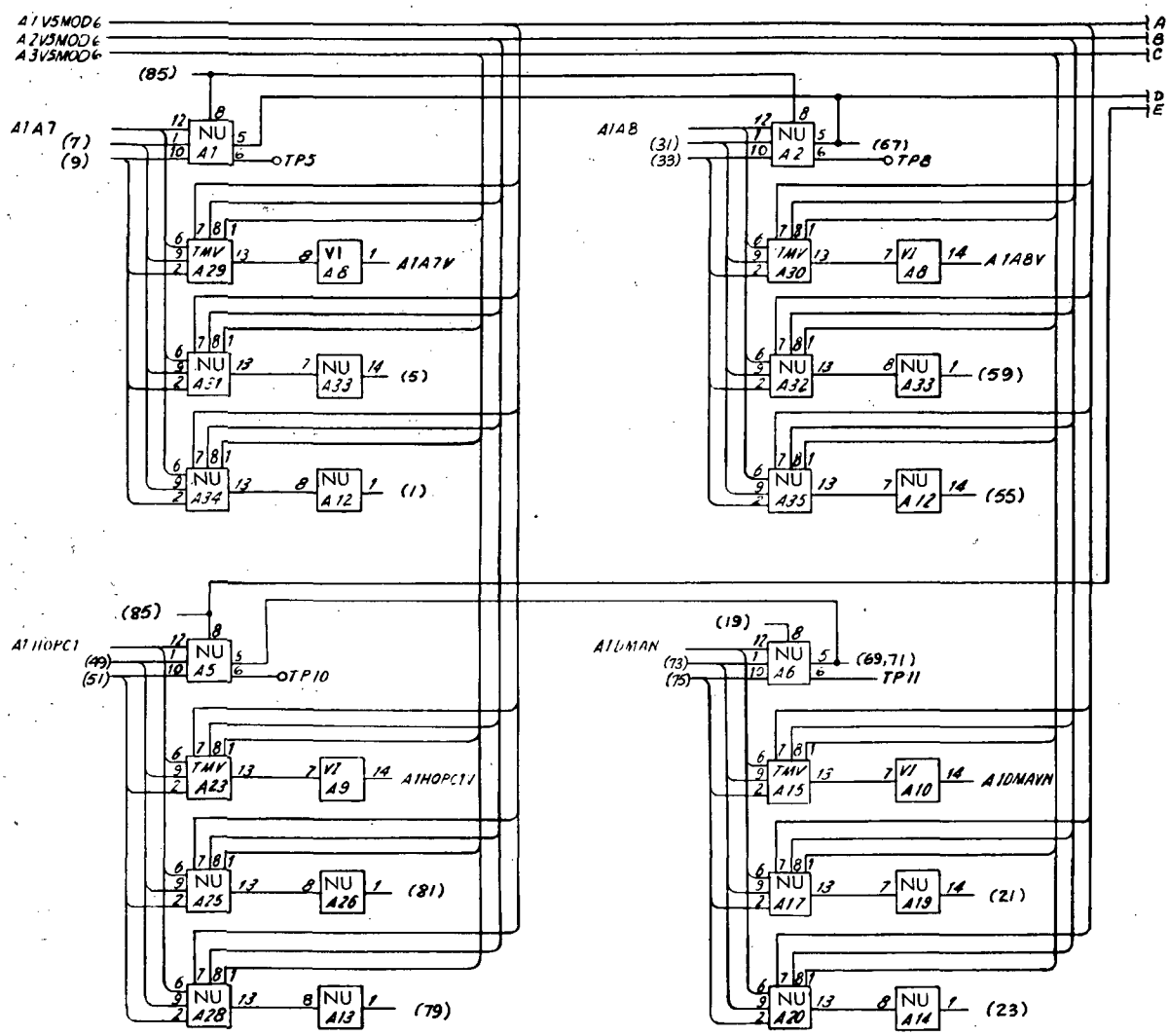
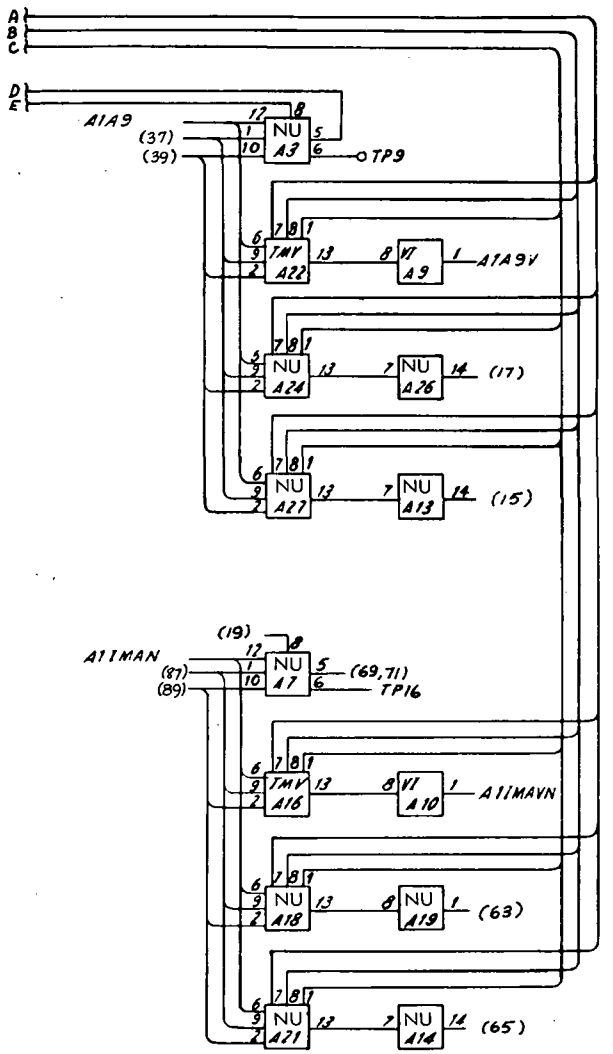


Figure 10-33. Address Register and Memory Module Register Voters, Logic Diagram (Sheet 1 of 4)

A5A12A



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1		51	
3	A1A7V	53	A1HOPC1
5		55	
7		57	A1A8V
9		59	
11	A1A7	61	A1IMAVN
13	A1A9V	63	
15		65	
17		67	
19	A1DMAVN	69	
21		71	
23		73	
25	V1	75	
27	V3	77	A1DMAN
29	SIG RET	79	
31		81	
33		83	A1HOPC1V
35	A1A8	85	
37		87	
39		89	
41	A1A9	91	A1IMAN
43	V1	93	SIG RET
45	V3	95	V1
47	SIG RET	97	V3
49			

THRU PINS			
Pin	Signal	Pin	Signal
1		16	A3V5MOD6
2	SIG RET	17	(74, 2)
3	V1	18	(4, 6)
4	V3	19	(4, 6)
5		20	
6		21	
7		22	
8	SIG RET	23	A2V5MOD6
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	A1V5MOD6

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A5A12A

Figure 10-33. Address Register and Memory Module Register Voters, Logic Diagram (Sheet 2)

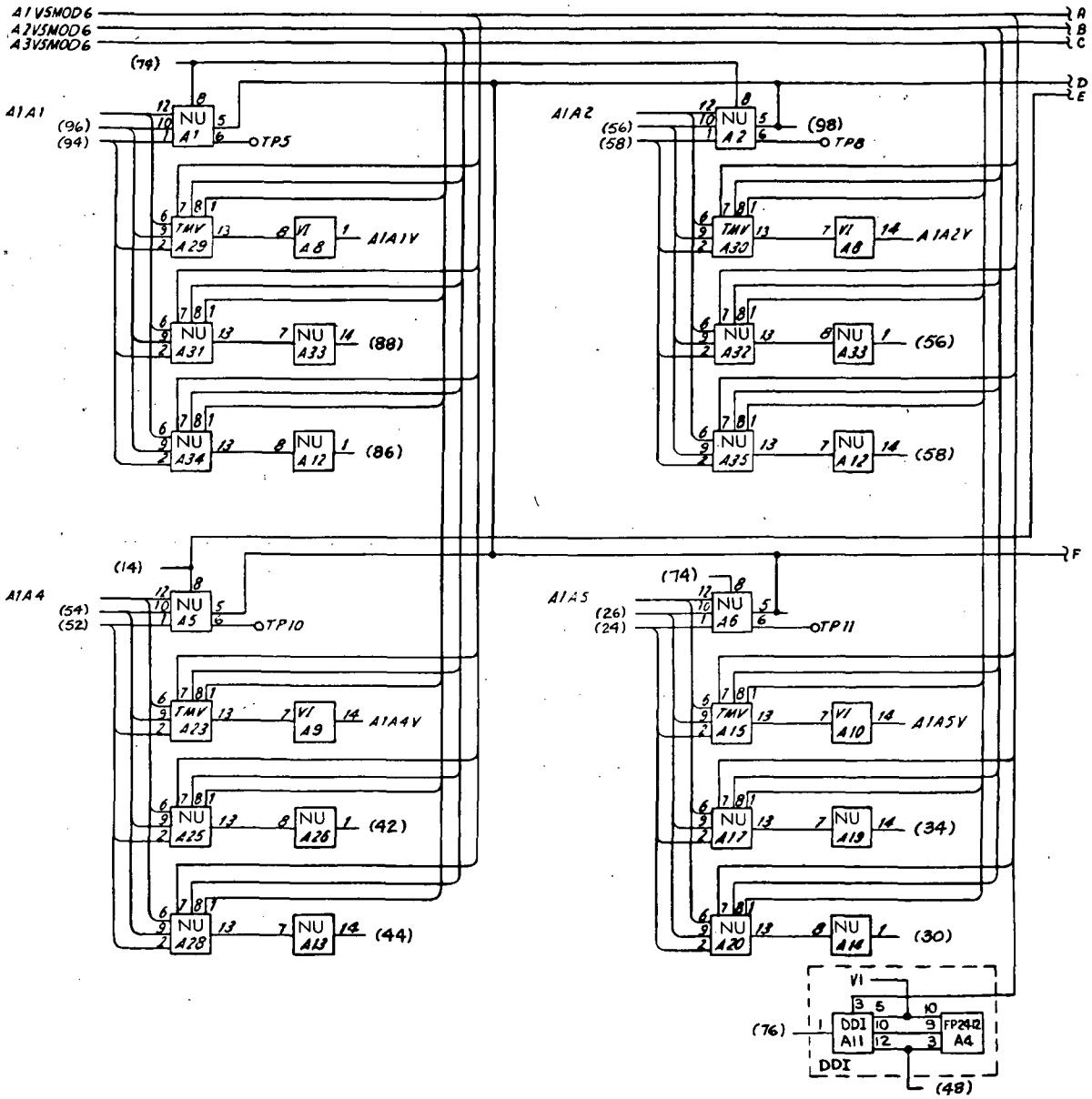
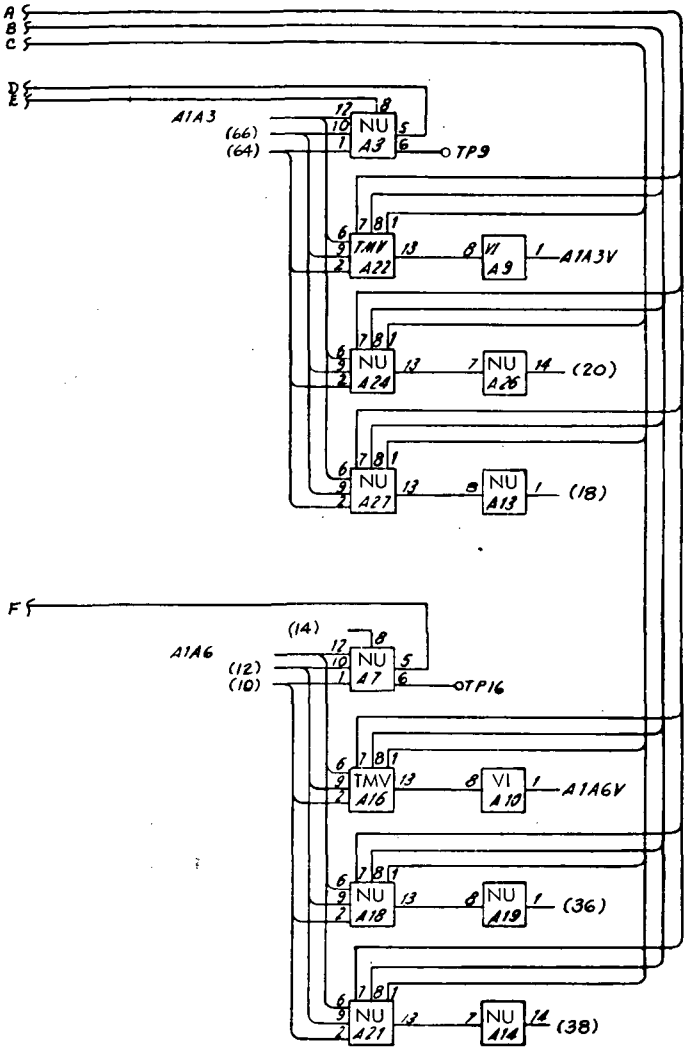


Figure 10-33. Address Register and Memory Module Register Voters, Logic Diagram (Sheet 3)

A5A12B

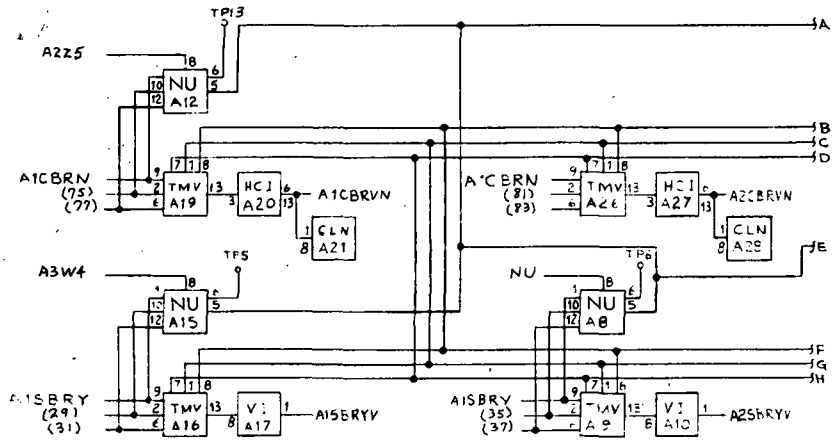


CONNECTOR PINS			
Pin	Signal	Pin	Signal
2		52	
4		54	
6		56	
8	A1A6	58	
10		60	A1A2V
12		62	A1A3
14		64	
16	A1A3V	66	
18		68	A1A2
20		70	
22	A1A5	72	
24		74	
26		76	
28		78	
30		80	A1V5MOD6
32	A1A5V	82	A2V5MOD6
34		84	A3V5MOD6
36		86	
38		88	
40	A1A6V	90	A1A1V
42		92	A1A1
44		94	
46	A1A4V	96	
48		98	
50	A1A4		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	A3V5MOD6
2	SIG RET	17	(74, 2)
3	V1	18	(4, 6)
4	V3	19	(4, 6)
5		20	
6		21	
7		22	
8	SIG RET	23	A2V5MOD6
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	A1V5MOD6

NOTES:
1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A5A12B

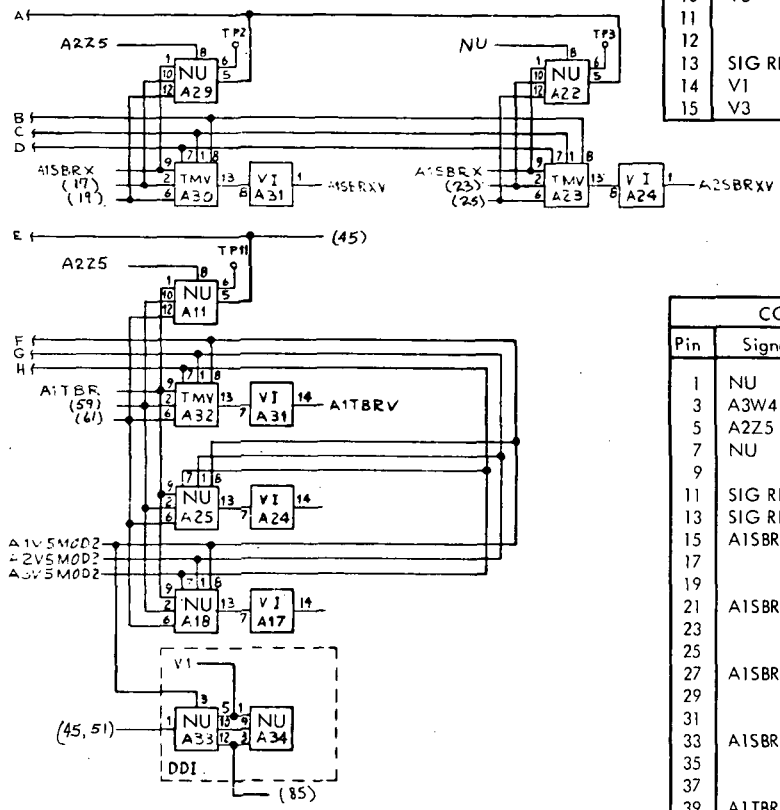
Figure 10-33. Address Register and Memory Module Register Voters, Logic Diagram (Sheet 4)



NOTES

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U. Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A5A13A

Figure 10-34. Transfer Register and Memory Module Register Voters, Logic Diagram (Sheet 1 of 4)



THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2	SIG RET	17	
3	V1	18	
4	V3	19	
5		20	
6		21	
7		22	
8	SIG RET	23	
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	

A5A13A

CONNECTOR PINS			
Pin	Signal	Pin	Signal
1	NU	51	
3	A3W4	53	A2SBRYV
5	A2Z5	55	A1SBRYV
7	NU	57	A1TBR
9		59	
11	SIG RET	61	
13	SIG RET	63	A2SBRXV
15	A1SBRX	65	A1SBRXV
17		67	A3V5MOD2
19		69	A2V5MOD2
21	A1SBRX	71	A1V5MOD2
23		73	A1CBRN
25		75	
27	A1SBRY	77	
29		79	A1CBRN
31		81	
33	A1SBRY	83	
35		85	
37		87	V3
39	A1TBRV	89	V3
41		91	A2Z5
43		93	A2Z5
45		95	A1CBRVN
47	V1	97	A2CBRVN
49	V1	99	

Figure 10-34. Transfer Register and Memory Module Register Voters, Logic Diagram (Sheet 2)

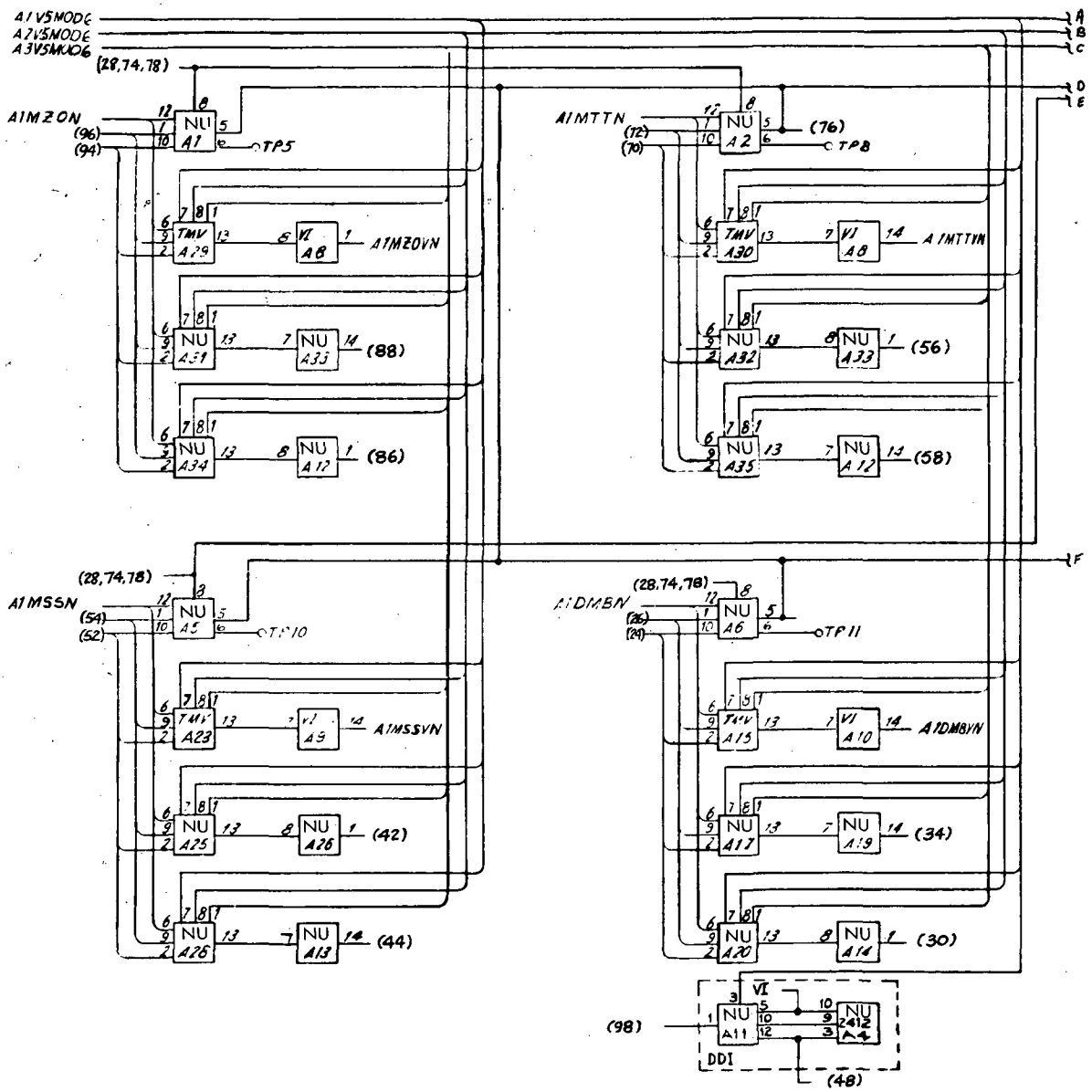
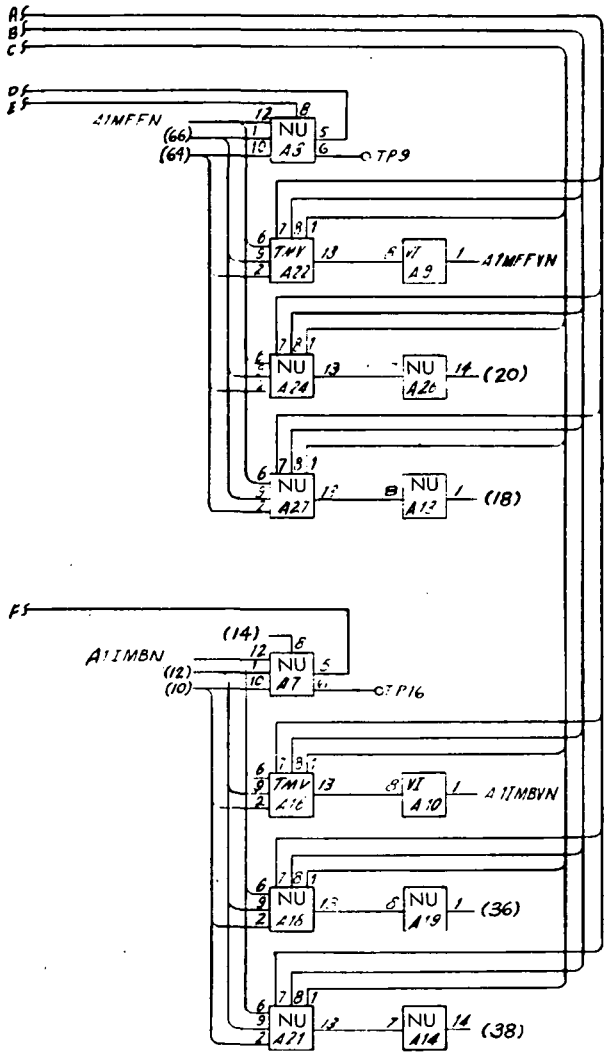


Figure 10-34. Transfer Register and Memory Module Register Voters, Logic Diagram (Sheet 3)



CONNECTOR PINS			
Pin	Signal	Pin	Signal
2	NU1	52	
4	NU2	54	
6	NU3	56	
8	A1IMBN	58	
10		60	A1MTTVN
12		62	A1MFFN
14		64	
16	A1MFFVN	66	
18		68	A1MTTN
20		70	
22	A1DMBN	72	
24		74	
26		76	
28		78	
30		80	A1V5MOD6
32	A1DMBVN	82	A2V5MOD6
34		84	A3V5MOD6
36		86	
38		88	
40	A1IMBVN	90	A1MZOVN
42		92	A1MZON
44		94	
46	A1MSSVN	96	
48		98	
50	A1MSSN		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	A3V5MOD6
2	SIG RET	17	NU1
3	V1	18	NU2
4	V3	19	NU3
5		20	
6		21	
7		22	
8	SIG RET	23	A2V5MOD6
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	A1V5MOD6

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A5A13B

Figure 10-34. Transfer Register and Memory Module Register Voters, Logic Diagram (Sheet 4)

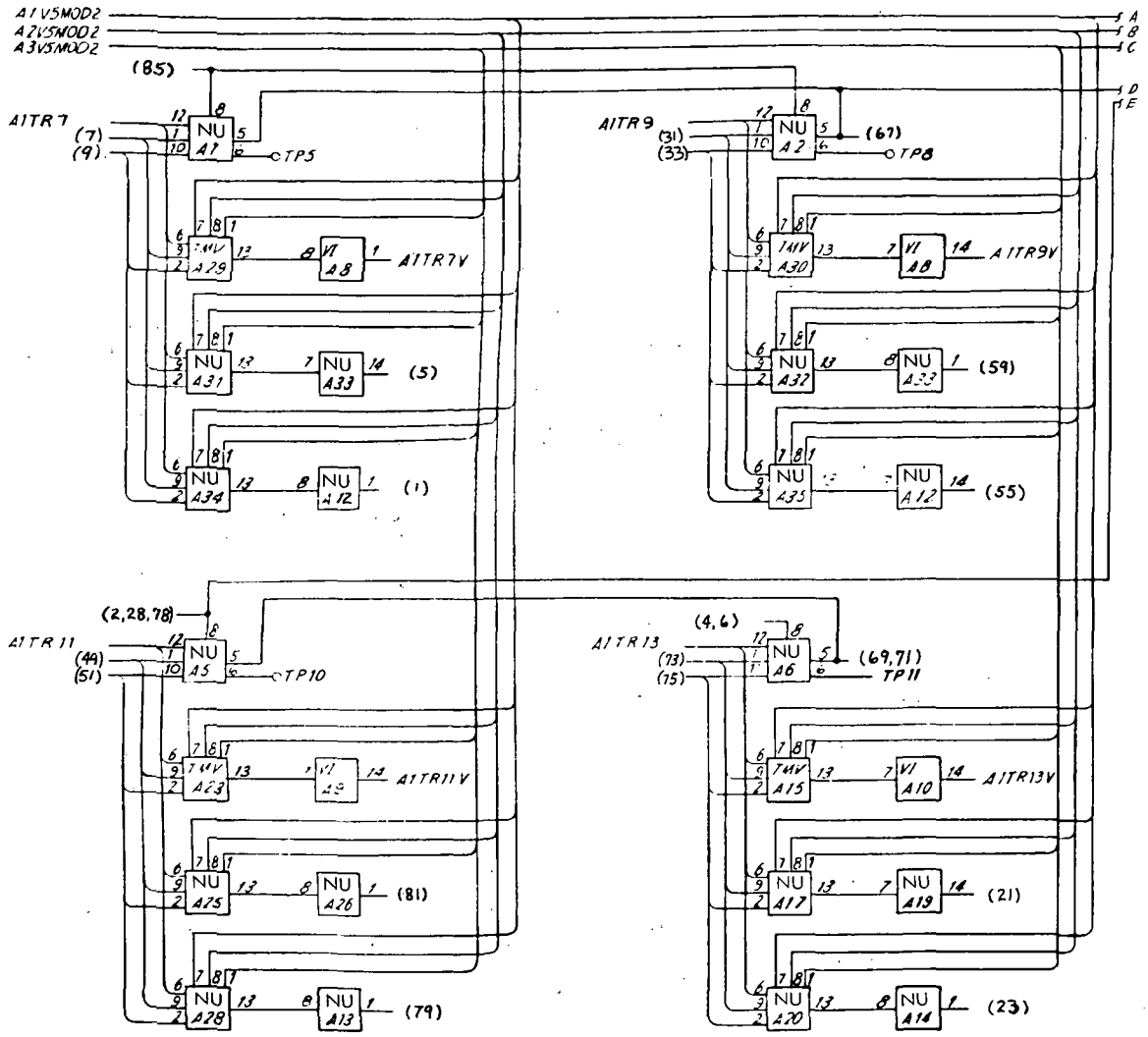
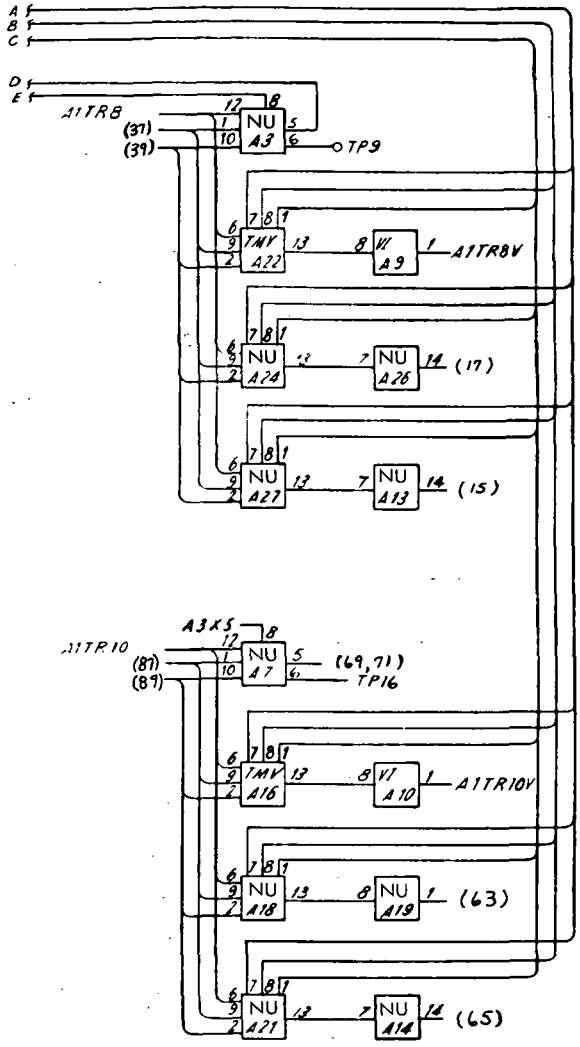


Figure 10-35. Transfer Register Voters, Logic Diagram (Sheet 1 of 6)

A5A14A



NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate it
5. Prefix Reference Designations as Follows: A5A14A

CONNECTOR PINS			
Pin	Signal	Pin	Signal
1		51	
3	A1TR7V	53	A1TR11
5		55	
7		57	A1TR9V
9		59	
11	A1TR7	61	A1TR10V
13	A1TR8V	63	
15		65	
17		67	
19	A1TR13V	69	
21		71	
23		73	
25	V1	75	
27	V3	77	A1TR13
29	SIG RET	79	
31		81	
33		83	A1TR11V
35	A1TR9	85	
37		87	
39		89	
41	A1TR8	91	A1TR10
43	V1	93	SIG RET
45	V3	95	V1
47	SIG RET	97	V3
49			

THRU PINS			
Pin	Signal	Pin	Signal
1		16	A3V5MOD2
2	SIG RET	17	(2, 28, 78)
3	V1	18	(4, 6)
4	V3	19	(4, 6)
5		20	
6		21	
7		22	
8	SIG RET	23	A2V5MOD2
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	A1V5MOD2

Figure 10-35. Transfer Register Voters, Logic Diagram (Sheet 2)

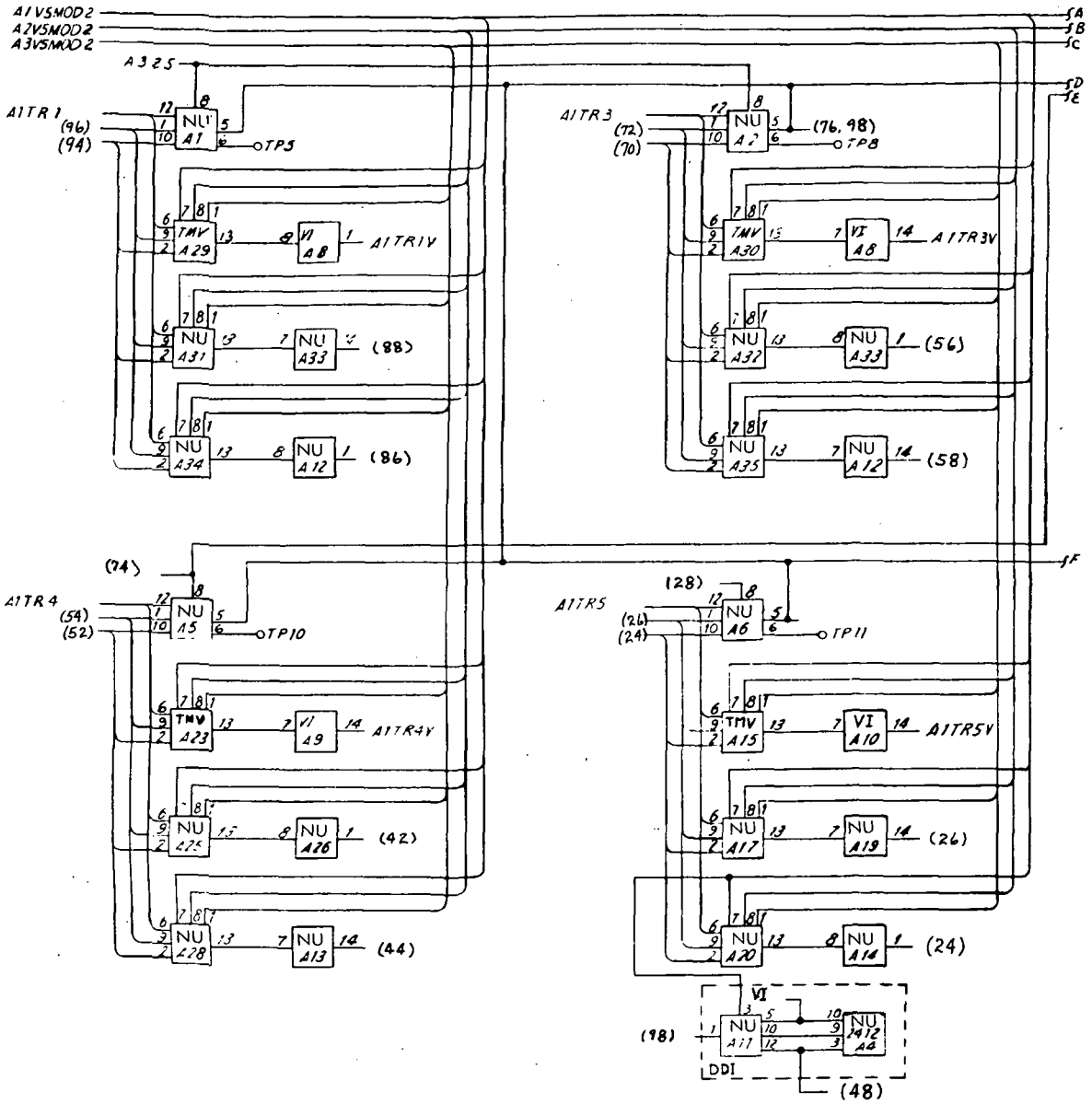
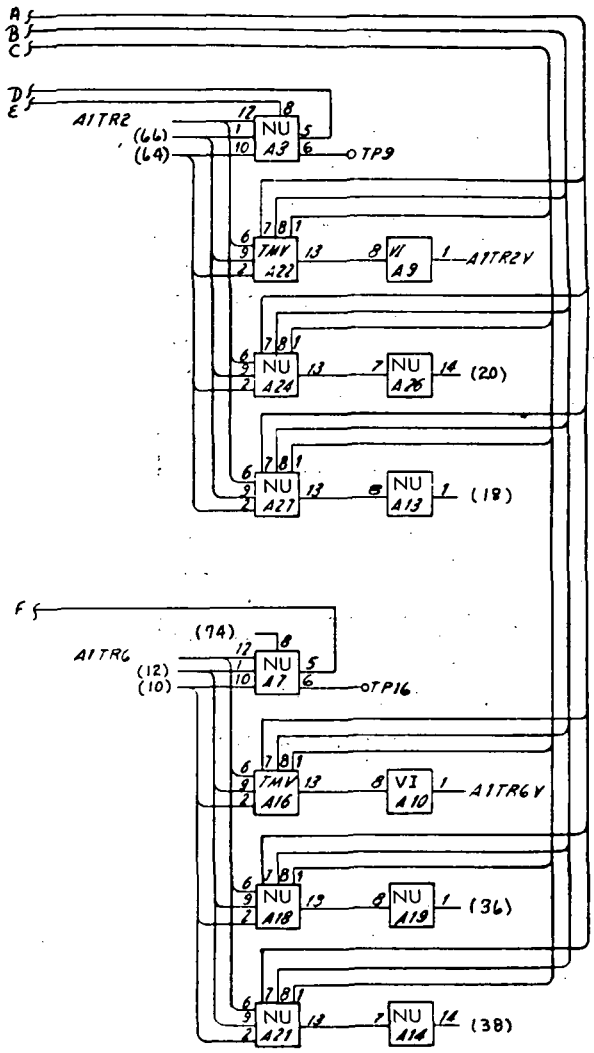


Figure 10-35. Transfer Register Voters, Logic Diagram (Sheet 3)



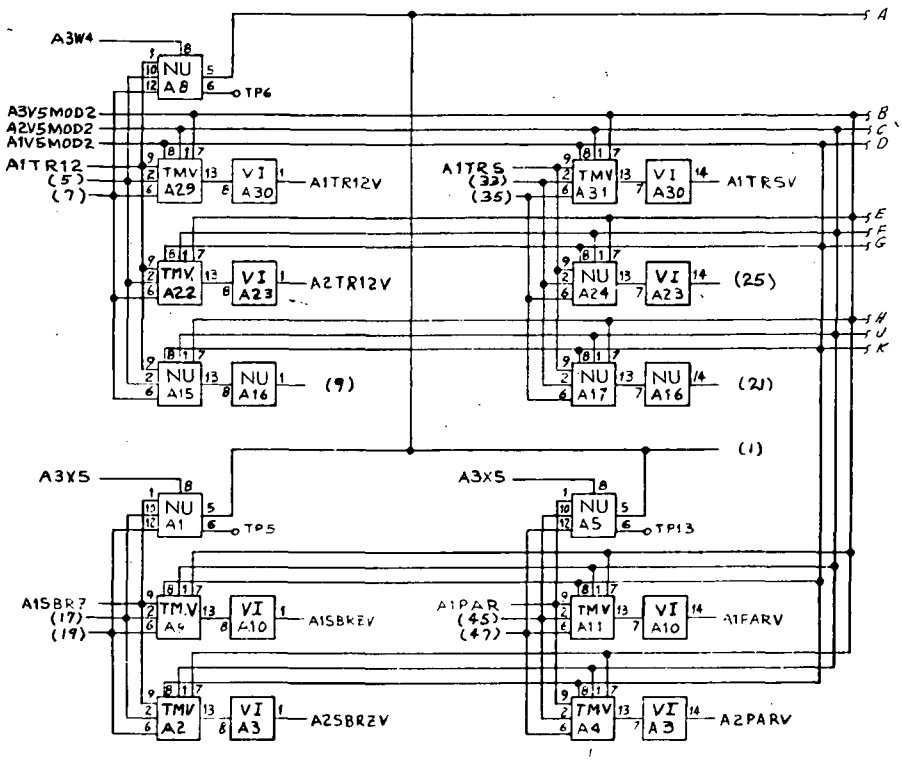
NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotten Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A5A14B

CONNECTOR PINS			
Pin	Signal	Pin	Signal
2		52	
4		54	
6		56	
8	A1TR6	58	
10		60	A1TR3V
12		62	A1TR2
14		64	
16	A1TR2V	66	
18		68	A1TR3
20		70	
22	A1TR5	72	
24		74	
26		76	
28		78	
30		80	A1V5MOD2
32	A1TR5V	82	
34		84	
36		86	
38		88	
40	A1TR6V	90	A1TR1V
42		92	A1TR1
44		94	
46	A1TR4V	96	
48		98	
50	A1TR4		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	A3V5MOD2
2	SIG RET	17	(28, 2, 78)
3	V1	18	(4, 6)
4	V3	19	(4, 6)
5		20	
6		21	
7		22	
8	SIG RET	23	A2V5MOD2
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG RET	28	
14	V4	29	
15	V3	30	A1V5MOD2

Figure 10-35. Transfer Register Voters, Logic Diagram (Sheet 4)

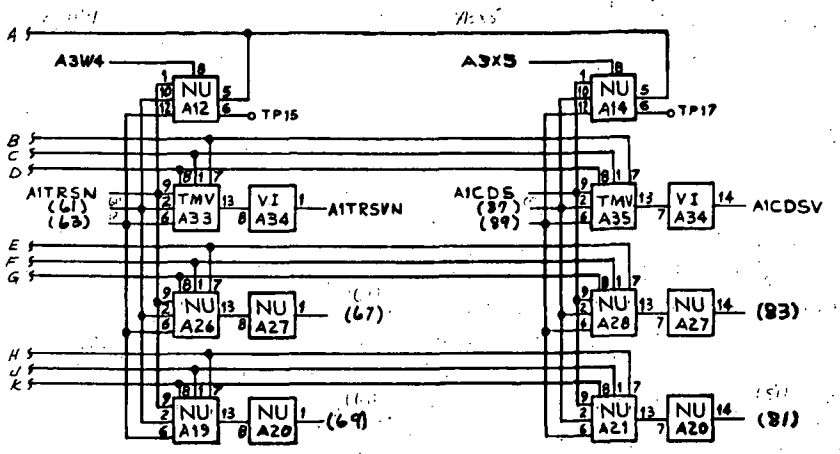


NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A5A15A

Figure 10-35. Transfer Register Voters, Logic Diagram (Sheet 5)

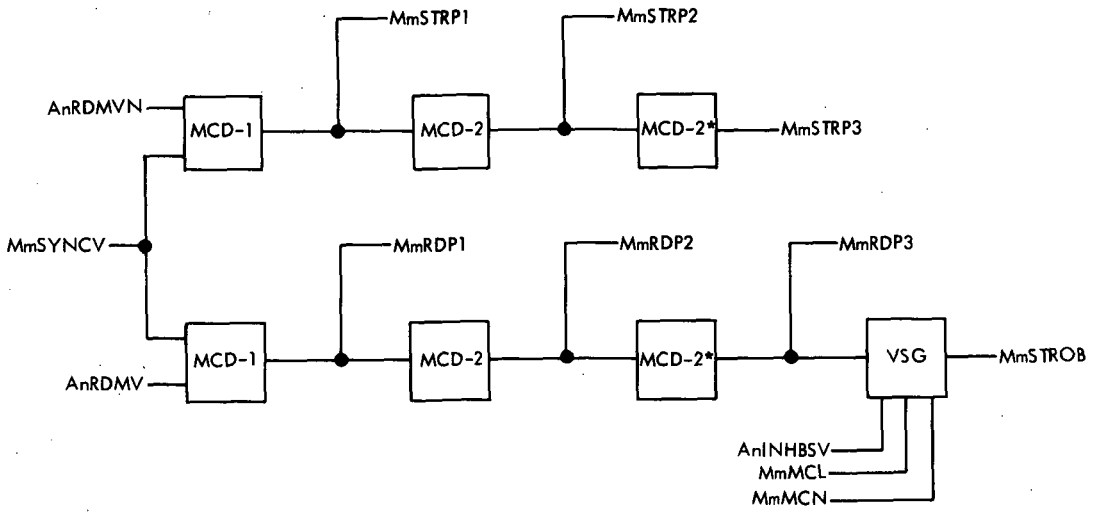
A5A15A



CONNECTOR PINS			
Pin	Signal	Pin	Signal
1		51	SIG RET
3	A1TR12	53	A3X5
5		55	V3
7		57	A3X5
9		59	A1TRSN
11	A2TR12V	61	
13	A1TR12V	63	
15	A1SBRZ	65	V3
17		67	
19		69	
21		71	A1TRSVN
23	A1TRSV	73	A3W4
25		75	V1
27	A2SBRZV	77	A3X5
29	A1SBRZV	79	A1CDSV
31	A1TRS	81	
33		83	
35		85	A1CDS
37	A3W4	87	
39	A1PARV	89	
41	A2PARV	91	A1V5MOD2
43	A1PAR	93	A2V5MOD2
45		95	A3V5MOD2
47		97	V1
49	SIG RET		

THRU PINS			
Pin	Signal	Pin	Signal
1		16	
2		17	
3		18	
4		19	
5		20	
6		21	
7		22	
8		23	
9		24	
10		25	
11		26	
12		27	
13		28	
14		29	
15		30	

Figure 10-35. Transfer Register Voters, Logic Diagram (Sheet 6)

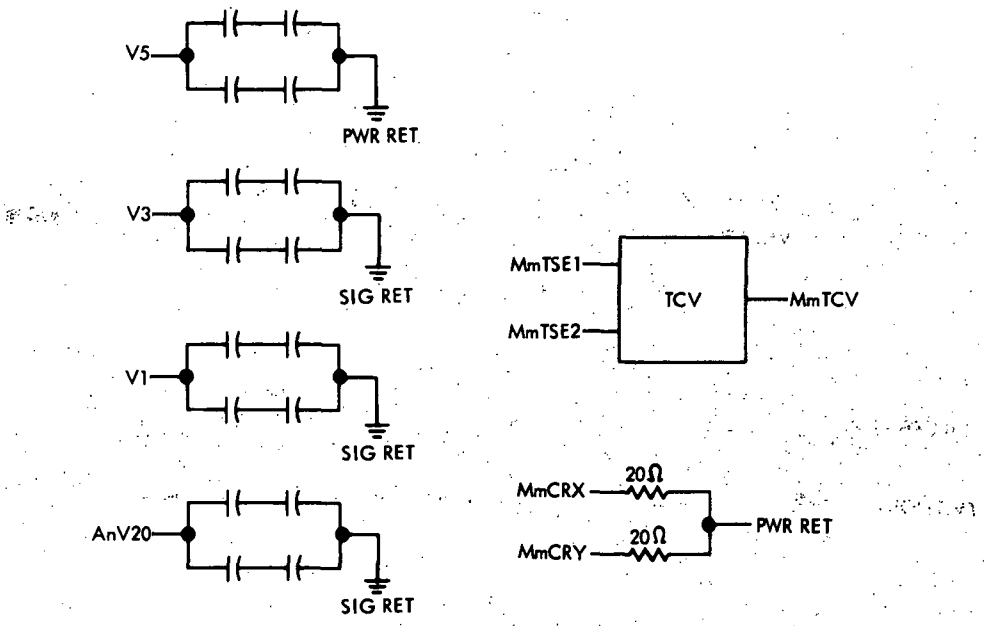


NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate it
5. Prefix Reference Designations as Follows: A6AMA6A1, where M = Memory Module Assembly Number 1 through 4
6. Terminals with Numbers Prefixed by "A" are Located on the MIB. All Others are Located on the Printed Circuit Board
7. m Represents the Memory Module Number 0 through 3
8. n is a 1 if m is an Even Number, and a 2 if m is an Odd Number
9. Asterisk Indicates Narrower Output Pulse than from Preceding MCD-2 Circuit

Figure 10-36. Memory Clock Driver and TCV, Logic Diagram (Sheet 1 of 2)

A6AMA6A1



TERMINAL AREA - E 1			
PIN	SIGNAL	PIN	SIGNAL
1	MmTSE2	22	MmMCN
2	MmTSE1	23	MmMCL
3	V5	24	PWR RET
4	V5	25	PWR RET
5		26	MmSTRP1
6		27	MmSTRP2
7	V1	28	AnM20ID
8	V1	29	AnM20ID
9		30	MmINH2
10	TCVADJ	31	MmINH4
11	AnM20	32	MmINH6
12	AnM20ID	33	MmINH8
13	AnM20ID	34	MmINH10
14	AnRDMV	35	MmINH12
15	V3	36	MmINH14
16	V3	37	V3
17	AnRDMVN	38	MmTCV
18	SIG RET	39	MmTCV
19	SIG RET	40	SIG RET
20	MnSYNCV	41	SIG RET
21	AnINHBSV	42	MmSTROB

TERMINAL AREA - E 2			
PIN	SIGNAL	PIN	SIGNAL
1	MmCRX	6	MmSTRP1
2	MmCRX	7	MmSTRP3
3	MmTCV	8	MmRDP3
4	MmTCV	9	MmRDP2
5	SIG RET		

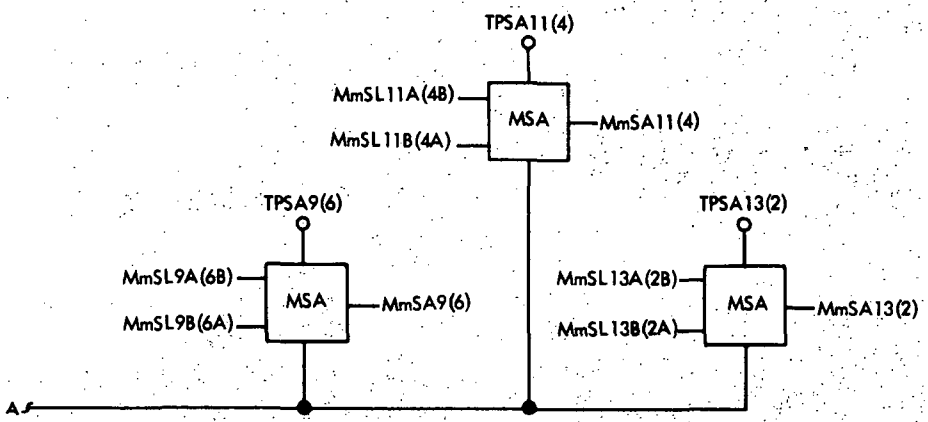
TERMINAL AREA - E 4			
PIN	SIGNAL	PIN	SIGNAL
1	MmCRY	6	MmRDP2
2	MmCRY	7	MmSTRP1
3	MmTCV	8	MmSTRP2
4	MmTCV	9	MmRDP1
5	SIG RET		

Figure 10-36. Memory Clock Driver and TCV, Logic Diagram (Sheet 2)

Figure 10-37. Memory Sense Amplifiers, Logic Diagram (Sheet 1 of 2)

Changed 4 January 1965

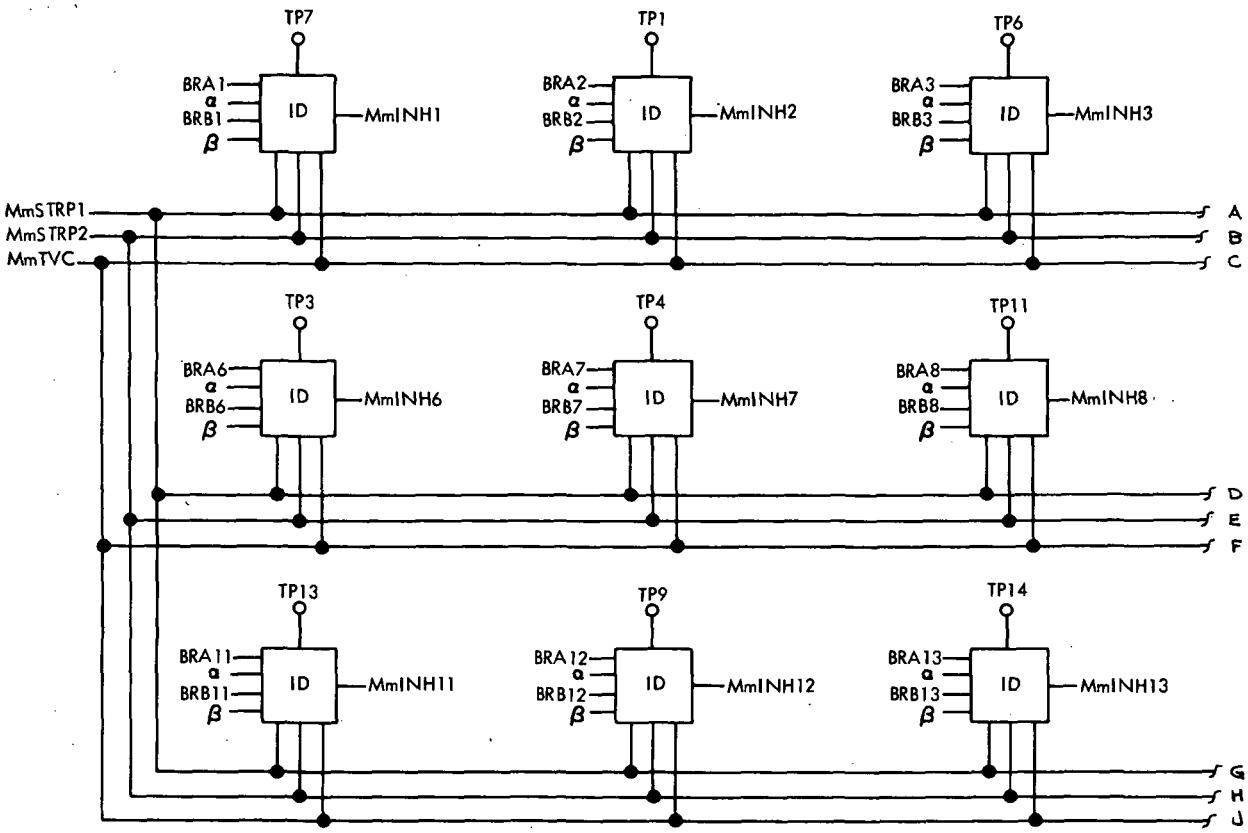
A6AMA3A1



TERMINAL AREA - E 1			
PIN	SIGNAL	PIN	SIGNAL
1	MmSL14B	16	MmSL7A
2	MmSL14A	17	MmSL6B
3	MmSL13B	18	MmSL6A
4	MmSL13A	19	MmSL5B
5	MmSL12B	20	MmSL5A
6	MmSL12A	21	MmSL4B
7	MmSL11B	22	MmSL4A
8	MmSL11A	23	MmSL3B
9	MmSL10B	24	MmSL3A
10	MmSL10A	25	MmSL2B
11	MmSL9B	26	MmSL2A
12	MmSL9A	27	MmSL1B
13	MmSL8B	28	MmSL1A
14	MmSL8A		
15	MmSL7B		

TERMINAL AREA - E 3			
Pin	Signal	Pin	Signal
1	MmSTROB	30	MmSTROB
2		31	
3		32	
4	TPSA14	33	MmSA14
5	TPSA13	34	MmSA13
6	TPSA12	35	MmSA12
7	TPSA11	36	MmSA11
8	TPSA10	37	MmSA10
9	TPSA9	38	MmSA9
10	V3	39	V3
11	TPSA7	40	MmSA7
12		41	
13	V1	42	V1
14	V5	43	V5
15	SIG RET	44	SIG RET
16	SIG RET	45	SIG RET
17	V5	46	V5
18	V1	47	V1
19		48	
20	TPSA8	49	MmSA8
21	V3	50	V3
22	TPSA6	51	MmSA6
23	TPSA5	52	MmSA5
24	TPSA4	53	MmSA4
25	TPSA3	54	MmSA3
26	TPSA2	55	MmSA2
27	TPSA1	56	MmSA1
28		57	
29		58	

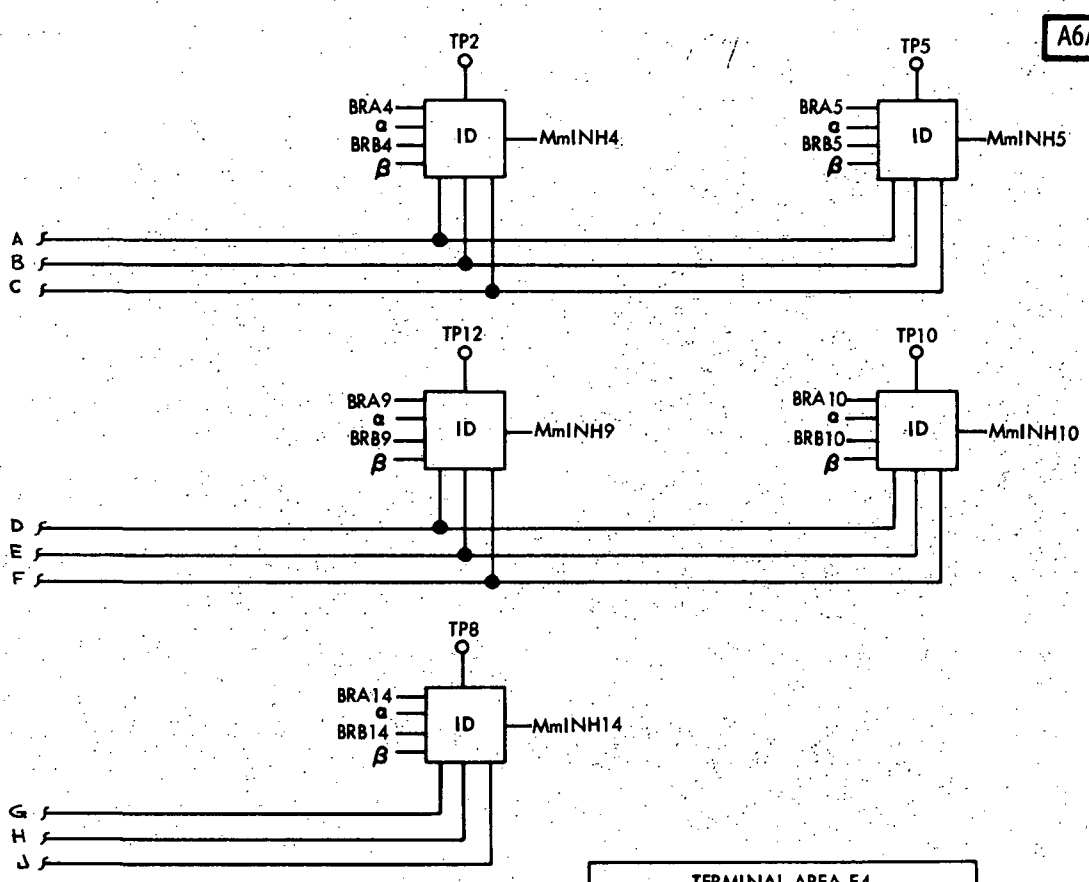
Figure 10-37. Memory Sense Amplifiers, Logic Diagram (Sheet 2)



NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate it
5. Prefix Reference Designations as Follows: A6AMA7A1, where M = Memory Module Assembly Number 1 through 4
6. m Represents the Memory Module Number 0 through 3
7. n is a 1 if m is an Even Number, and a 2 if m is an Odd Number
8. If m is an Even Number, α = A1BRAOV and β = A2BRAOVN
9. If m is an Odd Number, α = A1BRBOVN and β = A2BRBOV

Figure 10-38. Memory Inhibit Drivers, Logic Diagram (Sheet 1 of 2)



TERMINAL AREA E2			
PIN	SIGNAL	PIN	SIGNAL
1	AnM20	6	MmINH9
2	MmINH1	7	MmINH11
3	MmINH5	8	MmINH13
4	MmINH5	9	AnM20
5	MmINH7		

TERMINAL AREA E4			
PIN	SIGNAL	PIN	SIGNAL
1	β	26	BRA9
2	α	27	BRB11
3	BRA1	28	BRA11
4	BRB1	29	BRB13
5	BRA3	30	BRA13
6	BRB3	31	PWR RET
7	BRA5	32	PWR RET
8	BRB5	33	PWR RET
9	BRA7	34	MmSTRP1
10	BRB7	35	MmSTRP2
11	BRA6	36	AnM20
12	BRB6	37	AnM20
13	BRA4	38	MmINH2
14	BRB4	39	MmINH4
15	BRA2	40	MmINH6
16	BRB2	41	MmINH8
17	BRB10	42	MmINH10
18	BRA12	43	MmINH12
19	BRB12	44	MmINH14
20	BRA14	45	V3
21	BRB14	46	MmTCV
22	BRA10	47	MmTCV
23	BRB8	48	SIG RET
24	BRA8	49	SIG RET
25	BRB9	50	

Figure 10-38. Memory Inhibit Drivers, Logic Diagram (Sheet 2)

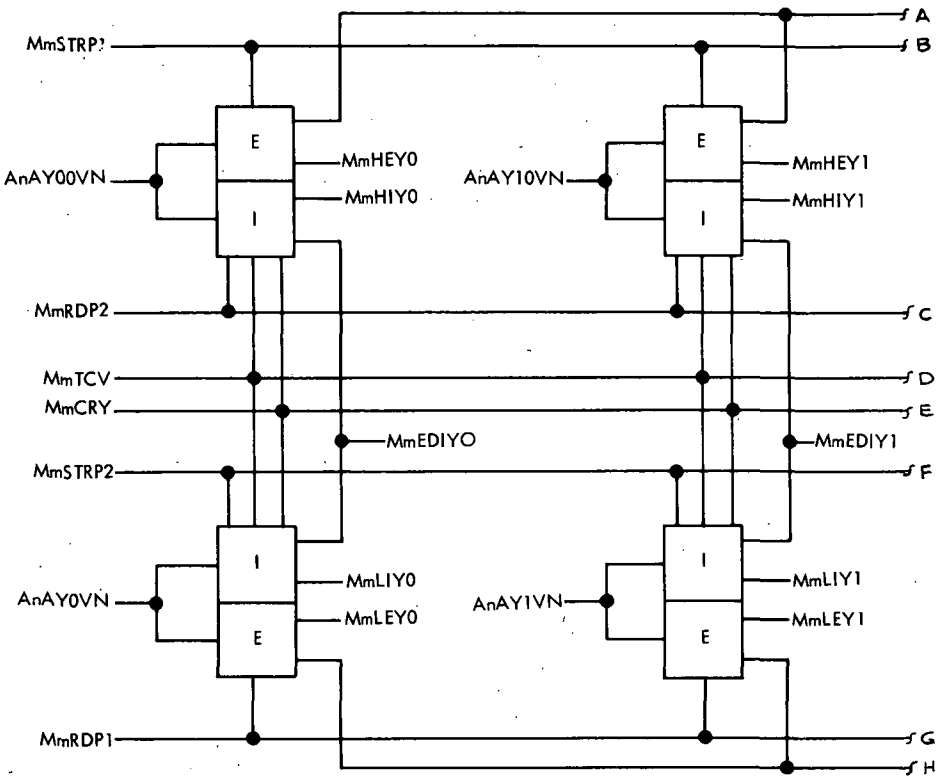
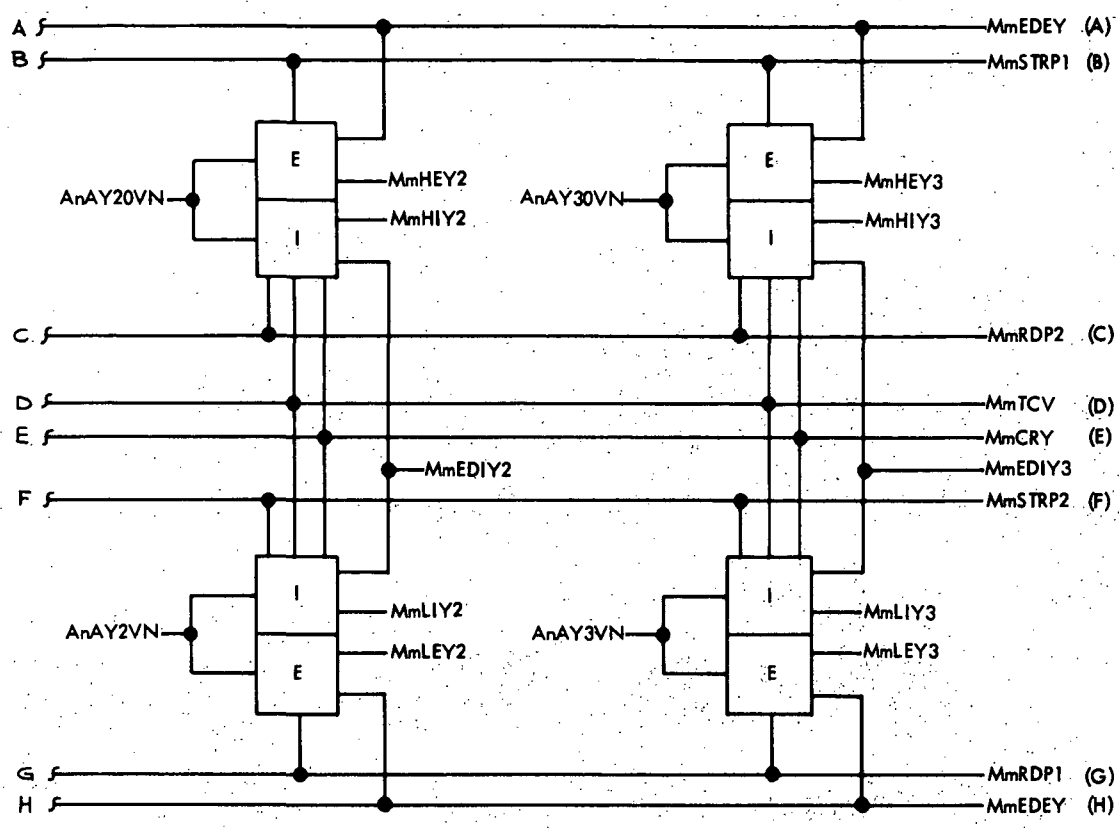


Figure 10-39. Memory Y-Address Drivers, Logic Diagram (Sheet 1 of 4)



TERMINAL AREA - E 1			
PIN	SIGNAL	PIN	SIGNAL
1		20	MmLIY6
2		21	
3		22	MmLEY7
4		23	
5		24	MmLIY7
6	MmLEY0	25	
7		26	MmLEY5
8	MmLIY0	27	
9		28	MmLIY5
10	MmLEY2	29	
11		30	MmLEY3
12	MmLIY2	31	
13		32	MmLIY3
14	MmLEY4	33	
15		34	MmLEY1
16	MmLIY4	35	
17		36	MmLIY1
18	MmLEY6	37	
19		38	

TERMINAL AREA - E 3			
PIN	SIGNAL	PIN	SIGNAL
1		23	
2	MmHEY0	24	MmHIY4
3		25	
4	MmHIY0	26	MmHEY5
5		27	
6	MmHEY1	28	MmHIY5
7		29	
8	MmHIY1	30	
9		31	MmHEY6
10		32	MmHIY6
11		33	MmHEY7
12	MmHEY2	34	MmHIY7
13		35	MmCRY
14	MmHIY2	36	MmCRY
15		37	MmTCV
16	MmHEY3	38	MmTCV
17		39	
18	MmHIY3	40	MmRDP2
19		41	MmSTRP1
20		42	MmSTRP2
21		43	MmRDP1
22	MmHEY4		

TERMINAL AREA - E 4			
PIN	SIGNAL	PIN	SIGNAL
1	MmTCV	18	V3
2		19	EDMY
3	AnM20	20	V1
4	AnAY7VN	21	
5	AnAY5VN	22	PWR RET
6	AnAY3VN	23	PWR RET
7	AnAY0VN	24	AnAY60VN
8	AnAY1VN	25	AnAY40VN
9	AnAY2VN	26	AnAY20VN
10	AnAY4VN	27	AnAY10VN
11	AnAY6VN	28	AnAY00VN
12	SIG RET	29	AnAY30VN
13	SIG RET	30	AnAY50VN
14		31	AnAY70VN
15	V1	32	AnM20
16	EDmY	33	
17	V3	34	MmTCV

Figure 10-39. Memory Y-Address Drivers, Logic Diagram (Sheet 2)

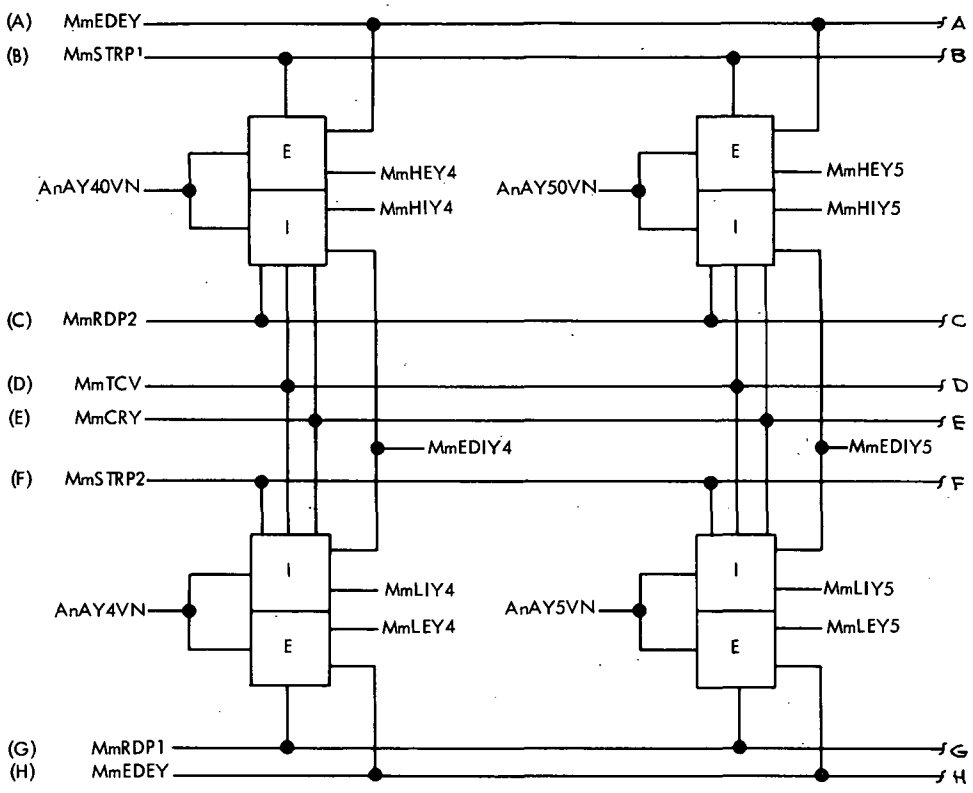
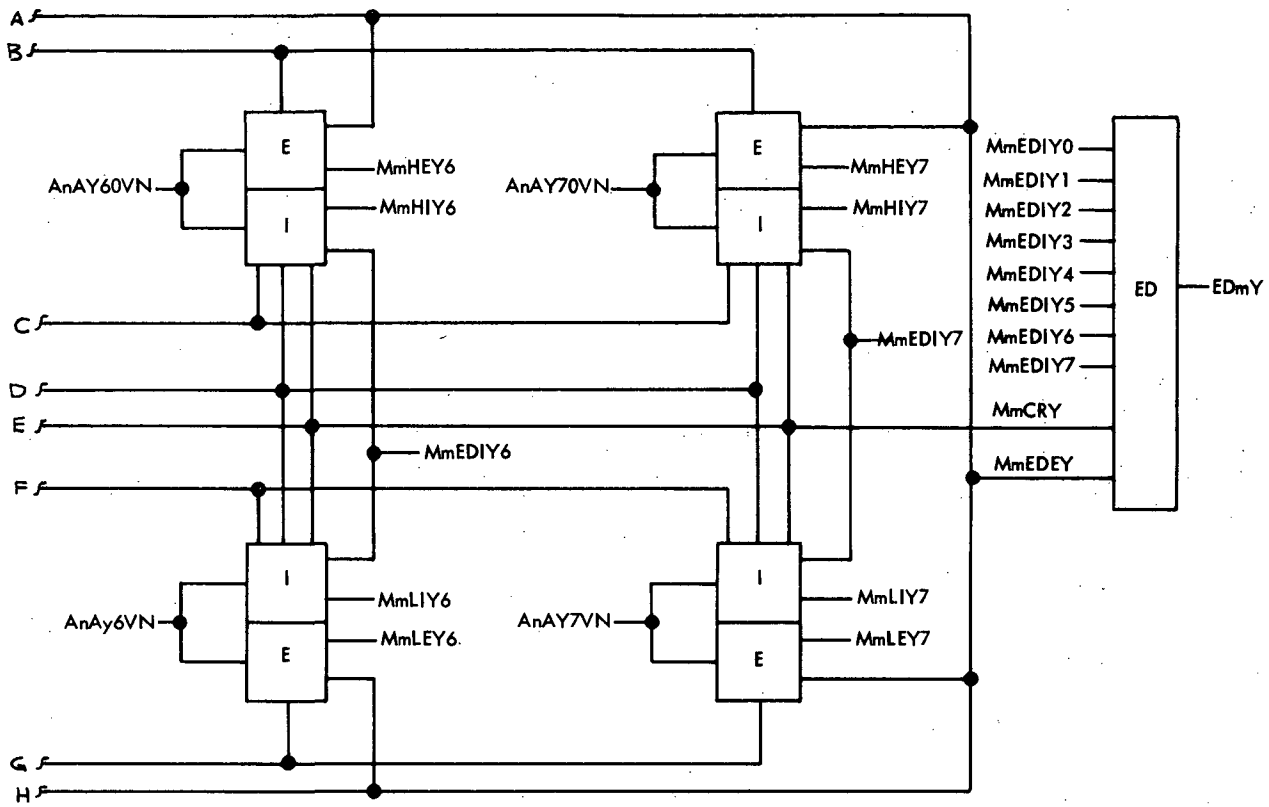


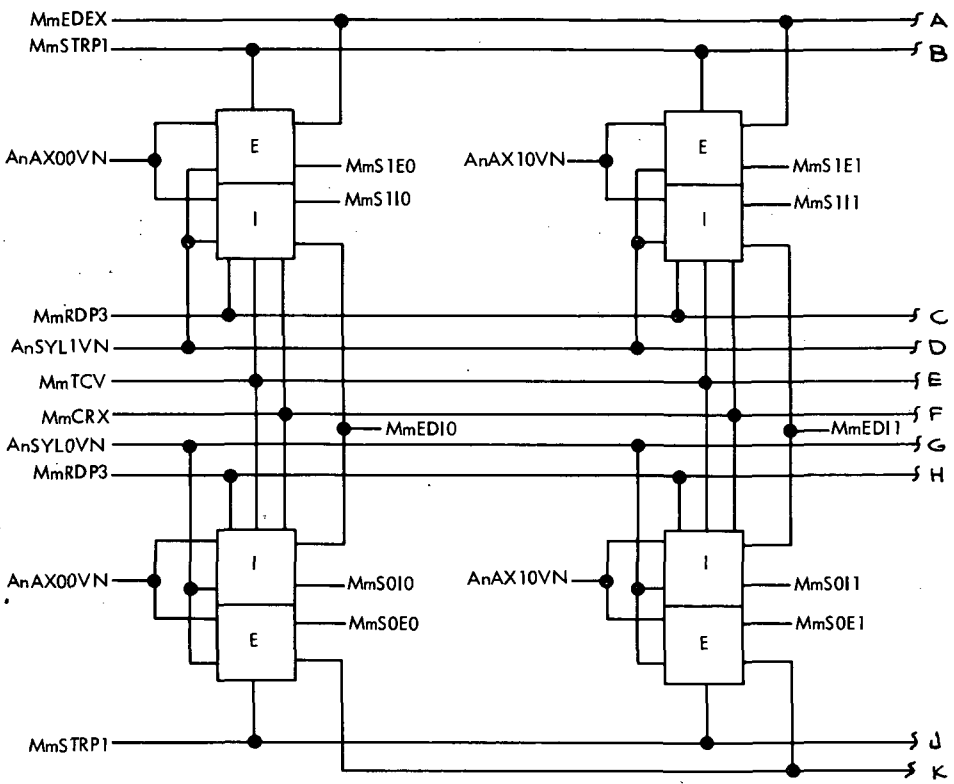
Figure 10-39. Memory Y-Address Drivers, Logic Diagram (Sheet 3)



NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate it
5. Prefix Reference Designations as Follows: A6AMA5A1, where M = Memory Module Assembly Number 1 through 4
6. m Represents the Memory Module Number 0 through 3
7. n is a 1 if m is an Even Number, and a 2 if m is an Odd Number.

Figure 10-39. Memory Y-Address Drivers, Logic Diagram (Sheet 4)

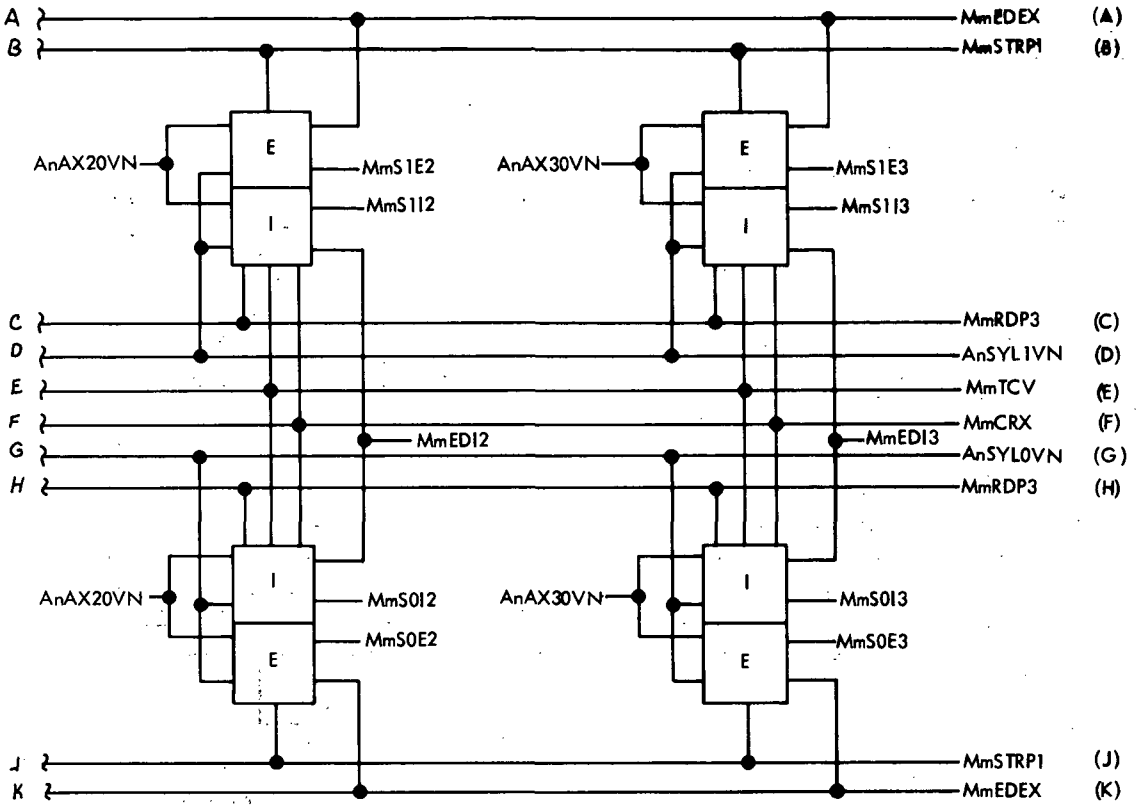


NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate it
5. Prefix Reference Designations as Follows: A6AMA1A1 where M = Memory Module Assembly Number 1 through 4
6. m Represents the Memory Module Number 0 through 3
7. n is a 1 if m is an Even Number, and a 2 if m is an Odd Number

Figure 10-40. Memory Hi-X Address Drivers, Logic Diagram (Sheet 1 of 4)

A6AMA1A1



TERMINAL AREA - E 1			
PIN	SIGNAL	PIN	SIGNAL
1	MmLEX7	23	
2	MmLIX7	24	MmEDI3
3	MmEDI7	25	MmSOI3
4	MmLEX6	26	
5	MmLIX 6	27	MmSOE3
6	MmLEX5	28	
7	MmLIX5	29	MmSOI2
8	MmLEX4	30	
9	MmLIX4	31	MmSOE2
10	MmEDI6	32	MmEDI2
11	MmSOI7	33	MmSOI1
12	MmSOE7	34	MmSOE1
13	MmSOI6	35	MmEDI1
14	MmSOE6	36	MmSOI0
15	MmEDI5	37	MmSOE0
16	MmSOI5	38	MmEDI0
17	MmSOE5		
18	MmSOI4		
19	MmSOE4		
20	MmEDI4		
21			
22	MmEDEX		

TERMINAL AREA - E 2			
PIN	SIGNAL	PIN	SIGNAL
1	MmTCV	23	PWR RET
2		24	AnAX2VN
3	AnM20	25	AnAX00VN
4	AnAX70VN	26	AnAX0VN
5	AnAX7VN	27	AnAX20VN
6	AnAX50VN	28	AnAX1VN
7	AnAX5VN	29	AnAX40VN
8	AnAX30VN	30	AnAX3VN
9	AnAX4VN	31	AnAX60VN
10	AnAX10VN	32	AnM20
11	AnAX6VN	33	
12	SIG RET	34	MmTCV
13	SIG RET	35	
14	AnSYL0VN	36	
15	V1		
16	EDmX		
17	V3		
18	V3		
19	EDmX		
20	V1		
21	AnSYL1VN		
22	PWR RET		

X TERMINAL AREA - E 3			
PIN	SIGNAL	PIN	SIGNAL
1	MmRDP2	23	
2	MmRDP3	24	MmS1E4
3	MmSTRP3	25	
4	MmSTRP1	26	MmS1I3
5		27	MmS1E3
6	MmTCV	28	MmS1I2
7	MmTCV	29	MmS1E2
8	MmCRX	30	MmS1I1
9	MmCRX	31	MmS1E1
10	MmS1I7	32	MmS1I0
11	MmS1E7	33	MmS1E0
12		34	MmLIX3
13	MmS1I6	35	MmLEX3
14		36	MmLIX2
15	MmS1E6	37	MmLEX2
16		38	MmLIX1
17	MmS1I5	39	MmLEX1
18		40	MmLIX0
19	MmS1IE5	41	MmLEX0
20		42	
21		43	
22	MmS1I4	44	

Figure 10-40. Memory Hi-X Address Drivers, Logic Diagram (Sheet 2)

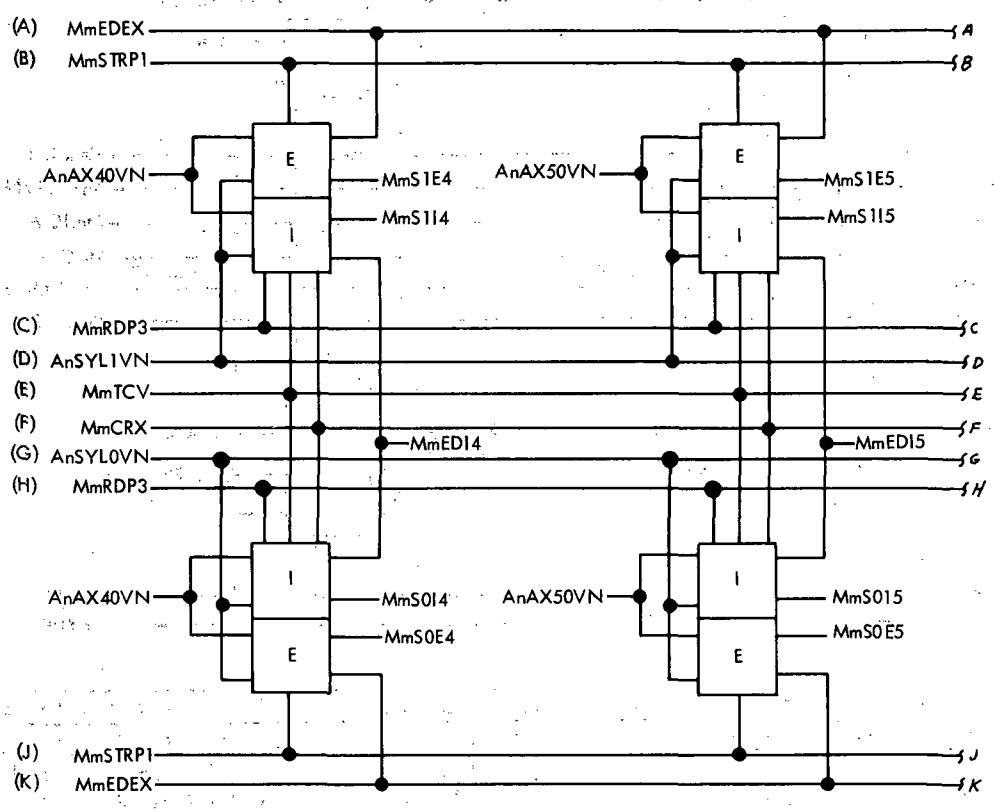
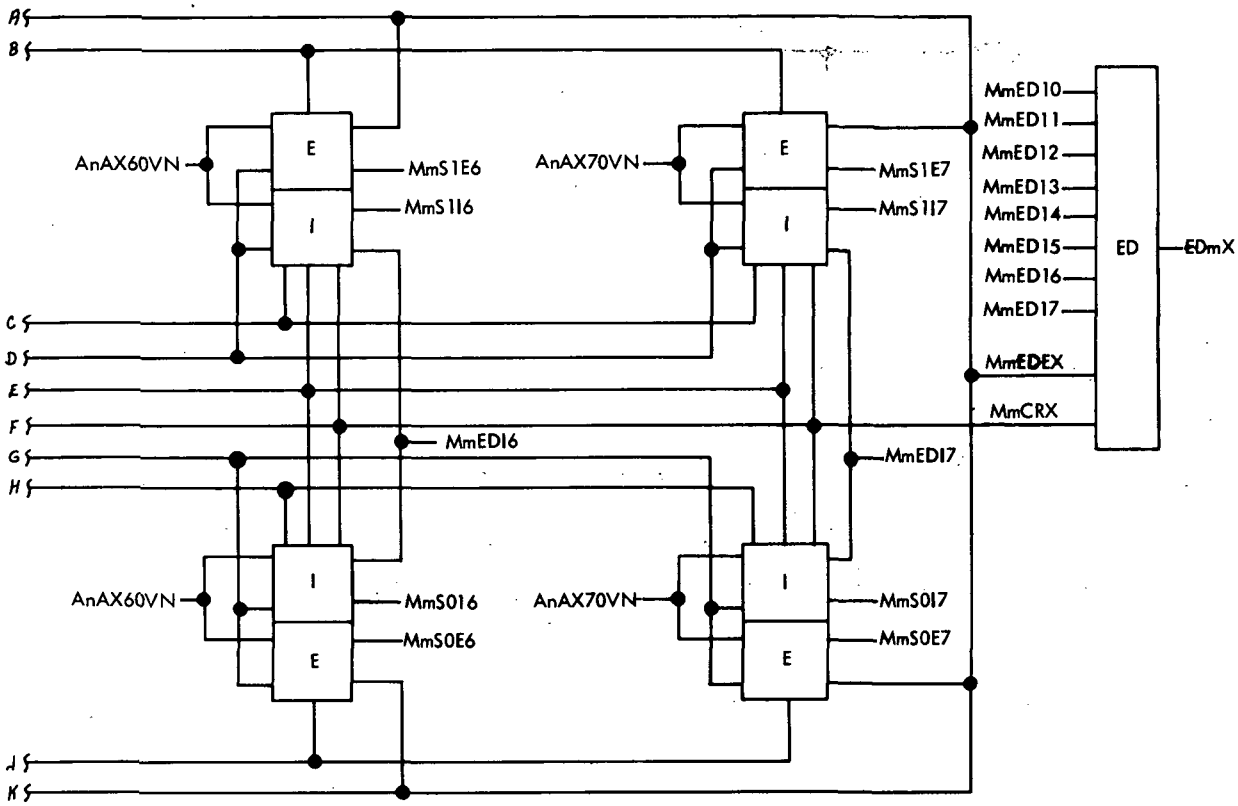


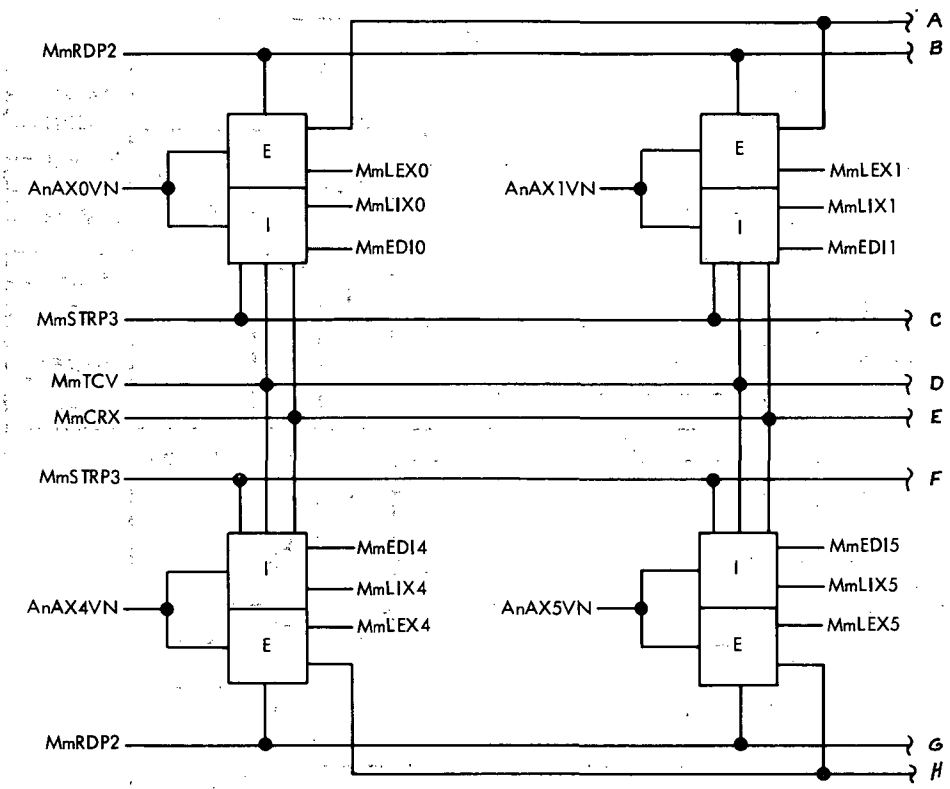
Figure 10-40. Memory Hi-X Address Drivers, Logic Diagram (Sheet 3)



NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate it
5. Prefix Reference Designations as Follows: A6AMA1A1 where M = Memory Module Assembly Number 1 through 4
6. m Represents the Memory Module Number 0 through 3
7. n is a 1 if m is an Even Number, and a 2 if m is an Odd Number

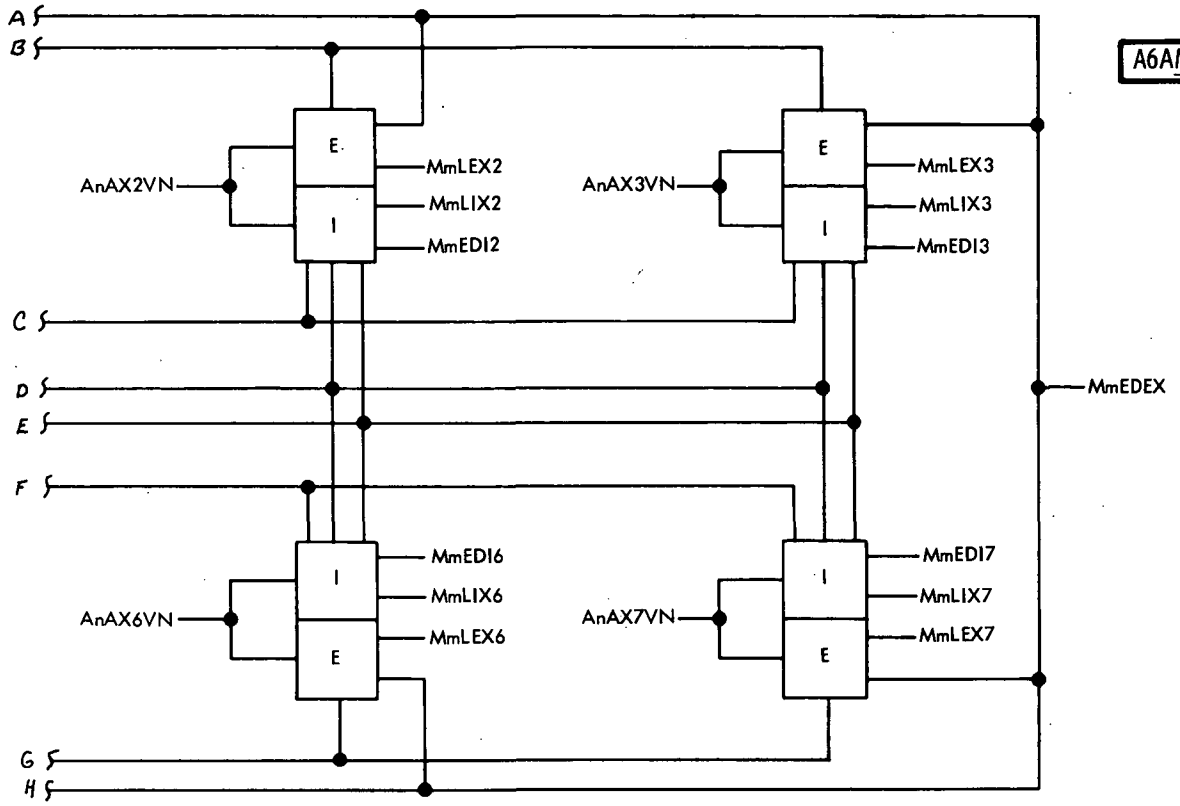
Figure 10-40. Memory Hi-X Address Drivers, Logic Diagram (Sheet 4)



NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate it
5. Prefix Reference Designations as Follows: A6AMA1A2, where M = Memory Module Assembly Number 1 through 4
6. m Represents the Memory Module Number 0 through 3
7. n is a 1 if m is an Even Number, and a 2 if m is an Odd Number

Figure 10-41. Memory Lo-X Address Drivers, Logic Diagram (Sheet 1 of 2)



TERMINAL AREA - E 1			
PIN	SIGNAL	PIN	SIGNAL
1	MmEDI0	20	MmSOE4
2	MmSOE0	21	MmSOI4
3	MmSOI0	22	MmSOE5
4	MmEDI1	23	MmSOI5
5	MmSOE1	24	MmEDI5
6	MmSOI1	25	MmSOE6
7	MmEDI2	26	MmSOI6
8	MmSOE2	27	MmSOE7
9		28	MmSOI7
10	MmSOI2	29	MmEDI6
11		30	MmLIX4
12	MmSOE3	31	MmLEX4
13		32	MmLIX5
14	MmSOI3	33	MmLEX5
15	MmEDI3	34	MmLIX6
16		35	MmLEX6
17	MmEDEX	36	MmEDI7
18		37	MmLIX7
19	MmEDI4	38	MmLEX7

TERMINAL AREA - E 3			
PIN	SIGNAL	PIN	SIGNAL
1		23	
2		24	
3	MmLEX0	25	MmS1E5
4	MmLIX0	26	
5	MmLEX1	27	MmS1I5
6	MmLIX1	28	
7	MmLEX2	29	MmS1E6
8	MmLIX2	30	
9	MmLEX3	31	MmS1I6
10	MmLIX3	32	
11	MmS1E0	33	MmS1E7
12	MmS1I0	34	MmS1I7
13	MmS1E1	35	MmCRX
14	MmS1I1	36	MmCRX
15	MmS1E2	37	MmTCV
16	MmS1I2	38	MmTCV
17	MmS1E3	39	
18	MmS1I3	40	MmSTRP1
19		41	MmSTRP3
20	MmS1E4	42	MmRDP3
21		43	MmRDP2
22	MmS1I4		

TERMINAL AREA - E 4			
PIN	SIGNAL	PIN	SIGNAL
1	MmTCV	19	EDmX
2		20	V1
3	AnM20	21	AnSYL1VN
4	AnAX70VN	22	PWR RET
5	AnAX7VN	23	PWR RET
6	AnAX50VN	24	AnAX2VN
7	AnAX5VN	25	AnAX00VN
8	AnAX30VN	26	AnAX0VN
9	AnAX4VN	27	AnAX20VN
10	AnAX10VN	28	AnAX1VN
11	AnAX6VN	29	AnAX40VN
12	SIG RET	30	AnAX3VN
13	SIG RET	31	AnAX60VN
14	AnSYL0VN	32	AnM20
15	V1	33	
16	EDmX	34	MmTCV
17	V3	35	
18	V3	36	

Figure 10-41. Memory Lo-X Address Drivers, Logic Diagram (Sheet 2)

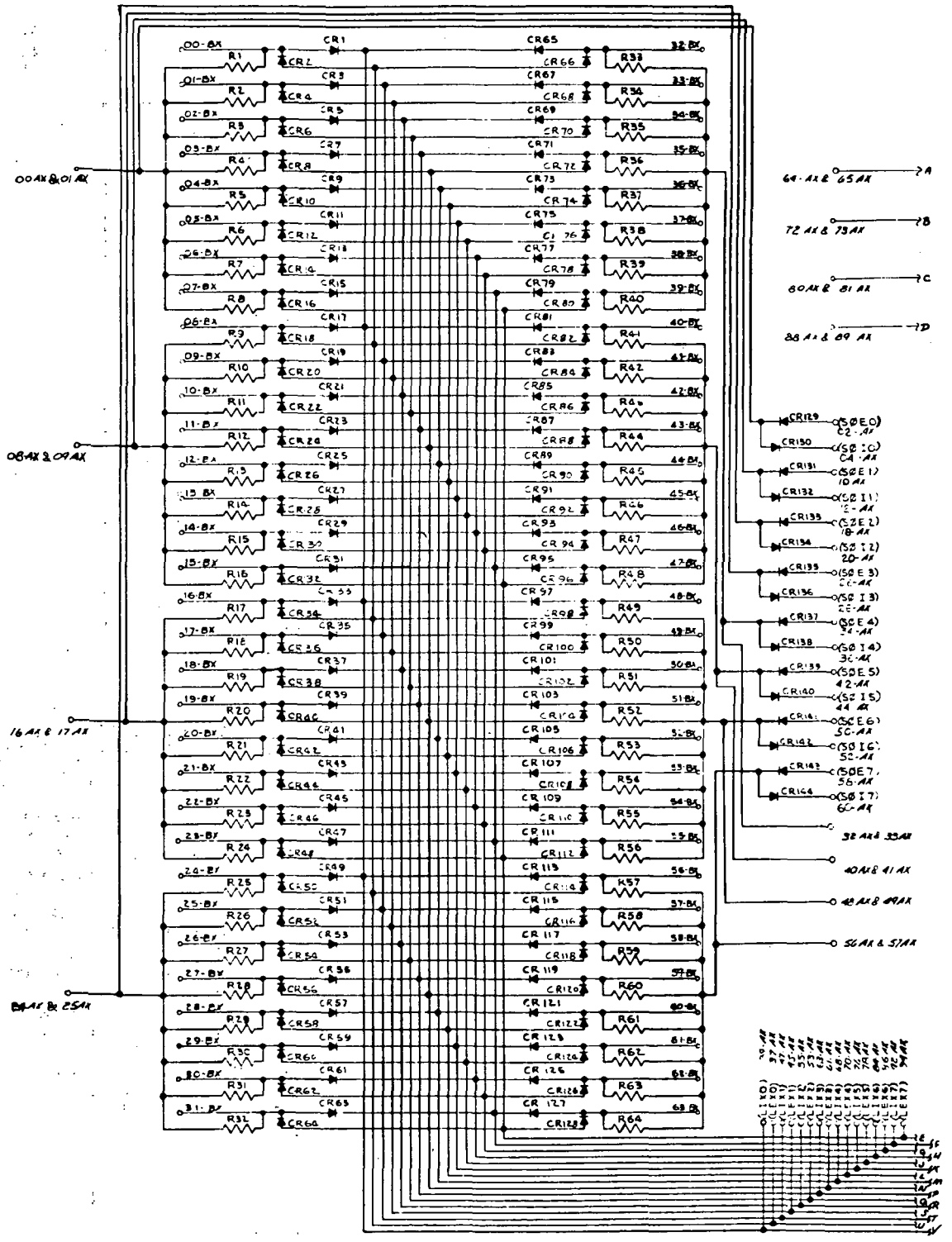


Figure 10-42. X Memory Address Diode Matrix, Schematic Diagram (Sheet 1 of 2)

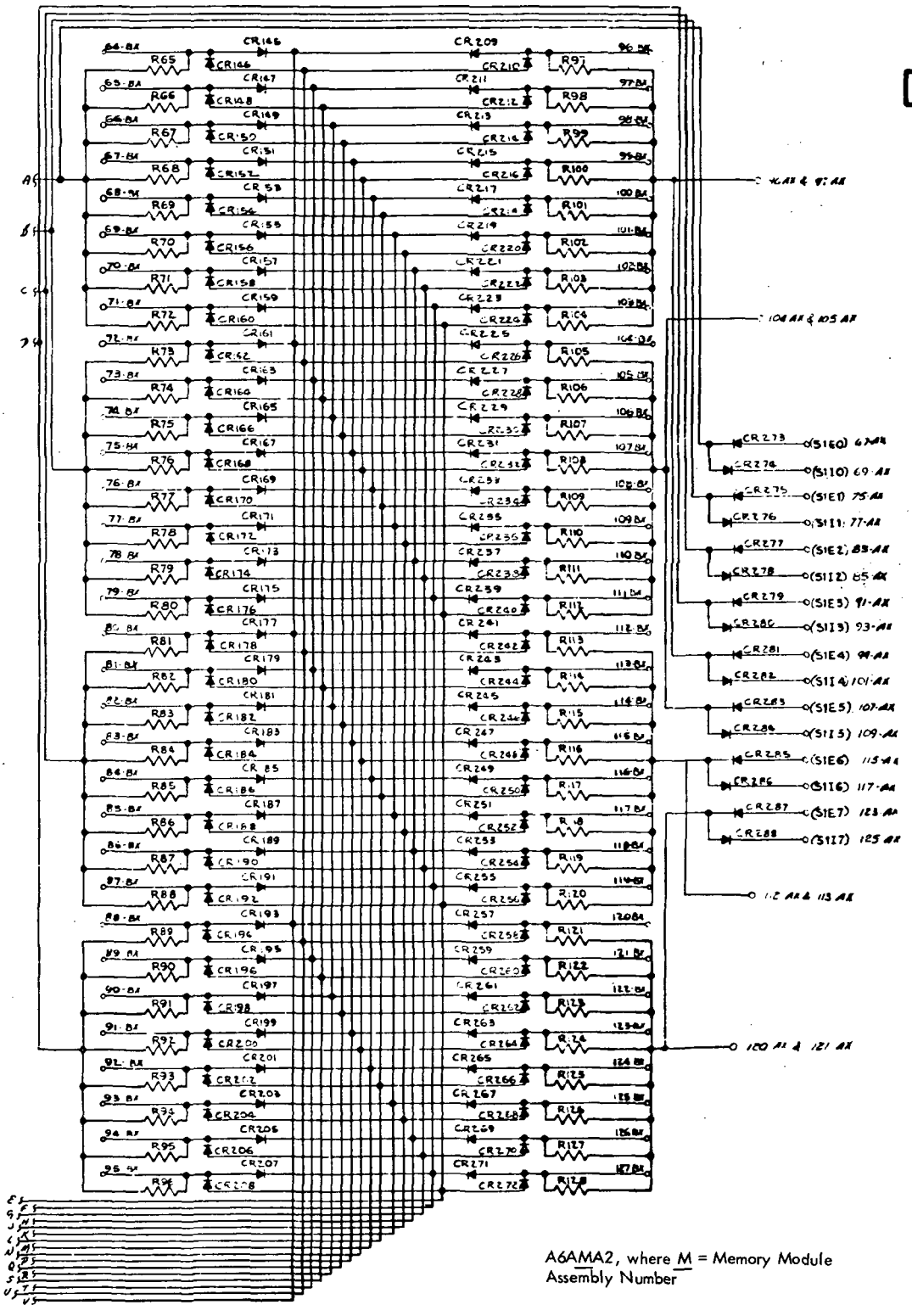


Figure 10-42. X Memory Address Diode Matrix, Schematic Diagram (Sheet 2)

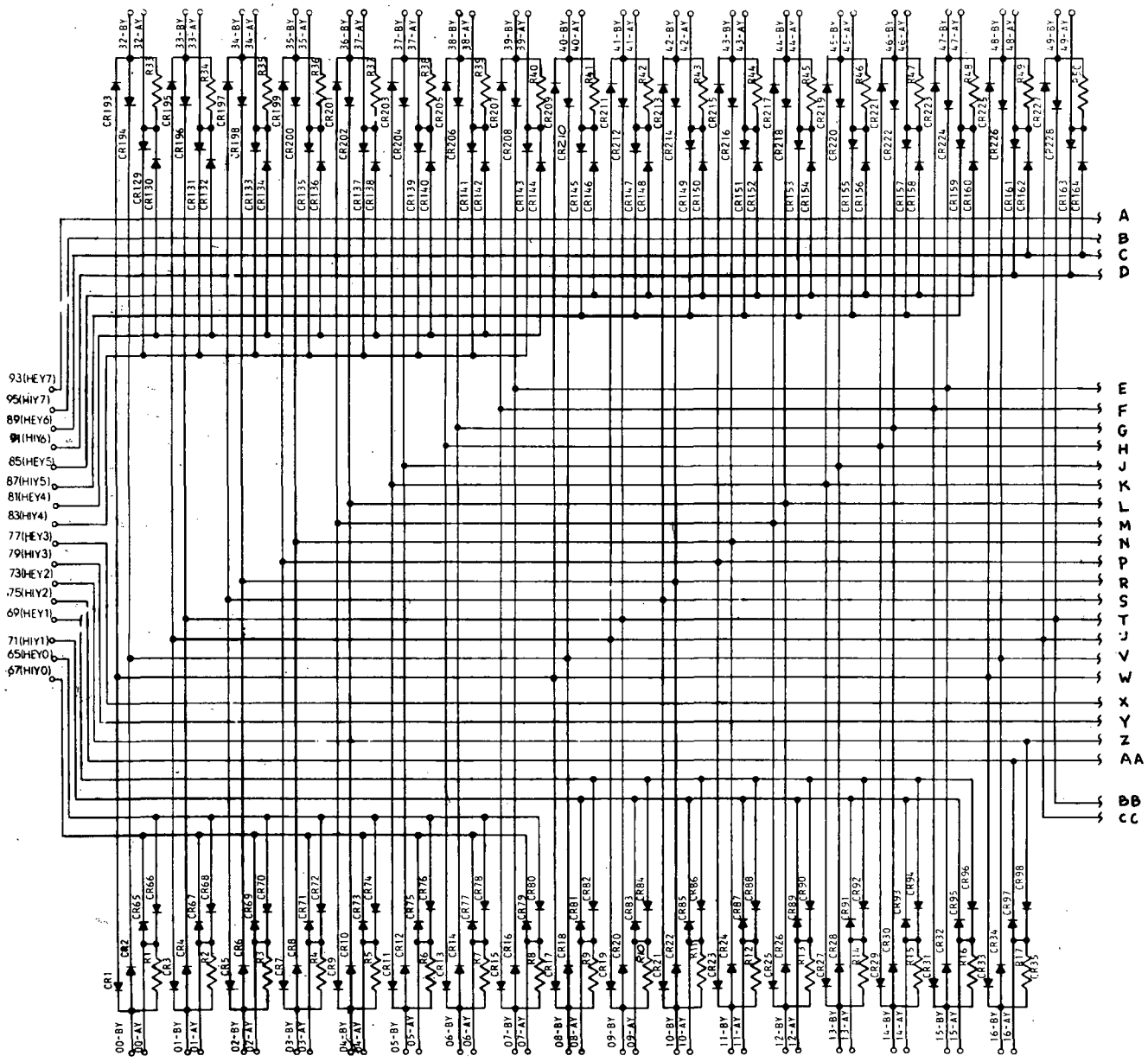
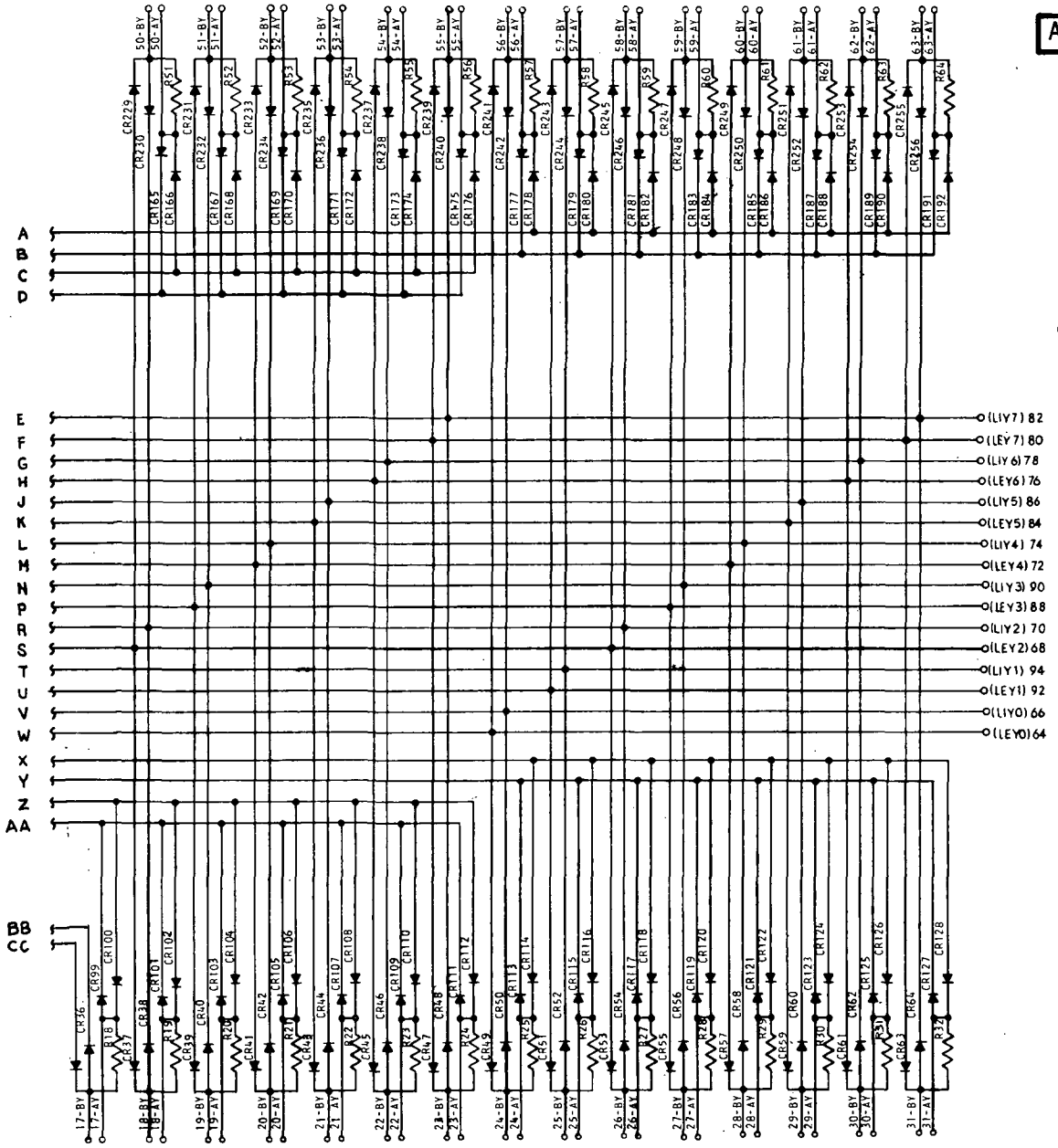


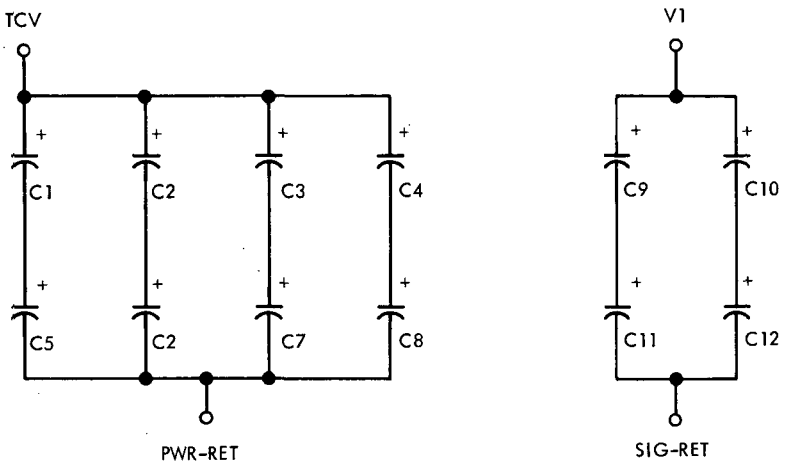
Figure 10-43. Y Memory Address Diode Matrix, Schematic Diagram (Sheet 1 of 2)



NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition of Logic Symbols
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate It
5. Prefix Reference Designations as Follows: A6AMA4, where M = Memory Module Assembly Number

Figure 10-43. Y Memory Address Diode Matrix, Schematic Diagram (Sheet 2)

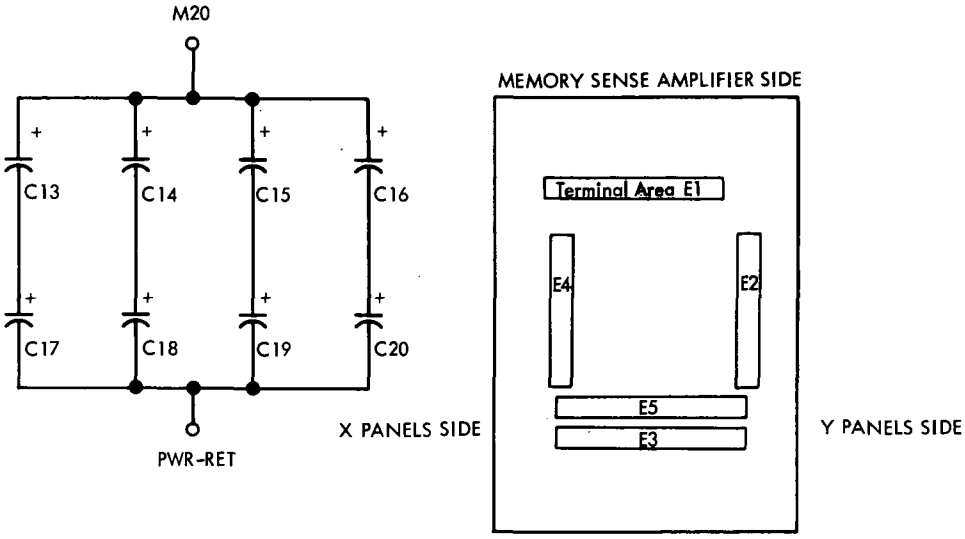


TERMINAL AREA E1			
Pin	Signal	Pin	Signal
1			
2			
3	MmSA14		
4	MmSA13		
5	MmSA12		
6	MmSA11		
7	MmSA10		
8	MmSA9		
9	V3		
10	MmSA7		
11			
12	V1		
13	V5		
14	SIG RET		
15	SIG RET		
16	V5		
17	V1		
18			
19	MmSA8		
20	V3		
21	MmSA6		
22	MmSA5		
23	MmSA4		
24	MmSA3		
25	MmSA2		
26	MmSA1		
27			
28			

TERMINAL AREA E2			
Pin	Signal	Pin	Signal
1	MmTCV		
2			
3	AnM20		
4	AnAY7VN		
5	AnAY5VN		
6	AnAY3VN		
7	AnAY0VN		
8	AnAY1VN		
9	AnAY2VN		
10	AnAY4VN		
11	AnAY6VN		
12	SIG RET		
13	SIG RET		
14			
15	V1		
16	EDmY		
17	V3		
18	V3		
19	EDmY		
20	V1		
21			
22	PWR RET		
23	PWR RET		
24	AnAY60VN		
25	AnAY40VN		
26	AnAY20VN		
27	AnAY10VN		
28	AnAY00VN		
29	AnAY30VN		
30	AnAY50VN		
31	AnAY70VN		
32	AnM20		
33			
34	MmTCV		

TERMINAL AREA E3			
Pin	Signal	Pin	Signal
1	AnAX60VN	28	BRB9
2	AnAX3VN	29	BRA8
3	AnMCL	30	BRB8
4	AnMCN	31	BRA10
5	AnINHSV	32	BRB14
6	MmSYNCV	33	BRA14
7	SIG RET	34	BRB12
8	SIG RET	35	BRA12
9	AnRDMVN	36	BRB10
10	V3	37	BRB2
11	V3	38	BRA2
12	AnRDMV	39	BRB4
13	AnM20ID	40	BRA4
14	AnM20ID	41	BRB6
15	AnM20	42	BRA6
16	V1	43	BRB7
17	V1	44	BRA7
18	V5	45	BRB5
19	V5	46	BRA5
20	PWR RET	47	BRB3
21	PWR RET	48	BRA3
22	PWR RET	49	BRB1
23	BRA13	50	BRA1
24	BRB13	51	α
25	BRA11	52	β
26	BRB11	53	AnAY50VN
27	BRA9	54	AnAY70VN

Figure 10-44. Memory Input-Output Panel, Schematic Diagram (Sheet 1 of 2)



TERMINAL AREA E4			
Pin	Signal	Pin	Signal
1	MmTCV	18	V3
2		19	EDmX
3	AnM20	20	V1
4	AnAX70VN	21	AnSYL1VN
5	AnAX7VN	22	PWR RET
6	AnAX50VN	23	PWR RET
7	AnAX5VN	24	AnAX2VN
8	AnAX30VN	25	AnAX00VN
9	AnAX4VN	26	AnAX0VN
10	AnAX10VN	27	AnAX20VN
11	AnAX6VN	28	AnAX1VN
12	SIG RET	29	AnAX40VN
13	SIG RET	30	AnAX3VN
14	AnSYLOVN	31	AnAX60VN
15	V1	32	AnM20
16	EDmX	33	
17	V3	34	MmTCV

TERMINAL AREA E5			
Pin	Signal	Pin	Signal
1	AnSYL1VN	26	AnAY5VN
2	MmSA13	27	AnAY1VN
3	AnSYL0VN	28	AnAY00VN
4	MmSA11	29	AnAX00VN
5	MmSA2	30	AnAX30VN
6	AnAX40VN	31	AnAX70VN
7	MmSA1	32	AnAY10VN
8	AnAX4VN	33	AnAX1VN
9	MmSA4	34	AnAY0VN
10	AnAX2VN	35	AnAX50VN
11	MmSA8	36	EDmX
12	AnAX20VN	37	AnM20
13	MmSA5	38	MmTCV
14	MmSA3	39	EDmY
15	MmSA7	40	AnAY20VN
16	AnAX7VN	41	AnAY7VN
17	MmSA10	42	AnAY2VN
18	AnAX10VN	43	AnAX6VN
19	MmSA14	44	AnAY4VN
20	AnAX0VN	45	AnAY40VN
21	MmSA6	46	AnAY60VN
22	AnAX30VN	47	AnAX5VN
23	MmSA12	48	AnAY3VN
24	MmSA9	49	AmM20
25	AnAY6VN		

NOTES:

1. See Glossary or Index for Signal Definitions
2. See Logic Symbols Appendix for Definition
3. Dotted Line (if any) Indicates Internal ULD Connection
4. "N.U." Indicates that ULD is Not Installed although Page is "Wired" to Accommodate it
5. Prefix Reference Designations as Follows: A6AMA8A1, where $\overline{M}$ = Memory Module Assembly Number 1 $\overline{\text{through}}$ 4
6. m Represents the Memory Module Number 0 through 3
7. n is a 1 if m is an Even Number, and a 2 if m is an Odd Number

	FOR MEMORY MODULE 0,2,4 & 6	FOR MEMORY MODULE 1,3,5, & 7
β	A1BRA0VN	A1BRB0V
α	A1BRA0V	A1BRB0VN

Figure 10-44. Memory Input-Output Panel, Schematic Diagram (Sheet 2)

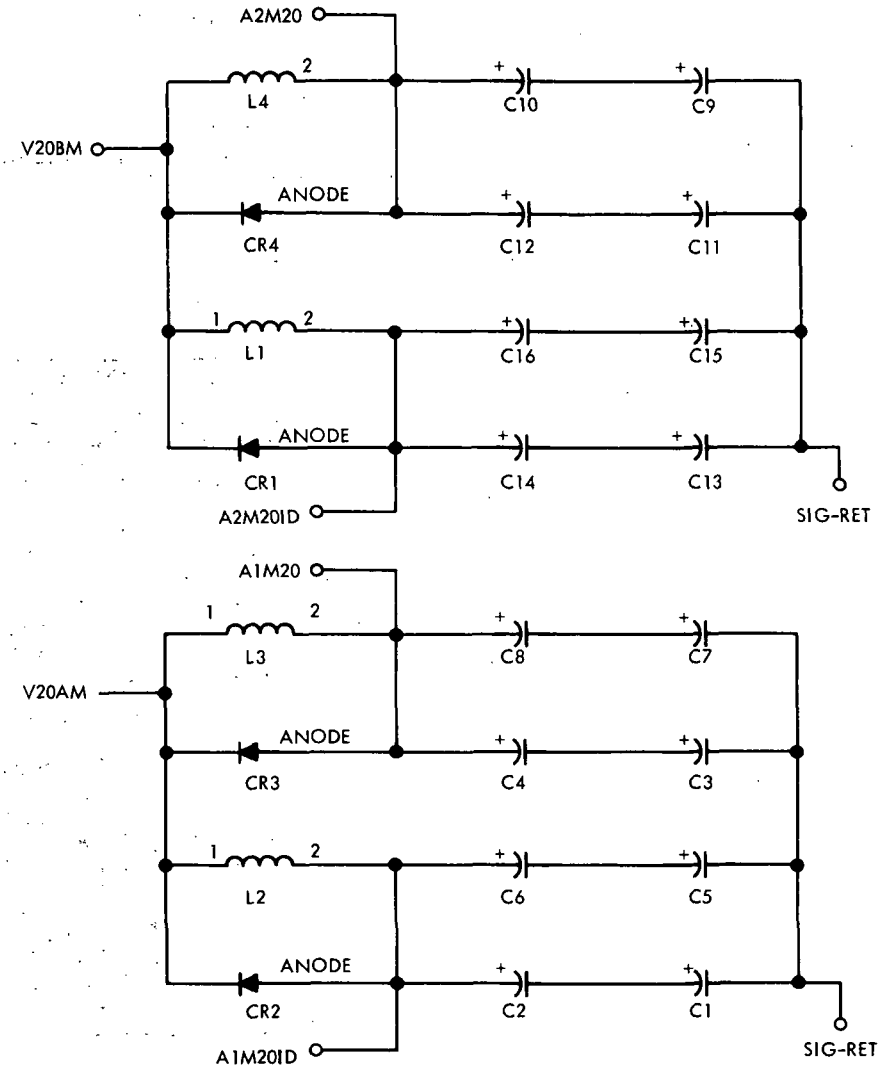


Figure 10-45. Memory Distribution Panel, Schematic Diagram (Sheet 1 of 4)

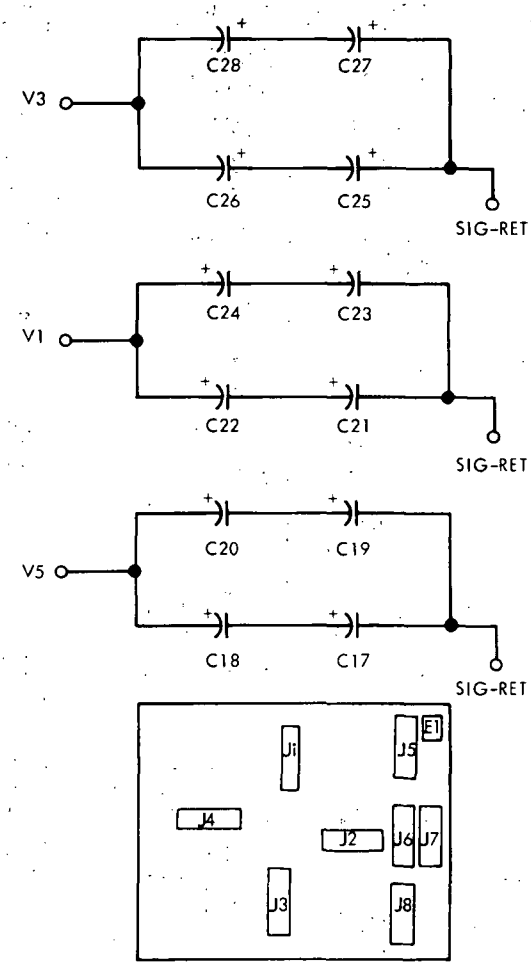


Figure 10-45. Memory Distribution Panel, Schematic Diagram (Sheet 2)

TERMINAL AREA J3			
PIN	SIGNAL	PIN	SIGNAL
1	A2SYL1VN	50	BRB8
2	A2AX60VN	51	A2AY5VN
3	M1SA13	52	BRA10
4	A2AX3VN	53	A2AY1VN
5	A2SYL0VN	54	BRB14
6	A2MCL	55	A2AY00VN
7	M1SA11	56	BRA14
8	A2MCN	57	A2AX00VN
9	M1SA2	58	BRB12
10	A2INH5V	59	A2AY30VN
11	A2AX40VN	60	BRA12
12	M1SYNCV	61	A2AX70VN
13	M1SA1	62	BRB10
14	SIG RET	63	A2AY10VN
15	A2AX4VN	64	BRB2
16	SIG RET	65	A2AX1VN
17	M1SA4	66	BRA2
18	A2RDMVN	67	A2AY0VN
19	A2AX2VN	68	BRB4
20	V3	69	A2AX50VN
21	M1SA8	70	BRA4
22	A2RDMV	71	ED1X
23	A2AX20VN	72	BRB6
24	A2M20ID	73	A2M20
25	M1SA5	74	BRA6
26	A2M20ID	75	M1TCV
27	M1SA3	76	BRB7
28	V1	77	ED1Y
29	M1SA7	78	BRA7
30	V5	79	A2AY20VN
31	A2AX7VN	80	BRB5
32	PWR-RET	81	A2AY7VN
33	M1SA10	82	BRA5
34	PWR-RET	83	A2AY2VN
35	A2AX10VN	84	BRB3
36	BRA13	85	A2AX6VN
37	M1SA14	86	BRA3
38	BRB13	87	A2AY4VN
39	A2AX0VN	88	BRB1
40	BRA11	89	A2AY40VN
41	M1SA6	90	BRA1
42	BRB11	91	A2AY60VN
43	A2AX30VN	92	A1BR80VN(α)
44	BRA9	93	A2AX5VN
45	M1SA12	94	A1BR80V(β)
46	BRB9	95	A2AY3VN
47	M1SA9	96	A2AY50VN
48	BRA8	97	A2M20
49	A2AY6VN	98	A2AY70VN

TERMINAL AREA J4			
PIN	SIGNAL	PIN	SIGNAL
1	A2SYL1VN	50	BRB8
2	A2AX60VN	51	A2AY5VN
3	M3SA13	52	BRA10
4	A2AX3VN	53	A2AY1VN
5	A2SYL0VN	54	BRB14
6	A2MCL	55	A2AY00VN
7	M3SA11	56	BRA14
8	A2MCN	57	A2AX00VN
9	M3SA2	58	BRB12
10	A2INH5V	59	A2AY30VN
11	A2AX40VN	60	BRA12
12	M3SYNCV	61	A2AX70VN
13	M3SA1	62	BRB10
14	SIG RET	63	A2AY10VN
15	A2AX4VN	64	BRB2
16	SIG RET	65	A2AX1VN
17	M3SA4	66	BRA2
18	A2RDMVN	67	A2AY0VN
19	A2AX2VN	68	BRB4
20	V3	69	A2AX50VN
21	M3SA8	70	BRA4
22	A2RDMV	71	ED3X
23	A2AX20VN	72	BRB6
24	A2M20ID	73	A2M20
25	M3SA5	74	BRA6
26	A2M20ID	75	M3TCV
27	M3SA3	76	BRB7
28	V1	77	ED3Y
29	M3SA7	78	BRA7
30	V5	79	A2AY20VN
31	A2AX7VN	80	BRB5
32	PWR-RET	81	A2AY7VN
33	M3SA10	82	BRA5
34	PWR-RET	83	A2AY2VN
35	A2AX10VN	84	BRB3
36	BRA13	85	A2AX6VN
37	M3SA14	86	BRA3
38	BRB13	87	A2AY4VN
39	A2AX0VN	88	BRB1
40	BRA11	89	A2AY40VN
41	M3SA6	90	BRA1
42	BRB11	91	A2AY60VN
43	A2AX30VN	92	A1BR80VN(α)
44	BRA9	93	A2AX5VN
45	M3SA12	94	A1BR80V(β)
46	BRB9	95	A2AY3VN
47	M3SA9	96	A2AY50VN
48	BRA8	97	A2M20
49	A2AY6VN	98	A2AY70VN

TERMINAL AREA J8			
PIN	SIGNAL	PIN	SIGNAL
1		50	
2		51	M3SA
3		52	
4		53	
5	BRB9	54	M3SA2
6		55	
7	M1SA8	56	
8	M2SA12	57	
9	BRB7	58	
10	M1SA14	59	
11	M3SA14	60	BRA14
12		61	
13		62	
14		63	
15	M3SA7	64	M3SA11
16	M1SA9	65	
17	M3SA8	66	
18	M1SA6	67	
19	M0SA12	68	M1SA4
20	M3SA6	69	
21	BRB10	70	M2SA9
22		71	
23		72	M3SA13
24		73	
25	BRB3	74	M1SA11
26	M1SA3	75	M0SA6
27		76	
28		77	
29	BRB5	78	M2SA6
30	M3SA9	79	
31	M1SA5	80	M1SA12
32		81	
33		82	M0SA9
34		83	BRB11
35		84	
36		85	
37		86	
38	BRA12	87	BRB13
39		88	M0SA14
40	BRB8	89	A2MCN
41		90	M3SA12
42		91	BRB1
43		92	M2SA14
44	BRB14	93	BRB12
45		94	
46		95	BRA9
47		96	M3SA4
48	BRB4	97	BRB2
49		98	BRA6

TERMINAL AREA J6									
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1		21		41		61		81	
2	V20BM	22	SIG-RET	42	SIG-RET	62	SIG-RET	82	
3		23		43		63		83	
4	V20BM	24	SIG-RET	44	V1	64	SIG-RET	84	V20AM
5		25		45		65		85	
6	V20BM	26	V3	46	V1	66	SIG-RET	86	V20AM
7		27		47		67		87	
8	V20BM	28	V3	48	V1	68	V5	88	V20AM
9		29		49		69		89	
10	V20BM	30	V3	50	SIG-RET	70	V5	90	V20AM
11		31		51		71		91	
12	V20BM	32	V3	52	V1	72	V5	92	V20AM
13		33		53		73		93	
14	V20BM	34	SIG-RET	54	V1	74	V5	94	V20AM
15		35		55		75		95	
16	V20BM	36	SIG-RET	56	V1	76	SIG-RET	96	V20AM
17		37		57		77		97	
18	SIG-RET	38	SIG-RET	58	SIG-RET	78	SIG-RET	98	V20AM
19		39		59		79			
20	SIG-RET	40	SIG-RET	60	SIG-RET	80	SIG-RET		

TERMINAL AREA E1	
PIN	SIGNAL
1	THERM 4
2	THERM 3

NOTE:
1. THE SIGNAL RETURN AND PWR RETURN PLANES ARE COMMONED AT ALL POSITIONS (WHEREVER POSSIBLE) THAT CONTAIN EITHER SIGNAL.
2. IBM ABBREVIATION AND LETTER SYMBOL SPECIFICATION 6109008 APPLIES.

Figure 10-45. Memory Distribution Panel, Schematic Diagram (Sheet 3)

TERMINAL AREA J1			
PIN	SIGNAL	PIN	SIGNAL
1	A1SYL1VN	50	BRB8
2	A1AX60VN	51	A1AY5VN
3	M2SA13	52	BRA10
4	A1AX3VN	53	A1AY1VN
5	A1SYL0VN	54	BRB14
6	A1MCL	55	A1AY00VN
7	M2SA11	56	BRA14
8	A1MCN	57	A1AX00VN
9	M2SA2	58	BRB12
10	A1INHSV	59	A1AY30VN
11	A1AX40VN	60	BRA12
12	M2SYNCV	61	A1AX70VN
13	M2SA1	62	BRB10
14	SIG-RET	63	A1AY10VN
15	A1AX4VN	64	BRB2
16	SIG-RET	65	A1AX1VN
17	M2SA4	66	BRA2
18	A1RDMVN	67	A1AY0VN
19	A1AX2VN	68	BRB4
20	V3	69	A1AX50VN
21	M2SA8	70	BRA4
22	A1RDMV	71	ED2X
23	A1AX20VN	72	BRB6
24	A1M20ID	73	A1M20
25	M2SA5	74	BRA6
26	A1M20ID	75	M2TCV
27	M2SA3	76	BRB7
28	V1	77	ED2Y
29	M2SA7	78	BRA7
30	V5	79	A1AY20VN
31	A1AX7VN	80	BRB5
32	PWR-RET	81	A1AY7VN
33	M2SA10	82	BRA5
34	PWR-RET	83	A1AY2VN
35	A1AX10VN	84	BRB3
36	BRA13	85	A1AX6VN
37	M2SA14	86	BRA3
38	BRB13	87	A1AY4VN
39	A1AX0VN	88	BRB1
40	BRA11	89	A1AY40VN
41	M2SA6	90	BRA1
42	BRB11	91	A1AY60VN
43	A1AX30VN	92	A1BRA0V(α)
44	BRA9	93	A1AX5VN
45	M2SA12	94	A1BRA0VN(β)
46	BRB9	95	A1AY3VN
47	M2SA9	96	A1AY50VN
48	BRA8	97	A1M20
49	A1AY6VN	98	A1AY70VN

TERMINAL AREA J5			
PIN	SIGNAL	PIN	SIGNAL
1	A1SYL1VN	50	
2	A2AX3VN	51	
3	A1SYL0VN	52	A2AX00VN
4	A2AX60VN	53	
5	A2SYL1VN	54	
6	A1AX3VN	55	
7		56	A1AX30VN
8	A1AX60VN	57	
9	A2SYL0VN	58	A1AX00VN
10		59	
11		60	A2AX70VN
12	A2AX40VN	61	A2INHSV
13		62	A1AX70VN
14	A2AX4VN	63	M2SYNCV
15		64	A2AX1VN
16	A1AX40VN	65	A2RDMV
17		66	A1AX1VN
18	BRB6	67	A1RDMV
19	ED0X	68	A2AX50VN
20	A2MCL	69	M0SYNCV
21		70	M3SYNCV
22	A1AX4VN	71	M1SYNCV
23	ED0Y	72	
24	A1AX2VN	73	A1INHSV
25		74	
26	A2AX2VN	75	ED3Y
27	ED1X	76	A1AX50VN
28	A2AX20VN	77	
29		78	
30	A2AX10VN	79	A1BRA0VN(β)
31	ED1Y	80	
32	A1AX20VN	81	A2RDMVN
33		82	A2AX6VN
34	A1AX7VN	83	A1BRB0VN(α)
35	ED2X	84	A2AX5VN
36	A1AX10VN	85	A1RDMVN
37		86	A1AX5VN
38	BRA3	87	
39	ED2Y	88	A1MCN
40	A2AX7VN	89	
41		90	THERM3
42	BRA5	91	A1BRA0V(α)
43	ED3X	92	A1AX6VN
44	A1AX0VN	93	A1BRB0V(β)
45		94	THERM4
46	A2AX30VN	95	
47	A1MCL	96	
48	A2AX0VN	97	
49		98	

TERMINAL AREA J2			
PIN	SIGNAL	PIN	SIGNAL
1	A1SYL1VN	50	BRB8
2	A1AX60VN	51	A1AY5VN
3	M0SA13	52	BRA10
4	A1AX3VN	53	A1AY1VN
5	A1SYL0VN	54	BRB14
6	A1MCL	55	A1AY00VN
7	M0SA11	56	BRA14
8	A1MCN	57	A1AX00VN
9	M0SA2	58	BRB12
10	A1INHSV	59	A1AY30VN
11	A1AX40VN	60	BRA12
12	M0SYNCV	61	A1AX70VN
13	M0SA1	62	BRB10
14	SIG-RET	63	A1AY10VN
15	A1AX4VN	64	BRB2
16	SIG-RET	65	A1AX1VN
17	M0SA4	66	BRA2
18	A1RDMVN	67	A1AY0VN
19	A1AX2VN	68	BRB4
20	V3	69	A1AX50VN
21	M0SA8	70	BRA4
22	A1RDMV	71	ED0X
23	A1AX20VN	72	BRB6
24	A1M20ID	73	A1M20
25	M0SA5	74	BRA6
26	A1M20ID	75	M0TCV
27	M0SA3	76	BRB7
28	V1	77	ED0Y
29	M0SA7	78	BRA7
30	V5	79	A1AY20VN
31	A1AX7VN	80	BRB5
32	PWR-RET	81	A1AY7VN
33	M0SA10	82	BRA5
34	PWR-RET	83	A1AY2VN
35	A1AX10VN	84	BRB3
36	BRA13	85	A1AX6VN
37	M0SA14	86	BRA3
38	BRB13	87	A1AY4VN
39	A1AX0VN	88	BRB1
40	BRA11	89	A1AY40VN
41	M0SA6	90	BRA1
42	BRB11	91	A1AY60VN
43	A1AX30VN	92	A1BRA0V(α)
44	BRA9	93	A1AX5VN
45	M0SA12	94	A1BRA0VN(β)
46	BRB9	95	A1AY3VN
47	M0SA9	96	A1AY50VN
48	BRA8	97	A1M20
49	A1AY6VN	98	A1AY70VN

TERMINAL AREA J7			
PIN	SIGNAL	PIN	SIGNAL
1		50	A1AY00VN
2		51	M1SA1
3		52	A1AY30VN
4		53	M1SA7
5		54	
6	BRA7	55	
7	BRA10	56	A2AY0VN
8		57	BRA4
9	M0SA8	58	A2AY30VN
10		59	M0SA13
11	M2SA10	60	A1AY10VN
12	A1AY6VN	61	
13		62	A1AY0VN
14	M0SA7	63	
15		64	A2AY7VN
16	A2AY5VN	65	M0SA2
17	M2SA7	66	A1AY7VN
18		67	
19	M2SA3	68	A2AY10VN
20	A1AY5VN	69	M0SA1
21		70	A1AY20VN
22	M2SA5	71	M2SA1
23		72	A2AY20VN
24	A1AY50VN	73	M2SA2
25	M3SA3	74	A2AY2VN
26	A2AY6VN	75	M2SA11
27	M3SA5	76	A1AY7VN
28		77	
29		78	A1AY4VN
30		79	
31	M0SA3	80	A1AY40VN
32	A2AY50VN	81	
33	M3SA10	82	A2AY4VN
34	A1AY1VN	83	M0SA4
35	M0SA5	84	A2AY40VN
36	A2AY1VN	85	
37	M2SA8	86	M2SA13
38	A1AY70VN	87	BRA11
39		88	M0SA11
40	A2AY70VN	89	
41		90	BRA13
42	BRA8	91	BRA1
43		92	A1AY60VN
44	M1SA10	93	
45	M1SA2	94	A2AY3VN
46	M0SA10	95	BRA2
47	M1SA13	96	A2AY60VN
48	A2AY00VN	97	M2SA4
49		98	A1AY3VN

Figure 10-45. Memory Distribution Panel, Schematic Diagram (Sheet 4)

SIGNAL	ORIGIN
A	A1A13-A
AB	
ABN	
ACC0	A1A5-A
ACC0N	
ACC1	A1A10-B
ACC1N	
ACC1V	A4A7-A
AI0	A1A5-A
AI0N	
AI1	A1A10-B
AI1N	
AI1V	A4A7-B
AI2	A1A10-B
AI2N	
AI2V	A4A7-B
AI2VN	
AI3	A1A10-B
AI3N	
AI3V	A4A7-B
AI3VN	
AI4	A1A10-B
AI4N	
AN	A1A13-A
AND	A1A10-A
ANDN	
AV	A4A9-A
AVN	
AX0N	A1A19-A
AX0VN	A5A7-A
AX1N	A1A19-A
AX1VN	A5A7-A
AX2N	A1A19-A
AX2VN	A5A7-A
AX3N	A1A19-A
AX3VN	A5A7-A
AX4N	A1A19-A
AX4VN	A5A7-A
AX5N	A1A19-A
AX5VN	A5A7-A
AX6N	A1A19-A
AX6VN	A5A7-A
AX7N	A1A19-A
AX7VN	A5A7-A
AX00N	A1A19-B
AX00VN	A5A7-B
AX10N	A1A19-B

SIGNAL	ORIGIN
AX10VN	A5A7-B
AX20N	A1A19-B
AX20VN	A5A7-B
AX30N	A1A19-B
AX30VN	A5A7-B
AX40N	A1A19-B
AX40VN	A5A7-B
AX50N	A1A19-B
AX50VN	A5A7-B
AX60N	A1A19-B
AX60VN	A5A7-B
AX70N	A1A19-B
AX70VN	A5A7-B
AY0N	A1A19-B
AY0VN	A5A8-A
AY1N	A1A19-B
AY1VN	A5A8-A
AY2N	A1A19-B
AY2VN	A5A8-A
AY3N	A1A19-B
AY3VN	A5A8-A
AY4N	A1A19-B
AY4VN	A5A8-A
AY5N	A1A19-B
AY5VN	A5A8-A
AY6N	A1A19-B
AY6VN	A5A8-A
AY7N	A1A19-B
AY7VN	A5A8-A
AY00N	A1A20-B
AY00VN	A5A8-B
AY10N	A1A20-B
AY10VN	A5A8-B
AY20N	A1A20-B
AY20VN	A5A8-B
AY30N	A1A20-B
AY30VN	A5A8-B
AY40N	A1A20-B
AY40VN	A5A8-B
AY50N	A1A20-B
AY50VN	A5A8-B
AY60N	A1A20-B
AY60VN	A5A8-B
AY70N	A1A20-B
AY70VN	A5A8-B
A1	A1A19-A
A1AN	

SIGNAL	ORIGIN
A1N	A1A19-A
A1V	A5A12-B
A2	A1A19-B
A2AN	
A2N	
A2V	A5A12-B
A3	A1A19-A
A3AN	
A3N	
A3V	A5A12-B
A4	A1A19-B
A4AN	
A4N	
A4V	A5A12-B
A5	A1A19-B
A5AN	
A5N	
A5V	A5A12-B
A6	A1A19-B
A6AN	
A6N	
A6V	A5A12-B
A7	A1A19-A
A7AN	
A7N	
A7V	A5A12-A
A8	A1A19-A
A8AN	
A8N	
A8V	A5A12-A
A9	A1A19-A
A9N	
A9PADN	A1A20-B
A9V	A5A12-A
B	A1A10-A
BD	A1A8-A
BDN	
BN	A1A10-A
BOT1	A4A11-A
BOT2	
BOT3	
BRA0	A1A16-A
BRA0N	
BRA0V	A5A6-A
BRA0VN	
BRA1	A5A9-A

Note: Origins of TMR signals are shown for channel 1 only.

Figure 10-46. Signal Origin List (Sheet 1 of 8)

SIGNAL	ORIGIN
BRA1N	A5A9-A
BRA2	
BRA2N	
BRA3	A5A9-B
BRA3N	
BRA4	A5A9-A
BRA4N	
BRA5	A5A9-B
BRA5N	
BRA6	A5A11-A
BRA6N	
BRA7	A5A9-A
BRA7N	
BRA8	A5A9-B
BRA8N	
BRA9	A5A11-A
BRA9N	
BRA10	A5A9-A
BRA10N	
BRA11	A5A9-B
BRA11N	
BRA12	A5A11-A
BRA12N	
BRA13	A5A9-B
BRA13N	
BRA14	A5A11-A
BRA14N	
BRA14P	
BRBO	A1A16-B
BRBON	
BRBOV	A5A5-A
BRBOVN	
BRB1	A5A10-A
BRB1N	
BRB2	
BRB2N	
BRB3	A5A10-B
BRB3N	
BRB4	A5A10-A
BRB4N	
BRB5	A5A10-B
BRB5N	
BRB6	A5A11-B
BRB6N	
BRB7	A5A10-A
BRB7N	
BRB8	A5A10-B

SIGNAL	ORIGIN
BRB8N	A5A10-B
BRB9	A5A11-B
BRB9N	
BRB10	A5A10-A
BRB10N	
BRB11	A5A10-B
BRB11N	
BRB12	A5A11-B
BRB12N	
BRB13	A5A10-B
BRB13N	
BRB14	A5A11-B
BRB14N	
BRB14P	
BO1	A4A11-B
BO1A	A4A12-B
BO1N	A4A11-B
BO1P	A4A12-B
BO2	A4A11-B
BO2A	A4A12-B
BO2N	A4A11-B
BO2P	A4A12-B
BO3	A4A11-B
BO3A	A4A12-B
BO3N	A4A11-B
BO3P	A4A12-B
C	A1A10-A
CBRN	A1A11-B
CBRVN	A5A13-A
CD	A1A8-A
CDN	
CDS	A1A11-A
CDSN	
CDSV	A5A15-A
CKP	A1A11-B
CKPN	
CLTR	A1A11-A
CLTRN	
CN	A1A10-A
CNC	A1A15-B
CNCN	
COC	
COCN	
CST	A1A15-A
CSTN	External
CSTV	A5A5-B

SIGNAL	ORIGIN
DATAV	External
DIN	
DLD31B	A1A5-A
DLD44B	
DL31	A1A7-A,
	A1A10-B
DL31SA	A1A5-A
DL44	A1A7-A,
	A1A10-B
DL44SA	A1A5-A
DMA	A1A16-A
DMAN	A1A14-A
DMAVN	A5A12-A
DMB	A1A16-B
DMBN	A1A14-A
DMBVN	A5A13-B
DM0	A1A14-A
DM1	
DM2	
DM2N	
DM3	
DM3N	
DSS	A1A20-A
DSSN	
DS1	
DS1M	
DS1MN	
DS1N	
DS2	
DS2M	
DS2MN	
DS2N	
DS3	A1A20-A
DS3N	
DS4	
DS4N	
DTM	A1A7-A
DTMN	
DTMV	A4A14-B
DTMVN	
DUPDN	A1A14-A
DUPIN	
EAC	A1A16-A
EADM	
EADMN	

Note: Origins of TMR signals are shown for channel 1 only.

Figure 10-46. Signal Origin List (Sheet 2)

SIGNAL	ORIGIN
EAIM	A1A16-A
EAIMN	
EAM	
EAMV	A5A6-A
EAP	A1A17-A
EAPN	A1A16-A
EBC	A1A16-B
EBDM	
EBDMN	
EBIM	
EBIMN	
EBM	
EBMV	A5A5-A
EBP	A1A17-B
EBPN	A1A16-B
EDAC	A1A16-A
EDACN	
EDBC	A1A16-B
EDBCN	
EDmX	A6AMA1A1
EDmY	A6AMA5A1
EIAC	A1A16-A
EIACN	
EIBC	A1A16-B
EIBCN	
EMDN	A1A8-A
ESD	A1A8-B
ESDN	
ESDV	A4A14-A
ESDVN	
EXM	A1A12-A
EXMD	A1A20-B
EXMDN	
EXMN	A1A12-A
EXMV	A4A6-B
EXMVN	
FCD	A1A12-A
FMDN	A1A8-A
FSA	A1A16-A
FSAN	
FSB	A1A16-B
FSBN	
G1	A1A13-A
G1N	

SIGNAL	ORIGIN
G1V	A4A7-A
G1VN	
G2	A1A13-A
G2N	
G2V	A4A13-A
G2VN	A4A7-A
G3	A1A13-A
G3N	
G3V	A4A13-A
G3VN	A4A6-A
G4	A1A13-A
G4N	
G4V	A4A8-B
G4VN	
G5	A1A13-A
G5N	
G5V	A4A8-A
G5VN	A4A13-A
G6	A1A13-A
G6N	
G6V	A4A6-A
G6VN	
G7	A1A13-A
G7N	
G7V	A4A9-A
G7VN	A4A6-A
HALTV	External
HOP	A1A12-A
HOPC1	A1A14-B
HOPC1N	
HOPC1V	A5A12-A
HOPN	A1A12-A
HOPV	A4A5-A
HOY	A1A7-A
HOYN	
HOYV	A4A13-B
HOYVN	
HP1	A1A14-B
HP1N	
IMA	A1A16-A
IMAN	A1A14-A
IMAVN	A5A12-A
IMB	A1A16-B
IMBN	A1A14-A

SIGNAL	ORIGIN
IMBVN	A5A13-B
IM0	A1A14-A
IM1	
IM2	
IM2N	
IM3	
IM3N	
INHBS	A1A15-A
INHBSV	A5A5-B
INT	A1A12-A
INTA	
INTAN	
INTB	
INTBN	
INTCV	External
INTN	A1A12-A
INTV	A4A6-B
ISS	A1A20-A
ISSN	
IS1	
IS1N	
IS2	
IS2N	
IS3	
IS3N	
IS4	
IS4N	
JBN	A1A12-B
K1	A1A7-B
K1N	
K2	
K2N	
MAO	A1A15-B
MAOV	A5A6-B
MBO	A1A15-B
MBOV	A5A6-B
MD0	A1A5-A
MD0N	
MD1	A1A7-B
MD1N	
MD2	
MD2N	
MD2V	A4A14-B

Note: Origins of TMR signals are shown for channel 1 only.

Figure 10-46. Signal Origin List (Sheet 3)

SIGNAL	ORIGIN
MD3	A1A7-B
MD3N	
MD4	
MD4N	
MD5	
MD5N	
MD6	
MD6N	
MD7	
MD7N	
MD7V	A4A14-B
MFF	A1A15-B
MFFN	A1A14-A
MFFVN	A5A13-B
MOP	A1A15-A
MR0	A1A5-A
MR0N	
MR1	A1A9-A
MR1N	
MR1V	A4A9-B
MR1VN	
MR2	A1A9-A
MR2N	
MSS	A1A15-A
MSSN	A1A14-A
MSSVN	A5A13-A
MSVB1	A1A4-A
	A4A3-A
	A5A3-A
MSVB2	A1A4-A
	A4A3-A
	A5A3-A
MTT	A1A15-A
MTTN	A1A14-A
MTTVN	A5A13-A
MZO	A1A15-A
MZON	A1A14-A
MZOVN	A5A13-A
MmCRX	A6AMA1A1
	A6AM̄A1A2
MmCRY	A6AM̄A5A1
MmEDEX	A6AM̄A1A2
MmEDEY	A6AM̄A5A1
MmEDIY0	A6AM̄A7A1
MmEDIY1	
MmEDIY2	
MmEDIY3	
MmEDIY4	

SIGNAL	ORIGIN
MmEDIY5	A6AMA7A1
MmEDIY6	
MmEDIY7	
MmEDI0	A6AMA1A1, 2
MmEDI1	
MmEDI2	
MmEDI3	
MmEDI4	
MmEDI5	
MmEDI6	
MmEDI7	
MmHEY0	A6AMA5A1
MmHEY1	
MmHEY2	
MmHEY3	
MmHEY4	
MmHEY5	
MmHEY6	
MmHEY7	
MmHIY0	
MmHIY1	
MmHIY2	
MmHIY3	
MmHIY4	
MmHIY5	
MmHIY6	
MmHIY7	
MmINH1	A6AMA7A1
MmINH2	
MmINH3	
MmINH4	
MmINH5	
MmINH6	
MmINH7	
MmINH8	
MmINH9	
MmINH10	
MmINH11	
MmINH12	
MmINH13	
MmINH14	
MmLEX0	A6AMA1A2
MmLEX1	
MmLEX2	
MmLEX3	
MmLEX4	
MmLEX5	
MmLEX6	

SIGNAL	ORIGIN
MmLEX7	A6AMA1A2
MmLEY0	A6AM̄A5A1
MmLEY1	
MmLEY2	
MmLEY3	
MmLEY4	
MmLEY5	
MmLEY6	
MmLEY7	
MmLIX0	A6AMA1A2
MmLIX1	
MmLIX2	
MmLIX3	
MmLIX4	
MmLIX5	
MmLIX6	
MmLIX7	
MmLIY0	A6AMA5A1
MmLIY1	
MmLIY2	
MmLIY3	
MmLIY4	
MmLIY5	
MmLIY6	
MmLIY7	
MmRDP1	A6AMA6A1
MmRDP2	
MmRDP3	
MmSA1	A6AMA3A1
MmSA2	A6AM̄A3A2
MmSA3	A6AM̄A3A1
MmSA4	A6AM̄A3A2
MmSA5	A6AM̄A3A1
MmSA6	A6AM̄A3A2
MmSA7	A6AM̄A3A1
MmSA8	A6AM̄A3A2
MmSA9	A6AM̄A3A1
MmSA10	A6AM̄A3A2
MmSA11	A6AM̄A3A1
MmSA12	A6AM̄A3A2
MmSA13	A6AM̄A3A1
MmSA14	A6AM̄A3A2
MmSL1A thru MmSL14A	Core Array
MmSL1B thru MmSL14B	
MmSTROB	A6AMA6A1
MmSTRP1	
MmSTRP2	

Note: Origins of TMR signals are shown for channel 1 only.

Figure 10-46. Signal Origin List (Sheet 4)

SIGNAL	ORIGIN
MmSTRP3	A6AMA6A1
MmS0E0	A6AMA1A1
MmS0E1	
MmS0E2	
MmS0E3	
MmS0E4	
MmS0E5	
MmS0E6	
MmS0E7	
MmS0I0	
MmS0I1	
MmS0I2	
MmS0I3	
MmS0I4	
MmS0I5	
MmS0I6	
MmS0I7	
MmS1E0	
MmS1E1	
MmS1E2	
MmS1E3	
MmS1E4	
MmS1E5	
MmS1E6	
MmS1E7	
MmS1I0	
MmS1I1	
MmS1I2	
MmS1I3	
MmS1I4	
MmS1I5	
MmS1I6	
MmS1I7	
MmTCV	A6AMA6A1
M0SYN	A1A16-A
M0SYNV	A5A6-A
M1SYNC	A1A16-B
M1SYNCV	A5A5-A
M2SYNC	A1A16-A
M2SYNCV	A5A6-A
M3SYNC	A1A16-B
M3SYNCV	A5A5-A
M4SYNC	A1A16-A
M4SYNCV	A5A6-A
M5SYNC	A1A16-B
M5SYNCV	A5A5-A

SIGNAL	ORIGIN
M6SYNC	A1A16-A
M6SYNCV	A5A6-A
M7SYNC	A1A16-B
M7SYNCV	A5A5-A
NU	A1A5-A
NUN	
OC	A1A14-B
OCN	
OP1	A1A12-A
OP1N	
OP1V	A4A5-B
OP1VN	
OP2	A1A12-A
OP2N	
OP2V	A4A5-B
OP2VN	
OP3	A1A12-A
OP3N	
OP3V	A4A5-B
OP3VN	
OP4	A1A12-A
OP4N	
OP4V	A4A6-B
OP4VN	
P	A4A12-B
PA	A1A13-B
PAD	A1A20-B
PADN	
PAE1	A1A17-A
PAE2	
PAE3	
PAE4	
PAE5	
PAE6N	
PAN	A1A13-B
PAO1	A1A17-A
PAO2	
PAO3	
PAO4	
PAO5	
PAO6	
PAO7	
PAO8	

SIGNAL	ORIGIN
PAO9	A1A17-A
PAO10	
PAO11	
PAO12	
PAR	A1A11-B
PARN	
PARV	A5A15-A
PAV	A4A8-A
PAVN	A4A8-B
PB	A1A13-B
PBE1	A1A17-B
PBE2	
PBE3	
PBE4	
PBE5	
PBE6N	
PBN	A1A13-B
PBO1	A1A17-B
PBO2	
PBO3	
PBO4	
PBO5	
PBO6	
PBO7	
PBO8	
PBO9	
PBO10	
PBO11	
PBO12	
PBV	A4A8-A
PBVN	A4A8-B
PC	A1A13-B
PCN	
PCV	A4A8-A
PCVN	A4A8-B
PDD	A1A11-B
PDDN	
PIO	A1A12-B
PIOV	A4A5-A
PN	A4A12-B
POD	A1A11-B
PODN	
PP	A4A12-B
PPN	
PQR	A1A5-A
PQRN	

Note: Origins of TMR signals are shown for channel 1 only.

Figure 10-46. Signal Origin List (Sheet 5)

SIGNAL	ORIGIN
PR	A1A5-A
PRN	
PR0	A1A9-B
PR0N	
PR0V	A4A9-B
PR0VN	
PR1	A1A9-B
PR1N	
PR2	
PR2N	
PR2V	A4A9-B
PR2VN	
PR3	A1A9-B
PR3N	
PR4	
PR4N	
PR5	
PR5N	
PR6	
PR6N	
PR7	
PR7N	
PR8	
PR8N	
PR9	
PR9N	
PR10	
PR10N	
PWR RET	External
P1N	A1A7-A
P1VN	A4A13-B
P2N	A1A7-A
P2VN	A4A13-B
P3N	A1A7-A
P3VN	A4A13-A
Q	A4A12-A
QN	
QP	A4A12-B
QPN	
Q1	A1A9-A
Q1N	
Q2	
Q2N	
Q3	
Q3N	

SIGNAL	ORIGIN
Q4	A1A9-A
Q4N	
Q5	
Q5N	
Q6	
Q6N	
Q7	
Q7N	
Q8	
Q8D	A1A10-A
Q8DN	
Q8N	A1A9-A
Q8V	A4A9-A
Q9	A1A7-A
Q9N	
R	A4A12-A
RAC	A1A10-A
RACN	
RD	A1A15-A
RDM	A1A15-B
RDMN	
RDMV	A5A6-B
RDMVN	
RDV	
RECN	A1A15-B
RED	A1A14-B
REDN	
REI	
REIN	
RN	A4A12-A
RP	
RPN	
RUN	A1A15-A
RUNN	
RUNV	A5A5-B
RUNVN	
RV	A4A12-A
RVN	
S	A4A12-A
SAPO	A1A12-B
SBRX	A1A11-B
SBRXN	
SBRXV	A5A13-A
SBRY	A1A11-B

SIGNAL	ORIGIN
SBRYN	A1A11-B
SBRYV	A5A13-A
SBRZ	A1A11-B
SBRZN	
SBRZV	A5A15-A
SG1	A1A8-B
SG1N	
SG2	
SG2N	
SHF	A1A12-B
SHFV	A4A5-A
SIG RET	External
SINK	A1A15-A
SINKN	
SLD	
SLDN	
SMDN	A1A8-A
SN	A4A12-A
SRTR	A1A11-A
SRTRN	
SS	A1A18-A
SSF	A1A12-B
SSFSN	
SSN	A1A18-A
STMD	
STMDN	
STO	A1A11-B
STON	A1A12-B
STOVN	A4A5-A
STP	A1A5-A
STPN	
SV	A4A12-B
SVN	
SYLC1	A1A15-A
SYLC1N	
SYLC1V	A5A6-B
SYL0N	A1A15-A
SYL0VN	A5A5-B
SYL1N	A1A15-A
SYL1VN	A5A6-B
SYNC	A1A15-B
SYNCN	
S4	A1A19-A
S4N	
TA	A1A19-B

Note: Origins of TMR signals are shown for channel 1 only.

Figure 10-46. Signal Origin List (Sheet 6)

SIGNAL	ORIGIN
TAN	A1A19-B
TBC	A1A13-B
TBCN	
TBCV	A4A8-B
TBR	A1A11-B
TBRN	
TBRV	A5A13-A
TER	External
TFD	A1A8-B
TFDN	
TFDV	A4A14-A
TFDVN	
THERM1	A4A11-B
THERM2	
TIME	A1A15-B
TIMEN	
TLC	
TLCN	
TLCV	A5A5-B
TM	A1A7-A
TMDN	A1A8-A
TMN	A1A7-A
TMV	A4A14-B
TMVN	
TR1	A1A18-A
TR1D	
TR1DN	
TR1N	
TR1V	A5A14-B
TR2	A1A18-A
TR2N	
TR2V	A5A14-B
TR3	A1A18-A
TR3D	
TR3DN	
TR3N	
TR3V	A5A14-B
TR4	A1A18-B
TR4N	
TR4V	A5A14-B
TR5	A1A18-B
TR5N	
TR5V	A5A14-B
TR6	A1A18-B
TR6D	
TR6DN	

SIGNAL	ORIGIN
TR6N	A1A18-B
TR6V	A5A14-B
TR7	A1A18-B
TR7N	
TR7V	A5A14-A
TR8	A1A18-B
TR8N	
TR8V	A5A14-A
TR9	A1A18-B
TR9D	
TR9DN	
TR9N	
TR9V	A5A14-A
TR10	A1A11-A
TR10N	
TR10V	A5A14-A
TR11	A1A11-A
TR11N	
TR11V	A5A14-A
TR12	A1A11-A
TR12D	
TR12DN	
TR12N	
TR12V	A5A15-A
TR13	A1A11-A
TR13N	
TR13V	A5A14-A
TRS	A1A11-A
TRSN	
TRSV	A5A15-A
TRSVN	
TTL	A1A12-B
TTLN	
TTLV	A4A6-B
TTT	A1A11-B
UACCO	A1A10-B
UTR	
UTRV	A4A7-B
VOY	A1A7-A
VOYN	
VOYV	A4A13-B
VOYVN	
V1	External
V3	

SIGNAL	ORIGIN
V4MOD1	External
V4MOD2	
V4MOD3	
V4MOD4	
V4MOD5	
V4MOD6	
V4MOD7	
V5	
V5MOD1	
V5MOD2	
V5MOD3	
V5MOD4	
V5MOD5	
V5MOD6	
V5MOD7	
V20	
WDA	A1A3-A
WF	
WN	
W1	
W2	
W3	
W4	
W5	
W6	
W7	
W8	
XDA	A1A3-A
XF	
XN	
X1	
X2	
X3	
X4	
X5	
X6	
X7	
X8	
YDA	A1A3-B
YF	
YN	
Y1	

Note: Origins of TMR signals are shown for channel 1 only.

Figure 10-46. Signal Origin List (Sheet 7)

SIGNAL	ORIGIN
Y2	A1A3-B
Y3	
Y4	
Y5	
Y6	
Y7	
Y8	

SIGNAL	ORIGIN
ZDA	A1A3-B
ZDHN	A1A8-A
ZDLN	
ZER	A1A10-A
ZERN	
ZF	A1A3-B
ZN	

SIGNAL	ORIGIN
Z1	A1A3-B
Z2	
Z3	
Z4	
Z5	
Z6	
Z7	
Z8	

Note: Origins of TMR signals are shown for channel 1 only.

Figure 10-46. Signal Origin List (Sheet 8)

Refer to Back Panel Lists for the Saturn V Launch Vehicle Digital Computer. (Supplied under separate cover.)

Figure 10-47. Interconnection A1 Back Panel, List for LVDC

Refer to Back Panel Lists for the Saturn V Launch Vehicle Digital Computer. (Supplied under separate cover.)

Figure 10-48. Interconnection A4 Back Panel, List for LVDC

Refer to Back Panel Lists for the Saturn V Launch Vehicle Digital Computer. (Supplied under separate cover.)

Figure 10-49. Interconnection A5 Back Panel, List for LVDC

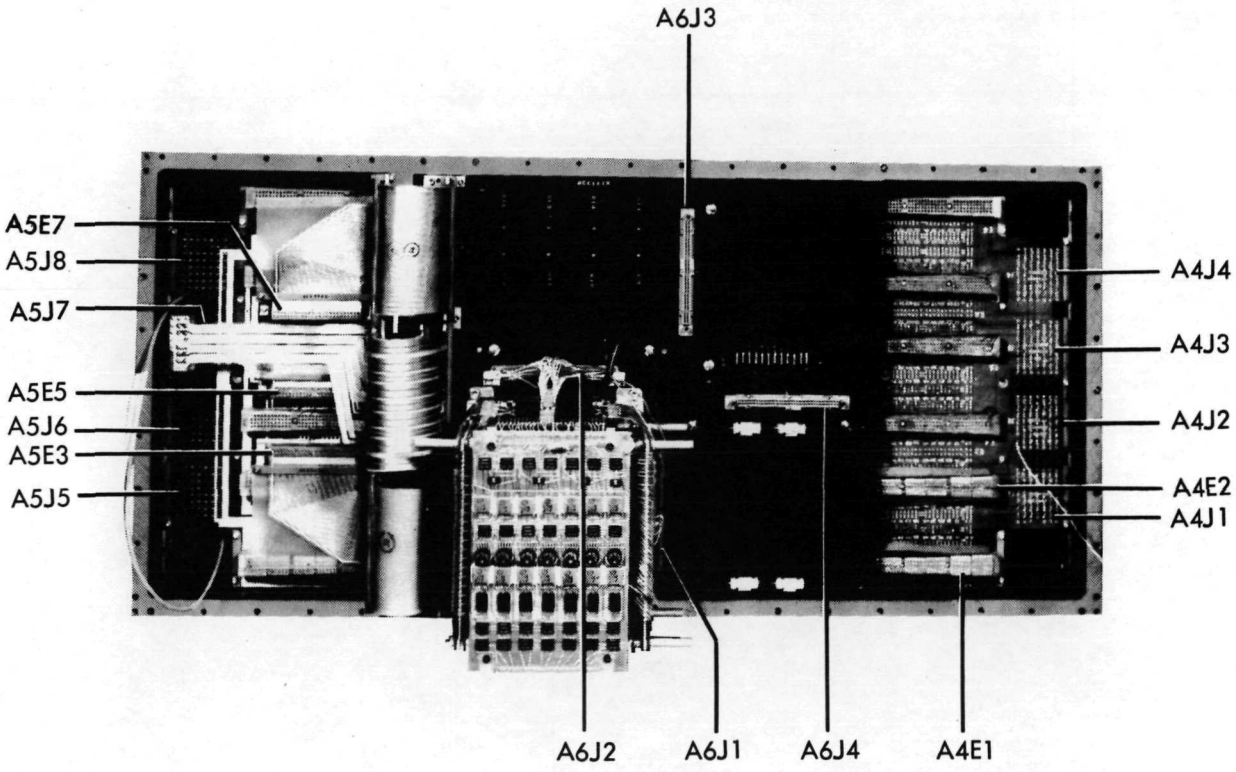


Figure 10-50. Computer, Rear View

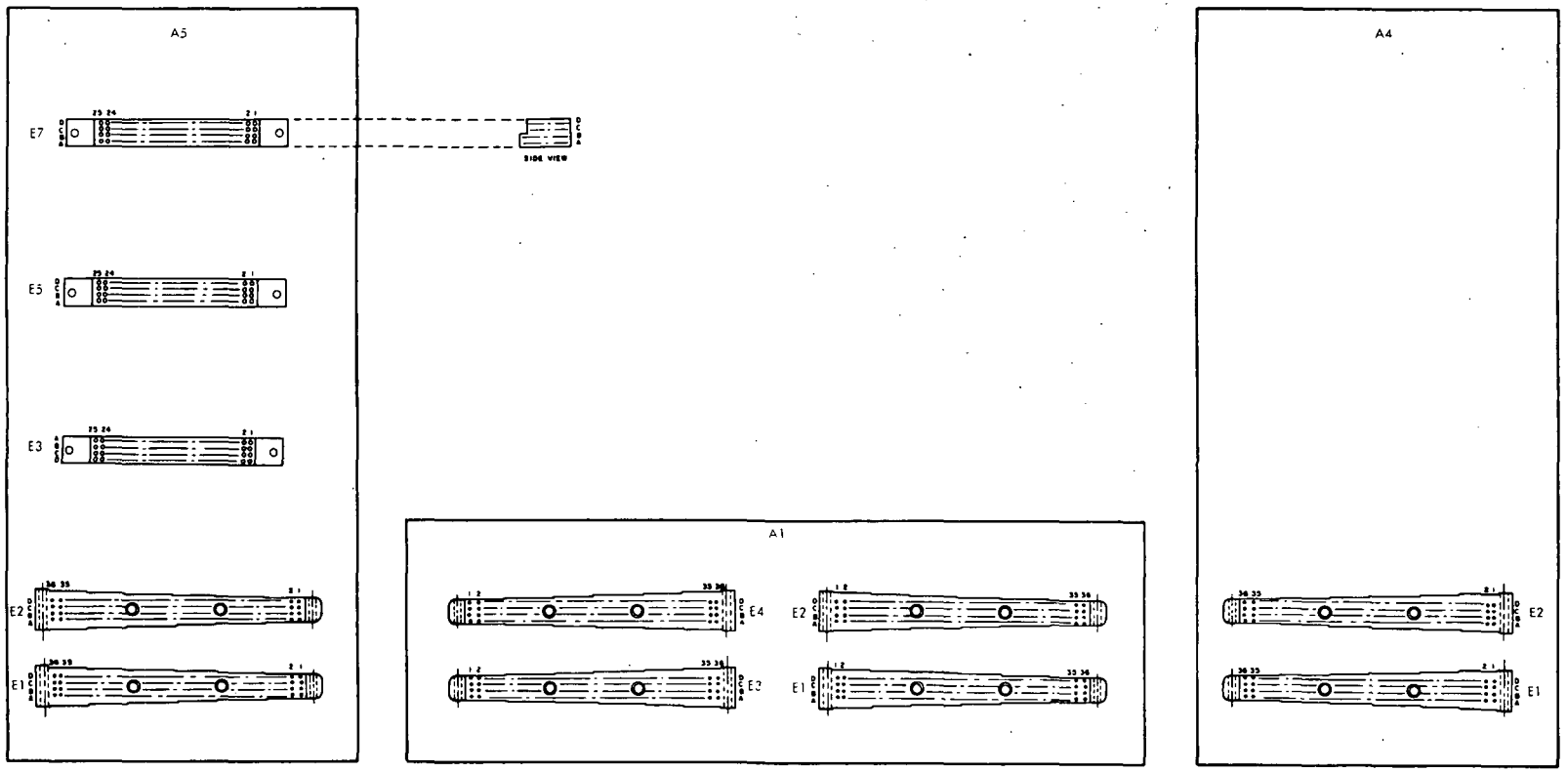


Figure 10-51. Terminal Block Pin Identification; Channels 1, 4, and 5

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