BASIC CIRCUITS

FOR

AN/FSQ-7
COMBAT DIRECTION CENTRAL

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PART 1
INTRODUCTION

1.1 SCOPE OF MANUAL

This manual presents the theory of operation for the basic circuits in AN/FSQ-7 Combat Direction Central and AN/FSQ-8 Combat Control Central. Electronically, these equipments are a complex combination of many circuits. They have been subdivided into seven functional systems: the Input, Output, Drum, Central Computer, Display, Power Supply and Marginal Checking, and Warning Light Systems. By definition, a basic circuit is used in more than one system; a special circuit is used in only one system.

Figure 1–1 illustrates the relationship between a basic circuit and a part of the equipment. As shown, the basic circuit represents a fundamental building block of the electronic portion of the equipment. The schematic drawing is a model C cathode follower. Behind it is the logic block symbol which represents the model C cathode follower in logic block schematics. The logic block schematic is the functional diagram of the electronic operation of a pluggable unit, which is, in turn, a small replaceable unit of the equipment.

This circuit is a member of the cathode follower group, which is a part of the 14 groups discussed in Part 3 of this manual. Since they are used in one form or other throughout the entire equipment, the 14 groups constitute a large majority of the circuits in the equipments. This fact emphasizes their importance as fundamental building blocks.

The logic block symbol is designed to facilitate the explanation of equipment operation. It permits the presentation of relatively simple logic block schematics to describe equipment function. A comparison (fig. 1–1) of the electrical symbol presentation of the circuit and its equivalent logic block symbol will indicate the degree of simplification introduced by the logic block symbol. Equipment function (logic) is explained in other manuals in terms of these symbols. This manual presents the theory of operation of the basic circuits represented by certain logic block symbols.

1.2 ORGANIZATION OF MANUAL

1.2.1 General

This manual consists of three parts. Part 1 introduces the manual. Part 2 discusses circuit elements with a common function; the extensive repetition of these circuit elements throughout the AN/FSQ-7 and AN/FSQ-8 Systems permits a separate treatment of their function, thereby adding to the simplification of basic circuit theory discussion. Part 3 presents the theory of operation of 14 basic circuits.

1.2.2 Contents of Part 1 — Introduction

Part 1 explains the organization of the manual and introduces the basic circuit, demonstrating the significance of the basic circuit in the equipment and relating the circuit to the equipment.

1.2.3 Contents of Part 2 — Common Circuit Characteristics

Certain mechanical and electrical information necessary in the study of the basic circuits is discussed in Part 2. Common signals are identified and discussed. The physical characteristics of the basic circuits are investigated, and the electrical limitations that result are noted. The compensation of these electrical limitations is resolved, and parasitic suppression and resistance-capacitance (RC) decoupling are thoroughly analyzed.

Common circuits employed in the clamping and coupling of levels are discussed and supported with mathematical calculations where such support is applicable. Finally, speedup circuits are analyzed as to their application in the basic circuits.

1.2.4 Contents of Part 3 — Theory of Operation

Part 3 describes the theory of operation of the 14 basic circuits employed throughout the AN/FSQ-7 and AN/FSQ-8 equipments. The circuits fall into two general groups: logic and nonlogic circuits.

Note

Logic and *nonlogic* (as applied to basic circuits) are terms used to differentiate functionally between electrical circuits. Logic circuits are those that perform the operational functions of the equipment. Nonlogic circuits are those that facilitate the signal transfer between logic circuits, ensuring system dependability.

Chapters 1 through 6 include the nonlogic circuits, arranged in the following order: cathode follower, d-c level setter, pulse amplifier, register driver, thyratron relay driver, and vacuum-tube relay driver. Chapters 7 through 14 include the logic circuits, arranged in the

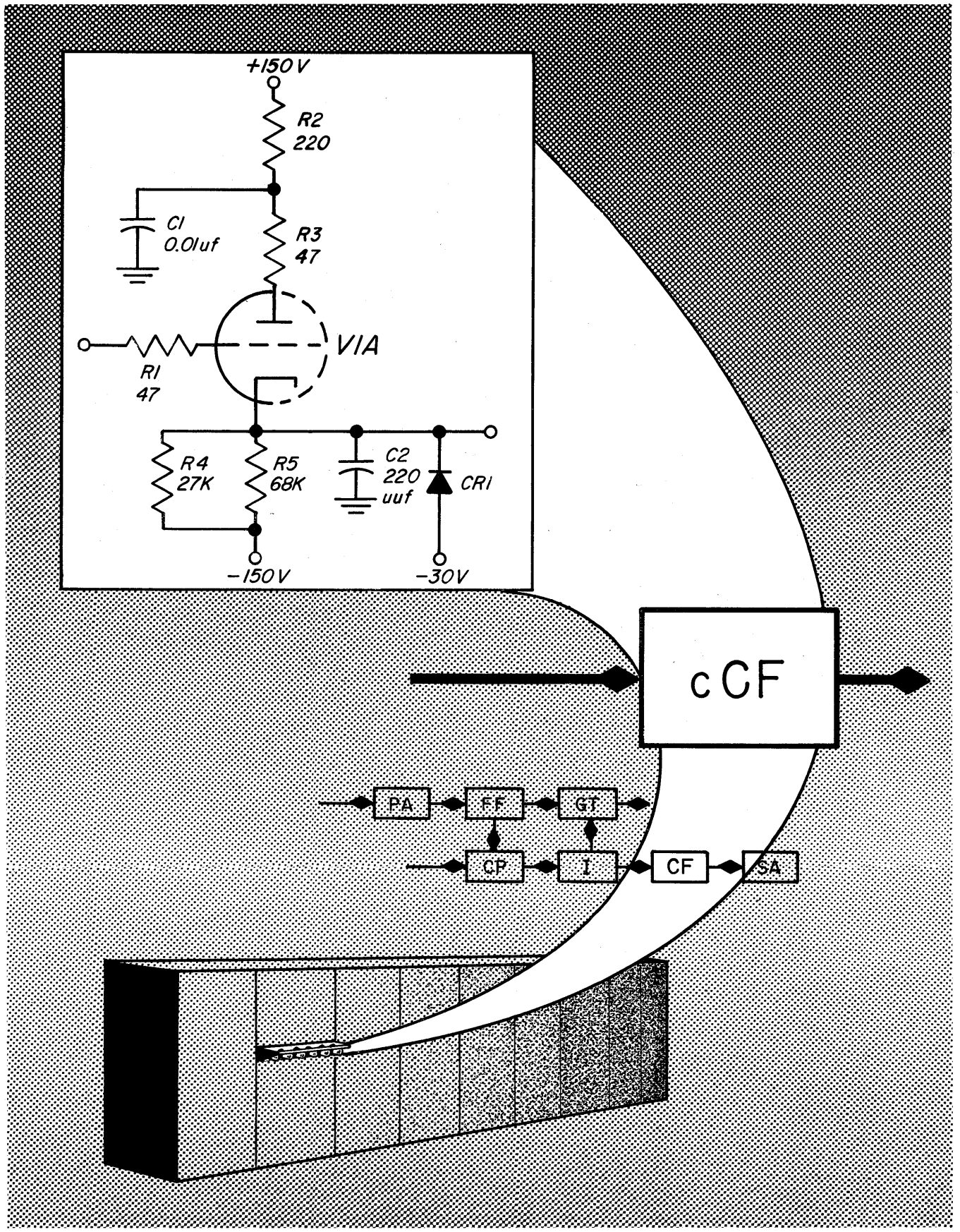


Figure 1—1. Basic Circuit, A Fundamental Building Block

following order: AND, OR, gate, inverter, flip-flop, single-shot multivibrator, pulse generator, and delay unit.

Each chapter follows the same format and comprises, in general, three paragraphs. The first paragraph (Definition and Description) identifies the circuit logic block symbol, describes circuit function, and enumerates the significant differences between the models in terms of capabilities, limitations, or operational characteristics.

The second paragraph (Principles of Operation) discusses the operation of the circuit. The treatment of each circuit proceeds from basic considerations to specific functions of detail parts. Where circuit complexity requires such treatment, each circuit is reduced to its simplest operating elements, and the fundamental principles of operation are explained in terms of this circuit. A detailed discussion follows in terms of a specific model of the circuit, which consists of the simplified circuit and the added refinements used to adapt the simple circuit to its operational environment.

The third paragraph (Circuit Refinements) may or may not appear in a chapter. The complexity of a circuit and the nature of its refinements dictate the need for a separate detailed discussion. Wherever possible, the circuit refinements are discussed under principles of Operation; otherwise, they are discussed in the third paragraph.

Generally, each chapter will contain one complete schematic for each model of a circuit. In many cases, these schematics have been simplified to reduce the number of detail parts shown. For example, parallel and series resistors are combined in a representative single resistor of equivalent value. For this reason the schematics, though electrically correct, are not wiring diagrams of the actual circuit. The distinction between the simple or fundamental circuit and its refinements is made on the complete circuit schematics by drawing the parts of the fundamental circuit with a heavier line.

Table 1–1 lists the 14 basic circuits in their logic and nonlogic categories and groups them in their general classifications.

The voltages discussed in this manual are approximate, and nominal values are assumed. When voltage levels are specified, they are referenced to ground unless otherwise indicated. Waveforms are idealized and deviate slightly from the actual. Current flow from negative to positive potentials (electron flow) is assumed unless otherwise specified.

TABLE 1–1. FUNCTIONAL BREAKDOWN OF BASIC CIRCUITS

	POWER AMPLIFIERS	CONTROL	RESTORER
NONLOGIC	Cathode followers Pulse amplifiers Register drivers	Thyratron relay drivers Vacuum-tube relay driver	D-C level setters

	COINCIDENCE	CONVERSION	TIMING	STORAGE
LOGIC	Diode AND Diode OR Gate	Inverter Pulse generator	Delay unit Single shot	Flip-flop

PART 2
COMMON CIRCUIT CHARACTERISTICS

2.1 INTRODUCTION

A thorough knowledge of signal inputs and outputs is a prerequisite in the study of basic circuits. These inputs and outputs are pulses and levels, which are further categorized as standard and nonstandard.

2.1.1 Standard Pulses

The standard pulse (fig. 2–1) is a +30-volt pulse

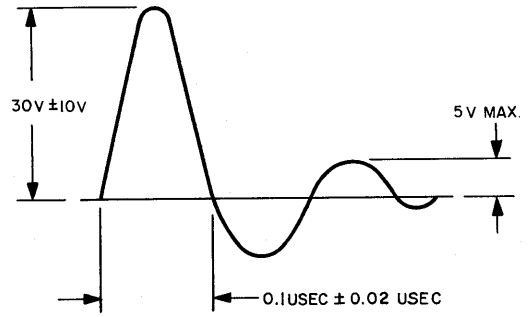


Figure 2–1. Standard Pulse

(nominal) with a tolerance of ±10 volts. The pulse shape approaches that of the positive half of a sine wave, with a negative tail of indefinite value. The pulse width measured at the base has a nominal value of 0.1 microsecond and a tolerance of ±0.02 microsecond. It is evident that a standard pulse is defined by its amplitude, pulse width, and shape.

2.1.2 Standard Levels

There are two standard levels (fig. 2–2): the up level is a d-c potential of +10 volts (nominal); the down level is a d-c potential of −30 volts (nominal). Rise time (T_R) is the period during which the potential climbs 40 volts from a down level to an up level. Fall

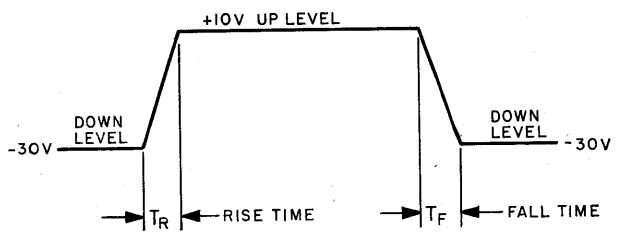


Figure 2–2. Standard Levels

time (T_F) is the period during which the potential drops 40 volts from an up level to a down level. The standard signals just discussed are represented as logic lines with characteristic terminating symbols (fig. 2–3).

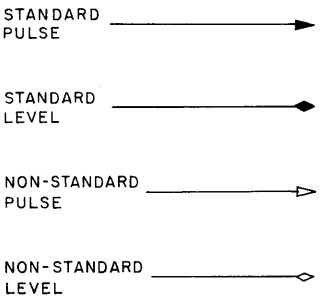


Figure 2–3. Signal Symbols

The standard pulse is indicated by a line terminated in a solid arrowhead. The standard level, either up or down, is indicated by a line terminated in a solid diamond.

2.1.3 Nonstandard Signals

A nonstandard pulse is indicated by a line terminated in an open arrowhead. Any other nonstandard signals will be indicated by a line terminated in an open diamond.

2.2 PHYSICAL CHARACTERISTICS

Several electrical circuit refinements are dictated by the physical layout and by the techniques employed in the packaging of the circuits of the AN/FSQ-7 and AN/FSQ-8 Systems. To appreciate the necessity of the electrical requirements peculiar to this equipment, it would be advantageous to become acquainted with the physical characteristics of the machine.

A basic circuit consists of one or more card assemblies, together with other detail parts and wiring. The card assembly consists of a card detail upon which detail parts are automatically mounted and automatically dip-soldered. Figure 2–4 presents front and rear views of a typical card detail. The card is composed of a phenolic base which has been tooled as indicated in this figure. Both sides of the card detail contain printed circuitry which interconnects the appropriate lands. A typical card assembly, depicted in figure 2–5, has the detail parts and lugs mounted. A number of these card

assemblies are then mounted in a mechanical assembly and electrically connected to various detail parts, such as vacuum-tube sockets, individual resistors, capacitors, and electrical connectors. This complete assembly is called a pluggable unit (fig. 2–6). The pluggable unit may consist of several basic and special circuits which are electrically connected.

This method of physical construction makes possible the automatic manufacture of the card assembly (which contains most of the detail parts employed) and easy removal and replacement of the pluggable unit. There are two standard types of pluggable units: one accommodates a maximum of nine vacuum tubes (shown in fig. 2–6); the other, a maximum of six tubes (not shown). The electrical connectors mounted along the bottom of the pluggable unit provide a means of supplying service voltages and inputs to the unit. Outputs are also taken off at these points.

2.3 PARASITIC SUPPRESSION

The manufacturing and packaging techniques just discussed result in lead lengths longer than those in common use. (See fig. 2–6.)

The basic circuits, for the most part, include vacuum tubes; in circuits of this type, where long leads are prevalent, parasitic oscillations result. Parasitic oscillations are undesirable, self-generated, cyclic voltages, produced by unplanned resonant circuits appearing in the grid, plate, and screen circuits of a vacuum tube. Figure 2–7 illustrates the effects of lumping long leads into equivalent inductances and of lumping stray wiring and tube capacitances into equivalent capacitors. This circuit,

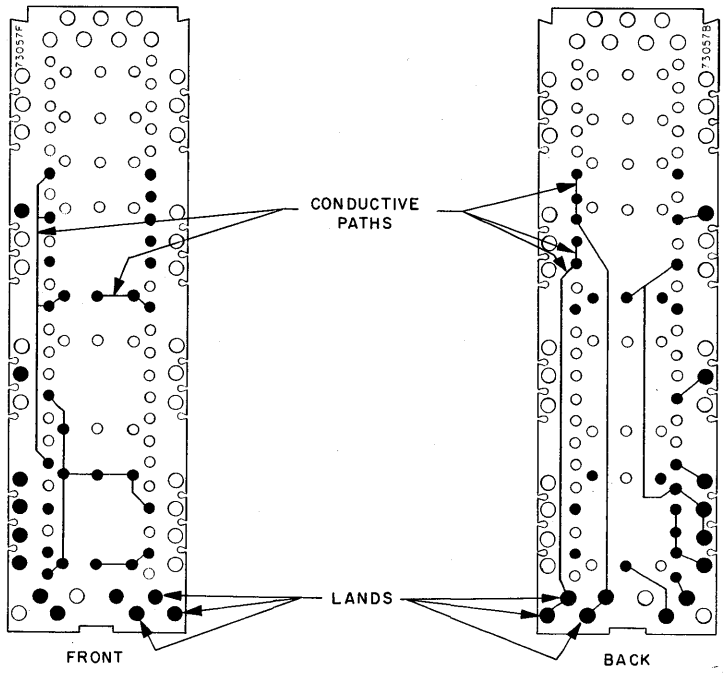


Figure 2–4. Typical Card Detail

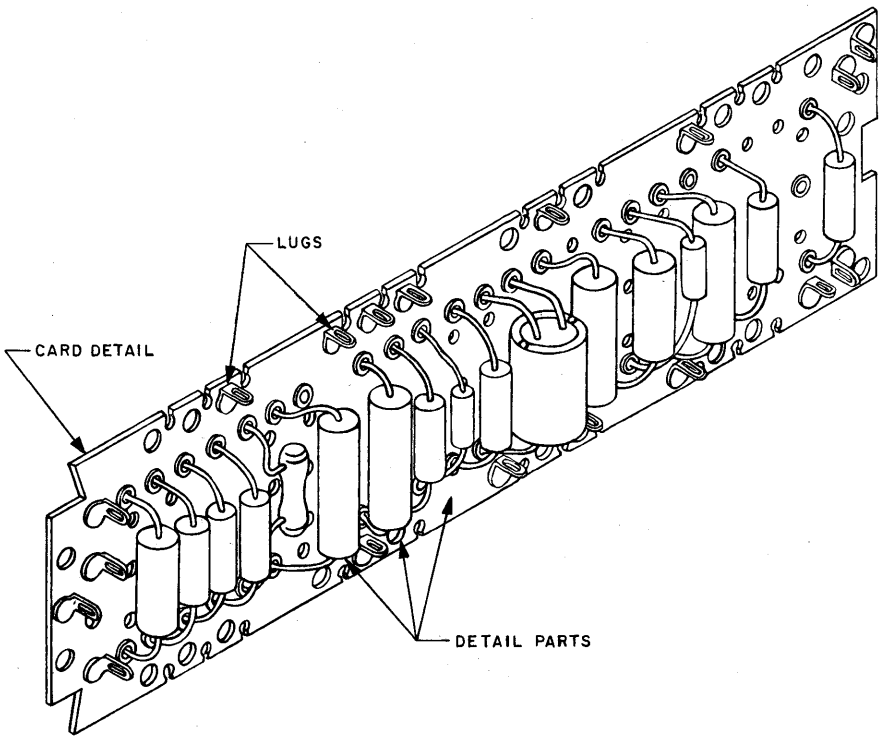


Figure 2–5. Typical Card Assembly

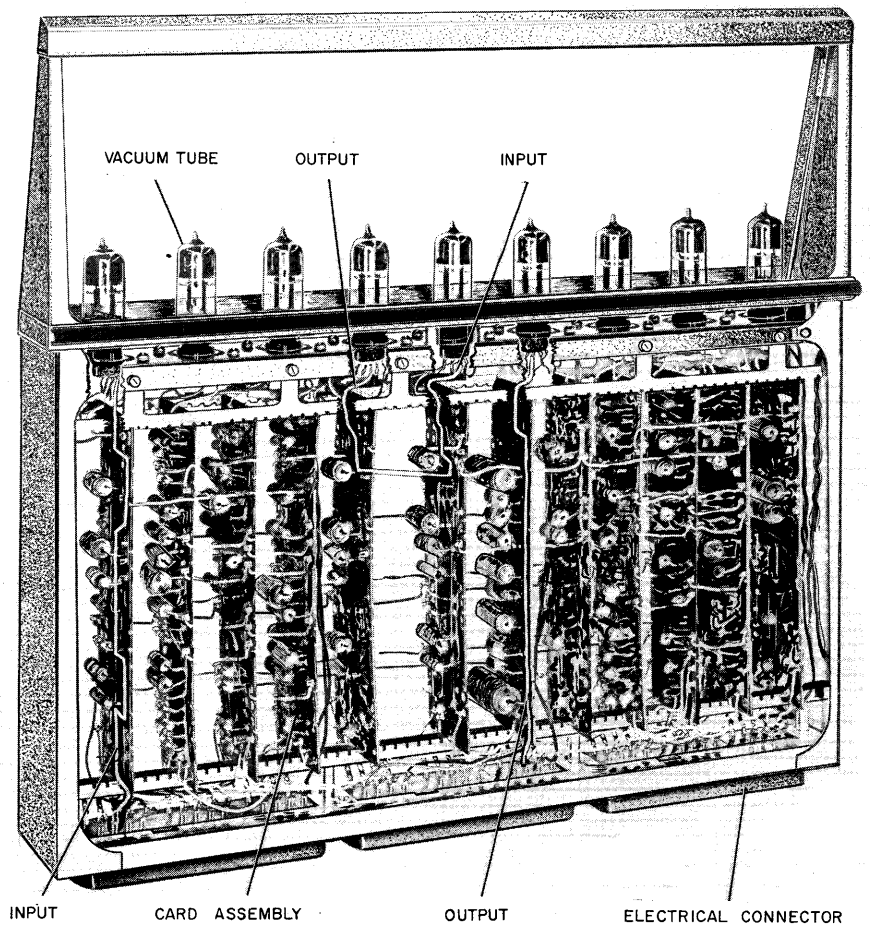


Figure 2–6. Typical Pluggable Unit

which closely resembles a tuned-grid tuned-plate oscillator, could support oscillations.

To eliminate parasitic oscillations in this and in comparable circuits, parasitic suppressing resistors are used. Such resistors add loss into an undesirable resonant circuit, reducing the circuit's efficiency to such a degree that parasitic oscillation is no longer possible.

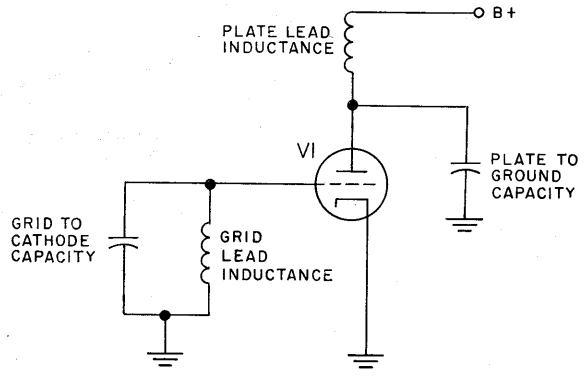


Figure 2–7. Lumped Constants, Equivalent Circuit, Simplified Schematic Diagram

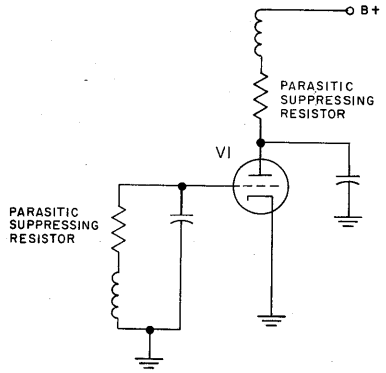
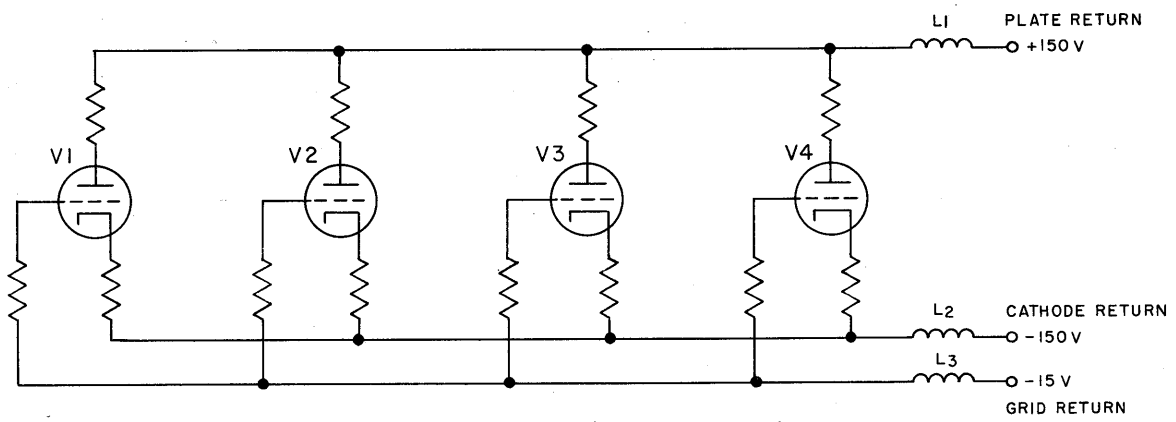


Figure 2–8. Lumped Constants, Equivalent Circuit with Parasitic Suppressing Resistors Added, Simplified Schematic Diagram

Figure 2–8 shows the circuitry of figure 2–7 with the parasitic suppressing resistors added. For maximum effectiveness, resistors are mounted at the vacuum-tube socket. They will be found in all the plate and control grid leads of the vacuum tubes employed in the basic circuits and also, where necessary, in basic circuit vacuum-tube cathode and screen leads.



L_1, L_2, L_3 REPRESENT THE LUMPED INDUCTANCES OF THE SERVICE VOLTAGE LINES.

Figure 2–9. Common Return Paths, Simplified Schematic Diagram

2.4 RC DECOUPLING

The various circuits that constitute the AN/FSQ-7 and AN/FSQ-8 Systems, of which the basic circuits are a major part, derive their service voltages from common power supplies. For this reason, numerous vacuum-tube circuits have their plate, control grid, cathode, and screen grid circuits returned through common leads (see fig. 2–9). Long power leads and the fact that a large number of circuits share a common return contribute to the generation of undesired signals. Because these signals would affect machine dependability, resistance-capacitance (RC) decoupling circuits are employed in all the vacuum-tube return circuits to attenuate them. Figure 2–10 is a simplified schematic of one vacuum-tube circuit employing an RC decoupling filter in each of its return paths. These RC filters attenuate undesirable signals appearing at the plate, cathode, control grid, and screen grid return circuits to such a degree that machine dependability is no longer threatened.

Figure 2–11 presents a typical RC decoupling circuit, with the associated mathematics to explain its operation. It can be shown that, if an RC decoupling filter functions satisfactorily at the lowest frequency (the frequency for which it was designed), its effectiveness will increase at higher frequencies. It should be noted that, although the attenuation of one of the RC filters has been calculated to be approximately 15, the attenuation between any two circuits, each employing one of these filters, is 15^2, or 225 (fig. 2–12).

Note

The d-c potential at the output of the RC decoupling filter is assumed to be the same as the input or supply potential. The ohmic value of the decoupling resistor, R, is small when compared with the resistance of the circuit returning at this point. For the same reason, this point is considered to be at a-c ground because of the extremely low value of reactance of decoupling capacitor C.

2.5 COMMON CIRCUITS FOR CLAMPING AND COUPLING LEVELS

There are a number of circuit techniques dictated by the functional requirements of the equipments. Two of these techniques, diode clamping and d-c coupling, are repeated in several of the basic circuits and are treated, therefore, as a general circuit consideration.

2.5.1 Diode Clamping

Diode clamping is treated by considering this function in the output circuit of a model C flip-flop. (For a detailed discussion of crystal diode characteristics, refer to Part 3, Ch 7.)

Figure 2–13 shows the output circuit and the associated triode section of a model C flip-flop. For the purpose of this discussion, two states of conduction are as-

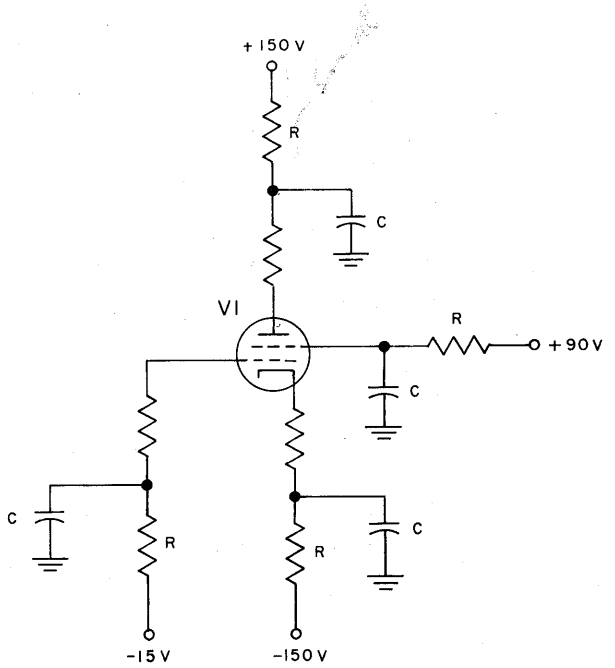
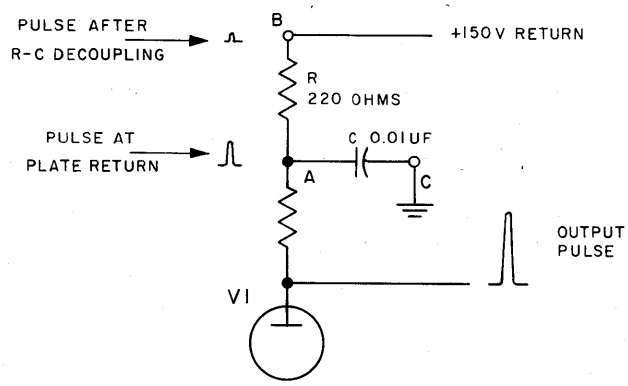


Figure 2–10. RC Decoupled Returns, Simplified Schematic Diagram



REACTANCE OF C IS

$$X_C = \frac{1}{2\pi FC}$$

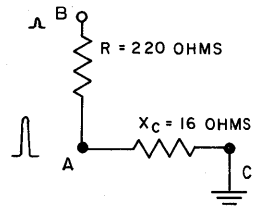
WHERE

$2\pi = 6.28$
$F = 10^6$ CPS (LOWEST FREQUENCY WHERE DECOUPLING IS REQUIRED)
C = 0.01 UF

THEN

$$X_C = \frac{1}{6.28 \times 10^6 \times 0.01 \times 10^{-6}} = 15.9 \text{ OHMS}$$

FOR SIMPLICITY LET X_C = 16 OHMS AND CONSIDER IT TO BE RESISTIVE. THEN THE DECOUPLING CIRCUIT MAY BE REDRAWN AS A VOLTAGE DIVIDER.



AN ALTERNATING VOLTAGE (PULSE) AT A, WILL CAUSE CURRENT TO FLOW IN TWO PATHS A-B AND A-C.

IT IS $\frac{220}{16}$ TIMES EASIER FOR CURRENT TO FLOW THROUGH A-C THAN IT IS THROUGH A-B; $\frac{220}{16}$ = 14 APPROX.

THEREFORE 14 TIMES MORE PULSE CURRENT WILL FLOW THROUGH A-C THAN A-B AND THE AMPLITUDE OF THE PULSE REMAINING AT B WILL BE ATTENUATED 15 TIMES.

Figure 2–11. RC Decoupling, Simplified Schematic Diagrams and Calculations

sumed: the unclamped output is either more positive than +10 volts or more negative than −30 volts.

The cathode of diode CR1 is biased at +10 volts. When the output voltage is less positive than +10 volts, diode CR1 is cut off. When the output rises slightly above +10 volts, diode CR1 conducts. The current through CR1 (I1) adds to the current through V1 (I2) to produce a voltage drop across R1 sufficient to maintain the output at +10 volts.

The anode of diode CR2 is biased at −30 volts. When the output voltage is more positive than −30 volts, CR2 is cut off. When the output falls slightly

below —30 volts, diode CR2 conducts. Current through R2 (I2 + I3) increases, raising the potential at the output to —30 volts. In this manner, the output of the flip-flop in figure 2–13 is limited to an up level of +10 volts and a down level of —30 volts. Varying loads and aging of components could produce undesirable variations of level at the output if they were not clamped as indicated. Clamping either one or both standard levels is a technique employed in certain applications of cathode followers, level setters, inverters, and flip-flops.

2.5.2 D-C Coupling

In several of the basic circuits it becomes necessary to dc-couple the plate of one stage to the control grid of another. This requirement will be found in the circuits either operating on or producing levels. Included are the flip-flops, d-c inverters, and d-c level setters.

Figure 2–14A is a simplified schematic diagram illustrating a dc-coupling network. Assume that the output levels required are —30 volts and +10 volts, alternately. This would require that the voltages at the control grid of V2 be d-c levels of approximaely —30 volts and +10 volts, alternately. Since levels are being coupled, d-c coupling is indicated (one that will pass direct current); therefore, neither a transformer nor a capacitor may be employed as the primary coupling device. The control grid, on the other hand, cannot be directly connected to the plate, because the level conditions (+10 v and —30 v) could never be reached in this manner. The method of d-c coupling illustrated in figure 2–14A employs a voltage divider consisting of plate resistor V1 (R1), resistor R2, and resistor R3. With vacuum tube V1 cut off, the current flowing through resistors R1, R2, and R3 develops a +10-volt level (E2) at the control grid of vacuum tube V2.

The mathematics supporting this conclusion follows. The voltage (E_1) across R1, R2, and R3 is

$$E_1 = +150\text{ v} - (-300\text{ v})$$
$$= 450\text{ v}$$

and the current (I_1) through resistors R1, R2, and R3 is

$$I_1 = \frac{E_1}{R_1 + R_2 + R_3}$$
$$\frac{450}{10 \times 10^3 + 130 \times 10^3 + 310 \times 10^3}$$
$$= \frac{450}{450 \times 10^3}$$
$$= 1 \times 10^{-3}\text{ amperes}$$

Therefore, the voltage (E_2) developed across resistor R_3 is

$$E_2 = I_1 R_3$$
$$= 1 \times 10^{-3} \times 310 \times 10^3$$
$$= 310\text{ v}$$

and the voltage at the grid of V2 with respect to ground is

$$E_g = E_2 + (-300\text{ v})$$
$$= +310 - 300\text{ v}$$
$$= +10\text{ v}$$

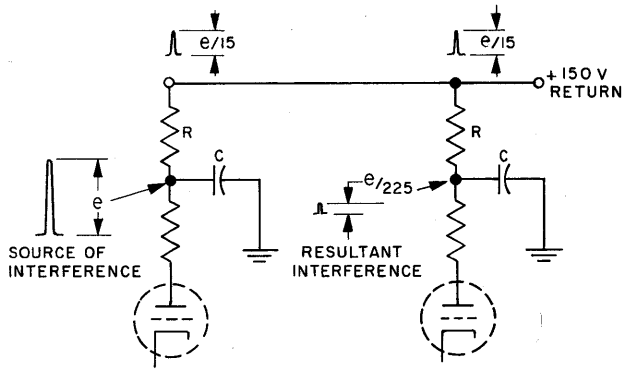
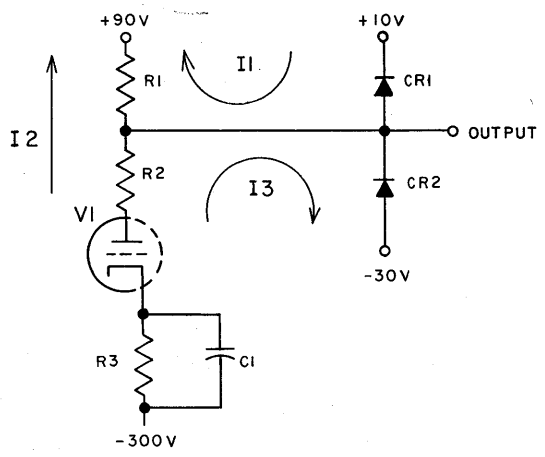


Figure 2–12. Attenuation of Interaction through RC Decoupling, Simplified Schematic Diagram



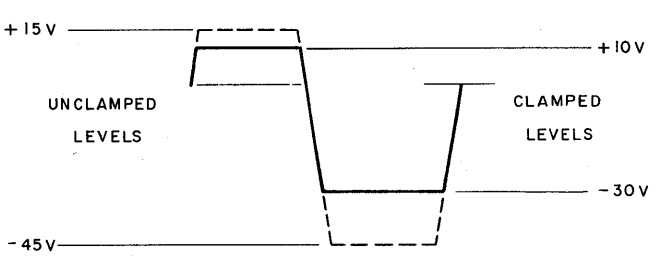
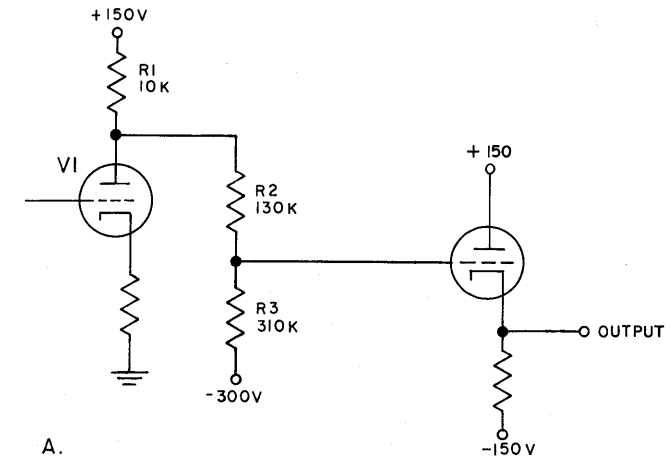
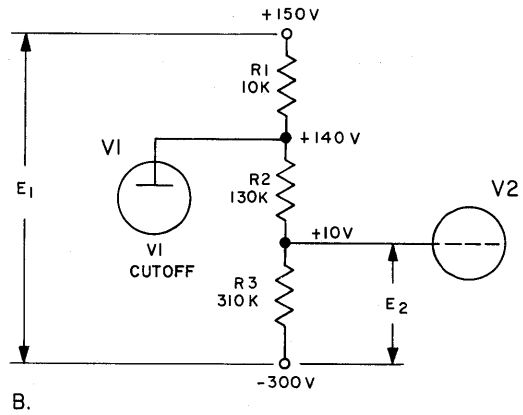


Figure 2–13. Diode Clamped Output Levels, Simplified Schematic Diagram





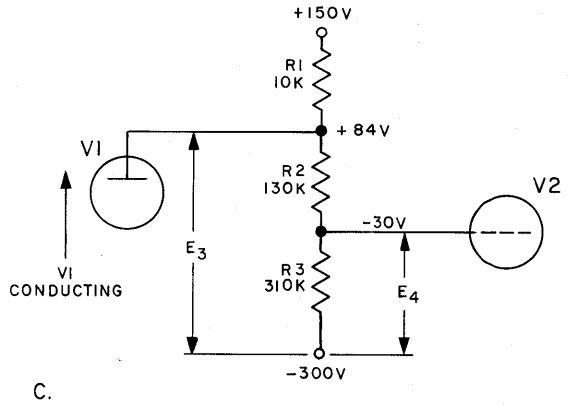


Figure 2–14. D-C Coupling Network, Simplified Schematic Diagram

where

E_g = voltage at control grid of V2 with respect to ground.

With vacuum tube V1 conducting, the additional current flowing through resistor R1 drops the potential at the plate of V1 to +84 volts (fig. 2–14C). As a result, the voltage (E_3) across resistors R2 and R3 becomes

$$E_3 = +84 \text{ v} - (-300 \text{ v})$$
$$= 384 \text{ v}$$

and the current (I_3) through resistors R2 and R3 is reduced

$$I_3 = \frac{E_3}{R2 + R3}$$
$$= \frac{384}{130 \times 10^3 + 310 \times 10^3}$$
$$= 0.873 \times 10^{-3} \text{ amperes}$$

The voltage drop (E_4) across resistor R3 is now

$$E_4 = I_3 \times R3$$
$$= 0.873 \times 10^{-3} \times 310 \times 10^3$$
$$= 270 \text{ v}$$

and the voltage (E_g) at the control grid of V2 with respect to ground is

$$E_g = E_4 + (-300 \text{ v})$$
$$= 270 \text{ v} - 300 \text{ v}$$
$$= -30 \text{ v}$$

It can be seen that this method of returning the plate to a highly negative potential through a voltage divider enables the coupling of levels from a plate operating at a higher bias to a grid operating at a lower bias.

2.6 SPEEDUP CIRCUITS

Machine operation frequently depends on the speed at which levels shift. This makes rise and fall time an important characteristic of level outputs. The speedup of rise and fall time is a requirement satisfied by circuit configurations in certain of the basic circuits which produce levels. Flip-flops, d-c inverters, and d-c level setters are compensated to speed up the rise and fall of level outputs.

2.6.1 Voltage Divider Compensation

One of the most routine methods employed to effect the shortening of rise and fall time is voltage divider compensation. Figure 2–15 is a simplified schematic diagram of a compensated d-c coupling network. This schematic includes two capacitors not included in figure 2–14A, C1 and C2. Capacitor C1 is a compensating capacitor, and capacitor C2 is the input capacity of V2. This input capacity, which must be compensated for, consists of stray capacity plus the effective grid-to-

ground capacity of V2. Were it not for compensation, the capacity of C2 would result in a slow rise and fall at the output of V2 (fig. 2–16). It can be seen that, in the uncompensated output, there is considerable curvature at the corners of the waveform. This is caused by the attenuation of the high-frequency components of which level shifts are composed. The level itself is not affected because it consists of low-frequency and d-c components, which are not attenuated by C2 capacitance.

Capacitor C1 bypasses resistor R2 (fig. 2–15), increasing the amplitude of high-frequency components at the grid of V2 by the same amount that they are attenuated by capacitor C2. This results in a compensated (speeded-up) output, shown in figure 2–16.

2.6.2 Peaking Coils

Another method of speeding up rise and fall time entails the use of a peaking coil (fig. 2–17). The various capacities affecting the resultant output at the plate of vacuum tube V1 are represented as capacitor C1. Without compensation, the high-frequency components of the output waveform would be attenuated by the effect of capacitor C1, and the resultant waveform would be that indicated by the broken line.

Including L1 in series with R1 produces an effective plate load

$$Z = R1 + X_L$$

where

Z = the plate load impedance

X_L = the inductive reactance of peaking coil L1

in addition

$$X_L = 2\pi FL$$
$$= 6.28\,FL$$

where

F = frequency in cycles per second

L = inductance of peaking coil L1 in henries

It is apparent that the load impedance (Z) is a function of frequency: the higher the frequency, the larger X_L becomes and, hence, the larger Z becomes.

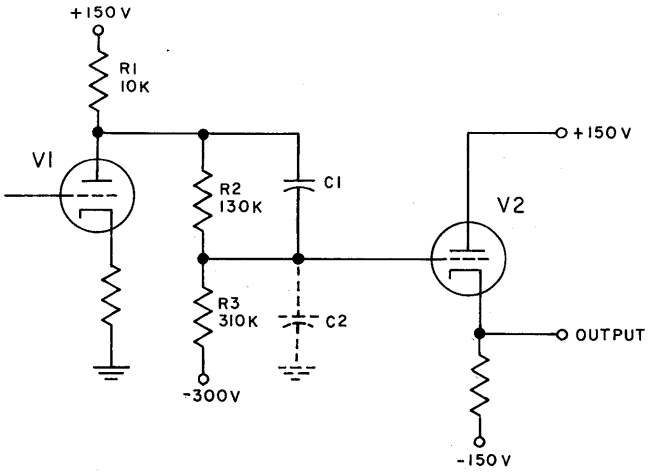


Figure 2–15. Compensated D-C Coupling Network, Simplified Schematic Diagram

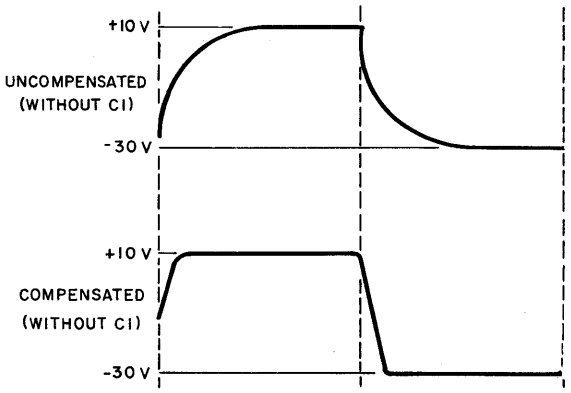
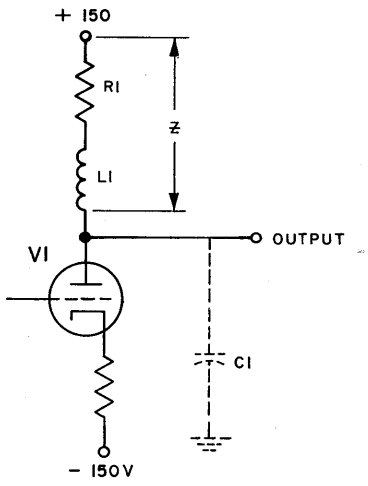


Figure 2–16. Output Waveform (V2 in Figure 2–15)



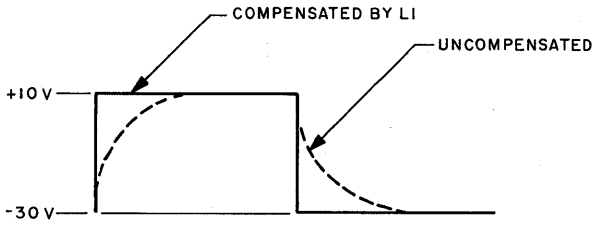


Figure 2–17. Peaking Coil Compensated Plate Circuit, Simplified Schematic Diagram with Waveform

The gain of an amplifier is proportional to the expression

$$\frac{Z}{R_p + Z}$$

where

R_p = plate resistance of V1, a constant.

It therefore follows that the greater Z becomes, the greater the gain of this stage becomes.

As was previously stated, Z increases with frequency. Therefore, the gain and eventually the output of V1 will increase with frequency. This is opposite to the effect of capacitor C1, and the resultant waveform is compensated as indicated by the solid line.

At dc and low frequencies, the reactance (X_{L1}) of peaking coil L1 is of extremely small magnitude and, therefore, has no effect on the circuit. It can be seen that the level output is not affected by the inclusion of peaking coil L1. On the other hand, the rise and fall times which include high-frequency components are effectively shortened (speeded up).

PART 3
THEORY OF OPERATION

CHAPTER 1
CATHODE FOLLOWER

1.1 DEFINITION AND DESCRIPTION

The cathode follower (CF) is a nonlogic circuit which amplifies power. It has a voltage gain approaching 1. Since the cathode follower has high input and low output impedance, it is particularly useful as an isolating device. There are eight basic cathode follower models, identified by the letters B through H and J. Each model contains two $_{x}$CF circuits. When two circuits of different models are paired, the designations B and F, D and G, etc., are used. The representative cathode follower logic block symbol appears in figure 3–1.

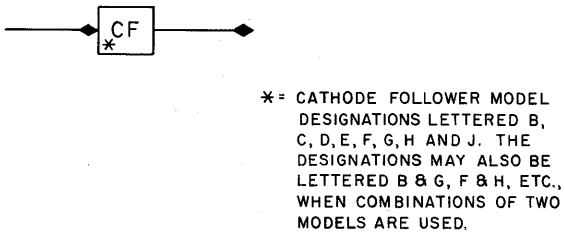


Figure 3–1. Cathode Follower, Logic Block Symbol

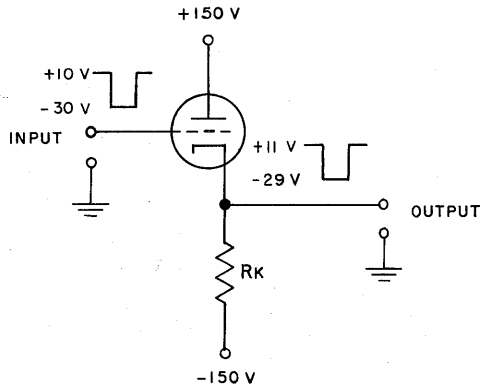


Figure 3–2. Cathode Follower, Simplified Schematic Diagram

1.2 PRINCIPLES OF OPERATION

Figure 3–2 is a simplified circuit schematic diagram of a cathode follower. The cathode follower output is produced across load resistor R_k, which is returned to the —150-volt supply.

A +10-volt level applied to the cathode follower grid causes a rise in plate current flowing through R_k. The increased voltage drop across R_k makes the cathode (output) more positive. A —30-volt level applied to the grid causes a decrease in plate current through R_k, making the output less positive. Although the cathode follower output voltage approaches its input voltage, the voltage gain is always less than 1. The level shift caused by cathode buildup, inherent in cathode followers, produces an output level more positive than the input level (see input and output waveforms in fig. 3–2). However, because of its large input and small output impedance, the cathode follower produces a power gain. The examples that follow show arithmetically the power amplification of a cathode follower.

Note

The values of impedances and potentials used in the examples are nominal, and input and output level potentials are assumed to be equal.

$$Z_{in} \text{ (input impedance)} = 10 \text{ meg}$$
$$Z_{out} \text{ (output impedance)} = 10\text{K}$$
$$E_{in} \text{ (input level)} = 10 \text{ volts}$$
$$E_{out} \text{ (output level)} = 10 \text{ volts}$$

$$\text{Power in} = \frac{E^2_{in}}{Z_{in}} = \frac{10^2}{10 \times 10^6} = \frac{100}{10{,}000{,}000} =$$
$$10 \times 10^{-6} = 10 \text{ microwatts}$$

$$\text{Power out} = \frac{E^2_{out}}{Z_{out}} = \frac{10^2}{10 \times 10^3} = \frac{100}{10{,}000} =$$
$$10 \times 10^{-3} = 10{,}000 \text{ microwatts}$$

$$\text{Power gain} = \frac{\text{Power Out}}{\text{Power In}} = \frac{10{,}000}{10} = 1000$$

The eight cathode follower models differ basically in the value of R_k for each model. The models, model

combinations, and associated types must meet certain load requirements, the load in many cases being resistive and capacitive. Figure 3–3 is a simplified circuit

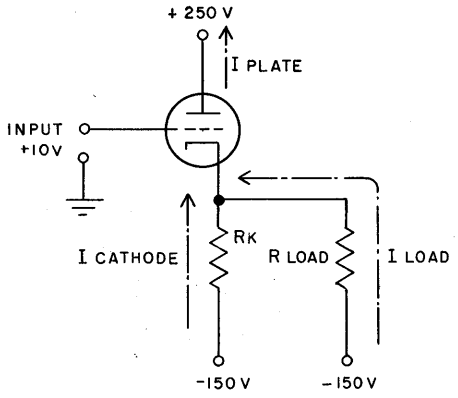


Figure 3–3. Cathode Follower with Resistive Load, Simplified Schematic Diagram

schematic diagram of a cathode follower and of a representative resistive load. The plate current is the sum of cathode and load currents; therefore, the load current equals the plate current minus the cathode current.

$$I_{plate} = I_{cathode} + I_{load}$$

$$\text{and } I_{load} = I_{plate} - I_{cathode}$$

Maximum load current results from minimizing cathode current by employing a large value of R_k.

The load also has an inherent capacitance which, although not a physical capacitor, nevertheless exists. A simplified circuit schematic diagram of a cathode follower with a capacitive load is shown in figure 3–4. When a —30-volt level is applied to the cathode follower grid, the capacity charges to —30 volts.

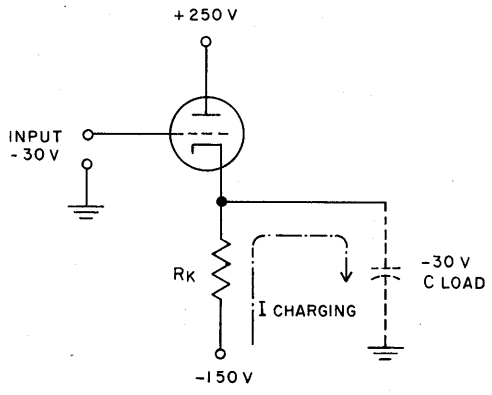


Figure 3–4. Cathode Follower with Capacitive Load, Simplified Schematic Diagram

Since the charging current (electron flow) necessary to establish a —30-volt level on this capacity flows through R_k, the charging time required to reach this potential is a function of the resistor value of R_k. Hence the lower the value of R_k, the shorter this charging (fall) time.

A large value of R_k is desirable when driving a resistive load, and a small value of R_k makes for a last fall time where a capacitive load is considered. It therefore follows that the value of R_k may be selected to produce an optimum condition for either of the two load conditions, or a compromise value may be decided upon to satisfy a resistive, capacitive load.

A circuit schematic of the $_{C}$CF is shown in figure 3–5A. Table 3–1 is the associated list of detail parts and their functions. The basic operation of a $_{C}$CF is the same as that of the simplified cathode follower discussed previously.

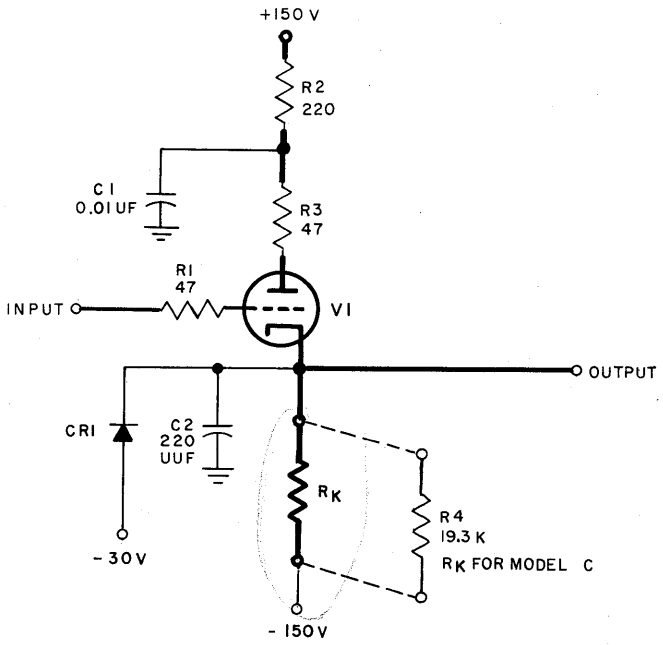
The $_{C}$CF circuitry shown in the diagram contains all the components found in a particular cathode follower model. A general discussion of these components follows:

TABLE 3–1. CATHODE FOLLOWER, MODEL C, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Part of decoupling network (with R2).
C2	Increases cathode-follower fall time.
CR1	Clamps V1 cathode at —30 volts.
R1	Parasitic suppressor.
R2	Part of decoupling network (with C1).
R3	Parasitic suppressor.
R4	Cathode resistor for V1.
V1	Cathode-follower vacuum tube.

For a particular cathode-follower model, there is a definite value of R_k, the reference symbol being R4. The cathode-resistor values for all cathode-follower models are indicated in figure 3–5B. These resistors are inserted in the cathode of their associated cathode follower as indicated in figure 3–5.

Components CR1 and C2 may be present in the cathode-follower circuitry, depending upon the particular cathode follower model and type. Catcher diode CR1 has a safety function: it "catches" the cathode at —30 volts, thereby preventing it from becoming more negative than this potential if the vacuum-tube filament should open or the plate supply voltage fail. Capacitor



A CATHODE FOLLOWER, MODEL C, SCHEMATIC DIAGRAM

MODEL	R_K	MODEL	R_K
B	R4 17.1 K	F	R4 27.8 K
C	R4 19.3K	G	R4 33.0K
D	R4 21.2K	H	R4 40.1 K
E	R4 24.0K	J	INFINITE

B. R_K FOR MODELS B THROUGH H AND J

Figure 3–5. Cathode Followers, Models B through H and J, Schematic Diagram

C2 is used only when a delay in fall time is required. Parasitic suppressor resistors R1 and R3 and decoupling networks C1 and R2 are common to most circuits.

Although there are many cathode-follower models and types, only the CF is discussed because it contains all the components found in the other models. Refer to table 3–1 for the function of detail parts not discussed.

CHAPTER 2

D-C LEVEL SETTER

2.1 DEFINITION AND DESCRIPTION

The models A and B d-c level setters, ($_{x}$LA), shown in logic block symbols in figure 3–6, are nonlogic circuits which restore signal levels to their nominal +10- and −30-volt upper and lower limits. Figure 3–7 is a graphic presentation of the typical input and output levels of a level setter. The input levels are plotted to the same time base as the restored output level. In addition to level restoration, the rise and fall times have been shortened. Incorrect levels are the results of level variations as the signal passes through various circuits. Level setters are introduced at points where levels deviate markedly from their +10- and −30-volt levels, eliminating the possibility of logic failure due to improper levels.

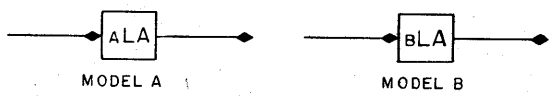


Figure 3–6. D-C Level Setters, Logic Block Symbols

The two models of level setters differ in the minimum input level requirements and rise and fall time restoration. Table 3–2 presents the maximum and minimum input level requirements. It will be seen that the $_{A}$LA operates over a wider range of input levels and

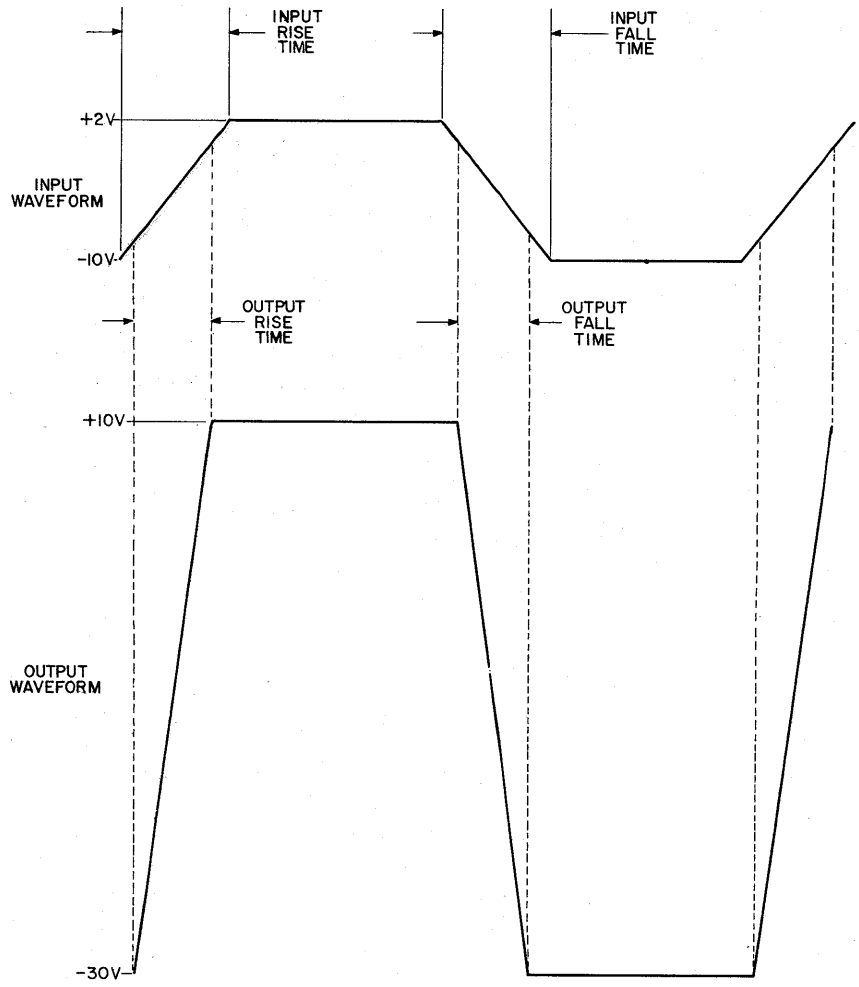


Figure 3–7. Input and Output Levels of a D-C Level Setter

TABLE 3–2. MAXIMUM AND MINIMUM INPUT LEVELS FOR D-C LEVEL SETTER MODELS A AND B

	MODEL			
	$_{A}$LA		$_{B}$LA	
LEVEL	MAX	MIN	MAX	MIN
Upper	+12 volts	0 volt	+12 volts	+6 volts
Lower	−30 volts	−8 volts	−30 volts	−11 volts

that the $_{B}$LA has the advantage of producing a faster rise and fall time.

2.2 PRINCIPLES OF OPERATION

2.2.1 Basic Operation

Figure 3–8 is a block diagram of a d-c level setter. It consists of two cathode followers and a grounded grid amplifier. Figure 3–9 is a simplified circuit schematic of a grounded grid amplifier. An input level is applied to the cathode, and the grid is grounded. When the input level is positive with respect to ground, the grid (maintained at ground potential) is effectively negative with respect to the cathode. This causes the plate current flowing through R to decrease, raising the plate potential to a value approaching B+. When the input drops to a negative potential, the grid is effectively positive with respect to the cathode. Plate current increases, dropping the plate potential in a negative direction.

A positive input results in a more positive output, and a negative input results in a less positive output. Thus the output of a grounded grid amplifier is amplified and in phase with the input.

A level applied to the level setter input cathode follower is matched to the input of the grounded grid amplifier. The grounded grid amplifier amplifies this level and, in turn, drives the output cathode follower, which is alternately clamped at +10- and −30-volt levels. (See fig. 3–8.)

2.2.2 Detailed Operation, Model A Level Setter

Figure 3–10 is a schematic diagram of a model A level setter. Table 3–3 is the associated list of detail parts and their functions. When the level at the grid of input cathode follower V1A is −8 volts, the cathode falls to this potential. The cathode of grounded grid amplifier V1B is also at a −8-volt potential because the cathodes of V1A and V1B are common. A voltage divider consisting of resistors R4 and R6 between ground and −15 volts places the grid of V1B at a −4-volt potential. The grid of V1B is positive with respect to its cathode (at −8 volts). This produces a current flow which drops the plate potential of V1B to +66 volts. A difference of potential of 366 volts across the divider consisting of resistors R7 and R8 would produce a potential of −58 volts at the grid of output cathode follower V2A. However, the grid of V2A is never more negative than −35 volts because of the clamping action of diode CR1. Diode CR3 clamps the cathode of V2A at −30 volts. Cathode resistors R11 and R12 form a voltage divider between −30 volts and −150 volts, placing the anode of CR1 at a potential of −35 volts. The grid of V2A is therefore clamped at −35 volts, preventing the cutoff of V2A on negative excursions.

When the level at the grid of the input cathode follower V1A is +2 volts, the cathodes of V1A and

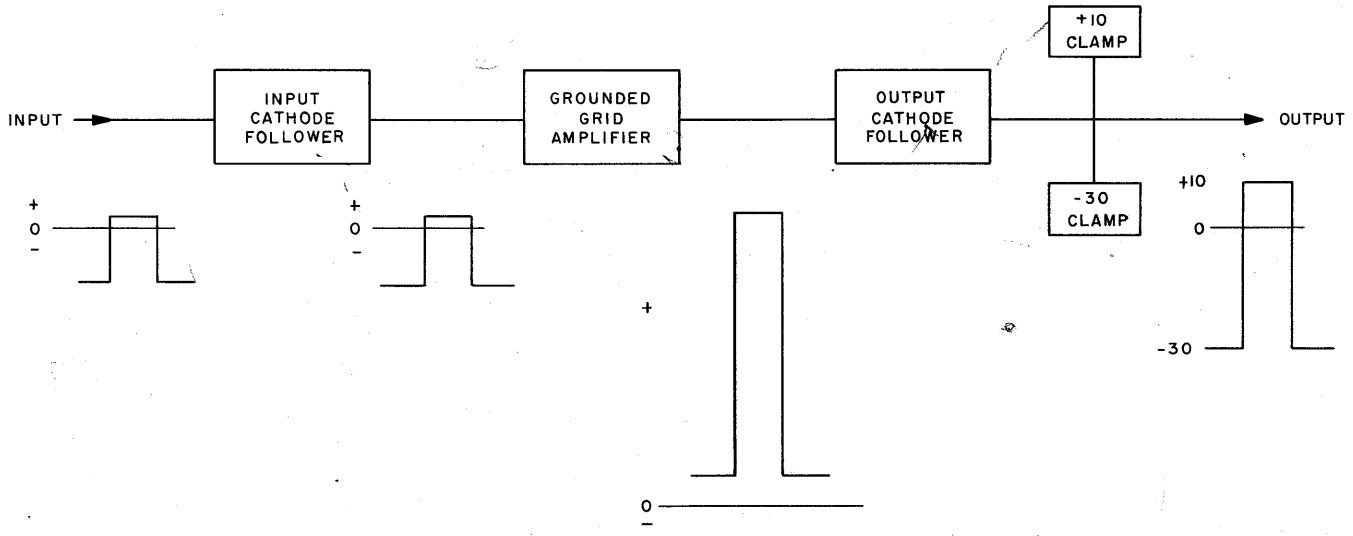


Figure 3–8. D-C Level Setter, Block Diagram

TABLE 3–3. D-C LEVEL SETTER, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Bypass capacitor.
C2	Speeds rise and fall time.
CR1	Clamps grid of V2A to −35 volts.
CR2	Clamps cathode of V2A to +10 volts.
CR3	Clamps cathode of V2A to −30 volts.
R1	Parasitic suppressor.
R2	Cathode load for V1A.
R3	Plate load resistor for V1B.
R4	Part of voltage divider biasing network (with R6).
R5	Parasitic suppressor.
R6	Part of voltage divider biasing network (with R4).
R7	Part of voltage divider (with R8).
R8	Part of voltage divider (with R7).
R9	Parasitic suppressor.
R10	Current limiting resistor, protects CR2.
R11	Part of V2A cathode load (with R12) and voltage divider for CR1 bias.
R12	Part of V2A cathode load (with R11) and voltage divider for CR1 bias.
V1A	Input cathode follower.
V1B	Grounded grid amplifier.
V2A	Output cathode follower.

grounded grid amplifier V1B rise to +2 volts. With −4 volts on the grid of V1B and +2 volts on the cathode, V1B is cut off. The voltage divider formed by resistors R3, R8, and R7 across a 550-volt potential sets the VIB plate potential at +200 volts. The divider formed by resistors R8 and R7 between +200 volts and −300 volts would produce a potential of +31 volts at the grid of output cathode follower V2A were it not for the following: the cathode of V2A is clamped to +10 volts by diode CR2; a potential more positive than +10 volts at the grid of V2A causes grid current to flow; the grid, therefore, cannot become more positive than +10 volts.

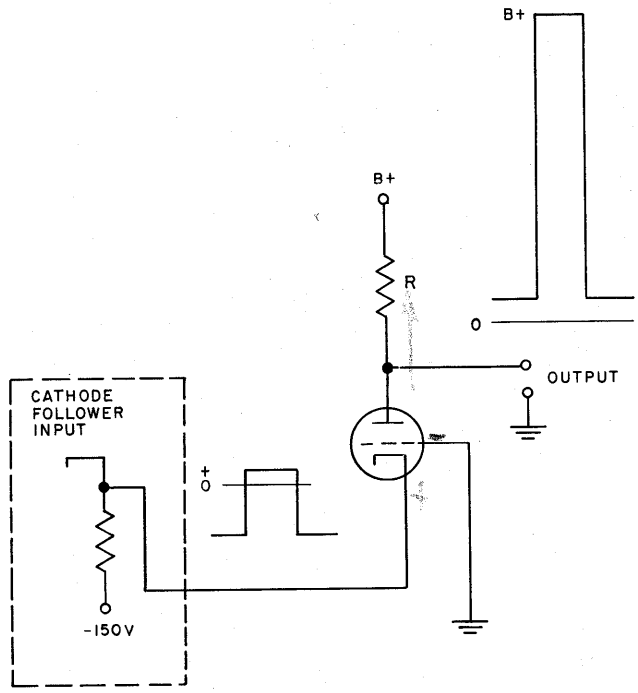


Figure 3–9. Grounded Grid Amplifier, Simplified Schematic Diagram

In addition to re-establishing levels, the level setters also improve the transition (rise and fall) time. Compensating capacitor C2 speeds up the rise and fall of the levels applied to the grid of V2A. Refer to table 3–3 for the function of detail parts not discussed.

2.2.3 Detailed Operation, Model B Level Setter

Figure 3–11 is a schematic diagram of the $_{B}$LA. Table 3–4 is the associated list of detail parts and their functions. If the model B schematic is compared with the model A (fig. 3–10), certain circuit variations are noted. Cathode voltage divider resistor R4 and speedup capacitor C2 have been added to the cathode of V1A, while R5 has been reduced in value. The cathode of V1B is tied to the junction of resistors R4 and R5. The values of voltage divider biasing resistors R8 and R10 have been interchanged, increasing the V1B bias from −4 to −10.4 volts. Bypass capacitor C3 has increased in value, and resistor R12 has decreased.

The variations noted in the $_{B}$LA increase the speed of rise and fall times slightly over the $_{A}$LA. This gain in speed, however, results in a more limited input level requirement than that in the $_{A}$LA. Refer to table 3–4 for the function of detail parts not discussed.

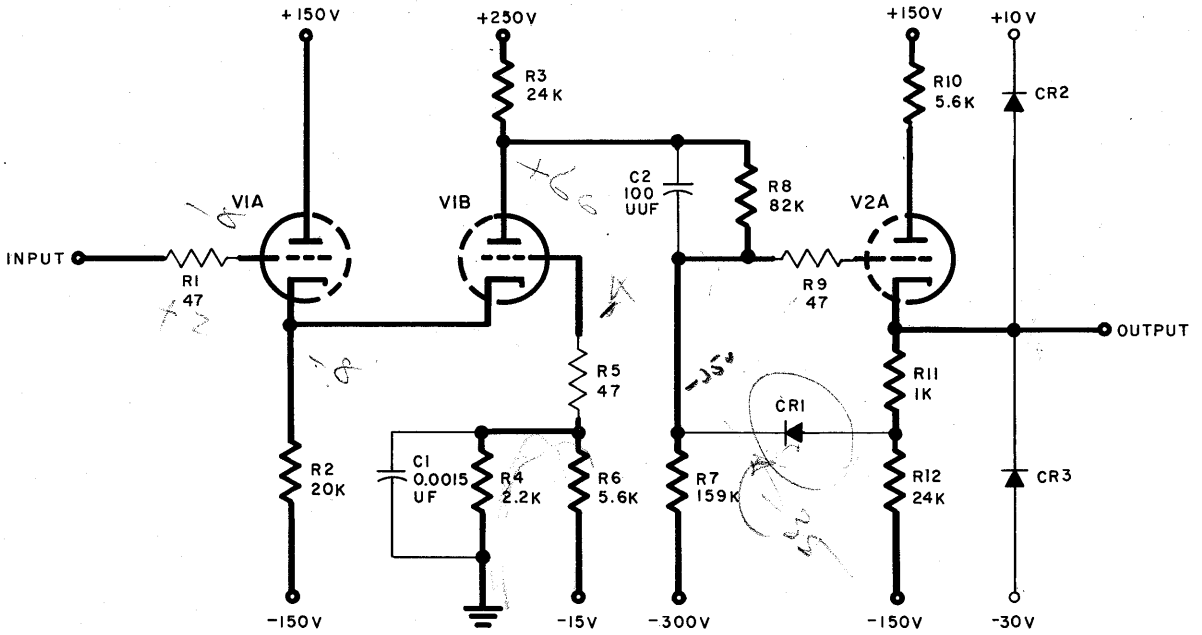


Figure 3–10. D-C Level Setter, Model A, Schematic Diagram

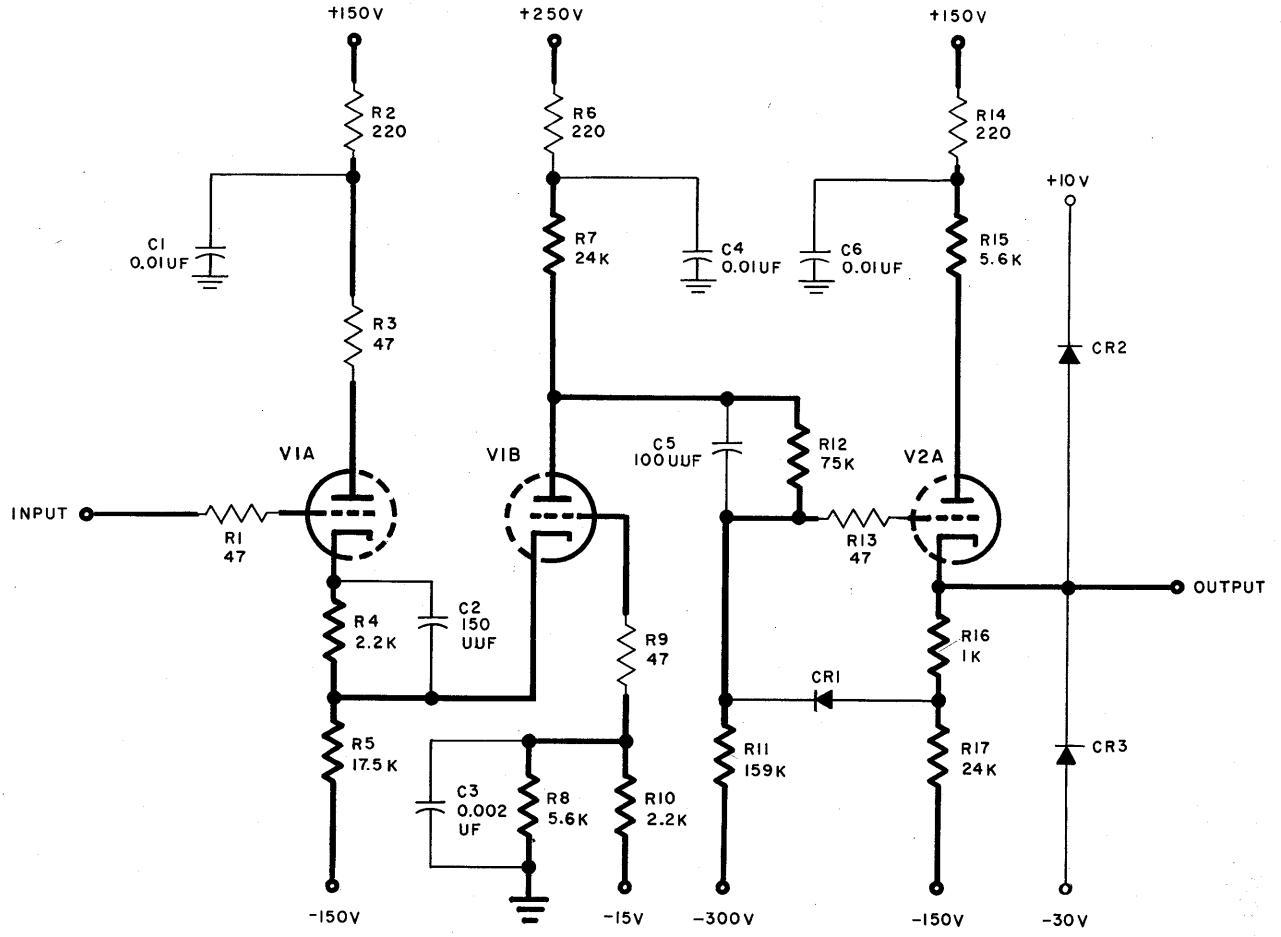


Figure 3–11. D-C Level Setter, Model B, Schematic Diagram

TABLE 3–4. D-C LEVEL SETTER, MODEL B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Part of decoupling network (with R2)
C2	Speeds rise and fall time.
C3	Bypass capacitor.
C4	Part of decoupling network (with R6).
C5	Speeds rise and fall time.
C6	Part of decoupling network (with R14).
CR1	Clamps grid of V2A to −35 volts.
CR2	Clamps cathode of V2A to +10 volts.
CR3	Clamps cathode of V2A to −30 volts.
R1	Parasitic suppressor.
R2	Part of decoupling network (with C1).
R3	Parasitic suppressor.
R4	Part of V1A cathode load (with R5).
R5	Part of V1A cathode load (with R4).
R6	Part of decoupling network (with C4).
R7	Plate load resistor for V1B.
R8	Part of voltage divider (with R10).
R9	Parasitic suppressor.
R10	Part of voltage divider (with R8).
R11	Part of voltage divider (with R12).
R12	Part of voltage divider (with R11).
R13	Parasitic suppressor.
R14	Part of decoupling network (with C6).
R15	Current limiting resistor, protects CR2.
R16	Part of V2A cathode load (with R17) and voltage divider for CR1 bias.
R17	Part of V2A cathode load (with R17) and voltage divider for CR1 bias.
VIA	Input cathode follower.
VIB	Grounded grid amplifier.
V2A	Output cathode follower.

CHAPTER 3

PULSE AMPLIFIERS, MODELS A, B, AND C

3.1 DEFINITION AND DESCRIPTION

The pulse amplifiers (PA's) are nonlogic circuits and are represented in complete logic schematics by the logic block symbols in table 3–5. Pulse amplifiers are employed to increase the load-driving capabilities (to amplify power) of a standard pulse. Three models of this circuit are employed to cover the range of loads that must be driven and are used separately or in combination, depending upon the specific load to be driven. Table 3–5 lists the three models and gives their logic block symbols and load-driving capabilities.

The differences between the models are in the point of connection of the suppressor grid and the value of plate voltage applied. In the $_{A}$PA, the suppressor is tied to +10 volts. This connection limits the maximum value of current through the pentode. Current-carrying capacity is increased in the $_{B}$PA by connecting the suppressor grid to the plate of the pentode and operating the tube as a tetrode-connected pentode. In the $_{C}$PA, a tetrode-connected pentode is employed, and the plate supply voltage is either +250 volts or +150 volts. Although the plate supply voltage is reduced by 100 volts, the tetrode connection of the $_{C}$PA provides sufficient current to drive loads below the capabilities of $_{A}$PA. When greater output is required, a +250-volt plate return is employed. One other major difference between the $_{C}$PA and the others ($_{A}$PA and $_{B}$PA) is in the termination requirements. The $_{A}$PA and the $_{B}$PA drive constant loads. The terminating resistor satisfies the minimum load requirements for each load the circuit drives and will be different for each load. The $_{C}$PA can satisfy termination requirements for a varying load (no load to maximum load in any one application) while using only one value of terminating resistor. Thus, the three PA circuits are a versatile group, capable of driving a wide range of loads. Refer to the discussion of the register drivers in Chapter 4 for further modifications of this basic circuit which have increased the load carrying capacity to 34 load units.

Just as each model of the pulse amplifier is used to meet a specific range of load requirements, each model has variations (types) which are designed to meet specific input requirements for a given loading. These type-distinguishing features are detailed in the input circuits in figures 3–12, 3–13, and 3–14, and are discussed in 3.3.

3.2 PRINCIPLES OF OPERATION

3.2.1 Basic Considerations

The basic parts of the pulse amplifier are a pentode vacuum tube and a transformer. The pentode serves a power-amplifying function. The transformer provides the proper phase relationship at the output and, at the same time, serves an impedance matching function. This is accomplished by so connecting the transformer that a negative pulse at the plate of the pentode produces a positive pulse at the output. The transformer turns ratio of 4 to 1 provides an impedance stepdown of 16 to 1.

$$\frac{\text{output impedance}}{\text{input impedance}} = \left(\frac{\text{turns output}}{\text{turns input}}\right)^2$$

3.2.2 Detailed Operation

Figure 3–12 is a schematic diagram of the $_{A}$PA. Table 3–6 is the associated list of detail parts and their functions. A standard pulse applied to the input of the $_{A}$PA is coupled to the control grid of pentode V1 through capacitor C1. This capacitor allows signals at the input to pass to the grid while blocking the –15-volt d-c bias at the grid from the input circuit. The standard pulse overcomes the negative bias, which has held the grid of V1 considerably past cutoff, and tube V1 conducts. The resultant pulse of current produced in the plate circuit of V1 is transformer-coupled to the output through T1. This transformer, with a 4-to-1 turns

TABLE 3–5. PULSE AMPLIFIER, LOGIC BLOCK SYMBOLS AND LOAD-DRIVING CAPABILITIES

NAME	LOGIC BLOCK SYMBOL	LOAD DRIVING CAPABILITIES
Pulse amplifier, model A	→ $_{A}$PA →	Constant light load (2 to 8 units of load)
Pulse amplifier, model B	→ $_{B}$PA →	Constant heavy load (5 to 11 units of load)
Pulse amplifier, model C	→ $_{C}$PA →	Varying light load (0 to 3 units of load)

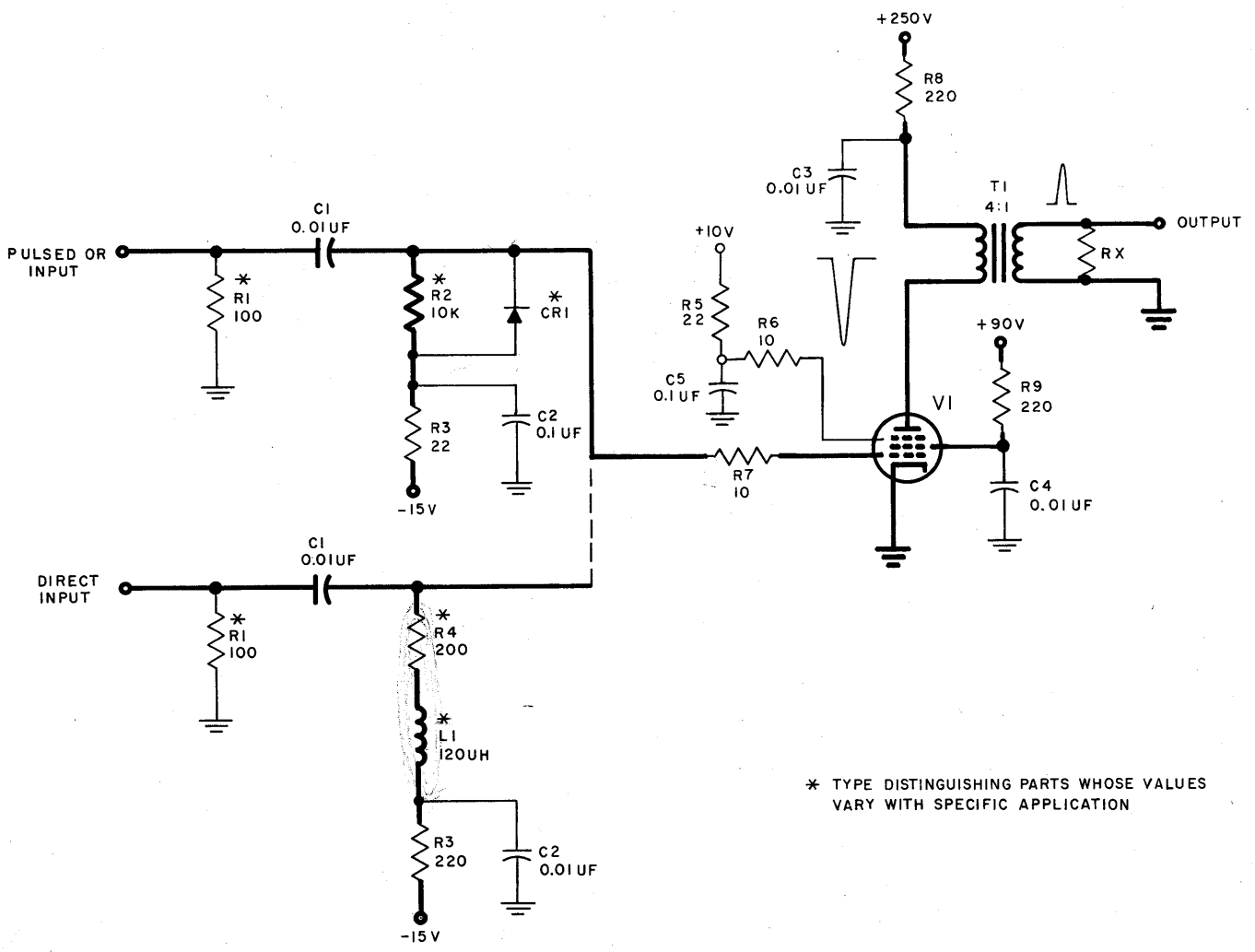


Figure 3–12. Pulse Amplifier, Model A, Schematic Diagram

ratio, steps down the voltage at the secondary (output) to ¼ of that appearing at the primary. The output current, in turn, is 4 times that appearing in the primary. Transformer T1 is connected to produce a positive pulse at the secondary (output) as a result of a current pulse in the primary. Thus a standard pulse applied to the input of PA appears as a standard pulse at the output. The $_{A}$PA, a nonlogic circuit, amplifies the power of the input pulse but does not otherwise change the standard pulse characteristics.

The pulse amplifier may be used to drive delay lines. For this application, the screen grid is returned to +90 volts, and the suppressor grid is returned to +90 volts through a 470-ohm resistor.

3.3 INPUT CIRCUIT VARIATIONS

Figures 3–12, 3–13, and 3–14 illustrate the input circuit variations for each model. Tables 3–7 and 3–8 are the associated lists of detail parts and their functions for figures 3–13 and 3–14, respectively. A comparison of the figures reveals the close similarity between the type-distinguishing parts for each model. Therefore, only the input circuits to the $_{A}$PA will be discussed.

The input circuits are classified in two groups: the pulsed OR and the direct. Consider the network used with the pulsed OR input, and note that this network has the same configuration in each schematic. The parallel combination of R2 and CR1 serves two functions: resistor R2 provides a high-resistance load for the input pulse, and CR1 provides a low-resistance discharge path for capacitor C1, preventing bias buildup on the control grid. The series connection of R4 and L1 used with the direct input type $_{A}$PA ensures the return of the control grid to −15 volts shortly after the standard pulse at the input returns to 0. Inductor L1 presents a high impedance to a rapidly changing voltage, ensuring an undistorted coupling of the input pulse to the grid. Thus the high impedance to pulses and the low impedance to dc of L1 ensure a rapid response of the control grid to input pulses and quick recovery to the control grid bias level to prepare the circuit for the next pulse.

TABLE 3–6. PULSE AMPLIFIER, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Input coupling capacitor.
C2	Part of decoupling network (with R3).
C3	Part of decoupling network (with R8).
C4	Part of decoupling network (with R9).
C5	Part of decoupling network (with R5).
CR1	Provides low-impedance discharge path for C1, preventing bias buildup.
L1	Peaking coil for input pulse.
R1	Input coaxial cable termination.
R2	Grid d-c return.
R3	Part of decoupling network (with C2).
R4	Damping resistor for inductor L1.
R5	Part of decoupling network (with C5).
R6	Parasitic suppressor.
R7	Parasitic suppressor.
R8	Part of decoupling network (with C3).
R9	Part of decoupling network (with C4).
Rx	Terminating resistor.
T1	Output transformer.
V1	Power amplifier electron tube.

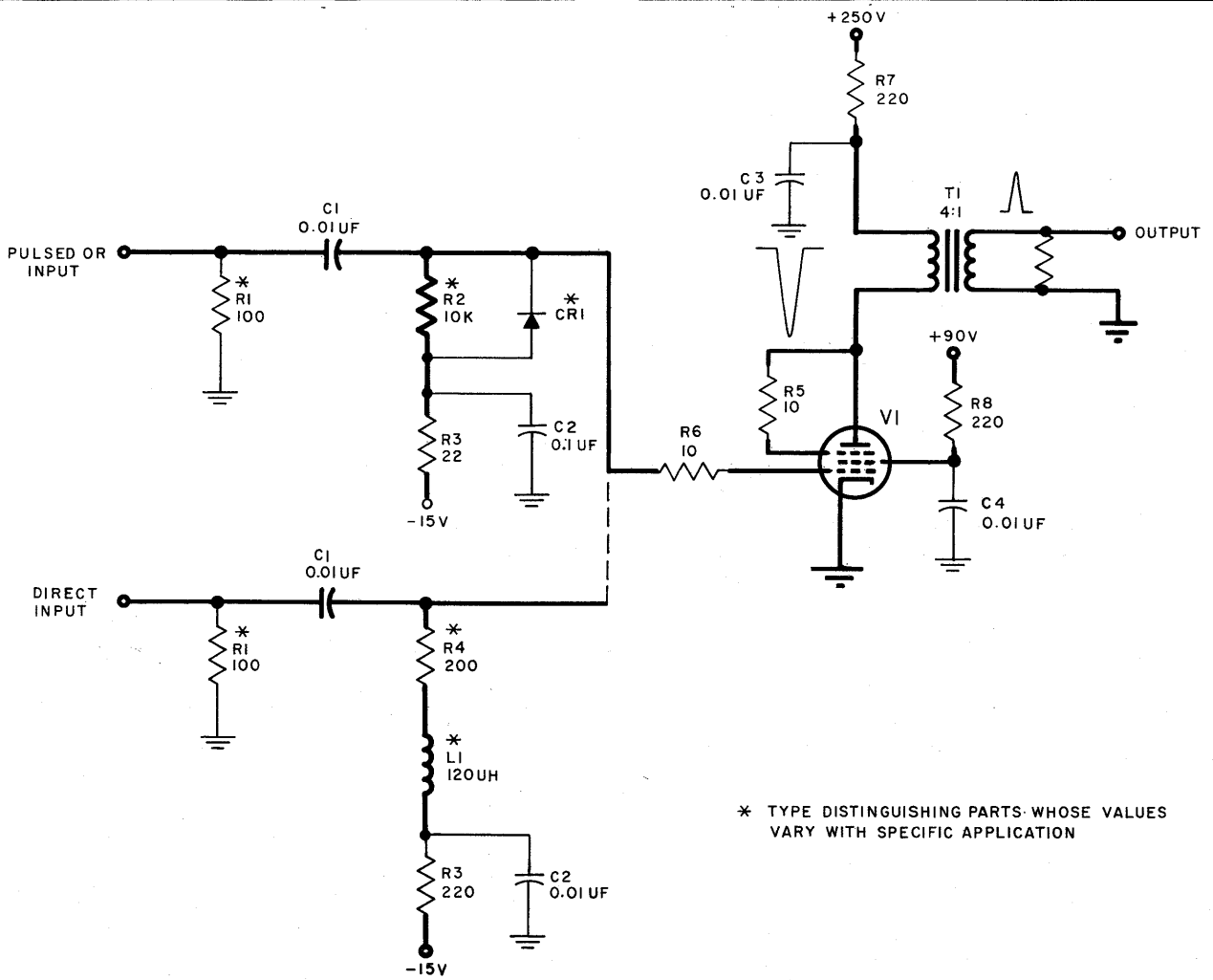


Figure 3–13. Pulse Amplifier, Model B, Schematic Diagram

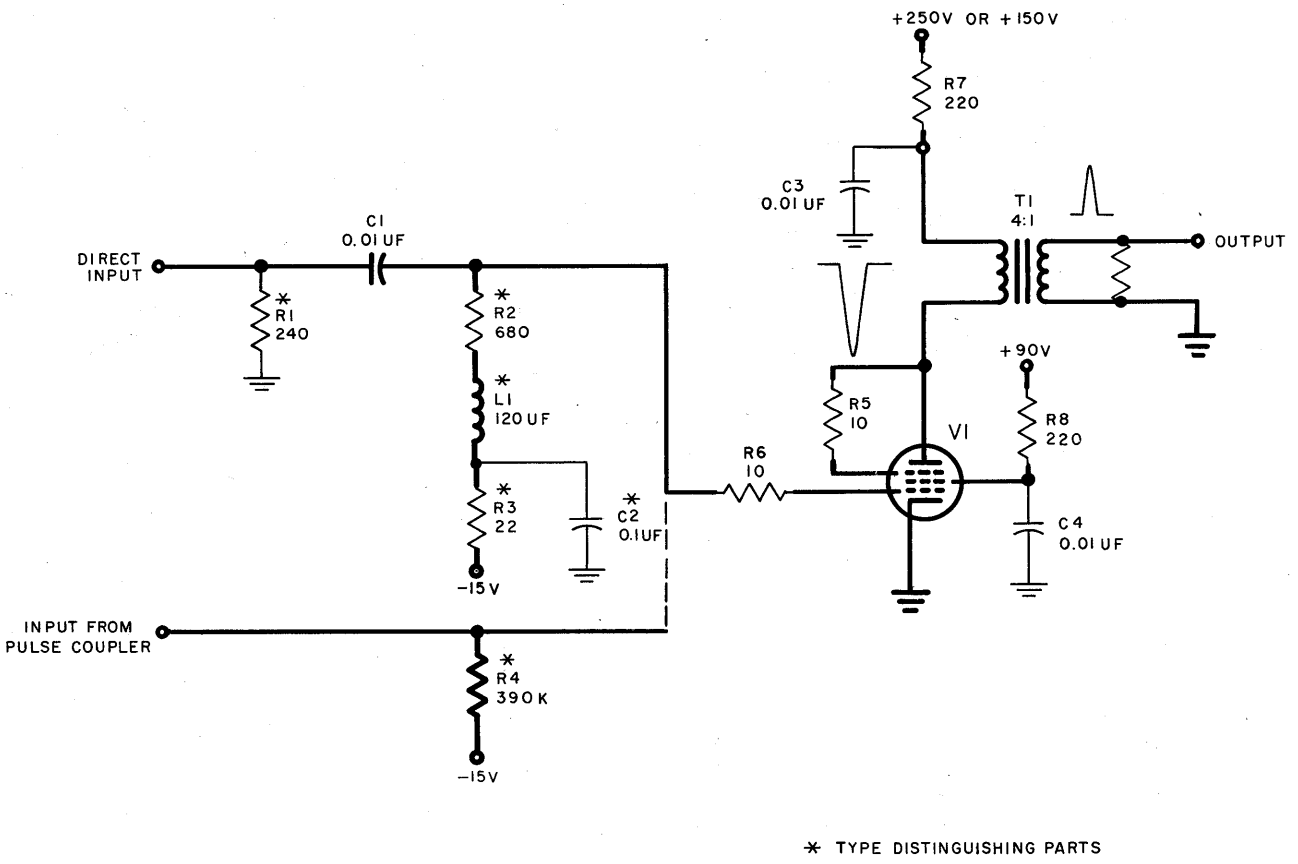


Figure 3–14. Pulse Amplifier, Model C, Schematic Diagram

TABLE 3–7. PULSE AMPLIFIER, MODEL B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Input coupling capacitor.
C2	Part of decoupling network.
C3	Part of decoupling network.
C4	Part of decoupling network.
CR1	Provides low-impedance discharge path for C1, preventing bias buildup.
L1	Peaking coil for input pulse.
R1	Input coaxial cable termination.
R2	Grid return.
R3	Part of decoupling network (with C2).
R4	Damping resistor for inductor L1.
R5	Parasitic suppressor.
R6	Parasitic suppressor.
R7	Part of decoupling network (with C3).
R8	Part of decoupling network (with C4).
Rx	Terminating resistor.
T1	Output transformer.
V1	Power amplifier electron tube.

TABLE 3–8. PULSE AMPLIFIER, MODEL C, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Input cooling capacitor.
C2	Decoupling network (with R3).
C3	Decoupling network (with R7).
C4	Decoupling network (with R8).
L1	Peaking inductor for input pulse.
R1	Input coaxial cable termination.
R2	Damping resistor for inductor L1.
R3	Decoupling network (with C2).
R4	Grid return.
R5	Parasitic suppressor.

TABLE 3–8. PULSE AMPLIFIER MODEL C, FUNCTION OF DETAIL PARTS (Cont'd)

REFERENCE SYMBOL	FUNCTION
R6	Parasitic suppressor.
R7	Decoupling network (with C3).
R8	Decoupling network (with C4).
Rx	Terminating resistor.
V1	Power amplifier electron tube.

Resistor R1 connected across the input is not properly a part of the pulse amplifier circuit. It terminates coaxial lines connected between the driver and the pulse amplifier. The requirement for a close physical proximity to the pulse amplifier dictates its inclusion in the pulse amplifier assembly. Refer to tables 3–6, 3–7, and 3–8 for the function of detail parts not discussed.

CHAPTER 4
REGISTER DRIVERS, MODELS A AND B

4.1 DEFINITION AND DESCRIPTION

The register drivers ($_{X}$RD) are nonlogic circuits used to increase the load-driving capabilities (to amplify power) to a standard pulse. Table 3–9 lists the models by name with their logic block symbols and load-driving capabilities. The register drivers are essentially model B pulse amplifiers (see Ch. 3) with extended load-driving capabilities. There are two models: the $_{A}$RD is a $_{B}$PA with a transformer input circuit; the $_{B}$RD is a parallel input combination of two $_{B}$PA's with a single transformer feeding the inputs.

4.2 PRINCIPLES OF OPERATION

4.2.1 Basic Considerations

Figure 3–15 is a circuit schematic for both models of the register driver. Table 3–10 is the associated list of detail parts and their functions. As indicated, the $_{A}$RD is converted into a $_{B}$RD by connecting two identical pentode circuits to the output terminal of input transformer T1. The $_{B}$RD connection is shown by the dashed line. As with the pulse amplifier, a standard pulse input produces a standard pulse output. Transformer T1 is connected to produce a positive pulse output three times the amplitude of a standard pulse input. As a result, a standard pulse impressed on the primary appears as a positive potential at the control grid of V1. Tube V1 produces a pulse of current, and transformer T2 delivers a standard output. With proper termination, this standard pulse has much greater drive capabilities (power). Thus the register driver, a nonlogic circuit, power-amplifies standard pulses.

4.2.2 Detailed Operation

The input of the $_{A}$RD (see fig. 3–15) is fed a standard pulse. Transformer T1 amplifies this input three times and, in addition, provides a low-impedance d-c path for the grid bias of —30 volts and isolates the driving (preceding) circuit from the d-c grid bias voltage source. The —30-volt bias maintains the control grid of V1 far below cutoff. This prevents undesirable positive noise pulses, generated in the associated circuit by ringing and mismatch, from driving V1 into conduction.

The other detail parts in the input circuit serve a matching function and minimize effects of ringing in the secondary winding of T1. The parallel combination of resistor R1 and inductor L1 compensates for the mismatch under two conditions of loading in the secondary circuit. Because of ringing, a standard pulse applied to T1 tends to appear as a positive pulse with a large negative overshoot. During the positive pulse, V1 is driven past the point of initial grid conduction. The load across the secondary winding, during this period of grid conduction, is the series combination of resistor R4 and the grid to cathode resistance of V1. During the negative overshoot, current flows in the opposite direction through a load consisting of the forward resistance of CR1 and R3. Inductor L1 and resistor R1 supplement these loads to provide optimum termination for the coaxial input line feeding the primary of T1. The series combination of diode CR1 and resistor R3 limits the magnitude of the negative overshoot to a value approximately equal to the voltage drop across R3. If CR1 were used alone, the negative overshoot would be further limited, but the recovery time of the diode (return of grid to —30 volts) might be slower than the repetition rate of the pulses. Since the diode recovery is a function of the current through it, the addition of R3 speeds up the process by limiting the magnitude of current during diode conduction.

The positive pulse of voltage appearing at the secondary of T1 overcomes the —30-volt bias and causes grid current to flow. Grid-limiting resistor R4 prevents this current from becoming excessive. The grid of V1 is

TABLE 3–9. REGISTER DRIVERS, LOGIC BLOCK SYMBOLS AND LOAD-DRIVING CAPABILITIES

NAME	LOGIC BLOCK	LOAD-DRIVING CAPABILITIES
Register driver, model A	→ $_{A}$RD →	1–17 flip-flops or gate tubes with suitable termination resistor.
Register driver, Model B	→ $_{B}$RD →	17–34 flip-flops or gate tubes with suitable termination resistor.

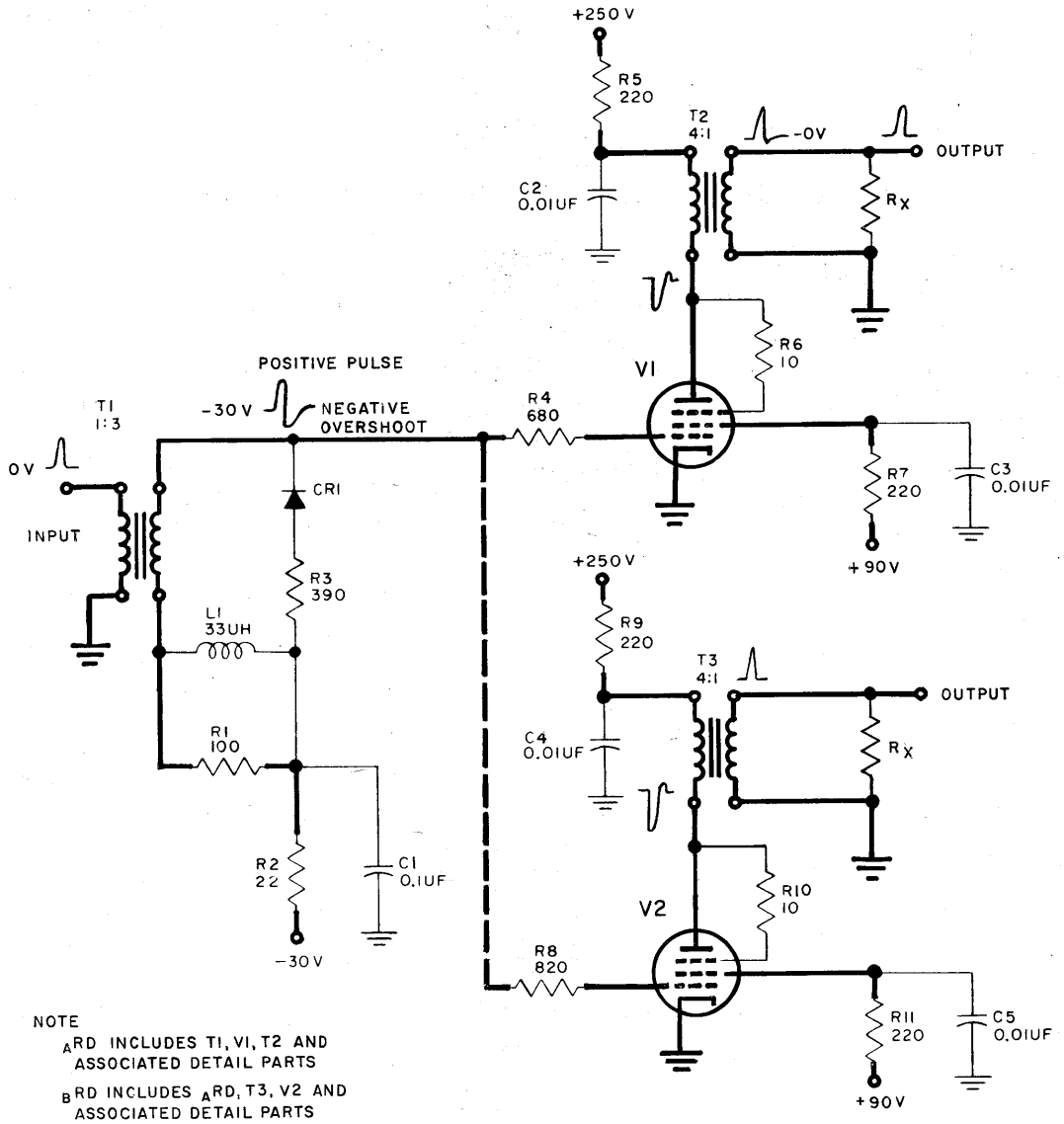


Figure 3–15. Register Driver, Models A and B, Schematic Diagram

TABLE 3–10. REGISTER DRIVERS, MODELS A AND B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	USED ON MODEL	FUNCTION
C1	AB	Forms decoupling network for V1 and V2 grid bias return (with R2).
C2	AB	Forms decoupling network for V1 plate return (with R5).
C3	AB	Forms decoupling network for V1 screen grid return (with R7).
C4	AB	
C5	AB	Forms decoupling network for V2 screen grid return (with R11).
CR1	AB	Damps negative overshoot.
L1	AB	Forms a matching network for terminating coaxial line input (with R1).
R1	AB	Forms a matching network for terminating coaxial line input (with L1).

TABLE 3—10. REGISTER DRIVERS, MODELS A AND B, FUNCTION OF DETAIL PARTS (Cont'd)

REFERENCE SYMBOL	USED ON MODEL	FUNCTION
R2	AB	Forms decoupling network for V1 and V2 grid bias return (with C1).
R3	AB	Speeds up recovery of CR1.
R4	AB	Grid current limiting resistor.
R5	AB	Forms decoupling network for V1 plate return (with C2).
R6	AB	Parasitic suppressor.
R7	AB	Forms decoupling network for V1 screen return (with C3).
R8	B	V2 grid limiting resistor.
R9	B	Forms decoupling network for V2 plate return (with C4).
R10	B	Parasitic suppressor.
R11	B	Forms decoupling network for screen grid return (with C5).
RX	AB	Load-compensating resistor (variable value).
T1	AB	Input transformer amplifies input pulse in voltage and matches grid circuit to input circuit.
T2	AB	V1 output transformer impedance-matching and pulse-forming.
T3	B	V2 output transformer impedance-matching and pulse-forming.
V1	A	Pentode vacuum tube.
V2	B	Pentode vacuum tube.

maintained at a reduced positive potential during this time, producing a pulse of current in the plate circuit of V1, which is converted into a standard pulse by transformer T2. This output transformer, in addition to pulse-forming, matches the low impedance of the load to the relatively high impedance of the plate of pentode V1. The value of Rx is a variable and depends on the load driven by the output transformer. Its selection enables a large variation in loads to appear relatively the same.

The $_{B}$RD (fig. 3—15) consists of the basic input circuit of the $_{A}$RD except for the addition of pentode V2 and associated detail parts in parallel with V1. The output circuit of the $_{B}$RD is identical with two $_{A}$RD's enabling the driving of twice the load of an $_{A}$RD (split).

Although the function of the $_{A}$RD is comparable with that of the $_{B}$PA, certain marked differences exist. The $_{A}$RD has much greater drive capabilities. This is accomplished by increased grid drive. To accommodate this increased drive and to limit noise, the grid bias is increased to —30 volts as compared with the —15-volt bias on the $_{B}$PA.

Refer to table 3—10 for the function of detail parts not discussed.

CHAPTER 5

THYRATRON RELAY DRIVERS, MODELS A AND B

5.1 DEFINITION AND DESCRIPTION

The thyratron relay drivers (RYD's) identified by the logic block symbols in table 3–11, are nonlogic circuits. They are used to provide the current necessary to energize duo-relays, print and punch magnets, and wire contact relays. The thyratron relay drivers are essentially current switches which are triggered (made to pass current) by a positive shift in standard level from −30 volts to +10 volts.

There are two models of the thyratron relay driver, A and B. Model A performs its function when one positive level shift is applied to its input. Model B performs its function with the application of a positive level shift, after a second input is conditioned with a positive level. Thus, when the logic requires that a specific relay be energized on every occurrence of a positive level shift, the $_{A}$RYD circuit is used between the source of the standard level shift and the specific relay. When the logic requires that a specific relay or magnet be energized each time a positive level shift occurs some time after a conditioning level, the $_{B}$RYD circuit is used. In this application, the $_{B}$RYD includes the function of a gate circuit (Ch. 9). These examples of one application for each circuit point out the specific difference between the two models: the $_{A}$RYD is controlled by one input; the $_{B}$RYD is controlled by two inputs.

In addition, each model on the thyratron relay driver occurs as one of two types: cathode-loaded ($_{A}$RYD, circuit 1, and $_{B}$RYD, circuit 1) and plate-loaded ($_{A}$RYD, circuit 2, and $_{B}$RYD, circuit 2). This designation, according to type, specifies the location of the relay or magnet in the thyratron circuit.

Table 3–11 lists the models of the thyratron relay drivers, giving their names, logic block symbols, and functional description.

5.2 PRINCIPLES OF OPERATION

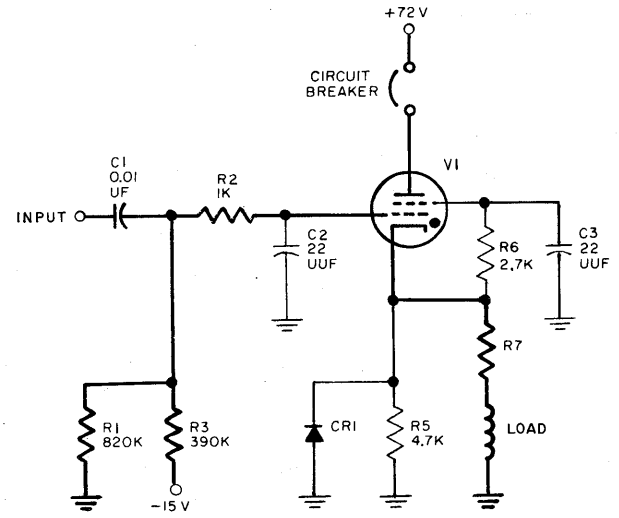
5.2.1 Basic Principles and Definitions

This paragraph presents a review of thyratron characteristics and defines the terms used to describe these characteristics, as an aid toward understanding the detailed circuit operation. Two basic considerations are involved in the operation of a thyratron circuit: the start of current and the extinction of current through the thyratron. For this reason, the RYD circuits are functionally divisible into the basic thyratron circuit and circuit refinements. The basic thyratron circuit consists of the thyratron and those detail parts that control the operation of the thyratron. The circuit refinements include those detail parts that serve a protective, isolating, and reliability function. The $_{A}$RYD and $_{B}$RYD schematic diagrams (figs. 3–16 and 3–17) indicate this distinction between the basic circuit and its refinements by the difference in line weight. The heavy lines are reserved for basic circuit elements. Table 3–12 is the associated list of detail parts and their functions for figures 3–16 and 3–17.

The thyratron used in the $_{A}$RYD and $_{B}$RYD is a gas-filled (Xenon) tetrode, containing a plate, cathode, control grid, and shield grid. The shield grid serves the function of a second control or input grid. The

TABLE 3–11. THYRATRON RELAY DRIVERS, LOGIC BLOCK SYMBOL AND FUNCTIONAL DESCRIPTION

NAME	LOGIC BLOCK SYMBOL	FUNCTIONAL DESCRIPTION
Thyratron relay driver, model A		A current switch which permits passage of current through a relay or magnet coil when triggered by a positive level shift from −30 volts to +10 volts.
Thyratron relay driver, model B		A current switch which permits passage of current through a relay or magnet each time a level shift from −30 volts to +10 volts is applied to one input, while the other input is conditioned with a +10-volt level.



CATHODE LOADED, CIRCUIT 1

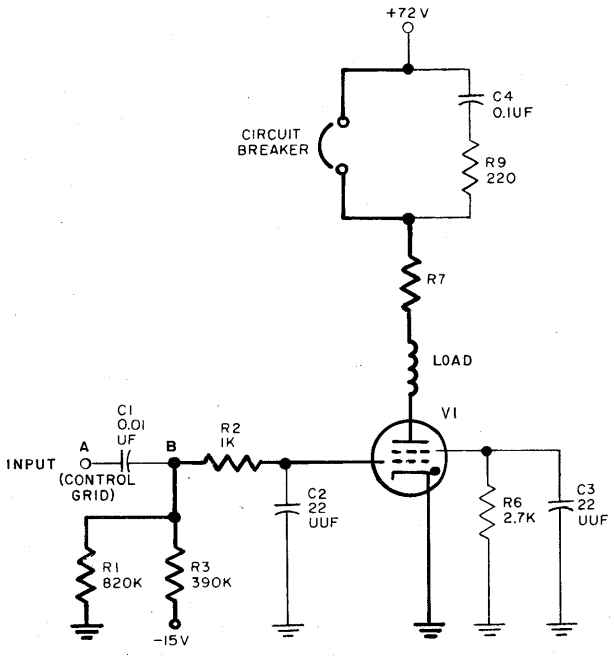
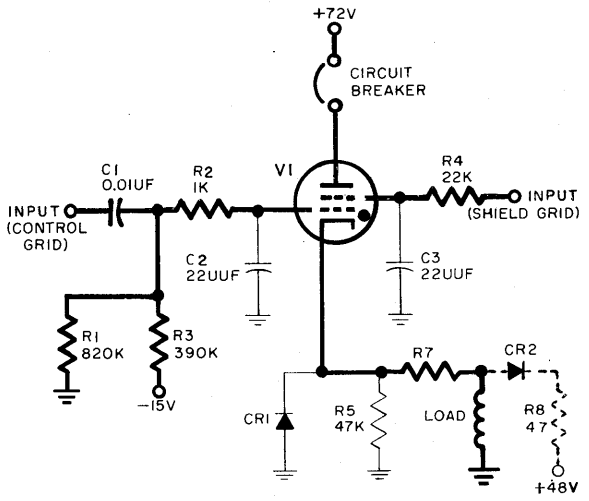


PLATE LOADED CIRCUIT 2

Figure 3–16. Thyratron Relay Driver, Model A, Schematic Diagram

other three elements are similar in function to their counterparts in a vacuum tube, except that the control grid loses control of plate current through the thyratron once conduction is started.

The two states of operation of the thyratron conducting and nonconducting are termed ionized and deionized, respectively. Ionization occurs when the potential between the anode and the cathode in a gas-filled thyratron is large enough to cause electrons to leave the cathode with sufficient energy to convert a gas molecule into an ion on impact. Such a potential between anode and cathode is termed the ionizing potential. Ionization occurs in a thyratron whenever the anode voltage is equal to, or greater than, the ionizing potential, and the control grid voltage is equal to, or greater than, a specified value termed the critical grid voltage. Once the thyratron is ionized, positive ions form a sheath around the control grid and cause this grid to lose control of current through the thyratron. The magnitude of the current, then depends on the load in the anode or cathode circuit of the thyratron. The thyratron may be deionized (made nonconducting) only by reducing the ionizing potential below a value termed the extinction voltage.



CATHODE LOADED CIRCUIT 1

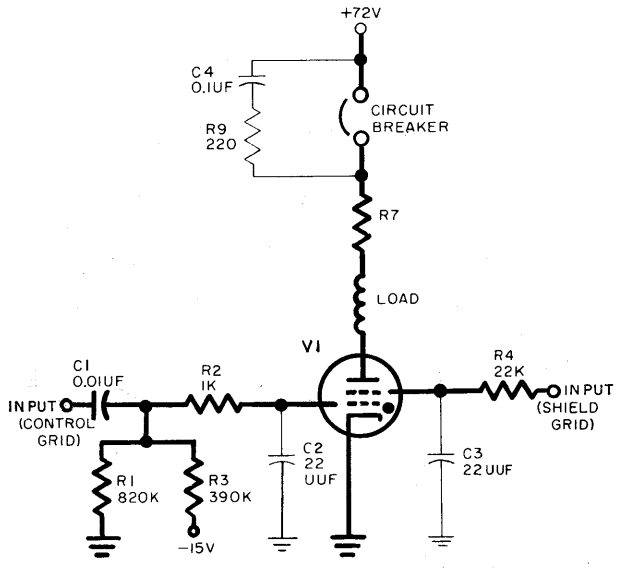


PLATE LOADED CIRCUIT 2

Figure 3–17. Thyratron Relay Driver, Model B, Schematic Diagram

TABLE 3–12. THYRATRON RELAY DRIVERS, MODELS A AND B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	USED ON	FUNCTION
C1	A, B	Input coupling capacitor.
C2	A, B	Neutralizes control grid-plate interelectrode capacitance.
C3	A, B	Neutralizes shield grid-plate interelectrode capacitance.
C4	A, B	Arc-suppressor network in plate-loaded circuit (with R9).
CR1	A, B	Clamps cathode at ground in cathode-loaded circuits during negative excursion.
CR2	B	Limits positive rise of cathode in cathode-loaded circuits.
R1	A, B	Control grid, voltage divider (with R3).
R2	A, B	Limits control grid current.
R3	A, B	Control grid, voltage divider (with R1).
R4	B	Limits shield grid current.
R5	A, B	Reduces cathode circuit impedance to ensure ionization in cathode-loaded circuit.
R6	A	Limits shield grid current.
R7	A, B	Limits current through relay or magnet coil.
R8	B	Limits current through CR2.
R9	A, B	Arc-suppressor network in plate-loaded circuit (with C4).
V1	A, B	Current switch.
Circuit Breaker	A, B	Opens plate circuit to deionize VI.

In its application in the $_{A}$RYD and $_{B}$RYD circuits, the thyratron is ionized by an appropriate rise in control grid voltage (well above critical grid voltage) and deionized by opening a circuit breaker (manually or automatically) in the anode circuit, reducing anode to cathode voltage well below extinction voltage.

5.2.2 Detailed Operation, Model A

Figures 3–16 contains the two circuits of the $_{A}$RYD. Consider circuit 2, and assume that the circuit breaker is closed and that the input is at the —30-volt standard level. The anode-to-cathode voltage is well above the ionizing potential, and the control grid is biased at —10 volts by the voltage divider consisting of resistors R1 and R3 between —15 volts and ground. This voltage is below the critical grid voltage for the given ionizing potential. A standard level rise of 40 volts from —30 volts to +10 volts at the input, point A, raises the control grid above the critical grid voltage.

Capacitor C1 will start to discharge through resistor R3, bringing point B down towards the bias voltage. The time constant of C1 and R3 is large (approximately 400 milliseconds) in comparison with the time it takes the tube to ionize (approximately 0.5 microsecond). Therefore, the thyratron will ionize before the grid voltage can fall appreciably. As soon as the thyratron ionizes, grid current brings point B rapidly down to cathode potential (ground level). A shift in standard level to —30 volts at point A will be coupled to point B by C1, lowering point B from ground to —40 volts. Since V1 is ionized, however, this fall in voltage at the control grid will not affect current through the tube, and C1 will discharge, raising point B to —10 volts.

Current through V1 passes through the relay or magnet coil in the plate circuit, energizing the relay or magnet. The circuit breaker then opens. With less than

extinction voltage across the tube, V1 will deionize. The time required to deionize V1 is approximately 150 microseconds. Whether the circuit breaker is manually operated or automatically operated, the time between the opening and the closing of the circuit breaker will always be greater than the time required for deionization. Thus, when the anode voltage is reapplied to the anode, the control grid, now at less than critical grid voltage, resumes control of the V1, and the circuit is ready for the next positive rise in standard level at point A.

Circuit 1 in figure 3–16 operates in the same manner. The location of the load in the cathode circuit requires special circuitry that is protective and ensures reliable performance. These are discussed in 5.3.

5.2.3 Detailed Operation, Model B

Both circuits of the $_{B}$RYD operate in the same manner. However, in comparing figures 3–16 and 3–17, it will be noted that the shield grids in figure 3–16 are at ground potential and that the shield grids in figure 3–17 are input terminals at standard level potential. In the $_{B}$RYD, prior to ionization, both grids are at the —30-volt standard level. It is a property of the thyratron that a positive voltage rise on the control grid cannot initiate ionization if the shield grid is maintained at a negative level with respect to the cathode. A positive level must be impressed on the shield grid before a positive shift in level on the control grid will ionize V1. This circuit performs its function, then, whenever a positive rise in level is applied to the input after a positive level shift has conditioned the shield grid. Once ionization takes place, a change in voltage at either input grid has no effect on current through V1.

5.3 CIRCUIT REFINEMENTS

The circuit refinements which ensure reliable performance are dictated in part by the location of the load-coil and in part by interelectrode capacity in V1. With the load in the cathode circuit (circuit 1, figs. 3–16 and 3–17), the coil presents a high impedance to (opposes) current. Resistor R5, connected across the coil and R7, decreases the impedance of the cathode circuit to a point where sufficient current will flow to ensure ionization with each occurrence of positive rise in level at the control grid. If R5 were removed, the cathode voltage would initially rise, reducing the anode-to-cathode potential to less than the ionizing potential. Unless the input level remained at the +10-volt level longer than it takes for the cathode potential to fall and restore the ionizing potential, the thyratron could not ionize, and the $_{A}$RYD would not perform its function. Thus R5 ensures ionization by lowering cathode impedance.

Diode CR1 maintains the cathode at ground level in the presence of negative signals. If the cathode were to fall below ground level when the tube is in its quiescent state, the control grid bias would be raised above critical grid voltage, and the thyratron would ionize. A —10-volt pulse, for example, would reduce control grid bias to 0 and fire the thyratron. The negative pulses, generated by collapsing fields in relay and magnet coils, can be coupled into nonenergized circuits through interconnecting cables. Diode CR1 prevents the adverse effects of these pulses when they occur. In addition, the coils in the circuits proper induce these negative pulse voltages each time current through the coil is stopped. Such pulses can carry the cathode below ground sufficiently to maintain ionization between grid and cathode until the circuit breaker recloses. In such a case, the thyratron would not deionize. Diode CR1 also prevents this.

In figure 3–17, whenever circuit 1 is used to drive a print or punch magnet, an additional network (shown in dashed line) is used to eliminate positive transient pulses which would raise the cathode above 48 volts. Such a rise would prevent the ionization of the gas in the thyratron for reasons already stated.

Capacitors C2 and C1 also ensure reliable performance. Each time the circuit breaker closes, the surge voltage appearing at the thyratron anode is coupled to the grids of the thyratron by the inherent capacitance between the tube elements. Capacitors C2 and C3 (relatively much larger than these inherent capacities) drain off the charge on the grids as fast as it tends to accumulate and thus prevent the grid or grids from rising above critical grid voltage. Thus C2 and C3 prevent a misfiring of the thyratron due to the effects of interelectrode capacitance each time the circuit breaker closes.

Resistors R6 and R9 and capacitor C4 are protective circuit elements. Resistor R6 limits shield grid current and protects the shield grid from being burned out. If it were removed, the life of the thyratron would be greatly shortened by the destruction of the shield grid. Parts C4 and R9 form an arc-suppressing network. They prevent the occurrence of an arc at the circuit breaker terminals each time the circuit breaker is opened. This protective circuit is used only in the plate-loaded thyratron relay driver. The same property of the coil to generate self-induced voltages with each initiation and interruption of current, which made the use of R5, CR1, CR2, and R8 necessary in the cathode-loaded circuit, makes the arc-suppressor network necessary in the plate-loaded circuit.

Resistor R7 is a protective part which limits the magnitude of current through the coil and thyratron.

Refer to table 3–12 for the function of detail parts not discussed.

CHAPTER 6

VACUUM-TUBE RELAY DRIVER, MODEL B

6.1 DEFINITION AND DESCRIPTION

The logic block symbol for the model B vacuum-tube relay driver ($_{B}$VRD) circuit is shown in figure 3–18. This is a nonlogic circuit and is used to energize

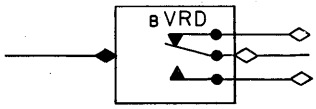


Figure 3–18. Vacuum-Tube Relay Driver, Model B, Logic Block Symbol

a sensitive relay each time a positive standard level (+10 volts) is applied to its input terminal (left input). The input and output levels shown on the right side of the logic block symbol indicate inputs and outputs of the relay which is a part of the $_{B}$VRD. Figure 3–18 shows the relation of these levels and the state of the relay being driven. An input level is applied to the movable arm or armature of the relay. The state of the relay (energized or de-energized) will determine at which output this level will appear. Thus, although two outputs are shown in the logic block symbol, they occur one at a time. The function of the $_{B}$VRD can now be stated more completely as follows: the $_{B}$VRD is a nonlogic circuit which applies a nonstandard level to one of two outputs. A standard down level produces a nonstandard level at output 1; a standard up level produces a nonstandard level at output 2.

6.2 PRINCIPLES OF OPERATION

Figure 3–19 is a schematic diagram of the $_{B}$VRD. Table 3–13 is the associated list of detail parts and their functions. The circuit consists of a triode, a relay, and the circuit elements required to provide decoupling and plate current limiting and to satisfy input requirements.

Triode V1 has two states of operation in this circuit, conducting and nonconducting. When the standard level input to the gird is +10 volts, V1 conducts. When the standard level input to the control grid is −30 volts, V1 is cut off. Assume the input level is at −30 volts, with capacitor C1 charged negatively to this voltage. In this state, a level is being applied to channel 1 through relay K1. A shift of input level from −30 volts to +10 volts does not immediately appear at the grid

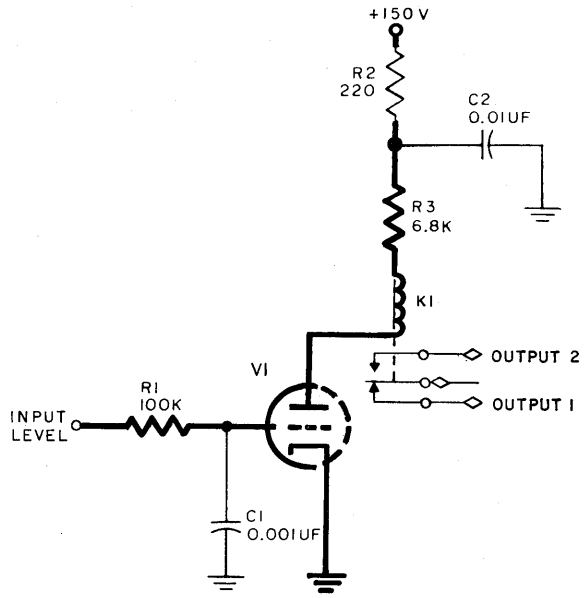


Figure 3–19. Vacuum-Tube Relay Driver, Model B, Schematic Diagram

TABLE 3–13. VACUUM-TUBE RELAY DRIVER, MODEL B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Slows down rise and fall times of input to prevent chatter in relay K1 (with R1).
C2	Decoupling network (with R2).
K1	Plate load for V1 and used to switch a non-standard level into one of two channels.
R1	Grid-limiting resistor; slows down input rise and fall times preventing chatter in relay K1 (with C1).
R2	Decoupling network (with C2).
R3	Plate load (with K1) and limits plate current through K1.
V1	Controls current through sensitive relay K1.

of V1. The negative charge on C1 maintains the grid at —30 volts. The value of R1 is chosen to translate the rapid shift at the input (0.5 usec) into a slower and more gradual rise of voltage (100 usec) at the grid. Capacitor C1 discharges toward the +10-volt input level through R1. Plate current starts when the point of grid cutoff voltage is passed and increases as the grid voltage continues to rise. Grid current flows when the grid becomes more positive than the cathode. The grid-limiting action of R1 maintains the grid at ground level (cathode potential), and V1 assumes its alternate state of conduction. In this state, plate current energizes relay K1, and a level is switched to channel 2. Note that, with the grid at ground level, C1 is completely discharged. A rapid shift of voltage at the input to the —30-volt standard level again appears as a gradual change at the grid as a result of the slow charging time of C1 through R1. The gradual fall in grid voltage causes a decrease in plate current until cutoff voltage is reached. At this point, the tube becomes nonconducting, and the relay reverts to its former state. Capacitor C1 continues to charge through R1 to the —30-volt level.

Refer to table 3—13 for the function detail parts not discussed.

CHAPTER 7
DIODE AND CIRCUITS

7.1 DEFINITION AND DESCRIPTION

Figure 3–20 is a logic block symbol of a diode AND circuit.

A diode AND circuit is a logic circuit which develops a positive level output, provided all inputs are positive levels. If any input is a negative level, the AND circuit may have several inputs.

The crystal diode is an essential part of the diode AND circuit. It is therefore important to become acquainted with the mechanical and electrical characteristics of the crystal diode to better understand the theory of operation of the diode AND circuit.

The crystal diode is 0.75 inch in length and 0.25 inch in diameter. It has two pigtails, one attached to the anode and one to the cathode. To guard against the harmful effects of humidity, it is hermetically sealed. (See figs. 3–21 and 3–22.)

The crystal diode has a unidirectional electrical characteristic utilized in the AND circuit. When the anode of a diode is positive with respect to its cathode, the diode will conduct. When the anode of a diode is negative with respect to its cathode, the diode will not conduct.

When a diode is conducting, its forward resistance is 50 ohms (see fig. 3–23).

When a diode is cut off, its backward resistance is approximately 500,000 ohms (see fig. 3–24).

This property of high resistance for one polarity and low resistance for the opposite polarity is employed in AND circuitry.

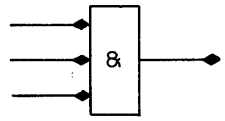


Figure 3–20. Diode AND Circuit, Logic Block Symbol

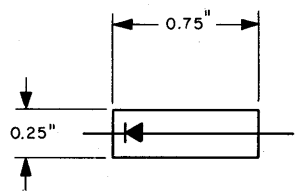


Figure 3–21. Crystal Diode, Physical Dimensions

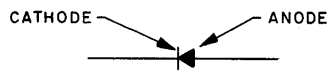


Figure 3–22. Crystal Diode, Electrical Symbol

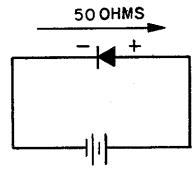


Figure 3–23. Forward Resistance of Crystal Diode, Schematic Diagram

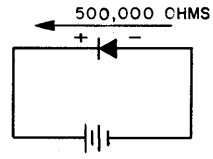


Figure 3–24. Backward Resistance of Crystal Diode, Schematic Diagram

7.2 PRINCIPLES OF OPERATION

7.2.1 Basic Operation

Figure 3–25 is a simplified schematic diagram of a diode AND circuit. With —30 volts applied to the cathode of CR1, the diode conducts. Because of the low forward resistance of a crystal diode, the voltage drop in the circuit will occur across resistor R_{AND}. The voltage at point C is then —30 volts. With +10 volts applied to the cathode of CR2 and —30 volts on its anode, CR2 is cut off. Point C remains at —30 volts. The high backward resistance of crystal diode CR2 isolates one input circuit (point B) from the output circuit (point C). If both crystal diodes CR1 and CR2 have +10 volts applied to their cathodes, both will conduct, and the potential at point C will be +10 volts.

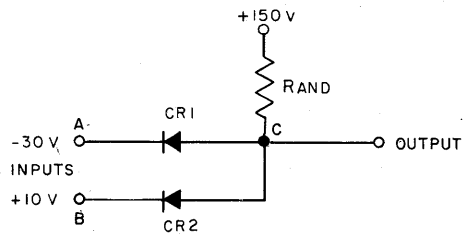


Figure 3–25. Two-way AND Circuit, Simplified Circuit Diagram

It can be seen that, to make point C positive, inputs A and B must be positive and that, to make point C negative, either one or both of the inputs must be negative. Figure 3–26 is a schematic diagram of a diode AND circuit.

Crystal diode CR3 is a protective feature of the circuit. It clamps point C at +10 volts, limiting the positive level at point C to +10 volts. This prevents the grid of a vacuum tube in a following stage from being driven so far positive that destruction of the tube might result.

7.2.2 Detailed Operation

The effect of load capacitance on the circuit may be seen in the output waveshape (Eo in fig. 3–27). The leading (left-hand) edge does not rise vertically. The reason for this is shown in figure 3–27. Capacity C represents the capacitance of the output circuit load and stray wiring capacitance. If both inputs are at −30 volts, electrons will flow through the low forward resistance of the diodes to the positive power supply. The outputs will be −30 volts. If both inputs are raised to +10 volts, the diodes will stop conducting, since C will hold the anodes at −30 volts until C can charge through R_{AND} toward +150 volts; C charges to +10 volts. The time constant of RC will determine the rate at which the voltage waveform (Eo) will rise. When one of the inputs returns to −30 volts, C will discharge through the low forward resistance of the diode. Since the forward resistance is low (about 50 ohms), the fall time will be negligible. The comparatively long rise time limits the applications of the diode AND circuit.

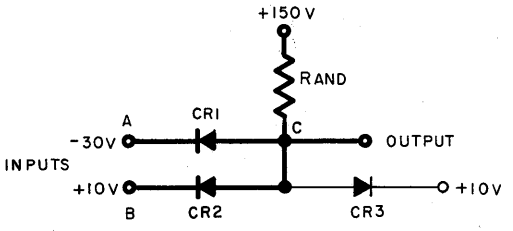


Figure 3–26. Two-Way AND Circuit, Schematic Diagram

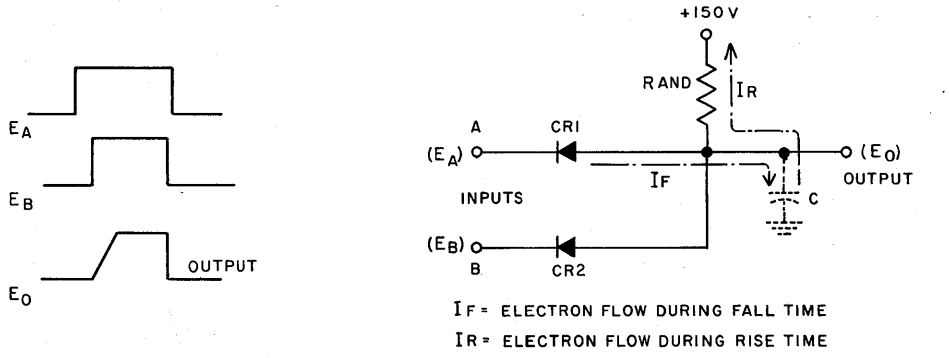
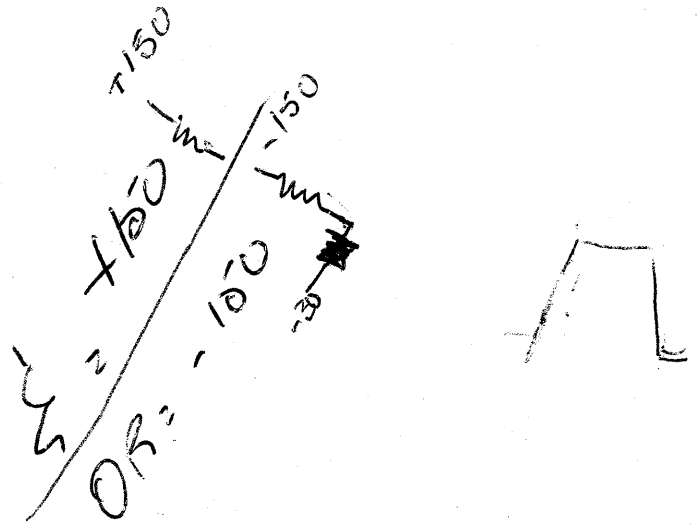


Figure 3–27. AND Circuit, Effect of Load Capacitance, Schematic Diagram and Waveforms



CHAPTER 8
DIODE OR CIRCUITS

8.1 DEFINITION AND DESCRIPTION

Figure 3–28 is a logic block symbol of a diode OR circuit.

A diode OR circuit is a logic circuit which develops a negative level output, provided that all inputs are negative levels. If any input is a positive level, the OR circuit develops a positive level output. This type of circuit may have several inputs. For information concerning the crystal diode, an essential part of the diode OR circuit, see 7.1.

8.2 PRINCIPLES OF OPERATION

8.2.1 Detailed Operation of Diode OR Circuit

Figure 3–29 is a schematic diagram of a diode OR circuit. With +10 volts applied to the anode of CR_1, the diode conducts. Because of the low forward resistance of the crystal diode, the voltage drop in the circuit will be across resistor R_{OR}. The voltage at point C is then +10 volts. With +10 volts applied to the cathode of CR^2 and −30 volts on its anode, CR_2 is cut off. Point C remains at +10 volts. The high backward resistance of crystal CR^2 isolates one input circuit (point B) from the output circuit (point C).

If both crystal diodes CR^1 and CR^2 have −30 volts applied to their anodes, both will conduct, and the potentional at point C will be −30 volts. It can be seen that, to make point C negative, A and B must be negative and, to make point C positive, either one or both of the inputs (A and B) must be positive. Crystal diode CR_3 is a −30-volt clamp.

If all the OR circuit inputs are fed from AND circuits, there is nothing to prevent the output from going extremely negative should the +150-volt supply fail. A protection diode, clamping the circuit to −30 volts, is connected to the outputs of all OR circuits of this category.

The effect of load capacitance on the circuit may be seen in the output waveshapes of figure 3–30. The effect is the same as in the AND circuit, except that the trailing (right-hand) edge is affected. For a discussion of this, see 7.2.2.

8.2.2 Detailed Operation of Pulsed OR Circuit

The fast rise time of the OR circuit permits a pulse input. This is not possible with the AND circuit because

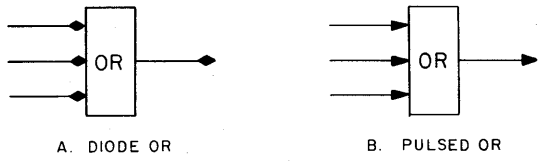


Figure 3–28. Diode OR Circuit, Logic Block Symbols

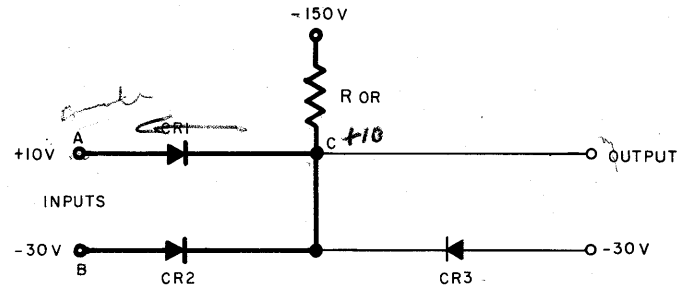


Figure 3–29. Two-Way OR Circuit, Schematic Diagram

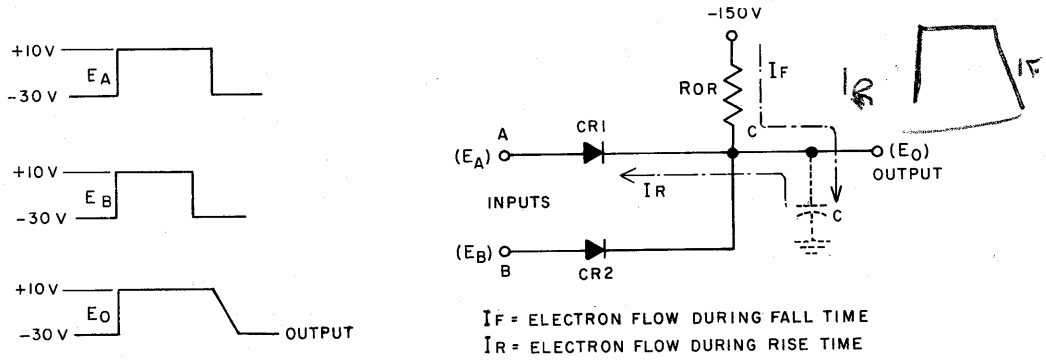


Figure 3–30. Effect of Load Capacitance in OR Circuit

load capacitance gives the circuit a slow rise time. Figure 3–31 shows a pulsed OR circuit. In order for this circuit to function with pulse inputs, the fall time must be speeded up. This is accomplished by replacing resistor R_{OR} with an inductor, L. Resistor R_L is used to prevent oscillation between L and C (stray capacitance). Resistor R_L is of low ohmic value.

It can be seen that any positive pulse applied to either input will appear at the output. The cathodes of the diodes are grounded through inductor L and resistor R_L. When a positive pulse appears at the input, the diode involved will conduct, and the pulse will appear at the output.

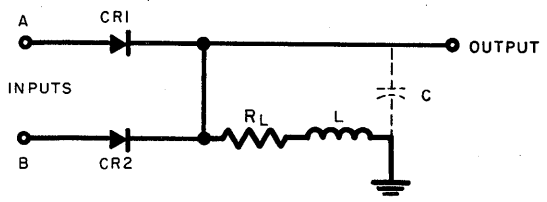


Figure 3–31. Pulsed OR Circuit, Schematic Diagram

8.2.3 Operation of $_Y$OR Operation

When the output from a pulsed OR is applied to a pulse transformer, the $_Y$OR circuit shown in figure 3–32 is employed.

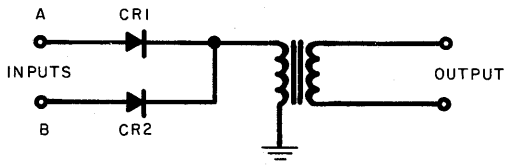


Figure 3–32. $_Y$OR Circuit, Schematic Diagram

CHAPTER 9
GATE TUBE, MODEL A

9.1 DEFINITION AND DESCRIPTION

The model A gate ($_A$GT) is a logic coincidence circuit. Figure 3–33 is the logic block symbol. A standard pulse applied to the input of the $_A$GT will appear at the output only when the $_A$GT is conditioned by a positive standard level.

9.2 PRINCIPLES OF OPERATION

9.2.1 Basic Operation

Figure 3–34 is a schematic diagram of the $_A$GT. Table 3–14 is the associated list of detail parts and their functions. The $_A$GT consists of a pentode vacuum tube, an output transformer, and associated circuitry. A standard pulse input is applied to the control grid of pentode V1, and a standard level is applied to its suppressor grid. Pentode V1 is biased past cutoff by a fixed —15 volts applied to the control grid.

The $_A$GT has two states: conditioned and nonconditioned (see fig. 3–35). In the nonconditioned state, a —30-volt level is applied to the suppressor grid (input B). In this state, although a standard pulse is applied to input A, overcoming the —15-volt bias, no current will flow through V1 because the —30-volt level is sufficient to hold this pentode at cutoff.

The $_A$GT is conditioned by the application of a +10-volt level of the suppressor grid of V1. In this state, the application of a standard pulse at input A overcomes the —15-volt grid bias, and the pentode conducts, producing a standard pulse at the output.

9.2.2 Detailed Operation

The standard pulse source is coupled to the control grid through capacitor C1 (see fig. 3–34). This capacitor blocks the —15-volt bias from the pulse source. For direct pulse inputs, inductor L1 presents a high impedance to the high-frequency pulse and a low impedance to the d-c discharge path of C1. This provides the proper loading to the input pulse while preventing bias buildup on C1. The standard level source is coupled directly to the suppressor grid. When coincidence occurs, the tube conducts. The resulting pulse of current in the plate circuit of V1 is transformer-coupled by T1, producing a standard pulse at the output. Transformer T1 also matches the high impedance of the plate to the low impedance of the load.

Decoupling networks are provided where the $_A$GT is connected to common power supplies. These networks isolate the gate from other circuits powered from the same supplies. Resistors R5 and R6 are parasitic suppressors.

Capacitor C2 is used when the $_A$GT is fed from a flip-flop. Pentode V1 conducts heavily for a brief pe-

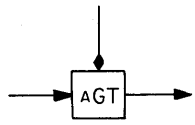
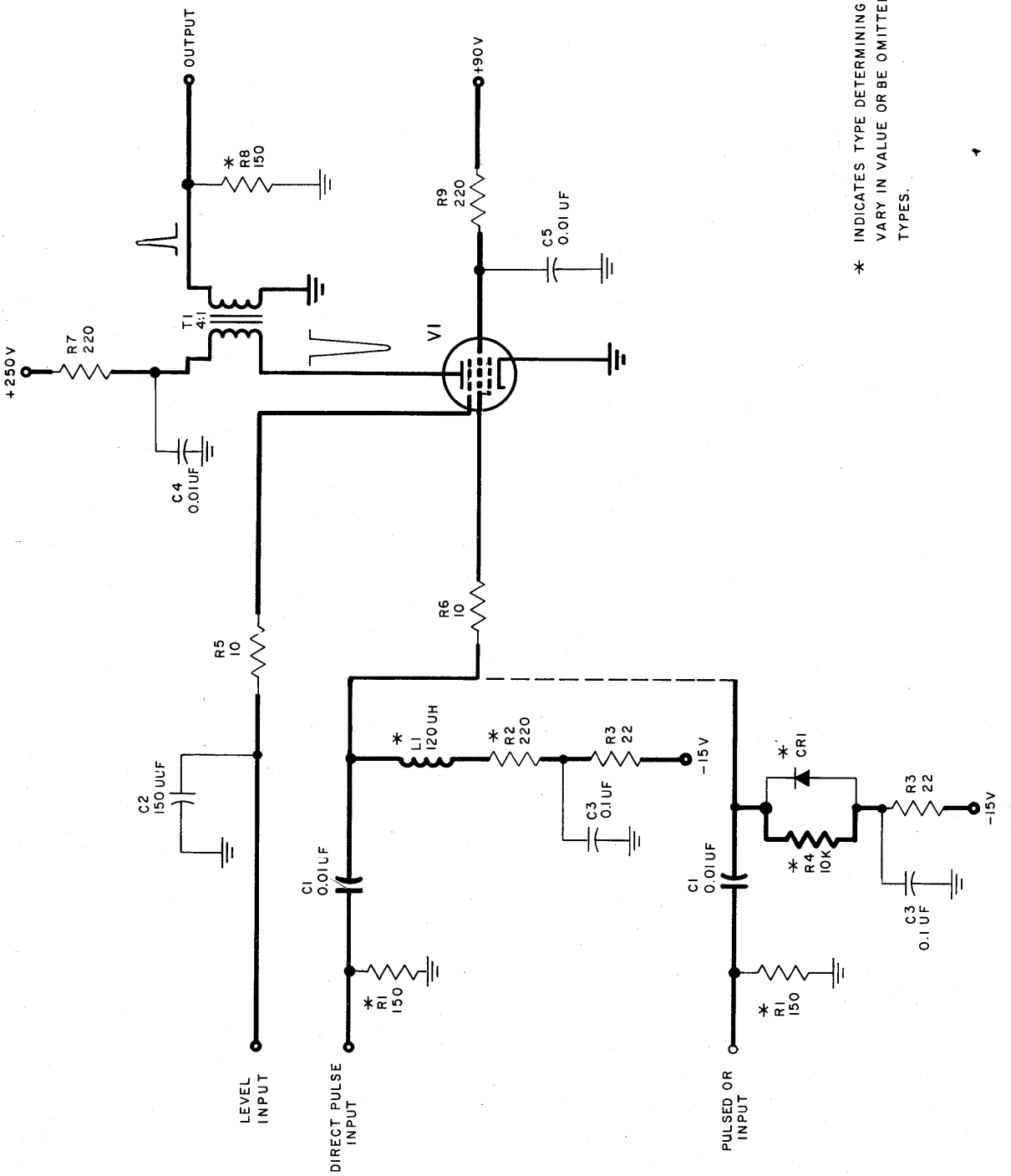


Figure 3–33. Gate Tube, Model A, Logic Block Symbol

TABLE 3–14. GATE TUBE, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Input coupling capacitor.
C2	Suppressor grid bypass capacitor.
C3	Part of decoupling network (with R3).
C4	Part of decoupling network (with R7).
C5	Part of decoupling network (with R9).
CR1	Provides low impedance discharge path for C1, preventing bias buildup.
L1	Peaking coil for input pulse.
R1	Input coaxial cable termination.
R2	Damping resistor for inductor L1.
R3	Part of decoupling network (with C3).
R4	Grid d-c return.
R5	Parasitic suppressor.
R6	Parasitic suppressor.
R7	Part of decoupling network (with C4).
R8	Terminating resistor.
R9	Part of decoupling network (with C5).
T1	Output transformer.
V1	Gate electron tube.



* INDICATES TYPE DETERMINING COMPONENTS. THESE MAY VARY IN VALUE OR BE OMITTED FROM CIRCUIT IN DIFFERENT TYPES.

Figure 3–34. Gate Tube, Model A, Schematic Diagram

riod. The suppressor grid draws current during this time. Capacitor C2 smooths out these current surges, establishing a more desirable loading effect on the conditioning flip-flop. Resistor R1 is the terminating resistor for a coaxial cable input; R8 is the terminating resistor for the transformer.

Resistor R4 and diode CR1 are employed in the grid circuit for pulsed OR inputs. Resistor R4 provides a high-resistance load to the pulse, and crystal diode CR1 provides a low-resistance discharge path for capacitor C1. When input A is pulsed, the control grid draws current. A negative charge accumulates on capacitor C1. If this capacitor has not discharged by the time the next pulse arrives, a residual charge will add to the —15-volt bias. Succeeding pulses will then develop a bias buildup which will cause circuit failure. Refer to table 3—14 for the function of detail parts not discussed.

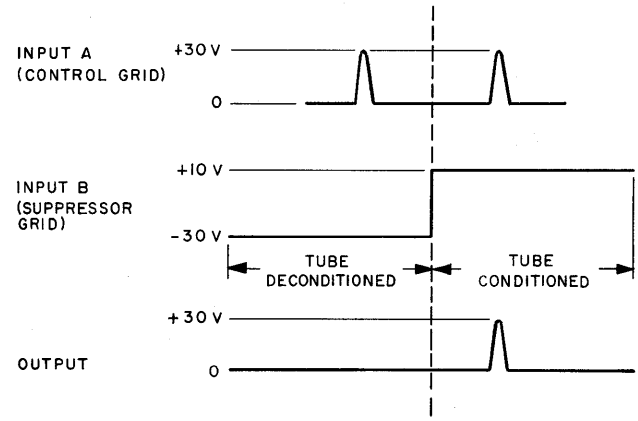


Figure 3—35. Gate Tube, Model A, Input-Output Relationship

CHAPTER 10
D-C INVERTER

10.1 DEFINITION AND DESCRIPTION

The model A d-c inverter ($_A$I), shown in logic symbol form in figure 3–36, is a logic circuit. The $_A$I

Figure 3–36. D-C Inverter, Model A, Logic Block Symbol

produces a −30-volt level when the input level is positive and a +10-volt level when the input level is negative. The $_A$I is the only inverter model and is used when logic requires a level reversal.

10.2 PRINCIPLES OF OPERATION

10.2.1 Basic Operation

Figure 3–37 is a simplified block diagram of the $_A$ I. The circuit consists of an overdriven amplifier (driven to grid-limiting or cutoff) and a cathode follower whose output is clamped at levels of +10 and −30 volts.

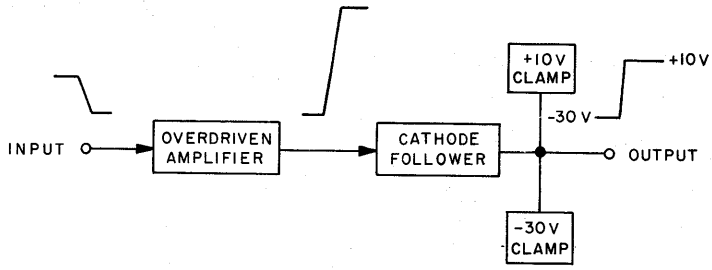


Figure 3–37. D-C Inverter, Simplified Block Diagram

A positive level between 0 and +12 volts applied to the overdriven amplifier input is amplified and inverted and fed to the cathode follower, whose output circuit clamps the inverted level of −30 volts. Similarly, a negative level between −8 and −30 volts applied to the overdriven amplifier is amplified, inverted, and clamped at +10 volts at the cathode follower output.

TABLE 3–15. D-C INVERTER, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Resistor R1 bypass; speeds rise time of input level (and fall time of output level).
C2	Part of decoupling network (with R3).
C3	Resistor R5 bypass; speeds rise and fall time.
C4	Part of decoupling network (with R8).
CR1	Clamps V1B grid at −35 volts.
CR2	Clamps V1B cathode at +10 volts.
CR3	Clamps V1B cathode at −30 volts.
R1	Grid-limiting resistor.
R2	Parasitic suppressor.
R3	Part of decoupling network (with C2).
R4	Plate load resistor for V1A.
R5	Part of voltage divider network (with R6).
R6	Part of voltage divider network (with R5).
R7	Parasitic suppressor.
R8	Part of decoupling network (with C4).
R9	Diode CR2 current-limiting resistor.
R10	Part of cathode load resistor and of voltage divider for CR1 bias (with R11).
R11	Part of cathode load resistor and of voltage divider for CR1 bias (with R10).
V1A	Overdriven amplifier.
V1B	Cathode follower.

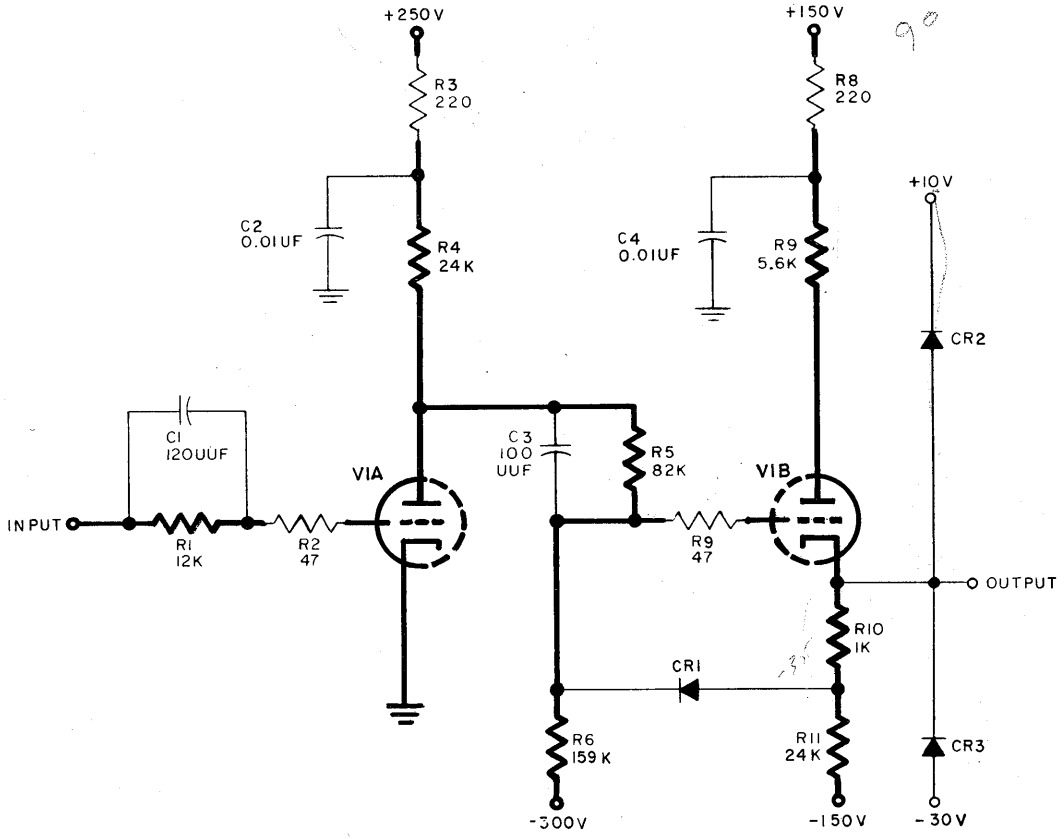


Figure 3–38. D-C Inverter, Model A, Schematic Diagram

10.2.2 Detailed Operation

Figure 3–38 is a circuit schematic of the $_{A}$I. Table 3–15 is the associated list of detail parts and their functions. When a —8-volt level is applied to V1A, this tube is cut off. With no plate current flow, the plate potential of V1A would rise to +250 volts. However, the voltage divider formed by resistors R4, R5, and R6 holds the plate at +200 volts when V1A is cut off. With a +200-volt potential at the plate of V1A, there is a 500-volt potential across the voltage divider formed by resistors R5 and R6. The voltage drop across R5 would place the grid of V1B at +31 volts. The grid of V1B, however, does not become more positive than +10 volts because diode CR2 clamps the cathode of V1B at +10 volts. A more positive potential at the input of V1B results in grid current flow through R5, keeping the grid from becoming more positive in potential than +10 volts.

A positive potential of +2 volts applied to the grid of V1A results in its plate current's reducing the plate potential to +66 volts. The potential across the voltage divider formed by resistors R5 and R6 is now 366 volts. The voltage drop across R5 would place the grid of cathode follower V1B at —58 volts. The grid, however, never becomes more negative than —35 volts because diode CR3 clamps the cathode of V1B at —30 volts. Cathode resistors R10 and R11 form a voltage divider between potentials of —30 and —150 volts. The anode of CR1 is at —35 volts, preventing the grid from becoming more negative than this potential.

A positive input level becomes a —30-volt output level, and a negative input level becomes a +10-volt output level. Refer to table 3–15 for the function of detail parts not discussed.

CHAPTER 11
FLIP-FLOPS

11.1 DEFINITION AND DESCRIPTION

Because of circuit complexity, the flip-flops and their associated models will be discussed in the manner that follows. The logic block function will be presented, followed by a tabulation of logic symbols and fundamental circuit characteristics of each model. This, in turn, will be followed by discussions of the flip-flop block diagram and basic circuit. The remainder of the text will discuss the significant features of each flip-flop circuit.

The flip-flop are logic circuits capable of storing a binary digit. The model A flip-flop ($_A$FF) produces d-c output levels only when the input is a standard pulse. The $_B$FF and $_C$FF produce standard d-c output levels when the input is either a standard pulse or a negative d-c level shift. Table 3–16 depicts the logic block symbols for the three flip-flop models and indicates generally the speed and drive characteristics of each. As indicated, the $_B$FF and $_C$FF operate with either standard pulses or standard level inputs.

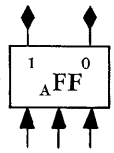
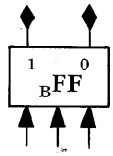
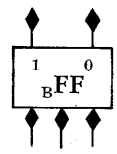
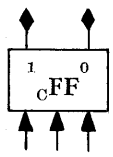
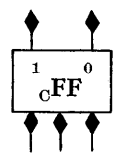
11.2 PRINCIPLES OF OPERATION

11.2.1 Basic Operation

Figure 3–39 is a simplified block diagram of a flip-flop. It consists of two amplifiers, designated A and B. The output of each amplifier feeds the input of the other. Circuits of this type are called multivibrators. The flip-flop itself is a form of multivibrator having two stable states and, for this reason, is called a bistable multivibrator.

By definition, the output of amplifier B (see fig. 3–39) is the set or 1 output of the flip-flop, and the output of amplifier A is the clear or 0 output. When the set output is up (+10-volt level), the clear output is down (—30-volt level), and the flip-flop is in the set state. Conversely, the flip-flop is in the clear state when

TABLE 3–16. FLIP-FLOPS, LOGIC BLOCK SYMBOLS AND CHARACTERISTICS

FLIP-FLOP MODEL	LOGIC BLOCK SYMBOL		CHARACTERISTICS	
	PULSE INPUT	LEVEL INPUT	SPEED	DRIVE
A			High speed	Can drive load directly
B			Low speed	Cannot drive load directly
C			Low speed (lower than BFF)	Can drive load directly

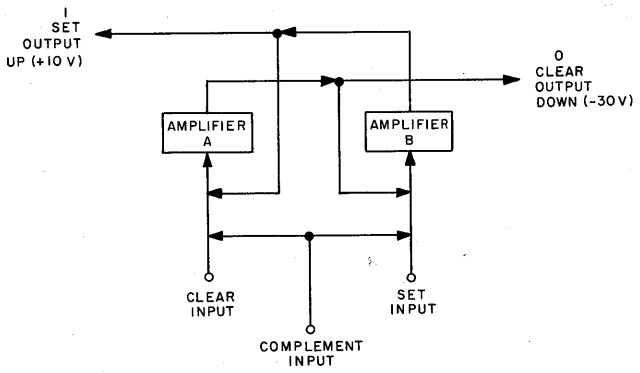


Figure 3—39. Flip-Flop, Block Diagram

the clear output is up and the set output is down. The flip-flop is always in one of these two states.

Applying an appropriate signal to the clear input ensures that the clear output will be up. Likewise, the set output is up when an appropriate signal is applied to the set input. By applying signals to both inputs simultaneously, the state of the flip-flop is changed. This process is known as complementing.

Figure 3—40 is a simplified schematic diagram of a flip-flop. Before circuit operation is discussed, the following should be noted:

a. Resistors R3, R1, and R2 are equal to resistors R4, R5, and R6, respectively.

b. An increase in plate current through plate load resistor R3 lowers the plate potential of V1. Conversely, a decrease in plate current raises the V1 plate potential. The same is true of V2 and associated plate load resistor R4.

c. The voltage divider formed by resistors R4, R1, and R2 between B+ and B— serves several functions. When V1 is conducting and V2 is cut off, the voltage divider provides a proper up level at the set output and, at the same time, keeps the grid of V1 sufficiently positive to ensure full conduction. When V2 is conducting and V1 is cut off, the divider provides sufficient bias to keep V1 cut off and provides a proper down level at the set output. The voltage divider formed by R3, R5, and R6 between B+ and B— serves the same function at the opposite side of the flip-flop.

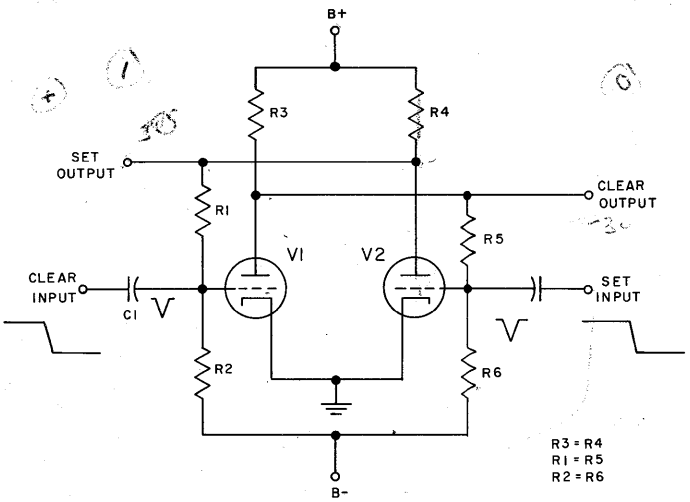


Figure 3—40. Flip-Flop, Simplified Schematic Diagram

With the flip-flop in its set state, V1 is conducting and V2 is cut off. A negative-going level applied to the clear input is changed to a negative pulse (fig. 3—40) by the combination of coupling capacitor C1 and resistor R2. This negative pulse at the grid of V1 decreases the plate current, which, in turn, increases the plate potential of V1. The voltage divider formed by resistors R5 and R6 between the plate of V1 and B— presents a positive rise of voltage at the grid of V2. This increases the plate current through V2 and, in turn, reduces its plate potential. The voltage divider formed by resistors R1 and R2 between the plate of V2 and B— presents a negative fall in voltage at the grid of V1. This further decreases plate current through V1. The resultant rise of voltage at the V1 plate leads to the increase of V2 plate current, causing a further drop in its plate potential. This action is cumulative and continues until V1 is cut off and V2 is conducting fully. Since V1 and V2 amplify the potential changes appearing at their respective grids, regeneration results and the process of changing state is very rapid. The flip-flop is now in a clear state, with an up level at the clear output and a down level at the set output. Figure 3—41 depicts the flip-flop output levels being changed from a set to a clear state.

When a negative-going level is applied to the set input, V2 is cut off and V1 conducts fully, changing the flip-flop to a set state. The action is similar to those in the previous discussions.

The detailed operation of the flip-flop circuits is explained in the following manner. The $_{B}$FF is described first, followed by the $_{C}$FF and $_{A}$FF, in that order. The $_{B}$FF description includes a brief discussion of function and operating characteristics. This is followed by a brief description of circuit operation based on the previous discussion of basic circuit operation. (Because of circuit symmetry, this description deals mainly with components for one-half of the flip-flop.) The components that serve speedup, stabilization, protective, and type-distinguishing functions are explained.

The $_{C}$FF and $_{A}$FF are explained in a manner similar to that for the $_{B}$FF. However, the $_{C}$FF circuit is discussed mainly with reference to change from the $_{B}$FF,

and the $_{A}$FF circuit is discussed with reference to change from the $_{B}$FF and $_{C}$FF.

A tabulated list of parts and their circuit function is included in the discussion of each flip-flop model.

11.2.2 Detailed Operation of Low-Speed, Model B Flip-Flop

The low-speed $_{B}$FF produces standard d-c level outputs for either a standard pulse or negative-going level shift input, depending upon the configuration of the input circuits.

The $_{B}$FF operates at a maximum pulse repetition frequency of 500 kc (400 kc for complement input).

Figure 3–42 is a schematic diagram of the $_{B}$FF. Table 3–17 is the associated list of detail parts and their functions. In the set state of the $_{B}$FF, V1A is conducting, and V1B is cut off. A negative pulse at the grid of V1A reverses this state, and, as a result, V1A is cut off and V1B conducts. (The flip-flop action leading to this result is the same as that discussed in the basic flip-flop circuit.) At this time, the clear output is at +10 volts (up), and the set output is at −30 volts (down). These output voltages are obtained from voltage dividers similar to those in the basic flip-flop circuit.

The set output is maintained at a −30-volt potential by a combination of two voltage dividers. One voltage divider, in the plate circuit of V1B, is formed by resistors R11 and R10 between +90 volts and ground potential. The other divider consists of inductor L2 and resistors R3 and R5. The effect of L2 on the voltage divider is negligible (except during transitions) because of its low d-c resistance. A similar combination of voltage dividers keeps the clear output at +10 volts. When a negative pulse at the grid of V1B changes the state of the $_{B}$FF, the set output returns to +10 volts, and the clear output returns to −30 volts. These levels are set by the respective voltage dividers when V1A conducts and V1B is cut off.

In order to speed up rises and falls (transitions), capacitor C2 is connected across resistor R3. This capacitor couples the grid of V1A to the plate of V1B (for high frequencies) and, in this way, serves as a speedup device. Capacitor C6 across resistor R13 serves the same function in the grid circuit of V1B. Inductors L1 and L2 are peaking coils and speed up rises and falls (transitions) at the plates of V1A and V1B, respectively. As indicated in figure 3–42, levels are applied directly to the set and clear inputs. Standard pulses are applied through a special network, consisting of input diodes, transformer, and damping diode, to these inputs.

With V1A conducting and V1B cut off, a negative shift applied to the clear input is changed to a peaked negative pulse by the differentiating network composed of capacitor C1 and resistor R1. (This negative pulse is similar to the one depicted in figure 3–40.) Crystal diode CR4 passes this negative pulse to the grid of V1A, causing a reduction in plate current. This diode prevents positive voltages from reaching the grid, thereby isolating this grid from the cathode of V1A and V1B and permitting V1A to be cut off.

A standard pulse is applied to either crystal diode CR1 or CR2 at the clear input. These diodes, together with pulse transformer T1, form a pulsed $_{Y}$OR circuit similar to that discussed in Chapter 10, except that the secondary connections of T1 are interchanged to invert the positive input. The resultant negative pulse is unaffected by C1 and R1. This pulse is fed to the grid of V1A through diode CR4, causing a reduction in plate current.

Diode CR3 provides a low resistance (forward resistance) to a positive pulse and, in this way, damps the positive overshoot.

Circuits feeding pulses to input diodes CR1 and CR2 at the primary of T1 are isolated from each other by these diodes. An input diode is added to the pulse input circuit for each additional source feeding the $_{B}$FF.

The $_{B}$FF is complemented when the set and clear inputs are pulsed simultaneously, producing a change of state each time the complement input is pulsed.

Load current drawn from either output of the $_{B}$FF would upset the associated divider, causing the output

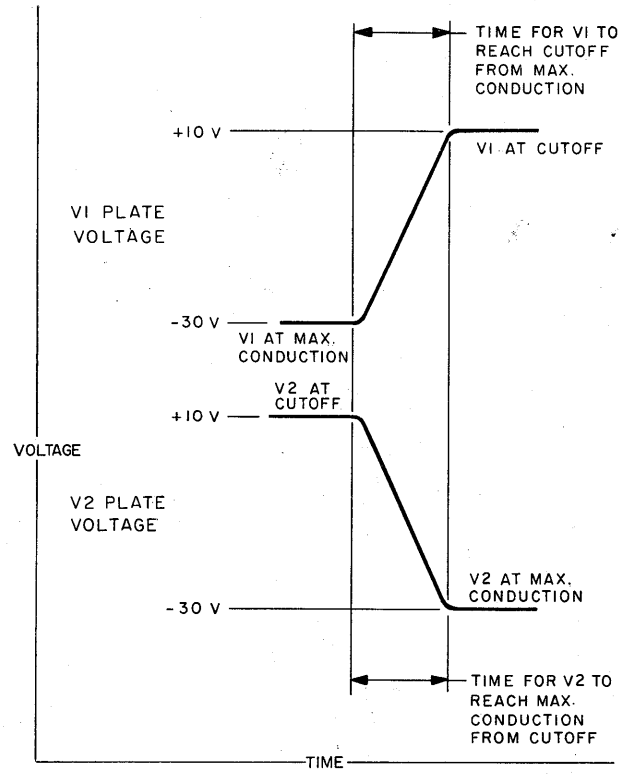


Figure 3–41. Flip-Flop Output Levels When Changing from a Set to a Clear State

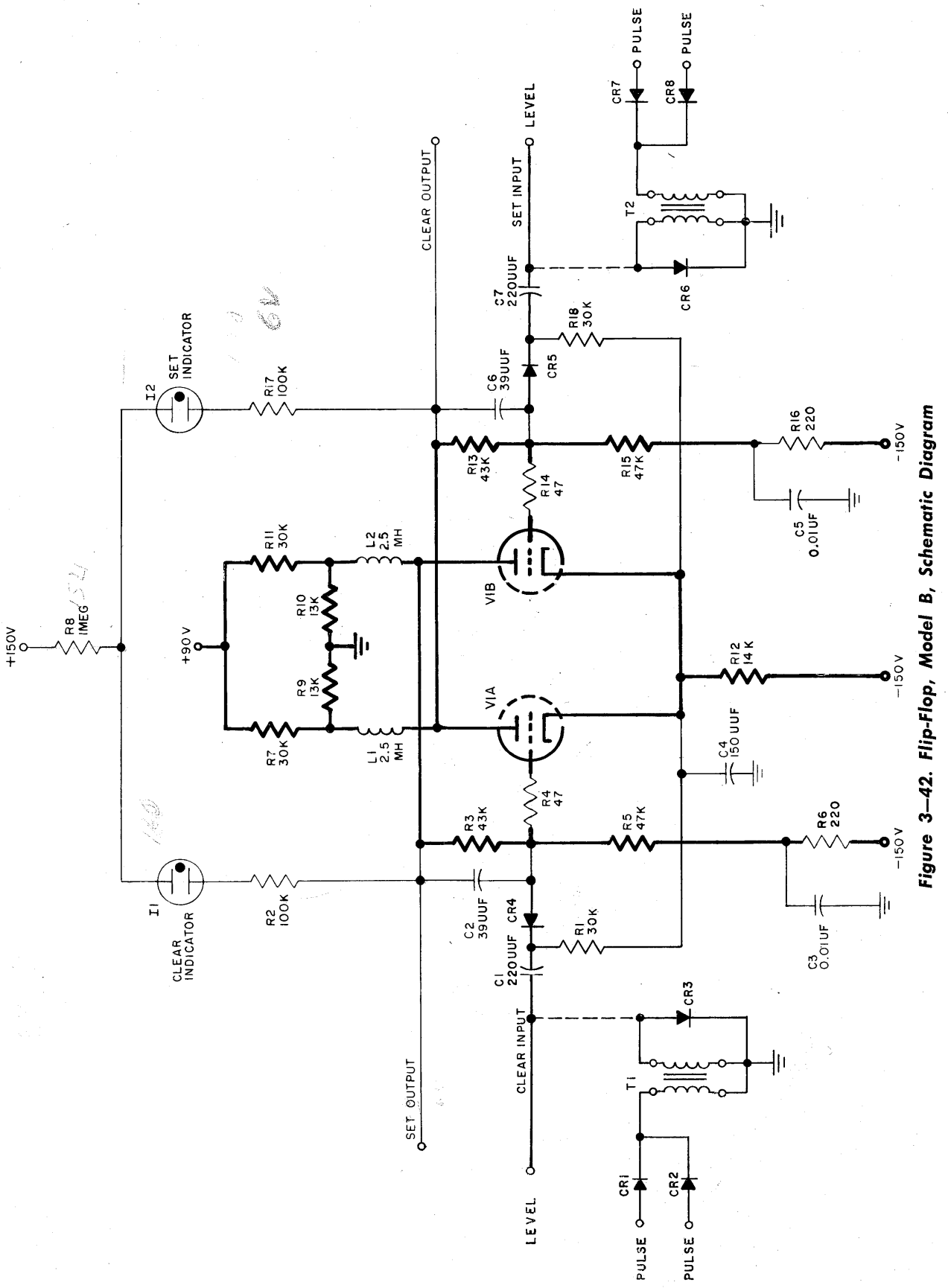


Figure 3–42. Flip-Flop, Model B, Schematic Diagram

TABLE 3–17. FLIP-FLOP, MODEL B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Part of differentiating network (with R1).
C2	Speedup capacitor, improves rise and fall time.
C3	Part of decoupling network (with R6).
C4	Ground return (ac).
C5	Part of decoupling network (with R16).
C6	Speedup capacitor, improves rise and fall time.
C7	Part of differentiating network (with R18).
CR1	Pulsed OR input diode.
CR2	Pulsed OR input diode.
CR3	Clips positive overshoot.
CR4	Isolates grid of V1A from V1A and V1B cathodes.
CR5	Isolates grid of V1B from V1A and V1B cathodes.
CR6	Clips positive overshoot.
CR7	Pulsed OR input diode.
CR8	Pulsed OR input diode.
I1	Indicates clear state.
I2	Indicates set state.
L1	Peaking coil, improves rise and fall time.
L2	Peaking coil, improves rise and fall time.
R1	Part of differentiating network (with C1).
R2	Isolates set output from I1.
R3	Part of voltage divider (with R5).
R4	Parasitic suppressor.
R5	Part of voltage divider (with R3).
R6	Part of decoupling network (with C3).
R7	Part of voltage divider (with R9).
R8	Limits current through I1 and I2.
R9	Part of voltage divider (with R7).
R10	Part of voltage divider (with R11).
R11	Part of voltage divider (with R10).
R12	Cathode resistor for V1A and V1B.
R13	Part of voltage divider (with R15).
R14	Parasitic suppressor.
R15	Part of voltage divider (with R13).
R16	Part of decoupling network (with C5).
R17	Isolates clear output from I2.
R18	Part of differentiating network (with C7).
T1	Input transformer.
T2	Input transformer.
V1A	Flip-flop triode.
V1B	Flip-flop triode.

levels which are dependent upon the voltage dividers to vary from their nominal values. For this reason, the $_{B}$FF must be isolated from its load by a cathode follower.

There are two neon indicators, I1 and I2. Indicator I1 glows when the set output is down, indicating a clear state; I2 glows when the clear output is down, indicating a set state. These indicators are located at appropriate positions on the computer. Resistors R2 and R17 isolate each indicator circuit from its respective output. Refer to table 3–17 for the function of detail parts not discussed.

11.2.3 Detailed Operation of Low-Speed, Model C Flip-Flop

Figure 3–43 is a schematic diagram of the $_{C}$FF, which operates with a maximum pulse repetition frequency of 200 kc. Table 3–18 is the associated list of detail parts and their functions. The $_{C}$FF is slower than the $_{B}$FF; however, it can drive a load directly.

The set output is clamped at +10 volts by CR4 and at −30 volts by CR5. The clear output is clamped at +10 volts by CR7 and at −30 volts by CR8. The voltage divider associated with V1A consists of resistors

R11, R12, R17, and R18 between potentials of +90 and —300 volts. The $_{C}$FF does not employ peaking coils in its plate circuits as does the $_{B}$FF. The RC network formed by capacitor C3 and resistor R9 ensures circuit stability with the aging of VA and V1B. This is accomplished by the development of a positive bias on the grids of V1A and V1B. Such a bias enables each flip-flop triode to function properly after cathode emission has decreased because of aging. The input circuits for pulses and levels are similar to those discussed with the $_{B}$FF. The values of C1 and R1 vary to meet input requirements. Complementing is accomplished in the same manner as in the $_{B}$FF. Refer to table 3–18 for the functions of detail parts not discussed.

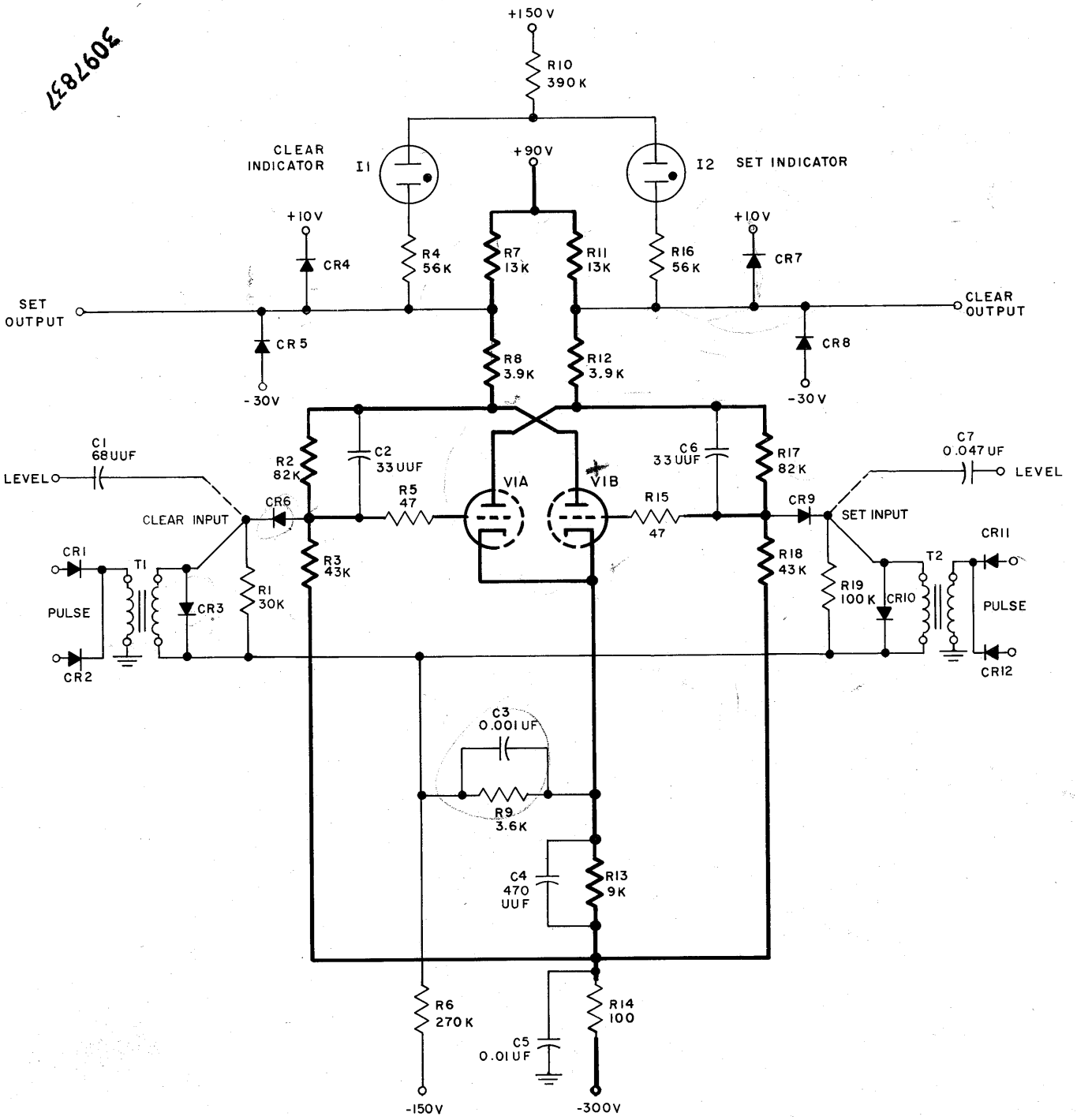


Figure 3–43. Flip-Flop, Model C, Schematic Diagram

11.2.4 Detailed Operation of High-Speed, Model $_A$FF Flip-Flop

The high-speed $_A$FF, shown in figure 3–44, operates with a maximum pulse repetition frequency of 2 megacycles. Table 3–19 is the associated list of detail parts and their functions. The input signal to the $_A$FF is a standard pulse. The use of cathode follower output circuits enables the $_A$FF to drive a load directly. Cathode follower V2A isolates the plate circuit of V2B from the grid circuit of V1B. Cathode follower V1A isolates the plate of V1B from the grid circuit of V2B. This permits faster flip-flop action.

TABLE 3–18. FLIP-FLOP, MODEL C, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Part of differentiating network (with R1).
C2	Speedup capacitor, improves rise and fall time.
C3	Ensures circuit stability (with R9).
C4	Cathode bypass capacitor.
C5	Part of decoupling network (with R14).
C6	Speedup capacitor, improves rise and fall time.
C7	Part of differentiating network (with R19).
CR1	Pulsed OR input diode.
CR2	Pulsed OR input diode.
CR3	Clips positive overshoot.
CR4	+10-volt clamp (set output).
CR5	−30-volt clamp (set output).
CR6	Isolates grid of V1A.
CR7	+10-volt clamp (clear output).
CR8	−30-volt clamp (clear output).
CR9	Isolates grid of V1B.
CR10	Clips positive overshoot.
CR11	Pulsed OR input diode.
CR12	Pulsed OR input diode.
I1	Indicates clear state.
I2	Indicates set state.
R1	Part of differentiating network (with C1).
R2	Part of voltage divider (with R3, R7, and R8).
R3	Part of voltage divider (with R2, R7, and R8).
R4	Isolates set output from I1.
R5	Parasitic suppressor.
R6	Part of voltage divider (with R9 and R13).
R7	Part of voltage divider (with R2, R3, and R8).
R8	Part of voltage divider (with R2, R3, and R7).
R9	Part of voltage divider (with R6) ensures circuit stability (with C3).
R10	Limits current through I1 and I2.
R11	Part of voltage divider (with R12, R17, and R18).
R12	Part of voltage divider (with R11, R17, and R18).
R13	Cathode resistor for V1A and V1B.
R14	Part of decoupling network (with C5).
R15	Parasitic suppressor.
R16	Isolates clear output from I2.
R17	Part of voltage divider (with R11, R12, and R18).
R18	Part of voltage divider (with R11, R12, and R17).
R19	Part of differentiating network (with C7).
T1	Input transformer.
T2	Input transformer.
V1A	Flip-flop triode.
V1B	Flip-flop triode.

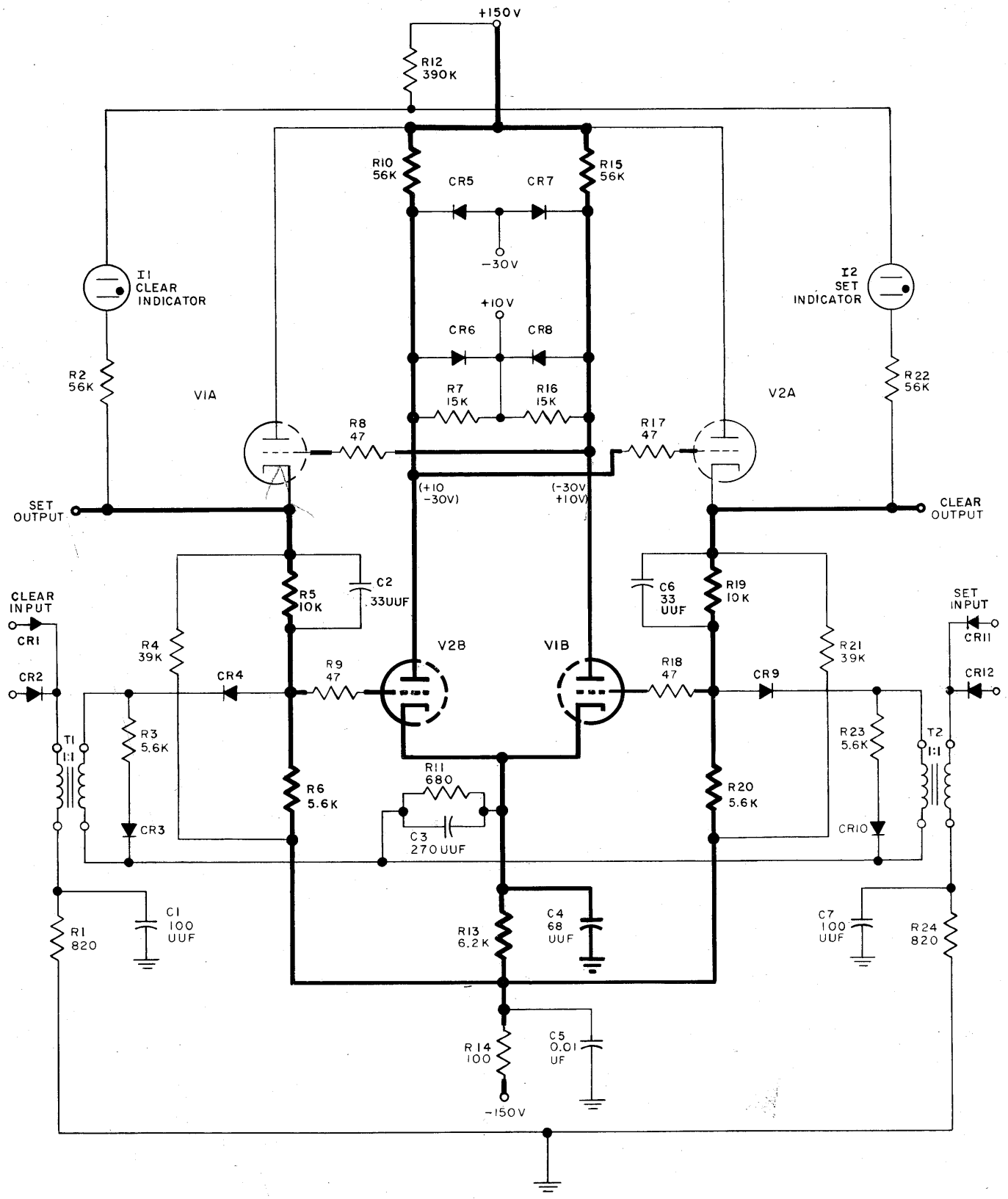


Figure 3–44. Flip-Flop, Model A, Schematic Diagram

TABLE 3–19. FLIP-FLOP, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Part of input diode biasing network (with R1).
C2	Speedup capacitor, improves rise and fall time.
C3	Ensures circuit stability (with R11).
C4	Cathode bypass capacitor.
C5	Part of decoupling network (with R14).
C6	Speedup capacitor, improves rise and fall time.
C7	Part of input diode biasing network (with R24)
CR1	Pulsed OR input diode.
CR2	Pulsed OR input diode.
CR3	Clips positive overshoot.
CR4	Isolates grid of V2B.
CR5	−30-volt clamp (clear output).
CR6	+10-volt clamp (clear output).
CR7	−30-volt clamp (set output).
CR8	+10-volt clamp (set output).
CR9	Isolates grid of V1B.
CR10	Clips positive overshoot.
CR11	Pulsed OR input diode.
CR12	Pulsed OR input diode.
I1	Indicates clear state.
I2	Indicates set state.
R1	Part of input diode biasing network (with C1).
R2	Isolates set output from I1.
R3	Current-limiting for CR3.
R4	Part of cathode load for V1A with R5 and R6.
R5	Part of voltage divider (with R6).
R6	Part of voltage divider (with R5).
R7	Protection against failure of CR6.
R8	Parasitic suppressor.
R9	Parasitic suppressor.
R10	Plate load resistor for V2B.
R11	Ensures circuit stability (with C3).
R12	Limits current through I1 and I2.
R13	Cathode resistor for V1B and V2B.
R14	Part of decoupling network (with C5).
R15	Plate load resistor for V1B.
R16	Protection against failure of CR8.
R17	Parasitic suppressor.
R18	Parasitic suppressor.
R19	Part of voltage divider (with R20).
R20	Part of voltage divider (with R19).
R21	Part of cathode load for V2A with R19 and R20.
R22	Isolates clear output from I2.
R23	Current limiting for CR10.
T1	Input transformer.
T2	Input transformer.
V1A	Isolating cathode follower (plate of V1B from grid of V2B)
V1B	Flip-flop triode.
V2A	Isolating cathode follower (plate of V2B from grid of V1B).
V2B	Flip-flop triode.

The plate supply voltage for the $_{A}$FF is greater than that used on the $_{B}$FF and $_{C}$FF.

In order to minimize wiring capacitance which would slow down the $_{A}$FF, each of the twin triodes contains an amplifier and associated cathode follower in the same envelope.

The network consisting of resistor R1 and capacitor C1 connected to the return of the primary of T1 prohibits noise pulses from affecting the $_{A}$FF. Resistor R3, in series with diode CR3 across the secondary of T1, limits the current through CR3. Resistor R7 across diode CR6 (+10-volt clamp) prevents a large positive potential from being applied to the grid of V2A should CR6 open. The $_{A}$FF may have numerous diode inputs accompanying diodes CR1 and CR2.

Refer to table 3–19 for function of detail parts not discussed.

CHAPTER 12
SINGLE-SHOT MULTIVIBRATORS

12.1 DEFINITION AND DESCRIPTION

The single-shot multivibrator ($_{X}$SS) is a logic circuit which generates a level of predetermined duration when a standard pulse is applied to its input. Figure 3–45 depicts the logic block symbol of each multivibrator model with its associated outputs.

12.2 PRINCIPLES OF OPERATION

12.2.1 Basic Operation

The SS has one stable state; in this it differs from the flip-flop multivibrator, which has two stable states.

Figure 3–46 is a block diagram of an SS consisting of amplifiers A and B. Normally, amplifier B is conducting and amplifier A is cut off. This is the stable state of the SS.

An appropriate signal applied to the input will cause amplifier B to cut off and amplifier A to conduct. This change of state is maintained, for a predetermined period of time, by the RC network. The SS then returns to its stable state. The output level of the SS is down in its stable state and up in its nonstable state.

Figure 3–47 is a simplified diagram of the single-shot multivibrator. Initially, V2 conducts because its cathode is at B— and its grid is at ground potential. Because of the conduction of V2, resistors R3 and R4 between the plate of V2 and B— apply a potential to

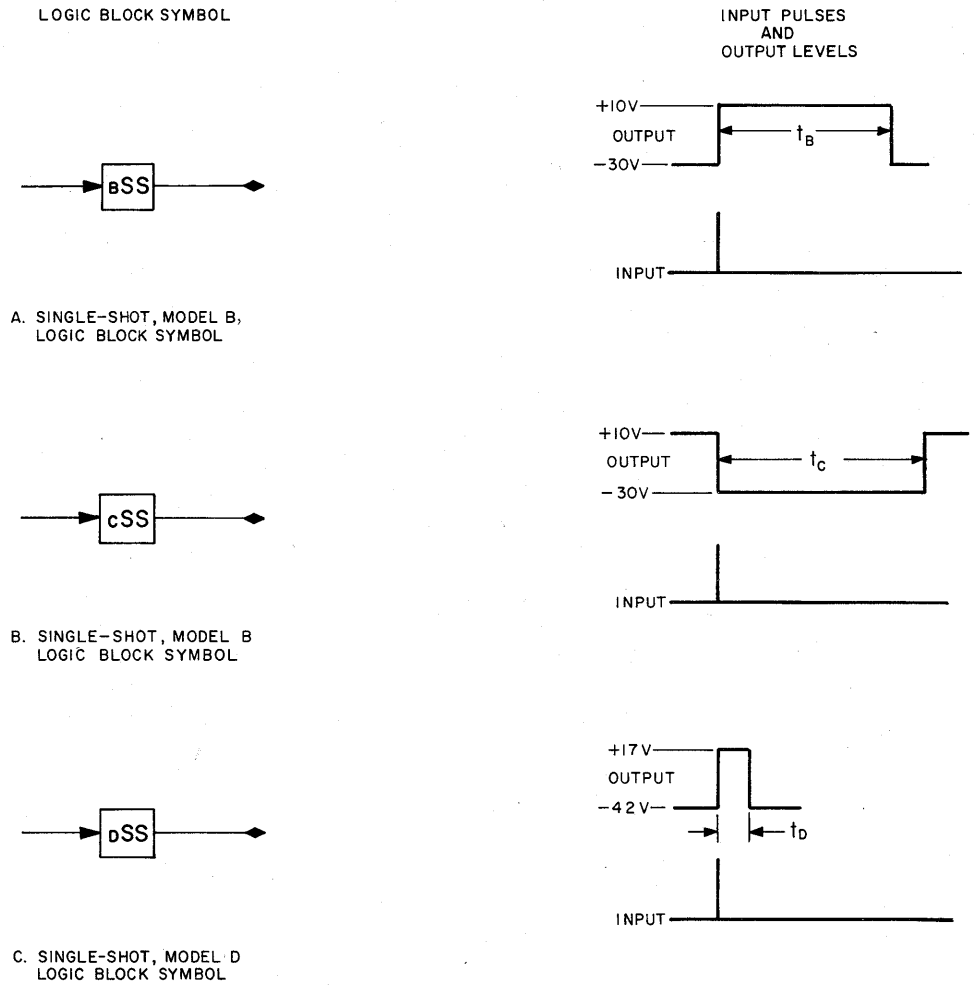


Figure 3–45. Single-Shot, Logic Block Symbols and Output Waveforms

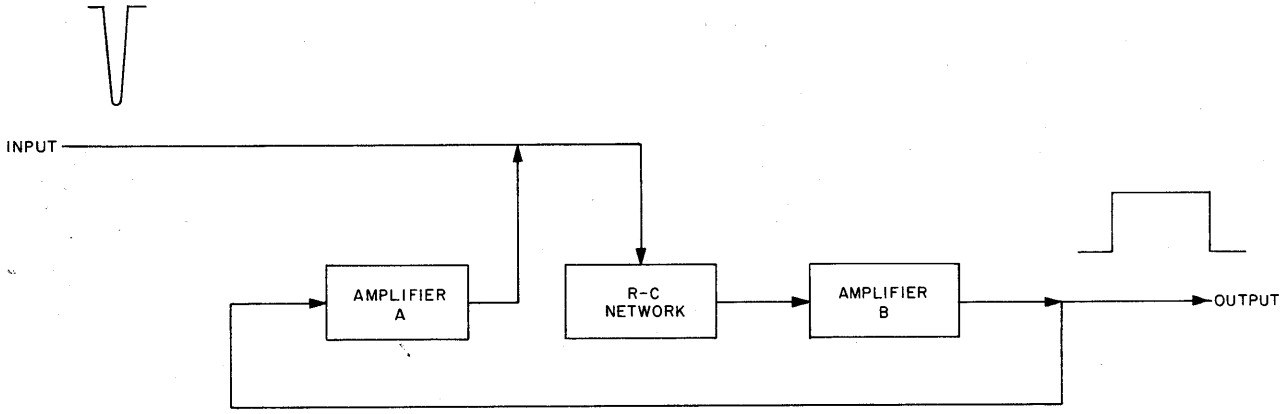


Figure 3–46. Single-Shot, Simplified Block Diagram

the grid of V1 sufficiently negative to maintain V1 at cutoff. With V1 cut off and V2 conducting, capacitor C1 charges to (B+) – (B—) through the cathode to grid circuit of V2.

A negative pulse applied at the input is coupled by capacitor C1 to the grid of V2, reducing the plate current through R6.

The reduction in voltage drop across R6 results in a rise of potential at the plate of V2. This rise is coupled to the grid of V1 through the voltage divider consisting of resistors R3 and R4. Tube V1 conducts, and its plate voltage falls. This negative shift in potential at the plate of V1 adds to the negative pulse input and is coupled by C1 to the grid of V2. The plate voltage of V2 rises, and this action continues in a regenerative manner until V2 is cut off. At this time, the plate potential of V2 is at maximum, the plate potential of V1 is at minimum, and the grid potential of V2 is below B—. As was previously indicated, the initial charge across C1 is B+ – B—, with the potential at the grid of V2 at B— and the potential at the plate of V1 at B+. When the plate of V1 falls, the grid potential of V2 falls a like amount (fig. 3–48). This is accomplished by the coupling action of capacitor C1 (the charge across a capacitor cannot change instantaneously). At the instant V2 is cut off, a positive level shift occurs, and the level is maintained until V2 resumes conduction. Tube V2 will remain cut off until the charge on C1 leaks off

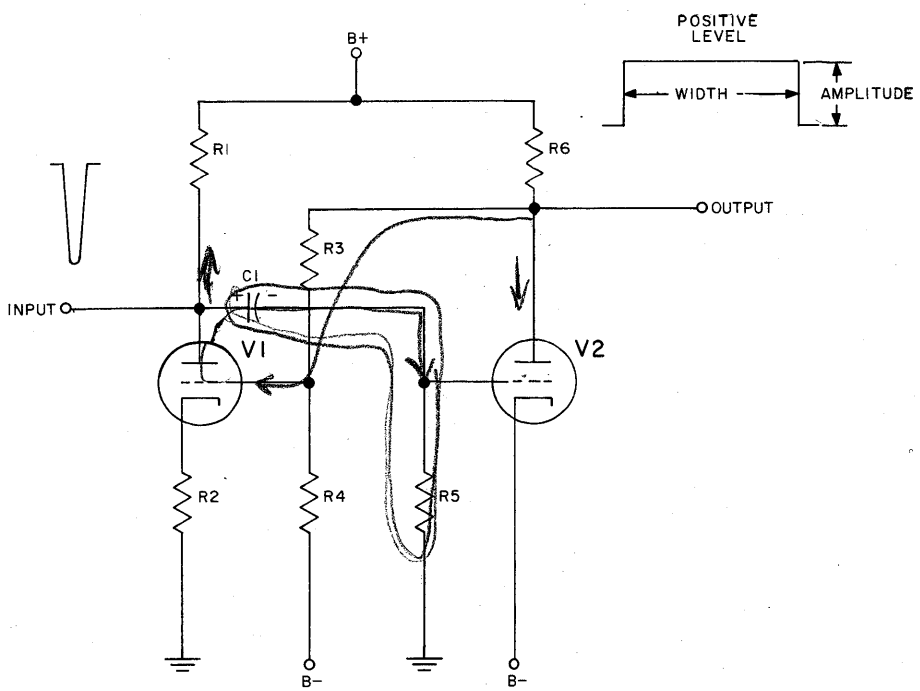
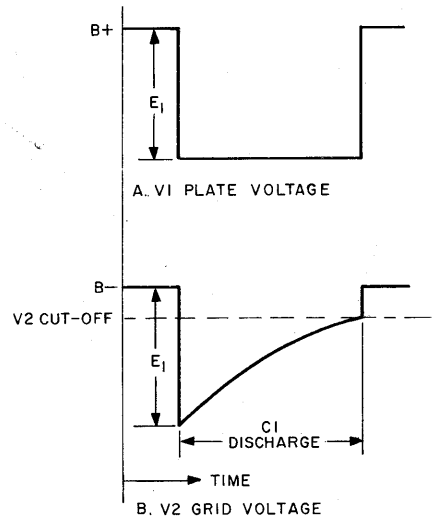


Figure 3–47. Single-Shot, Simplified Schematic Diagram



$E_1 = I_1 \times R1$ = VOLTAGE FALL AT PLATE OF V1 WHEN V1 CONDUCTS
WHERE:
I_1 = CURRENT THROUGH V1
R1 = PLATE LOAD RESISTANCE OF V1

Figure 3–48. V1 Plate Voltage and V2 Grid Voltage

through R5. As the charge on C1 is decreased, the grid of V2 approaches B— and reaches the point where V2 conducts. Current through V2 causes a fall in voltage at the plate of V2. This fall is coupled to the grid of V1 through resistors R3 and R4. The plate of V1 rises, and regenerative action returns the SS to its stable state (V1 cut off and V2 conducting). In the stable state, the grid and cathode of V2 are at B—, and the plate potential of V2 is reduced to its minimum value; hence, the output level falls (fig. 3–47). The width of the output waveform (the time required for capacitor C1 to discharge sufficiently to enable V2 to conduct) is determined by the capacity of C1 and the resistance of R5. The duration of the up level output is predetermined by, and directly proportional to, the product of C1 and R5: an increase of either C1 or R5 increases the time; a decrease of either C1 or R5 decreases the time.

Figure 3–49 depicts the grid and plate voltage waveforms of C2 for varying values of C1 and R5. From this figure, it can be seen that the width of the positive level output is dependent upon values of C1 and R5.

12.2.2 Detailed Operation, Single-Shot, Model B

Figure 3–50 is a composite schematic diagram of the $_B$SS. Table 3–20 is the associated list of detail parts and their functions. The $_B$SS produces a +10-volt (up) level for a predetermined duration when a standard pulse is applied to its input. The range of duration of the up level is from 1 to 100,000 microseconds and is determined by the values of C1 and R8. Two input circuits are employed to cover the range. The high-speed input circuit is used for the range of 1 to 4 microseconds. The low-speed input circuit is used for the range of 4 to 100,000 microseconds. Cathode follower V2A increases the load-driving capabilities of the $_B$SS.

The stable state of $_B$SS is determined by the considerations that follow. Tube V1B conducts because its grid is returned to ground and its cathode is at —150 volts. With V1B conducting, the junction of plate load

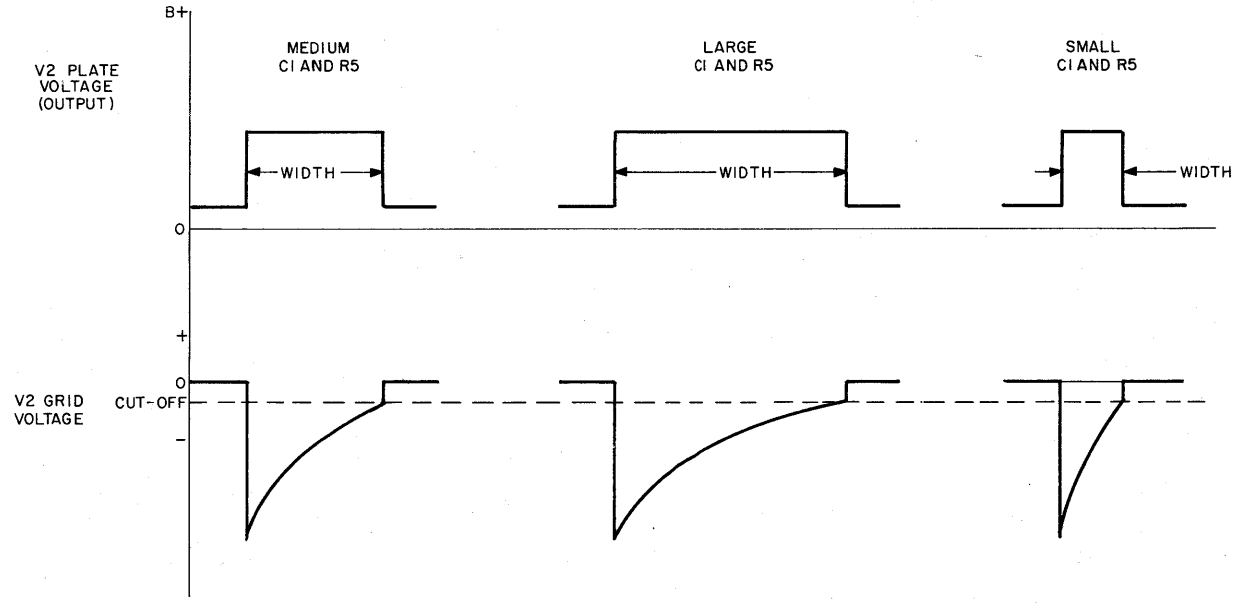


Figure 3–49. Plate and Grid Voltages of V2 for Varying Values of C1 and R5

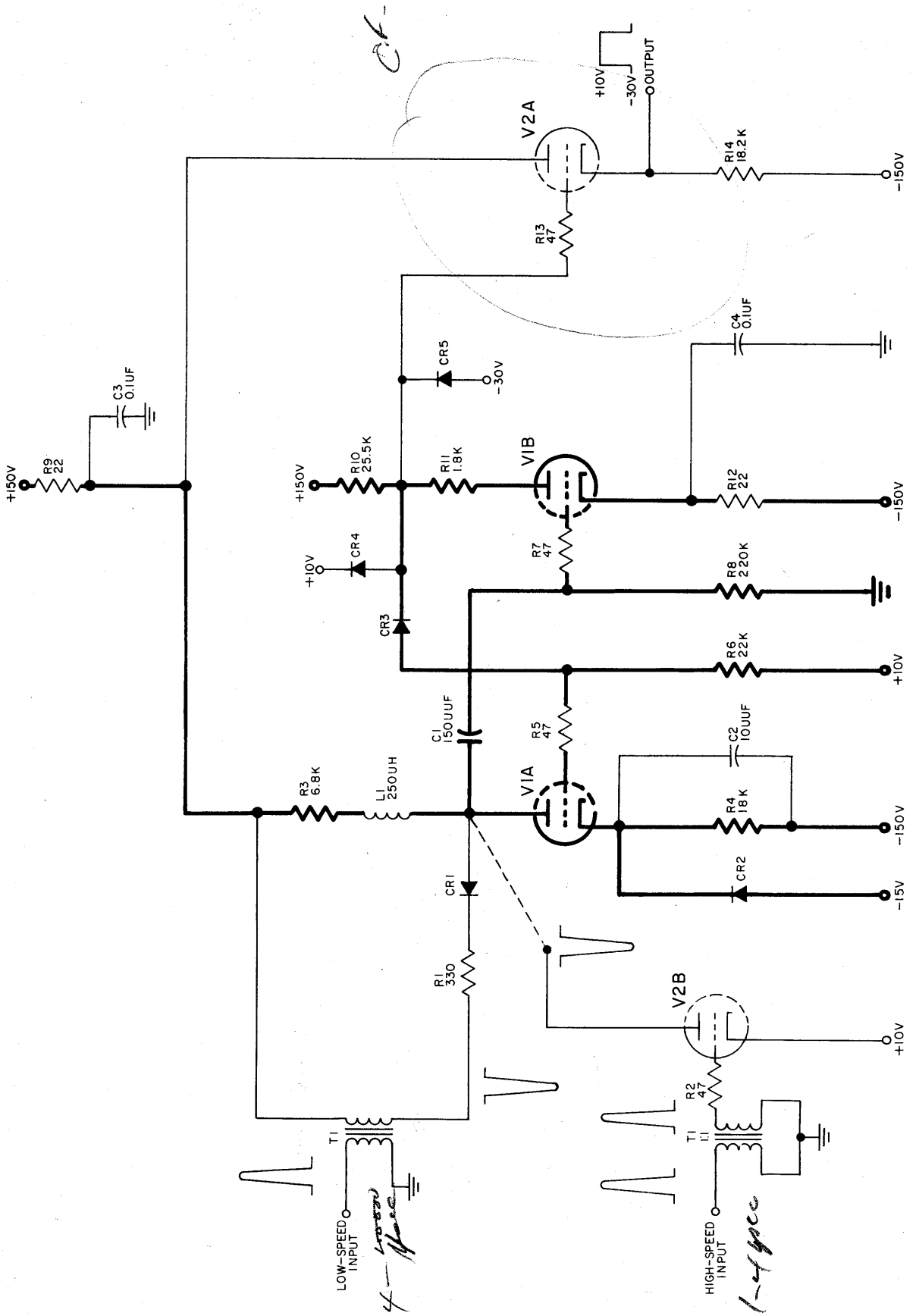


Figure 3–50. Single-Shot, Model B, Schematic Diagram

resistors R10 and R11 is maintained at —30 volts by diode CR5. Diode CR3, in series with R6, conducts, maintaining the grid of V1A at —30 volts. Diode CR2, in series with R4 between —15 volts and —150 volts, conducts, maintaining the cathode of V1A at —15 volts. This —15-volt bias (—15 volts at the cathode and —30 volts at the grid) is sufficient to hold V1A cut off. The plate potential of V1A is at the plate supply potential, +150 volts. Consider the path between +150 volts and —150 volts, consisting of R9, R3, L1, C1, and R7 and the grid and cathode of V1B. With V1A cut off and V1B conducting, capacitor C1 charges to 300 volts [+150 volts − (—150 volts)] = 300 volts through this path. Since the grid of cathode follower V2A, connected to the junction of resistors R10 and R11, is clamped at —30 volts, the output at the cathode of V2A is a —30-volt level.

Therefore, in the stable state of the $_{B}$SS, capacitor C1 is charged to 300 volts, V1A is cut off, V1B conducts, and V2A produces an output of —30 volts.

When a standard pulse is applied to the primary of input transformer T1, a negative pulse appears at the plate of V1A. Capacitor C1 couples this negative pulse to the grid of V1B, reducing current through V1B. The resultant rise of plate voltage initiates the regenerative action discussed in 12.2.1. The $_{B}$SS assumes its unstable state (V1A conducting and V1B cut off). With V1B cut off, CR4 conducts, and the junction of plate load resistors is clamped at +10 volts, maintaining the grids of V1A and V2A at +10 volts. As a result, the output of V2A rises and is held at +10 volts, and the plate of V1A falls and is held at a voltage below +150 volts by the voltage drop across R3. Initially, the unstable state of the $_{B}$SS is characterized by the following conditions: V1A conducts, V1B is cut off, the output of V2A is at +10 volts, and capacitor C1 is charged to 300 volts. This unstable state is maintained until the charge on capacitor C1 is discharged through R8 sufficiently to raise the grid of V1B above cutoff. As soon as V1B conducts, regenerative action is initiated, and the $_{B}$SS returns to its stable state.

The low-speed input circuit, consisting of T1, R1, and CR1, is used when the required single-shot output width (delay) is between 4 and 100,000 microseconds. For this application, the value of C1 varies between 68 micromicrofarads and 0.5 microfarad, and R6 varies between 220K and 700K. The specific values are determined by the delay required.

A standard pulse applied to the primary of T1 appears as a negative pulse across the secondary. Diode CR1 passes this negative pulse to the plate of V1A. This diode serves to isolate the plate circuit of V1A from the input. Resistor R1 prohibits noise pulses from triggering the SS when a large value of capacitance is used for C1.

TABLE 3–20. SINGLE-SHOT MULTIVIBRATOR, MODEL B, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Determines duration of unstable state (with R8).
C2	Cathode bypass capacitor for V1A.
C3	Part of decoupling network (with R9).
C4	Part of decoupling network (with R12).
CR1	Isolates plate circuit of V1A from input.
CR2	Clamps cathode of V1A at —15 volts.
CR3	Coupling diode between plate circuit of V1B and grid of V1A.
CR4	Clamps V1B output at +10 volts.
CR5	Clamps V1B output —30 volts
L1	Part of plate load for V1A and V2B, peaking coil.
R1	Prohibits noise pulses.
R2	Parasitic suppressor.
R3	Part of plate load for V1A and V2B (with L1).
R4	Cathode resistor for V1A.
R5	Parasitic suppressor.
R6	Grid return for V1A.
R7	Parasitic suppressor.
R8	Determines duration of unstable state (with C1).
R9	Part of decoupling network (with C3).
R10	Part of plate load for V1B (with R11).
R11	Part of plate load for V1B (with R10).
R12	Part of decoupling network (with C4).
R13	Parasitic suppressor.
R14	Cathode load for V2A.
T1	Input transformer.
V1A	Single-shot triode.
V1B	Single-shot triode.
V2A	Cathode follower triode.
V2B	Plate-pullover triode.

When the output is delayed between 1 and 4 microseconds, the input circuit employing V2B is connected to the plate of V1B, and the other input circuit is removed. The value of C1 is then either 22 or 33 micromicrofarads, and R6 varies between 220K and 420K.

A standard pulse at the primary of T1 is peaked and applied to the grid of V2B. Plate load resistor R3 and inductor L1 provide the plate load for plate pullover tube V2B as well as for V1A. The plate current of V2B flows through R3 and L1, and an amplified inverted (negative) pulse appears at the plate of V1A. Because of this amplification, the output from V2A rises faster. (Rise time becomes more significant when the level output is up for short durations.)

Inductor L1 in the plate circuit of V1A speeds rise time for both long and short delays. Refer to table 3–20 for the function of detail parts not discussed.

12.2.3 Detailed Operation, Single-Shot, Model C

Figure 3–51 is a schematic diagram of the $_{C}$SS. Table 3–21 is the associated list of detail parts and their functions. This circuit produces a −30-volt level for a duration of from 4 to 100,000 microseconds for each standard pulse input. The output then returns to a +10-volt level (stable state).

The $_{C}$SS circuit is essentially the same as the $_{B}$SS; however, a modified inverter, V2A, precedes cathode follower V1A to invert the level. The voltage divider formed by resistors R12 and R13 couples the plate of V2B to the grid of V2A. Capacitor C5 speeds transition time. For up levels wider than 10 microseconds, R1 is shorted. Refer to table 3–21 for the function of detail parts not discussed.

12.2.4 Detailed Operation, Single-Shot, Model D

Figure 3–52 is a schematic diagram of the $_{D}$SS. Table 3–22 is the associated list of detail parts and their functions. The output of the $_{D}$SS in its stable state is a −42-volt level. For each standard pulse applied to its input, the $_{D}$SS produces a +17-volt level of 2.2-microsecond duration.

The $_{D}$SS circuit is the same as the $_{B}$SS, utilizing a pullover tube input with the modifications that follow. The positive rise of output from V2B is clamped to +30.8 volts by diode CR3 during the 2.2 microseconds this tube is cut off, permitting the $_{D}$SS output to rise to +17 volts. This +30.8-volt bias is obtained from the junction of divider resistors R7 and R8 between +90 volts and ground. Capacitor C4 maintains the voltage across R8 constant. Because of the heavy load requirement, the $_{D}$SS output circuit consists of paralleled cath-

TABLE 3–21. SINGLE-SHOT MULTIVIBRATOR, MODEL C, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Determines duration of unstable state (with R7).
C2	Cathode bypass capacitor for V1B.
C3	Part of decoupling network (with R10).
C4	Part of decoupling network (with R11).
C5	Speeds rise and fall time.
CR1	Isolates plate circuit of V1B from input.
CR2	Clamps cathode of V1B at −15 volts.
CR3	Coupling diode between plate circuit of V2B and grid of V1B.
CR4	Clamps V2B at +10 volts.
CR5	Clamps V2B output at −30 volts.
CR6	Clamps V2A output at +10 volts.
CR7	Clamps V2A output at −30 volts.
L1	Part of plate load for V1B, peaking coil.
R1	Prohibits noise pulses.
R2	Part of plate load for V1B (with L1).
R3	Cathode resistor for V1B.
R4	Parasitic suppressor.
R5	Grid return for V1B.
R6	Parasitic suppressor.
R7	Determines duration of unstable state (with C1).
R8	Part of plate load for V2B (with R9).
R9	Part of plate load for V2B (with R8).
R10	Part of decoupling network (with C3).
R11	Part of decoupling network (with C4).
R12	Part of voltage divider (with R13).
R13	Part of voltage divider (with R12).
R14	Parasitic suppressor.
R15	Part of plate load for V2A (with R16).
R16	Part of plate load for V2A (with R15).
R17	Parasitic suppressor.
R18	Cathode load for V1A.
T1	Input transformer.
V1A	Cathode follower triode.
V1B	Single-shot triode.
V2A	Inverter triode.
V2B	Single-shot triode.

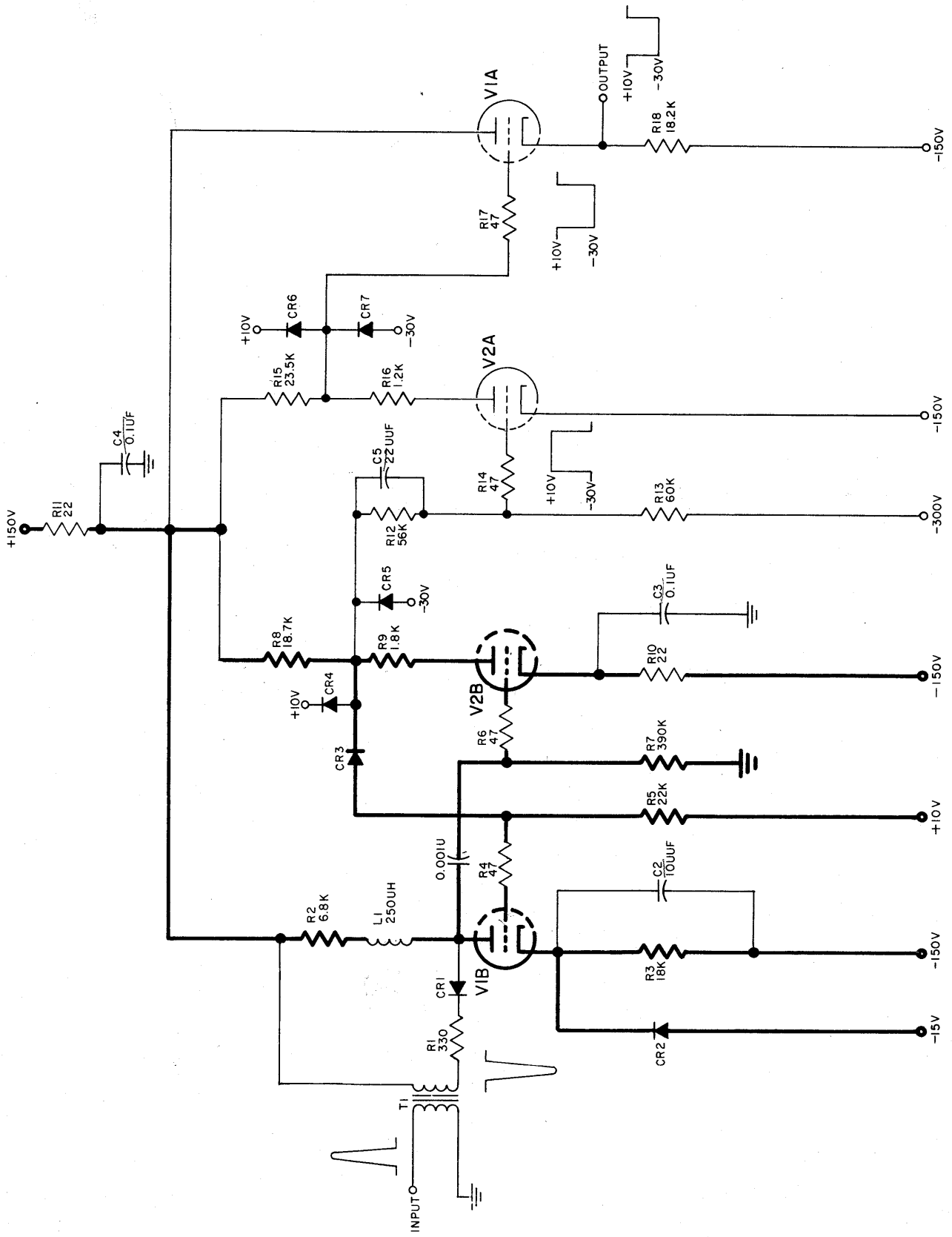


Figure 3–51. Single-Shot, Model C, Schematic Diagram

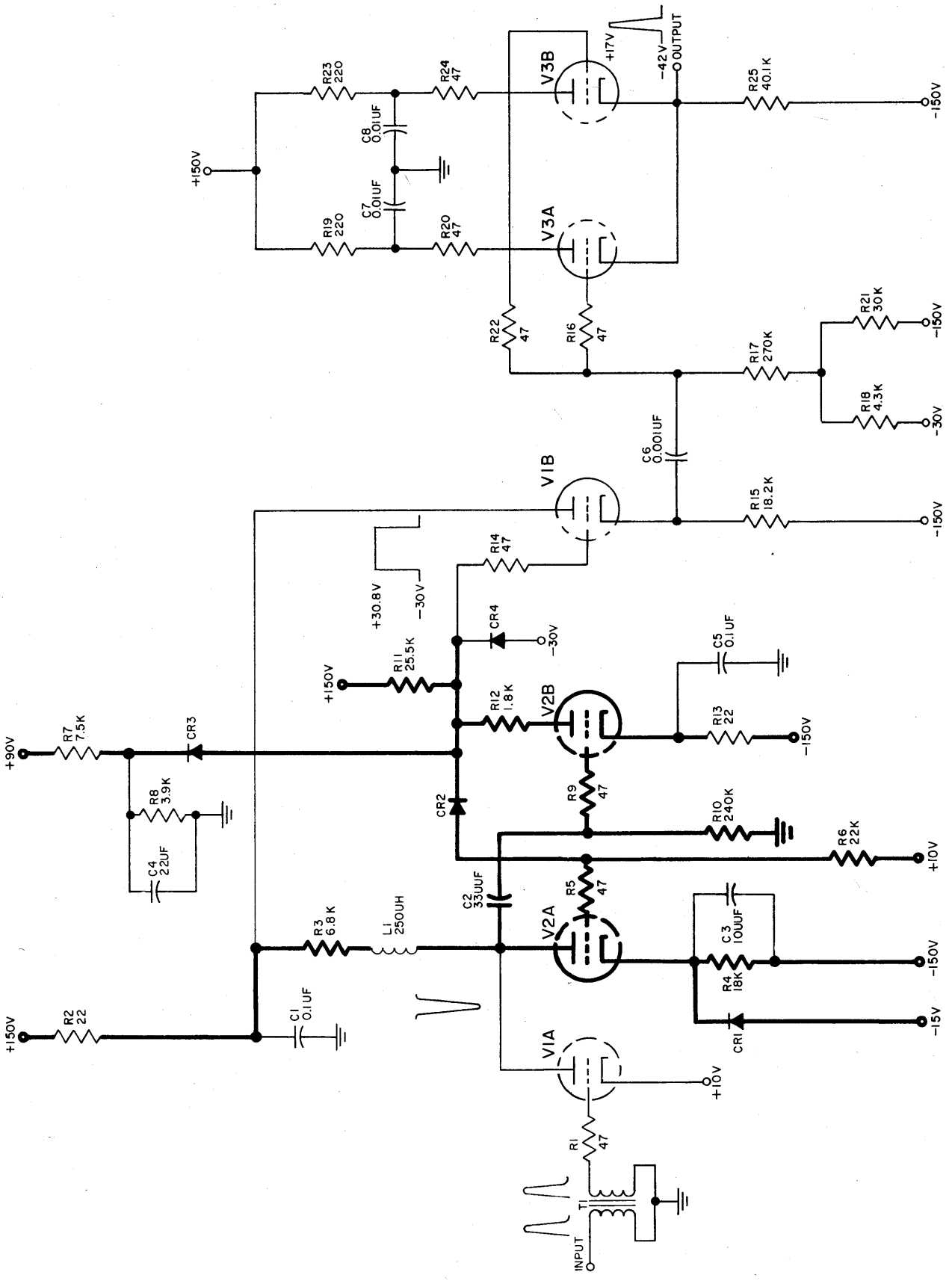


Figure 3–52. Single-Shot, Model D, Schematic Diagram

ode followers V3A and V3B. Capacitor C6 couples the output of cathode follower V1B to the grids of V3A and V3B. Grid return resistor R17 is common to V3A and V3B and is tied to the junction of the voltage divider composed of resistors R18 and R21. This divider develops a potential of —45 volts at the junction of R18 and R21, enabling the $_{D}$SS output to fall to —42 volts during the stable state.

When a standard pulse is applied to the input, the output pulse rises to +17 volts for 2.2 microseconds. (Refer to table 3–22 for the function of detail parts not discussed.)

TABLE 3–22. SINGLE-SHOT MULTIVIBRATOR, MODEL D, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Part of decoupling network (with R2).
C2	Determines duration of unstable state (with R10).
C3	Cathode bypass capacitor for V2A.
C4	Maintains voltage across R8 constant.
C5	Part of decoupling network (with R13).
C6	Couples cathode of V1B to grids of V3A and V3B.
C7	Part of decoupling network (with R19).
C8	Part of decoupling network (with R23).
CR1	Clamps cathode of V2A at —15 volts.
CR2	Coupling diode between plate circuit of V2B and grid of V2A.
CR3	Clamps V2B output at +30.8 volts.
CR4	Clamps V2B output at —30 volts.
L1	Part of plate load for V1A and V2A, peaking coil.
R1	Parasitic suppressor.
R2	Part of decoupling network (with C1).
R3	Part of plate load resistor for V1A and V2A (with L1).
R4	Cathode resistor for V2A.
R5	
R6	Grid return for V2A.
R7	Part of voltage divider (with R8).
R8	Part of voltage divider (with R7).
R9	Parasitic suppressor.
R10	Determines duration of unstable state (with C2).
R11	Part of plate load for V2B (with R12).
R12	Part of plate load for V2B (with R11).
R13	Part of decoupling network (with C5).
R14	Parasitic suppressor.
R15	Cathode load for V1B.
R16	Parasitic suppressor.
R17	Grid return resistor for V3A and V3B.
R18	Part of voltage divider (with R21).
R19	Part of decoupling network (with C7).
R20	Parasitic suppressor.
R21	Part of voltage divider (with R18).
R22	Parasitic suppressor.
R23	Part of decoupling network (with C8).
R24	Parasitic suppressor.
R25	Cathode load for V3A and V3B.
T1	Input transformer.
V1A	Plate-pullover triode.
V1B	Cathode follower triode.
V2A	Single-shot triode.
V2B	Single-shot triode.
V3A	Cathode follower triode.
V3B	Cathode follower triode.

CHAPTER 13

PULSE GENERATORS, MODELS A, B, C, D, AND E

13.1 DEFINITION AND DESCRIPTION

Pulse generators (PG's) are logic circuits which provide standard pulse outputs for appropriate inputs. Figure 3–53 is the logic block symbol of the several model groups. Pulse generators, models A, B, and C, are essentially the same circuit, the only difference being the means of input. Model A is actuated by hand-operated switching at a maximum repetition rate of 240 pulses per minute; model B, by a cam-operated switch at a maximum rate of 3,600 pulses per minute; model C, by a positive level shift at a maximum rate of 30,000 shifts per minute. The output of each is a standard pulse.

The model D input is a rapid shift in standard level from −30 volts to +10 volts. The output is a nonstandard pulse. The model E input is a standard level shift from +10 volts to −30 volts. The output is a standard pulse.

13.2 PRINCIPLES OF OPERATION

13.2.1 Basic Operation, Models A, B, and C

Models A, B, and C consist basically of an input circuit, a tetrode thyratron, and an output transformer. These pulse generators produce standard pulses whenever a switch is actuated in the input grid circuit or, as in model C, a positive shift in voltage is applied to the input.

13.2.2 Detailed Operation, Models A, B, and C

Figure 3–54 is a schematic diagram for the models A, B, and C pulse generators. Table 3–23 is the associated list of detail parts and their functions.

With application of power, tetrode thyratron V1 is biased below critical grid voltage by the −15 volts applied to the grid through resistor R3 and R5. Capacitor C1 charges to −150 volts through resistor R2. When discharge path P1 is completed, C1 discharges through resistor R1. The change in potential on the grid side of C1 is coupled to the control grid of thyratron V1 through capacitor C2. The potential at the juncture of capacitor C2 and resistor R2 was −150 volts. The potential at the juncture of capacitor C2 and R3 was −15 volts. The capacitor only passes the change in levels, −150 to 0 volts, not the level itself; therefore, the upward change of potential rises from −15 volts to + 135 volts.

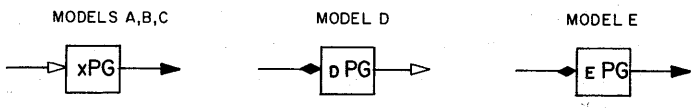


Figure 3–53. Pulse Generators, Logic Block Symbols

This positive potential exceeds that required to ionize the thyratron, resulting in the flow of grid and plate current. The grid current flowing through limiting resistor R5 maintains the grid at cathode potential. Capacitor C3 discharges through the primary of transformer T1 and the thyratron V1 until the plate of V1 reaches extinction potential. Transformer T1 is connected so that a positive output pulse results. This transformer, together with C3 and R4, shapes the pulse. The value of terminating resistor R7 will vary with the value of output load.

13.2.3 Circuit Refinements, Models A, B, and C

While the thyratron is conducting, the shield grid draws current, and a representative pulse appears across current limiting resistor R8, for testing purposes.

The only difference between model B and model A is in the value of resistor R2. In model B, the value for resistor R2 is 0.2 megohm. The reduction in the resistance of R2 decreases the charging time for capacitor C1, permitting the circuit to be actuated at a higher repetition rate by a cam-operated switch.

Model C is triggered by a positive level shift at capacitor C2. Resistor R3 and capacitor C2 convert this positive level shift into a positive trigger at the grid side of C2. Capacitor C2 discharges through the now conducting grid and resistors R5 and R3. The trigger generating components, R1, C1, P1, and R2, are not used. A composite schematic diagram of models A, B, and C is shown in figure 3–54.

An optional arrangement in the form of a special switch (P2) is incorporated in the circuit as shown in figure 3–54. This switch eliminates the possibility of multiple output pulses caused by switch (P1) bounce. Removing the +250-volt plate supply before P1 is closed prevents capacitor C1 from charging during the bounce period and eliminates the possibility of accidental triggering of thyratron V1. Refer to table 3–23 for the function of detail parts not discussed.

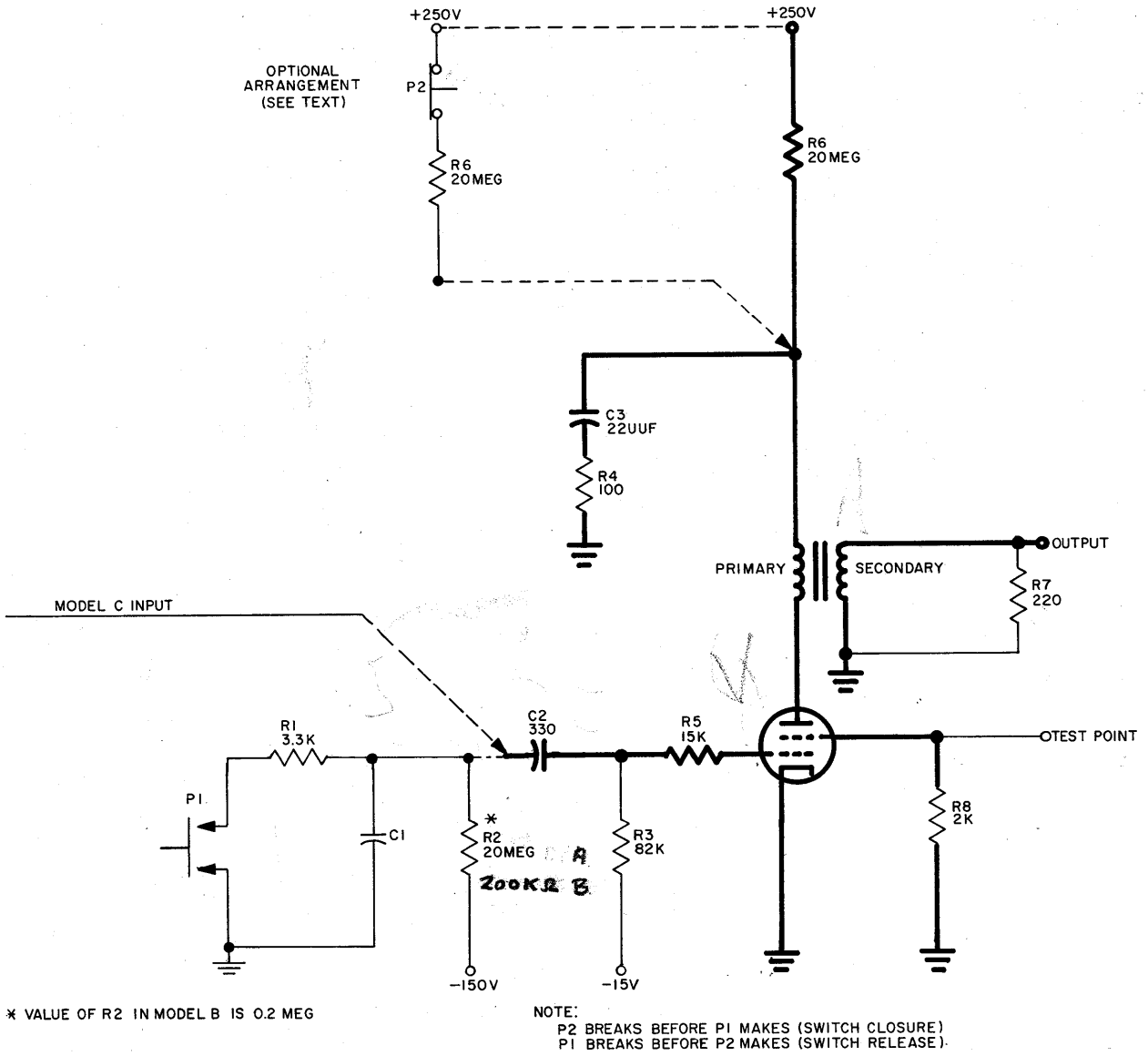


Figure 3–54. Pulse Generators, Models A, B, and C, Schematic Diagram

13.2.4 Basic Operation, Model D

This blocking-oscillator type pulse generator consists of a plate pullover triode, a tetrode-connected oscillator, and a pulse-shaping transformer. A shift from the down to the up level at the input is necessary to trigger the circuit. The output is a standard pulse.

13.2.5 Detailed Operation, Model D

A schematic diagram of the $_{D}$PG is shown in figure 3–55. Table 3–24 is the associated list of detail parts and their functions.

With the application of power to the pulse generator, both tubes are cut off. Tube V1 is maintained at cutoff by —15 volts applied to the grid through resistors R1 and R2. Tube V2 is cut off by —30 volts applied to the control grid through resistor R3 and the secondary of transformer T1. A positive level shift is applied to the grid of triode V1 through coupling capacitor C2, driving V1 into conduction. Plate current then flows through the primary of transformer T1, inducing a voltage in the secondary. The transformer is so connected that an increase of current in the primary causes the grid of pentode V2 to become positive, overcoming the —30-volt cutoff bias. With tube V2 conducting, additional current flows in the primary of transformer T1, increasing the positive voltage on the control grid of tube V2. Plate current increases until plate saturation is reached. Plate current is now constant, and the induced voltage on the secondary drops to 0 volt. The unopposed —30-volt bias cuts off tube V2, returning it to its original state. The resultant output pulse developed

TABLE 3–23. PULSE GENERATORS, MODELS A, B, AND C, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	USED ON	FUNCTION
C1	A & B	Part of trigger generating network (with P1, R1, and R2).
C2	A, B, & C	Grid coupling V1.
C3	A, B, & C	Supplies current to tetrode V1 and aids in pulse forming.
P1	A & B	Part of trigger generating network (with C1, R1, and R2).
P2	A & B	Spurious pulse prevention.
R1	A & B	Part of trigger generating network (with P1, R2, and C1).
R2	A & B	Part of trigger generating network (with C1, P1, and R1).
R3	A, B, & C	Part of pulse forming network (with C3 and T1).
R4	A, B, & C	Grid return.
R5	A, B, & C	Grid limiting.
R6	A, B, & C	Charging resistor for C3.
R7	A, B, & C	Terminating resistor.
R8	A, B, & C	Grid return for V2 (test point).
T1	A, B, & C	Impedance matching and pulse-shaping transformer.
V1	A, B, & C	Thyratron tetrode.

TABLE 3–24. PULSE GENERATOR, MODEL D, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Decoupling network (with R3).
C2	Grid coupling capacitor for V1.
C3	Decoupling network (with R2).
C4	Decoupling network (with R4).
C5	Decoupling network (with R8).
C6	Output coupling capacitor for V2.
CR1	Damping diode for positive overshoot.
CR2	Damping diode for positive overshoot.
R1	Grid return for V1.
R2	Decoupling network (with C3).

SYMBOL REFERENCE	FUNCTION
R3	Decoupling network (with C1).
R4	Decoupling network (with C4).
R5	Cathode load resistor.
R6	Parasitic suppressor.
R7	Current limiting resistor for CR1 and CR2.
R8	Decoupling network (with C5).
T1	Pulse forming and feedback to grid of V2.
V1	Plate pullover triode.
V2	Tetrode-connected pentode.

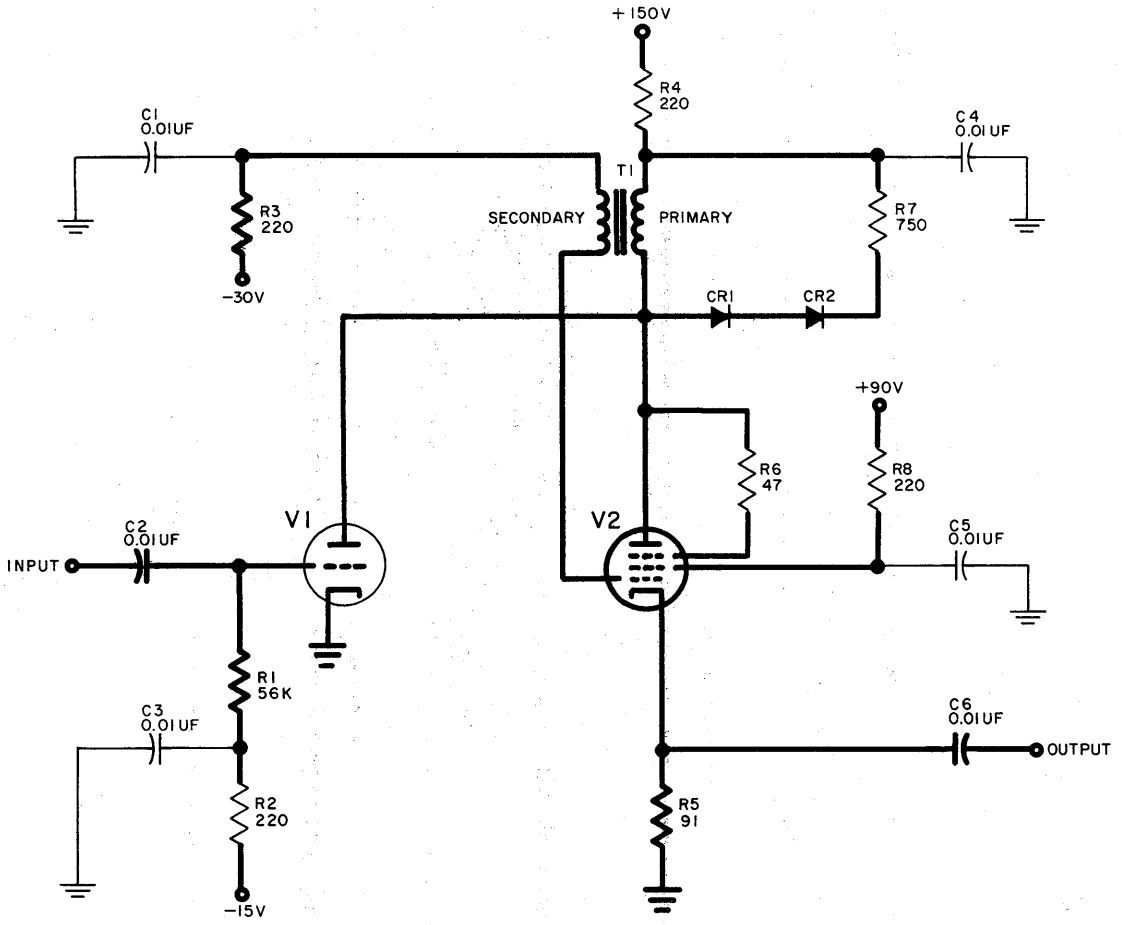


Figure 3–55. Pulse Generator, Model D, Schematic Diagram

across resistor R5 is coupled to a load through capacitor C6.

Diodes CR1 and CR2 and resistor R7 damp out oscillations of transformer T1. Resistor R2 and capacitor C3, capacitor C5 and resistor R8, capacitor C4 and resistor R4, and capacitor C1 and resistor R3 form decoupling networks.

Refer to table 3–24 for the function of detail parts not discussed.

13.2.6 Detailed Operation, Model E

The $_{E}$PG consists of a duo-triode tube, a pulse transformer, a pentode tube, and an output transformer.

A schematic diagram of the $_{E}$PG is shown in figure 3–56. Table 3–25 is the associated list of detail parts and their functions.

When power is first applied to the $_{E}$PG, triode V1A conducts and triode V1B is cut off. Triode V1B and pentode V2 are cut off by the —15 volts applied to the control grid of each tube. Triode V1A conducts as a result of the 10-volt level applied to the input of the $_{E}$PG. When the level at the grid input of the $_{E}$PG shifts to —30 volts, tube V1A is cut off. With plate

TABLE 3–25. PULSE GENERATOR, MODEL E, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Decoupling network (with R3).
C2	Grid coupling capacitor for V1B.
C3	Decoupling network (with R7).
C4	Grid coupling capacitor for V1A.
C5	Grid coupling capacitor for V1B.
C6	Decoupling network (with R9).
C7	Grid coupling capacitor for V2.
C8	Decoupling network (with R11).
C9	Decoupling network (with R12).
C10	Decoupling network (with R14).
CR1	Damping diode.
L1	Peaking coil.
R1	Input isolating and limiting.

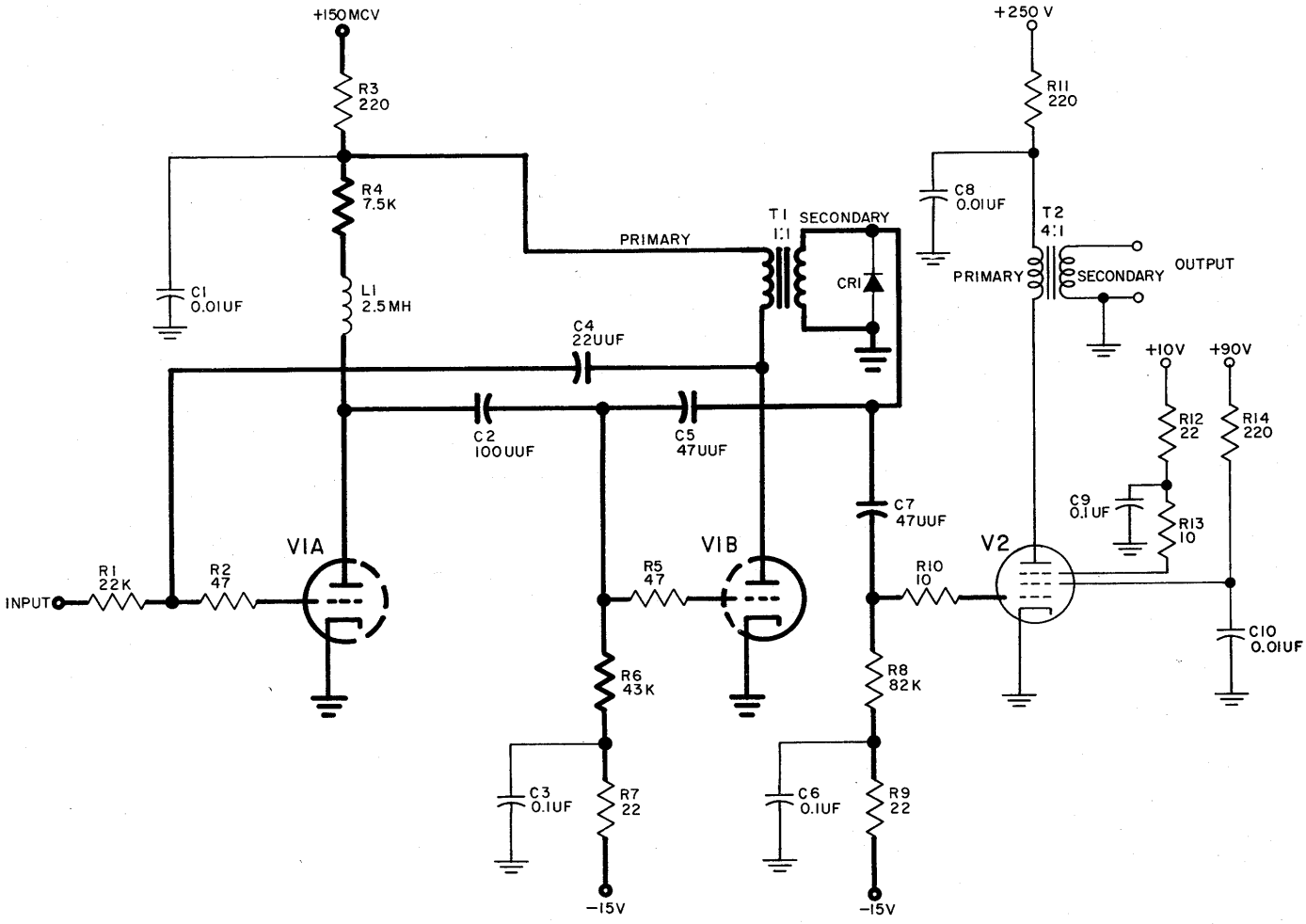


Figure 3–56. Pulse Generator, Model E, Schematic Diagram

TABLE 3–25. PULSE GENERATOR, MODEL E, FUNCTION OF DETAIL PARTS (cont'd)

REFERENCE SYMBOL	FUNCTION
R2	Parasitic suppressor.
R3	Decoupling network (with C1).
R4	Plate load V1A.
R5	Parasitic suppressor.
R6	Grid leak V1B.
R7	Decoupling network (with C8).
R8	Grid leak V2.
R9	Decoupling network (with C6).
R10	Parasitic suppressor.

REFERENCE SYMBOL	FUNCTION
R11	Decoupling network (with C8).
R12	Decoupling network (with C9).
R13	Parasitic suppressor.
R14	Decoupling network (with C10).
T1	Pulse forming.
T2	Transformer output coupling.
V1A	Plate pullover triode.
V1B	Blocking oscillator triode.
V2	Amplifier pentode.

current reduced to 0, the plate of triode V1A rises to +150 volts. The rise of plate voltage is coupled to the grid of triode V1B by capacitor C2, causing V1B to conduct. Increasing plate current through the primary of transformer T1 induces a potential on the secondary. This positive voltage coupled to the grid of V1B through capacitor C5 causes grid current to flow, charging capacitors C2 and C5.

The plate current through triode V1B increases until plate saturation is reached and then levels off. At this point, where the current through transformer T1 is constant, the voltage across the secondary drops to 0. The charges developed across capacitors C2 and C5, added to the —15-volt bias, holds triode V1B well past cutoff, blocking further operation of the $_{E}$PG, until this charge leaks off through resistor R6.

The positive shift in voltage that appears at the plate of V1B is coupled to the grid of V1A through capacitor C4. This results in a negative shift at the plate of V1A which, coupled to the grid of V1B, aids in bringing V1B to cutoff more rapidly.

The action just described maintains the $_{E}$PG in an insensitive state for several microseconds after cutoff of triode V1B is reached, eliminating the possibility of erroneous multiple pulse output.

The pulse at the secondary of transformer T1 is coupled to the grid of pentode V2 by capacitor C7. This pulse overcomes the —15-volt bias on the control grid of pentode V2, and the tube conducts. The resulting pulse of plate current through the primary of transformer T2 results in a standard pulse output. The 4-to-1 ratio of primary to secondary turns effects a 16-to-1 impedance match from the pentode V2 plate to the output. The transformer also shapes the output pulse.

A more detailed description of the amplifier section of this generator (V2) is found in Chapter 3. Refer to table 3—25 for the function of detail parts not discussed.

CHAPTER 14
DELAY UNIT GROUP

14.1 DEFINITION AND DESCRIPTION

Delay unit, model C ($_C$D), is a logic circuit consisting of a delay line and a delay line driver. Table 3–26 shows the logic block symbols for the delay unit and its component parts. The purpose of the delay unit is to delay information (a standard pulse) for a fixed length of time. The standard pulse is fed to the delay line by the delay line driver. It appears at the output of the delay line a fixed time after the initial pulse is applied to the input.

14.2 PRINCIPLES OF OPERATION

14.2.1 Detailed Operation of Delay Line

The delay line consists of a series of LC filter sections (see fig. 3–57). A standard pulse applied to the input of the delay line charges C1 in a finite period of time. The voltage developed across C1 causes current to flow through L1, charging C2. This process continues with L2 and C3, L3 and C4, and L4 and C5. Finally, C5 discharges through terminating resistor R1, producing a voltage pulse. This pulse will appear a fixed time after the standard pulse is applied to the input. The time difference between these pulses (the delay) is determined by the values of L and C and the number of LC sections. The nominal time difference of a delay unit is 0.5 microsecond. When a smaller delay is needed, the delay line may be tapped at one of the LC sections. For greater delays, lines are cascaded (connected in series).

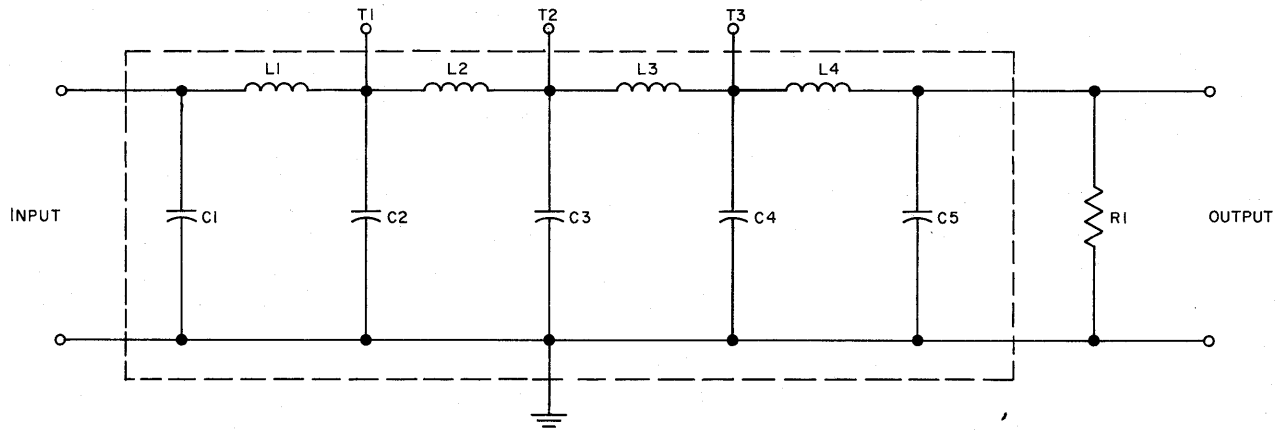


Figure 3–57. Typical Delay Line

TABLE 3–26. DELAY UNIT, LOGIC BLOCK SYMBOLS AND FUNCTIONS

NAME	LOGIC BLOCK SYMBOL	FUNCTION
Delay unit, model C ($_C$D)	$_C$D 0.5 usec	Delays information for a fixed period of time. Composed of delay line and driver.
Delay line	0.5 usec	Provides necessary delay.
Delay driver, model A ($_A$DD)	$_A$DD	Provides power amplification necessary to drive delay line.

14.2.2 Detailed Operation of Model A Delay Line Driver

Figure 3–58 is a schematic diagram of the model A delay line driver. Table 3–27 is the associated list of detail parts and their functions. Pulse power is required to drive the delay line because a 40-volt standard pulse is being fed to a 100-ohm load (the impedance of the delay line). The model A delay line driver provides this power. It is basically composed of an input transformer, a tetrode-connected pentode, and an output transformer. A standard pulse is applied to the input transformer. The output of the transformer is a positive pulse amplified by a factor of 3. This pulse is applied to the control grid of vacuum tube V1. Tube V1 is a tetrode-connected pentode; this arrangement provides more power output than a pentode. Bias considerably below cutoff is provided by a fixed —30 volts on the control grid. The pulse at the secondary of the input transformer overcomes this bias and causes V1 to conduct heavily. The resulting plate current flows through the primary of the output transformer. The negative-voltage pulse at the plate of V1 is inverted at the output of transformer T1, feeding a positive pulse to the delay line. Transformer T1 matches the high impedance of the plate of V1 to the low impedance of the delay line. It also steps down the voltage by a factor of 4, thereby increasing the current four times.

Decoupling networks are provided because the $_{A}DD$ is connected to common service voltage lines. These networks isolate the $_{A}DD$ from other circuits powered from the same supplies. Diode CR1 is a clamping diode for negative overshoots.

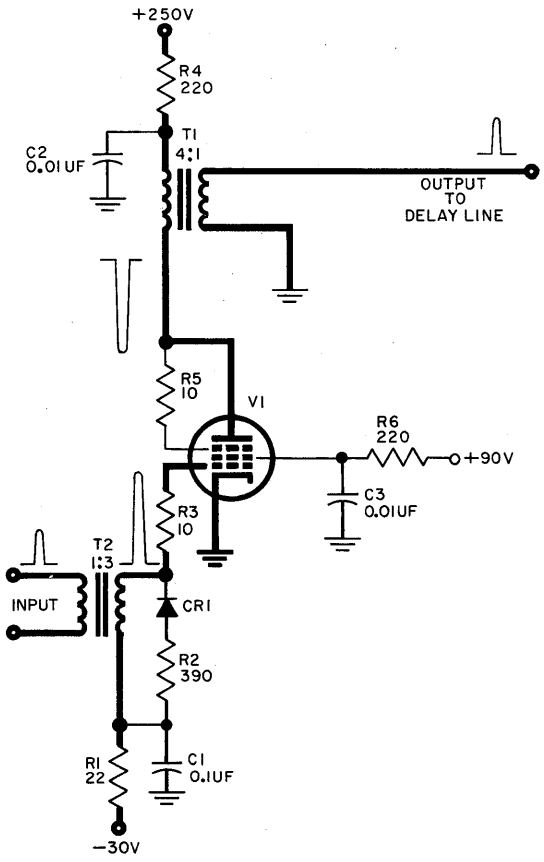


Figure 3–58. Delay Line Driver, Model A

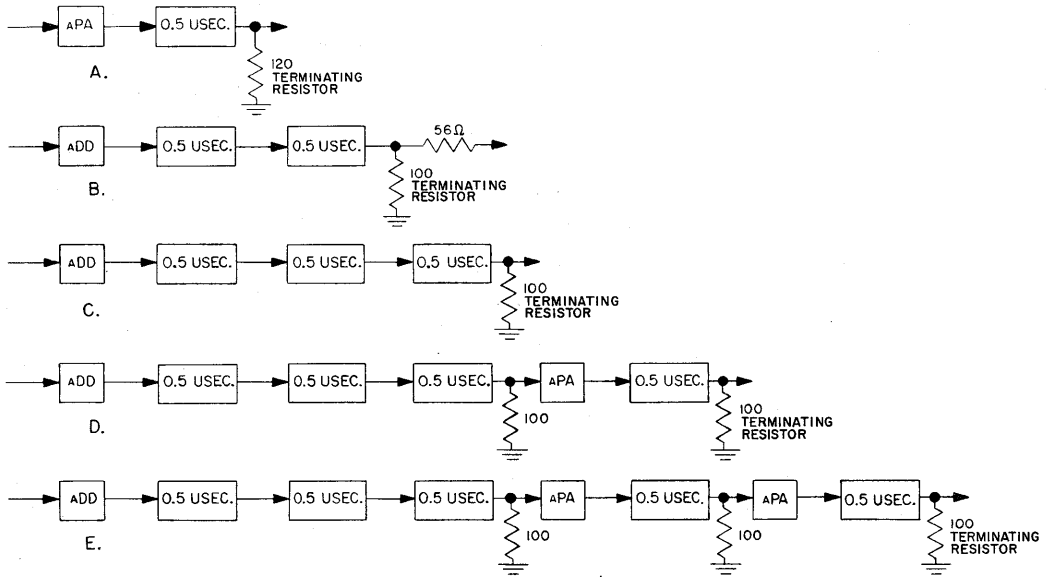


Figure 3–59. Typical Arrangements of Delay Units

When it is necessary to cascade delay lines for longer delays, the standard pulse is distorted beyond acceptable limits. To correct this condition, $_{A}$PA is used instead of an $_{A}$DD to drive each additional delay line. Arrangements of delay lines and driving sources are shown in figure 3–59. When tapped delay lines are used for delays shorter than 0.5 microsecond, series-limiting resistors are used to limit pulse amplitude. The values of these resistors depend on the load and on the position of the tap in the delay line. Refer to table 3–27 for the function of detail parts not discussed.

TABLE 3–27. DELAY LINE DRIVER, MODEL A, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
C1	Part of RC decoupling network (with R1).
C2	Part of RC decoupling network (with R4).
C3	Part of RC decoupling network (with R6).
R1	Part of RC decoupling network (with C1).
R2	Current-limiting resistor for CR1.
R3	Parasitic suppressor.
R4	Part of RC decoupling network (with C2).
R5	Parasitic suppressor.
R6	Part of RC decoupling network (with C3).
T1	Output transformer.
T2	Input transformer.
V1	Tetrode-connected pentode.

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