THEORY OF OPERATION

OF

DRUM SYSTEM

FOR

AN/FSQ-7

COMBAT DIRECTION CENTRAL

15 November 1956

Revised 1 April 1957

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PART 1
INTRODUCTION

CHAPTER 1
PURPOSE AND SCOPE OF MANUAL

The purpose of this manual is to provide a comprehensive description of the operation of the Drum System employed in AN/FSQ-7 equipment. The manual is intended to assist field engineers engaged in the maintenance of the Drum System and to aid in training other technical personnel who require detailed knowledge of the AN/FSQ-7 Combat Direction Central.

The manual is divided into four parts. Part 1 indicates the function of the Drum System as a part of the AN/FSQ-7 equipment, and describes the functional subdivisions of the Drum System itself. Part 1 concludes with an overall description of the composition and physical characteristics of the Drum System.

Part 2 presents a detailed description of the operation of the six main drums of the Drum System and of their associated circuits. Part 2 is organized to explain the primary function of the main drums. This function is the transfer of information between the Central Computer System and the Input, Output, and Display Systems of the AN/FSQ-7.

Part 3 describes the operation of the circuits connected with auxiliary memory drums C, D, E, F, G, and H. Part 3 presents the auxiliary drums as a medium capacity, medium access time, auxiliary storage facility for the Central Computer System.

Part 4 describes the special circuits and assemblies of the Drum System which are essential to the operation of the Drum System, but which are not included among the basic circuits employed by the system.

The manual concludes with an index which lists, in alphabetical order, the major circuits and assemblies of the Drum System. The page references in the index cite the pages on which either a functional or an operational description of the circuit may be found. If a circuit performs several functions, these functions are listed alphabetically as subcategories under the circuit name.

CHAPTER 2
DESCRIPTION OF DRUM SYSTEM

2.1 FUNCTION OF DRUM SYSTEM IN COMBAT DIRECTION CENTRAL AN/FSQ-7

The Drum System (fig. 1–1) of AN/FSQ-7 Combat Direction Central effects the exchange of information between the Central Computer System and the other systems of the Combat Direction Central. The component systems of the Combat Direction Central are illustrated in figure 1–2. During combat operations, tactical data is transferred from the Input System to the Central Computer System via the Drum System. Data from the Central Computer System is transferred through the Drum System to the Output and Display Systems.

The primary function of the Drum System in data transfers is to act as a time buffer. The Drum System can store information for as long as necessary; it has an average access time of 10 milliseconds (ms). The Drum System, being a storage device, performs no computations. Data is entered into, and removed from, the Drum System without alteration.

Tactical information to be applied to the Drum System for transfer to the Central Computer System arrives in large quantities and at random times. The Drum System stores this information until it is required by the Central Computer System. Tactical data processed by the Central Computer System for use in other systems of AN/FSQ-7 Combat Direction Central is applied to the Drum System at a relatively high rate of speed. The Drum System transmits this data to the other systems of the equipment at speeds compatible with their operation.

Central Computer System programs and subprograms are too extensive to be stored in the Central Computer System core memory in their entirety. Additional storage space is supplied by the Drum System. The access time of data stored in the Drum System (10 ms average), while longer than the access time of data stored in the core memory (6 microseconds (usec)), is still short enough to make the Drum System a valuable source of auxiliary memory space.

In addition to its storage function, another important function of the Drum System is the development of the timing information used by all systems of the Combat Direction Central except the Central Computer System. This timing information not only provides the systems with a means of timing and controlling operations, but also serves as a means of synchronizing these systems with the Drum System during data transfers. Synchronization of Drum System and Central Computer System operations is performed by circuit components within both systems.

Circuits are built into the Drum System to provide for rapid detection of Drum System malfunctions by allowing automatic testing by Central Computer System programs. Additional circuits permit testing to be performed under manual control. These circuits allow Drum System tests to be performed with the Drum System disconnected from the other systems of the Combat Direction Central. As a result, they serve as a valuable aid to installation as well as to maintenance.

Drum System operations are performed to rigorous reliability standards. Many self-checking circuits are included which reduce the time required to isolate the cause of faulty operation. Should faulty operation be produced by component failure, alarms and indicating circuits distributed throughout the Drum System would facilitate rapid detection and location of the failure.

The AN/FSQ-7 Combat Direction Central contains two Drum Systems and two Central Computer Systems (duplex system). One Drum and Central Computer System combination actively processes and transfers data. The other combination is in a standby state. When maintenance is to be performed on the active combination, the functions of the active Drum and Central Computer System are switched to the standby systems. In order to shorten the data-transfer time, intercommunication is maintained between active and standby equipment at all times. Intercommunication between Central Computer Systems is also used to enable the standby Central Computer System to check the operation of the active Central Computer System. The active Central Computer System constantly generates intercommunication data for transfer to the standby system. The circuits between computer and drums (CD) in the active Drum System transfer this intercommunication data from the active Central Computer System to the magnetic drums so that it may be stored and transferred to the standby Central Computer System. The transfer from the magnetic drum to the standby Central Computer System is through the CD circuits of the standby Drum System.

2.2 OPERATIONAL ANALYSIS OF DRUM SYSTEM

Drum System circuits fall into two major categories: those exchanging information with the Central Computer

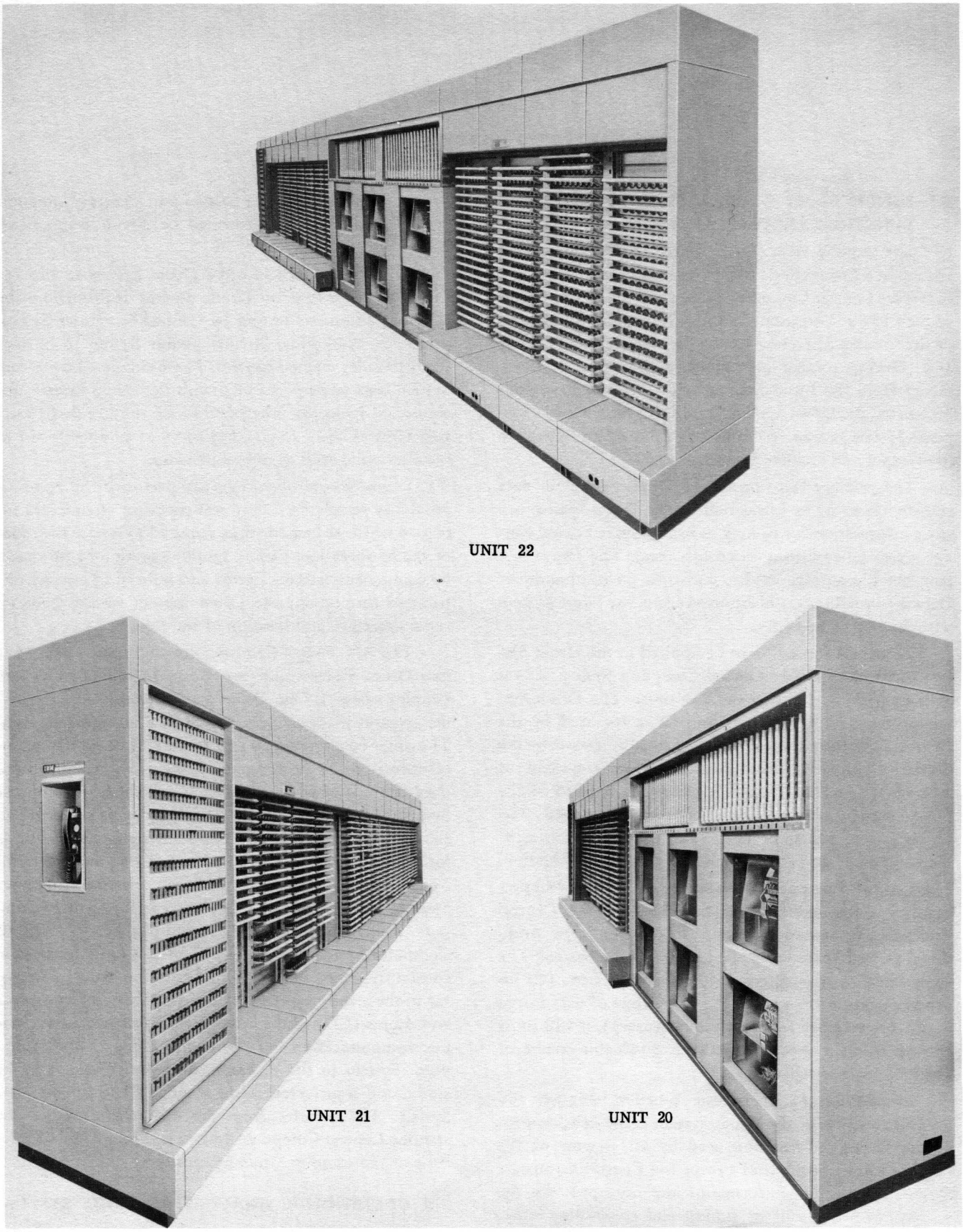


Figure 1–1. Drum System, Units 20, 21, and 22

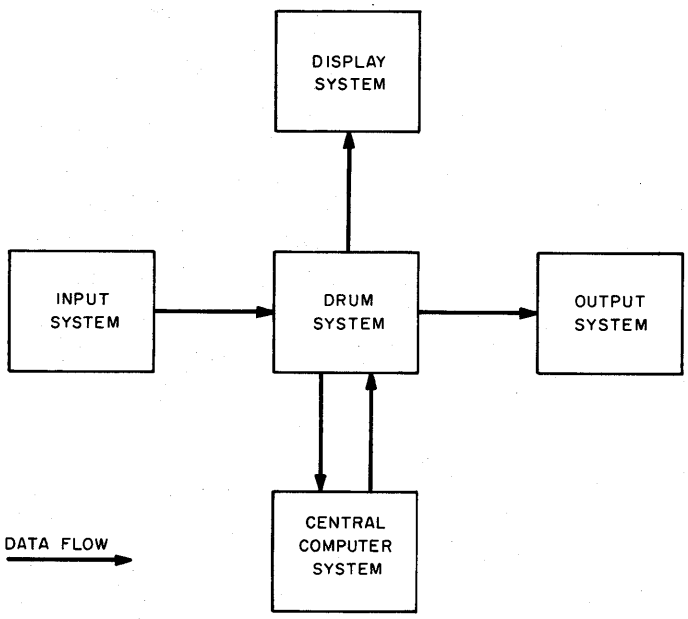


Figure 1–2. Component Systems of AN/FSQ-7, Block Diagram

System and those exchanging information with other systems. Information exchanges with the Central Computer System are known as CD operations. Information exchanges with other systems are known as OD (other than Central Computer System-Drum System) operations. In figure 1–3 are shown the major circuits of the main drums; the corresponding circuits for the auxiliary drums are shown in figure 1–4. For purposes of clarity, the test circuits are omitted. The function and relative position of the test circuits are described in 2.2.11.

The following subsections describe from a functional point of view the circuits and assemblies shown on figures 1–3 and 1–4, beginning with the drums themselves.

2.2.1 Magnetic Drums

The magnetic drums in the Drum System serve as electromagnetic storage devices. The number of registers available for data storage in the Drum System is large in relation to that in the core memory in the Central Computer System. Each drum has a capacity of approximately 405,504 information bits. The access time of drum-stored data is short in relation to the access time of the data stored on card and tape machines used in other portions of the Combat Direction Central. Drums, therefore, are storage devices that fulfill the requirements of medium access time and medium storage capacity.

Each magnetic drum is divided into logical divisions known as fields. Each field, except track display (TD) and radar data (RD) fields, contains 2,048 axially oriented registers, which are numbered consecutively about the circumference of the drum. One 33-bit information word can be stored in each register. All but one of the magnetic drums contain six fields which are named for the type of data they store. The RD drum has nine fields. Magnetic drums are named for the fields they contain. The LOG and MIXD drums are the only magnetic drums which contain more than one type of field. The names LOG and MIXD were evolved in the following manner: The letter L in LOG is the first letter of the long-range radar input field name; the letter O is the first letter of the output buffer field name; and the letter G is the first letter of the gap-filler input field name. Similarly, the letter M in MIXD is the first letter of the manual input field name; the letter I is the first letter of the intercommunication field name; the letter X is the first letter in the abbreviation for the crosstelling field name; and the letter D is the first letter in the digital display field name. All other magnetic drums contain only one type of field; each drum is named for the particular type field that it contains. (Refer to table 1–1.)

The access time to information stored on the magnetic drums averages 10 ms. The maximum access time is 20 ms (the time taken by one revolution), but successive data transfers can occur as rapidly as 10 usec apart. This access time is relatively fast when compared with that of tape or card machine storage devices, but is slower than the access time of the Central Computer System core memory (6 usec).

2.2.2 CD Field Selection and Switching Circuitry

The field selection and switching circuitry (figs. 1–3 and 1–4, logic drawings 1.1.1 and 1–2.1.1) performs two functions required for an information exchange between the drum fields and the Central Computer. It activates the field designated by the Central Computer and

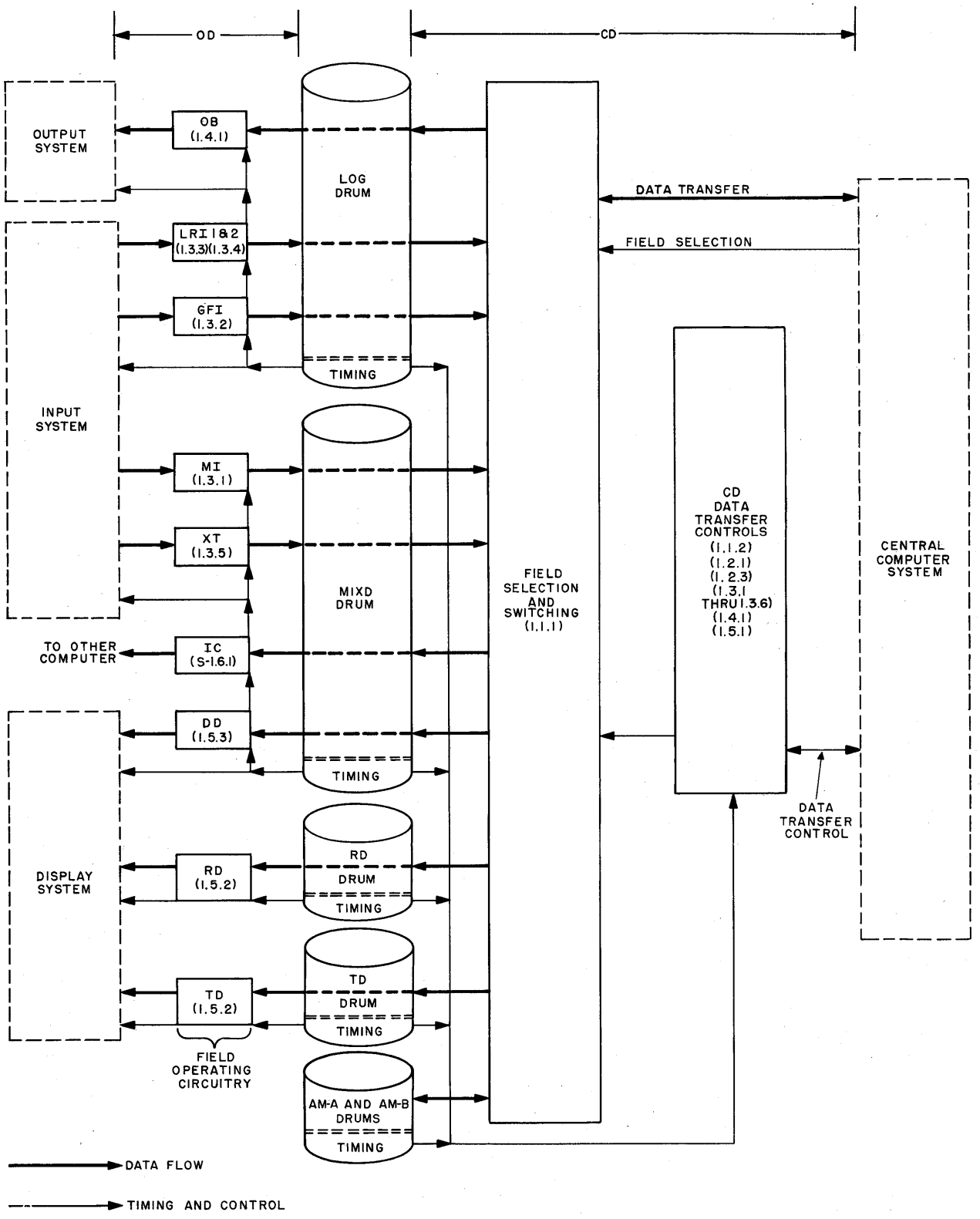


Figure 1–3. Operational Block Diagram of Main Drum Circuitry

that field only, and it conditions the timing and control circuits of the drum in which the field is located. These functions are accomplished by the decoding circuits and the diode switching circuits.

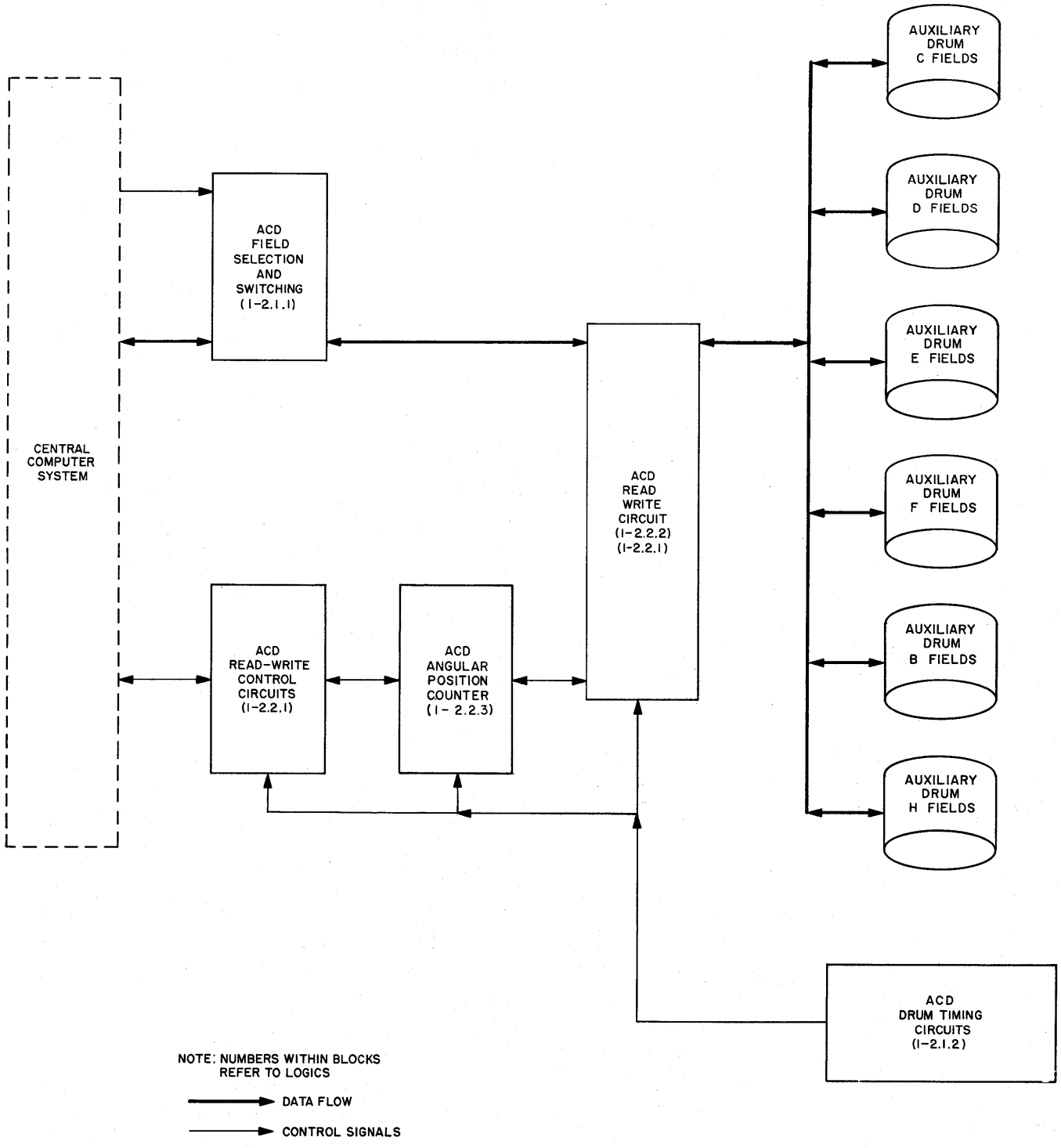


Figure 1–4. Operational Block Diagram of ACD Drum Circuitry

2.2.3 Drum Timing Circuitry

The drum timing circuitry, logic drawings 1.1.2 and 1–2.1.2, times the operations of the Drum System and of all other systems of the AN/FSQ-7 with which the drums exchange information, except the Central Computer. Each drum generates timing pulses for itself. The timing pulses are used to initiate and to effect the operations which cause the Drum System circuits to write and to read. They are also used to step the various counters used in the Drum System circuits.

TABLE 1–1. MAGNETIC DRUM AND FIELD DESIGNATIONS

DRUM DESIGNATION	DRUM ABBREVIATION	FIELD TYPE AND QUANTITY	FIELD ABBREVIATION
LOG	None	Long-range radar input (2)	LRI 1 and 2
		Output buffer (3)	OB 1, 2, 3
		Gap-filler input (1)	GFI
MIXD	None	Manual input (1)	MI
		Intercommunication (1)	IC
		Crosstelling (1)	XTL
		Spare crosstelling (1)	SP XTL
		Digital display (1)	DD
		Spare aux memory (1)	SP AM
Aux memory A	AM-A	Aux memory (6)	AM-A 1 to 6
Aux memory B	AM-B	Aux memory (6)	AM-B 7 to 12
Aux memory C	AM-C	Aux memory (6)	AM-C 13 to 18
Aux memory D	AM-D	Aux memory (6)	AM-D 19 to 24
Aux memory E	AM-E	Aux memory (6)	AM-E 25 to 30
Aux memory F	AM-F	Aux memory (6)	AM-F 31 to 36
Aux memory G	AM-G	Aux memory (6)	AM-G 37 to 42
Aux memory H	AM-H	Aux memory (6)	AM-H 43 to 48
Radar data	RD	Radar data (9)	RD 1 to 9
Track display	TD	Track display	TD 1 to 6

2.2.4 Read-Write Control Circuitry

The key Drum System circuits in any information exchange with the Central Computer are the read-write control circuits, shown on logic drawings 1.2.1 and 1–2.2.1. The Central Computer sends transfer control instructions into this circuit, where they are combined with drum-timing pulses and field-selection levels to produce drum-transfer-control levels. These levels activate the Drum System circuits which select the field registers to or from which information will be transferred, and also control the transfer.

2.2.5 Angular-Position-Counter Circuits

The angular-position-counter circuits, logic drawings 1.2.3 and 1–2.2.3, are used in conjunction with the aforementioned read-write control circuits to determine explicitly the field registers to or from which data is to be transferred. When the Central Computer designates, by number, the register or registers with which the data exchange is required, the angular position counter counts the drum registers passing under the read-write heads. When the number so counted compares with the Central Computer designation, the data transfer is performed. This method of register selection, known as address control, is used in CD writing and reading from the display fields, from the auxiliary memory fields, and from the intercommunication field.

2.2.6 Read-Write Circuitry

The read-write circuitry consists of two separate groups of circuitry: the read circuitry (shown on logic 1.2.2) and the write circuitry (logic 1.2.1). The write circuitry is capable of placing, at one instant of time, a complete information word (33 bits) on the drum surface. Only one write circuit is employed on the CD side of the drums. A separate write circuit for each of the input fields is employed on the OD side of the drums. The read circuitry is the means by which a complete information word (33 bits) is read at one instant of time from the drums. Only one read circuit is employed on the CD side of the drums. On the OD side of the drums, separate read circuits are employed for the OB fields cir-

cuitry and for the intercommunication field circuitry. Two read circuits are used in the display fields circuitry.

2.2.7 Input Fields Operate Circuitry

Four data types (LRI, MI, GFI, and XTL) comprise the input to the Combat Direction Central. Information is received by the input fields operate circuitry, logic drawings 1.3.1 through 1.3.6, at different rates and at random intervals. The input fields operate circuits store this data on the drums for later transfer to the Central Computer. The transfer from the Drum System to the Central Computer System is performed at Central Computer System command.

These circuits employ a method of register selection, the criterion for which is the full or empty status of the register. Under appropriate control conditions, information is automatically transferred into empty registers by the Input System and is removed from full registers. Upon removal, the data is sent to the Central Computer circuits. This method of transfer, known as status-controlled transfer, is used by all the input field operate circuits.

The input fields operate circuitry consists of six separate circuits. Each circuit handles a particular type of input data and is associated with one of the six input fields on the main drums. These fields, in summary, are: the MI, the GFI, LRI 1 and LRI 2, the XTL and SP XTL fields (table 1–1).

2.2.8 Output Buffer Fields Operate Circuitry

The Central Computer System develops large quantities of tactical data for transfer to the Output System. This transfer is performed by the OB fields operate circuitry, logic drawing 1.4.1, using the status transfer method outlined in 2.2.7. Since the operations of the Central Computer are considerably faster than the operation of the Output System, the transfer of tactical data is regulated by the OB fields operate circuitry to provide data for the Output System at a rate compatible with the Output System operations.

2.2.9 Display Fields Operate Circuitry

The display fields operate circuitry, logic drawings 1.5.2 and 1.5.3, takes display data that has been stored on the magnetic drums by the CD circuits and transfers it to the Display System. Like output data, display data is generated at speeds that are too great to be handled in the Display System. The Drum System, therefore, reduces the rate of transfer of display data to the Display System.

The display fields operate circuitry consists of three distinct circuits. The first of these circuits is used for reading digital display information from the drums and into the Display System. The second and third circuits are used for consecutively reading track display information and radar display information from the drums into the Display System.

2.2.10 Intercommunication Field Circuitry

The intercommunication field circuitry, logic drawing S–1.6.1, takes intercommunication data that has been stored on the magnetic drums by the CD circuits in the active Drum System and transfers it to the standby Central Computer System. This transfer takes place under the control of the standby Central Computer System. The intercommunication field thus provides a means of storing intercommunication data until needed by the standby Central Computer System.

2.2.11 Drum System Test Circuitry

Drum System test circuitry is of two types: loop test and manual test circuitry. The computers (loop) test circuitry (fig. 1–5, logic drawings 1.8.1 and 1.8.2) provides the Central Computer System with a means of performing tests on the Drum System to detect alteration of data. When the Drum System is in an operate mode, the Central Computer System exchanges information with the magnetic drums via the CD circuits only. However, when the Drum System is in a computer test mode, the computer test circuits provide the Central Computer System with access to OD circuits. The additional data paths made possible are shown by dashed lines on figure 1–5.

The manual test circuitry (fig. 1–5, logic drawing 1.7.2) enables maintenance personnel to exercise manual control over Drum System operations so that Drum System performance can be checked. The manual drum test circuitry has facilities for checking the storage operations of the magnetic drums and the control operations of the CD and OD circuits, as shown by the light lines of figure 1–5. In addition, the manual drum test circuitry contains manually operated controls that energize and de-energize the Drum System, and lamps that indicate the condition of Drum System circuits.

2.3 COMPOSITION AND PHYSICAL CHARACTERISTICS OF THE DRUM SYSTEM

Drum System operating circuits are contained in the three units shown in figure 1–1. These are unit 20, the auxiliary drum control and housing unit; unit 21, the main drum control unit; and unit 22, the main drum housing unit. These units are of modular construction; their dimensions are listed in table 1–2.

The back panels of units 20 and 21 contain test doors from which manual tests can be performed on the system. Each one of the six drum assemblies housed in units 20 and 22 is mounted on a hinged frame, which permits the drum to be swung out of the housing when checking or maintenance is required. Each module of the three units has a letter designation. The Z module of each unit monitors the power circuits which feed the circuits of that unit. Each module which contains control or transfer

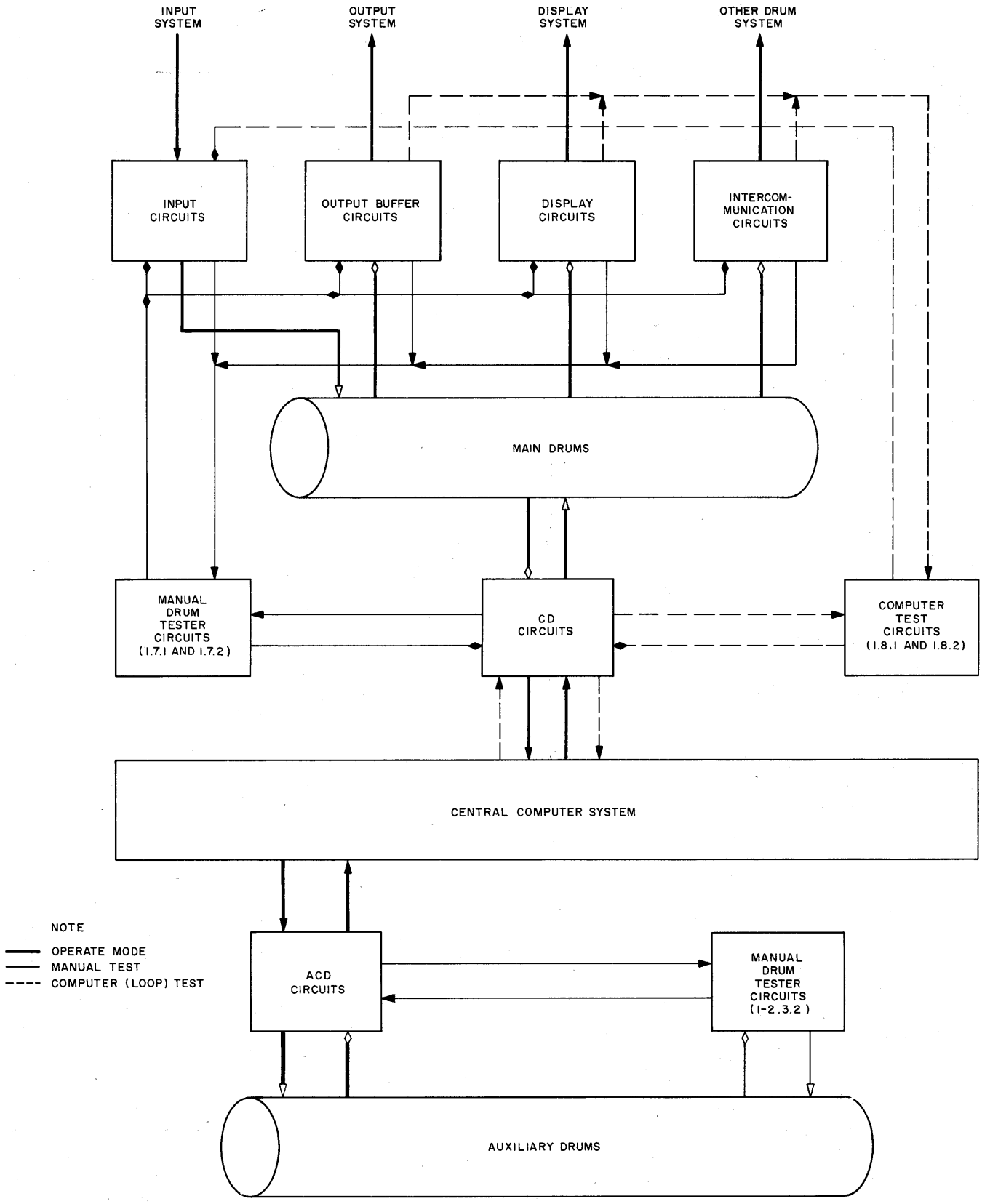


Figure 1–5. Drum System Test Operation, Block Diagram

TABLE 1–2. DRUM SYSTEM UNIT DIMENSIONS

DIMENSION	UNIT 20	UNIT 21	UNIT 22
Width	27 ft 1 in.	30 ft 11 in.	34 ft 2 in.
Depth	32 in.	32 in.	32 in.
Height	6 ft 8 in.	6 ft 8 in.	6 ft 8 in.
Weight (pounds)	10,165	9,755	12,488

circuitry consists of pluggable units which, like the modules, are designated by letter. The module designations run from left to right; the pluggable unit designations run from top to bottom.

These designations are used to advantage on the Drum System logics to locate the physical circuitry. A circuit with the designation 21 BE, for example, is located in pluggable unit E of module B in unit 21. All circuits in the Drum System logics are so designated, with the result that their locations are immediately known.

The six main drums of the Drum System are mounted in the drum housing of unit 22, the main drum housing unit. Six additional auxiliary drums are mounted in the drum housing of unit 20. Each of the drums rotates on a fixed shaft at high speed. As the drum rotates, fixed drum heads transfer information in binary form to and from the surface of the drum. Information is stored in the form of electromagnetic flux patterns which are retained without distortion unless deliberately removed or accidentally changed. The flux patterns will be retained even if the power is turned off. If the power fails or if the voltages are not sequenced off properly, however, it is possible that the flux patterns will be altered. Transfer of information from the magnetic drums does not disturb the flux patterns, which can be altered only by transferring new information into the same storage space occupied by the old information. Since transfer does not change the flux patterns, magnetic drum storage is described as nondestructive.

A detailed description of the magnetic drum assembly is given in Chapter 2 of Part 4; paragraph 2.2 includes a discussion of the arrangement of the read-write heads about the surface of the drum.

PART 2
DETAILED THEORY OF OPERATION OF THE MAIN DRUMS

CHAPTER 1
INTRODUCTION

The main drums function as the connecting link and time buffer for information exchanges between the Central Computer System and the Input, Output, and Display Systems.

This Part describes how the transfer of data is accomplished between the Central Computer System and the Input, Output, and Display Systems via the main drum fields and the associated CD and OD circuits. The theory of operation of the main drum fields and circuits is presented in a sequence which conforms to the normal flow of data through the Drum System. For example, in a description of the transfer of data originating at the Central Computer System, the CD circuits involved in field selection and drum writing are presented first. The OD circuits concerned with field selection and reading are next discussed. When the transfer of data originating at the Input System is described, the sequence of presentation is reversed.

The drum fields and the associated CD and OD circuits used in the transfer of different types of data (input, output buffer, display, and intercommunication) are discussed in separate chapters. Timing generation and distribution, being similar for all drums, is incorporated in one chapter. The CD field selection is also similar for all the drum fields; therefore, it, too, is discussed in detail in a single chapter. All CD data transfers are controlled through a single CD read-write control circuit. A single read circuit is employed for all CD read transfers, and a single write circuit for all CD write transfers. For this reason, the operation of the CD read-write control circuits and the read-write circuits are also described in one chapter (Ch 4, CD Data Transfer Control). Any modifications of CD field selection and CD data transfer processes which occur in the data transfer circuits of a given field are discussed in the chapter devoted to that field.

The following chapters contain the information outlined below:

Chapter 2 (Timing Generation and Distribution) discusses the function and formation of the drum timing and index pulses, and their distribution.

Chapter 3 (CD Field Selection) explains the function of field selection, and describes the field selection and switching circuits of the system.

Chapter 4 (CD Data Transfer Control) discusses the function and source of the signals which control CD writing and reading. Descriptions of the flow path of CD data, and the circuitry required for CD writing and reading, are included.

Chapters 5, 6, 7, and 8 describe the transfer of input fields data, output buffer fields data, display fields data, and intercommunication fields data. Descriptions of the respective fields and associated circuits are presented. Chapter 7 also includes a detailed description of the precession process utilized in the OD reading of the display fields.

Chapter 9 (Main Drum Testing) describes the manual tests and checks that can be performed on the functions of the Drum System. The test circuits utilized for the performance of these tests are discussed. Included in this chapter are descriptions of the manually initiated timing-rewrite, and erase controls, and of the drum-motor-control circuits.

CHAPTER 2
TIMING GENERATION AND DISTRIBUTION

The drum timing system times the operation of all systems except the Central Computer System. There is no fixed time relationship between individual drums, since each drum is rotated by a separate motor. It is necessary, therefore, that each drum generates the timing pulses that time and control its own operations and the operations of the systems (excepting the Central Computer System) with which it is directly associated.

The timing pulses are used to initiate the control operations which prepare Drum System circuits to write or read; they are also used to trigger reading and writing operations and to step the various counters used in the Drum System circuitry.

2.1 TIMING PULSE GENERATION

Drum circuit timing pulses are obtained from a timing channel recorded on each drum. Timing channels on all drums contain a closed series of sine waves. During the operation of each drum, each sine wave cycle is read from the timing channel and is converted to four standard pulses, 2.5 usec apart. These four pulses, known as drum timing pulses (DTP 1, 2, 3, and 4) constitute one 10-usec operational period of the drum. The DTP 1 and DTP 3 pulses are produced directly from the timing channel; their repetition rate is a direct function of drum speed. The DTP 2 and DTP 4 pulses are produced by delaying DTP 1 and DTP 3 pulses for 2.5 usec. Drum timing pulses which time Drum System operations during information exchanges with the Central Computer System are designated as CD 1, 2, 3, and 4. Drum timing pulses which time Drum System operations involved in other information exchanges, and which time the operations of other systems, are designated as OD 1, 2, 3, and 4.

Drum timing pulses are formed from the closed sine wave series recorded on each drum. In a closed series, there is no method of distinguishing between any two sine wave cycles. It is, therefore, necessary to arbitrarily select one cycle to represent the beginning or ending of a drum revolution. This selection is performed by recording an additional channel, known as an index channel, on each drum. Each index channel contains a single 1 bit which establishes a zero reference point in drum rotations. The remainder of the index channel contains 0 bits.

The single 1 bit in the index channel is used to represent the beginning of a drum revolution during information exchanges between the Drum System and the Central Computer System. During information exchanges between the Drum System and all other systems, the single 1 bit indicates the end of a drum revolution. Drum timing and index channels are written at the same time; the writing operation will be performed whenever the drum has been erased.

2.1.1 Writing of Timing and Index Channels

The timing and index channels are written before Drum System operations are begun or following maintenance procedures in which timing and index channels are erased. A block diagram for the writing of a timing and index channel on any one of the drums is shown in figure 2–1. A timing disc is mounted on one end of each drum. This timing disc is opaque except for a small optical track near the outer edge. The disc is mounted so that the optical track varies the intensity of a beam of light from an exciter lamp falling on a photoelectric cell. As the drum rotates, the optical track varies the amount of light passing through it at a sinusoidal rate. The photoelectric cell converts this varying light to sine waves of electrical energy. For all drums (except the

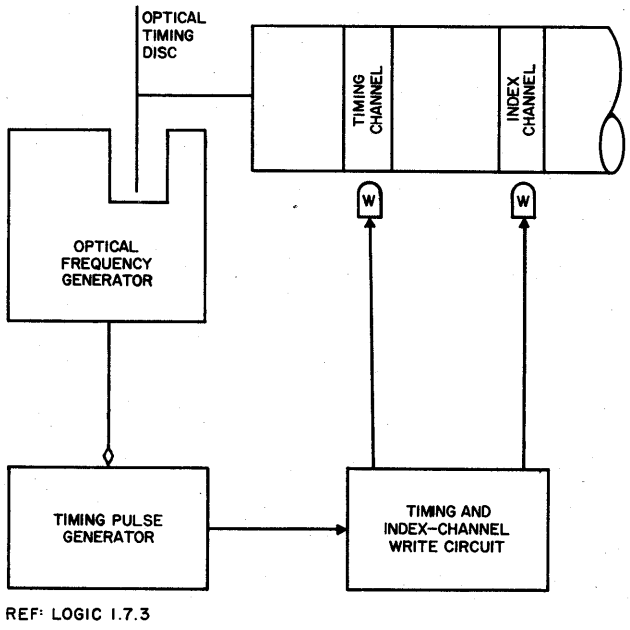


Figure 2–1. Writing of Timing and Index Channels, Block Diagram

RD and TD drums), a closed series of 2,048 sine waves is recorded for one complete revolution of the drum. (A closed series of 2,060 sine waves is recorded on the RD and TD drums for one complete revolution.) At normal drum speed (2,914 revolutions per minute), the frequency of the sine waves is approximately 100 kc per second. These sine waves are read from the optical frequency generator and are applied to a timing pulse generator, which converts each input sine wave cycle to two successive standard timing pulses. These pulses (fig. 2–2) are called TP 1 and TP 3. The 1 timing pulses are formed at each negative-going zero crossing of the input sine wave. The 3 timing pulses are formed at each positive-going zero crossing of the input sine wave. At normal drum rotation, there are 5 usec between zero-crossing points. This interval is, therefore, present between a TP 1 and a TP 3 of the same cycle.

These timing pulses are applied to a timing-and-index-channels-write circuit. This circuit writes a 1 bit in the timing channel and a 0 bit in the index channel on receipt of each TP 3. Thus, for all drums except the RD and TD drums, 2,048 evenly spaced 1 bits are recorded in the timing channel. For the RD and TD drums, 2,060 evenly spaced 1 bits are entered in the timing channel. When timing channel writing is completed, the next TP 3 that is produced records a single 1 bit in the index channel. Timing and index channel writing is then stopped. The circuits used to write the timing and index channels of the main drums are part of the erase-and-timing-write circuits of the Drum System. These circuits are described in Chapter 9 and are shown on logic 1.7.3.

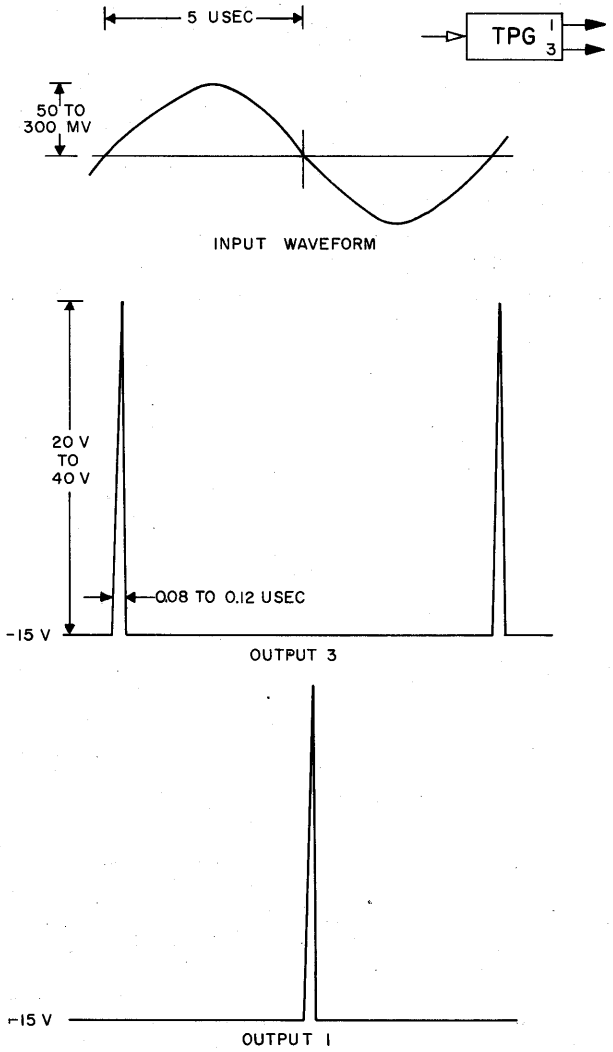


Figure 2–2. Output of Timing Pulse Generator

2.1.2 Reading of Timing and Index Channels

The timing and index channels of each drum are read continuously during operation of the Drum System. (See fig. 2–3.) The flux pattern on the timing channel of a drum causes a series of sine waves to be induced in the timing channel read head. (These sine waves are similar to the sine waves developed by the optical frequency generator.) The induced sine waves are applied to a timing pulse generator, which converts them to two of the four fundamental timing pulses used to time the circuits of the drum. These pulses are called drum timing pulses (DTP's) 1 and 3.

The DTP 1 pulses are formed at each negative-going zero crossing of the input sine wave; the DTP 3 pulses are formed at each positive-going zero crossing of the input sine wave. At normal drum rotation speeds, there are 5 usec between zero-crossing points (fig. 2–2). The same interval is, therefore, present between DTP 1 and DTP 3 pulses.

In each drum timing circuit the DTP 1's are sent to a 2.5-usec delay line. The output of this delay line is called a DTP 2 pulse. The DTP 3 pulses are also sent to a 2.5-usec delay line, the output of which is termed a DTP 4 pulse. The DTP pulses 1 through 4 comprise the fundamental timing pulses of each drum. The 2.5-usec interval between each pulse results in a pulse cycle of 10 usec. This corresponds to the time required for one register on the drum surface to pass a read or write head during normal rotation of the drum.

Drum timing pulses which time drum operations during information exchanges between the Drum System and the Central Computer System are designated as CD 1, CD 2, CD 3, and CD 4. Drum timing pulses which time drum operations during information exchanges with systems other than the Central Computer System are designated OD 1, OD 2, OD 3, and OD 4.

Within the Drum System, CD 1 and OD 1 pulses are used for reading, and CD 3 and OD 3 pulses are used for writing. The CD 2, CD 4, and the OD 2, OD 4 pulses are used for control operations which prepare the Drum System circuits to read or write.

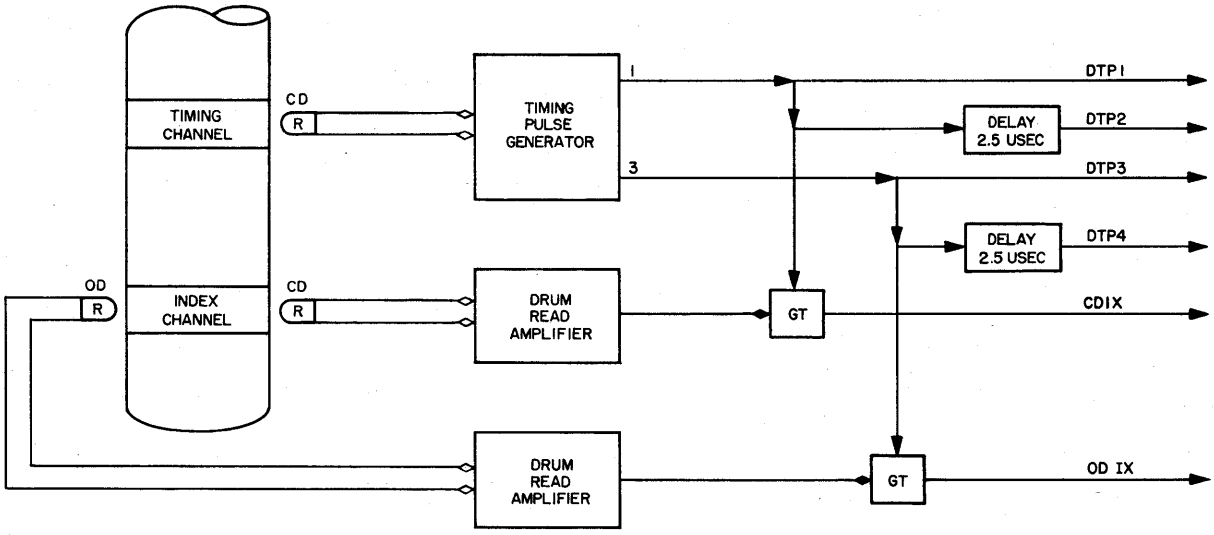


Figure 2–3. Timing Channel and Index Channel Read Circuit, Simplified Logic Diagram

The index channel is read by two index channel drum read heads, the CD index head and the OD index head (except in the AM drum, where there is only a CD index head).

The CD index read head sends the sine wave produced by the index bit to the index channel drum read amplifier. The drum read amplifier conditions a gate to pass the DTP 1 pulse occurring at that time. This gated DTP 1 pulse is called the CD-index pulse. The OD head sends its sine wave to another drum read amplifier, which conditions another gate to pass a DTP 3 pulse. This DTP 3 pulse is called the OD-index pulse. The CD-index pulse coincides with a DTP 1 timing pulse, and the OD-index pulse coincides with a DTP 3 timing pulse.

The CD-index pulse is a reference point that indicates the beginning of a drum revolution during information transfers between the Drum System and the Central Computer System (i.e., the CD-index pulse will be associated with the first of the 2,048 registers).

The OD-index pulse represents the end of a drum revolution during information exchanges between the Drum System and the Input, Output, or Display Systems (i.e., the OD-index pulse will be associated with the last of the 2,048 registers).

2.1.3 RD and TD Drum Timing Pulses

The timing circuits of the TD and RD drums are modified slightly so as to delay the application of OD and CD pulses to the TD and RD circuitry. A delay of 120 usec is required to allow time for switching transients, developed during RD and TD field switching operations, to subside. The modification is accomplished as follows.

The timing disc on the TD and RD drums is constructed to cause the writing of 2,060 timing cycles in the TD and RD timing channels, instead of the 2,048 timing cycles found on all other drums. The DTP 1 and DTP 3 pulses derived from these channels are fed into gap counters which cause the first 12 cycles during each revolution of the drums to be skipped. The counters prevent the DTP 1 pulses and DTP 3 pulses of the first 12 cycles of each revolution from being sent to the read and write circuits of the TD and RD drums, thereby delaying the RD and TD operations for 12 cycles (120 usec).

In the case of the RD and TD drums, a distinction is made between the DTP pulses and the equivalent OD or CD pulses. The DTP can be taken from any point on the 2,060-cycle timing channel; OD and CD signals are taken only from the 2,048 cycles that are present after 12 cycles are skipped. The OD and CD pulses represent the output of the gap counters. With 120 usec skipped at the beginning of each revolution, no register on any of the TD or RD fields is read before the required switching time has elapsed.

2.1.3.1 TD Timing Circuit, Circuit Analysis

The optical timing disc, employed in the writing of the timing channel of the radar data and track display drums, contains 2,060 sinusoidal cycles. The timing pulse generator in the timing channel read circuit for these drums (fig. 2–4) alternately generates two timing pulses, DTP 1 and DTP 3, for each sine wave cycle detected by the timing channel read head. Both timing pulses are delayed 2.5 usec to produce DTP 2 and DTP 4.

The DTP 1 and DTP 3 pulses are passed by the output of the TD CD gap counter, to produce the TD

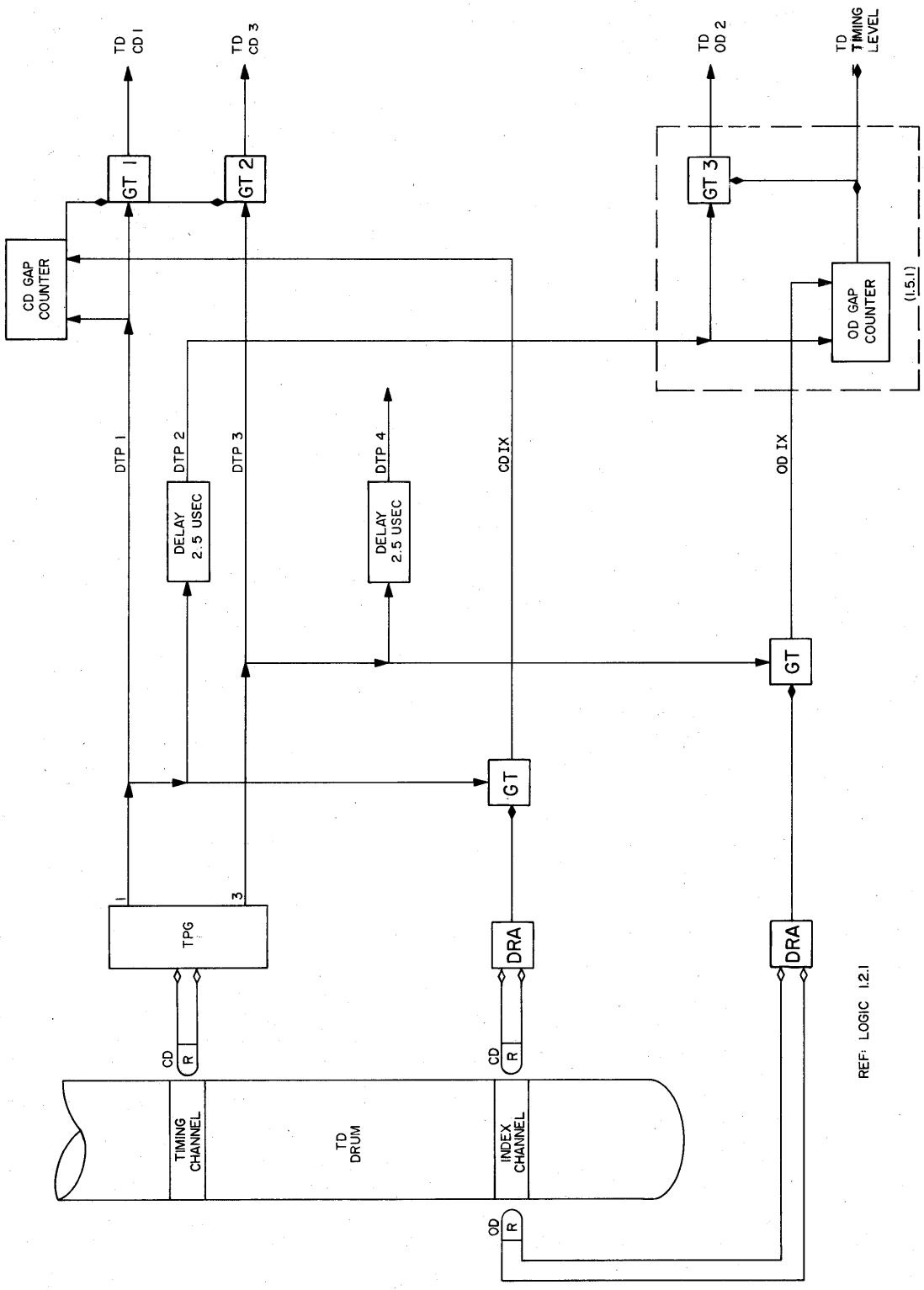


Figure 2–4. Track Display Timing Circuit, Simplified Logic Diagram

CD 1 and TD CD 3 pulses used by the TD angular position counter. The DTP 2 pulse is passed by the TD OD gap counter to produce the TD OD 2 pulse and a TD timing level. The TD OD 2 pulse is used to step the TD register counter; the TD timing level is a necessary condition for the operation of the TD OD read circuits.

The TD CD gap counter is shown in figure 2–5. The counter is initially cleared by the index pulse. With flip-flops 3 and 4 at 0, OR circuit 1 conducts. The output of OR circuit 1 conditions gate 1 to pass DTP 1's to the counter. The 0 outputs of flip-flop 3, flip-flop 4, or both flip-flops maintain conduction in OR circuit 1 until 12 DTP 1's have been counted. At this time flip-flops 3 and 4 are both in the 1 state and OR circuit 1 conduction stops. With OR circuit 1 output level removed from gate 1, counting stops until the next index pulse clears the counter and resumes conduction in the OR circuit. In the period before the index pulse arrives (from the 13th to the 2,060th DTP 1 pulse), flip-flops 3 and 4 are in the 1-state; and AND circuit 1 conducts, producing an output level. The level at the output of gap counter 1 passes the 13th through the 2,060th DTP 1 and DTP 3 pulses at gates 1 and 2 of figure 2–4, respectively.

The TD OD gap counter uses the OD index pulse to clear its flip-flops and uses DTP 2 pulses for counting. In all other respects, the TD OD gap counter is identical with the TD CD gap counter. The output level of the TD OD gap counter passes the 13th through 2,060th DTP 2 pulses at gate 3 (fig. 2–4). In addition, the output level is used as a necessary condition for TD reading.

By skipping the first 12 pulses after every index, the track-display-timing-circuit-and-gap counter produces a 120-usec period during which OD timing pulses are not available for reading, writing, or register counting purposes. At the end of the delay, however, 2,048 timing cycles remain during which the drum can read and write the usual number of drum registers.

2.1.3.2 RD Timing Circuit, Circuit Analysis

The radar drum (RD) timing circuits are shown in figure 2–6. The generation of the DTP and CD pulses for the radar field circuits is identical to the generation described in 2.1.3.1 above for the corresponding pulses of the track drum. The RD CD gap counter is identical with the TD OD gap counter. The RD OD gap counter is identical to the TD OD gap counter. The level generated by this counter conditions gates 3, 4, and 5 to pass the 13th through 2,060th DTP 1, 2, and 4 pulses respectively; thereby producing the RD OD 1, the RD OD 2, and the RD OD 4 pulses used for RD OD reading, writing, or counting purposes.

2.1.4 Formation of Special Purpose Timing Pulses and Levels

The application of drum timing pulses to key points in the transfer control circuits of the Drum System is dependent on the drum involved in the transfer. This dependence is effected by feeding the required timing pulse into gates. In order to conduct, the gates must be conditioned by a select drum level. The select drum level is present whenever a field is selected by the Central Computer for an information exchange. The array of gates and the subsequent OR's into which the timing pulses are fed is called the timing pulse distributor. The output of each gate is called a selected-drum-timing pulse. The timing pulse distributor poduces a selected-CD-index and CD 3 pulse for each drum; in addition,

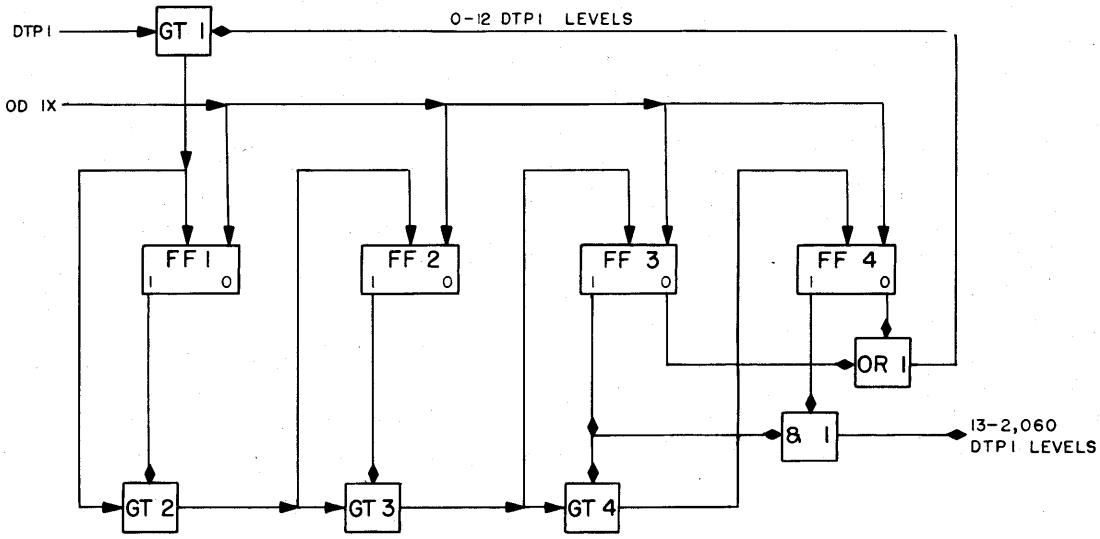


Figure 2–5. TD CD Gap Counter, Simplified Logic Diagram

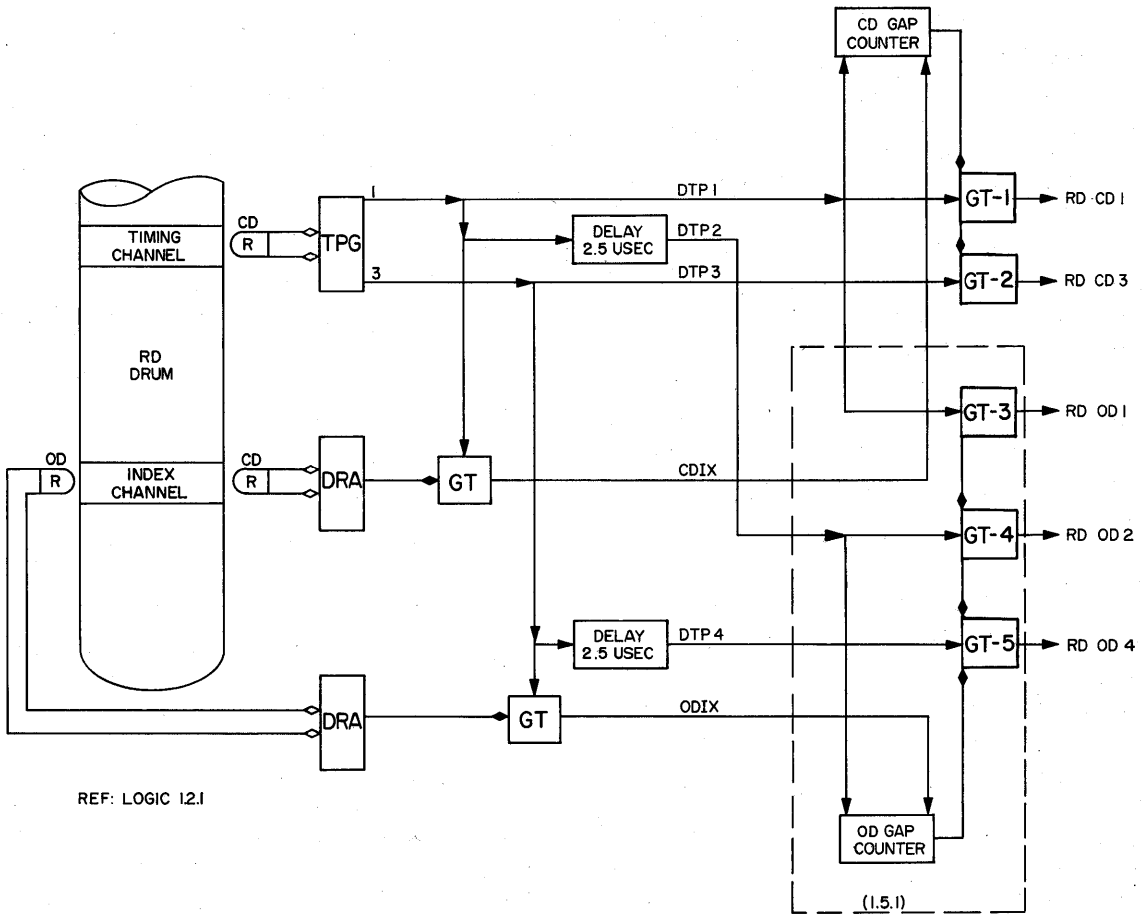


Figure 2–6. Radar Display Timing Circuit, Simplified Logic Diagram

it produces a selected CD 1 pulse for each drum, excepting the LOG drum. The derivation of the select AM-A CD 1, CD 3, and index pulses is shown on figure 2–7.

In addition to the select drum classification of timing pulses, there is a select CD classification. The select CD 4 pulses, the select CD 3 pulses, the select CD 1 pulses, and the address select CD 1 pulses are included in the select CD classification.

The select CD 3 pulses are derived from an OR (OR 1, fig. 2–7) whose inputs include five of the six select drum CD 3 lines. (The select LOG CD 3 is not used here.)

The select CD 4 pulses are derived from an OR (OR 2, fig. 2–7) whose three inputs consist of a select CD 3 line in which a 2.5-usec delay has been inserted, a LOG CD 4 line, and a select MIXD CD 4 line. Availability to the OR of LOG CD 4 pulses is dependent on the presence of a select-field level corresponding to one of the fields on the LOG drum.

The address select CD 1 pulses are derived from an OR (OR 3, fig. 2–7) whose five inputs consist of five of the six select drum CD 1 lines (from those drums which have fields read or written by address). (The select LOG CD 1 is not used here.)

The select CD 1 pulses are derived from an OR (OR 4, fig. 2–7) whose inputs include an address select CD 1 line and a LOG CD 1 line. Availability of LOG CD 1 pulses is dependent on a select OB field level, which is generated upon the selection of the OB fields for an information transfer.

The drum timing circuitry also produces LOG OD 3 + 1.7-usec pulses and MIXD OD 3 + 1.7-usec pulses. These pulses are obtained by inserting a 1.7-usec delay in one of the LOG OD 3 lines and in one of the MIXD lines. The pulses are used to deactivate the drum write drivers in the MI, GFI, LRI, and XTL circuits.

2.2 TIMING DISTRIBUTION

Within the Drum System the drum CD 1 and OD 1 pulses have their primary application in the read circuits, where they are gated to act as read sample pulses. The drum CD 3 and OD 3 pulses have their primary application in the write circuits, where they initiate the write-on-drums operation. The drum CD 3 pulses are also used to step APC's associated with each drum. The

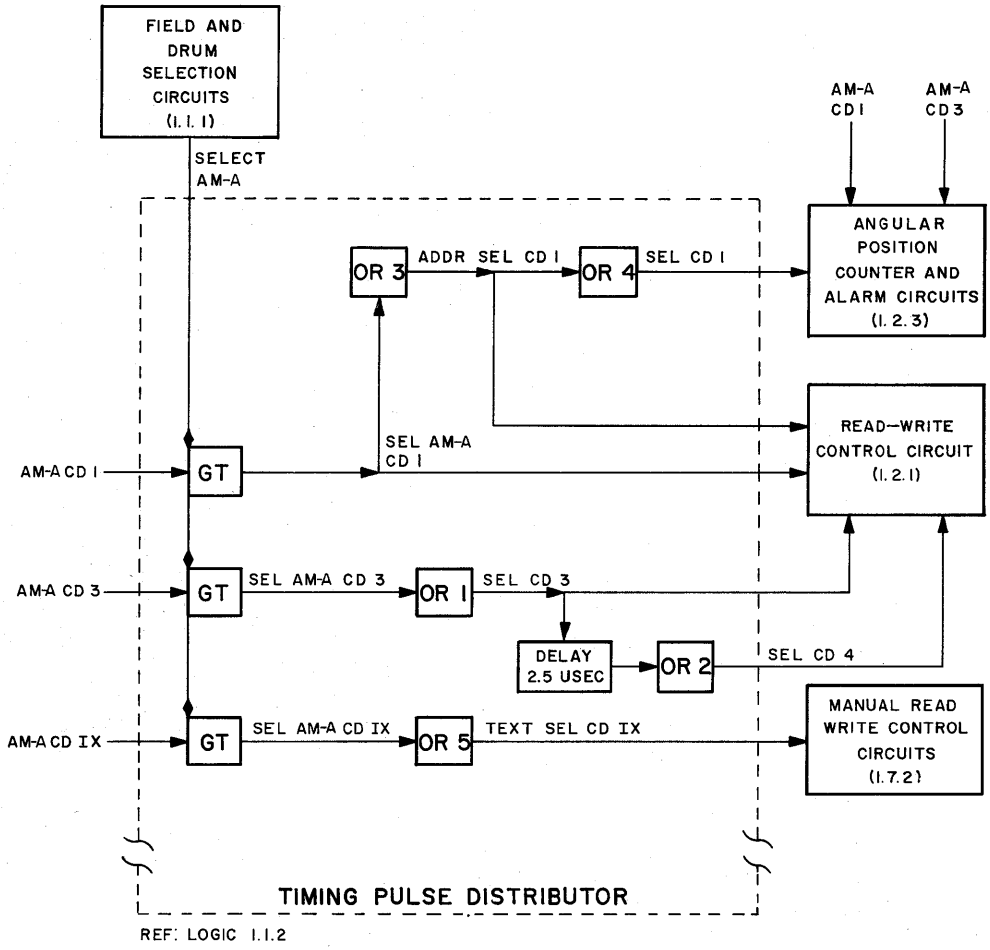


Figure 2–7. Development of Select AMA-Timing Pulses

drum CD 2, CD 4, OD 2, and OD 4 pulses are used for subsidiary control and short time (10 usec or less) reset functions throughout the System. The various counters employed in the Drum System are stepped by one of the timing pulses; the timing pulse used is dependent on the purpose of the counter. The drum-index pulses (both OD and CD) have their primary application in the various counter and synchronizing circuits, where they perform the resetting function required at the completion of one or more drum revolutions. The OD-index pulse is also used as an extra counting pulse during the precessed reading of the display fields.

The following paragraphs consider the distribution of the pulses associated with each drum.

2.2.1 LOG Drum, Pulse Distribution

The LOG timing pulses time the operation of the CD and OD circuits of six fields; the GFI field, the two LRI fields, and the three OB fields. The LOG-OD pulses are also sent to the Input and Output Systems to synchronize the Output System operations with the operations of the circuits of the Drum System. The overall distribution of the LOG timing pulses is shown in figure 2–8. An important phase of the LOG timing distribution is accomplished in the timing pulse distributor circuit, which channels selected timing pulses to the CD read-write control circuits and test circuits. The operation of the timing pulse distributor with reference to the LOG drum timing pulses is shown in figure 2–9.

2.2.2 MIXD Drum, Pulse Distribution

The distribution of the MIXD-drum timing pulses is shown in figure 2–10. These pulses time the operation of the CD and OD circuits of four fields: the MI field, the digital display field, the XTL field, and the IC field. The MIXD OD pulses are also sent to the Display System, the Input System, and the CD circuits of the standby computer drums. The timing pulses are used in these equipments to synchronize information exchanges with the Drum System. The production of select-CD pulses by the timing pulse distributor, using the basic pulses of the MIXD timing circuits, is shown in figure 2–11. The select-CD pulses which are developed control reading and writing on the MIXD drum fields.

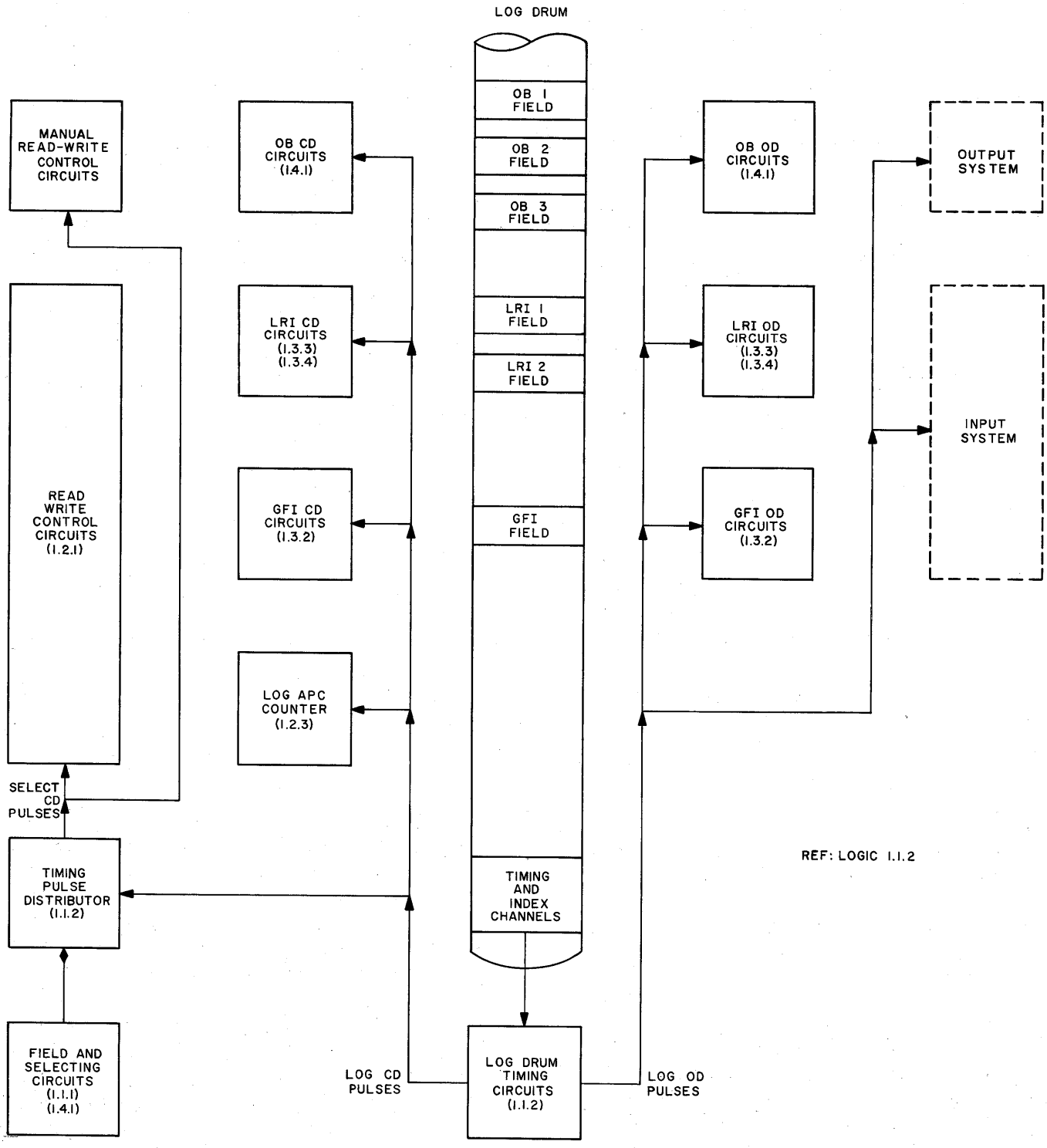


Figure 2–8. LOG Timing Pulse Distribution, Block Diagram

2.2.3 TD Drum, Pulse Distribution

The TD drum timing pulses time information exchanges with the six fields of the TD drum. The TD CD 1, 3, and index pulses are sent to the timing pulse distributor, where the select CD pulses required by the CD-read-write-control circuits are developed. The circuit used in the timing pulse distributor for obtaining the CD select pulses from the basic TD CD pulses is identical to the circuit shown in figure 2–7, except for the basic pulses and levels employed; in the case of TD

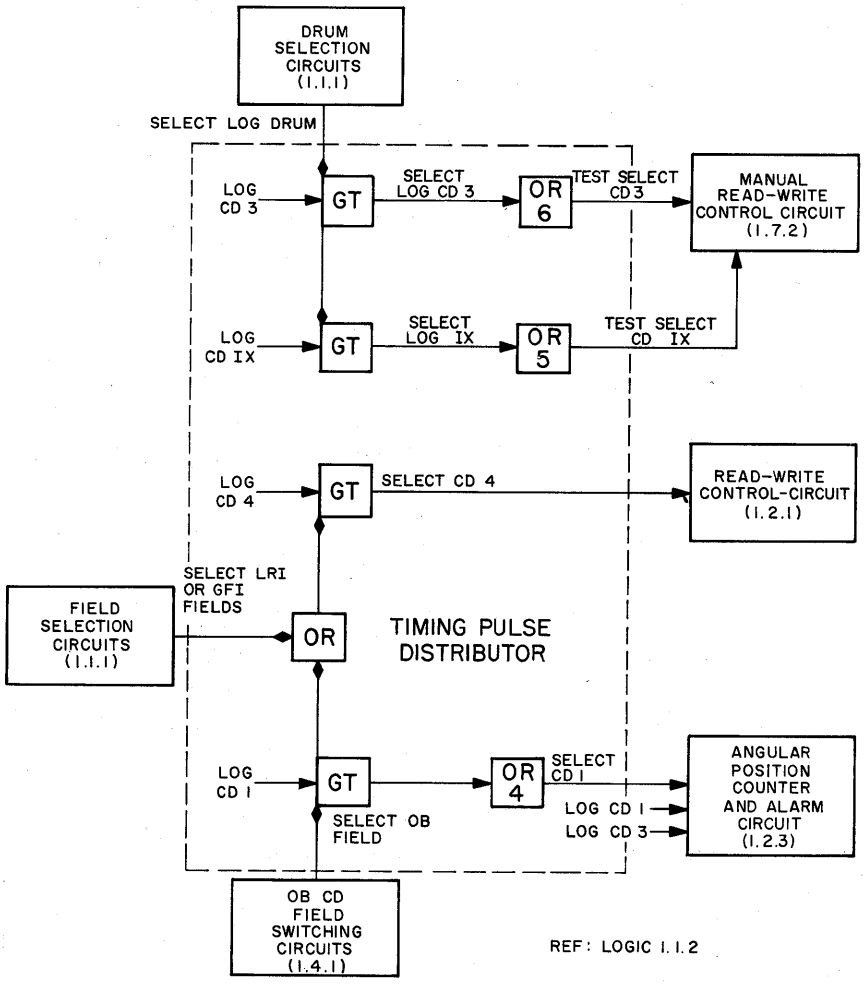


Figure 2–9. Development of Select-LOG-Timing Pulses

timing, the gates of the distributor are conditioned by a select TD level from the field and drum selection circuits. The TD CD 1, CD 2, and CD IX pulses are also sent to the CD-angular-position-counter-and-alarm circuits. The TD-OD pulses time the OD circuits of the TD fields. In addition, the TD-OD-index pulse and TD DTP's 1, 2, 3, and 4 are sent to the situation display circuits of the Display System to synchronize the operation of those circuits with the operation of the TD OD circuits.

2.2.4 RD Drum, Pulse Distribution

The RD drum timing pulses time information exchanges with the nine fields of the RD drum. The distribution of these pulses is identical to that described in 2.2.3 for the TD timing pulses.

2.2.5 AM-A and AM-B Drum, Pulse Distribution

The AM-A and AM-B drums exchange information with the Central Computer System only. For this reason, the AM-A and AM-B timing circuits produce CD pulses but no OD pulses. These pulses are sent to the timing pulse distributor (fig. 2–7) and the CD angular-position-counter-and-alarm circuits. In the timing pulse distributor, the AM-A (or AM-B) CD pulses become the select-CD pulses required to control reading or writing on the AM-A (or AM-B) drum fields. Only CD 1, 3, and index pulses are used. CD 2 and 4 pulses are produced by the timing channels but are not applied to the CD circuitry.

2.2.6 Special Purpose, Pulse Distribution

The distribution of the select-drum-timing pulses, the select-CD-timing pulses, and the address-select-timing pulses is shown in figures 2–9 and 2–11.

The LOG OD 3 + 1.7-usec pulses are sent to the OD write circuits of the GFI, LRI 1, and LRI 2 fields, where they deactivate the drum write drivers of these fields after each word transfer. The MIXD OD 3 + 1.7-usec pulses are sent to the OD write circuits of the MI, XTL, and SP XTL fields, where they deactivate the drum write drivers of these fields after each word transfer. In the case of the OD status channels of the above

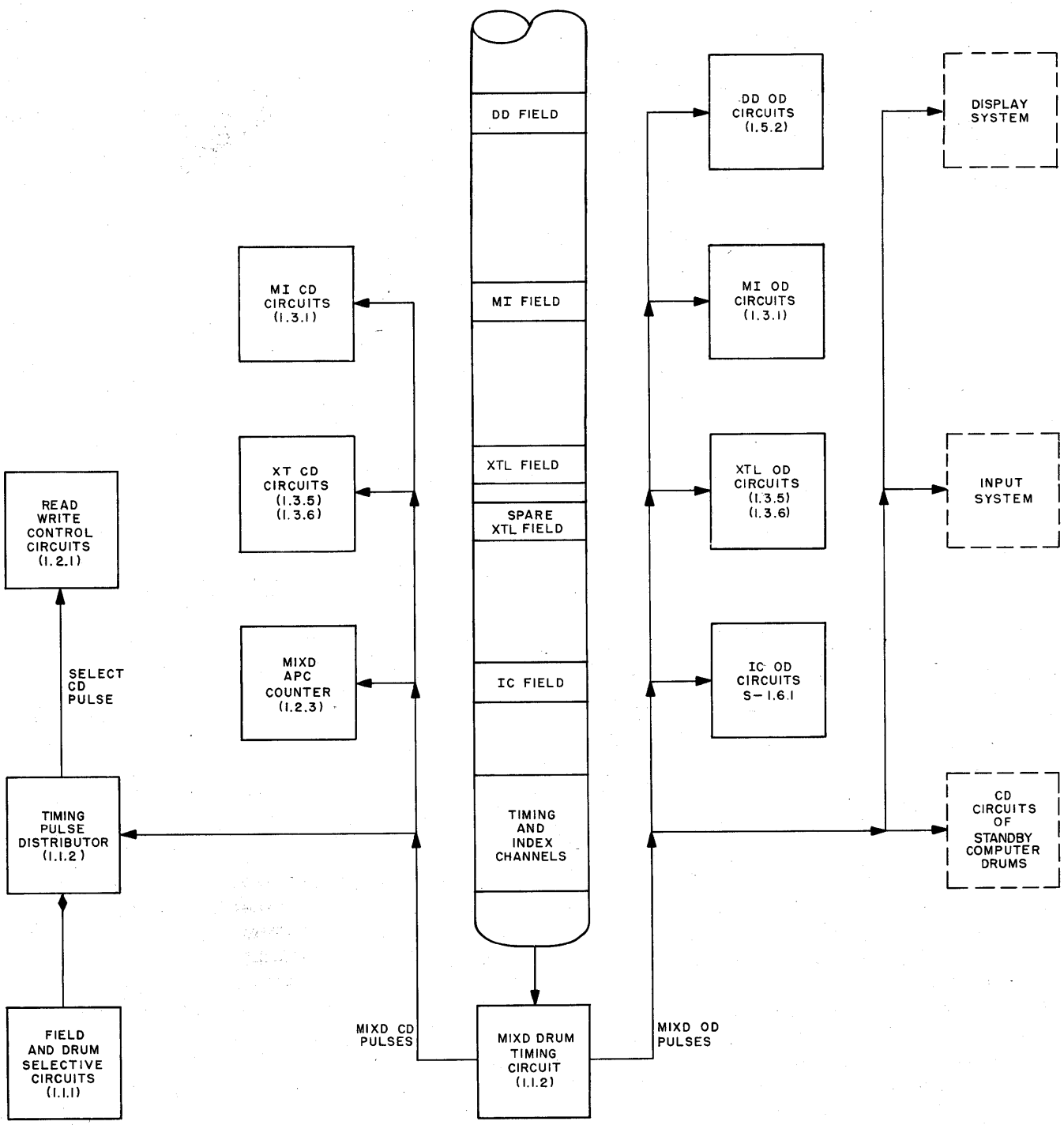


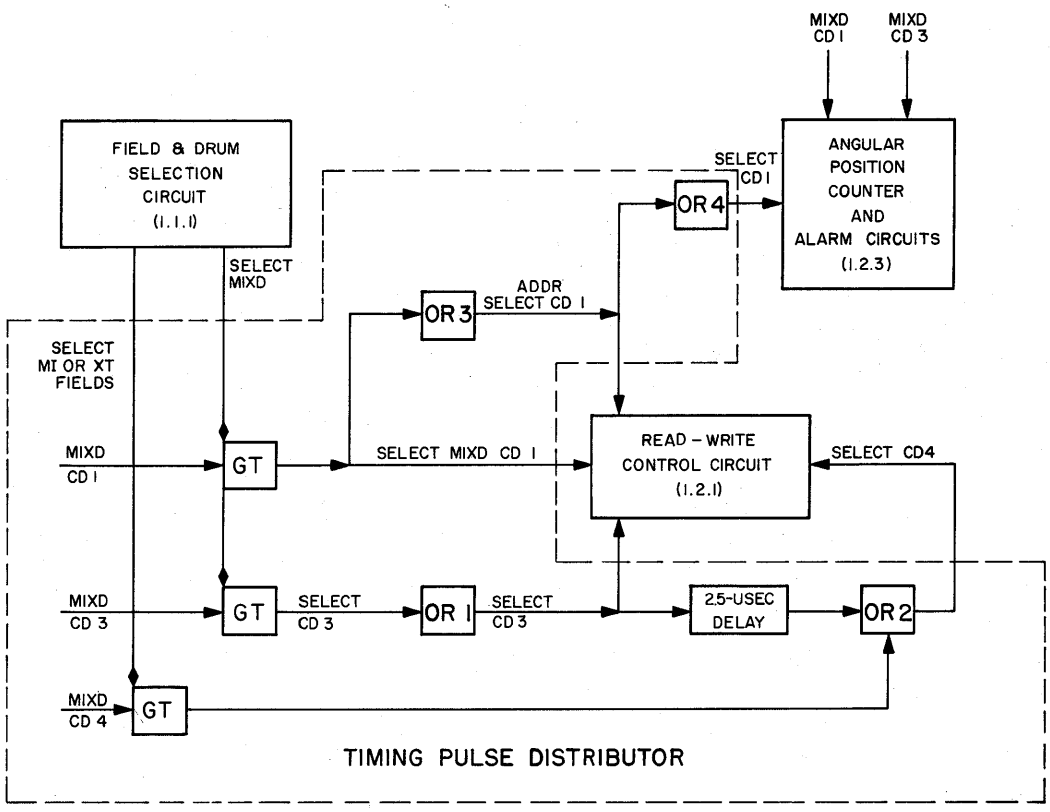
Figure 2–10. MIXD Timing Pulse Distribution, Block Diagram

fields, the deactivation of the drum write driver occurs after the writing of each bit.

2.3 MAIN DRUM SYSTEM AND OTHER SYSTEMS OF AN/FSQ-7, TIMING RELATIONSHIPS

An important function of the Drum System is to serve as a time buffer between the Central Computer System and the Input-Output Systems of the AN/FSQ-7. The Central Computer makes information available at a relatively high rate of speed. The Drum System organizes and slows the rate of data transfer so that information can be applied to the Display and Output Systems at speeds compatible with their operations.

Tactical information from the Input System, which is applied to the Drum System for transfer to the Central Computer, occurs at random times. The Drum System will store this information until it is requested and accepted by the Central Computer. In such cases, the



rigure 2–11. Development of Select-MIXD-Timing Pulses

Central Computer System will transfer information from the Drum System to its own circuits at the maximum rate of which the Drum System is capable.

2.3.1 Drum System and Central Computer System, Timing Relationship

The Central Computer System is a faster operating system than the Drum System. It employs a 6-usec timing cycle consisting of 12 timing pulses, as distinguished from the 10-usec timing cycle of the Drum System. Data transfers occur at the maximum speed permitted by the drum timing. Any individual word is transferred within the 10-usec period of the drum timing cycle. The Central Computer interrupts its other operations to receive or transmit a word whenever the Drum System is ready to transmit or to receive the word.

2.3.2 Input System and Drum System, Timing Relationships

The rate of data flow in Drum System operation is considerably faster than the rate of data flow through the Input System. This permits the skipping of those registers of the input fields which contain unused information, and the placement of input information on the first empty registers, without impeding the flow of data through the Input System. The flow of information between the two Systems is synchronized by Drum System timing pulses, which are sent to the Input System for that purpose.

2.3.3 Output System and Drum System, Timing Relationships

The rate at which data can be transferred by the Drum System is approximately twice as great as the permissible rate of data flow through the Output System. Because of this rate, the Central Computer writes consecutive words of OB information on alternate registers of the OB fields. Only the information on the odd (or even) registers, as selected, is accepted by the Output System. The flow of information between the two Systems is synchronized by Drum System timing pulses, which are sent to the Output System for that purpose.

2.3.4 Display System and Drum System, Timing Relationships

Although the Drum System can transfer successive digital display words with a repetition rate of 6 usec, the operation of the digital display subsystem requires a minimum time interval of 620 usec between word transfers. The situation display subsystem requires a 50- to 60-usec interval between RD transfers, and a 960- to 1.040-usec interval between TD data transfers. The necessary time delay between successive words is affected by employing separate precessed reading patterns for each of the above fields.

Digital display information is interleaved by the program element at the Central Computer System before being written on the CD side of the Drum System.

Therefore, successive words of a message are not written in successive drum registers. During OD reading, the message is transferred in the proper sequence by having the read circuits alternately skip and then read in a pattern that results in 640-usec intervals between the readings of consecutive message words. This pattern makes it necessary for the drum to turn through 64 revolutions before the entire digital display field is read. At the end of each revolution, the reading pattern is stepped one number ahead of its normal count to insure that all registers are read.

During OD reading of situation display data, the OD display element alternately skips and reads in patterns that produce the desired interval between readings. The patterns make it necessary for the TD drum to turn through 13 revolutions for each field to be read; the RD drum must turn through six revolutions for each field to be read. Whenever necessary, the reading pattern being employed is precessed (stepped one slot ahead of its normal count) to insure that all registers are read.

The flow of information between the Drum System and the Display System is synchronized by Drum System timing pulses, which are sent to the Display System for that purpose.

2.4 DRUM TIMING ERASURE

During normal operation of the Drum System, information written on the drums is not affected by reading operations. The magnetic flux patterns on the drums, which represent binary data, are normally changed only by being written over or by accidental introduction of spurious fields. But in certain cases, such as the period following maintenance or during installation, it is desirable to clear all information from the drum surface. This is accomplished via an erasing operation performed by manually controlled circuits of the Drum System.

When a drum is erased, its surface is cleared of all magnetic flux patterns, including any random fields that might have been established by noise in the drum writing heads. The entire information surface of the drum is, therefore, returned to an unbiased or demagnetized condition. The timing and index channels are automatically rewritten after each erasure operation. The erase and timing write circuitry is described in Chapter 9.

CHAPTER 3
CD FIELD AND DRUM SELECTION

Exchanges of information between the Central Computer System and the Drum System (CD exchanges) are initiated by programmed instructions from the Central Computer. One part of these instructions designates the drum fields with which the Central Computer desires to exchange information. The field designation, in the form of parallel pulses, activates the Drum System field selection circuitry. The Drum System selection circuitry performs two operations required in an information transfer between the Drum System and the Central Computer System. These operations are selecting the designated drum field and selecting the drum in which the field is located.

The purpose of the first operation is to activate the drum field with which the information exchange is to take place and to condition the control circuits directly associated with the designated field. The drum selection operation is required in order that the designated field circuits may be correctly timed. Each drum has only one timing channel which is utilized by all the fields on that drum. The designated field could not be correctly timed using the timing channel of another drum due to the asynchronous operation of the drums.

Field and drum selection circuits are shown on logic drawings 1.1.1 and 1.1.1-2. The function and detailed operation of the CD field selection circuits are described in 3.1 through 3.3.

3.1 FIELD DESIGNATION

Field selection instructions from the Central Computer are transferred to the Drum System by index-interval pulses which represent the six bits, L10 through L15, of a programmed instruction word. These bits are called index interval bits and contain the field designation octally encoded in two groups of three bits each. The octal code for each field is shown in figure 2–12.

Three of these Central Computer System instruction word bits represent the 10's-column digit. The other three represent the units-column digit. For example, if the sixth field of the AM-A drum is selected by the Central Computer System, the instruction word bits are 000111, in that order, representing code number 07_8. If the GFI field is chosen, the instruction word bits are 011011, in the same order, representing code number 33_8. In the same manner, any one of the 50 fields and conditions listed in the octal field code chart of figure 2–12 can be selected.

3.2 FIELD SELECTION

The index interval bits designate a field selected by the Central Computer System. The function of the field selection circuitry is to activate the designated field and the control circuits which are used only with that field.

Some fields may be selected by more than one code. For instance code 23_8 selects the MI field. (See fig. 2–12.) Code 22_8 selects the same field, but in this case additional control circuits are activated so that the operation of the field may be tested.

Selection is accomplished by means of decoding circuits and diode switching circuits.

The decoding circuits transform the positive levels representing the two groups of three binary instruction bits into positive levels representing an equivalent octal number. The levels are applied to the read-write heads of the field designated by the octal code, and through the read-write heads to the diode-switching circuits. The diode-switching circuits are the means by which the designated field is connected to the drum writers and the read switch. In order for information to be read from, or written on, a designated drum field, the diode switch associated with that field must be conditioned by the field-selection level.

3.2.1 Field Selection Decoding Circuits

The decoding circuits used for CD field and drum selection are shown in simplified form in figure 2–13. Field selection is initiated by a deselect pulse from the Central Computer which clears the six selection register flip-flops. The 1 bits of bits L10 through L15 of the Central Computer instruction word are then transmitted to the selection register, causing the associated flip-flops to be set. The pulses used to set the register flip-flop are known as index-interval pulses.

The d-c levels from the register flip-flops are sent to the 10's and units decoders respectively. Each decoder consists of eight AND circuits. Each AND represents a numeral from 0 through 7. The AND's are arranged so that, for any particular combination of index-interval pulses, only one AND in each decoder will conduct.

The output of the units decoder combines with the output of the 10's decoder in the appropriate AND of the field selection decoder (fig. 2–14) to produce an output called a select-field level. This output, a +10-volt d-c level, is connected directly to the drum field driver of the selected field.

TENS	UNITS 0	1	2	3	4	5	6	7
0			AUXILIARY MEMORY–A 1	AUXILIARY MEMORY–A 2	AUXILIARY MEMORY–A 3	AUXILIARY MEMORY–A 4	AUXILIARY MEMORY–A 5	AUXILIARY MEMORY–A 6
1	AUXILIARY MEMORY–B 7	AUXLIARY MEMORY–B 8	AUXILIARY MEMORY–B 9	AUXILIARY MEMORY–B 10	AUXILIARY MEMORY–B 11	AUXILIARY MEMORY–B 12	INTERCOM-MUNICATION OTHER	DIGITAL DISPLAY TEST IDENTIFICATION
2	SPARE 1 XT	SPARE 2 (AUXILIARY MEMORY)	MANUAL INPUT STATUS (TEST)	MANUAL INPUT IDENTIFICATION	CROSSTELLING STATUS (TEST)	CROSSTELLING IDENTIFICATION	INTERCOM–MUNICATION OWN	DIGITAL DISPLAY
3	OUTPUT BUFFER ODD STATUS	OUTPUT BUFFER EVEN STATUS	GFI STATUS (TEST)	GFI IDENTIFICATION	LRI-1 STATUS (TEST)	LRI-1 BITS 12–15 IDENTIFICATION	LRI-2 STATUS (TEST)	LRI-2 BITS 12–15 IDENTIFICATION
4	CROSSTELLING MARKER	TRACK DISPLAY 1	TRACK DISPLAY 2	TRACK DISPLAY 3	TRACK DISPLAY 4	TRACK DISPLAY 5	TRACK DISPLAY 6	SITUATION DISPLAY TEST IDENTIFICATION
5	LRI-1 IDENTIFICATION BITS 7–15	LRI-2 IDENTIFICATION BITS 7–15						
6	RADAR DATA 1	RADAR DATA 2	RADAR DATA 3	RADAR DATA 4	RADAR DATA 5	RADAR DATA 6	RADAR DATA 7	RADAR DATA 8
7	RADAR DATA 9						IC (OWN TEST)	

NOTE: ALL FIELDS NOT INDICATED OTHERWISE READ TO OR WRITE FROM THE CENTRAL COMPUTER SYSTEM BY ADDRESS

Figure 2–12. Octal Code for Field Selection

The output of the units and 10's decoders are also combined in a separate decoder which provides conditioning levels for the transfer controls of the MI, GFI, XTL, and LRI fields, and test levels for all but the OB fields. The operation and design of this decoder is identical to that of the field selection decoder.

Individual OB fields are not selected by the Central Computer System. Selection by the Central Computer of either the odd or even registers of the OB fields is the only choice available. The Central Computer System thus sees the three OB fields as one continuous field. These fields are switched consecutively by means of OB field-switching circuits which are described in Chapter 6.

As a result, an octal code designation is required only for the even and odd register selection. The positive OB-even and OB-odd levels represent the encoded selection by the Central Computer of the OB-even or the OB-odd registers of the OB fields. The drum field drivers for these fields receive their inputs from the OB circuits described in Chapter 6.

3.2.2 Drum Field Driver Array

When a drum field driver receives a +10-volt input from the field selection decoder, it amplifies this input to a +125-volt output level. This output conditions the drum heads of the selected field for reading or writing and also furnishes plate voltage for the writing circuits. When a drum field driver is not selected, it receives a −30-volt input from the field selection decoder. This results in a +70-volt nonselect-field-output level from the drum field driver. The amplitude of the nonselect-field level is insufficient to permit the drum heads in that field to either read or write. The outputs of the drum field drivers are applied directly to the center taps of the read-write heads of the drum fields. The circuits are completed through a diode-switching arrangement which enables the selected heads to read or write but blocks conduction in nonselected heads. The diode-switching arrangement is discussed in the following subsection.

3.2.3 Diode-Switching

The diode-switching circuits consist of groups of semiconductor diodes. These diodes conduct when their anodes are maintained at a higher potential than their cathodes and block conduction when the opposite situation prevails. A simple diode array is shown in the upper portion of figure 2–15. The potential at the

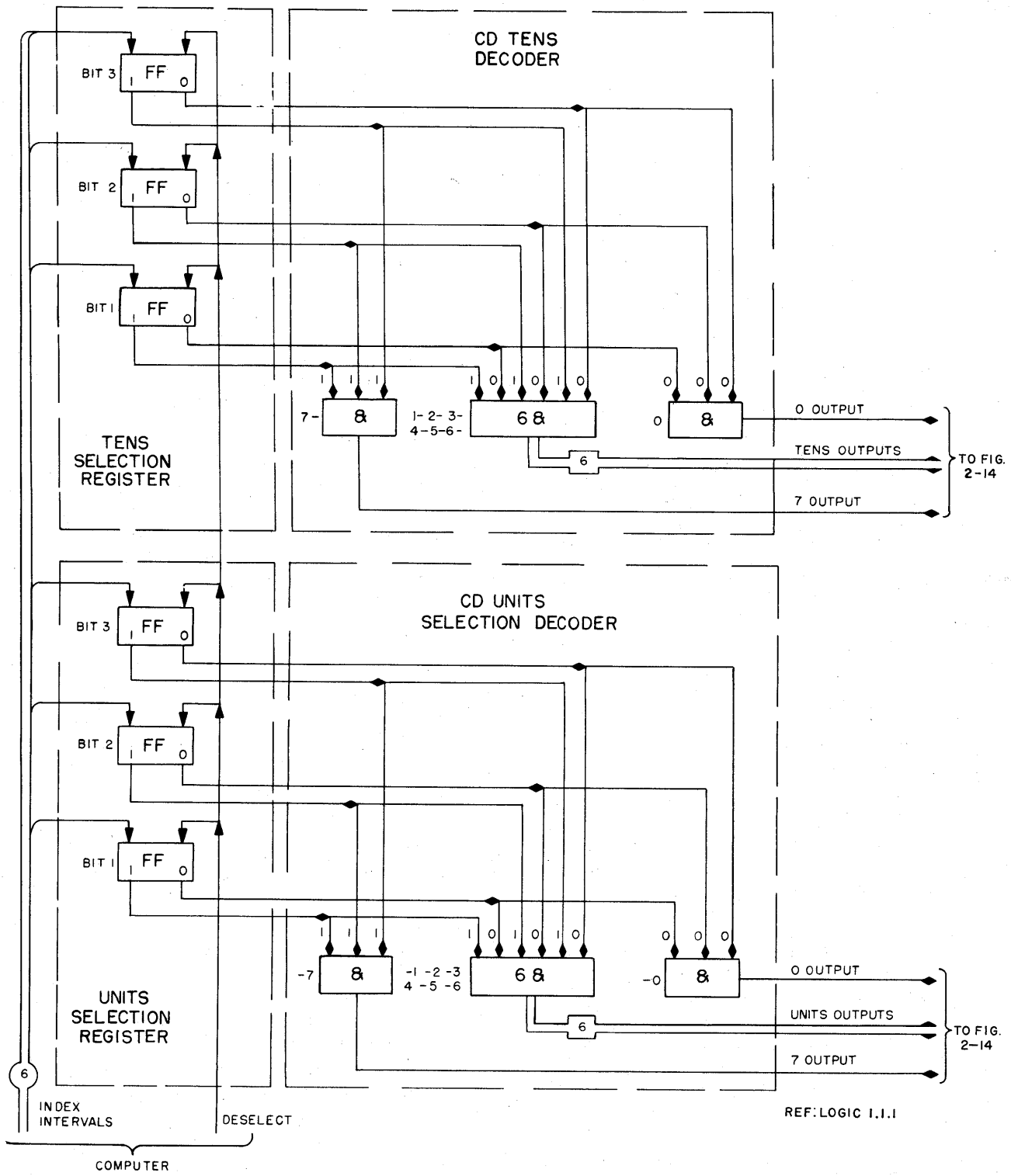


Figure 2–13. Selection Registers and Decoders, Simplified Logic Diagram

output of this array will correspond closely with the highest input potential. If a source of current is applied to the output terminal, current will flow through that diode on which the highest input voltage is maintained and will be blocked in the remaining diodes. In this manner any one of several circuit paths may be selected for current conduction. In the simple array of figure 2–15, path 2 was selected by placing +125 volts at the path 2 input, and +70 volts at the inputs of the remaining paths.

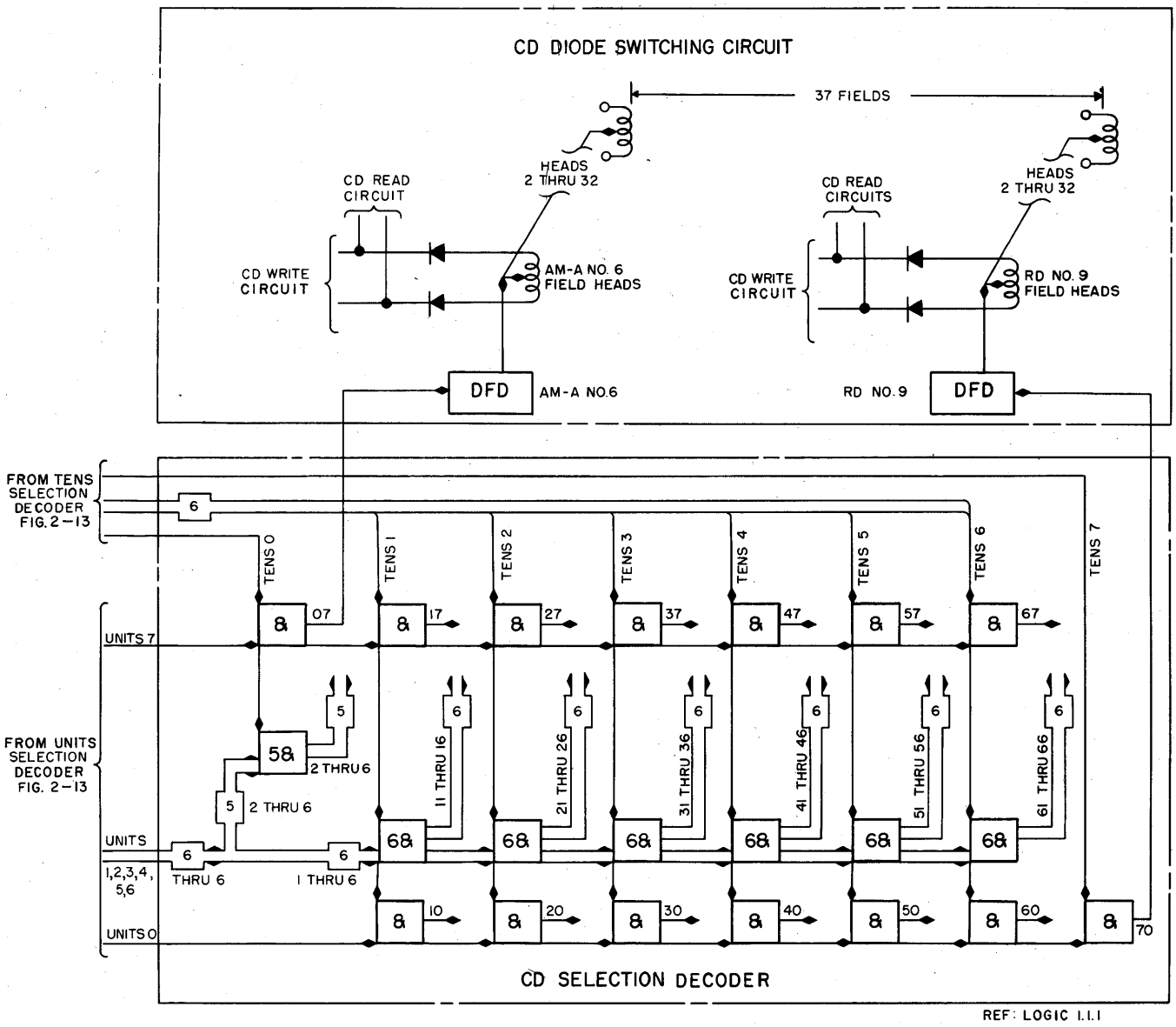


Figure 2–14. Field Selection Decoder Circuits, Simplified Logic Diagram

The number of diodes (and, therefore, the number of selections) cannot be increased indefinitely using a simple array because the back resistance of the nonconducting diodes will, when a sufficient number are paralleled, introduce a significant current loss. This drawback is circumvented by employing a cascaded array of diodes (fig. 2–15). The circuit operation of step 2 of the cascade is identical to the operation in step 1 with the result that the highest voltage applied to an input of step 1 will be mirrored at the output of step 2. In the example shown, any one of 11 paths could have been selected for conduction. Path 2 was selected for purposes of illustration.

The Drum System employs 33 cascaded diode arrays to provide the current paths required between the CD read-write circuits of the System and the CD read-write heads associated with the drum fields. Each of the 33 diode arrays is associated with one of the 33 bits of an information word and is fed into the part of the read-write circuitry which effects the writing (or reading) of the bit. The diode array which connects the left sign (LS) bit read-write heads to the LS drum writer (and read switch) is shown on figure 2–16. The remaining 32 arrays corresponding to bits L1 to R15 and the parity bit are substantially identical with the LS array. The only exceptions exist in the arrays for bits L11 to L13, R11 to R14, and the parity bit. In these arrays the RD field switch is replaced by an RD dummy load switch into which the select field lines are led. This arrangement stems from the fact that the RD informa-

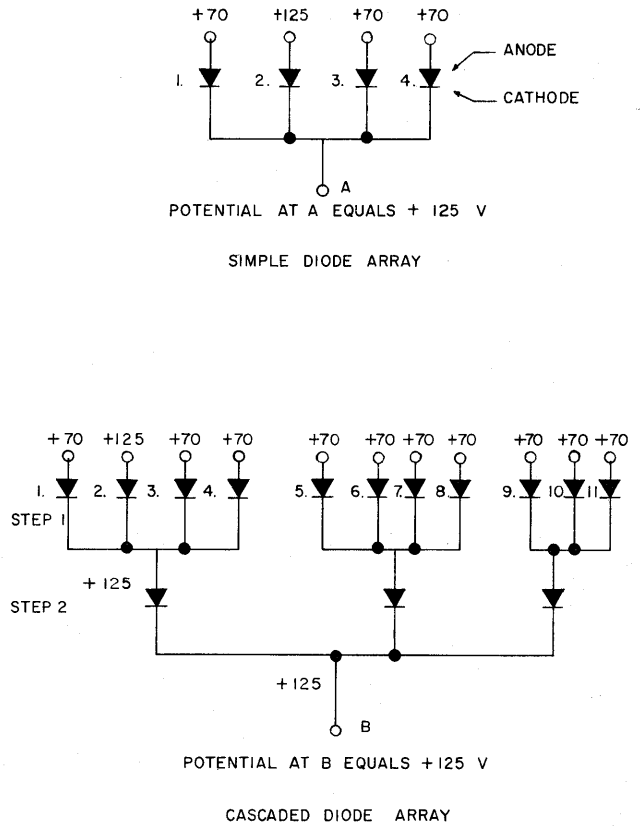


Figure 2–15. Diode Arrays Simplified Schematic Diagram

tion word lacks the above bits and, therefore, lacks the corresponding read-write heads on the RD drum. The dummy load is used in order that the load on the read-write circuits will be the same during the writing of RD information as it is during the writing of other information. The dummy load switch is a model D diode switch whose nine inputs are connected to the nine select field lines for the RD drum and whose output is fed into the CD drum switch.

The 33 diode arrays used in the CD circuits of the Drum System are substantially identical. For this reason, the operation of one array only (the LS array) will be described. (See fig. 2–16.)

Prior to field selection the select field lines from the 39 drum field drivers apply +70 volts to the read-write heads of their associated fields. As a result, each LS head (as well as the remaining CD information heads) will have 70 volts present at its center tap. This 70 volts is applied through the field switches and drum switch to the read-write circuitry. This voltage is insufficient, however, to condition the operation of the read-write circuitry.

When a field is selected, the output of the drum field driver for that field rises to +125 volts (3.2.2). This voltage is applied to the read-write heads of the selected field. The +70 volts remains at the heads of all other fields. If it is assumed that the AM-A1 field was selected, the LS head of that field will be at +125 volts and all other LS heads will remain at +70 volts. Due to the action of the diode array, the +125 volts will be applied to the read-write circuitry. This voltage conditions the operation of the read-write circuitry and effectively blocks conduction in all diodes of the array whose anodes are held at +70 volts. Therefore, signals can pass only between the read-write circuits and the selected field. The diode switching arrays are shown in detail on logic drawings 1.1.1 and 1.1.1-2. The blocks used in these drawings correspond to the diode switch models A, B, and C, illustrated and discussed in Part 4, Chapter 9.

3.3 DRUM SELECTION

Within the Drum System itself, there is no fixed time relationship between individual drums since each drum is rotated by a separate motor. Therefore, each drum generates the timing pulses which time and control its own operations and the operations of the system (or systems) with which it may be connected. It is necessary, therefore, for the Drum System to select the timing circuitry of the particular drum which contains the field designated by the Central Computer System.

When a particular field is designated by the index-interval pulses, the drum selection circuits produce a level which conditions gates in the CD timing pulse distributor. This section will treat the generation of the select-drum level. Drum timing and associated circuitry were discussed in Chapter 2.

The drum-selection-decoder uses the outputs of the units selection register and the 10's-selection register to select the drum containing the field designated by the Central Computer System.

For example, if AND 6, in the drum selection decoder (fig. 2–17) conducts, it indicates that one of the fields of the TD drum has been selected by the Central Computer System. The resulting d-c level is called a select-TD level. Figure 2–12 shows that the TD fields are designated by code numbers 41 through 46. Therefore, one requirement for conduction in AND 6 is the presence of the 4 output of the 10's selection decoder, and the other requirement is an output from OR 2. OR 2 conducts only when the units-selection-register outputs represent numbers between 1 and 6.

The presence of the 1 or 6 levels produces an output from OR 5 which is sent to OR 2. Similarly, if a 2 or 3 units selection is made, the resulting 1-state level from the bit 2 flip-flop and the 0-state level from the bit 3 flip-flop in the units selection register combine in AND 1. This sends a level to OR 2. In a like manner, a units selection of 4 or 5 produces a 0-state level in the bit 2 flip-flop and a 1-state level in the bit 3 flip-flop

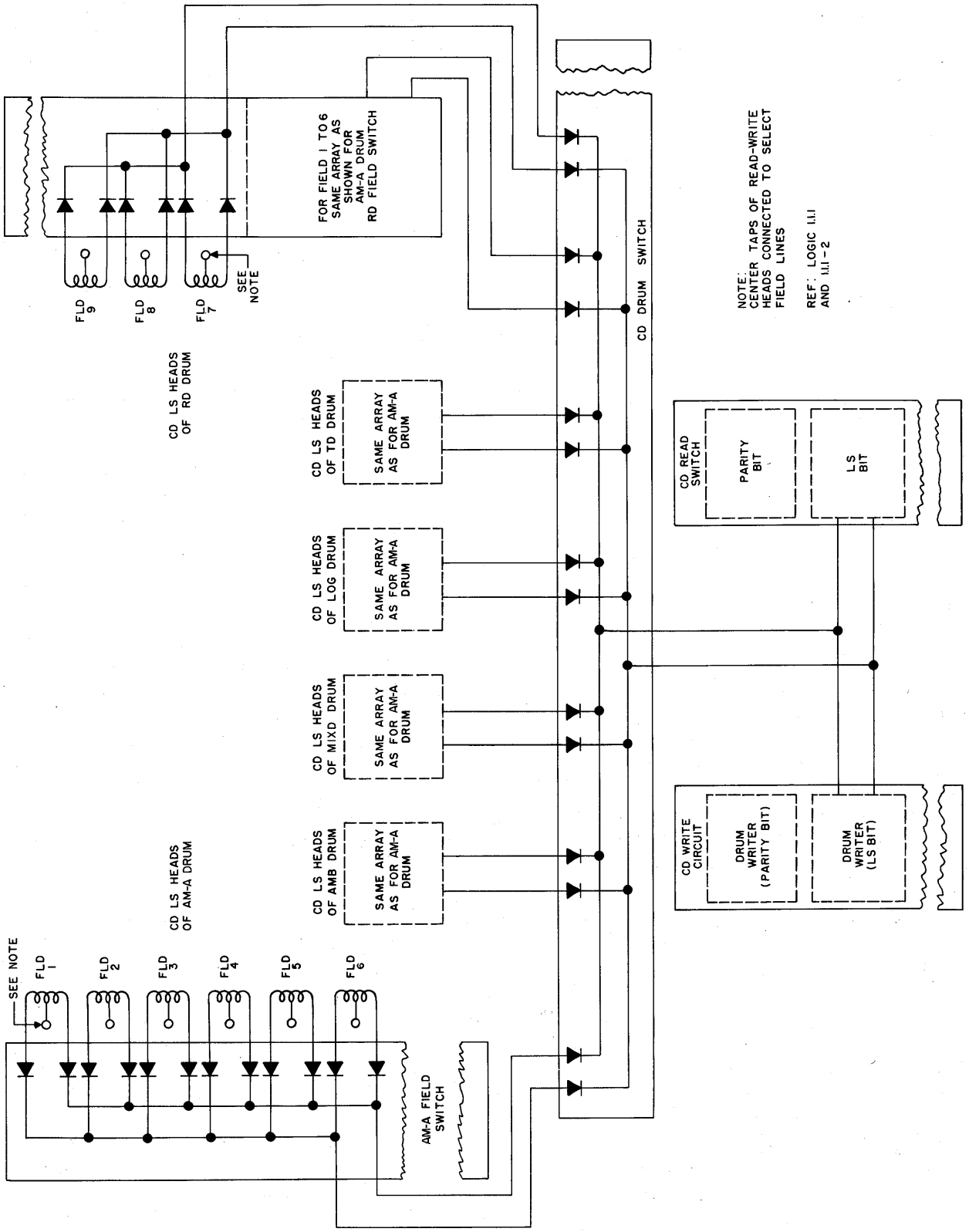


Figure 2–16. Diode Switches For CD LS Heads, Simplified Schematic Diagram

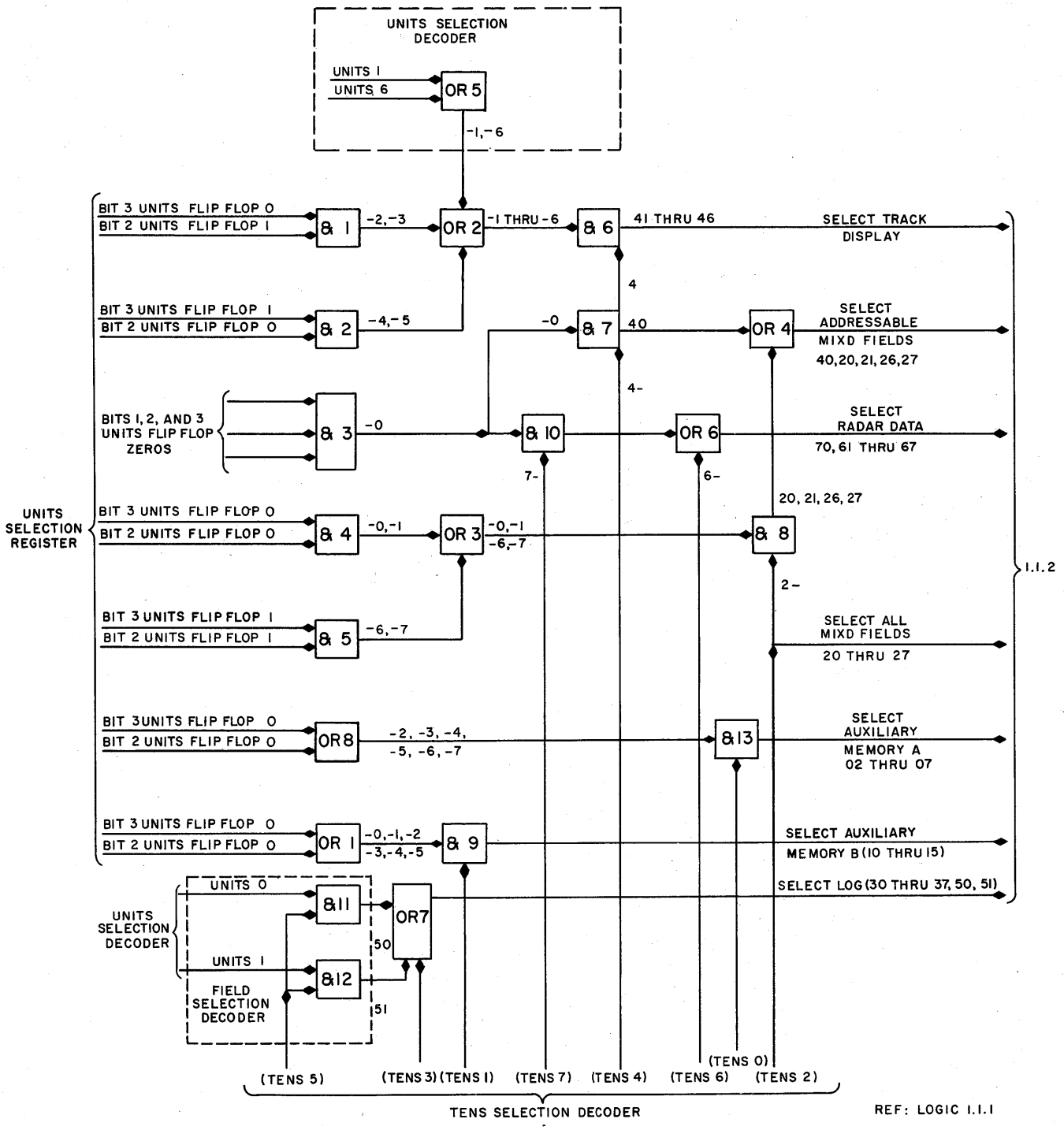


Figure 2–17. Drum Selection Decoder, Simplified Logic Diagram

of the units selection register. These last two levels combine in AND 2 to send a level to OR 2. Thus, OR 2 sends an output to AND 6 whenever a units selection from 1 to 6, inclusive, is made. The units-selection levels combine in AND 6 with the 4 level from the 10's-decoder to produce an output from AND 6 when a code number from 41 to 46, inclusive, is selected.

Other drum selections are made in the same manner. The code numbers for the fields on the LOG drum are 30 through 37, 50 and 51. The 3 output of the 10's selection decoder is sufficient to produce the 30 through 37 d-c level. Long-range radar 1 and 2 identification fields have code numbers 50 and 51, respectively. The level for code 50 is produced by combining in AND 11

(fig. 2–17) the units 0 level from the units selection decoder and the 10's-5 level from the 10's selection decoder. The units-1 level and 10's-5 level are similarly combined in AND 12 to produce the level for code 51. The outputs of AND 11 and AND 12 together with the 10's-3 level are led into OR 7 whose output then represents the select-LOG level. The output of OR 8 and the 0 output of the 10's selection decoder are combined in AND 13 to produce the select-AM-A-drum level.

The RD drum has octal designations 60 through 67 and 70. To produce the select-RD level, the 0-state levels of all three units-selection register flip-flops are combined with the 7 output of the 10's selection decoder to represent 70. The 6 output of the 10's selection decoder represents all octal code numbers in the 60's.

The 0-state level from the bit 2 flip-flop or the bit 3 flip-flop of the units selection register is sent to OR 1, which sends an output to AND 9 for units selection 0 through 5. When the 1 output of the 10's selection decoder is combined with the output from OR 1 in AND 9, the output of AND 9 is the select-AM-B level.

For the MIXD drum, units-selection-register outputs for 0, 1, 6, and 7 are combined in AND 8 with the 2 output of the 10's selection decoder. Thus, OR 4 receives a d-c level from AND 8 for octal code selections 20, 21, 26, and 27. A signal representing octal code selection 40 is sent from AND 7 to activate OR 4. Therefore, outputs (called select-MIXD-drum) are obtained from OR 4 for octal code selections 20, 21, 26, 27, and 40. The MIXD drum selection is made only for addressable fields of this drum. Selection of the XTL, MI, or SP XTL field produces an additional level called the select-XTL, -MI, or -SP-XTL level. This performs a function similar to that of the drum-selection level.

The select-drum levels are the outputs of the drum selection decoder and are sent to the CD timing pulse distributor. Only one drum can be selected at a time because the selection levels are ultimately dependent upon the octal code number represented by programmed index-interval bits from the Central Computer System.

CHAPTER 4

COMPUTER-DRUM DATA TRANSFERS

4.1 GENERAL

The Drum System of the Combat Direction Central AN/FSQ-7 equipment is the data transfer link between the Central Computer System and the Input, Output, and Display Systems. The Drum System stores input data temporarily until it is needed by the Central Computer; it stores output and display data from the Central Computer until it can be used by the Output and Display Systems; it stores intercommunication data awaiting transfer to the standby Drum System. The drums also provide the Central Computer with auxiliary memory storage space. This chapter describes the circuits which transfer, and control the transfer of, data between the main drums and the Central Computer.

All data transfers between the Drum System and the Central Computer System are directed by the Central Computer and are controlled by the Drum System circuits. The Central Computer selects the drum field to be read or written through the action of the drum and field selection circuits as described in Chapter 3. Selection is the result of a *Select Drums* instruction which also produces the deselect pulse which clears all the drum control circuits and prepares them to receive further instructions. After selection, a start-read or start-write pulse, the result of a *Read* or *Write* instruction, activates the Drum System circuits which perform the reading or writing operation.

4.2 BLOCK DIAGRAM ANALYSIS

Figure 2–18 shows the various subdivisions of the computer-drum data transfer control circuitry: read-write control, addressable control, status control, read circuitry, and write circuitry. The read-write control

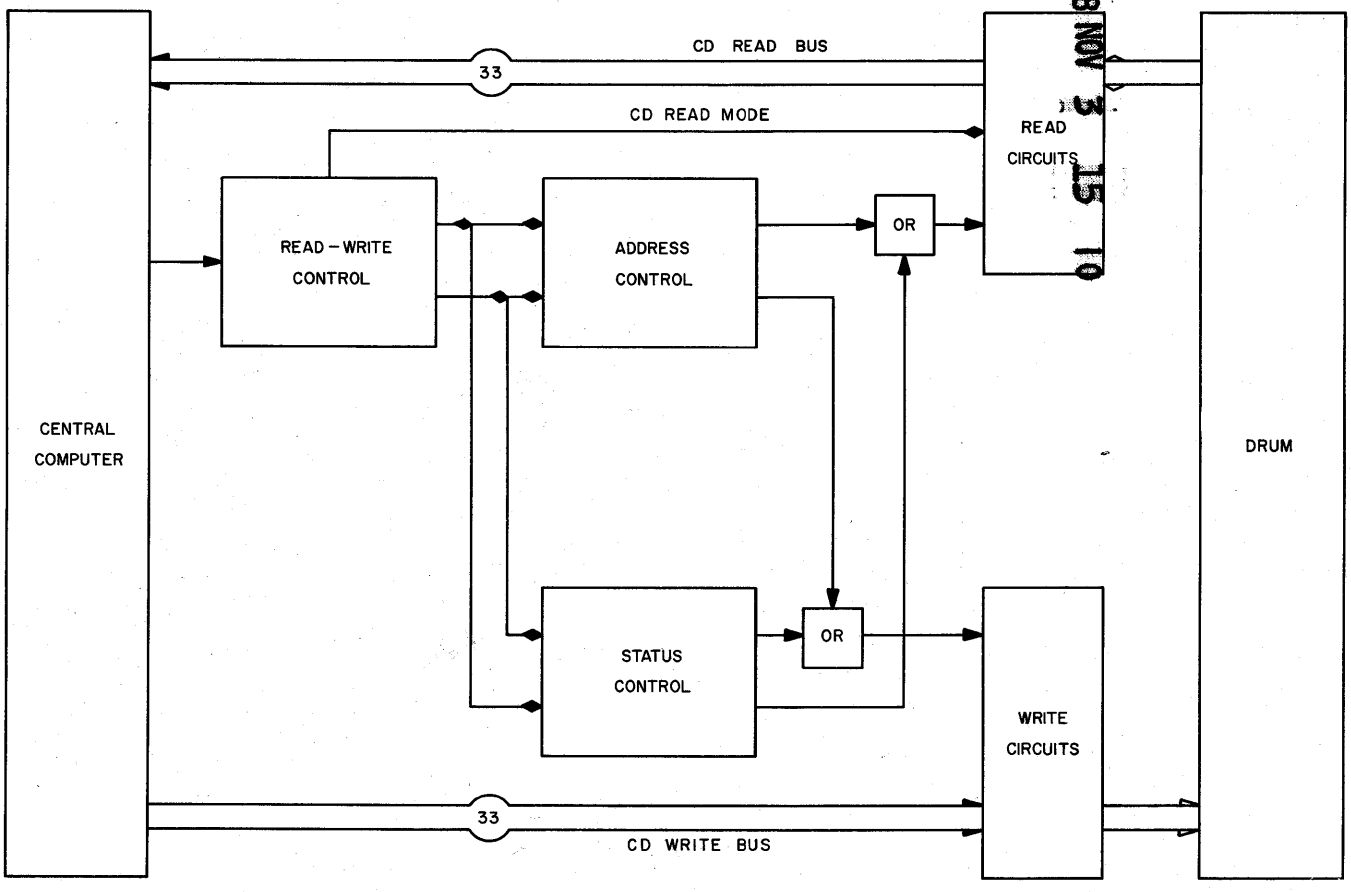


Figure 2–18. Computer Drum Data Transfer, Block Diagram

receives deselect, disconnect, start-read, start-write, and other pulses from the Central Computer and uses them to determine whether the selected field is to be read or written. The output of the read-write control consists of a read level or a write level, depending upon the operation to be performed. When reading is to be done, the read-write control also produces the CD-read-mode level which causes the drum read driver to produce the +100-volt output to enable the heads in the selected field to read.

The read or write level generated by the read-write control is applied to both address and status control. However, only one control circuit will be activated, depending upon the nature of the selected field (address or status). Timing pulses from the AM-A, AM-B, TD, RD, or MIXD drum (whichever is selected) are supplied only to the address control circuit. Note that, with the exception of the MIXD drum, all of these drums contain only addressable fields. The MIXD drum, however, does not provide timing to address control if the operation involves the transfer of XTL data. The LOG drum, which contains status fields only, and the MIXD drum, whenever an XTL or an MI field is selected, supply timing pulses directly to the status control circuit. Since the address or the status control function is performed by timing pulses from the selected drum, address or status handling of a data transfer is dependent upon the nature of the field and the timing generated by its corresponding drum. (Refer to Ch 2 for a detailed discussion of timing pulse generation and distribution.)

Under address control, data transfers from drum to computer (read operation) or from computer to drum (write operation) are controlled in the same manner. Timing pulses from the drum containing the selected field are utilized to step an angular position counter (APC). (Refer to 4.4.1.) The content of the counter is the address of the next register to come under the read-write heads. Successive APC counts are transferred to the Central Computer for comparison with the address specified for reading or writing by the program. Prior to a successful comparison, no-compare pulses are sent from the Central Computer to the drums which then resume their compare request until the APC count equals the drum address specified by the program. Upon successful comparison, the address control circuitry produces a read-compare or a write-compare level. The read-compare level conditions a gate which is sampled at CD 1 time and becomes a read-sample pulse applied to the read circuits. The write-compare level conditions another gate which is sampled at CD 3 time to produce a write pulse applied to the write circuits.

Under status control, a data transfer is dependent upon the condition of a drum register being either empty or full. A register is considered empty when it actually contains no word information or when it contains word information which has been used. A register is considered full when it contains information which has not been used. Fields that are read and written by status control are provided with two additional channels called the OD status channel and the CD status channel. A 1 bit appearing in a status channel indicates that the register is full, and a 0, indicates that the register is empty. The status control circuits examine the status channels and use the status information found there to control the reading or writing operation. In this manner, word information writing is done only on empty registers and reading is done only from full registers.

Even though the principles of address control and status control are different, the completion of an operation by either method of control is based on successful comparison. In the handling of status data transfers from the drums to the Central Computer, input word data stored on the drum is read from the drum and transferred to the Central Computer upon selection of the input field by the Central Computer. Whenever the program does not call for the particular type of data which has been transferred, the Central Computer discards the word and sends a no-compare pulse to the Drum System causing the writing of a 1 bit on the OD status channel to indicate a full register. If comparison is successful, the Central Computer does not generate the no-compare pulse, causing the writing of a 0 on the OD status channel to indicate an empty register.

Similar methods are used in the status transfer of output data from the Central Computer to the LOG drum and thence to the Output System. For a detailed description of the status control circuits, refer to Chapters 5 and 6.

The read circuits transfer data from the drum to the Central Computer. To do reading, three conditions must be satisfied: field selection, generation of a read sample pulse by either address or status control, and conditioning of the drum read driver by means of a CD-read-mode level from the read-write control circuitry. The above conditions result in enabling the heads in the selected field to pick up the information recorded on the drum surface and releasing this information to the Central Computer through the CD read bus. Along with the word being released, the read circuits also send the Central Computer an IO-buffer-loading pulse. This pulse informs the Central Computer that a word is being transferred.

The write circuits transfer data from the Central Computer to the drum. To do writing, two conditions must be satisfied: field selection and a write pulse from either the address or status control. Upon completion of writing, the write circuits reset the drum write register and produce a word-demand pulse which is sent to the Central Computer to request another word.

4.3 READ-WRITE CONTROL

The read-write control supplies the address and status controls with the read or write level necessary to their operation. It also generates the CD-read-mode level necessary for the operation of the read circuits. However, the read or write level can be produced only when all the conditions necessary to reading or writing have been met. These conditions are: first, at least 120 usec must have elapsed since any selection or other switching operation affecting the heads in the selected field has been performed; second, a start-read or start-write pulse must be received from the Central Computer; third, a field and its corresponding drum must have been selected. In addition, if writing is to be done, an IO-register-to-write-register pulse must be received from the Central Computer, indicating that the drum write register has been loaded with a word from the Central Computer.

4.3.1 Switching Delay

Switching operations in the selection circuits, and read switch introduce transient currents in the heads of the selected field, which interfere with the read or write operation. A delay circuit prevents the appearance of the read or write level for 120 usec after any of the switching operations.

Refer to figure 2–19. The deselect pulse, which is part of the *Select Drums* instruction appears immediately before any selection process. The deselect pulse triggers single-shot circuit SS1 which removes one of the inputs to AND 1 for 120 usec. With one of its inputs removed, AND 1 produces no output and a read or write lever cannot be generated.

The status of the CD mode flip-flop, FF4, determines the presence or absence of the CD-read-mode level which serves to activate the read switch. Whenever the status of FF4 is changed by a start-read or start-write pulse, SS2 is triggered through OR 4, thus removing one of the inputs to AND 1 and producing a delay of 120 usec before the read or write level can be generated. If FF 4 is cleared, and a start-read pulse appears, the flip-flop will be set and will produce the CD-read-mode level. The start-read pulse will also be passed by GT 1 and OR 4 to trigger SS 2. This action removes an input to AND 1, providing the necessary delay. A start-write pulse appearing when FF 4 is set will clear the flip-flop and will be passed by GT 2 and OR 4 to trigger SS 2.

As previously described, the action of SS 1 or SS 2 in removing one of the conditioning levels to AND 1,

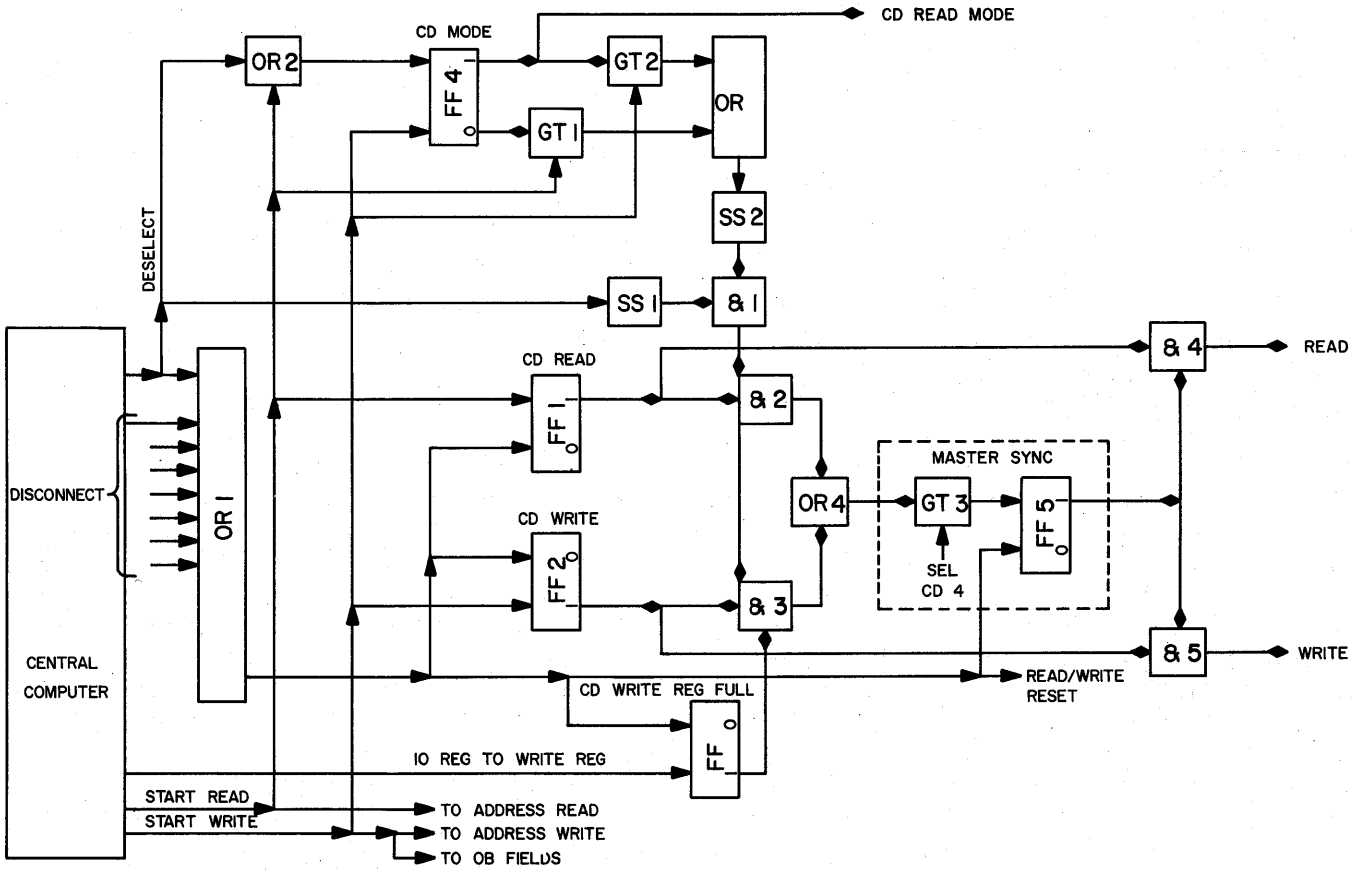


Figure 2–19. Read-Write Control Circuit, Simplified Logic Diagram

provides the delay necessary after any switching action to allow the heads in the selected field to operate effectively.

4.3.2 Generation of Read Level

Any reading or writing operation is initiated by a start-read or start-write pulse from the Central Computer. However, before a reading or writing operation is started, FF's 1,2,3, and 5 will have already been cleared by either the disconnect pulse which terminated the previous read or write operation, or by the deselect pulse which is part of the *Select Drums* instruction.

The start-read pulse from the Central Computer sets CD read FF 1, the output of which supplies a conditioning level to AND's 2 and 4. AND 2 requires another conditioning level from AND 1. The AND 1 output is present at all times except when a switching delay is in progress. The output of AND 2 is applied through OR 4 to GT 3 as a conditioning level. Gate 3 passes select CD 4 pulses to set FF 5. The output of FF 5 supplies the second conditioning level to AND 4. AND 4, thus, has an output. This output is the read level which goes to the address and the status control circuits.

The start-read pulse also sets FF 4 which sends the CD-read-mode level to the read switch to prepare the read circuits for reading.

4.3.3 Generation of Write Level

When a writing operation is programmed, the start-write pulse sets FF 2. The output of this flip-flop supplies a conditioning level to AND's 3 and 5. When the Central Computer transfers the first word to be written to the drum write register, the IO-register-to-write-register pulse sets FF 3. The output of FF 3 supplies a second input to AND 3. The third input to AND 3 comes from AND 1 after recovery from switching delays. AND 3 thus has an output which is applied through OR 4 to GT 3. This gate passes select CD 4 pulses to set FF 5. The output of FF 5 supplies the second input to AND 5. The output of AND 5 is the write level which goes to both the address and status control circuits.

The start-write pulse clears FF 4 which removes the CD-read-mode level to disconnect the read amplifiers.

4.3.4 Operation Timing

The preceeding discussions show that setting of master sync FF 5 must take place if a reading or writing operation is to be performed. The action of FF 5 insures that the reading or writing starts at the proper drum timing. Until GT 3 is conditioned, all actions in the read-write control are the result of pulses from the Central Computer and are independent of Drum System timing. Since each reading or writing cycle begins at CD 1 time, FF 5 is set at CD 4 time so that the read or write level can only appear immediately before the beginning of a full drum timing cycle.

Flip-flop 5 also insures that the Drum System does not attempt to perform a reading or writing operation unless a drum field is selected. The selected CD 4 pulse which sets FF 5 is generated only when a drum is selected. (Refer to 2.1.4 in Ch 2.)

4.3.5 Termination of Read or Write Operation

Reading or writing operations are stopped by means of a disconnect pulse. The disconnect pulse may originate at either the Central Computer System or the Drum System. When reading or writing by address, the Central Computer generates a disconnect pulse after the programmed number of words has been transferred. The Central Computer will also generate a disconnect pulse upon completion of writing of the programmed number of OB field words. When reading by status, the disconnect pulse is generated by the status disconnect counter (5.3.1) after all registers in the selected field have been examined.

The disconnect pulse clears FF's 1 and 5 to stop reading. It clears FF's 2, 3, and 5 to stop writing. With the control flip-flops cleared, the read or write levels are no longer generated and reading or writing stops.

4.4 ADDRESS CONTROL

The operation of this circuitry is dependent upon the following conditions: the selection of an addressable field, a read or write level, and a start-read or start-write pulse from the read-write control circuit. The generation of a read-sample pulse applied to the read circuits or a write-sample pulse applied to the write circuits is handled by address control in an identical manner.

4.4.1 Address Control Circuit Analysis

Refer to the address control simplified logic diagram of figure 2–20. The start-read or the start-write pulse from the read-write control clears compare addressable FF 1 through OR 3; this action results in a level being applied to one of the two inputs of AND 3. The read or the write level from the read-write control supplies the other level to AND 3. In this condition, AND 3 produces a start-compare level which simultaneously conditions GT's 1 through 5. One of these five gates passes CD 1 pulses from whichever drum has been selected.

Note that the LOG drum does not supply pulses to these gates since it does not contain addressable fields. The MIXD drum contains two status fields (XTL and SP XTL). However, in the field selection logic (Ch 3) selection of these fields inhibits the appearance of MIXD CD 1 pulses at GT 2.

The CD 1 pulse which passes through one of the five gates is used to transfer the contents of the APC

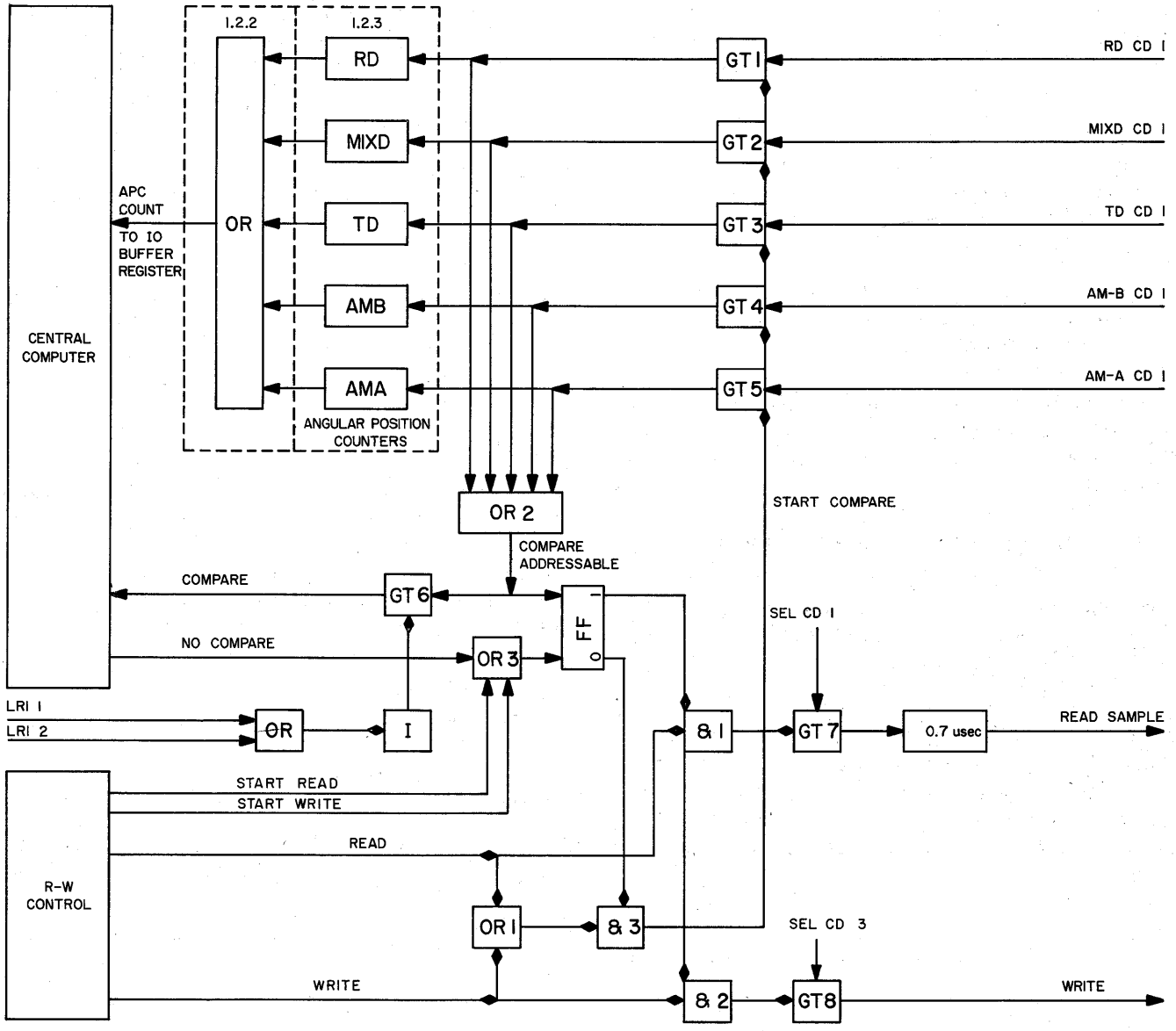


Figure 2-20. Address Control Circuit, Simplified Logic Diagram

corresponding to the selected drum to the Central Computer. Operation of these counters is described in 4.4.1. The same pulse which transfers the APC count is used to set compare addressable FF 1 through OR 2. The level produced by FF 1 is applied to AND's 1 and 2. In the case of read by address, the read level from the read-write control provides AND 2 with its second input. AND 1 conditions GT 7. However, the same CD 1 pulse which passes through one of the GT's 1 through 5 to set FF 1 cannot pass through GT 7. The first CD 1 pulse passed through GT 7 must be in a later register of the drum.

The compare-addressable pulse from OR 2, in addition to setting FF 1, is applied to GT 6. This gate is conditioned at all times, except on every other register during LRI data transfers. (Refer to 5.7 of Ch 5) the output of GT 6 is the compare pulse which is sent to the Central Computer along with each of the counts from the APC. For each unsuccessful comparison, the Central Computer returns a no-compare pulse in approximately 2 usec. The no-compare pulse clears compare addressable FF 1 which results in the removal of one of the levels from AND 1, thereby removing the conditioning level from GT 7. Therefore, CD 1 pulses cannot pass GT 7 and read-sample pulses are not produced. Clearing FF 1 also results in the application of the second level to AND 3 which again produces the start-compare pulse to begin a new cycle of comparison. When the APC count compares successfully with the address in the program, the no-compare pulse is not produced by the Central

Computer. Therefore, GT 7 remains conditioned and CD 1 pulses are passed through GT 7 as CD read-sample pulses. These pulses are sent through the 0.7 usec delay to be read circuits.

In the case of write-by-address the same process is employed except that AND 2 is conditioned by the write level and the output of FF 1 and produces the level to condition GT 8. Gate 8 passes CD 3 pulses to produce CD write pulses.

Address-controlled reading or writing is terminated by a disconnect pulse from the computer when the required number of words have been read or written. The disconnect pulse disables the read-write control which then removes the read or write level. With the read or write level absent, AND's 1 and 2 no longer condition GT 7 or 8 and no read-sample or write pulses can be produced.

4.4.2 Analysis of APC and Alarm Circuits

An APC is associated with each drum. A typical APC, the AM-A APC, is illustrated in figure 2–21. This is an 11-stage, scale-of-2,048 counter, which operates in the following manner:

Assume that all of the counter flip-flops are in the 0 state. The first CD 3 pulse input complements FF 1 to the 1 state. The d-c output of the flip-flop conditions GT 1, but not in time to pass the same step pulse that complements the flip-flop. This is so because the flip-flop rise time exceeds the 0.1-usec period of the step pulse.

The second step pulse input complements FF 1 back to the 0 state. Since the decay time of the 1 side of the flip-flop also exceeds the step pulse width, the output level remains at GT 1 long enough to pass the second step pulse to FF 2.

The gated second-step pulse complements FF 2 to the 1 state. The 1 output of this flip-flop has a longer rise time than the step pulse width.

With FF 1 in the 0 state and FF 2 in the 1 state, the third step pulse complements FF 1 to the 1 side. As before, GT 1 is not conditioned in time to pass the step pulse input. At the next (fourth) step pulse, FF's 1 and 2 remain up long enough to pass the step pulse through GT's 1 and 2, to FF 3.

This operation continues, with every step pulse input complementing FF 2, every 4th pulse complementing FF 3, every 8th pulse complementing FF 4, and every 16th pulse complementing FF 5. The number of pulses counted in this manner can be determined at any time in the counting process by examining the outputs of the counter flip-flops. The FF 1 output (1 or 0 d-c level) represents the lowest order column of a binary number; the FF 2 output represents the second column of the binary number, etc. The maximum number of pulses that can be represented by the d-c output of the counter is expressed by the function 2^n-1, in which n represents the number of flip-flops in the counter.

The counter is initially cleared by an AM-A-CD-index pulse which occurs at CD 1 time of the first

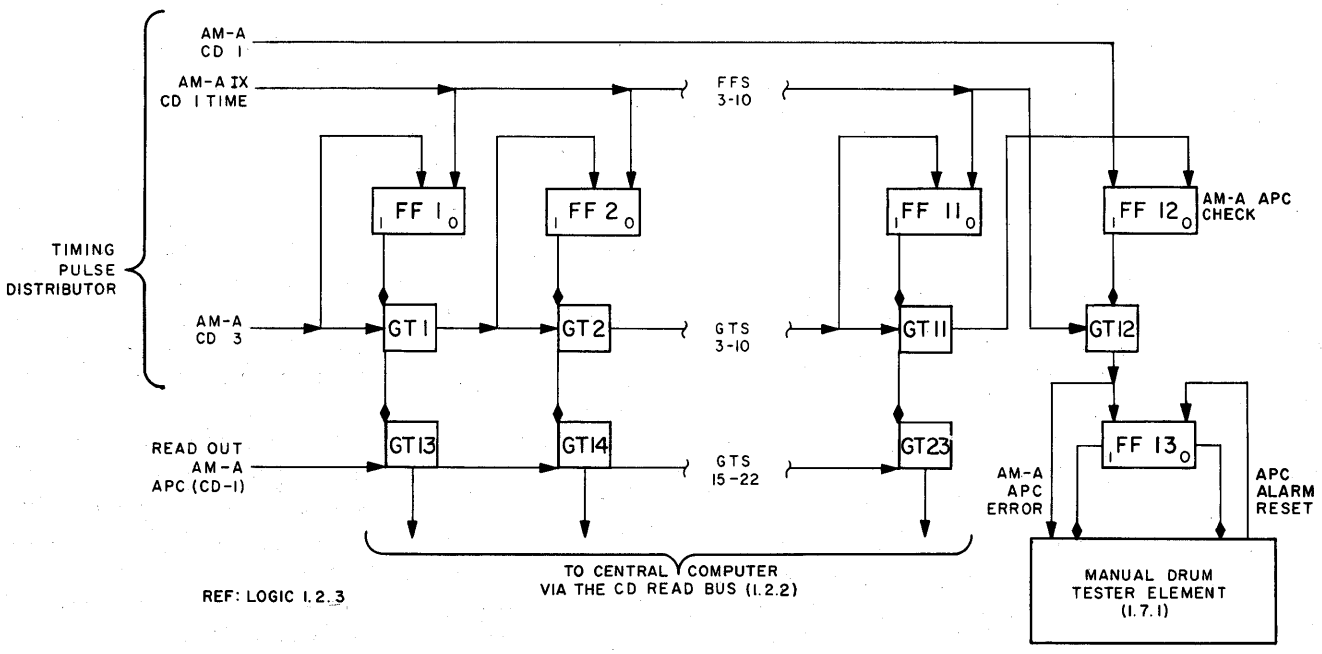


Figure 2–21. Auxiliary-Memory-Angular-Position-Counter-and-Alarm Circuit, Simplified Logic Diagram

register on the drum (register number 0). Five usec later, an AM-A-CD 3 pulse steps the counter to 1. At the CD 3 pulse of every register on the drum, the counter is stepped again. Since the first register on the drum is numbered 0, the counter setting (as represented by the states of its flip-flops) at any given time is one number higher than the number of the register under the read-write heads at that time.

Whenever one of the counter flip-flops from 1 to 11 is set, that flip-flop's output conditions the associated gate from among gates 13 through 23. When the read-out-AM-A-APC pulse is received, it pulses GT's 13 through 23. The gates that have 1-state levels pass the read-out pulse to the CD-read bus. Information received by the CD read bus is transferred directly to the Central Computer System.

Reviewing the operation of the AM-A-CD-APC, note that the counter setting at any given time is a binary number which is greater by one than the actual number of the last register counted. However, the setting is transferred during the next register (at CD 1 time, before the counter is stepped again) so that the count transferred represents the actual address of the drum register which is available for reading or writing when the next read or write sample pulse occurs.

When the AM-A-CD-APC has been stepped to 2,047, all the flip-flops are in the 1 state. The next CD 3 timing pulse (occurring during the last drum register) is passed through GT's 1 through 12, producing an end-carry pulse which clears FF 12, the APC check flip-flop.

Flip-flop 12 is normally set. It is cleared only by the APC-end-carry pulse and then set again by the next CD 1 pulse. Normally the index pulse occurs while FF 12 is cleared. At this time gate 12 is not conditioned and the index pulse is not passed. If there has been an error in counting, the end-carry pulse does not appear to clear FF 12 just before the index pulse appears. The index pulse, in this case, is passed by GT 12, producing an AM-A-APC-error pulse which is sent to the manual drum tester element. In the manual drum tester element, the AM-A-APC-error pulse sets a flip-flop which produces an error indication at the maintenance console. Also, FF 13 is set by the gated index pulse. The 1-state output of FF 13 goes to an error indicator on the drum unit test panel. Flip-flop 13 must be manually cleared after an error is indicated.

4.5 READ CIRCUIT ANALYSIS

The read circuits read words from the selected drum field and transmit them to the central computer. For a reading operation to take place the read switch must be activated by the CD-read-mode level from the read-write control circuit.

When the read switch is activated each read sample pulse transmits a word to the Central Computer.

The read switch (fig. 2–22) consists of a pair of diodes connected in each line carrying signals from a read-write head to a drum read amplifier. These diodes are used to isolate the drum read amplifier from the read-write heads when a writing operation is in progress. When reading is to be done, the diodes are used to connect the drum read amplifiers to the read-write heads. This is necessary because the same heads are used for both reading and writing.

Whenever a drum field is selected for either reading or writing the +125-volt-d-c-select-field level from the drum field driver is applied to the anodes of the read switch diodes. (See Ch 3.) Except when a reading operation is to be performed the CD-read-mode level is not present and the output of the drum read driver is a +150-volt-d-c level. This level is applied through the input transformers of the drum read amplifiers (only one transformer is shown on fig. 2–22) to the cathodes of the read switch diodes. With the cathodes at a higher d-c voltage than the anodes, the diodes cannot conduct and no signals from the write circuits can reach the drum read amplifiers.

When a reading operation is to be performed, the read-write control circuit sends the CD-read-mode level to the drum read driver. Under this condition, the output of the drum read driver is a +100-volt-d-c level. This level applied to the cathodes of the read switch diodes places the cathodes at a lower d-c voltage than the anodes and the diodes can conduct. This condition connects the drum read amplifiers to the read-write heads and reading can be done.

The information under each of the 33 read heads (a 1 bit or a 0 bit) is transferred through the read switch to the corresponding drum read amplifier. For each 1 bit read by the heads, the corresponding gates (1 through 33) will receive a conditioning level coincident with the read-sample pulse; the conditioning from 0 bits is not coincident with the read-sample pulse. Therefore, gates that produce an output represent 1 bits and gates with no output represent 0 bits.

Figure 2–22 shows that the gates connected to each of the 33 drum read amplifiers are divided into two groups; the first group consists of gates providing their output to bits LS through L10 and L14 through R10, and the second group to parity, L11, L12, L13, R11, R12, R13, R14, and R15 bits. The bits in the second gate group correspond to the unused bits in radar data words.

The above logic arrangement serves to ensure that when the RD fields are read during testing, false in-

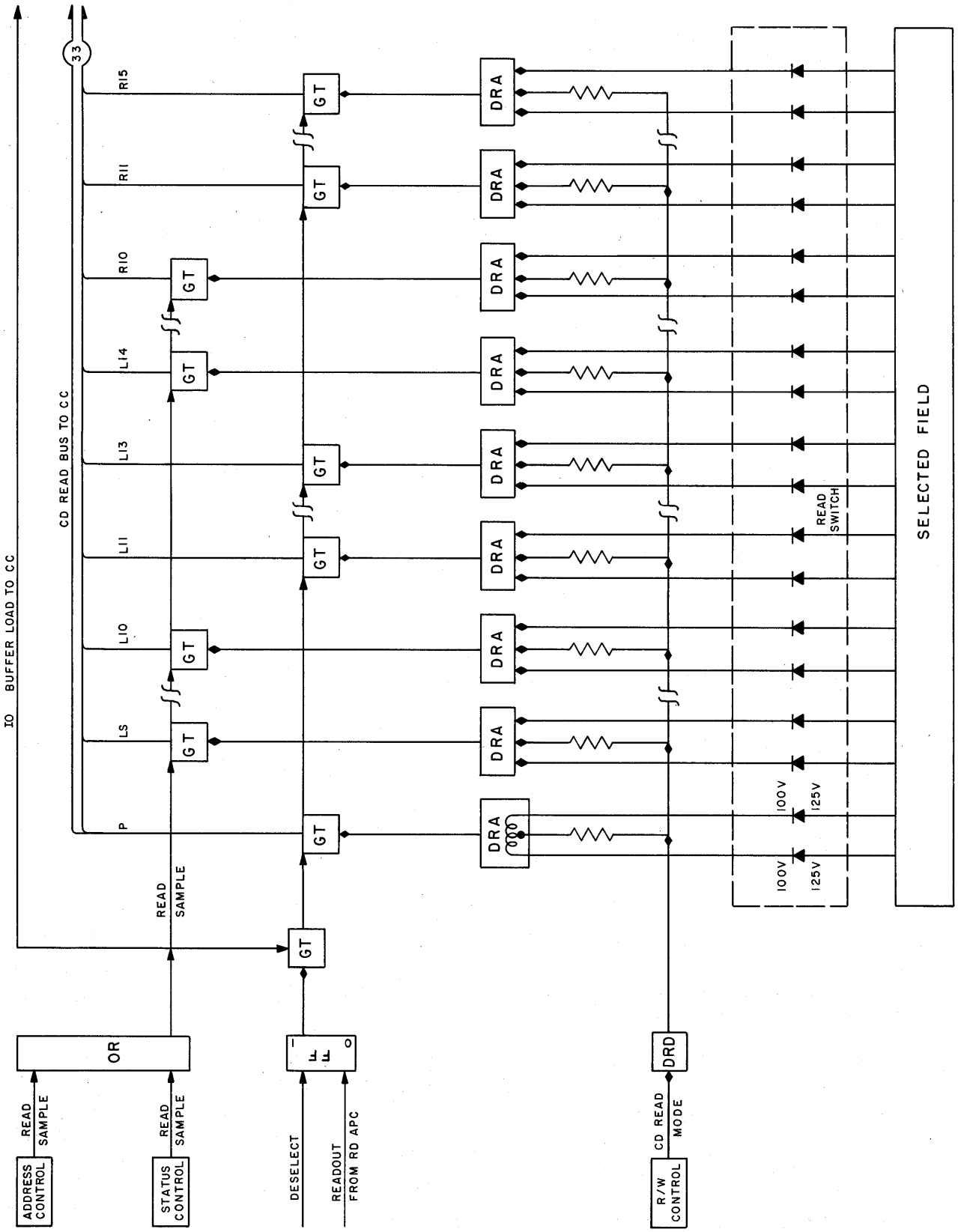


Figure 2–22. CD Read Circuit, Simplified Logic Diagram

formation is not produced by the unused gates and drum read amplifier.

During marginal checking operations, the drum read amplifiers without an input will normally provide an output of 0 to 5 volts which is sufficient to condition the gates. This results in false information being transmitted to the Central Computer through the CD read bus.

When reading is done from any field, except RD fields, the deselect pulse sets the flip-flop to condition the control gate to pass read-sample pulses. In this condition, all 33 read gates will receive read-sample pulses and provide a correct word pattern through the CD read bus.

During reading of RD fields, the readout-RD-APC pulse will clear the flip-flop to remove the conditioning level to the control gate. In this condition, the read gates in the second group previously mentioned will not receive read-sample pulses and accordingly will not produce an output.

The read-sample pulse which, in effect, releases the information word to the Central Computer also becomes an IO-buffer-loading pulse which indicates to the Central Computer circuits that a word is being transferred.

4.6 WRITE CIRCUIT ANALYSIS

The write circuit operates upon receipt of a write pulse from either address or status control circuitry. Refer to figure 2–23. The write pulse received is applied to OR 1 and OR 2. From OR 1, the pulse causes the writing on the drum surface of the word stored by the Central Computer in the drum write register. From OR 2, the pulse is delayed to reset the flip-flops in the write register; it also forms the word-demand pulse to the Central Computer, after the word has been written on the drum.

The pulse stretcher connected to the output of OR 1 effectively widens the write pulse to the width necessary for writing on the drum surface. The drum write driver produces an output which causes the drum writers to write when its input drops from +10 volts to −30 volts. The write pulse clearing the flip-flop applies the −30-volt level to the drum write driver. The same write pulse passes through the delay circuit and sets the flip-flop 1.7 usec later removing the −30-volt input to the drum write driver. Thus, for 1.7 usec the output of the drum write driver conditions the 33 drum writers to transfer the contents of the drum write register onto the drum surface.

The write pulse at the output of OR 2 is connected

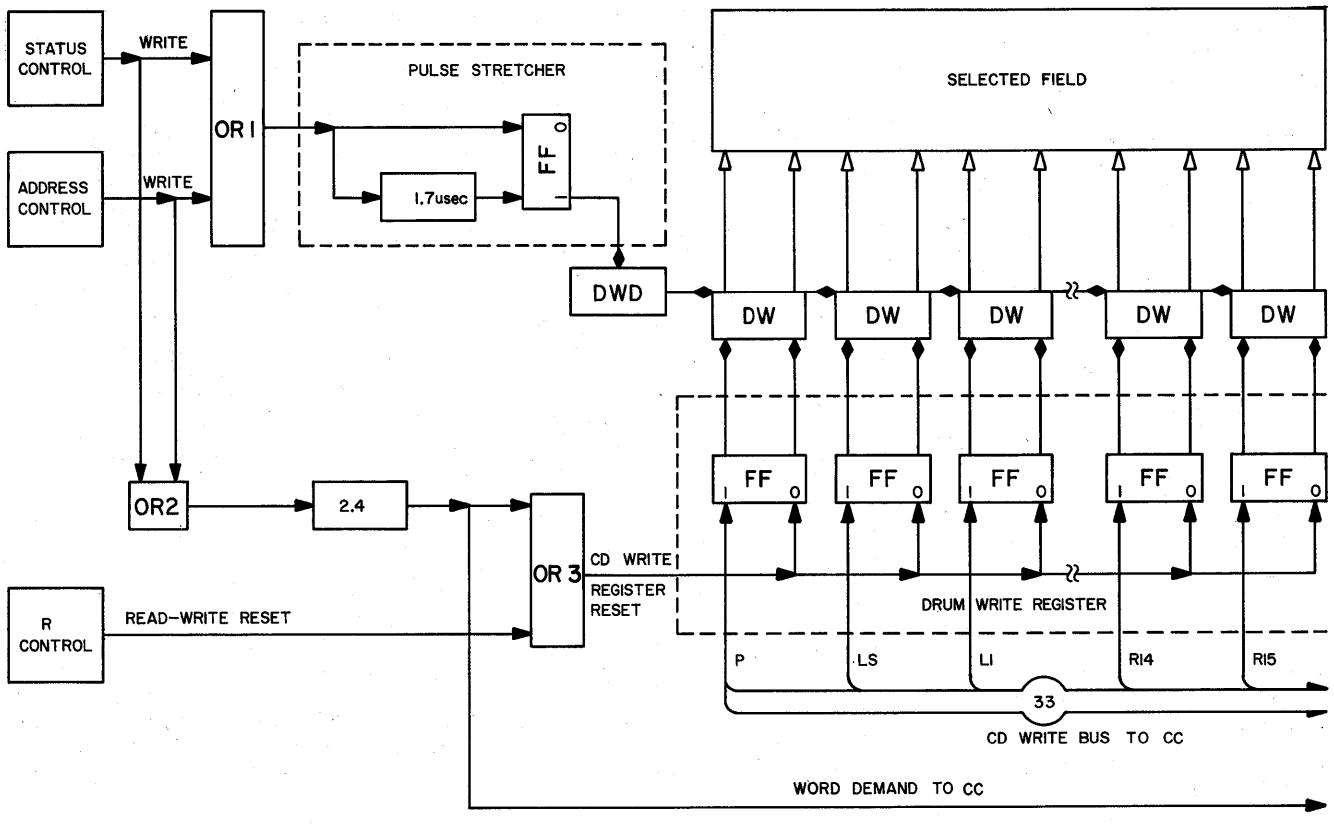


Figure 2–23. CD Write Circuit, Simplified Logic Diagram

to another delay circuit which at the end of 2.4 usec produces a pulse applied to OR 3. This 2.4-usec delay compared to the 1.7-usec delay at the pulse stretcher results in a time gap of 0.7 usec which ensures the writing process to be fully accomplished before resetting the drum write register and sending a word demand to the Central Computer. The write register reset originated by the write pulse and the read-write reset pulse originated at the read-write control are applied to the drum write register through OR 3.

CHAPTER 5

INPUT FIELDS DATA TRANSFER

The Input System of the AN/FSQ-7 receives large quantities of input data for transfer to the Central Computer System. This input information is received at different repetition rates and at random intervals. The Drum System stores this data for later transfer to the Central Computer System. The transfer from the Drum System to the Central Computer System is performed on Central Computer System command.

The drum fields on which information is written are named according to the source of their information. Manual input data is written on the MI field, crosstelling input data is written on the XTL field, etc. The LRI input differs from the other inputs in that it utilizes two drum fields instead of one. These fields are designated LRI 1 and LRI 2. The GFI data utilizes only one drum field.

In order to regulate the placement of input data on the drum fields, each field is provided with two control channels in addition to the channels assigned to store information words. These two channels are named the OD status channel and the CD status channel. The OD status channel indicates to the OD circuits of the field the availability of the individual registers as storage space for incoming words. The CD status channel indicates to the CD circuits of the field the presence of a word in a register, so that it may be transferred to the Central Computer System when requested.

An OD status control circuit associated with each of the input fields reads the contents of the OD status channel. When a storage space is found, the OD status control circuit notifies the Input System that such storage space is available. The Input System examines its own circuits to find a word or words (called a message) that can be written in the space available. If a word is found in the Input System, it is transferred to the OD write circuit of that field. The Input System notifies the OD status control circuit that a word is being sent. The status control circuit causes the OD write circuit to write the transferred word on the drum. The status control circuit also writes in the CD status channel to indicate that a word is being written in that register.

If the register space is available but the Input System has no data for transfer at that time, the status control circuit writes in the CD status channel to indicate that the register remains empty.

If the reading of the OD status channel for any given register does not reveal an empty storage space, the status control circuit doing the reading writes in the CD status channel. This indicates to the CD element that a word is still present in that register.

In addition to the OD and CD status channels, a third channel, known as the marker status channel, is provided for the XTL fields. The marker status channel contains markers written by the Central Computer System via the CD circuits. A marker is a 1 bit that is written in the marker channel. If there is to be no marker, a 0 bit is written in the marker channel. Each marker in this channel indicates to the XTL OD input circuit the register in which the wiring of a multiword message should begin. The writing operation performed under the control of marker status circuits is slightly different from the writing by status controlled circuits. Writing of a message can begin only in a register which is both empty and marked as the first register of a slot. The remaining words in the input data message may then be written in consecutive registers without the need for examining the status of the registers.

During the writing of GFI words, the GFI OD input circuits write relative time information as part of the GFI word. The relative-time-counter-step circuit receives time indications in the form of pulses from the Central Computer System and synchronizes these pulses with the drum timing pulse operating cycle. The synchronized pulses are used to step the relative time counter. Synchronization is necessary to prevent writing while the contents of the relative time counter is changing.

The operations of the MI and XTL fields, which are on the MIXD drum, are timed by the MIXD drum timing circuit. Timing data from this circuit is also sent to the Input System circuits associated with these fields.

The LRI fields and the GFI field are contained on the LOG drum. Their operations are timed by the LOG drum timing circuit. Timing data from the LOG timing circuit is also sent to the Input System circuits associated with those fields.

Manual input and GFI data are received in the form of one word (33 bit) messages. The LRI messages consist of two words and XTL messages consist of three words. The words of the LRI and XTL messages are written on consecutive registers of the respective fields.

The transfer of input data to the Central Computer from any input field is initiated by instruction pulses

from the Central Computer and controlled by status channel CD circuits associated with each input field. These circuits operate similarly to the status channel OD circuits described above. In the case of CD transfer, however, the information read from a drum register must be accepted by the Central Computer before that register is made available for further information.

This chapter describes in detail the transfer of input data from the Input System of the AN/FSQ-7 to the Drum System, and from the Drum System to the Central Computer System. Paragraph 5.1 is a block diagram analysis of the transfer operations using MI data transfer as an example. The paragraphs which follow consider separately each input field and analyze: first, the circuitry required for writing data on that field and, second, the circuitry required for reading data from the field.

5.1 INPUT FIELDS DATA TRANSFER, BLOCK DIAGRAM ANALYSIS

Figure 2–24 illustrates in block diagram form the data transfer and control circuitry associated with the MI field. The MI field was selected for detailed discussion because it illustrates most simply the method of transfer control which is common to all the input fields. Subsequent sections will analyze separately the transfer circuitry of each field and will explain deviations from the common pattern.

5.1.1 Input Fields OD Transfer

An input field OD transfer is initiated by control pulses from the OD status circuits of the associated input field.

A 1 bit in the MI OD status channel (fig. 2–24) indicates that the associated register contains a word written on a previous drum revolution that has not as yet been utilized by the Central Computer System. A 0 bit indicates that the register is available either because it is empty or because it contains a word already read by the Central Computer System. If a 0 is detected in the OD status channel, indicating that a specific register is empty or contains old information, the OD status control circuit produces a word-demand pulse.

The demand pulse goes to the Input System and examines the MI data storage registers for information intended for the Drum System. If no information is available, the Input System does not respond to the demand pulse. The absence of a response causes the MI OD status control circuit to write a 0 in the CD status channel. The 0 indicates that no data is present in that register for reading into the Central Computer System. However, if an input word is found, the Input System transfers the word into the MI OD write register. The Input System then sends a data-available pulse to the MI OD status control circuit.

The data-available pulse returned by the Input System causes a write pulse to be produced in the MI OD status control circuit. The write pulse goes to the OD write circuit, and causes the word in the write register to be written on the drum. The writing operation is performed during the period of the write-sample pulse which comes from the timing circuit. At the same time, in addition to forming the write pulse, the data-available pulse causes a 1 to be written in the CD status channel. Immediately after the word and CD channel are written, a reset-write-register pulse is sent to the OD write circuit from the MI OD status control circuit. This pulse clears the write register in the OD write circuit.

All operations of the OD status control circuit are synchronized by timing pulses. These pulses are generated by the timing circuit on the drum which contains the field being written. Drum timing is discussed in detail in Chapter 2.

The above discussion considered the condition in which the OD status channel contains a 0 bit. However, if a word has been written in a given register during an earlier drum revolution and if the word has not been read by the Central Computer, a 1 bit is read at the point in the channel associated with that register. Reading of the 1 bit prevents the production of the demand pulse. In such cases, a 1 is written in the CD status channel.

5.1.2 Input Fields CD Transfer

All input field CD transfers are initiated by a deselect pulse (fig. 2–24) from the Central Computer. The Central Computer then selects the field from which information is desired and initiates the operation of the CD status circuits of the selected field. The operation is as follows: The deselect pulse clears the CD-selection register and selection decoder of the Drum System (see fig. 2–24). This pulse is also used to clear the CD read-write control circuit. In the CD read-write control circuit the deselect pulse is changed to a read-write reset pulse and is sent to the CD read-status-fields disconnect counter to reset the counter. Thus, these circuits are prepared to receive new information from the Central Computer System.

A *Select* instruction, in the form of index-interval pulses, follows the deselect pulse. The index-interval pulses from the Central Computer System cause the CD selection register and selection decoder to produce a select-field level. The Central Computer System sends a start-read pulse to the CD read-write control circuit which develops the read-by-status level. The presence of the select-field and the read-by-status levels prepares the CD status control circuit of the selected field to permit reading to begin. Reading is then initiated by control pulses from the selected CD status circuit. In the case of the MI field, for example, a 1 bit detected on the CD status channel indicates the presence of a word on the associated drum register that has not beeen read. This

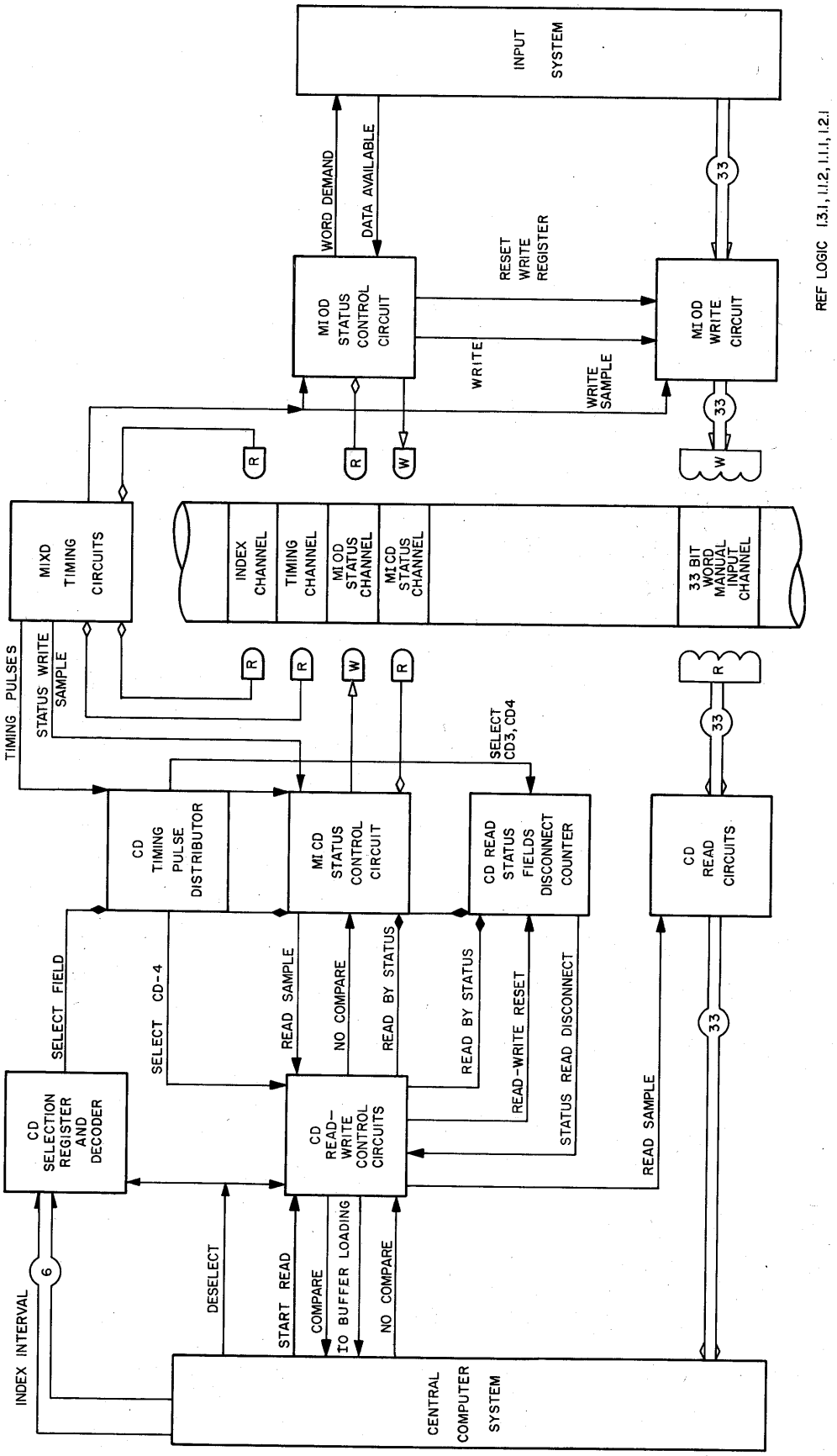


Figure 2–24. MI Data Transfer and Control Circuits, Block Diagram

causes the MI CD status circuit to send a read-sample pulse to the CD read-write control circuit.

The read-sample pulse branches in the CD read-write control circuit. It goes to the Central Computer System as an IO-buffer-loading pulse and a compare pulse and to the CD read circuit as a read-sample pulse. On receipt of the read-sample pulse, the CD read circuit transfers the word on the associated drum register to the Central Computer System.

The IO-buffer-loading pulse informs the Central Computer System that a word is being sent to it. The compare pulse is associated with status identification control and requests the Central Computer System to check the identification bits of the transferred word with special identification bits in the Central Computer System program.

If comparison fails, the Central Computer System rejects the word and sends a no-compare pulse to the MI CD status control circuit via the CD read-write control circuit. The MI CD status control circuit, at this time, causes the status-write-sample pulse from the MIXD timing circuit to be written as a 1 bit on the OD status channel. This prevents the writing of a new word on the drum register involved. If comparison is successful, the word is accepted by the Central Computer System and the no-compare pulse is not sent to the Drum System. The MI CD status-control circuit, at this time, causes the status-write-sample pulse to be written as a 0 bit on the MI OD status channel. This permits a new word to be written in the drum register that has been read.

Timing pulses from the MIXD timing circuit are fed to the CD status control circuit to perform various control functions. Timing pulses also go to the CD read status fields disconnect counter to cause a status-read-disconnect pulse to be developed at the end of one complete revolution of the MIXD drum, whenever a not-continuous-read-by-status level from the manual test circuit is present.

If it is desired to read all information contained in the registers of an input field, basic status control is used. In this type of operation, no-compare pulses are absent, and all information read is accepted by the Central Computer. Basic status-controlled reading is used only as a test procedure.

5.2 MI OD TRANSFER, CIRCUIT ANALYSIS

Figure 2–25 illustrates the circuitry which controls the MI OD data transfer. The MI OD transfer can be considered to be initiated by the first OD 4 pulse in any revolution.

This OD 4 pulse clears status FF's 1, 2, and 4 and is also applied to GT 4. Gate 4 is conditioned to pass this OD 4 pulse whenever an operate level from the computer test control circuit is present to produce conduction in OR 1. The operate level is present at all times, except when the Drum System is in the test mode of operation. The output of GT 4 becomes a reset-write-register pulse which is sent to the MI OD write circuit. Figure 2–26 shows the MI write circuit; write circuits associated with other OD input fields are similar. During normal operation, the write register of the MI OD write circuit is cleared every OD 4 time.

An OD 1 pulse from the timing circuit appears at GT 1 2.5 usec after clearing by OD 4. (See fig. 2–25.) Gate 1 is conditioned to pass this pulse if a 1 is detected in the MI OD status channel. Detection of a bit in the channel is performed by the channel read head and read circuit. By positioning of the read head, the OD status bit associated with a register is read 10 usec before the register is written. When a 1 is read in the MI OD status channel, indicating that the register associated with that bit contains a word, FF 1 is set. With FF 1 in the 1 state, FF 3, which had been cleared by an OD 2 pulse from the previous timing cycle, remains in the 0 state. This maintains a conditioning level at GT 6. Gate 6 passes an OD 1 pulse, thus causing conduction in OR 2. Conduction in OR 2 sets FF 4 in the status-write circuit to the 1 side. The FF 4 output is then applied to the drum-writer. When the status-write-sample pulse is received from the timing circuit (at approximately OD 3 to OD 3 plus 1.7 usec), the 1 level at the drum-writer input is written on the MI CD status channel. Placing of a 1 in the CD status channel indicates to the CD status circuit that the register contains a word.

If the MI OD status channel bit is a 0, there will be no output from the read amplifier to condition GT 1 and pass the OD 1 pulse. As a result, FF 1 will not be set to the 1 side but will remain in the 0 position where it had been placed by the previous OD 4 pulse. The output level from FF 1 goes to GT 2 and passes the next OD 3 pulse from the timing circuit.

The output of GT 2 sets FF 3, and goes to GT 3 which is conditioned by an operate level from the Central Computer System test control circuit. As stated previously, the operate level is present throughout normal operations. The output of GT 3 is the drum-demand pulse which goes to the Input System storage registers associated with the MI field.

In the Input System, the drum-demand pulse examines the MI registers in a serial sequence until it finds a storage register containing information. If a word intended for transfer to the Drum System is found, a data-available pulse is generated 1 usec after the OD 1 pulse following drum-demand pulse OD 3. The data-available pulse transfers the MI word to the OD write register of the MI OD write circuit, shown in figure 2–26 by having all the 1 bits in the input word set the corresponding flip-flops in the write register.

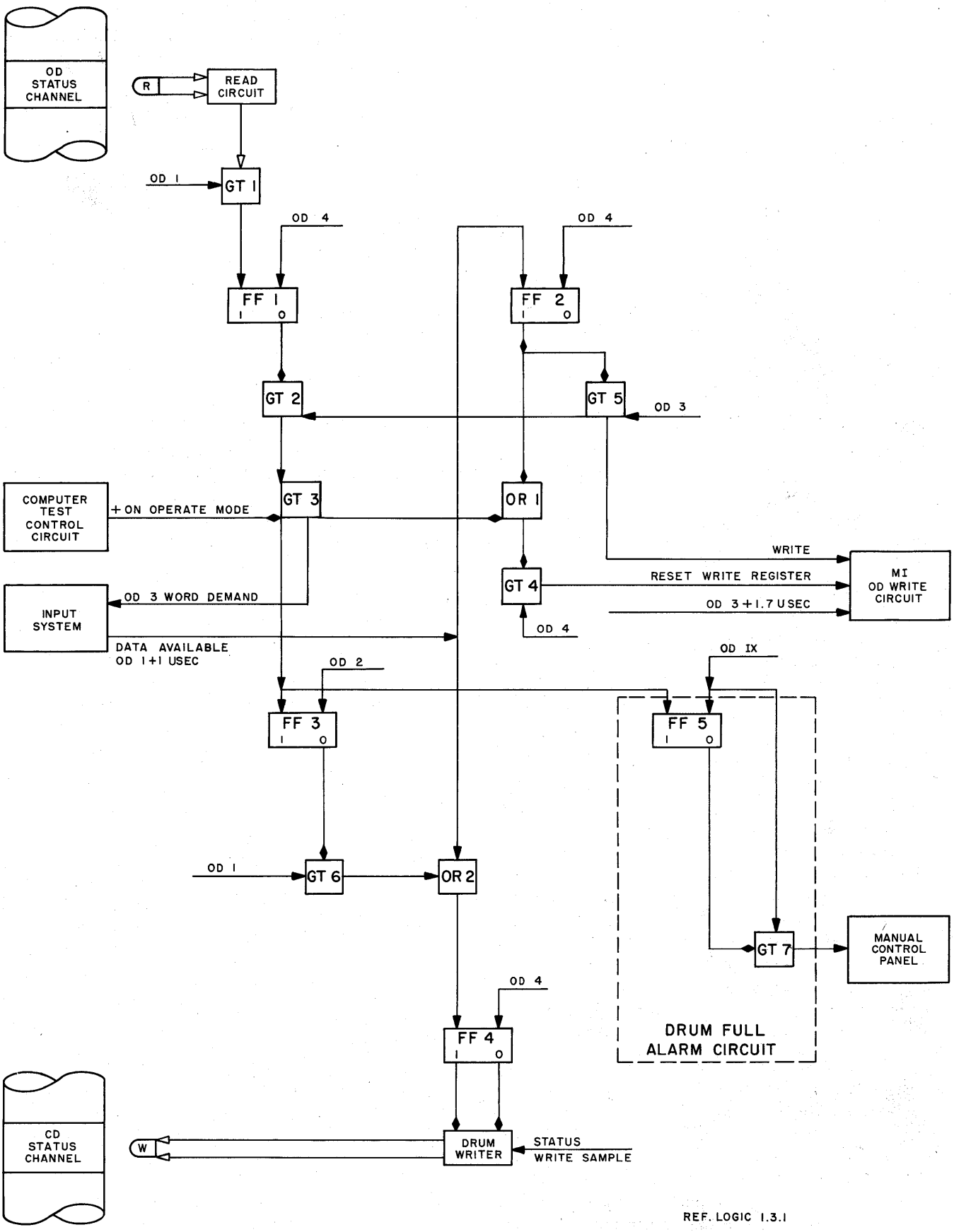


Figure 2–25. MI OD Status-Controlled Circuit, Simplified Logic Diagram

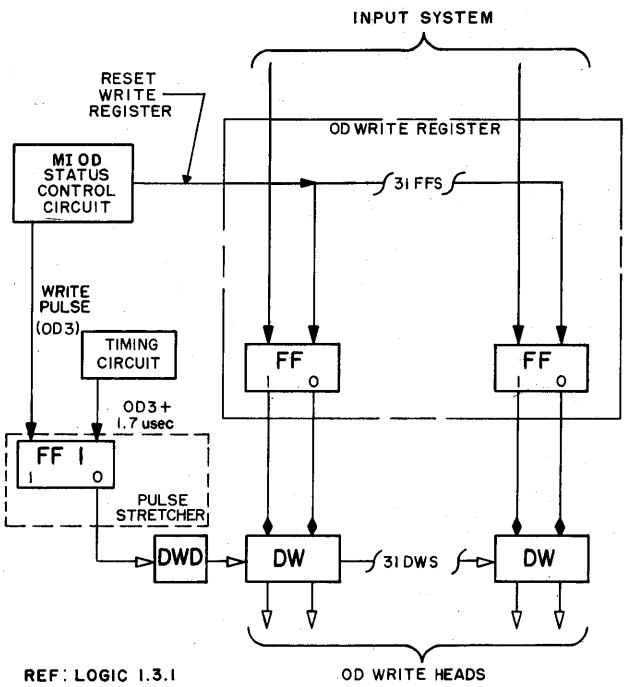


Figure 2–26. MI OD Write Circuit, Simplified Logic Diagram

The data-available pulse also goes to FF 2 and OR 2 in the status-control circuit. (See fig. 2–25.) In the status control circuit, the pulse is passed by OR 2 to set FF 4 to the 1 side. When the status-write-sample pulse is sent by the timing circuit (at OD 3 time), a 1 is written in the CD status channel.

The data-available pulse sets FF 2 to the 1 side. The 1 output of FF 2 goes to GT 5 and conditions the passing of the next OD 3 pulse. This OD 3 pulse is the write pulse; it goes to the pulse stretcher in the MI OD write circuit. (See fig. 2–26.) In the pulse stretcher, the write pulse sets FF 1 to the 1 side. After 1.7 usec, an OD 3 + 1.7-usec pulse from the timing circuit clears the flip-flop. During the 1.7 usec that FF 1 is in the 1 state, the flip-flop output produces a positive output from the drum write driver. The drum write driver's positive output causes the drum writers to conduct, transferring the contents of the write register to the write heads. The write heads then place the word on the drum surface.

If no information is found in the MI storage registers, no data-available pulse is produced; FF 2 is not set; therefore the write pulse is not produced. Also there is no input to OR 2. (GT 6 output is also absent because a 0 has been detected in the OD status channel.) As a result, FF 4 remains in the 0 state where it has been placed by the OD 4 pulse. This places a 0 level at the input to the drum writer. When the status-write-sample pulse from the timing circuit arrives at the drum writer (at OD 3 time), the 0 is written in the MI CD status channel to indicate that the register is still empty.

At the OD 4 pulse which follows the generation of the write pulse, status control circuit FF's 1, 2, and 4 (fig. 2–25) are cleared. A reset-write-register pulse is produced, which clears the write register in the OD write circuit.

During the operation of the OD status control circuit, FF 5 and GT 7 in the drum full alarm circuit serve as a check on the operation of the status-controlled reading and writing operations. At the end of each revolution, an index (OD IX) pulse from the timing circuit clears FF 5 and goes to GT 7. Gate 7 is conditioned when the 0 output of flip-flop 5 is present. However, GT 7 does not pass the same index pulse that clears the flip-flop because the rise time of the 0 side of the flip-flop exceeds the period of the index pulse. The index pulse at GT 7 decays before the 0 d-c level is present. If, at any time during the following revolution of the drum, a 0 bit is detected in the MI OD status channel to indicate that there is an empty register, the ouput of GT 2 sets FF 5 to the 1 side. However, if no empty register is detected, FF 5 remains in the 0 state. When the next index pulse arrives at the end of one complete drum revolution, the conditioning level is still present at GT 7. Gate 7, therefore, does have an output, the drum-full-alarm pulse. This pulse goes to the manual control panel as an indication that the MI field is full.

Figure 2–27 summarizes the sequence and timing of an OD-status-controlled writing operation. It can be seen from the figure that the status bit in the OD status channel must be detected 15 usec before the word is written on the field. Five of the 15 usec are provided because the reading of the OD status channel is performed at CD 1 time and the writing of the word is performed at OD 3 time. To provide the additional 10 usec, both the writing head (in the CD system) and the reading head (in the OD status control circuit) are offset. The OD status bit, consequently, comes under the read and write head 10 usec earlier than the associated register comes under the drum heads. The 10 usec produced by the physical arrangement of heads, added to the 5 usec between the operational timing pulses, result in the necessary 15-usec delay.

Since 15 usec are required to complete the status-controlled writing operation for each register on the field, it is necessary to overlap the operations for successive field registers. The registers are separated by only 10 usec. Overlapping has no effect on the sequence of status-controlled operations. However, it should be remembered that the last 5 usec of the first of two registers operation coincide with the first 5 usec of the second register.

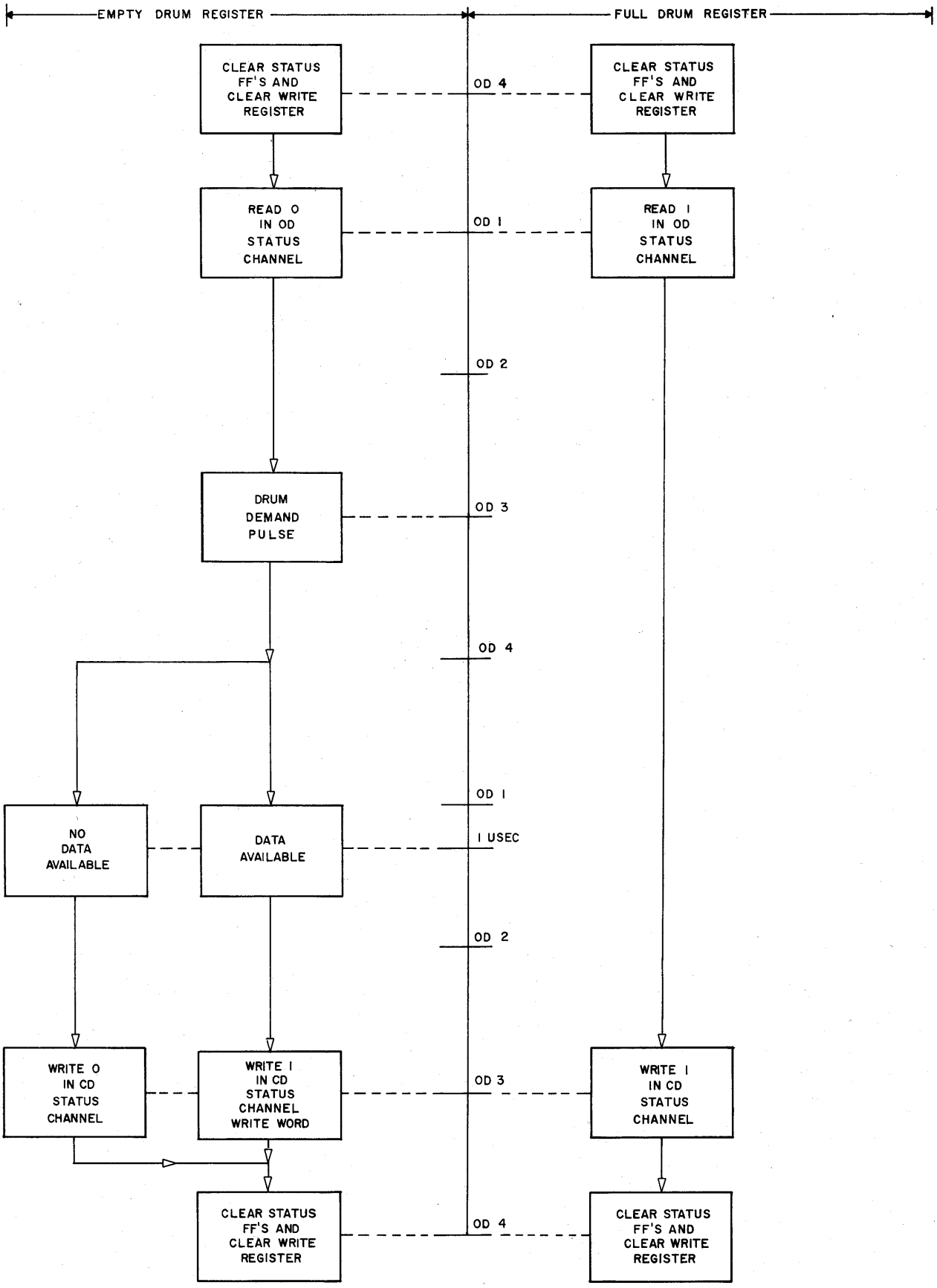


Figure 2–27. Time Sequence of Significant OD Status Writing Operations

5.3 MI CD TRANSFER, CIRCUIT ANALYSIS

Reading of the MI field is initiated by the Central Computer System. The computer selects the MI field through the action of the drum and field selection circuits as described in Chapter 2. After selection, the start-read pulse from the computer causes the CD read-write control circuit to produce the read-by-status level as described in Chapter 3. The read-by-status level and the select-MI-field level are combined to activate the MI CD status control circuit which then controls the reading of the MI field.

Figure 2–28 shows the MI CD status control circuit. There is a similar circuit for each of the other input fields. The read-by-status level and the select-field level cause AND 1 to conduct. The output of AND 1 conditions GT's 3 and 4.

When a 1 bit, indicating a full register, is detected on the MI CD status channel, the read amplifier produces an output that conditions gate 1 to pass a CD 1 pulse. The CD 1 pulse goes to GT 3, which has been conditioned by AND 1. The resulting GT 3 output is the read-sample pulse which is sent to the CD read circuit. The CD read circuit transfers the word on the associated drum register to the Central Computer System. The operation of the CD read circuit is discussed in Chapter 4.

The read-sample pulse is sent to the Central Computer System as a compare pulse and as an IO-buffer-loading pulse. The IO-buffer-loading pulse informs the Central Computer System that a word is being sent. The compare pulse requests the Central Computer System to check identification bits contained in the word transferred from the input field with special identification bits in the Central Computer System program. If these identification bits do not compare, the Central Computer System rejects the word and sends a no-compare pulse to GT 4 in the CD status control circuit. (See fig. 2–28.)

Gate 4 (which is conditioned by AND 1) passes the no-compare pulse to OR 1. The output of OR 1 sets FF 1. The 1-state output of FF 1 causes the drum writer to enter a 1 bit on the OD status channel when the write-sample pulse is received (CD 3 time). This 1 bit prevents the writing of a new word on the associated drum register. Two and one-half usec after the writing of the OD status channel, FF 1 is cleared by a CD 4 timing pulse.

If the comparison of the identification bits of the transferred word by the Central Computer System is successful, the Central Computer System accepts the word and the no-compare pulse is not sent. Flip-flop 1 remains in the 0 state, causing a 0 bit to be entered on the MI OD status channel by the drum writer. This 0 bit allows the associated drum register to be used for a new word. If basic status control is used, no-compare pulses are not returned by the Central Computer System, and

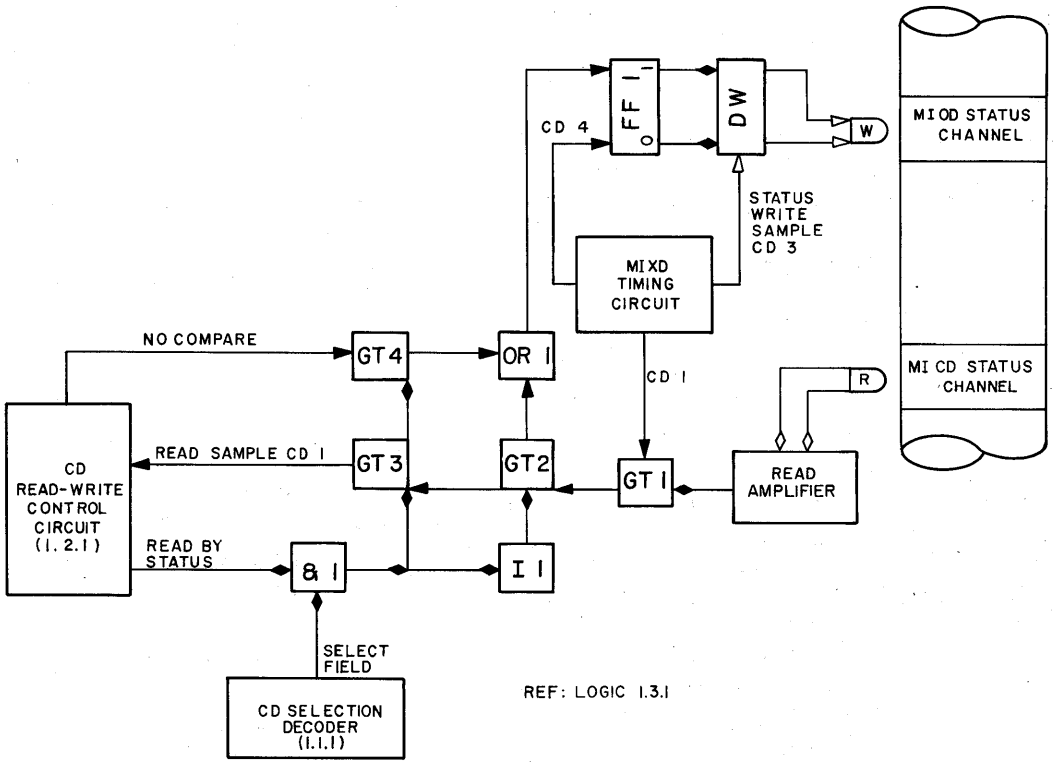


Figure 2–28. MI CD Status Control Circuit, Simplified Logic Diagram

all information read is accepted. Basic status-controlled reading is used only as a test procedure.

If the MI field is not the selected field, the select-field level is absent and AND 1 does not conduct. When AND 1 does not conduct, it allows inverter circuit 1 to produce a positive-output level which conditions GT 2. When a 1 bit is read on the OD status channel, the read circuit conditions GT 1 to pass a CD 1 pulse to GT 2. Gate 2, conditioned by the inverter output, sends the CD 1 timing pulse to FF 1 via OR 1. Flip-flop 1 is set, causing the drum writer to enter a 1 bit on the OD status channel when the status-write-sample pulse is received. The 1 bit on the OD status channel preserves the information on the associated drum register.

When a 0 bit is detected on the CD status channel, none of the gates conduct. Flip-flop 1 remains in the 0 state, causing a 0 bit to be entered on the OD status channel at CD 3 time.

The number of drum registers that are checked for the presence of information during a status read operation are counted by the CD read-disconnect-counter circuit. When 2,048 registers have been counted (one complete revolution of the drum), the CD read-disconnect counter sends a status-read-disconnect pulse to the CD read-write control circuit. The status-read-disconnect pulse stops the reading operation. A description of the operation of the CD read-status-disconnect counter is given below.

During normal operation, the not-continuous-read-by-status level is present. (See fig. 2—29.) This level comes from the manual test circuits and is applied to AND 1. The start-read pulse sent by the Central Computer System to the CD read-write control circuit causes a read-by-status level to be developed. The read-by-status level goes to AND 1 in the CD read-status-fields-disconnect counter. The selected field level provides the third level necessary for conduction in AND 1.

Gate 1, conditioned by the output of AND 1, passes the selected CD 3 pulse to FF 1. The 1-state output from FF 1 conditions GT 2 to pass the selected CD 4 pulse. The output from GT 2 steps the disconnect counter which is an 11-stage flip-flop, scale-of-2,048-counting circuit. This counter is similar to the angular position counter described in Part 2, Chapter 4. At the 2,048th pulse the disconnect counter circuit passes the selected CD 4 pulse to the CD read-write circuit where it stops the reading operation and produces a read-write-reset pulse. The read-write-reset pulse resets the counter and places FF 1 in the 0 state. With FF 1 in the 0 state, the selected CD 4 can not go through gate 2, unless AND 1 conducts to place FF 1 in the 1 state again. When AND 1 receives the necessary three levels to conduct, it will place FF 1 in the 1 state, thus starting the counting process again.

The deselect pulse generated by the Central Computer System at the start of a CD drum operation produces a read-write-reset pulse which clears all flip-flops in the disconnect counter. The CD 4 timing pulses from the selected drum timing circuit step the counter once every drum register at CD 4 time. At the end of 2,048 CD 4 timing pulses (one drum revolution), the counter produces a status-read-disconnect pulse. This pulse stops the CD status-controlled reading by clearing the CD read-write control circuit flip-flops. The CD read-write control circuit forms a drum-disconnect signal which notifies the Central Computer System to end drum operations. Thus, after reading begins, the status of every register of the selected field is examined once during a single revolution of the drum. The reading operation then stops until another operation is programmed by the Central Computer System.

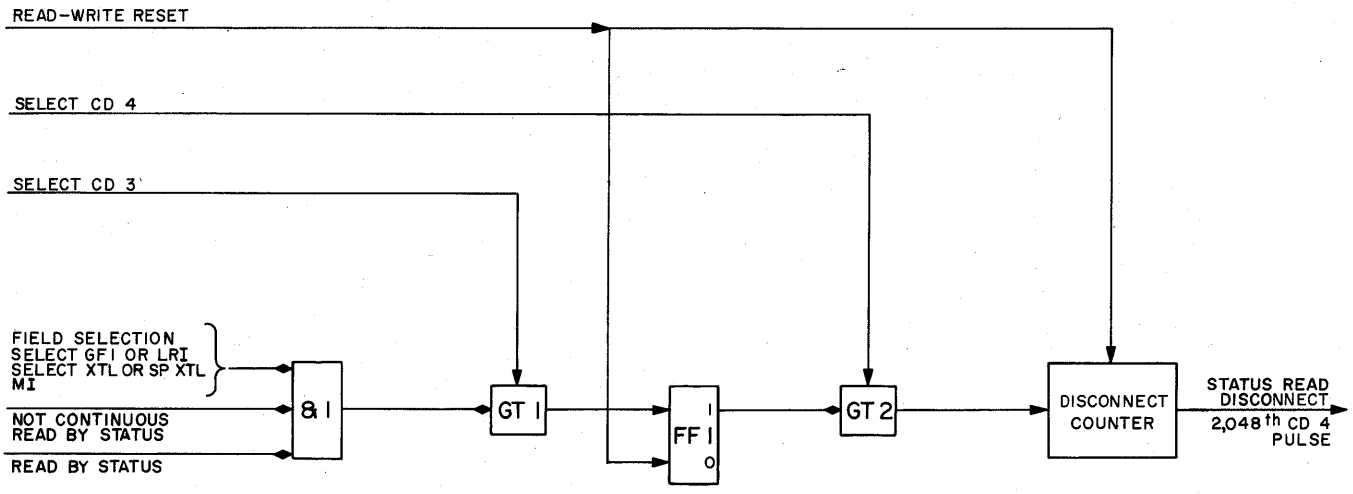


Figure 2—29. CD-Read-Status-Field-Disconnect Counter, Simplified Logic Diagram

5.4 GFI OD TRANSFER, CIRCUIT ANALYSIS

In the performance of certain Central Computer System functions, it is necessary to indicate the relative times at which separate portions of the data are received; for example, one computation that requires data-timing is the determination of target velocity. Since velocity is defined as the distance moved in a given period of time, it is necessary to be able to determine the time elapsed between different target-location samplings. Placing time information in each GFI word makes it possible to compute the time difference between the receipt of any two of these words. Timing data is written into bits L10 through L14 of the GFI word at the time the word is transferred onto the drum; for that reason the addition of timing data will be considered in conjunction with the data transfer process.

A block diagram of the OD circuits used to place data-timing information in words written on the GFI field is shown in figure 2–30.

The clock register in the Central Computer System develops relative-time-counter pulses and sync-relative-time-counter pulses, which go to the relative time-counter-step circuit. In the relative-time-counter-step circuit, these two series of pulses are synchronized with OD 4 pulses from the LOG timing circuit to produce step-relative-time-counter pulses and reset-relative-time-counter pulses, also at OD 4 time.

The two outputs of the relative-time-counter-step circuit go to the relative time counter. Each relative-time-counter-step pulse steps the counter. The output of the counter, therefore, represents the number of relative-time-counter-step pulses that have been counted.

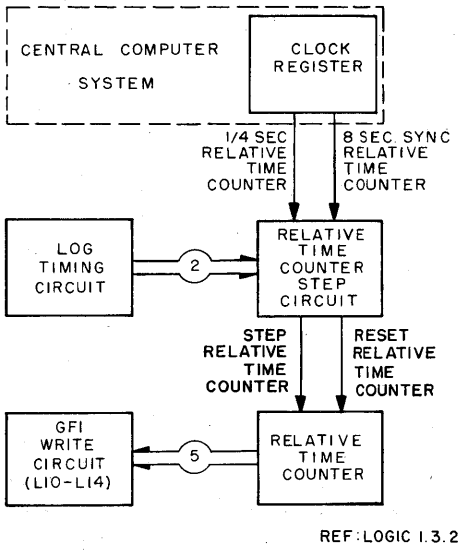


Figure 2–30. Gap-Filler Input Data Timing, Block Diagram

This output is sent to the OD write circuit of the GFI field, filling bits L10 through L14.

Since the maximum output of the counter, 31, can be expressed in five bits, the largest number of step pulses that can be counted is the binary number which is represented by all of the five flip-flops being in the 1 state. Once each 8 seconds, at the time which would correspond to the 32nd step pulse, the reset-relative-time-counter pulse is developed. This pulse clears the counter flip-flops. If all the counter flip-flops are not set at the time the reset-relative-time-counter pulse is received, an error indication is developed.

In the production of timing data for the GFI field, the clock register of the Central Computer System develops two sets of timing pulses. One set consists of relative-time-counter pulses, with a ¼-second recurrence rate. The other set, known as the sync-relative-time-counter pulses, occur once every 8 seconds. Both types go to the GFI relative-time-counter-step circuit. (See fig. 2–31.)

The relative-time-counter pulses set FF 1. The output level of FF 1 conditions gate 1 to pass OD 1 pulses from the LOG timing circuit. The gate output sets FF 2. The resulting d-c level at the output of FF 2 provides one of two levels necessary to produce conduction in AND 1 and 2.

Assuming that FF 3 is in the 0 state, AND 1 conducts, conditioning GT 2 to pass OD 4 pulses. The gated OD 4 pulses form step-relative-time-counter pulses which go to the relative-time counter and OR 1. Conduction in OR 1 clears FF's 1 and 2.

At the end of 8 seconds, the sync-relative-time-counter pulse is sent to the relative-time-counter-step circuit, at the same time as the relative-time-counter pulse. As before, the relative-time-counter pulse establishes a d-c level in AND's 1 and 2. However, the sync-relative-time-counter pulse sets FF 3. AND 2 conducts while AND 1 cannot conduct. Gate 3 is conditioned to pass an OD 4 pulse forming a reset-relative-time pulse. Since AND 1 does not conduct, GT 2 is not conditioned and the 32nd consecutive step-relative-time-counter pulse is not generated. The reset-relative-time-counter pulse goes to the relative time counter, OR 1, and clears FF 3. Conduction in OR 1 again clears FF's 1 and 2.

The relative-time-counter-step circuit, therefore, produces 31 step-relative-time-counter pulses, then one reset-relative-time-counter pulse, then another 31 step pulses, etc.

The relative time counter, shown in figure 2–32, counts the step-relative-time-counter pulses. It is cleared by the reset-relative-time-counter pulse. The FF 1 output (1 or 0 d-c level) represents the lowest order digit of a binary number; the FF 2 output represents the second digit of the binary number; etc. The complete num-

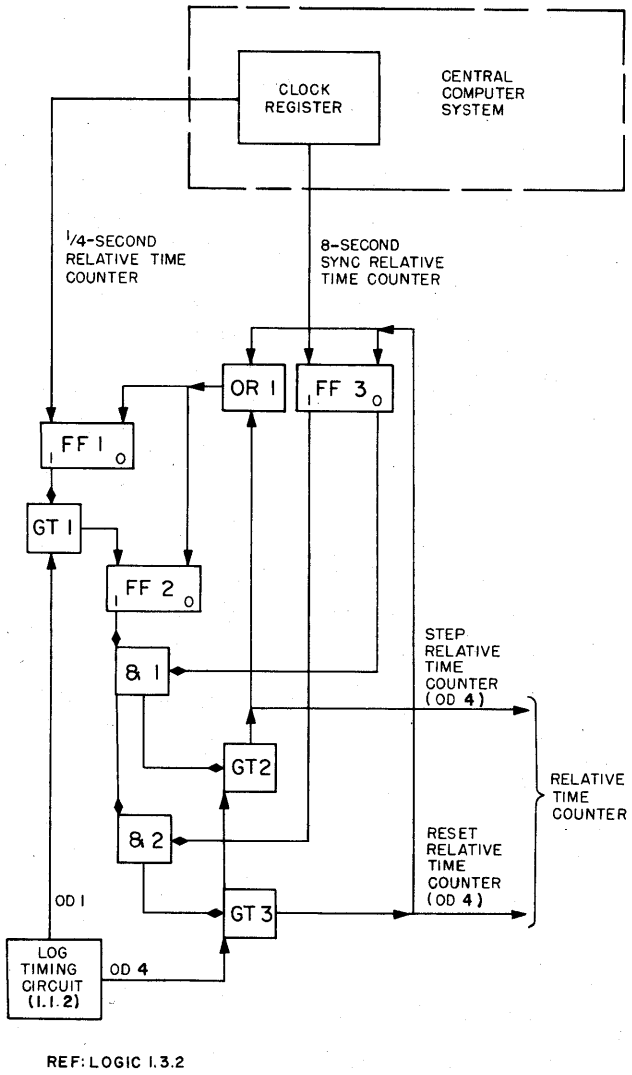


Figure 2–31. Relative Time Counter Step Circuit, Simplified Logic Diagram

ber of step pulses counted is 31. Refer to Part 2, Paragraph 4.4.1, for a discussion of counter circuit operation.

The reset-relative-time-counter pulse serves as a check on the counter. If an error in counting occurred, one or more of the counter flip-flops will provide a 0 output at the time of the reset-relative-time-counter pulse. The 0 output of the flip-flop(s) causes conduction in OR 1, which conditions GT 5 to pass the reset-relative-time-counter pulse as a relative-time-error pulse. The relative-time-error pulse causes an error indication at the maintenance panel.

The flip-flops of the relative time counter form a part of the GFI write register. The d-c levels at the output of the counter go to the GFI OD drum writers. Each time the gap-filler-status-control circuit develops a write-sample pulse (5.2) the output of the relative time counter is written on the drum as part of the GFI word.

With the exception of the addition of data-timing information, the GFI field is written in the same way as the MI field. The detailed discussion of the OD writing operation is described in 5.2.

5.5 GFI CD TRANSFER

Transfer of GFI data from the drums to the Central Computer is performed in the same manner for the GFI field as it is for the MI field. This transfer was described in detail in 5.3.

5.6 LRI OD TRANSFER, CIRCUIT ANALYSIS

An LRI message consists of two words. By a modification of the basic method of data transfer, an LRI message is written onto two consecutive registers with the first word of each message written in an odd-numbered register. The two registers which contain one complete message are read consecutively on the CD side of the drum. The group of two registers which contain the message is termed a slot.

Figure 2–33 illustrates a part of the circuits which control the writing of LRI messages. The word-demand pulse is an OD 3 pulse which is passed by gate 2 when FF 1 has been cleared by an OD 4 pulse and not set by the OD 1 pulse. This condition will exist when a 0 is read in the OD status channel.

Gate 3, which must be conditioned to pass the OD 3 or word-demand pulse, is controlled by the LRI slot counter, FF 2. AND 1 conducts when the Drum System is in the operate mode and when FF 2 is in the 1 state. The LRI slot counter flip-flop (FF 2), is complemented by each OD 1 pulse. Therefore, GT 3 will alternate between the conditions of conduction and non-conduction, and will remain in each condition for a period of 10 usec. Gate 3 will consequently block OD 3 pulses during alternate registers. Hence, the LRI status control circuit generates a word-demand pulse for each two consecutive vacant registers rather than for each vacant register as is done in basic-status control.

Once each drum revolution, the LRI slot counter is triggered by the LOG-IX pulse to insure that it is in the correct position to place the first word of each subsequent message in an odd-numbered register.

If the Input System contains an LRI message, its response to the LRI word-demand pulse is two data-available pulses, the second separated from the first by 10 usec. The two data-available pulses cause the message to be written on two adjacent registers and cause the complete message to be written in response to one word-demand pulse.

The two deviations from basic-status control necessary to write the LRI fields involve the generation of a word-demand pulse at every other OD 3 time (when the OD status channel indicates a slot available) and the Input System response of two data-available pulses.

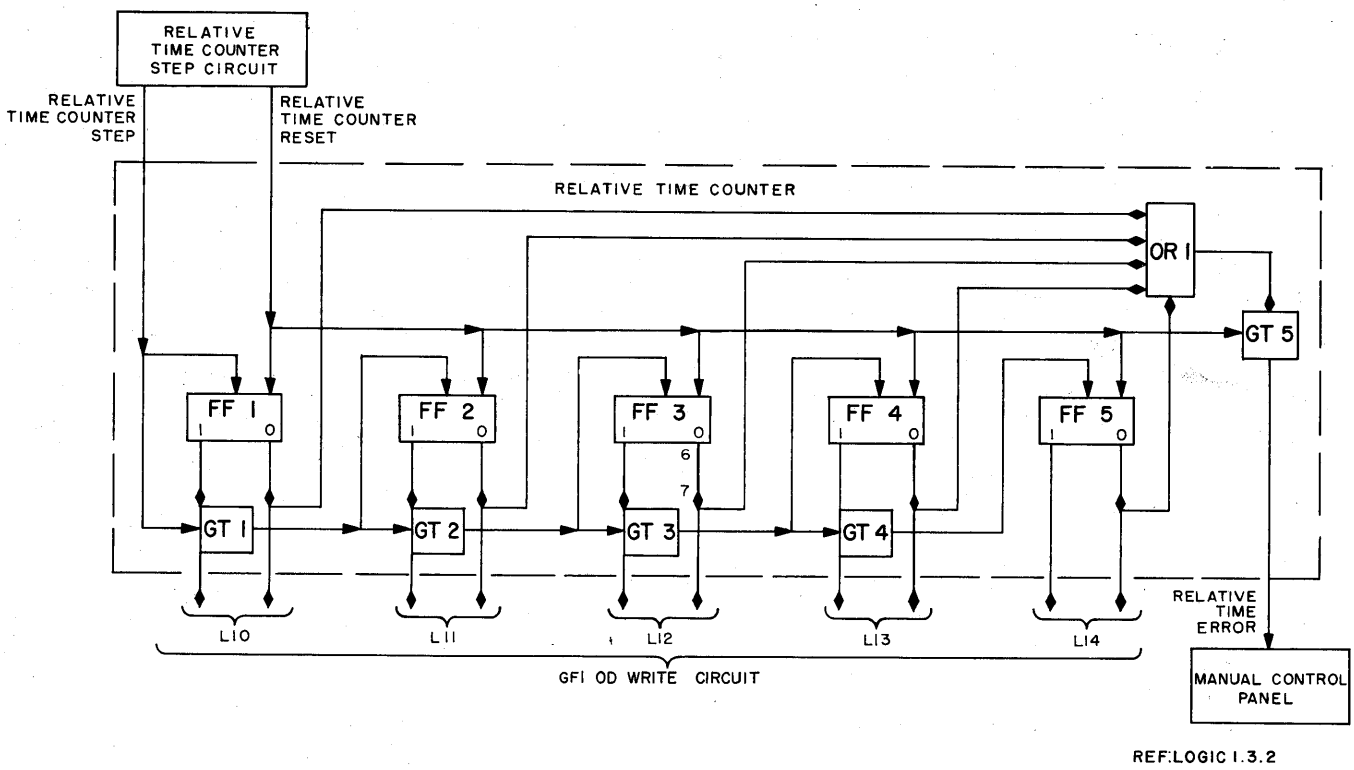


Figure 2–32. Relative Time Counter, Simplified Logic Diagram

LRI data is written in two fields, LRI 1 and LRI 2. The LRI slot counter is common to both fields, but GT 3 and the power amplifier are duplicated in the status control circuits of the two fields. Hence, the two word-demand pulses, occur simultaneously if both fields indicate an available slot. In this event, the Input System transfers the message of LRI field 1.

5.7 LRI CD TRANSFER, CIRCUIT ANALYSIS

LRI messages consist of two words which are written into consecutive registers with the first word of each message written in an odd-numbered register. For this reason, it is necessary to modify the basic data transfer procedure on the CD side of the LRI fields to assure that reading of a message is begun on the odd-numbered registers and to insure that all LRI messages are read in their entirety.

This modification is effected by the use of two single-stage counters, the LRI CD slot counter and the LRI status slot counter. The LRI CD slot counter assures that reading of full slots is begun on odd numbered registers. The LRI status slot counter establishes the register (the first odd register after arrival of the read-by-status level) at which stepping of the CD read status disconnect counter begins. This stepping is necessary to insure that the disconnect pulse will not be developed in the middle of a message.

Transfer of information from full registers of the LRI field to the Central Computer is initiated on odd-numbered registers only, due to the action of the LRI CD slot counter. This counter prevents generation of compare pulses during the reading of even registers. (Receipt of a compare pulse by the Central Computer is necessary for the acceptance by the Central Computer of a Drum System message.) The operation of the LRI CD slot counter is shown on figure 2–34. The LRI CD slot counter flip-flop (FF 2) controls conduction in AND 2, provided AND 1 conducts. AND 1 conducts when the read by status and select LRI levels are present. The d-c inverter causes GT 2 to pass the compare pulse when AND 2 does not conduct. Since the flip-flop of the LRI CD slot counter is complemented by the CD 3 pulse, the compare pulse can be generated on every other register. The LOG-CD-IX pulse insures that the compare pulse will coincide with the reading of an odd-numbered register.

The compare pulse is sent to the Central Computer System to request comparison of the identification bits of the first word of the LRI message with identification bits in the Central Computer System. If the comparison is successful and the word is accepted by the Central Computer System, both words are transferred from the drum and the no-compare pulse is not transmitted. Zero bits are then written into the OD status control channel. If the first word is rejected by the Central Com-

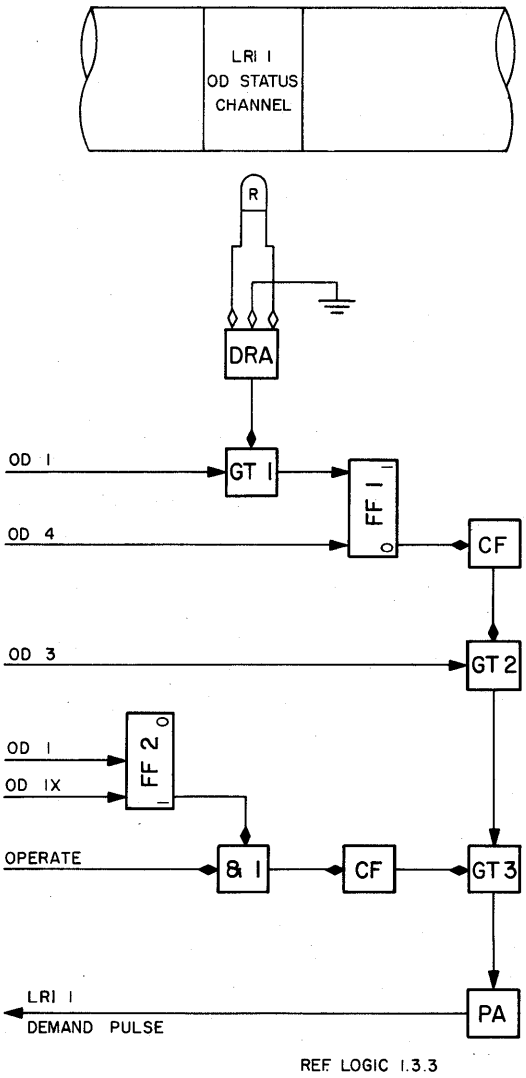


Figure 2–33. LRI OD Slot Counter, Simplified Logic Diagram

puter System, a no-compare pulse is returned for each of the two words, and 1 bits are written into the OD status channel, as illustrated in figure 2–34.

In order to assure that all LRI messages will be read in their entirety prior to the development of the status disconnect pulse, it is necessary that the stepping of the CD read status counter begin with an odd register. This assurance is effected by the LRI status slot counter shown on figure 2–35.

The LRI status slot counter controls the admission of the first CD 4 stepping pulse to the field disconnect counter by providing one of the necessary levels to cause conduction in GT 1, which allows the CD 3 pulse to set FF 2 and to cause conduction in GT 2. The status slot counter flip-flop is complemented by the CD 3 pulse and consequently alternates between the 0 and 1 output at 10-usec intervals. Therefore, when the select LRI level is present, AND circuit 1 alternates between conduction and nonconduction and remains in each condition for 10 usec. Counting can begin on every other register. It begins with the reading of an odd-numbered register and discontinues the reading operation after the reading of an even-numbered register. Compare pulse to coincide with the reading of an odd-numbered register and discontinues the reading operation after the reading of an even-numbered register. The CD-IX pulse triggers the status slot counter once each drum revolution to insure synchronization between the drum registers and the status slot counter.

The deviations from status-identification control necessary to read the LRI fields are the generation of the compare pulse to coincide with the reading of an odd-numbered register only and the initiation of counting in the status-disconnect counter to cause reading to discontinue after the reading of an even-numbered register.

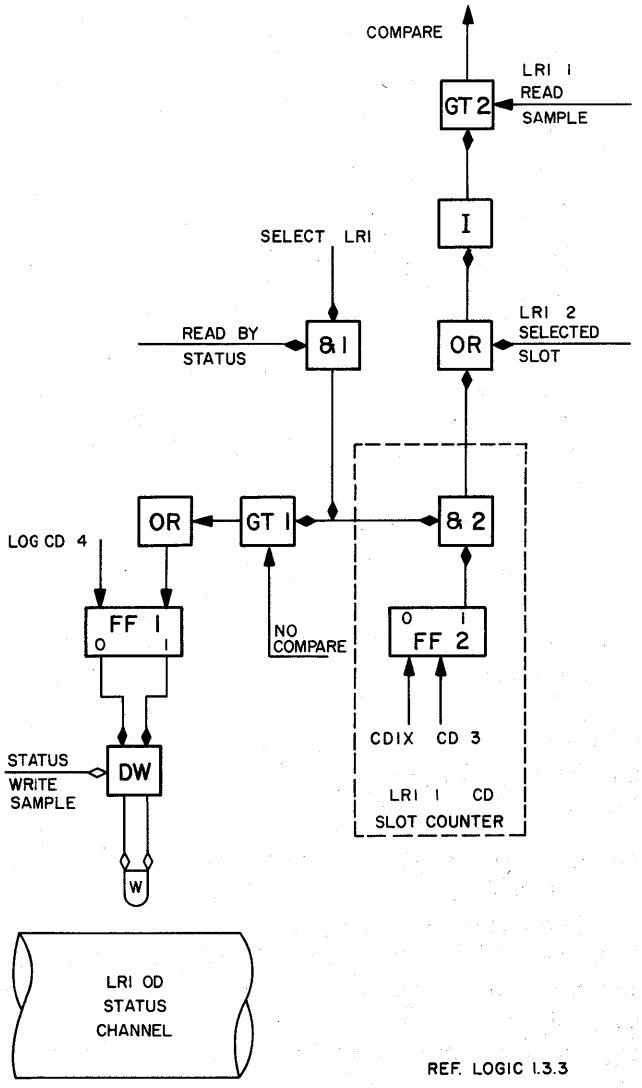


Figure 2–34. LRI CD Slot Counter and Associated Circuits, Simplified Logic Diagram

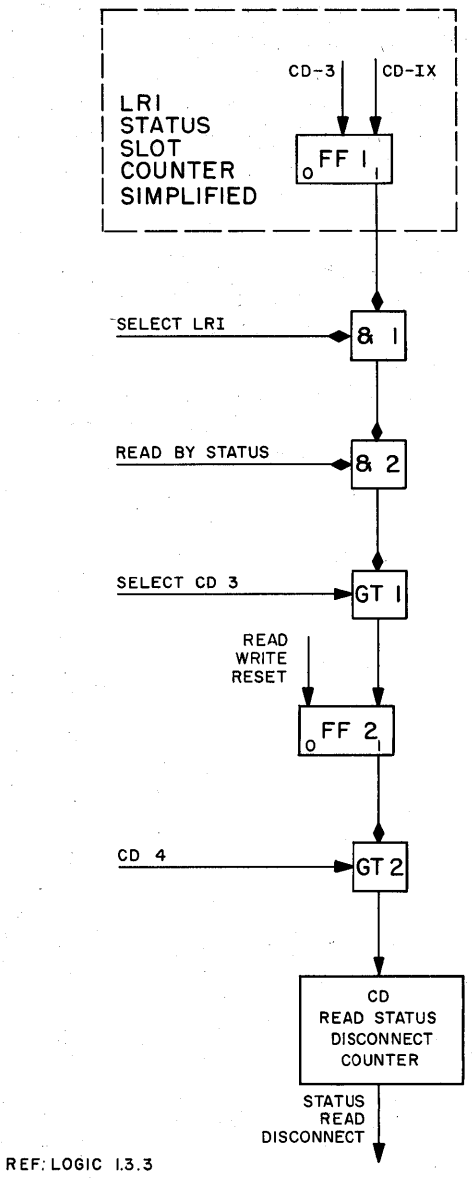


Figure 2–35. LRI Status Slot Counter and Associated Circuits, Simplified Logic Diagram

In other respects, the LRI fields are read similarly to the MI field (the reading of which was described in 5.3).

5.8 XTL OD TRANSFER, BLOCK DIAGRAM ANALYSIS

Information from the XTL input element, like that from the GFI and LRI elements, is of a random nature and has a repetition rate different from that of the Drum System timing cycle. However, since XTL messages consist of three words each, it is necessary to modify normal status control of the OD-writing operation. The modification employed to write XTL data is known as marker status control.

Crosstelling information is written on the XTL field of the MIXD drum. A spare field on the MIXD drum can also be utilized as an XTL field if certain wiring changes are made. The spare crosstelling field is designated SP XTL.

Examination of figure 2–36 reveals that the only difference at the block diagram level between the XTL fields and other fields lies in the addition of a marker status channel on the former. The marker channel is written at the start of drum operations under the control of the Central Computer which designates where in the channel the 1 bits, called markers, are to be placed. The markers in the channel indicate to the OD Input System the drum registers in which the first word of the 3-word XTL messages are to be written. The remaining two words are placed in the two registers immediately following the register associated with the marker.

As the drum rotates, the read heads on the XTL marker and OD status channels read continuously. If a 0 is read in the OD status channel in the same register that a marker (1 bit) is read in the marker status channel, the marker-status-control circuit produces a drum-demand pulse. The drum-demand pulse goes to the Input System and searches for an XTL message. If a message is found, three consecutive data-available pulses are returned to the XTL marker-status-control circuit at 10-usec intervals. The transfer of each of the data-available pulses is coincident with the transfer of a word to the XTL OD write circuit.

Data-available pulses cause the word in the write circuit to be written on the drum during the period of the write-sample pulse from the timing circuit. The data-available pulses also cause the writing of 1's in the

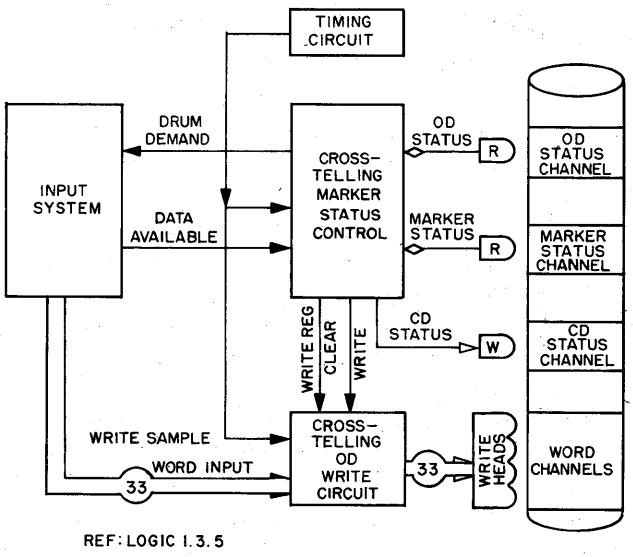


Figure 2–36. Marker Status Modification of Status Control, Block Diagram

OD status channel. After each word is written in the information channel, the XTL marker-status-control circuit produces a write-register-clear pulse. This pulse clears the register's flip-flops in the write circuit, preparing them for the next word.

As in normal status-controlled circuits, the XTL and SP XTL marker status operations are synchronized by timing pulses from the drum-timing circuit.

5.8.1 Marker Status Control, Circuit Analysis

The XTL (or SP XTL) marker-status controlled writing operation is almost identical with normal status control. The major difference between the two operations exists in the techniques employed to produce the drum-demand pulse, and in the subsequent response from the Input System.

The OD marker-status-control circuits are shown in figure 2–37. The writing procedure begins with the detection of a 0 in the OD status channel. This prevents gate 1 from passing the OD 1 pulse and the 0 state of FF 1 is maintained. The output of FF 1 conditions AND 01. In order to complete the requirements for conduction in AND 01, a 1 output level from FF 01 must also be present. This 1 level is produced by passing an OD 1 pulse from the MIXD timing circuit in GT 01. Gate 01 is conditioned to pass the OD 1 pulse only for those registers that have 1 bits in the corresponding areas in the XTL marker status channel.

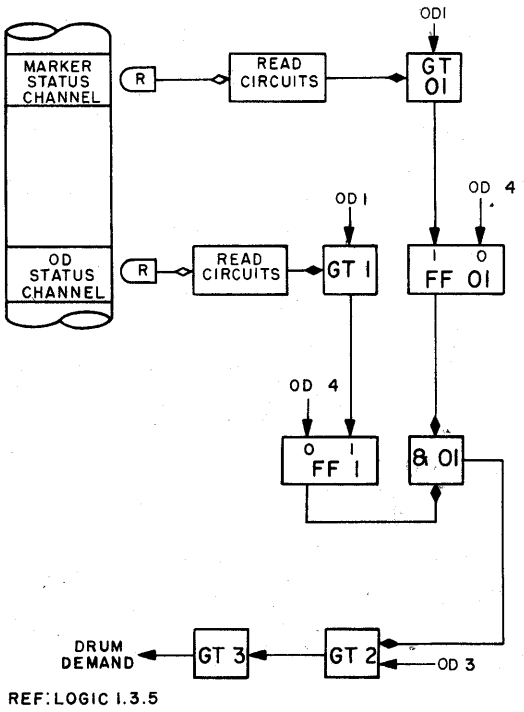


Figure 2–37. Marker-Status-Modification-of Status-Control Circuit, Simplified Logic Diagram

With inputs resulting from both a 1 in the marker status channel and a 0 in the OD status channel, AND 01 conducts, establishing a d-c level at GT 2. Gate 2 passes the next OD 3 pulse to GT 3. The GT 3 output is a drum-demand pulse. Immediately after the production of the drum-demand pulse, an OD 4 timing pulse from the MIXD timing circuit clears FF 01 in the marker-status-control circuit. No more drum-demand pulses are formed until the beginning of the next slot which finds a coincidence of a 1 in the marker channel and a 0 in the OD status channel.

The results of the receipt of an XTL drum-demand pulse in the Input System differ from the result obtained from a drum-demand pulse from fields controlled by normal status. The XTL drum-demand pulse does not search for a single-word, but for a 3-word message. When the message is found, three data-available pulses are returned to the XTL OD marker-status-control circuit. These pulses are 10 usec apart. They coincide with the transmission of three words into the write register of the OD write circuit.

As in normal status control, the receipt of each data-available pulse causes the word placed in the write register to be written at the next OD 3 time. The three words are written in three consecutive drum registers on the XTL field.

The XTL and SP XTL status modification of normal status control duplicates the effect of having a normal-status-control circuit detect three consecutive 0's in the OD status channel and that of having three words available at the time the resulting word-demand pulses are sent to the Input System.

5.8.2 Writing Marker-Status Channel, Circuit Analysis

To indicate the first word of each XTL (or SP XTL) field slot, a 1 bit is written in the marker channel.

When the select-XTL-marker level is sent to the marker-channel-write circuit, shown in figure 2–38,

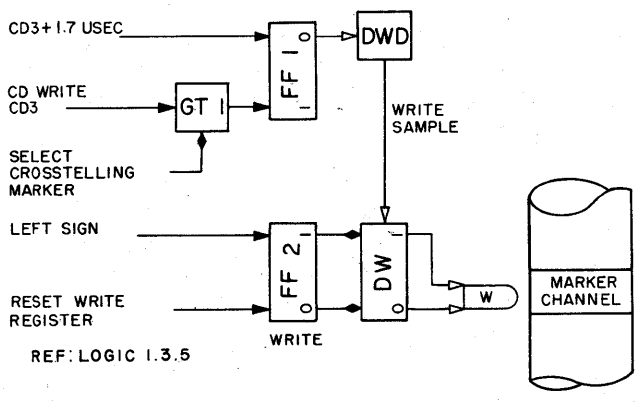


Figure 2–38. Crosstelling-Marker-Channel-Write Circuit, Simplified Logic Diagram

from the CD selection encoder circuits, GT 1 is conditioned to pass a CD write pulse (at CD 3 time) from the CD read-write control circuit. This CD write pulse sets FF 1. As a result, the flip-flop 0-state level is removed from the drum write driver. The drum write driver output becomes positive since the driver acts as an inverter. At CD 3 time +1.7 usec a CD 3 + 1.7 usec pulse from the MIXD drum-timing circuit clears FF 1 and restores the flip-flop 0-state level at the drum write driver, thus driving its output negative again. As a result, a positive write-sample pulse of 1.7-usec duration is applied to the drum writer, which causes the drum writer to write the contents of FF 2 on the marker-status channel. A left-sign pulse from the Central Computer System sets FF 2, causing the drum writer to write a 1 in the marker channel when the write-sample pulse occurs at CD 3 time. At CD 4 time, the write-register-reset pulse from the CD write circuit clears FF 2. Between the receipt of left-sign pulses, 0 bits are written in the marker channel. The registers of the drum on which the left sign causes a 1 marker to be written on the marker-status channel are controlled by Central Computer System programming. This is done by address control as described in Chapter 4. Writing in the marker-status channel is stopped by the disconnect counter (5.3) after one revolution of the MIXD drum.

5.9 XTL CD TRANSFER, CIRCUIT ANALYSIS

A simplified logic diagram of the marker-status-read-control circuit is shown in figure 2–39. Note that this circuit is identical to that for MI CD status control shown in figure 2–28 except for the addition of the marker status channel and GT 5. The operation of this circuit is identical to the operation of the MI CD status control circuit except that a compare pulse is generated only when the first word of a message is read.

When a 1 bit is read on the marker-status channel (during the reading of the first word of a message), read circuit 2 conditions GT 5. The read-sample pulse is passed through GT 5 as a compare pulse. Only one compare pulse is generated for each message. The compare pulse is sent to the Central Computer System to request comparison of the identification bits of the first word of the XTL message with identification bits in the Central Computer System.

If comparison is unsuccessful, a no-compare pulse is sent from the Central Computer System to the Drum System for each word of the message and the words are

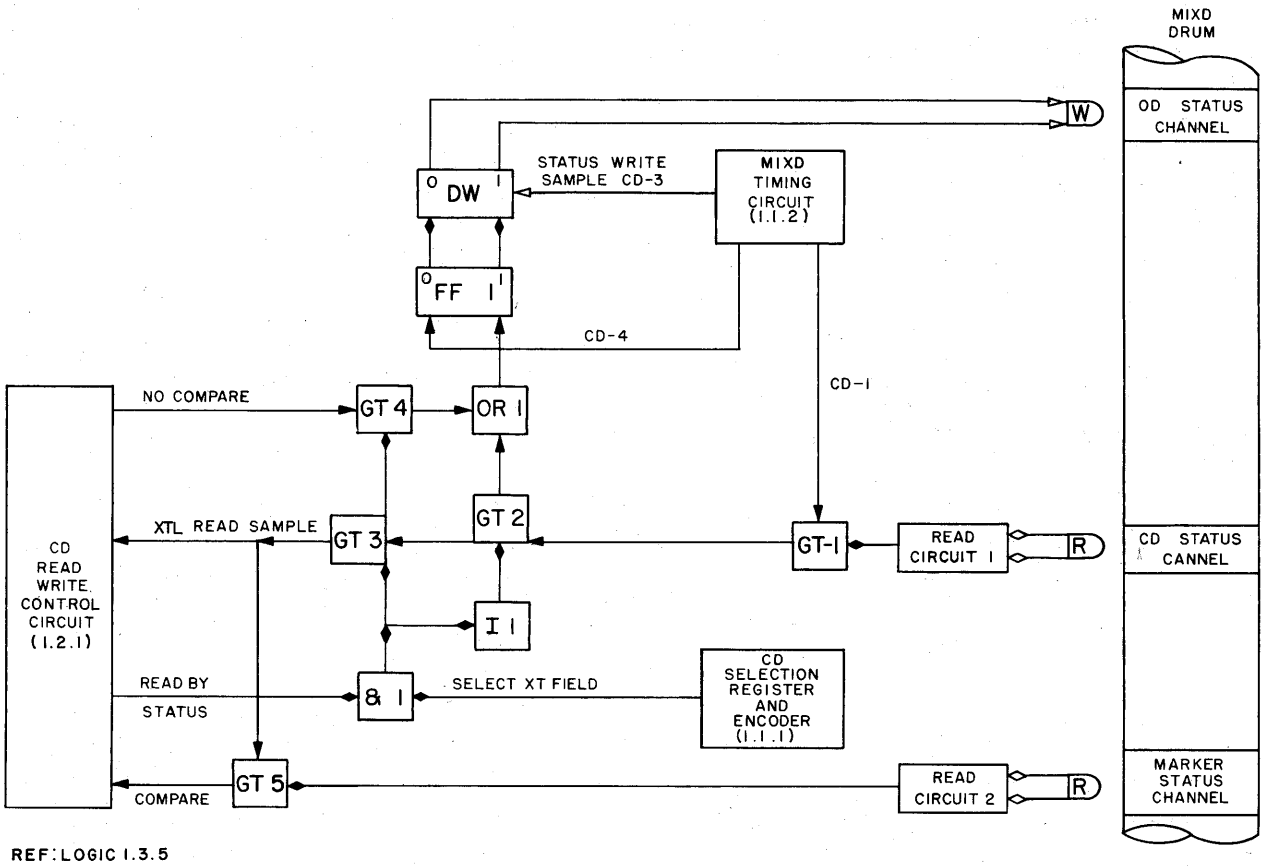


Figure 2–39. CD Marker-Status-Controlled XTL Field Reading, Simplified Logic Diagram

cleared from the IO buffer register. When a successful comparison is made in the Central Computer System, the message is accepted and the no-compare pulses are not sent to the Drum System.

The disconnect counter (5.3) stops operations after one revolution of the drum containing the XTL fields. The operation of the SP XTL field, when it is connected as such, is identical to that of the XTL field.

CHAPTER 6

OUTPUT BUFFER FIELDS DATA TRANSFER

The Central Computer System develops large quantities of tactical data for transfer to the Output System. This information is written on the three OB fields of the LOG drum. Since the Output System cannot process information at the rate it is developed by the Central Computer System, the rate of writing on the OB fields is reduced. Information from the Central Computer System is written on the odd or even registers of the output buffer fields by status control. Writing on every alternate register (odd or even) effectively reduces the rate of writing since only one-half of the available registers are written on during one complete drum revolution.

Data is transferred from the Drum System to the Output System by the OB OD circuits. The OB OD circuits read the information on the OB fields by status identification control. Since consecutive words are written in alternate registers, the speed of reading is effectively slowed to one-half the normal rate. This is true even though all drum registers of the three OB fields are inspected during the OD reading operation. Status identification control reading further enables the Output System to make selective acceptance of transferred information, so that only that data which is pertinent to Output System operation at a given time is taken from the drums.

Individual OB fields are not selected by the Central Computer System. Selection of either odd or even registers of the fields is the only choice available. The Central Computer System thus sees the three OB fields as one large continuous field. These fields are switched consecutively by means of the OB-CD field selector counter. After switching, there is a 120-usec delay before the start of writing on the next field. This delay permits decay of switching transients. When all of the odd or even registers (whichever have been selected) of the three OB fields have been inspected, an OB-disconnect pulse is generated which stops the writing operation.

Reading of the OB register is performed without distinguishing even or odd registers. The word identification circuits in the Output System determines whether the contents of a particular register are accepted. The OD reading of the three OB fields is done sequentially. Fields are switched for reading by means of the OB OD field switch circuits. After switching there is a 120-usec delay before the start of reading on the new field, to permit decay of switching transients.

6.1 OB FIELDS AND CD WRITING, BLOCK DIAGRAM ANALYSIS

The flow of data and control signals for CD status-controlled writing on the OB fields is shown in figure 2–40. CD writing on the OB fields is done by status control but only on alternate registers (odd or even). The status control circuit finds an empty register, but writing will not take place unless the register is odd or even depending on the mode selected by the Central Computer.

The writing operation begins with the selection of the OB odd or even registers by the Central Computer System followed by a start-write and an IO-buffer-to-write-register pulse. The CD read-write-control circuit then produces the write-by-status level as described in Chapter 4. Selection of OB odd or even registers by the Central Computer System causes the CD selection-register-and-selection encoder to set up either an OB-odd or an OB-even d-c level. The selected level and the write-by-status level go to the OB CD register-switch-control circuit where they are combined with the OB-operate level from the OB CD gap counter and the output of the OB CD field switch to produce a write-selected-OB-field level. This level is applied to one of the OB CD status-control circuits which controls writing on the selected field. The OB CD field-switch circuit generates a select-OB-field level which is applied to the drum field drivers to energize the heads of the selected OB field.

When the three OB fields have been inspected once, an OB-disconnect pulse is generated by the OB disconnect counter in the OB CD field-switch-control circuit and is applied to the CD read-write-control circuit. The CD read-write-control circuit converts the OB-disconnect pulse to a read-write-reset pulse which clears the flip-flops in both the CD read-write-control circuit and the CD write circuit, thus ending the writing operation.

The OB-disconnect pulse also serves as a drum-disconnect pulse which informs the Central Computer System to stop the transfer of words to the OB fields.

6.2 OB FIELDS CD SWITCHING

Writing of the three OB fields is accomplished by a modified form of status control which causes writing in the odd or even registers of these fields. The Central Computer System does not select the individual OB

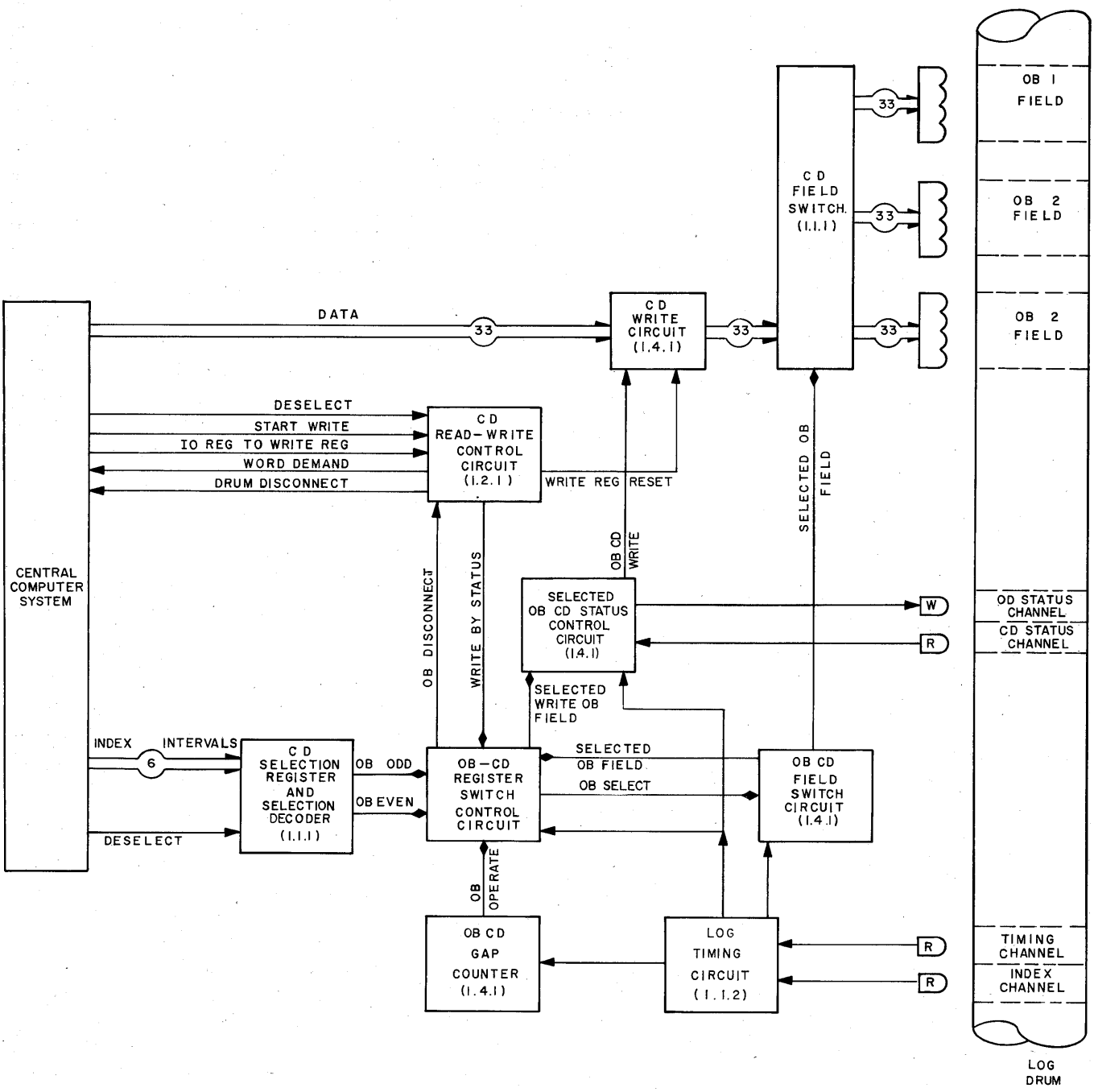


Figure 2–40. OB Fields CD Writing, Block Diagram

fields where writing is to take place. Switching is performed by the OB CD field-switch circuits. A delay is provided between OB field-switching and the start of writing in the new field by the OB CD gap counter. This time interval permits the decay of switching transients in the write heads. All three fields are switched in consecutive order and the three fields appear as one large field to the Central Computer System. When all three fields have been inspected once, an OB-disconnect pulse is generated, causing the writing operation to stop. The following analysis describes the functions of the circuits involved in switching.

6.2.1 OB CD Field-Switch-Control Circuitry

The OB-CD field switching is accomplished by the OB-CD field-switch control circuit (fig. 2–41) as follows.

When power is applied to the Drum System, a power-on-reset pulse sets FF 1 and clears FF 2. The 0-state output of FF 2 and the select-OB level causes

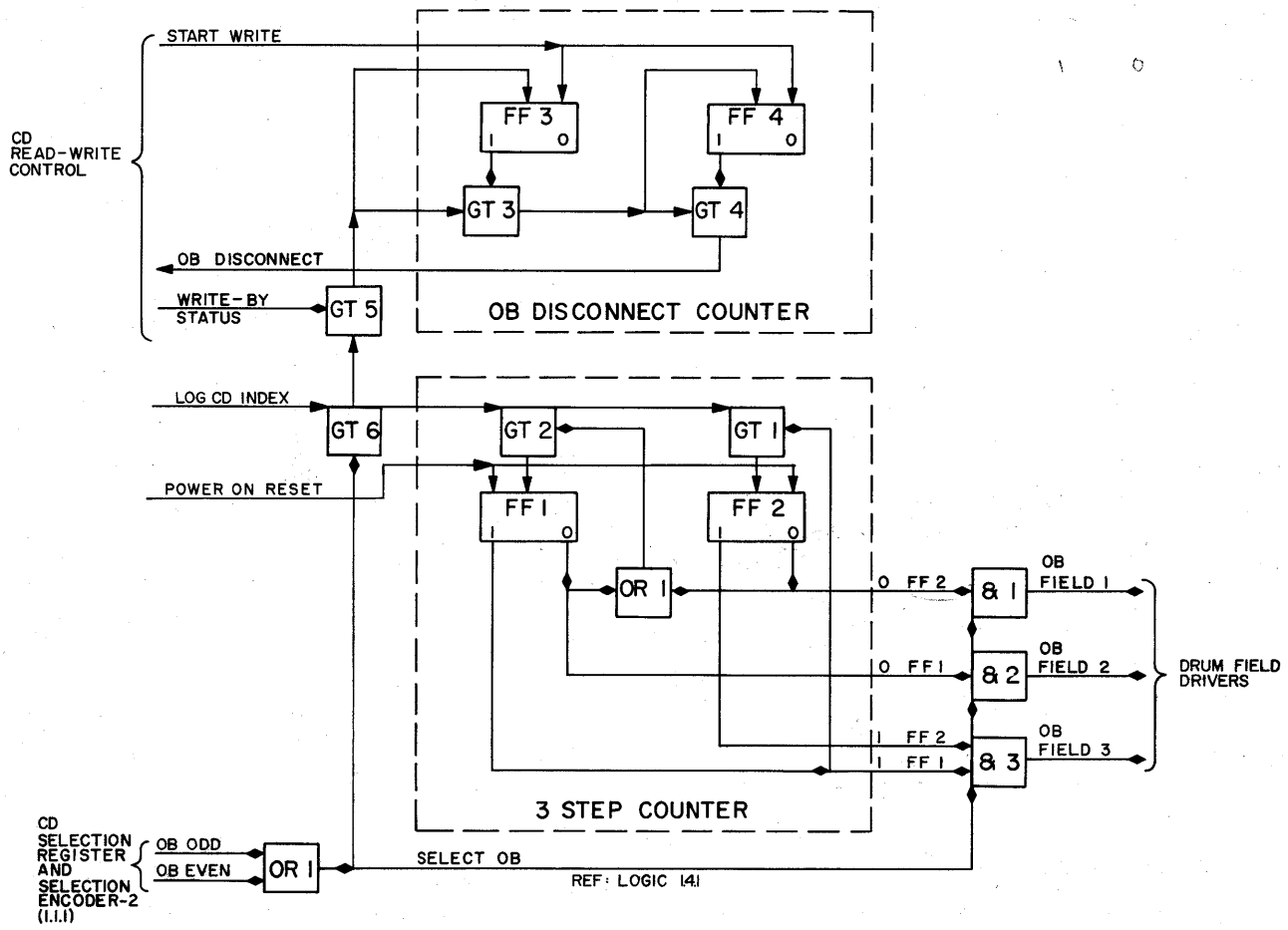


Figure 2–41. OB CD Field Switch Control Circuit, Simplified Logic Diagram

AND 1 to conduct. The output of AND 1 is the OB-select-field-1 level.

The 0-state output of FF 2 conditions GT 2 via OR 1; the 1-state output of FF 1 conditions GT 1. Gates 1 and 2 are now conditioned to pass a CD-index pulse from the LOG drum index channel. This causes FF's 1 and 2 to be complemented. Flip-flop 2 is changed to the 1 state and FF 1 to the 0 state. AND 1 is cut off. The 0-state output of FF 1 conditions AND 2 to produce the OB-field-2 level. Gate 2 remains conditioned by the 0-state output of FF 1 via OR 1.

The next CD-index pulse is passed by gate 2 to complement FF 1. Flip-flop 1 is now in the 1 state, causing AND 2 to be cut off. Flip-flops 1 and 2 are both in the 1 state, causing AND 3 to conduct, producing the OB-field-3 level. The 1 state of FF 1 conditions GT 1.

The next CD-index pulse is passed by gate 1 to complement FF 2. Flip-flop 2 is now in the 0 state, causing AND 3 to be cut off. The 0-state output of FF 2 causes AND 1 to conduct, producing the OB-select-field-1 level, the original condition.

In this manner, OB fields are automatically switched in sequence (1, 2, 3, 1, 2, 3, etc.). The flip-flop states occurring in this circuit are listed in table 2–1.

It should be noted that at no time during normal operation can both flip-flops be cleared and that one of the AND's will conduct whenever the OB fields are selected for writing.

The output of AND 1, 2, or 3 (whichever is conducting) goes to the CD-field switch and prepares the selected field drum heads to write.

TABLE 2–1. CONDITIONING LEVEL FOR OUTPUT BUFFER FIELD SWITCHING

FLIP-FLOP 1	FLIP-FLOP 2	OUTPUT LEVEL
1	0	OB 1
0	1	OB 2
1	1	OB 3
1	0	OB 1

The CD-index pulses are also counted by the OB-disconnect counter (fig. 2–41), which is a standard, 2-stage, scale-of-3 counter circuit. At the fourth CD-index pulse passed by GT 5, the status of all registers of the three OB fields will have been inspected once. The fourth CD-index pulse causes the OB disconnect counter to produce an OB-disconnect pulse. The OB-disconnect pulse goes to the CD read-write-control circuit to end the writing operation.

The OB CD gap counter provides the 120-usec delay necessary between OB field-switching and the start of writing in the new OB field.

The gap counter is a 4-stage, scale-of-12 counter circuit (fig. 2–42). A CD-index pulse from the LOG drum clears FF's 1 to 4. The 0-state level of FF 3 or 4 via OR 1 conditions GT 1 to pass CD-4 pulses from the LOG drum. At the 12th CD-4 pulse, FF's 3 and 4 will be in the 1 state. The 1-state levels of FF's 3 and 4 cause AND 1 to conduct, producing the CD-OB-operate level. The CD-OB-operate level goes to the OB CD field-switch-control circuit as a necessary condition for the writing operation. Also, since FF's 3 and 4 are both in the 1 state, the conditioning level is removed from GT 1. Gate 1 will not conduct until the next CD-index pulse clears FF's 1 to 4, initiating a new delay cycle.

6.2.2 OB CD Register Switch Control Circuitry, Function and Description

The OD CD register switch control circuit (fig. 2–43) provides the d-c levels required by the selected status control circuit to cause writing on either the odd or even registers of the OB fields as selected.

CD-4 timing pulses complement FF 1 continuously from the 0-state to the 1 state and back. Coincidence of the 0-state level of FF 1 and the OB-even level from the CD-selection-register-and-selection encoder produces an output level at AND 2. Similarly, the 1-state level of FF 1 and the OB-odd level produce an output at AND 2. The function of the CD-index pulse (at CD-1 time) is to make certain that the previous CD 4 pulse has brought FF 1 to the 0 state. The index pulse, therefore, acts as a check on the even or odd operations, and assures that the first CD-4 pulse at the beginning of every drum revolution places FF 1 in the 1 state.

As a result of the action described above, AND 2 conducts for even registers, and AND 1 conducts for odd registers when the respective selection levels are present. Thus, an output is obtained from one of these AND's every other register. There is an interval of 20 usec between the consecutive outputs from the selected AND.

The outputs of AND's 1 and 2 go to OR 1. The resulting condition of OR 1 produces an output level which is sent to AND's 3, 4, and 5. Thus, one condition for energizing AND's 3, 4, and 5 is the output described above, which is present every other register. Determination of which AND (3, 4, or 5) is to conduct is accomplished by output levels from the 3-step counter described in 6.2.1.

The CD read-write-control circuit sends a write-by-status level to be used as one of the necessary input levels to AND's 3, 4, and 5.

The CD-OB-operate level, which feeds AND's 3, 4, and 5, comes from the OB CD field switch gap counter. This level is the last necessary condition for conduction in these AND's. The output of the selected AND's (3, 4, or 5) is the write-OB-field level which enables the selected status control circuit to start writing operations on the selected field.

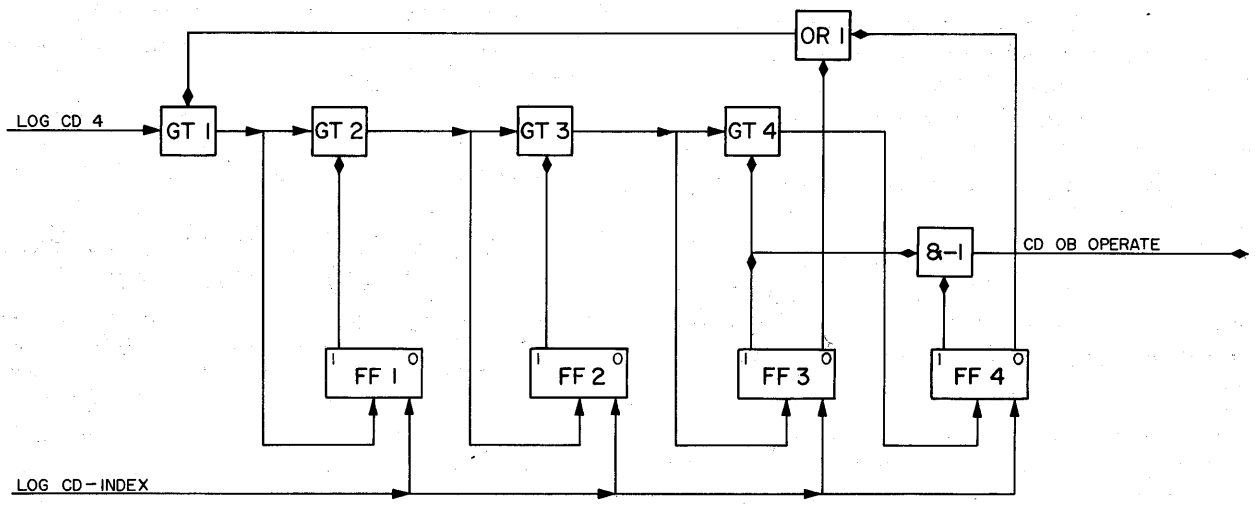


Figure 2–42. OB CD Gap Counter, Simplified Logic Diagram

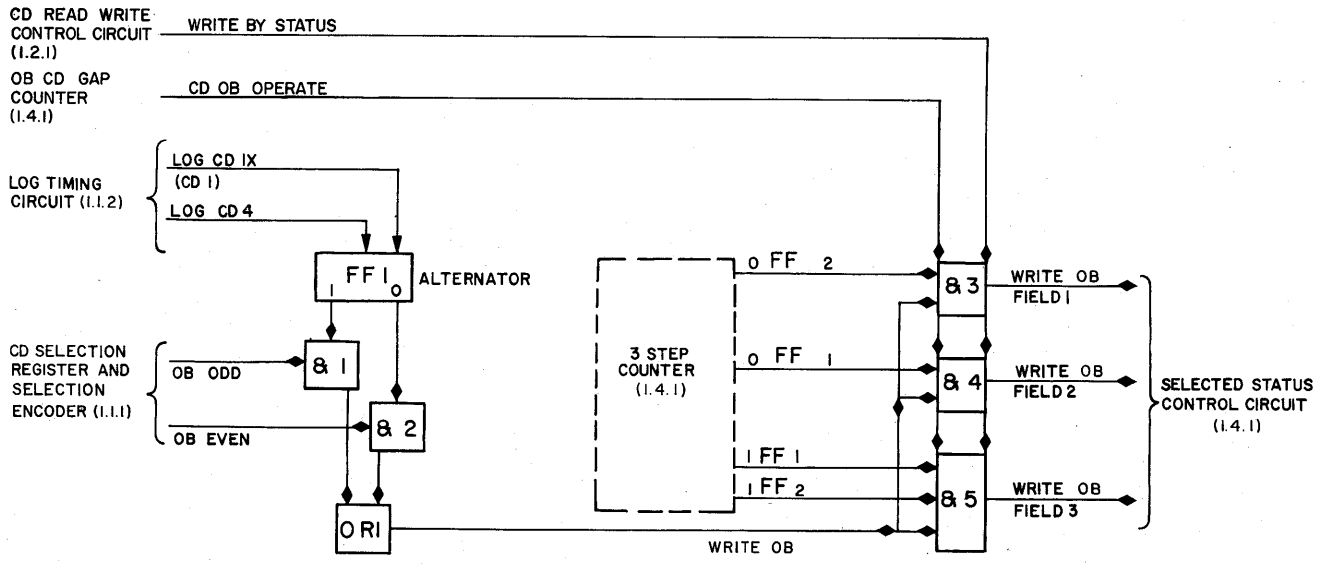


Figure 2–43. OB CD Register Switch Control Circuit, Simplified Logic Diagram

6.3 OB CD STATUS CONTROL CIRCUIT, FUNCTIONAL DESCRIPTION

The write-OB-field level from the OB CD register-switch-control circuit goes to the OB CD status control circuit. The write OB field is present at every odd or even register (6.2.2). Thus, this level is present for 10 usec (one drum register) and is absent for 10 usec. The write-OB-field level switches from one state to the other state every CD 4 time. The write-field level goes to AND 1. (See fig. 2–44.) The circuit shown is for OB field 1. The OB CD status control circuits controlling OB fields 2 and 3 are similar.

The sensing of a 0 bit in the CD status channel at CD 1 time permits FF 1 to remain in the 0 state. The 0-state output of FF 1 goes to AND 1. If the write-field level is present (the drum register is of the selected mode, odd or even), AND 1 sends an output level to gate 2. Gate 2 passes the next CD 3 timing pulse as an OB-CD-write pulse. This pulse is sent to the CD read-write-control circuit. There, the OB-CD-write pulse branches. One branch goes to the CD-write circuit as a CD-write pulse, causing the data in this circuit to be written on the drum register inspected. The second branch of the OB-CD-write pulse is delayed 2.5 usec (CD 4 time), splits, and is sent to the Central Computer System as a word-demand pulse and to the CD write circuit as a write-register-reset pulse. The word-demand pulse requests an additional word; the write-register-reset pulse clears the CD write circuit to prepare it to receive the next word.

The output from AND 1 also goes to GT 3 via OR 1. Gate 3 is conditioned to pass the CD 2 timing pulse after the empty drum register is sensed (CD 1 time). This gated pulse sets FF 2. The 1-state output of FF 2 is applied to the drum writer. When the status-write-sample pulse arrives (CD 3 time), the drum writer enters a 1 bit on the OD status channel, indicating that the associated drum register is full. The OD status channel is written at the same time that the associated drum register is written. Flip-flops 1 and 2 are cleared by the CD 4 timing pulse.

If the empty register had been of the wrong order (odd for the selection of even-writing, or vice versa), FF 2 would have remained in the 0-state and a 0 would be written in the OD status channel. Thus, the associated drum register is available for writing only when the corresponding type of operation is selected.

When a 1 bit indicating a full register is read in the CD status channel (CD 1 time), GT 1 is conditioned to pass the CD 1 timing pulse occurring during the timing cycle of the register being checked. This gated CD 1 pulse sets FF 1. The 1-state output of FF 1 conditions GT 3 via OR 1 to pass the next CD 2 timing pulse to set FF 2. The 1-state output of FF 2 causes the drum writer to enter a 1 in the OD status channel when the status-write-sample pulse is received (CD 3 time). This indicates that the register is still full. Writing of a new word is prevented by lack of the 0-state output from FF 1 at AND 1.

If the field shown is not selected, AND 1 is cut off. If a 1 is read on the CD status channel, GT 1 is conditioned to pass a CD 1 pulse. The gated CD 1 pulse sets FF 1, causing conduction in OR 1. The resulting output of OR 1 conditions GT 3 to pass a CD 2 timing pulse. The gated CD 2 timing pulse sets FF 2, causing the drum writer to enter a 1 on the OD status channel at CD 3 time. The 1 bit indicates that the associated drum register is full. Flip-flops 1 and 2 are cleared by

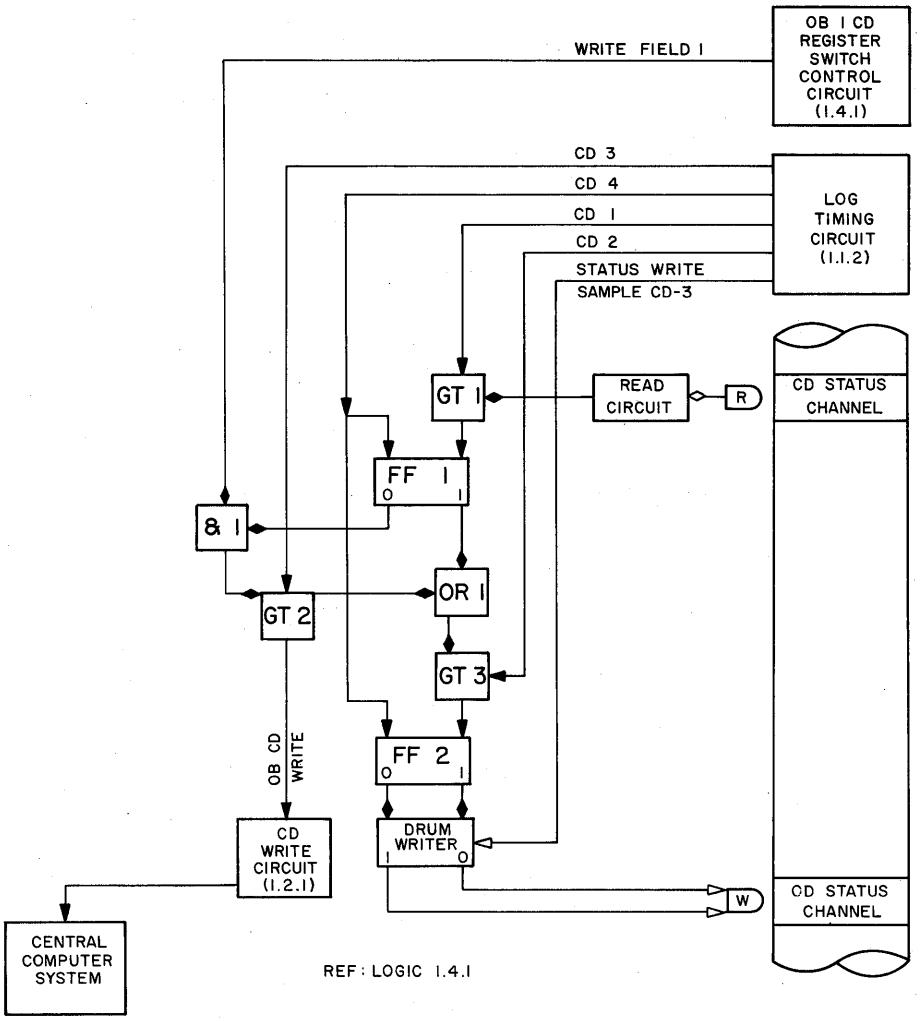


Figure 2–44. OB Field 1 CD Status Control Circuit, Write-by-Status Operation, Simplified Logic Diagram

the next CD 4 pulse. If a 0 is read on the CD status channel, FF's 1 and 2 remain in the 0 state. At CD 3 time, a 0 is written on the OD status channel, indicating that the associated drum register is empty.

Writing, therefore, is possible only on the selected registers (odd or even) of the selected field.

When the OB field switch counter is stepped by the next CD-index pulse, the write-OB-field level is removed until 12 CD 4 timing pulses have been counted by the OB CD gap counter. At this time, the OB CD status control circuit for the next OB field is conditioned for operation.

6.4 OB FIELDS OD READING, BLOCK DIAGRAM ANALYSIS

The status-indentification-controlled reading of the three OB fields is similar to the status-identification-controlled reading of the GFI, LRI, and MI fields performed by the CD circuits. The reading of the three OB fields by status identification control is a continuous operation. Each OB field has an associated OB OD status control circuit which controls the reading of that field. The three OB OD status control circuits are identical.

Each OB field is provided with two channels in addition to the 33 channels which store the drum word and the parity bit. (See fig. 2–45.) These channels are the OD status channel and the CD status channel. On any one field the bits in each channel refer to specific registers on the same field. A 1 bit in the OD status channel indicates that the register to which it refers contains a word to be read. A 0 bit in the OD status channel indicates that the register is empty.

A 1 bit in the CD status channel indicates to the CD circuits that a word is present in the drum register with which the bit is associated and that no word can be written in that register. A 0 bit in the CD status channel signifies that the register referred to is available and a word may be written in it.

The OD status channel is read by the OB OD circuits, and written by the CD circuits. The CD status

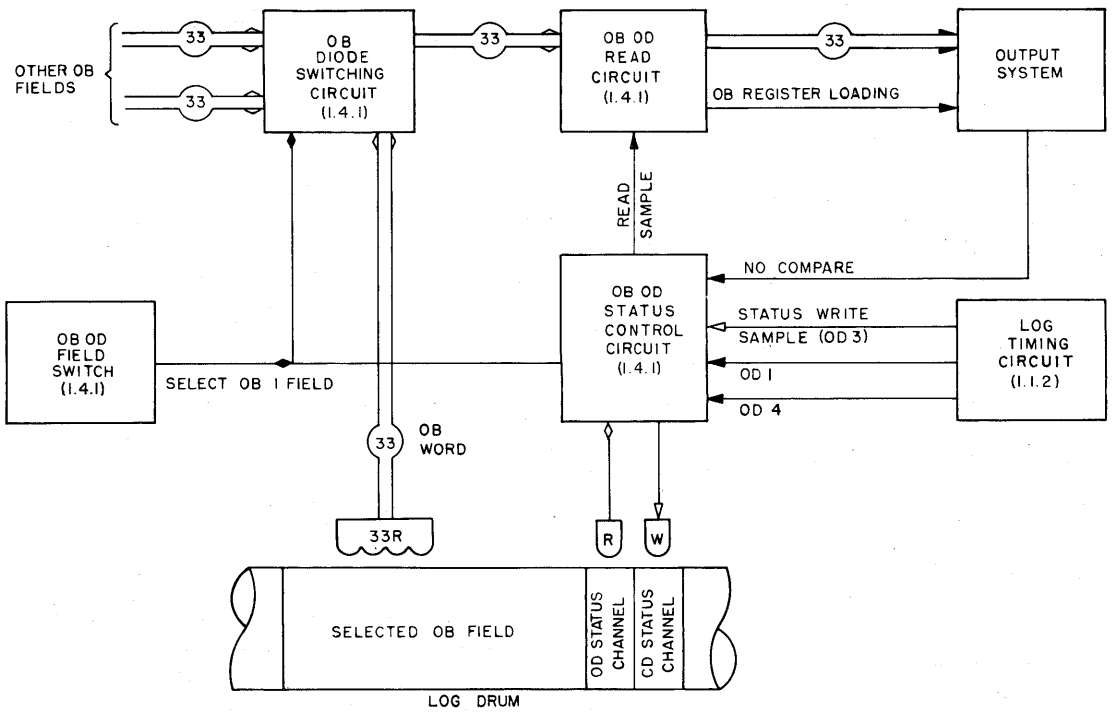


Figure 2–45. OB OD Status-Identification-Controlled Reading Block Diagram

channel is read by the CD circuits and written by the OB OD circuits. During any revolution of the LOG drum, the status channels of the three OB fields are read and written continuously. However, their contents effect the OD operations of only one field at a time. This field is the one that is chosen by the OB field selection circuits (6.5).

Figure 2–45 is the block diagram of the OD reading operation for the selected OB field. The reading operation for the other two OB fields is identical. When an OD 1 pulse is received by the OD status control circuit, from the LOG drum timing circuit, the read head for the OD status channel detects the bit for the drum register associated with the timing cycle occurring at that instant. The OD status control circuit is selected by a select level from the OB OD field switch circuit. If the OD status channel contains a 0, indicating that there is no word to be read into the Output System, the OD status control circuit produces no effect other than the writing of a 0 in the CD status channel when the status-write-sample pulse is received from the LOG drum timing circuit at OD 3 time. If, on the other hand, the OD status channel contains a 1, the OD status control circuit produces a read-sample pulse. This pulse is then sent to the OB OD read circuit. In the OB OD read circuit, the read-sample pulse produces an OB-register-loading pulse which goes to the Output System. The OB-register-loading pulse informs the Output System that a word is transmitted from the OB OD read circuit. The word is sent to the Output System at the same time as the OB-register-loading pulse. The word comes from the OB field through the OB OD diode-switching circuit.

The OB OD diode-switching circuit receives its word input from the OB field selected by the select-field level. The select-OB-field level comes from the field selection circuits. This level goes to the center taps of the read heads of the selected field. Only the contents of the selected field can pass through the OB OD diode-switching circuit.

The Output System compares identity bits in the OB word with identity bits in its own circuits. When the Drum System sends a word from one of the OB fields, the CD status channel write circuit is conditioned at OD 4 time to write a 0. If the Output System rejects the word, a no-compare pulse sets up the CD status channel write circuit to write a 1. This no-compare pulse must come to the status control circuit before the next OD 3 time when the status bit is to be written.

This operation is continuous, repeating for every register, on each OB field. At the next OD-index pulse, another OB field is selected in rotation. The reading operation remains the same, but it is now controlled by the OD status control circuit of the new OB field.

6.5 OB OD FIELD SWITCH CIRCUIT, FUNCTIONAL DESCRIPTION

The OB OD field switch circuit (fig. 2–46) switches reading operations from one OB field to the next OB field in rotational sequence. The operation of

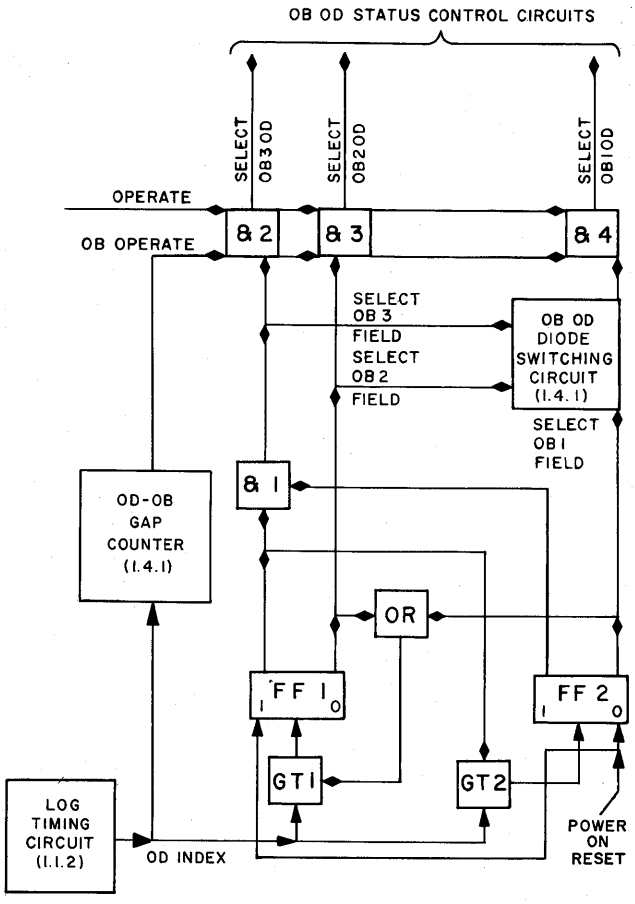


Figure 2–46. OB OD Field Switch Circuit, Simplified Logic Diagram

this circuit is similar to the operation of the OB CD field switch control circuit (6.2.1).

The OB OD field switch produces selected OB-field-levels which go to the center taps of the read heads in the OB OD diode-switching circuit, enabling them to send information to the OB OD read circuit. The OB OD field-switch circuit also produces the selected-OB OD levels at the outputs of AND's 2, 3, and 4. These levels, produced one at a time, activate the OB OD status-control circuits which control the reading of the OB fields.

In order for AND's 2, 3, and 4 to conduct, the Drum System must be in an operational mode rather than in a test mode (an operate level from the computer test control circuit must be present) and must have the OB-operate level from the OB OD gap counter. (Refer to 6.2.1 for a functional description of the OB CD gap counter. The OB OD gap counter operates in a similar manner.) The OB-operate level is present at all times except for the 120-usec period immediately following the OD-index pulse.

6.6 OB OD STATUS-CONTROL CIRCUIT

Figure 2–47 shows an OB OD status-control circuit which represents any one of the three OB OD status control circuits used in OD OB reading.

An OD 4 pulse from the LOG timing circuit clears FF 1. An OD 1 pulse from the LOG timing circuit appears at GT 1, 2.5 usec later. If a 1 is present in the OD status channel the read head for the channel and the drum read amplifier connected to this head places a wide pulse at gate 1. The presence of the 1 in the OD status channel indicates the presence of an information word in the drum register associated with that space in the status channel. The wide pulse at GT 1 conditions the gate to pass the OD 1 pulse to GT's 2 and 3. Gate 2 is conditioned by a select-OB-OD level from the OB OD field-switch circuit. Gate 2 conducts, producing an OB-read-sample pulse (at OD 1 time) which is sent to the OB OD read circuit. In the OB OD read circuit the read-sample pulse transfers the word in the drum register to the Output System and is sent to the Output System as the OB-register-loading pulse.

On receipt of the OB word and the OB-register-loading pulse (at OD 1 time), the Output System compares identity bits in the word with its own identity bits and performs a parity check on the word. The Out-

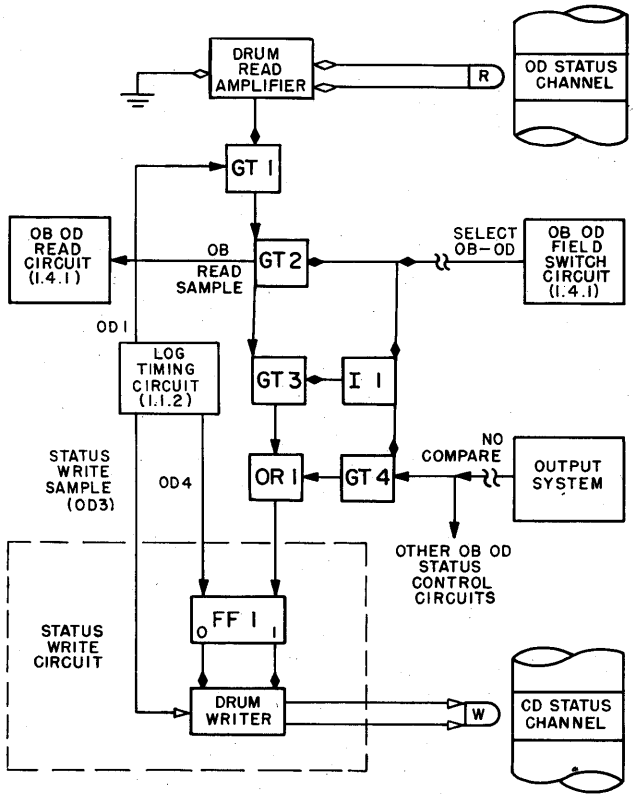


Figure 2–47. Typical OB OD Status Control Circuit, Simplified Logic Diagram

put System accepts the word if the drum word identity bits compare with the Output System identity bits. However, if the comparison produces negative results, the Output System returns a no-compare pulse to the OD status control circuits. (See fig. 2—47.) The no-compare pulse is received at GT 4. In the OB-OD-status-control circuit, the select-OB-OD level is present at GT 4 and conditions the passing of the no-compare pulse to OR 1. OR 1 also conducts if a 1 is read in the OD status channel and if the field is not selected. This is so because the inverter tube places a conditioning level at GT 3 during the absence of the select-OB-OD level. The conditioning level then passes the output of GT 1 (present when a 1 is read in the status channel) to OR 1.

Conduction in OR 1 sets FF 1, placing the 1-state

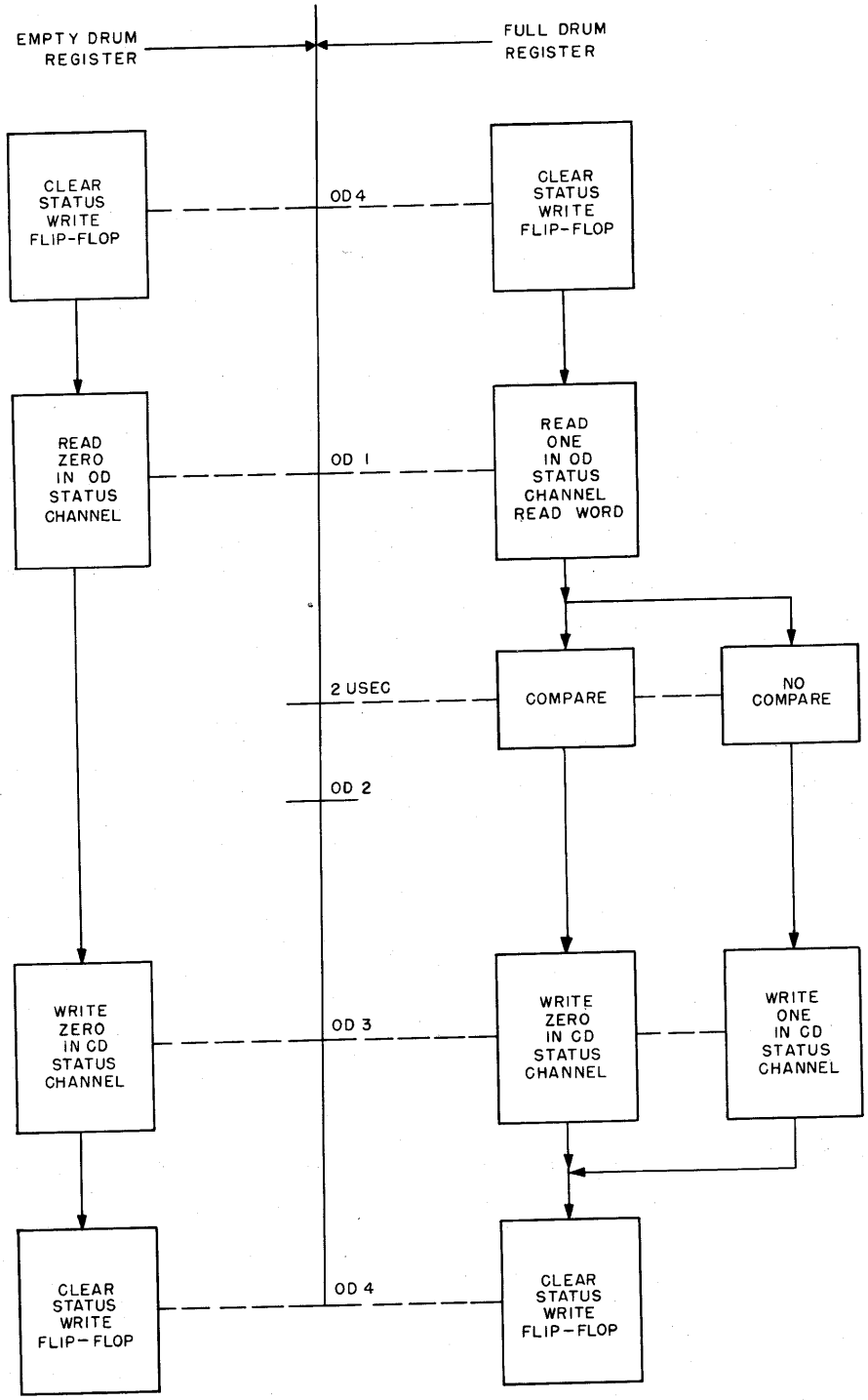


Figure 2—48. Time Sequence of Significant OD Reading Operations

output-d-c level at the drum writer. During the period of the status-write-sample pulse from the LOG timing circuit (OD 3 to OD 3 plus 1.7 usec), the drum writer places a 1 bit at the CD status channel write head. This bit causes a 1 to be placed in the point in the CD status channel that is associated with the register read into the Output System, providing an indication to the CD circuits that the word in the register has not been used during the drum revolution being considered. The Central Computer System does not write on registers whose CD status channel bits are 1's.

If a 0 bit is read at OD 1 time or if the Output System accepts the word, FF 1 sends a 0-state-output level to the drum writer because the flip-flop remains in the cleared state after the receipt of the OD 4 pulse. At these times, a 0 is written in the CD status channel, indicating to the Central Computer System that the register in question may be written into.

The next OD 4 pulse from the LOG timing circuit clears FF 1 to initiate the writing sequence for the next drum register appearing under the read heads as the drum rotates.

The status reading operation is reviewed in figure 2–48. At OD 4 time the status write flip-flop (FF 1) is cleared. At the OD 1 pulse which follows immediately thereafter, the bit in the OD status channel is detected. If the drum register is empty and the bit is a 0, the OB OD status-control circuit writes a 0 in the CD status channel at OD 3 time. If there is a word in the drum register, a 1 bit is read and the word is transferred to the Output System. If the word compares, no signal is returned, and the OB OD status-control circuit writes

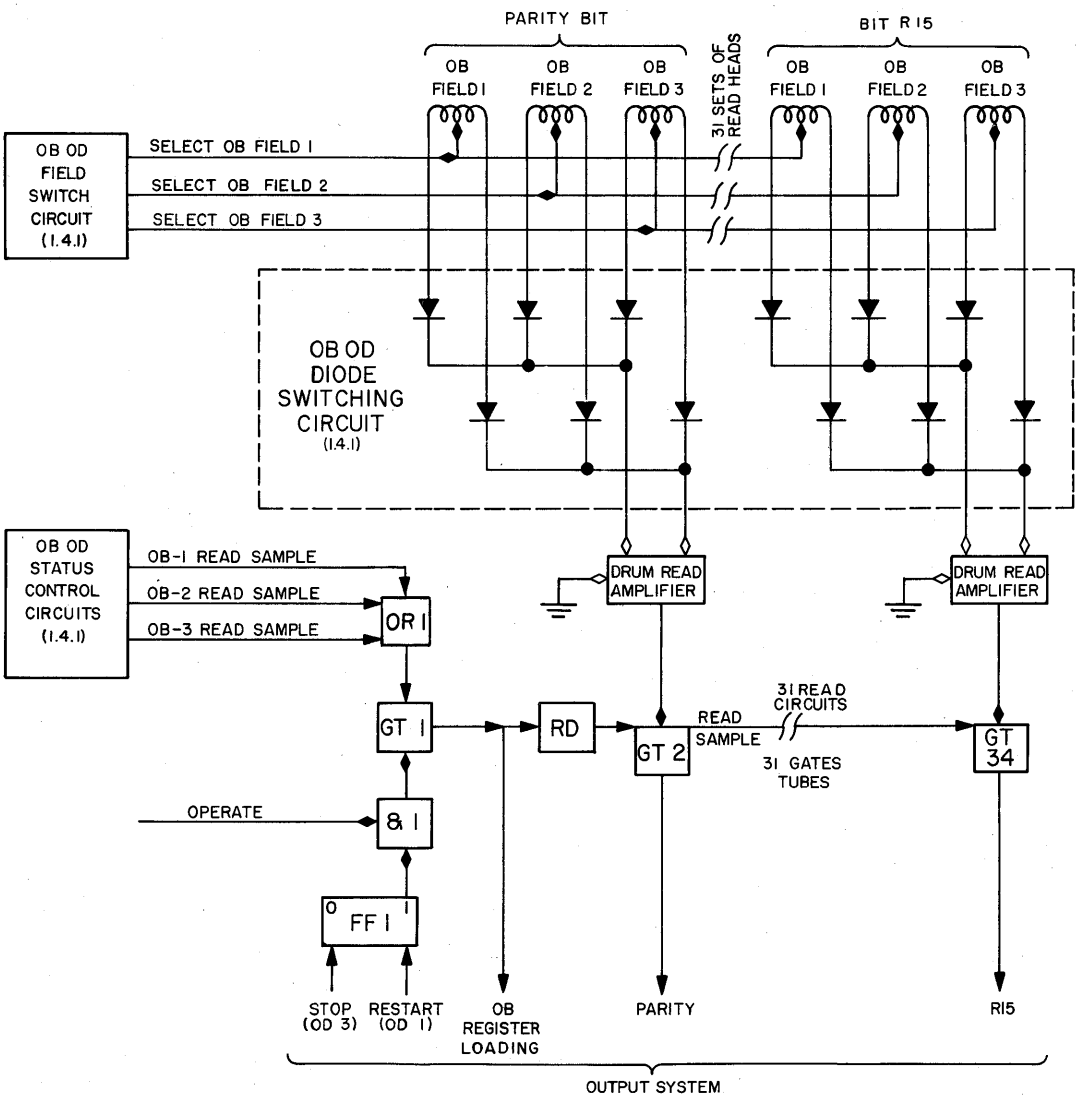


Figure 2–49. OB OD Read Circuit, Simplified Logic Diagram

a 0 in the CD status channel at OD 3 time. If, however, the word does not compare, a no-compare pulse is returned to the Drum System at OD 1 plus 2 usec. Under these circumstances, the OB OD status control circuit writes a 1 in the CD status channel at OD 3 time. At the OD 4 pulse which follows immediately, the status write flip-flop is again cleared.

6.7 OB OD READ CIRCUITS AND DIODE SWITCH

In the OB OD read circuit (fig. 2–49) the OB-read-sample pulse from the OB OD status-control circuit produces conduction in OR circuit 1. The output of OR 1 goes to GT 1. Gate 1 is conditioned if AND 1 conducts and places a d-c level at the gate. Assuming conduction in AND 1, the GT 1 output goes to the Output System as an OB-register-loading pulse. This pulse indicates to the Output System that the Drum System has placed a word in the drum word entry register. This pulse is amplified in the register driver and is applied to GT's 2 through 34 as a read-sample pulse. Each of these gates passes a read-sample pulse to the Output System whenever the gate is conditioned by a wide pulse from the drum-read amplifier to which it is connected.

The drum-read amplifier receives the read head outputs via the OB OD diode-switching circuit. The OB OD diode-switching circuit makes it possible for a single read circuit to transfer information from the three OB fields to the Output System by activating the read heads of only one field at a time. (For a detailed description of diode-switching refer to Chapter 3, 3.2.)

AND 1, (fig. 2–49) requires two d-c levels to produce an output; the operate level from the computer-test-control circuit and the 1-state output of FF 1 in the OB OD read circuit. The operate level is present whenever the Drum System is performing normal operations but is absent during test procedures. Flip-flop 1 in the OB OD read circuit is set by a restart pulse from the Output System and is cleared by a stop pulse. The stop pulse is transmitted to the Drum System OB OD circuits to stop OB reading when it is desired to perform tests on the Output System. At the conclusion of these tests, the restart pulse is sent and normal operations resume. Thus the normal operate mode of the Drum System OB OD element is the continuous reading of the three OB fields which is only interrupted when the Drum System or the Output System is in the test mode of operation.

CHAPTER 7

TRANSFER OF DISPLAY FIELDS DATA

The display fields of the Drum System are a data storage link between the Central Computer System and the Display System. Display data from the Central Computer System is sent to the display fields of the Drum System for storage. The data is then transferred from the Drum System to the Display System.

Display data from the Central Computer System is sent to the Drum System at rates too rapid for use by the Display System. Consequently, the rate of display data transfer to the Display System is reduced by interleaving the data written on the drum and employing a precessed reading pattern.

Display data is interleaved at the Central Computer System before it is written on the CD side of the drums. During OD reading, the interleaved message on the drums is transferred in the proper sequence by having the read circuits alternately skip and read in a pattern that corresponds to the programmed interleaving of the message. The skip-and-read pattern develops the necessary time delay between successive word transfers, resulting in a rate of data transfer compatible with Display System requirements.

Display data transfers are performed either automatically and continuously or at a programmed computer command, depending on the type of data being transferred. Two types of display data are sent to the Display System: digital display (DD) and situation display (SD) data. Digital display data is sent to the DD element of the Display System in a programmed operation. Situation display data is subdivided into track display (TD) data and radar data (RD). Track display and radar data are fed in continuous alternation to the situation display generator element (SDGE) of the Display System.

The circuits that transfer the DD and the SD data from the Central Computer System to the Display System are shown in figure 2—50. The heavy lines in the figure indicate the flow of display data; the lighter lines, the paths of control signals.

The CD-writing of display data is accomplished by address control. (For a detailed discussion of address-controlled writing, refer to Ch 4.) OD-reading is accomplished by the circuits on the OD side of the drums.

Digital display information is stored on one field of the MIXD drum. The DD-read circuit reads the information on the drum field under the control of the DD-read-control circuit. The DD-read-control circuit employs a reading pattern that introduces a time delay between successive DD word transfers. The reading pattern is generated by the timing circuit of the MIXD drum and involves the skipping of a fixed number of drum registers between readings of the individual words of a DD message. During the last register of each drum revolution, the reading pattern is precessed so that the next word is read one register earlier during the following revolution. This precession of the pattern ensures that no DD field registers are unread and that none are read more than once during a fixed number of drum revolutions. As the registers are read by the DD-read-circuit, the data is sent to the digital display generator element (DDGE).

Situation display information is stored on 15 fields: nine fields on one drum (RD) store RD information; six fields on a second drum (TD) store TD information. The two drums are read alternately, sending a continuous stream of display information to the SDGE.

As the TD drum is read, the contents of its fields are sent to the TD-field switch. The TD-read-control circuit selects one field at a time to be read into the SD-drum switch. The selection is made in a numerical sequence that begins with field 1.

When the reading of six TD fields is completed, eight of the nine radar fields are read (the ninth field is written on the CD side at the same time that the eight fields are read by the OD side). The fields are read through the RD-field switch under the control of the RD-read-control circuit, one field being read at a time. The field selection for RD as for TD data is consecutive, but begins with a field selected by the Central Computer System. The selected field contents are sent to the SD-drum switch. The RD field read first contains the oldest Central Computer System information. The RD field read last contains the most recent Central Computer System information. The RD field that is not read during the cycle is being written on by the Central Computer System.

The SD-drum switch transfers the data from the selected field of the drum being read to the SD-read circuit. During TD reading, the SD-read circuit is controlled by the TD-read-control circuit. This circuit employs a reading pattern that introduces a time delay between message transfers. The reading pattern is timed by the TD-timing-circuit-and-gap counter. The pattern

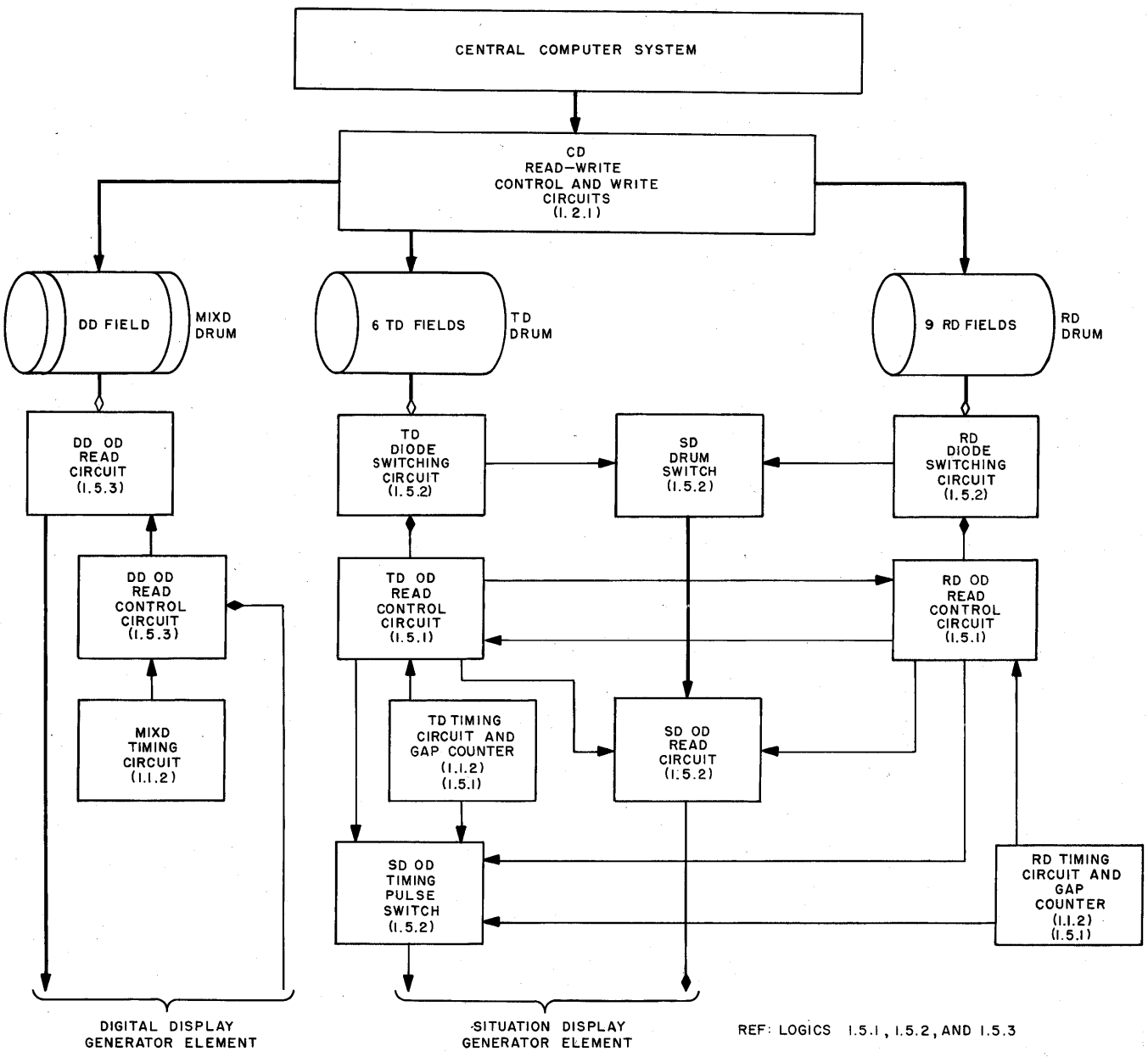


Figure 2–50. Transfer of Display Fields Data, Block Diagram

involves skipping a fixed number of multiword slots before the reading of each multiword slot. As in DD reading, the read pattern is precessed at the end of each revolution.

During RD reading, the SD-read circuit is controlled by the RD-read-control circuit. Like the other two display read-control circuits, the RD circuit has a precessed reading pattern that introduces a time delay between readings of successive slots.

When TD reading is completed, a signal from the TD-read-control circuit goes to the RD-read-control circuit and starts the RD reading operation. When reading of the RD fields is completed, the RD-read-control circuit sends a signal to the TD-read-control circuit, recommencing the TD reading operation.

During the time each drum is being read, its associated timing circuit, gap counter, and read-control circuit send control signals or timing pulses to the SD-timing-pulse switch. The signals from the drum being read are then switched to the SDGE. Two types of timing pulses are developed by the two timing circuits and gap counters: drum timing pulses which are developed during any of 2,060 timing cycles (RD or TD drum) and OD pulses from the 2,048 cycles between the 13th and the 2,060th timing cycle.

7.1 TRANSFER OF DIGITAL DISPLAY DATA

Digital display information is interleaved by the Central Computer System before it is written on the CD side of the Drum System. Therefore, successive words of a message are not written in successive drum registers.

During OD reading, the message is transferred in the proper sequence by having the read circuits alternately skip and read in a pattern that results in 6, 40-usec intervals between the readings of consecutive message words. This pattern makes it necessary for the drum to turn through 64 revolutions before the entire DD field is read. At the end of each revolution, the reading pattern is stepped one number ahead of its normal count to ensure that all registers are read.

7.1.1 DD OD Reading, Functional Analysis

Digital display reading is initiated in the OD display circuits when the start-read portion of the DD-read-control circuit receives a control pulse from the DDGE. The start-DD-read pulse conditions the start-read circuit to gate OD 2 and index pulses to the register counter as step pulses.

Step pulses are counted in the register counter, producing an output level when 63 have been counted. The output level goes to the read-sample gate, causing the development of a read-sample pulse at the 64th OD 1 pulse.

Read-sample pulses go to the DD read gates and the DDGE. In the drum read amplifiers, the read-sample pulse causes the transfer of the information word in the 64th drum register to the generator element. In the DDGE, read-sample pulses step a timing counter that counts the number of DD words received from the DDGE.

During the same drum register that the OD 1 read-sample pulse is produced, but 2.5 usec later, the 64th OD 2 step pulse returns the register counter to 0. The counter restarts its cycle of 64 when it receives the 65th step pulse.

In this manner, 63 drum registers are skipped, the 64th is read, 63 skipped again, the 128th read, and so on in the same reading pattern. During the 2,048 registers of one MIXD drum revolution, 32 read samples are produced. To prevent the read samples of the second revolution from being produced at the same registers as the read samples of the first revolution, the register counter is precessed by counting the index as well as the OD 2 pulse during the 2,048th register. As a result, the second-revolution-read-sample pulses are generated at the 63rd register, the 127th register, and so on.

Index pulses continue to form additional step pulses once each revolution. Each time an additional step pulse is formed, the read-sample pulses produced during the following revolution appear one register earlier. In 64 revolutions of the MIXD drum, 64 additional step pulses are formed and every register on the drum field is read once.

At the end of the 64th revolution, the index pulse coincides with the register counter d-c output level. This produces an end-DD pulse, which stops DD reading until a new start DD-reading pulse is sent by the DDGE.

7.1.2 DD OD Reading, Circuit Analysis

Digital display OD reading (fig. 2–51) begins with a start-DD-read pulse from the DDGE.

In the DD-OD-read-control circuit, the pulse sets flip-flop 1 (FF 1) of the start-read circuit to the 1 side. The resulting level conditions gate 1 (GT 1) to pass OD 2 and index pulses from OR 1 to the register counter as step pulses.

During the first 2,047 registers of the drum, OD 2 pulses provide the only inputs to OR 1. At the 2,048th register, the OD 2 pulse produces conduction in the OR circuit; in addition, conduction is produced by the MIXD-index pulse at OD 3 time.

The register counter (shown in fig. 2–52) counts the step pulse inputs from the start-read circuit. The counting process is the same as that described for the angular position counter in 4.4.1.

At the time of the 63rd step pulse, all flip-flops in the register counter are set, causing conduction in AND 1. The output of AND 1 conditions GT's 3 and 4 (fig. 2–51). Before the 64th OD 2 step pulse clears the counter, the 64th OD 1 pulse from the MIXD-timing circuit is passed by GT 3. Except for the time when the DD field is being tested, an operate level from the computer test control circuits conditions GT 5 to pass the output of GT 3. The resulting pulse is the DD-read-sample pulse, which is sent to the DD-read circuit to release a word to the DDGE.

In the DD-read-circuit, the read-sample pulse is gated to the DDGE by each of 32 drum read amplifiers, which detect 1 bits on the drum field. A 33rd drum read amplifier is present for the parity bit, but this bit is only for testing.

Although not indicated in figure 2–51, the read sample also goes directly to the DDGE as a load-DD pulse and to the test circuitry as a DD-test-read-sample pulse. In the generator element, the load-DD pulses are counted to determine the number of words read by the DD-read circuits.

This pattern of skipping 63 registers and producing a read-sample pulse every 64th register is continued for a complete drum revolution. During the last register of the revolution, the OD index pulse (at OD 3 time) serves as an alternate input to OR 1. The OR 1 output is passed by GT 1 to form a step pulse. This extra step pulse during the 2,048th register precesses the register counter so that the read-sample pulses produced by its

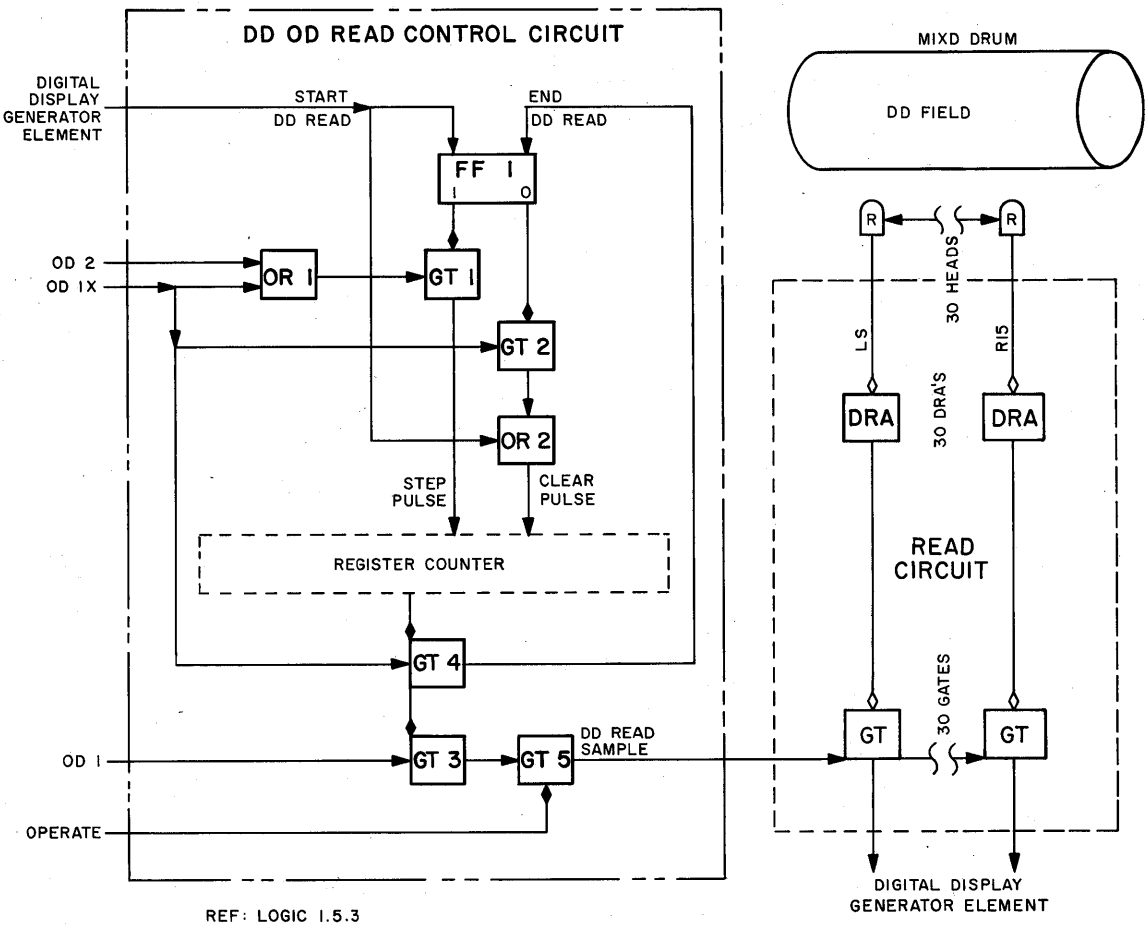


Figure 2–51. Digital Display OD Reading Operation, Simplified Logic Diagram

outputs coincide with the 63rd, 127th, 191st, and so on, registers of the second revolution. At the end of the second revolution, precession causes a read-sample pulse to coincide with the 62nd register, then the 126th,

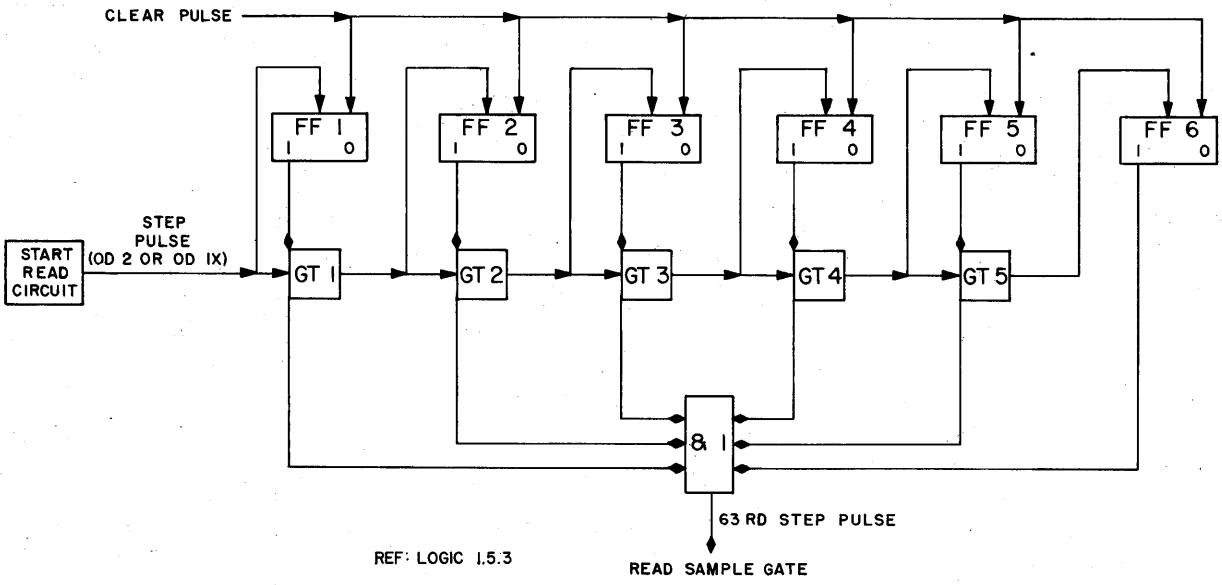


Figure 2–52. Digital Display Register Counter, Simplified Logic Diagram

190th, and so on. At the end of the 64th revolution, ail drum registers on the DD field are read, and the register counter output level coincides with an OD index pulse. This coincidence in GT 4 forms an end-DD-read pulse (see fig. 2–51).

The end-DD-read pulse goes to the start-read circuit, clearing FF 1. The rise time of the 0 output of the flip-flop is not fast enough to pass the same index pulse that is at GT 2; but, at the end of the following drum revolution, the next index pulse is passed. This gated index pulse clears the register counter flip-flops. No DD-read-sample pulses can be produced thereafter, until another start-DD-read pulse sets FF 1.

Figure 2–53 indicates the DD registers for which read-sample pulses are produced during each revolution of the MIXD drum.

7.2 TRANSFER OF SITUATION DISPLAY DAtA, FUNCTIONAL ANALYSIS

Situation display reading begins in the OD display element when the Drum System is energized. A power-on-reset signal from the manual control panel is sent to the TD-OD-read-control circuit (see fig. 2–54). In the read-control circuit, the power-on-reset pulse produces a field-select level. This level goes to the TD diode-switching circuit to cause the contents of field 1 to be switched into the SD-drum switch. The drum switch enables the OD display element to use one set of read circuits for both TD and RD words by transferring the contents of the selected field from the drum that is being read to the SD-OD-read circuits. At the end of every 13th TD drum revolution, the field-select level is changed, switching the contents of fields 1 through 6, in that order, into the read circuits. The TD-OD gap counter develops a 120-usec delay at the beginning of each revolution, which provides for decay of switching transients when fields are being switched. (Refer to 2.1.3 for a description of gap counters.)

The field contents are passed through the read circuits to the SDGE when an SD-read-sample pulse is received by the read circuits from the TD-OD-read-control circuit. Read-sample pulses are produced in a regular pattern. While the first 12 8-word slots of a TD field pass under the read heads, no read-sample pulses are produced; however, eight read-sample pulses are produced (one for each word) for the 13th slot. Twelve more slots are skipped, and one is read into the generator element. During the last drum register of each revolution, an index pulse from the TD-timing circuit advances the slot count. By the end of 13 drum revolutions, all slots of the selected TD field are read.

Two and one-half usec before each read-sample pulse is produced, a TD-word-on-way (WOW) pulse is generated to inform the SDGE that a word is about to be read. The WOW pulses go to the SDGE via the SD-

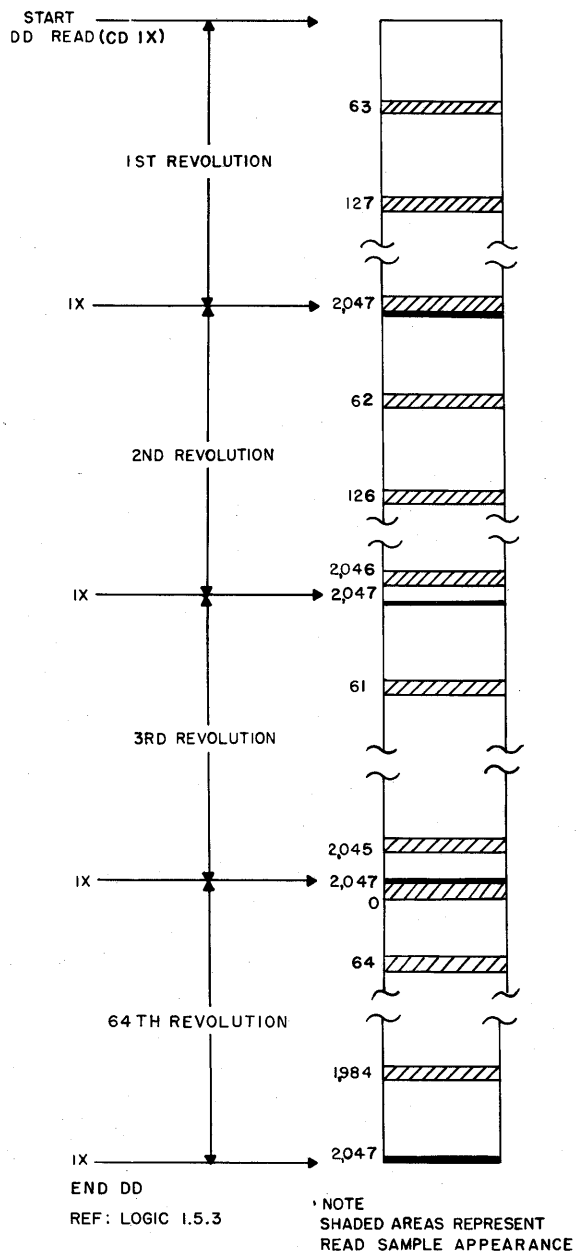


Figure 2–53. Sequence of Digital Display Reading

timing-pulse switch, which transfers them along with timing and index pulses from the TD-timing circuit.

After the drum has rotated 78 times (13 times for each of the six fields), all registers of the TD drum have been read, and an end-TD-start-RD pulse is produced in the TD-OD-read-control circuit. This pulse stops TD reading and goes to the RD-read-control circuit to begin RD reading. It also goes to the SDGE to condition the element to present RD information.

At the start of RD reading, the RD-read-control circuit produces a field-select level which designates the first field to be read. The first field selection to be made

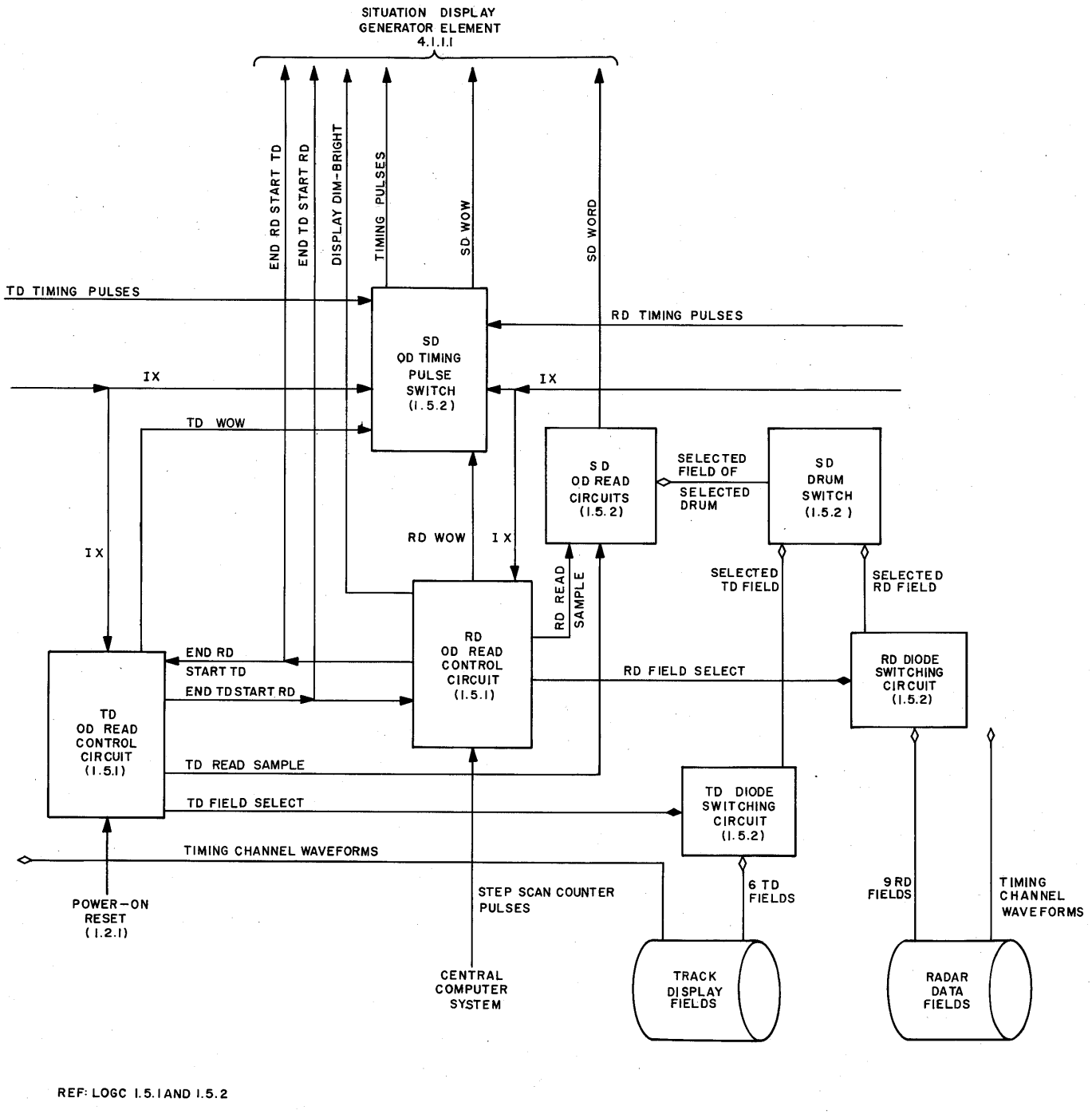


Figure 2–54. Situation Display Reading, Block Diagram

is computed by adding 1 to the number of step-scan-counter pulses that have been sent to the RD-read-control circuit by the Central Computer System. The total number of pulses that have been received indicates which field is being written on by the Central Computer System. By adding 1 to the number, RD selection circuits begin reading the earliest written information first. The next seven fields are selected for reading in numerical order. The field being written on by the Central Computer System is not read during the same read cycle as the other eight fields. The contents of the selected field are switched into the SD-read circuits by the RD diode switching circuit and the SD-drum switch. The RD gap counter provides the 120-usec delay required by the read circuits for switching time. (Refer to 2.1.3 for a description of gap counters.) Each time a read-

sample pulse is produced by the RD-read-control circuit, the information at the SD read circuits is sent to the SDGE.

Read-sample pulses for RD reading are produced according to a pattern which provides for the skipping of five registers between the production of two successive read-sample pulses. This pattern of reading one register and skipping five is repetitive, continuing for three drum revolutions. At the end of the third revolution, all the odd registers will have been read. At this time, the reading pattern is precessed one register by an RD index pulse, permitting reading of the even registers during the next three drum revolutions. Thus, by the end of six drum revolutions, all the registers of the selected RD field are read. Table 2–2 indicates the sequence in which the registers of the selected TD field are read. Only the registers of the first and last slot read during a given drum revolution are shown in the table. Similarly, table 2–3 indicates the sequence in which the registers of the selected RD field are read. Only the first register and the last register read during a given drum revolution are shown.

Two and one-half usec before the generation of each read-sample pulse, an RD-WOW pulse (fig. 2–54) is produced to inform the generator element that a word is to be read. The WOW pulses go to the SD-timing-pulse switch. During RD reading, the RD-WOW and RD-timing and IX pulses (the latter from the RD-timing circuit) are sent to the SDGE.

When the RD field containing the most recently written information is being read, the RD-read-control circuit sends display-bright pulses to the generator element. During the display of the other seven RD fields read during the same cycle, display-dim pulses are sent in place of the display-bright signal.

When all registers of eight RD fields are read, an end-RD-start-TD pulse is generated. This pulse is sent to the TD-read-control circuit and the SDGE. In the read-control circuit, it starts the TD reading operation. In the generator element, the start-TD pulse conditions the display circuits to present the data read out during the track data reading cycle.

TABLE 2–2. SEQUENCE OF READING OF TD FIELD REGISTERS

TD DRUM REVOLUTION	FIRST GROUP OF REGISTERS AT WHICH TD READ SAMPLES ARE PRODUCED	LAST GROUP OF REGISTERS AT WHICH TD READ SAMPLES ARE PRODUCED
1	96-103	1968-1975
2	16-23	1992-1999
3	40-47	2016-2023
4	64-71	2040-2047
5	88-95	1960-1967
6	8-15	1984-1991
7	32-39	2008-2015
8	56-63	2032-2039
9	80-87	1952-1959
10	0-7	1976-1983
11	24-31	2000-2007
12	48-55	2024-2031
13	72-79	1944-1951

TABLE 2–3. SEQUENCE OF READING OF RD FIELD REGISTERS

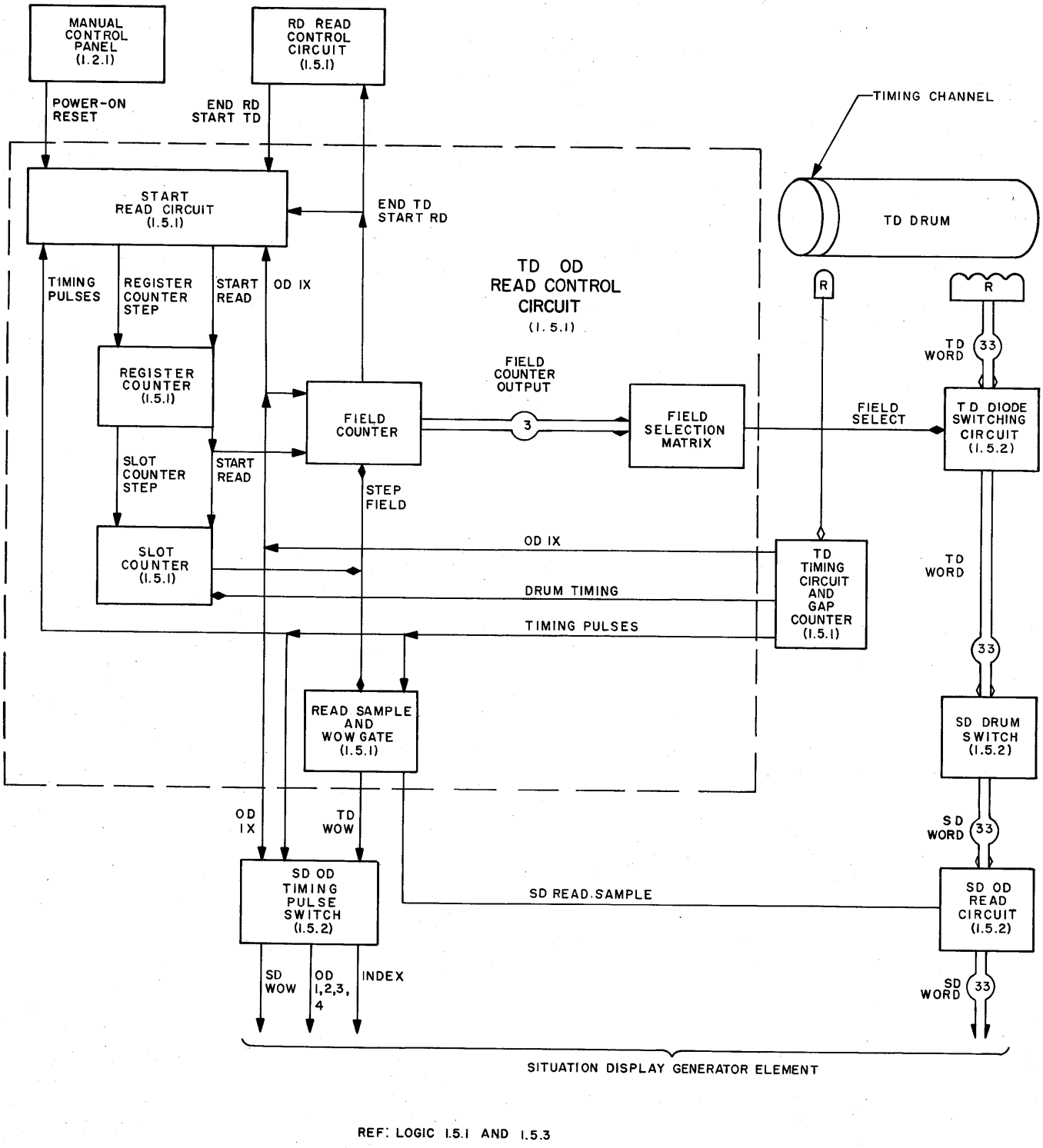
RD DRUM REVOLUTION	FIRST REGISTER AT WHICH RD READ SAMPLE IS PRODUCED	LAST REGISTER AT WHICH RD READ SAMPLE IS PRODUCED
1	1	2047
2	5	2045
3	3	2043
4	0	2046
5	4	2044
6	2	2042

7.3 TRACK DISPLAY OD READING, FUNCTIONAL ANALYSIS

Situation display OD operations begin with the reading of the TD drum. When the Drum System is energized, a power-on-reset pulse goes from the manual control panel to the TD-read-control circuit (fig. 2–55). In the start-read portion of the read-control circuit, the power-on-reset pulse produces a reset pulse, which clears the register, slot, and field counters.

The field counter, when cleared, produces a field-select level for TD field 1 in the field-selection matrix. The field-select level is applied to the read heads of TD field 1, to prepare them for a reading operation.

The start-read circuit passes OD 2 pulses to the register counter as register-counter-step pulses. The register counter is a scale-of-8 counter which produces a slot-counter-step pulse every time it counts eight register-counter-step pulses. The slot-counter-step pulses go to the slot counter, which is a scale-of-13 counter.



REF: LOGIC 1.5.1 AND 1.5.3

Figure 2–55. Track Display Reading, Block Diagram

The 12th slot-counter-step pulse counted produces a level which, in conjunction with the drum-timing level from the TD-OD gap counter, produces a read and step-field d-c level. (The TD-OD gap counter provides the 120-usec delay necessary to permit decay of field switching transients.)

The read level passes timing pulses in the read-sample and WOW gates to send WOW pulses to the SD-timing-pulse switch and TD-read-sample pulses to the SD read circuits.

A WOW pulse is sent to the SDGE to prepare the element to receive a TD word. The TD word is sent 2.5

usec later when the read-sample pulse samples the read gates in the SD-OD read circuit.

Eight read-sample pulses are produced, one for each of eight registers counted by the register counter. The eighth pulse counted produces the slot-step pulse which clears the slot counter.

Twelve more slots are counted before another slot is read. The process of skipping 12 slots and reading one continues until one drum revolution is completed. The index pulse then acts as a slot-counter-step pulse and advances the slot counter. As a result, all groups of eight read-sample pulses are produced one slot earlier than if normal counting had continued in the slot counter. This continues for 13 revolutions. At the end of the 13th revolution, all registers in the field have been read and the step-field level at the output of the slot counter coincides with the index pulse. The output resulting from this coincidence is used to step the field counters. The changed field counter output goes to the field-selection matrix and produces a field-select level that designates the next TD field.

7.4 TRACK DISPLAY OD READING, CIRCUIT ANALYSIS

Track display OD reading can be divided into two operations: development of the reading pattern and field switching. The circuits used to produce the precessed reading pattern employed for TD reading are described in 7.4.1; those used to switch from one TD field to another are described in 7.4.2.

7.4.1 TD Reading Pattern Development, Circuit Analysis

The SD OD circuits employed to develop the precessed reading pattern used for TD are shown in figure 2–56.

When the Drum System is first energized, a power-on-reset pulse is sent to the start-read portion of the TD-read-control circuit to initiate the SD reading operation. During subsequent SD reading cycles, end-RD-start-TD pulses from the RD-read-control circuit start the reading operation. Either pulse will produce at the output of OR 1 (fig. 2–56) a start-TD-and-reset pulse which sets FF 1 and clears the register counter, the slot counter, and the field selection counter. The start-TD-and-reset pulse also clears FF 2 by producing conduction in OR 2. The 1 output of FF 1 conditions the passing of index pulses at GT 1. The GT 1 output sets FF 2 to the 1 state. The level at the 1 output of FF 2 goes to the field switching circuits as a TD-select level and passes OD 2 pulses from the TD-timing circuit at GT 2. Gate 3 is also conditioned by the same level, but not in time to pass the index pulse that sets FF 2.

The GT 2 output pulses form register-counter-step pulses which clear FF 1 and step the register counter. The register counter is a scale-of-8 counter which operates on the principles described in 7.1.1. Every eighth step pulse counted by the register counter produces an end-carry-output pulse. Since the TD drum is written in 8-word slots by the Central Computer System, each register counter pulse output represents one slot.

The register counter output goes to OR 3, causing it to conduct. The pulses taken from the output side of OR 3 are called slot-counter-step pulses and are used to step the slot counter. The slot counter is a scale-of-13 counter, the operation of which follows. (See fig. 2–57.) The counter is initially cleared by the start-TD pulse at OR 2. With FF 3 or 4 at 0, OR 1 conducts. The output of OR 1 conditions GT 1 to pass slot-counter-step pulses to the counter. (Refer to 7.1.1 for a discussion of counting circuits.) The 0 output of either FF 3 or FF 4 or both maintains conduction in OR 1 until 12 slot-counter-step pulses have been counted. At this time, FF's 3 and 4 are in the 1 state. The 1 outputs of both flip-flops produce conduction in AND 1 when added to the TD-timing level. The level at the output of AND 1 is called the read-and-step-field level. It remains at the output of AND 1 until the next slot-counter-step pulse arrives at GT 5, eight registers (one slot) later. The step-field level conditions the passing of this 13th slot-counter-step pulse at GT 5 to OR 2. (Since there are no 0 outputs from FF's 3 and 4 during the 12th slot-counter-step pulse, GT 1 will not be conditioned to pass the 13th slot-counter-step pulse.) The output of OR 2 clears the counter. At the next slot-counter-step pulse, counting begins again.

During the period between the 12th and the 13th slot-counter pulses, the read level (fig. 2–56) passes eight drum-timing pulses in GT 5 to produce eight TD-WOW pulses. The WOW pulses go to the SD-timing-pulse switch. They are then relayed to the SDGE to prepare the generator element to receive words from the drums. The words are produced 2.5 usec later by having the step-field level pass DTP 1 pulses in GT 6. The output of GT 6 is the TD-read-sample pulse, which produces conduction in OR 6. The output of OR 6 is passed by GT 7, which is conditioned by an operate level from the computer-test-control circuit. (The operate level is present during normal operation but absent during test procedures.) The TD-read-sample pulses thus become SD-read-sample pulses. They go to the SD-read circuits and serve to transfer the TD word to the SDGE.

In this manner, 12, 8-word slots are counted before one slot of eight is read. At the end of the reading of that one slot, no read-sample pulses are developed until 12 more slots have been skipped.

The skip-12, read-1, skip-12 pattern continues until the first revolution of the drum is completed. At this time, an index pulse is passed through GT 3 to duplicate the functions of the slot-counter-step pulse. As a

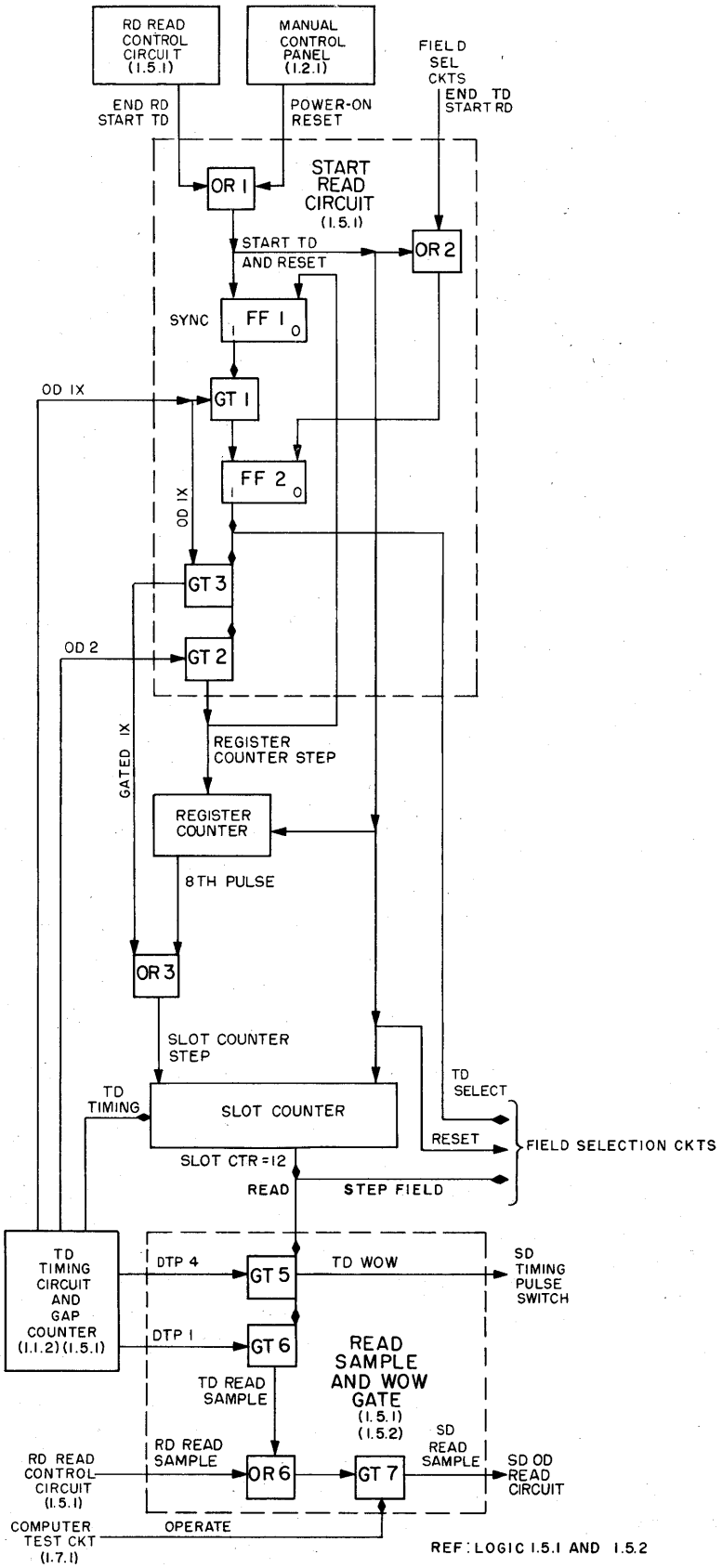


Figure 2–56. Track Display Reading Pattern Development, Simplified Logic Diagram

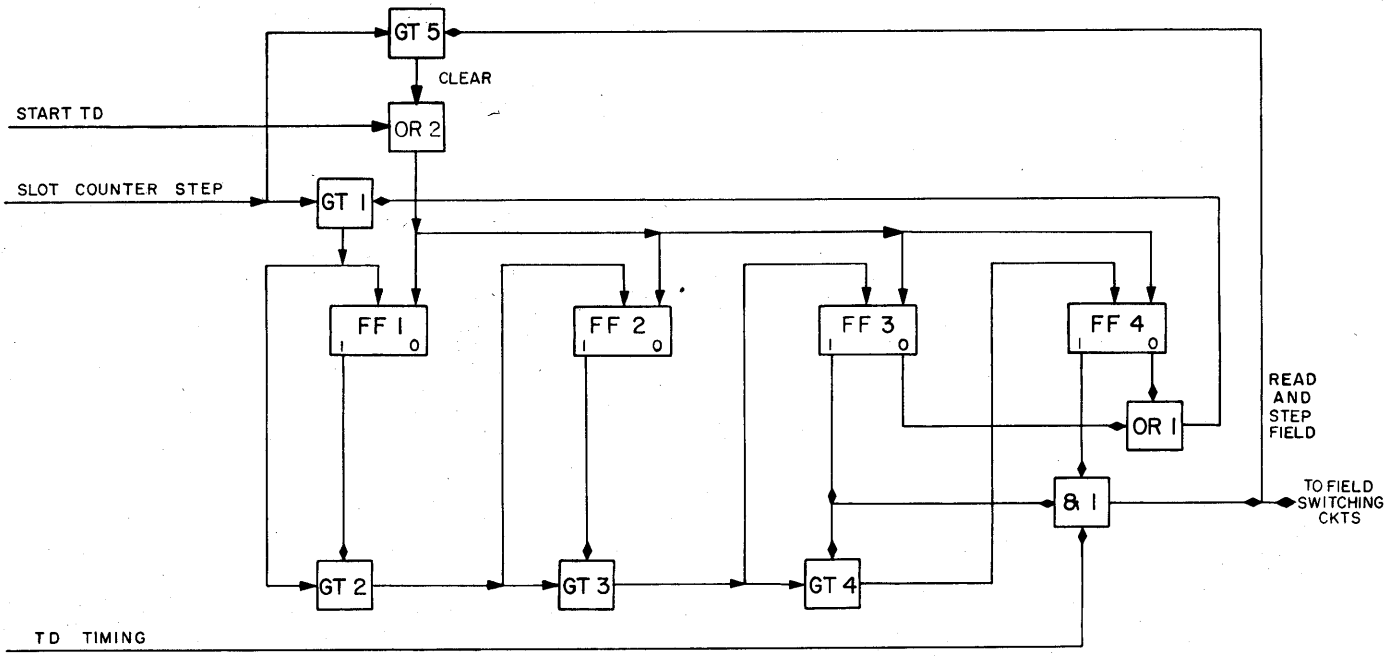


Figure 2–57. Track-Display Slot-Counter Circuit, Simplified Logic Diagram

result, the slot counter is stepped ahead in its count. Each group of eight read-sample pulses is produced one slot earlier at each successive revolution of the drum. The first group of read-sample pulses is delayed 120 usec to allow for field switching by skipping the first 12 timing cycles at the beginning of each revolution. This is accomplished by means of the gap counter.

At the end of 13 drum revolutions, all registers on the selected TD field have been read. The TD index pulse then clears the slot counter to prepare it to count for the next field.

7.4.2 TD Field Switching, Circuit Analysis

When the first TD reading operation begins (refer to 7.4.1), the start-TD-and-reset pulse which clears the counters in the read-pattern-development circuits also clears the field counter of the TD-field-switching circuits. (See fig. 2–58.) Thereafter, the field counter is stepped by the output of GT 1. Gate 1 conducts when the step-field level from the slot counter (described in 7.4.1) is coincident with the index pulse. This condition exists at the end of every 13th revolution of the drum. Thus, as soon as all registers of a field are read (after 13 revolutions), the field counter is stepped and the next field is selected.

The output of the field counter selects the next field by establishing a combination of d-c levels at the input to the field-selection matrix. (See fig. 2–58.)

When the field counter is cleared, the combination of the 0 outputs from its three flip-flops and the TD-select level (produced by starting TD reading) provides the necessary conditions for conduction in AND 1. When AND 1 conducts, it produces a select-field-1 level, which goes to the center taps on the 33 read heads of the first TD field, enabling them to conduct.

When the field counter is stepped, levels at its output change, causing different AND circuits in the field selection matrix to conduct. The earlier field select level decays, and a new one is produced. Table 2–4 shows the flip-flop output combinations that produce conduction in the different AND circuits in the matrix, and the field that is selected as a result.

At the sixth input (the 5th step-field pulse after the reset pulse) to the field counter, AND 7 conducts, conditioning GT 2.

TABLE 2–4. TRACK DISPLAY FIELD SELECTION

STEP FIELD GATED INDEX PULSES	COUNTER OUTPUTS			AND CIRCUIT	FIELD SELECTED
	FLIP-FLOP 1	FLIP-FLOP 2	FLIP-FLOP 3		
Reset Pulse	0	0	0	1	1
1st	1	0	0	2	2
2nd	0	1		3	3
3rd	1	1		4	4
4th	0		1	5	5
5th	1		1	6	6

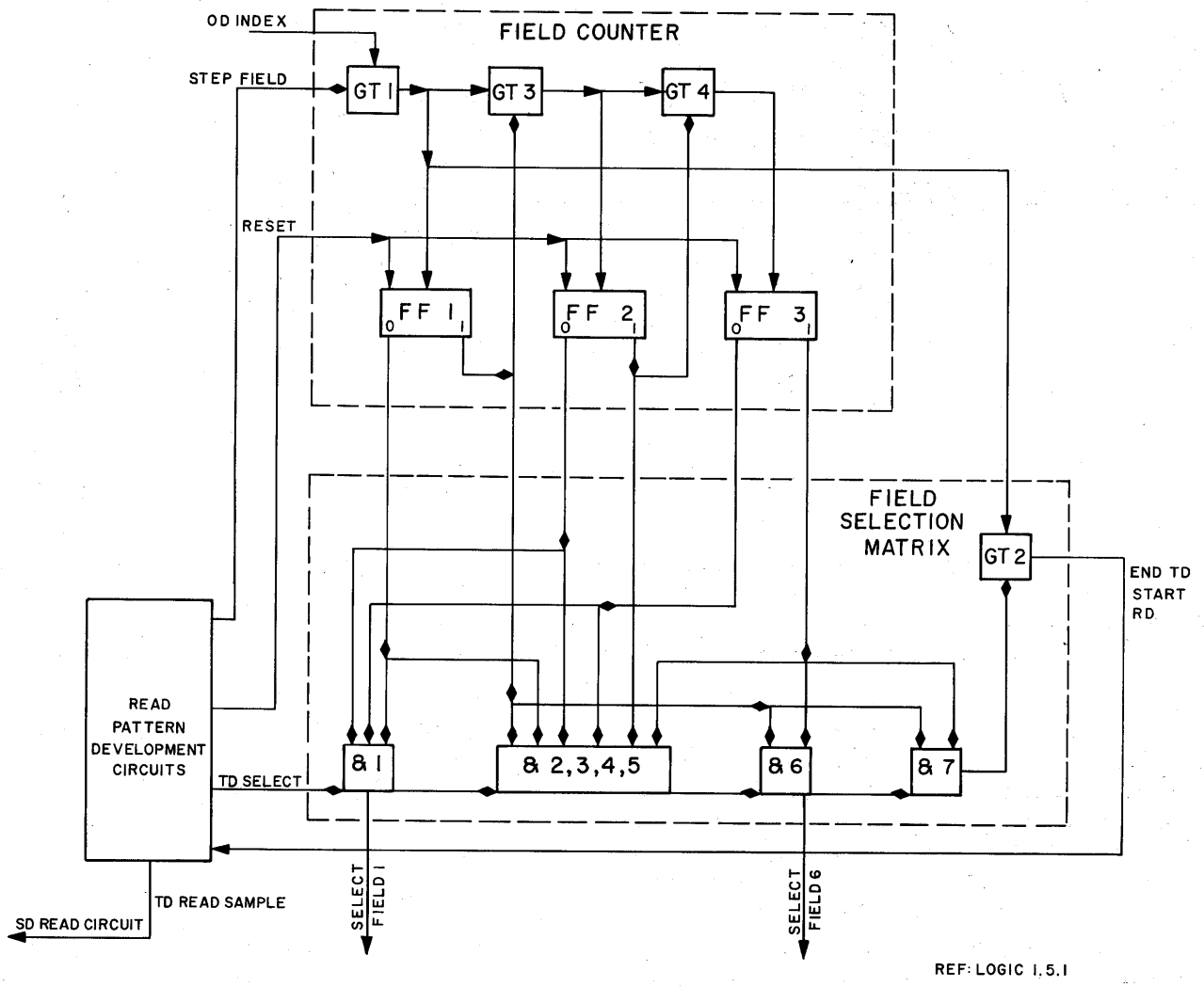


Figure 2–58. Track-Display Field Selection Circuits, Simplified Logic Diagram

The sixth-step-field pulse is passed to GT 2, forming an end-TD-start-RD pulse. This pulse is sent to the start-TD-read circuit (as shown in fig. 2–56), where it clears FF 2, thus stopping the development of the reading pattern.

The read heads for all TD fields are connected to the same 33 pairs of reading diodes in the SD-drum switch, but only the heads of the selected field conduct (fig. 2–59). The TD diode switching circuit prevents conduction of the read heads in nonselected TD fields by isolating the selected-TD-field level from these read heads.

Similarly, the SD-OD-drum switch permits the use of the same drum read amplifiers for reading of the TD or the RD drums. The reading diodes in the SD-OD-drum switch isolate the selected-field level of either drum from the circuits of the other. (Refer to 3.3 for a detailed discussion of diode switching.)

7.5 RADAR DATA OD READING, FUNCTIONAL ANALYSIS

Radar data reading follows TD reading, beginning when the end-TD-start-RD pulse, from the TD-read-control circuit, enters the RD-start-read-control circuit. (See fig. 2–60.) The start-read circuit is conditioned to pass OD 2 and index pulses to the register counter as step-register-counter pulses. The start-read circuit also forms an RD-select level which goes to the read-sample and WOW-gate circuit, field selection matrix, and SD OD timing pulse switch.

The register counter is a scale-of-6 counter. The first step-register-counter pulse counted in each counting cycle produces a read level of the register counter output. The step-field-read-counter level is sent to the read-sample-and-WOW-gate-and-intensity control. In the latter circuit, it conditions the passing of an OD 4 pulse to form an RD WOW pulse. This pulse is sent to

the SD timing pulse switch. From the timing pulse switch it is sent to the SDGE to inform the element that a word is about to be sent by the RD circuits.

Two and one-half usec after the production of the RD-WOW pulse, an OD 1 pulse is passed to produce an RD-read-sample pulse. The read-sample pulse is sent to the TD-read-sample-and-WOW gate to form an SD-read-sample pulse. (See fig. 2–56.) The SD-read-sample pulse is passed by the 1 bits in the SD-read circuits, thereby transferring the RD word to the SDGE.

During the second through the sixth step-register-counter pulses in the register counter counting cycle, there is no counter output. Therefore, no WOW pulses or read-sample pulses are produced for five registers. This pattern of reading one register and skipping five is repetitive, continuing for three drum revolutions. At the end of the third revolution, all the odd registers will have been read. At this time, the reading pattern is precessed one register by an RD index pulse, permitting reading of the even registers during the next three drum revolutions. At the end of six drum revolutions, all drum registers are read. An RD OD index pulse is gated by the read-sample-and-WOW-gate-and-intensity-control circuit and becomes a step-field-switching-counter pulse (see fig. 2–60). This pulse is sent to the fields counter, the field-switching counter, and the register counter. The levels at the field-switching counter's output go to the field-selection matrix to produce select-field levels, which indicate the RD field to be read next. Reading is done by sending the select-field levels to the RD diode-switching circuits, which transfer the contents of the selected RD field into the SD-OD-read circuit via the SD-drum switch. Radar data information bits at the SD-read circuit are transferred to the SDGE by SD-read-sample pulses. The SD-read-sample pulses, as indicated above, come from the RD-read-sample-and-WOW-gate whenever RD-read-sample pulses are produced by the RD-read-control circuit.

The field-switching counter selects the first RD field to be read by adding 1 to the number of step-scan pulses sent to the scan counter synchronizer by the Central Computer System. The total number of pulses received from the Central Computer System indicates the RD field that is to be written on by the Central Computer System. Each time the Central Computer System begins writing on a new field, another step-scan pulse is sent.

The step-scan-counter pulses from the Central

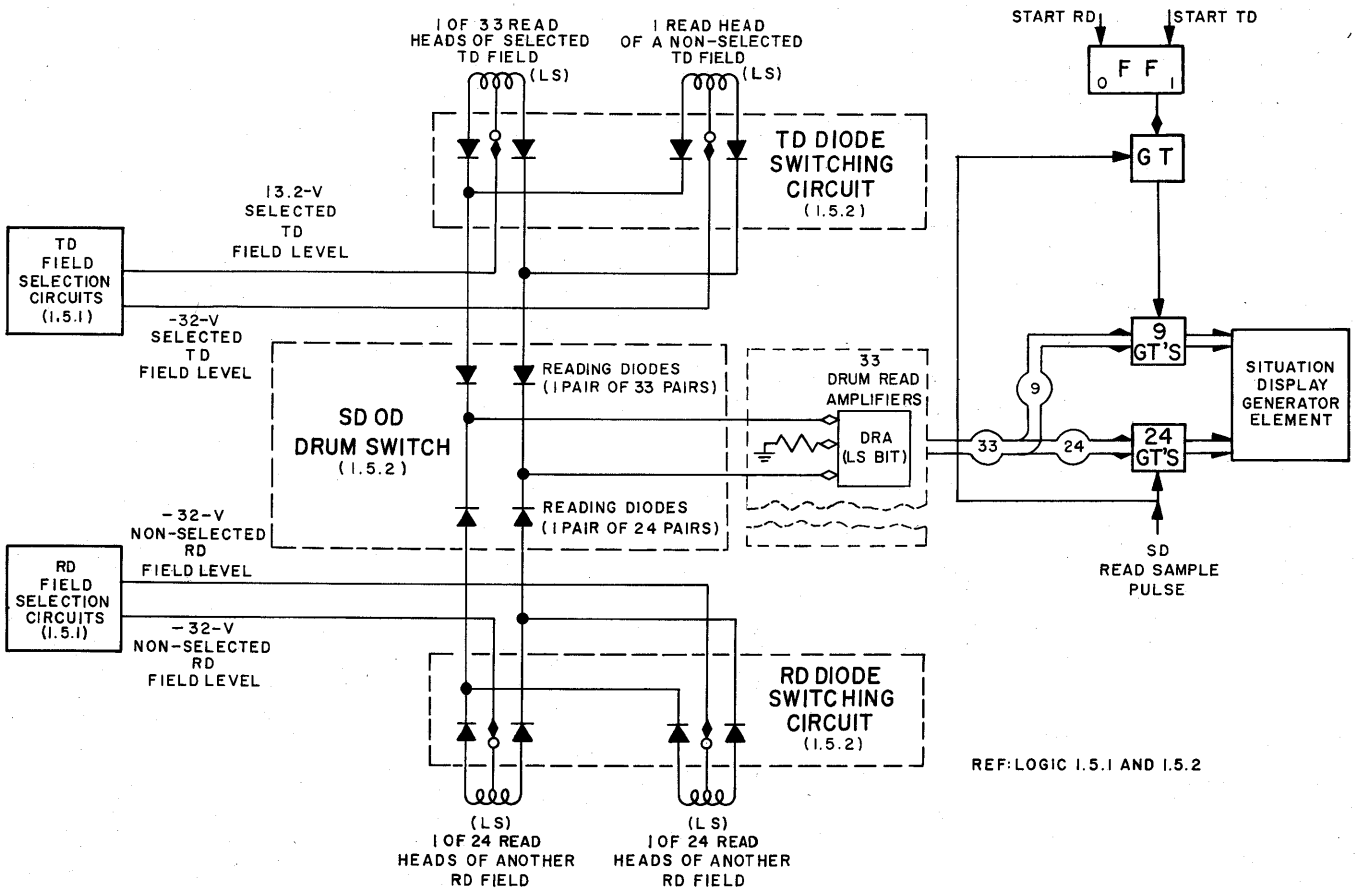


Figure 2–59. Track-Display and Radar-Data-Field-Switching-and-Reading Circuit, Simplified Logic Diagram

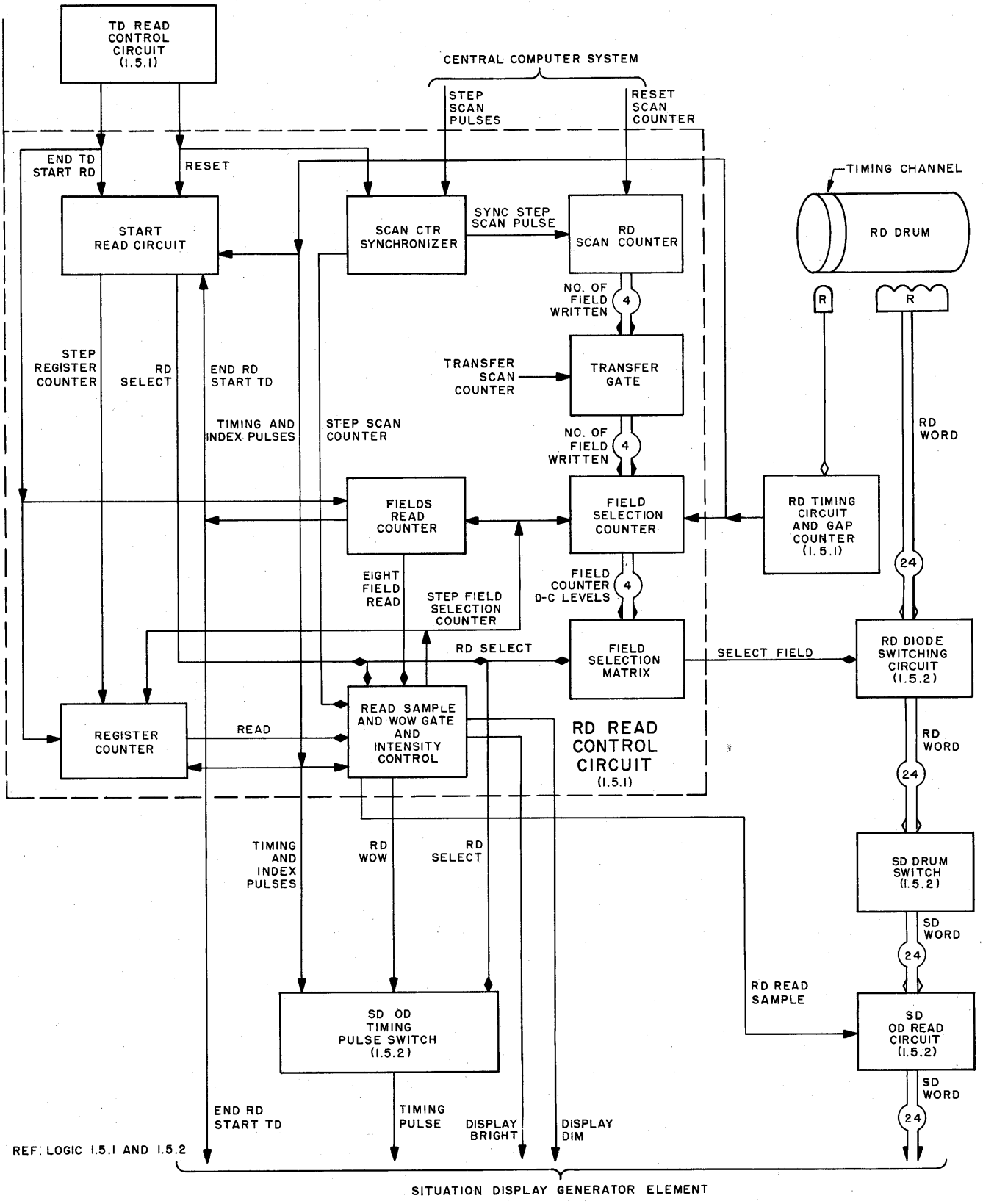


Figure 2–60. Radar Data OD Reading, Block Diagram

Computer System are synchronized with the RD timing pulses in the scan counter synchronizer. The synchronizer is initially cleared by the power-on-reset pulse, which initiates SD OD reading. The synchronized step-scan-counter pulses at the synchronizer output are sent to the scan counter, stepping it until it is set at the number of the field on which the Central Computer System is to write. During TD reading only, the contents of the scan counter (indicating the first field to be read) are transferred to the field-selection counter by a transfer-scan-counter pulse. Thereafter, the field selection counter is stepped by step-field-selection-counter pulses from the read-sample-and-WOW-gate-and-intensity control.

The RD field read first contains the oldest data; the field read last, the most recent data. During the time that the first seven selected fields are read, the read-sample pulses are passed through a gate in the read-sample-and-WOW-gate-and-intensity control to produce display-dim pulses. During the reading of the eighth field, the read-sample pulses are gated to produce display-bright pulses. These pulses are sent to the SDGE. In the generator element, these pulses cause either dimming of the presentation of those fields containing older data or brightening of the field containing the most recent data, depending on which pulse is present.

7.6 RADAR DATA OD READING, CIRCUIT ANALYSIS

Radar data OD reading can be divided into two separate operations, development of the reading pattern and field switching. The circuits used to produce the precessed reading pattern employed by the RD drums are described in 7.6.1. The circuits used to switch from one RD field to the next and the circuits that enable the Central Computer System to select the first RD field to be read during each SD reading cycle are described in 7.6.2.

7.6.1 RD Reading Pattern Development, Circuit Analysis

The OD display element circuits employed to develop the precessed reading pattern used by the RD drum are shown in figure 2–61.

When the Drum System is energized, a power-on-reset pulse is sent through the TD-read-control circuit to the start-read portion of the RD-read-control circuit. This pulse causes conduction in OR's 1 and 2. The outputs of the two OR circuits clear FF's 1 and 2. The first OD index pulse that occurs after the power-on-reset signal is passed in GT 3 by the 0 output of FF 2 to produce a reset-field-selection-counter pulse. The reset-field-selection-counter pulse clears the field-selection counter (as described in 7.6.2).

The RD-read-control circuit components cleared by the power-on-reset-and-index pulse remain in the 0 condition during the period of TD reading and field switching. When reading of the TD drum is completed, the TD read-control circuit produces an end-TD-start-RD pulse (described in 7.4.2). This pulse sets FF 1 to the 1 side and clears the RD register counter and the RD field counter flip-flops. The 1 output of FF 1 passes the next index pulse from the RD-timing-circuit at GT 1 to set FF 2. The 1 output of FF 2 is the RD-select level, which goes to the field-switching circuits (described in 7.6.2), the SD-timing-pulse switch (described in 7.7), and to GT 2. Gate 2 is conditioned to pass OD 2 pulses from OR 4. (The first OD 2 pulse passed is the 13th in the timing channel. This is due to the fact that the first 12 cycles of OD pulses are skipped in the RD-timing circuit.) The OR 4 outputs are called step-register-counter pulses, which go to the register counter.

The register counter is cleared by an end-TD-start-RD pulse (fig. 2–62). Gate 1 is conditioned by the output from OR 2. The first step-register-counter pulse is passed by GT 1 to set FF 1. Successive step pulses continue operating the counter in similar fashion to the counter previously explained in 7.1.1 (see fig. 2–52). AND circuit 1 (fig. 2–60) conducts when the flip-flops are in a 1-0-1 state. The output from AND 1 conditions GT 2 to pass the sixth step-register-counter pulse. This pulse clears the flip-flops, causing AND 2 to conduct. The output from AND 2 is a register-counter-at-0 level.

AND 1 (fig. 2–61) will conduct when the three flip-flops of the register counter are simultaneously in the 1-0-0 state and the RD select level is present. The output from AND 1 goes to GT's 5, 6, and 7. In GT's 5 and 6, the level conditions the passing of OD 4 and OD 1 pulses, respectively, to generate RD WOW (OD 4) and read-sample (OD 1) pulses. The WOW pulse goes to the SD-timing-pulse switch to be transferred to the SDGE. Receipt of this signal informs the generator element that a word will follow from the Drum System. Two and one-half usec later, the RD-read-sample pulse is developed and sent to the SD-read-sample-gate circuit (fig. 2–56) to produce an SD-read-sample pulse. The SD-read-sample pulse goes to the SD-read circuit. In the SD read circuit, it is passed to the SDGE by each 1 bit in the word that is switched by the SD-drum switch at that time (as described in 7.4.2).

The RD-read-control circuit produces a read-sample pulse at the second register (register 1; registers are numbered 0 through 2,047) and skips the next five registers (registers 2 through 6). Another read-sample pulse is produced at the eighth register (register 7). This pattern of reading one register and skipping five is repetitive, continuing for three drum revolutions. At the end of three drum revolutions, all odd-numbered registers on the field have been read. At this time, the

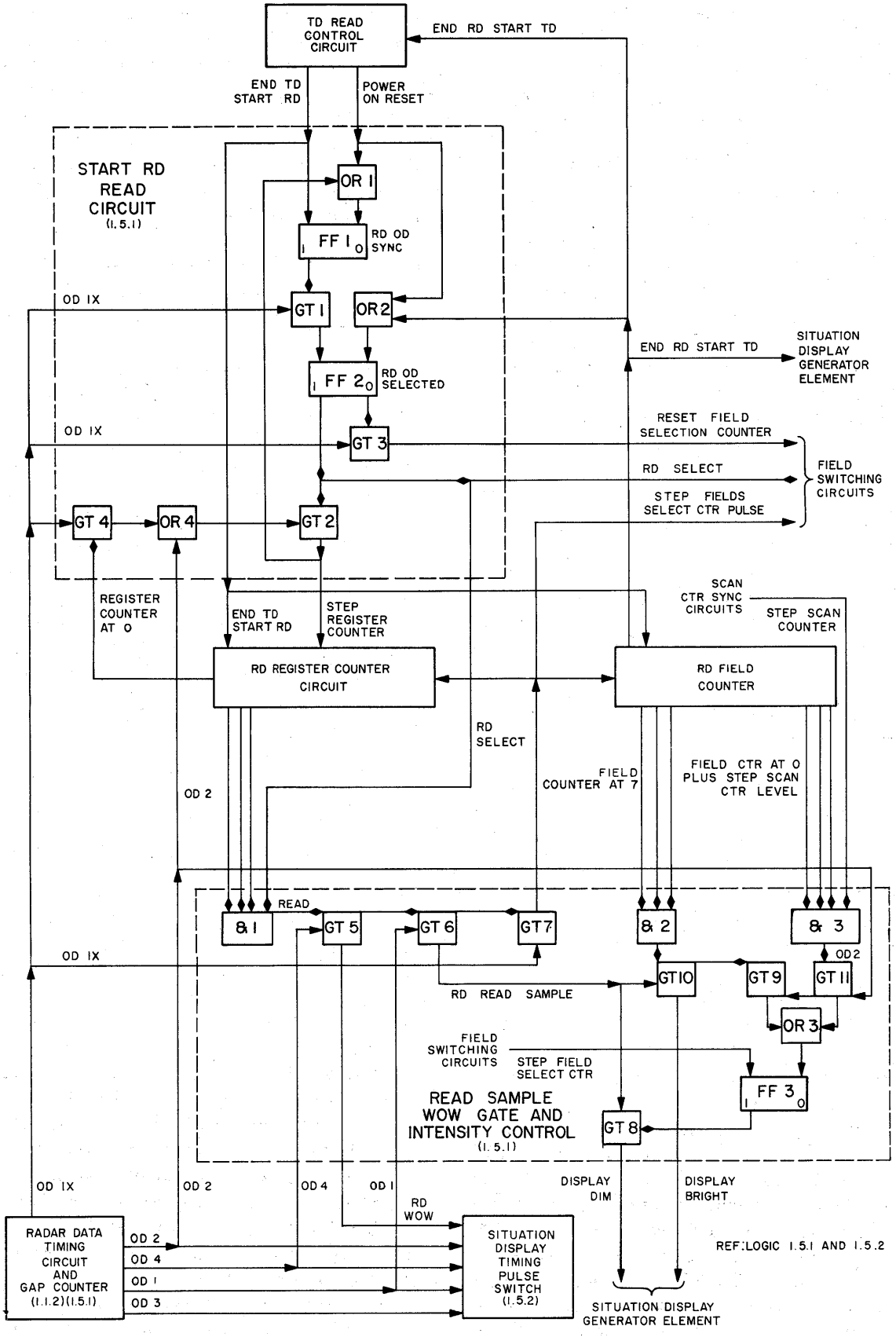


Figure 2–61. Radar Data Reading Pattern Development, Simplified Logic Diagram

OD-index pulse coincides with the register-counter-at-0 level in GT 4 (fig. 2–61). The resulting output goes to OR 4. Conduction in OR 4 produces a step-register-counter pulse at the output of GT 2. The additional step pulse generated at this time precesses the register counter. During the next three revolutions, all even-numbered registers are read. At the end of six revolutions, the step-fields-read-counter level is coincident with the index pulse in GT 7, to produce a step-field-select-counter pulse. The step-field-select-counter pulse clears the register counter and goes to the field-switching circuits.

In the read-pattern-development circuits (fig. 2–61), the step-field select-counter pulse sets FF 3. The resulting 1 output passes the RD-read-sample pulses through GT 8, generating display-dim pulses, which go to the SDGE. While the display-dim pulse is present, RD information is dimmed on the CRT screens.

A branch of the step-field-select pulse goes to the field counter and steps the counter each time the pulse is produced. The counter is a 3-flip-flop, scale-of-8 circuit. At the seventh step-fields-select-counter input, reading of the eighth field begins and the counter flip-flops are all at 1. The three 1 outputs are combined in AND 2 to indicate that the counter is at 7 and the eighth field is being read. The output of AND 2 conditions GT's 9 and 10. Gate 9 passes an OD 2 pulse from the RD-timing circuit to provide conduction in OR 3. Conduction in OR 3 clears FF 3 and prevents the generation of the display-dim pulse. Gate 10 passes read-sample pulses, producing display-bright pulses, which go to the SDGE during the reading of the eighth field. In the generator element, the display-bright pulses cause brightening of the RD information being displayed. This action highlights the display of the information most recently written by the Central Computer System.

It is possible for the flow of information from the Central Computer System to get ahead of the display cycle. Were this to occur, the computer would select for writing the first field in the RD display cycle while it is being read. This would present new information to the Display System in a dim display, whereas new information should be displayed brightly.

In order to prevent confusion at the CRT screens if this occurs, the step-scan-counter level generated in the field selection circuits by the Central Computer System selection is sent to the read-sample-and-WOW-gate-and-intensity control. Occurring as it does when the three flip-flops in the field-read counter are all at 0, it produces conduction in AND 3 to develop a field-counter-at-0-step-scan-counter level. This level passes an OD 2 pulse in GT 11 to cause conduction in OR 3. This clears FF 3. With FF 3 cleared, no display-dim pulse is developed. Since the fields-read counter is not at 7, no display-bright pulse is developed either. Therefore, the SD CRT's do not present any information during the reading of that first field.

The eighth step-fields-select-counter pulse received by the field-counter develops an end-RD-start-TD pulse output. This pulse clears FF 2, goes to the TD-read-control circuit to start reading there, and goes to the SDGE to inform it that TD reading is about to begin.

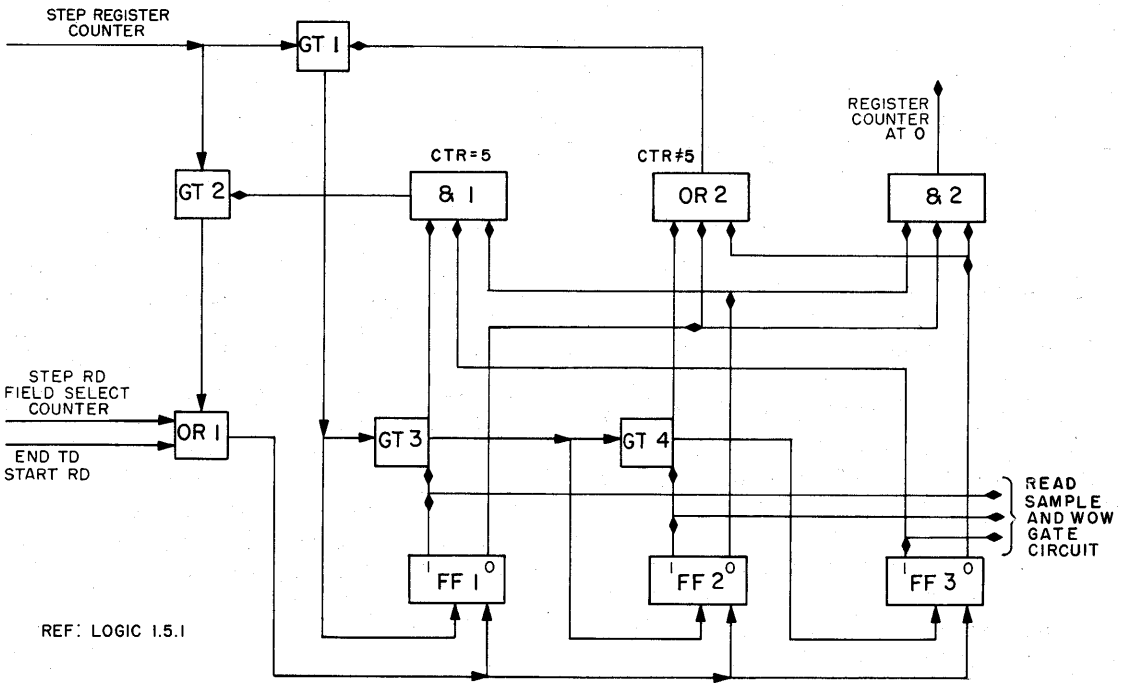


Figure 2–62. Radar Data OD Register Counter, Simplified Logic Diagram

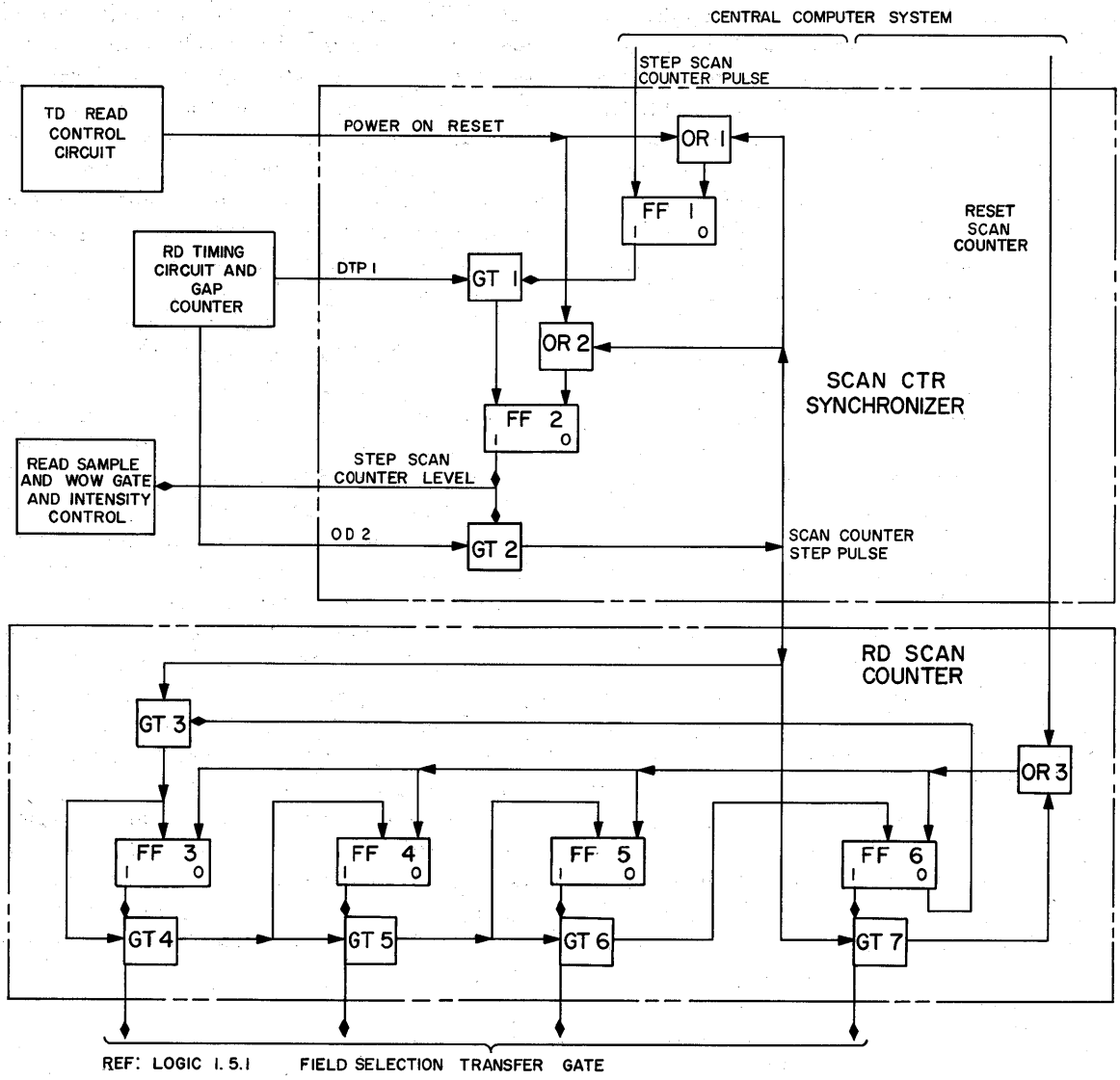


Figure 2–63. Radar Data Circuits for Selection of First RD Field for OD Reading, Simplified Logic Diagram

Thus, only eight of the nine RD fields are read during any one SD reading cycle. The ninth field is written by the Central Computer System during this time.

7.6.2 RD Field Switching, Circuit Analysis

When SD reading is first started, the power-on-reset pulse is sent through the TD-read-control circuit to the RD-step-scan synchronizer (fig. 2–63). In this circuit, which is part of the RD-read-control circuit, OR's 1 and 2 conduct, clearing FF's 1 and 2.

At any time thereafter, the Central Computer System indicates that it intends to write on a new RD field by sending a step-scan-counter pulse to the 1 side of FF 1. The step-scan-counter pulse establishes a 1 level at the output of FF 1 which passes a DTP 1 from the RD-timing circuit.

The passed DTP 1 pulse sets FF 2 to the 1 side, forming a step-scan-counter level. This level goes to the read-sample-and-WOW-gate-and-intensity control to make certain that no data is displayed if the step-scan-counter pulses from the Central Computer System arrive during the reading of the first selected RD field (as described in 7.6.1).

The step-scan-counter level also conditions GT 2 to pass an OD 2 pulse, producing a scan-counter-step pulse. This pulse represents the step-scan-counter pulse synchronized with the operations of the Drum System.

The scan-counter-step pulse is applied to OR's 1 and 2 to clear FF's 1 and 2. Therefore, there is only one scan-counter-step pulse produced by the scan counter synchronizer for each step-scan-counter pulse input.

The scan-counter-step pulse is also applied to the scan counter. The scan counter is a scale-of-9 counter whose basic operation is similar to that of counters previously discussed. When the Central Computer System selects RD field 1 for writing, a reset-scan-counter pulse is sent to the scan counter. In the scan counter, the reset-scan-counter pulse causes conduction in OR 3. Conduction in OR 3 clears all the scan-counter flip-flops. The output of FF 6 establishes a level at GT 3 which passes scan-counter-step pulses. Eight scan-counter-step pulses are counted in the normal fashion. The ninth scan-counter-step pulse is passed, not through GT 3, but through GT 7 by the 1-state level of FF 6 which is established by the eighth step pulse. The ninth pulse, when passed, goes to OR 3 and clears the counter. A cleared counter indicates that RD field 1 has once again been selected by the Central Computer System for a writing operation. The first scan-counter-step pulse counted represents field 2; the second, field 3; and so on. The d-c levels developed at the outputs of the flip-flops of the scan-counter are sent to the transfer gates (fig. 2–64).

A reset-field-select-counter pulse produced in the RD read-pattern-development circuits during TD reading (refer to 7.4.1) sets FF 1 in the field-selection counter (shown in fig. 2–64) and clears the counter. The FF 1 output conditions GT 1 to pass a DTP 4 pulse. The timing pulse is a transfer-scan-counter pulse which goes to GT's 3, 4, 5, and 6 of the transfer gate. Wherever a 1 level from the scan-counter conditions one of these gates, a pulse is sent to an associated flip-flop in the field selection counter, setting it. Thus, the binary

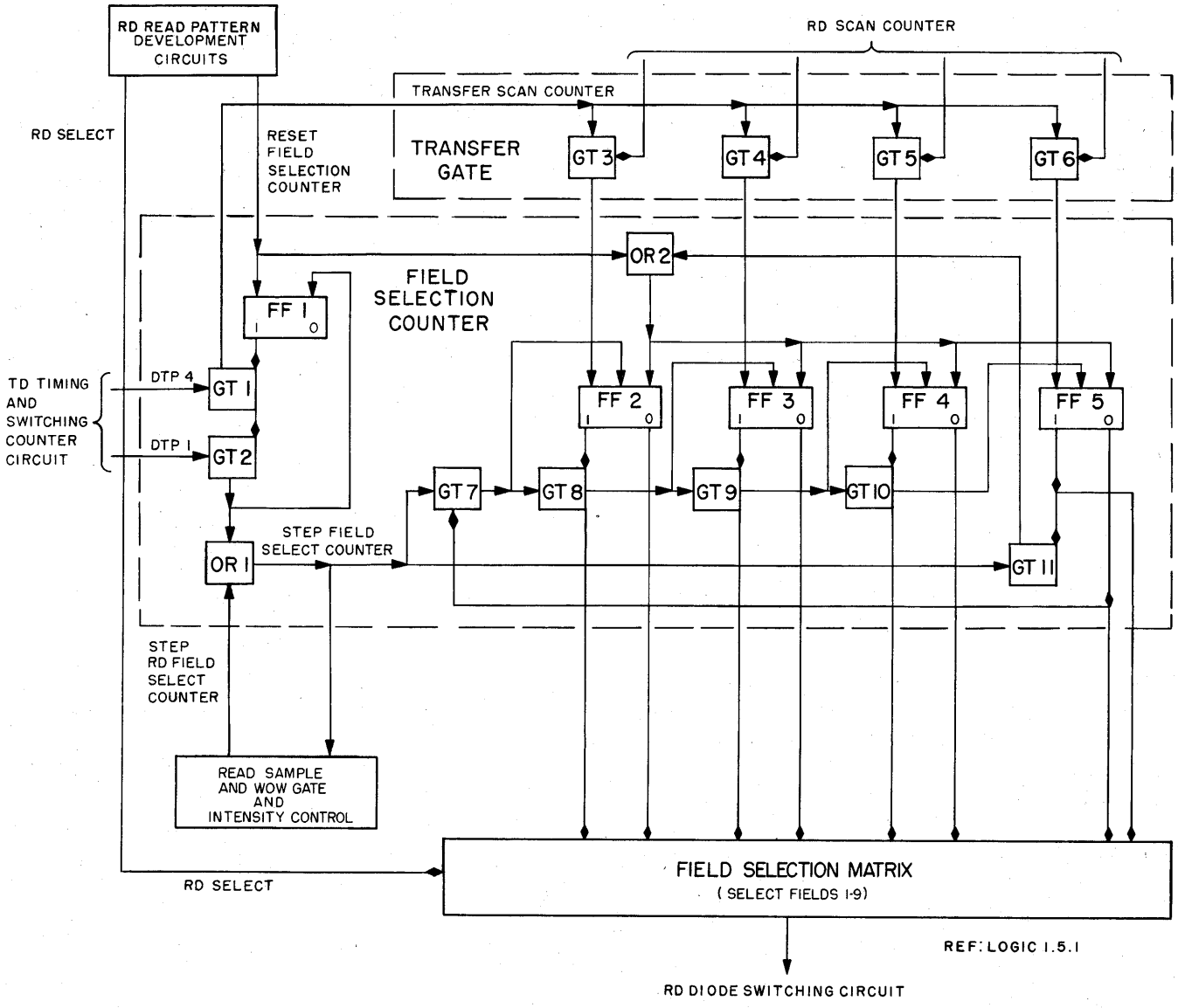


Figure 2–64. RD OD Field Selection Circuit, Simplified Logic Diagram

setting of the scan counter is transferred to the field-selection counter in such a manner that the field-selection counter indicates the field upon which the Central Computer System will write.

The level from FF 1 also conditions GT 2 to pass the first DTP 1 pulse following the DTP 4. This DTP 1 clears FF 1, preventing further production of transfer-scan-counter pulses, and goes to OR 1. OR 1 conducts, developing a single step-field-selection-counter pulse for the field selection counter. As a result, the counter assumes a setting that represents a number that is 1 greater than the setting of the scan counter.

The field-selection counter operates in a manner similar to that of the scan counter. After the initial setting of the field-switching counter by the transfer gate ouput and the DTP 1 step pulse, the counter is stepped by the output of the read-sample-and-WOW-gate-and-intensity control. Each time this control indicates the completion of the reading of a field, it sends a step-field-selection-counter pulse to OR 1 in the field-selection counter. The output of OR 1, thereafter, steps the field-switching counter each time the reading of a field is completed.

The output of the field-selection-counter levels goes to the RD-field-selection matrix. This matrix operates in the same manner as the TD-field-selection matrix (described in 7.4.2) except that levels are available for nine fields instead of six as in the latter matrix.

In order for any of the AND circuits of the field-selection matrix to conduct, an RD-select level from the read-pattern circuits must be present. This signal indicates that the RD drum has been selected for SD reading.

The output of the field-selection matrix goes to the RD diode switching circuit. This circuit is identical in its operation with the TD diode switching circuit, except that the d-c select field levels produce conduction in 24 read heads instead of in 33 (fig. 2–59).

As shown in figure 2–59, the RD-field switch output supplies an alternate input to the SD-drum switch, which in turn feeds the SD-read circuit. The read-sample pulses produced by the read-pattern-development circuits described in 7.6.1 pass the selected RD field contents to the SDGE.

7.7 SITUATION DISPLAY TIMING PULSE SWITCH, CIRCUIT ANALYSIS

The SD-timing-pulse switch of the OD display element is employed to alternately switch RD and TD timing, index and WOW pulses to the SDGE.

The SD-timing-pulse switch is shown in figure 2–65. The drum timing pulses from the TD-timing circuit go to OR 1. The drum timing pulses from the RD-timing circuit go to OR 2. OR's 1 and 2 conduct each time they receive one of the four drum timing pulses. The outputs of OR's 1 and 2 go to GT's 1 and 2, respectively. The drum (RD or TD) being read at a given time has a select level generated in its read-control circuit. This select level goes to the gate pulsed by the drum timing pulses of the selected drum. For example, if the TD drum is being read, the TD-select level goes from the TD-read-control circuit to GT 1.

The gate conditioned by a select level passes the drum timing pulse inputs to OR 3. The OR 3 outputs are thereafter referred to as SD-drum-timing pulses and are sent to the SDGE.

Each select-drum level (when present) conditions a gate which is pulsed by the index pulses of the associated timing circuit. Thus the TD-select level is established at GT 3 during TD reading and the RD-select level at GT 4 during RD reading. The index pulses go to OR 4. The OR 4 outputs are referred to as SD-index pulses and go to the SDGE.

The drum being read at any given time produces a WOW pulse before sending a word into the SDGE.

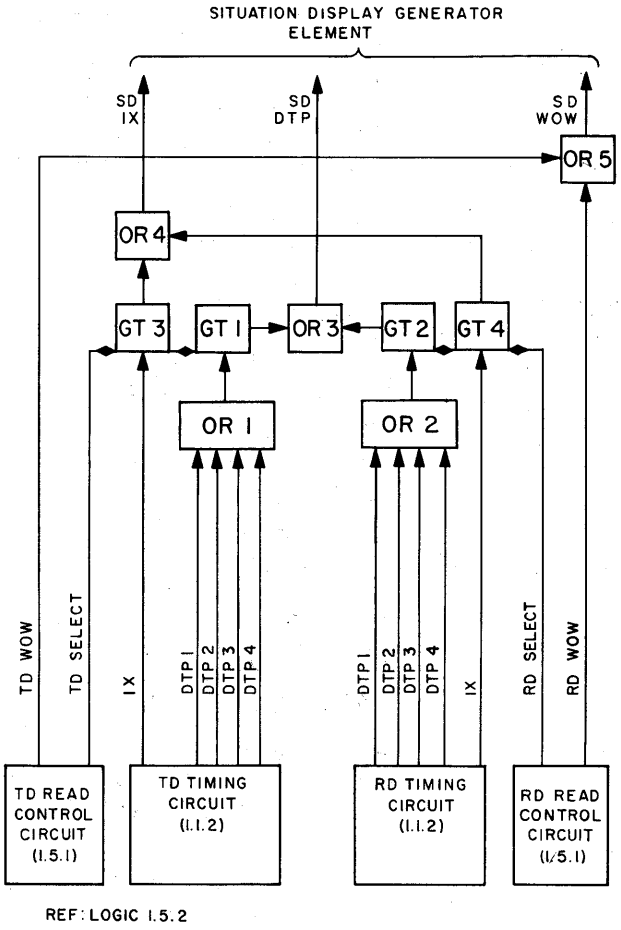


Figure 2–65. SD Timing Pulse Switch, Simplified Logic Diagram

The TD or RD-WOW pulse, whichever is present, produces conduction in OR 5. The OR 5 output is referred to as an SD-WOW pulse and goes to the generator element.

The SD-timing-and-index pulses are used to time the operation of the generator element, and the WOW pulses prepare it to receive the words read from both drums.

CHAPTER 8

INTERCOMMUNICATION FIELDS DATA TRANSFER

The AN/FSQ-7 Combat Direction Central contains two complete Drum Systems and two Central Computer Systems. One Drum and Central Computer System combination actively processes and transfers data. The other combination is in a standby state. When maintenance is to be performed on the active combination, the functions of the active pair are switched to the standby pair. In order to shorten the switching time, intercommunication is maintained between active and standby equipment at all times by means of information exchanges between the intercommunication field in the active Drum System and the standby Central Computer System. This allows data on the current air defense situation to be stored by the standby computer and drums. Intercommunication between Central Computer Systems is also used to enable the standby Central Computer System to check the operation of the active Central Computer System.

The active Central Computer System generates intercommunication data for transfer to the standby system. (Fig. 2–66 illustrates the transfer of data from the active to the standby Central Computer System.) The CD circuits in the active Drum System transfer this intercommunication data from the active Central Computer to the intercommunication field of the active Drum System. The intercommunication OD circuits of the active Drum System read the active intercommunication field at the instruction of the standby Central Computer. This IC information is then transferred to the standby Central Computer via the CD circuits of the standby Drum System.

Throughout this Chapter, the active system is referred to as system A, the standby system as system B.

8.1 INTERCOMMUNICATION FIELD CD WRITING

The CD circuits in the active Drum System transfer IC data from the active Central Computer System to the active IC field by address control. The use of address control in CD writing on the active IC field enables the standby Central Computer System to know exactly where pertinent data has been placed. This ensures the transfer of the correct data from the active to the standby Central Computer System. (Refer to 4.3 and 4.4 for a detailed description of address-controlled transfer operations.)

8.2 INTERCOMMUNICATION OD READING, BLOCK DIAGRAM ANALYSIS

Reading of the IC field in Drum System A is performed under the direction of Central Computer System B and Drum System B. Figure 2–67 is a block diagram of this reading operation.

A deselect pulse is sent by Central Computer System B to the CD-read-write-control cricuit in Drum System B. Central Computer System B sends index interval bits to Drum System B field selection circuits, where they are decoded to produce the IC-other select level. The CD-read-write-control circuit, in turn, sends a

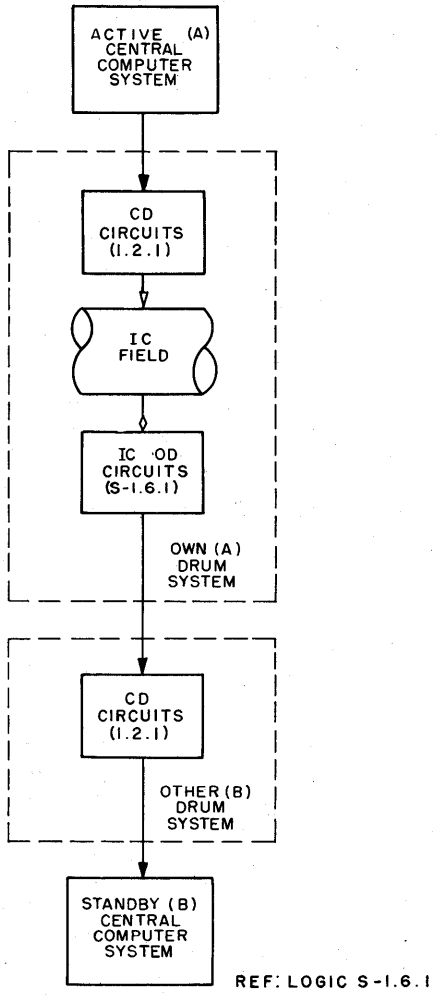


Figure 2–66. Intercommunication Information Transfer, Block Diagram

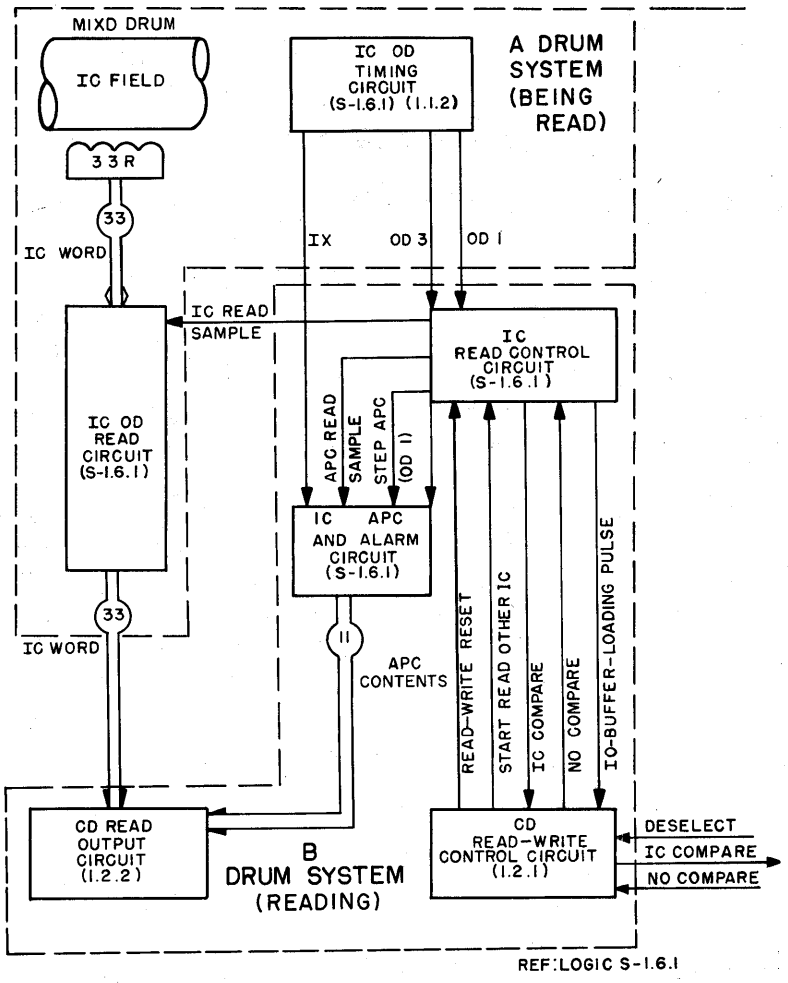


Figure 2–67. Intercommunication-OD Circuits, Block Diagram

read-write-reset pulse to the IC-read-control circuit in Drum System B.

The read-write-reset pulse and the IC-other select level prepare the IC-read-control circuit to receive the start-read-other-IC pulse from Central Computer System B via the B Drum System CD-read-write-control circuit.

The start-read-other-IC pulse causes the B system IC-OD-read-control circuit to produce an angular-position-counter readout pulse. The angular-position-counter-readout pulse gates the contents of the IC angular-position-counter to the CD-read-output circuit (Drum System B), from which it goes to Central Computer System B. This information represents an address on the IC field of the A system MIXD drum. The contents of the IC-angular-position-counter are determined by the number of step-angular-position-counter pulses received from the IC-read-control circuit, after the index pulse from the A system IC-OD-timing circuit has cleared the counter. The step-angular-position-counter pulses are actually MIXD OD 1 pulses from the A system MIXD drum that pass through the B system read-control circuit. The angular-position-counter circuit output is sent to the B system CD-read-output circuit. At the same time, the B system IC-read-control circuit sends an IC-compare pulse to Central Computer System B via the CD-read-write-control circuit in Drum System B.

The IC-compare pulse from the B system IC-read-control circuit causes Central Computer System B to compare the angular position counter contents from Drum System A with 11 bits in the Central Computer System B comparison circuits. The comparison circuit bits represent the desired address on the drum in Drum System A. Until comparison is successful, Central Computer System B sends no-compare pulses back to the B system IC-read-control circuit.

When the no-compare pulse is not returned, IC-read-system pulses are developed by the B system IC-read-control circuit. The read-sample pulses go to the A system IC-OD-read circuit, where they gate the intercommunication word on the A system MIXD drum to

the CD-read-output circuit of Drum System B. The IC-read-sample pulses continue to be developed until Central Computer System B produces a disconnect pulse, which enters the IC-read-control circuit as a read-write-reset pulse.

With each word read into Central Computer System B in this manner, the IC-read-control circuit sends an IO-buffer-loading pulse to the B system CD-read-write-control circuit for transfer to Central Computer System B. Central Computer System B counts the IO-buffer-loading pulses to determine when it has received the desired number of words. Timing and index pulses from Drum System A are used by the B system IC-read-control circuit to time and control reading operations. The IC-OD index pulse is used in intercommunication field reading only. The OD 1 and OD 3 pulses are standard pulses generated by the A system MIXD timing circuits.

8.3 INTERCOMMUNICATION OD TIMING CIRCUIT, FUNCTIONAL DESCRIPTION

Timing pulses from the MIXD drum of the active Drum System are used in the transfer of data from the active to the standby Drum System. Drum timing pulses are transmitted from the A system drum being read to the intercommunication and the IC angular-position-counter control of Drum System B doing the reading (fig. 2–68). The read-sample pulse is generated in the IC read controls of Drum System B.

The timing pulses from Drum System A used in Drum System B in the transfer of IC data are the OD 1 and OD 3 pulses derived from the MIXD drum timing circuits, and an OD index pulse generated for use with the IC field by the IC OD timing circuit (fig. 2–68). The OD index pulse for the IC field is derived from an additional read head mounted on the index channel of the MIXD drum. The read head is energized by the 1 bit in the index channel and causes the drum read amplifier to produce a wide pulse at GT 1 that coincides with the OD 3 timing pulse from the MIXD timing circuit. The wide pulse, therefore, acts as a conditioning level and produces the OD index pulse at OD 3 time.

In Drum System B, the index pulse clears the IC-angular-position-counter-and-alarm circuit. The OD 1 and OD 3 timing pulses go to the IC-read-control circuits and the IC-angular-position-counter-and-alarm circuit. The uses of both OD 1 and OD 3 pulses in the IC read control and IC read circuits are discussed in 8.4.

8.4 INTERCOMMUNICATION OD READING CIRCUITRY, FUNCTIONAL DESCRIPTION

8.4.1 IC OD Read-Control Circuit

The OD reading of the intercommunication field in Central Computer System A is performed under the control of Central Computer System B. The CD-read-write-control circuit in Drum System B sends a read-write-reset pulse to the B system IC-read-control circuit (fig. 2–69).

The read-write-reset pulse causes conduction in OR's 1, 2, and 3, clearing FF's 1, 2, and 3. Clearing the intercommunication-read-control circuit flip-flops prepares the circuits to receive a programmed start-read-other-IC pulse from the CD-read-write control circuit of Drum System B.

The start-read-other-IC pulse sets FF 1 in the B system IC-read-control circuit. The 1-state output of FF 1 conditions GT 1 to pass an OD 1 pulse from the MIXD timing circuit of Drum System A, synchronizing the instruction pulse from the B system with the timing cycle of the A system the gated OD 1 pulse sets FF 2. the resulting FF 2 output conditions GT 2 to pass an OD 3 pulse from the MIXD timing circuit of Drum System A.

The GT 2 output goes to the CD-read-write-control circuit of Drum System B as an IC-compare-pulse and to the IC-angular-position-counter-and-alarm circuit (8.4.2) as a readout APC pulse.

The IC-compare pulse and the counter setting of the IC-angular-position-and-alarm circuit are sent to Central Computer System B. The counter setting is compared with a programmed address in the circuits of Central Computer System B. If the two addresses do not compare, Central Computer System B sends a no-compare pulse to the CD-read-write control of Drum System B within 1.1 usec. The CD-read-write-control circuit of system B immediately transfers the no-compare pulse to the IC-read-control circuit. The no-compare pulse produces conduction in OR 3, clearing FF 3.

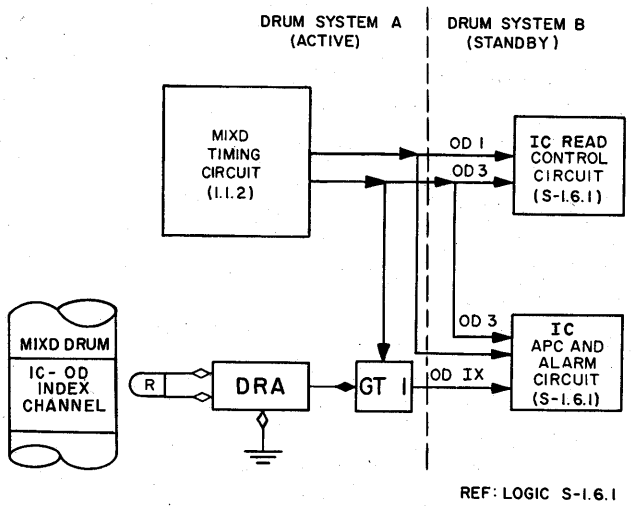


Figure 2–68. Intercommunication-OD-Timing Circuit, Simplified Logic Diagram

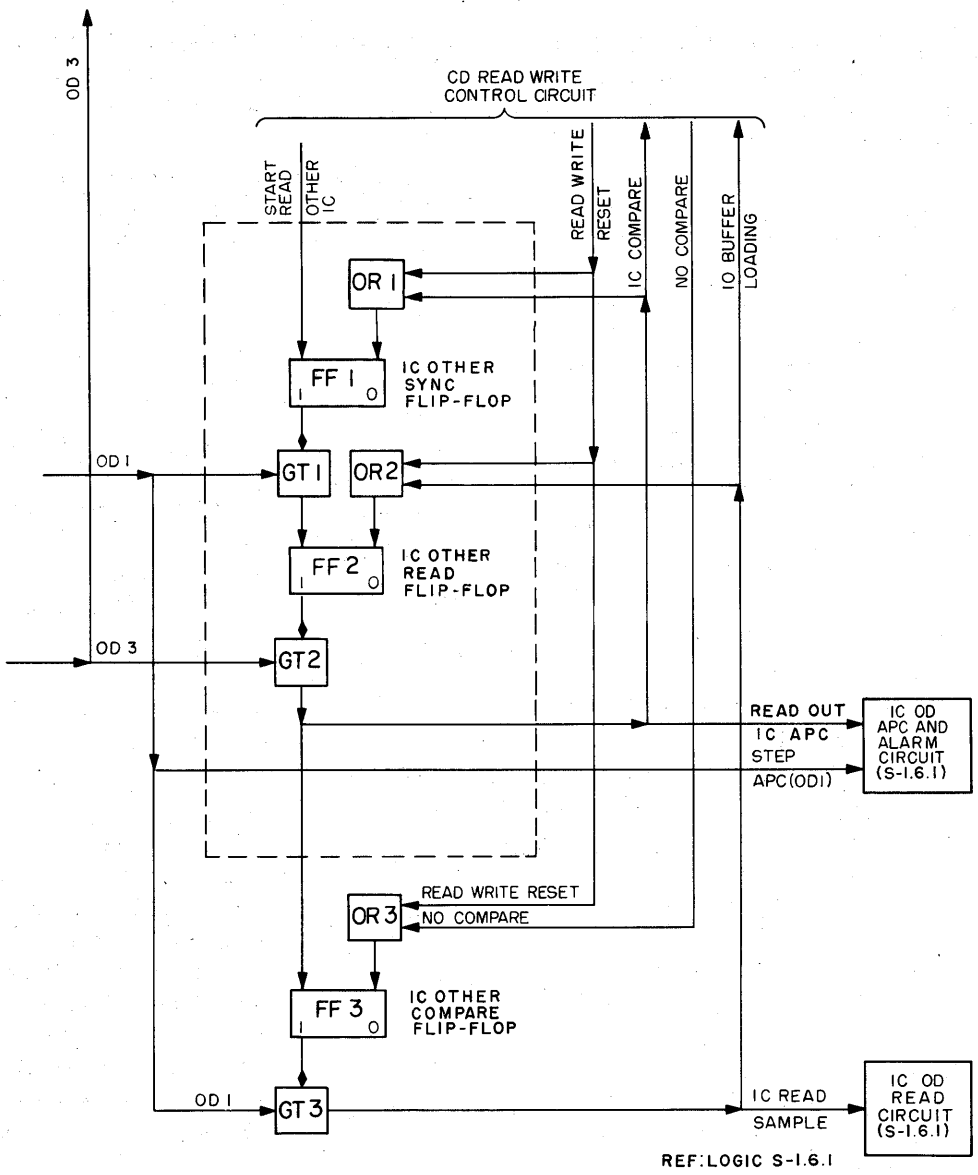


Figure 2–69. Intercommunication-Read-Control Circuit, Simplified Logic Diagram

Conversely, if the comparison is successful, the no-compare pulse is not developed and FF 3 remains in the 1 state, where it has been placed by the output of GT 2. With FF 3 in the 1 condition, GT 3 is still conditioned when the next OD 1 pulse arrives. The GT 3 output pulse goes to the A system IC-OD-read circuit as an IC-read-sample pulse and to the CD-read-write-control circuit of Drum System B as an IO-Buffer-loading pulse. The IO-buffer-loading pulse also clears FF 2 in the IC-read-control circuit by producing conduction in OR 2. With FF 2 cleared, no further GT 2 outputs can be produced until the next start-read-other-IC pulse is received from the CD-read-write-control circuit of Drum System B.

The IO-buffer-loading pulses are transferred to Central Computer System B by the CD-read-write-control circuit of Drum System B to be counted. Counting the IO-buffer-loading pulses enables Central Computer System B to determine the number of IC-read-sample pulses and, therefore, the number of words transferred by the A system IC-OD circuit. When the number of words received represents the total number of words specified by the Central Computer System B program, a read-write-reset pulse is produced which stops the IC-OD reading operation by clearing FF 3.

Figure 2–70 is a chart that summarizes the sequence of events in the OD reading of the IC field.

8.4.2 IC-Angular-Position-Counter-and-Alarm Circuit

The IC-angular-position-counter-and-alarm circuit is similar to the other angular-position-counter-and-

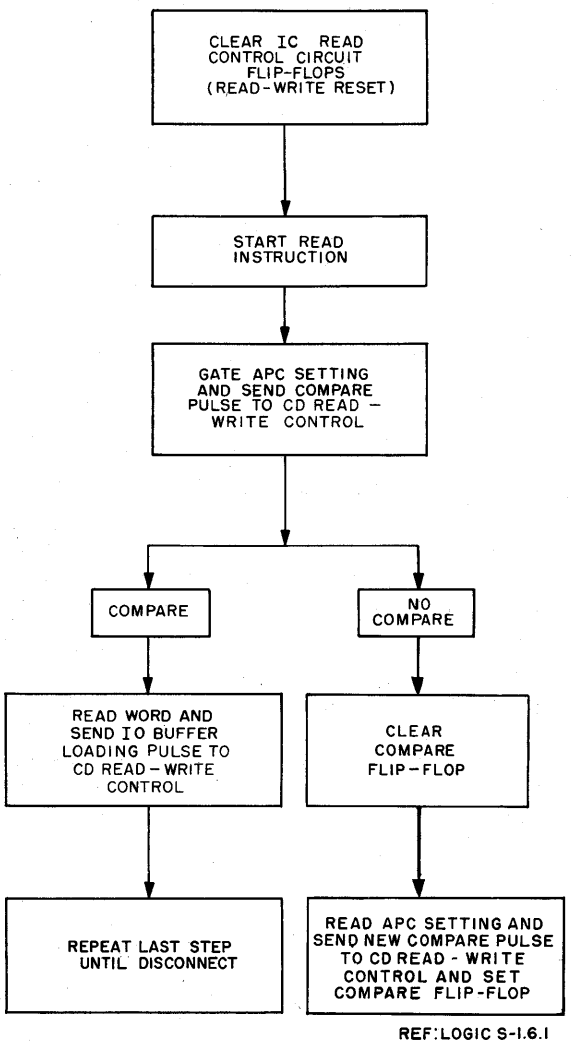


Figure 2–70. Sequence of IC Field Reading Operations

alarm circuits used in the Drum System. The only difference is that the IC-APC is stepped by OD 1 pulses and the APC check flip-flop is set by OD 3 pulses. The operation of a typical angular-position-counter-and-alarm circuit is discussed in detail in 4.4.1.

8.4.3 IC-OD Read Circuit

The IC-read-sample pulses from the B system IC-

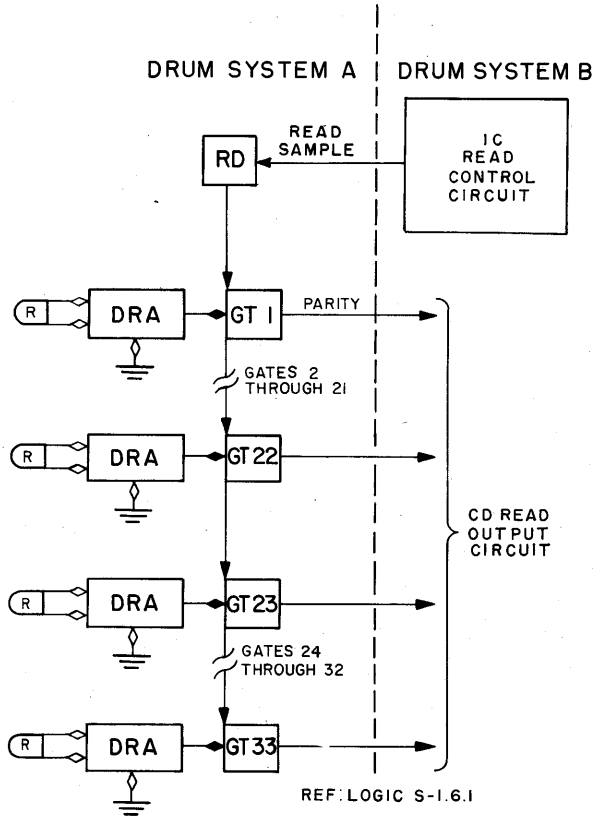


Figure 2–71. Intercommunication-OD-Read Circuit, Simplified Logic Diagram

read-control circuit are amplified by the register driver and applied to GT's 1 through 33 of the IC-OD-read circuit in Drum System A (fig. 2–71). Each gate is connected to a read head via a drum read amplifier. If a head reads a 1 bit on the drum surface, the drum read amplifier detects it and applies it to the gate to which it is connected as a conditioning level. When the read-sample pulse is received at gates that are so conditioned, a pulse is sent to the CD-read-output circuit in Drum System B. The outputs of the 33 gates then represent the word that has been on the drum. The absence of a pulse output from any of the gates indicates the 0 bits in that word. The CD-read-output circuit of Drum System B transfers the words received in this manner into Central Computer System B.

CHAPTER 9
MAIN DRUM TESTING

This chapter describes the theory of operation of the computer-drums loop-test circuits, the manual-drum-test circuits, the manually initiated timing-rewrite-and-erase controls, and the drum-motor-control circuitry.

The computer-drums loop-test circuits enable the Central Computer System to exercise control over the OD circuits as well as the CD circuits of the Drum System. Information written on the CD side of the drums by the Central Computer System is read from the OD side by the Central Computer System through a loop which bypasses the Output and Display Systems. Similarly, information is written on the OD side of the drums through a loop which bypasses the Input System and is read by the Central Computer System on the CD side. Both test loops are formed by means of computer-drums loop-test circuits. With both OD and CD data available to the Central Computer System, they are compared to ensure that storage by, and transfer through, the Drum System have not changed their content.

Special circuits in the Drum System enable maintenance personnel to perform manual checks and tests on Drum System circuits. These tests, known as manual tests, provide a way of localizing most malfunctions to a specific circuit, channel, pluggable unit, or circuit component. The tests are conducted from the test door on unit 21 and involve Drum System circuitry only. Checks on every circuit in each of the drum operating elements and on some circuits of the computer test element can be performed.

The drum timing-rewrite-and-erase circuits are manually activated circuits which erase all magnetic flux on any drum and automatically rewrite the timing and index channels of that drum.

The drum motor-control circuits control the manual starting and stopping of any or all of the six drums.

9.1 COMPUTER-DRUMS LOOP TEST CIRCUITS

In its operation as an intermediate storage device between the Central Computer System and external systems, the Drum System does not perform computations. Testing of all circuits of the Drum System by external means is therefore necessary. It is desirable that such tests be performed by the Central Computer System. Computer-drums loop-test circuits enable the Central Computer System to perform these tests without any change in Central Computer System logic by providing access to Drum System circuits not normally controlled by Central Computer System programs. In the paragraphs that follow, the computer-drums loop-test circuits are called computer-test circuits, and the tests performed through these circuits are referred to as computer tests. These tests are also known as loop tests or system tests. The logic for the computer-test circuits is shown in detail on logic drawings 1.8.1 and 1.8.2.

This paragraph describes the theory of operation of the computer test circuits of the Drum System. The computer-test mode of operation serves to provide a thorough check, not only of the Drum System itself, but also of its interaction with the Central Computer System.

Two basic types of computer tests are performed: one for fields that are written on the CD side of the drums and read on the OD side (SD, DD, and OB fields); and one for fields that are written on the OD side of the drums (MI, GFI, LRI, and XTL fields). Since there is no OD operation in auxiliary memory, no computer tests are performed on those fields.

In both types of computer tests, special programming is used by the Central Computer System. The specific field to be tested (or, in the case of the display fields, the specific tests to be performed) is selected. An operational instruction which normally cannot be performed on the CD side of the drums is then originated. This instruction is sent with the field test selection to a computer-test-controls circuit via a CD-read-write-control circuit and the CD-selection-register-and-selection decoder (fig. 2—72).

If a read pulse is programmed with the selection of an OD reading field, a computer-test-controls circuit provides the control signals required by the selected OD-read circuit to read that field (OB, SD, or DD). The computer-test-controls circuit transfers the data through the computer-test-read switch to OR circuits which feed the Central Computer System. This enables the Central Computer System to compare data read on the OD side of the drums with data written on the CD side.

To prevent reading on the CD side during the transfer operation, control signals to the CD read equipment are stopped; the CD read equipment is disabled when the control signals are not present.

If a write pulse is programmed, an OD writing field is selected, and the computer-test-controls circuit

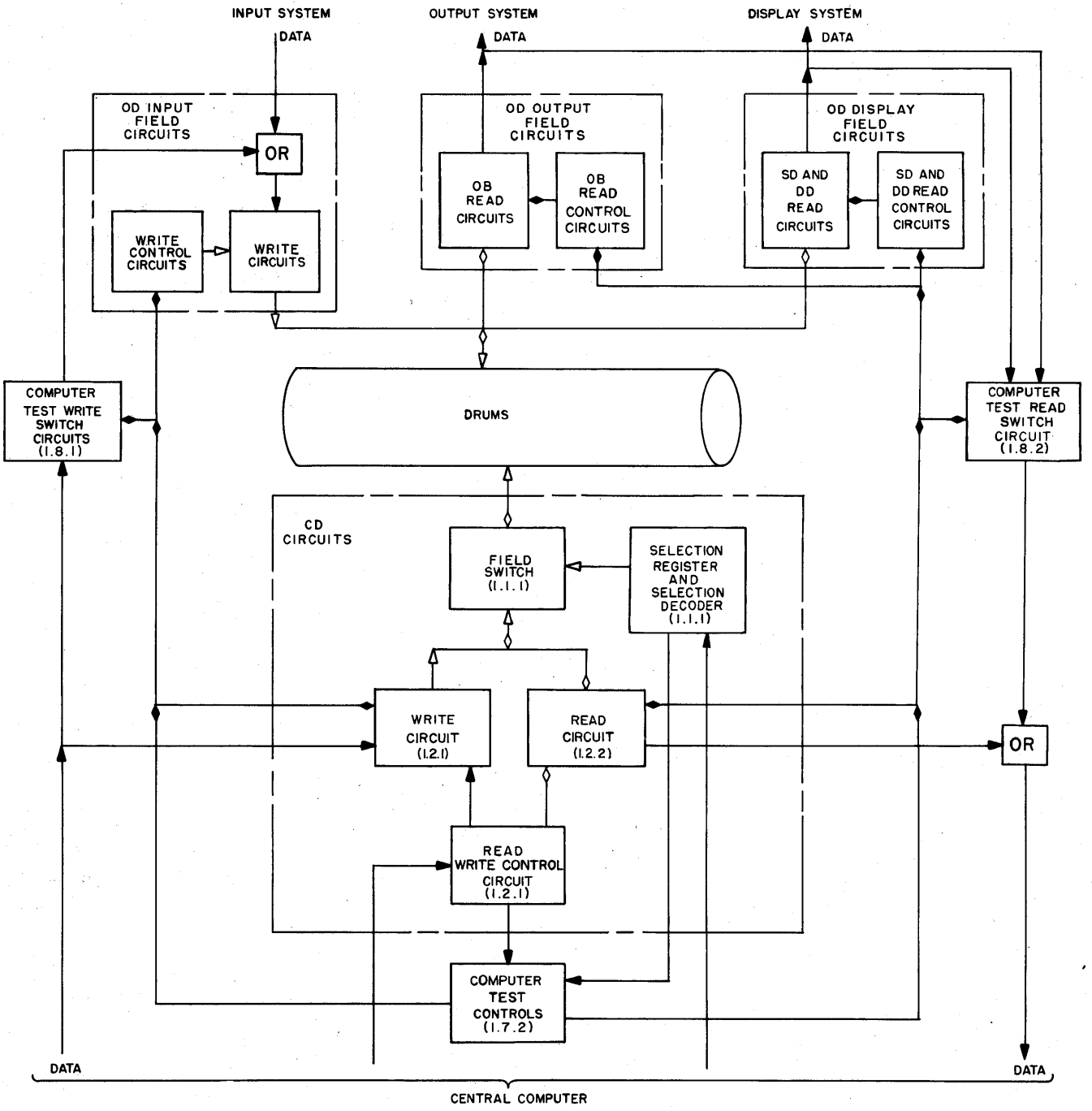


Figure 2–72. Computer-Drum Loop Test Paths, Block Diagram

conditions the computer-test-write-switch circuits to transfer information from the Central Computer System into the selected OD-write circuit. The computer-test-controls circuit then conditions the selected OD-write control circuits to write the information on the drum.

Writing on the CD side of the drum during OD writing is prevented by the absence of a CD-write pulse. Information transfer from the Input System to the OD-write circuit is stopped because of the absence of the necessary control signals.

The special OD read and OD write loops provided by the computer-test circuits enable the Central Computer System to control operations on both sides of the drums. This makes it possible to compare words read with words written, to make certain that no change has occurred during the transfer.

9.1.1 Input Field Computer Test

Input field computer-test circuits permit the Central Computer System to write programmed test words on the OD side of the drums. The test words are read afterward on the CD side of the drums and compared in the Central Computer System with the written test words to see whether any change has occurred in the transfer.

The circuits of the input fields of the Drum System normally write Input System information on the OD side of the drum fields. During computer tests on these fields, a test signal path is provided which allows the Central Computer System to write on the OD side of the drum fields. In the performance of computer tests, the computer-test-controls circuit is first conditioned by a test level from the manual-drum-tester circuit (fig. 2–73). To initiate a writing operation on the OD side of the drums, the Central Computer System first sends a deselect pulse to the CD-read-write-control circuit. This pulse clears flip-flops in the CD-read-write-control circuit and, at the same time, is converted into a read-write-reset pulse. The read-write-reset pulse clears flip-flops in the computer-test-controls circuit and in the selected OD-status-control circuit. The read-write-reset pulse is converted in the OD-status-control circuit into a write-register-reset pulse which clears the selected OD-write register. The computer-test signal path is now ready for programmed operating instructions from the Central Computer System.

A Central Computer System instruction, in the form of six index-interval pulses, enters the CD-selection circuit, causing the generation of a d-c test-select level. When applied to the computer-test-controls circuit, this level determines which field is selected for test. A start-write pulse from the Central Computer System goes to the computer-test-controls circuit via the CD-read-write-control circuit. In combination with the test-select level the start-write pulse results in the formation of the OD-drum-test-write level. This level goes to the computer-test-write-switch circuit and conditions it to pass data from the Central Computer System to the OD-write registers. An IO-register-to-write-

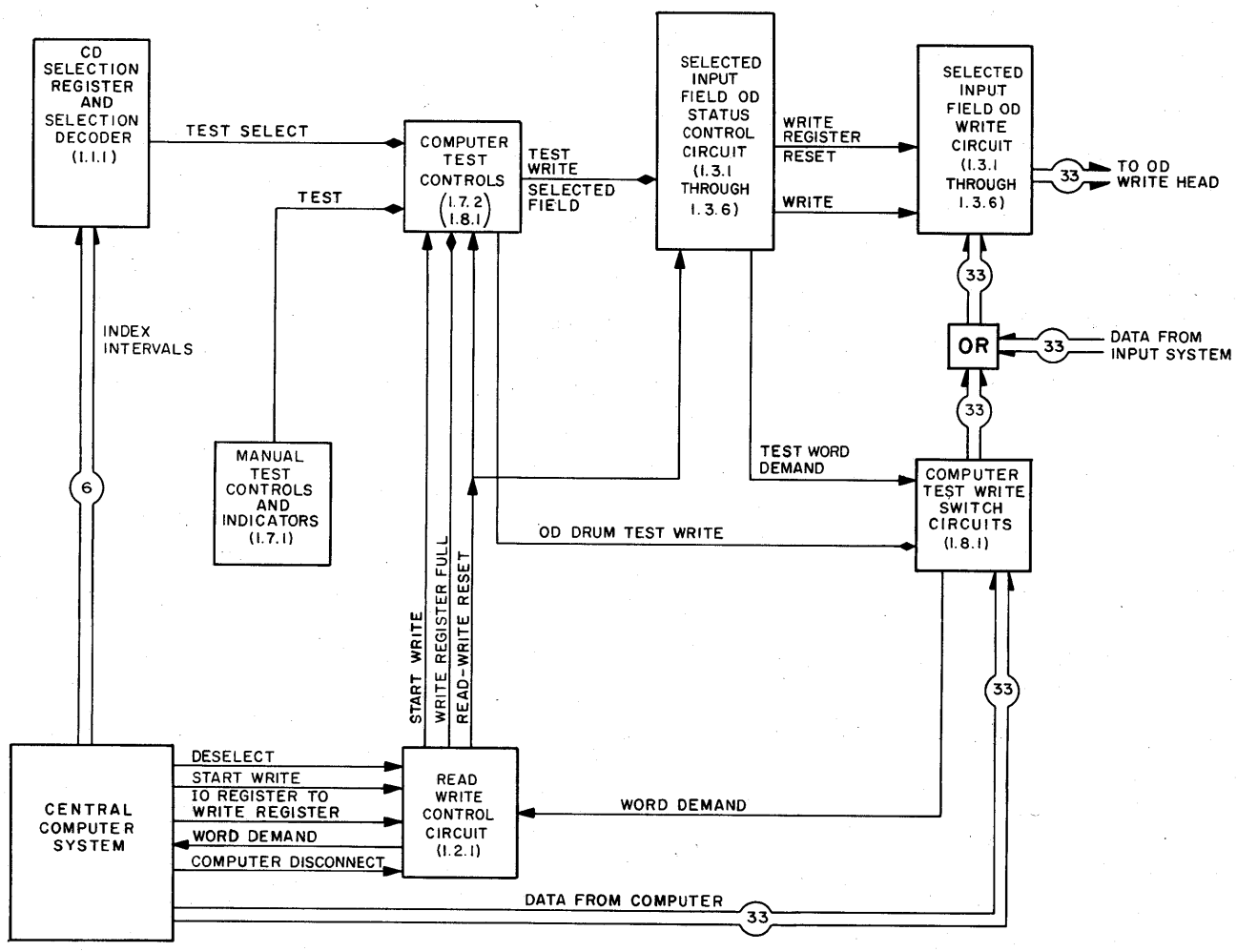


Figure 2–73. Computer Test of Input Fields, Block Diagram

register pulse from the Central Computer System informs the CD-read-write-control circuit that a word has been transferred from the Central Computer to the computer-test-write-switch circuits and, therefore, to the selected OD-write register. The pulse produces a write-register-full level which is sent to the computer-test-controls circuit. On receiving the write-register-full d-c level, the computer-test-controls circuit generates the test-write-selected-field level which conditions operations in the status-control circuit of the selected field.

Sensing of an empty register by the selected status-control circuit produces a d-c level, which, when combined with the test-write-selected-field level, causes the production of a write pulse. The write pulse goes to the selected OD-write register. The word in the selected OD-write register is written on the drum, and the register is cleared in preparation for the next word. At the same time that the write register is cleared, a test-word-demand pulse is sent to the CD-read-write-control circuit via the computer-test-write switch to be converted into a word-demand pulse. The word-demand pulse goes to the Central Computer System to request another word. When all words programmed by the Central Computer System have been written, a computer-disconnect pulse from the Central Computer System clears the control circuits and write registers, stopping the test.

9.1.2 Input Fields Computer Test, Circuit Analysis

Circuits of the Drum System input fields are normally used by the Input System to write on the OD side of the drums. When computer tests are performed on the input fields, a test signal path is provided which allows the Central Computer System to write on the OD side of the drums.

Before a computer test can be performed on the input element, a +10-volt d-c test level is supplied to the computer-test-controls circuit. This level is produced by setting the TEST-OPERATE switch on the maintenance console to the TEST position and the MANUAL TEST-COMPUTER TEST-OPERATE switch on the unit 21 test door to the COMPUTER TEST position (fig. 2–74).

During test procedures, INVERTER 1 is cut off by the presence of the test level. This removes the operate level which goes to the status-control circuit during normal operation.

The test is performed as follows: a deselect pulse is sent from the Central Computer System to OR 1 in the CD-read-write-control circuit. The OR 1 output is the read-write-reset pulse which clears FF's 1 and 3 in the computer-test-controls circuit. It also goes through OR 2 to clear FF 2 in the CD-read-write-control circuit.

The test level, fed through the two test switches, conditions GT 1 to pass the read-write-reset pulse to the selected OD-status-control circuit as the computer-test-reset pulse. (This pulse is described later.)

Instructions from the Central Computer System, in the form of index-interval pulses, produce normal field selection in the CD-selection circuits. The CD-selection circuits produce the test-select-OD-input-field level which is sent to AND's 1 and 3 in the computer-test-controls circuit. A start-write pulse from the Central Computer System is also sent to the computer-test-controls circuit and FF 1. The addition of the 1 output of FF 1 to the test level and the test-select-OD-input field level causes AND 1 to form the test-write-select-drum-OD level. The test-write-select-drum-OD level goes to the computer-test-write-switch circuit and also provides one of the conditions for conduction in AND 2.

Flip-flop 2 in the CD-read-write-control circuit receives the IO-register-to-write-register pulse from the Central Computer System. The IO-register-to-write-register pulse informs the CD-read-write-control circuit that a word has been transferred to the Drum System. A CD-write-register-full level is developed by FF 2 and sent to AND 2 in the computer-test-controls circuit. The Central Computer System word is stored in the CD write register and, as will be seen, in all five OD write registers. In AND 2, the CD-write-register-full level is combined with the test level and the test-write-select-drum-OD levels to form the test-write-select-drum level. Since GT's 2 and 3 are now both conditioned, the next OD index pulse from the selected timing circuit is passed to set FF 3 to the 1 side. The output of FF 3 is added in AND 3 to the test level and to the test-select-OD-input-field level, forming the test-write-selected-field level, which is sent to the selected OD-status-control circuit.

In this selected OD-status-control circuit (shown in fig. 2–75), a computer reset-write-register pulse clears the write register flip-flops of the selected OD-write circuit. Thereafter, the Central Computer System places a word in the write register.

As the drum rotates, the first empty register is indicated by the detection of a 0 bit in the OD status channel of the selected OD-status-control circuit. When a 0 bit rather than a 1 bit is detected, the read circuit cannot condition GT 1 in time for this stage to pass the OD 1 pulse to FF 1. Flip-flop 1, which has been cleared by the preceding OD 4 pulse, remains cleared. The O-state output of FF 1 conditions GT 2 to pass the next OD 3 pulse. This pulse is fed to both GT 3 and FF 2. In normal operation, the operate d-c level conditions GT 3 to pass the OD 3 (drum-demand) pulse which is fed to the associated input circuits of the Input System. The Input System then feeds a normal data-available pulse to FF 3. In the absence of the drum-demand

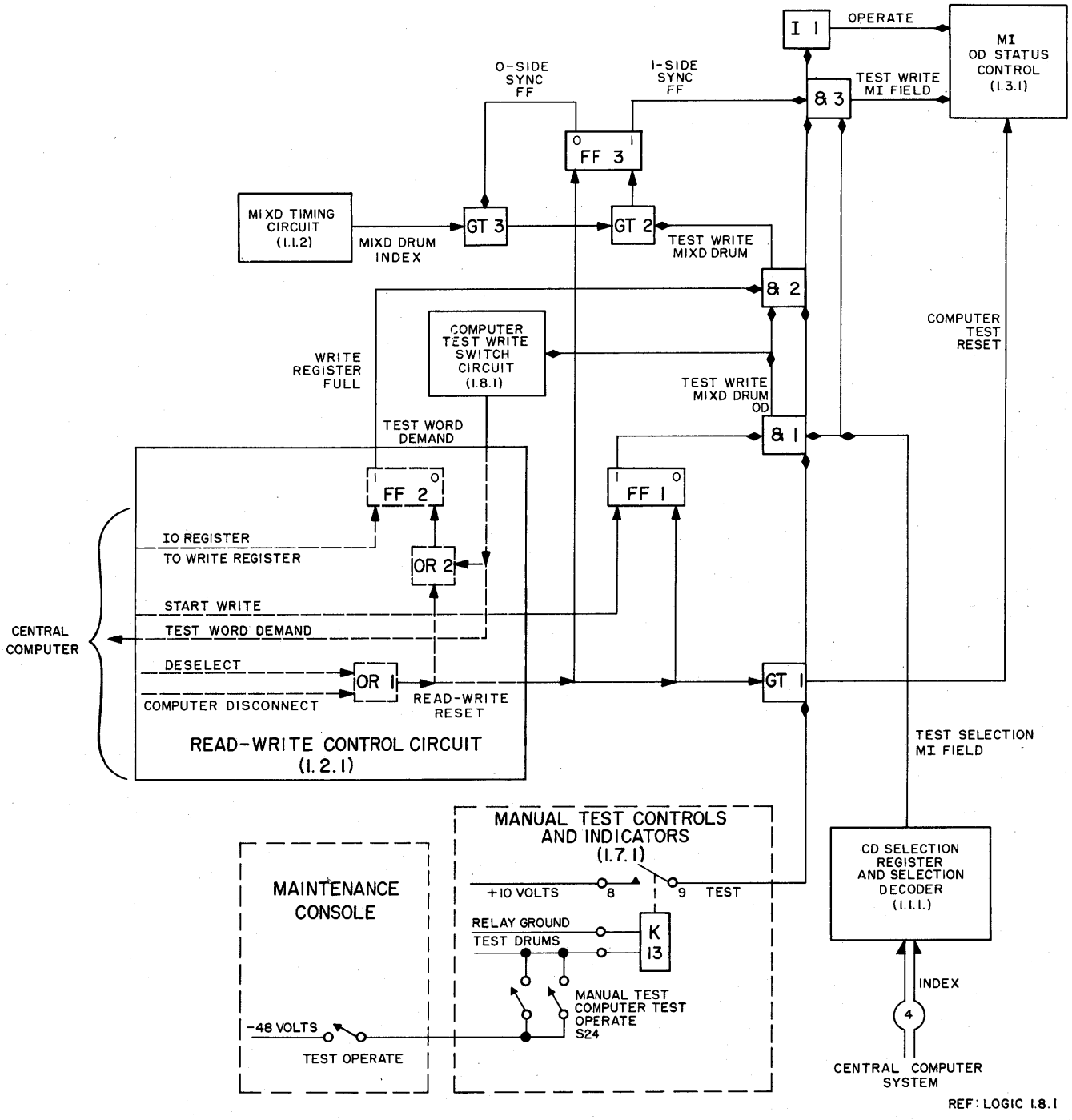


Figure 2–74. Computer Test Write Control for Input Fields, Simplified Logic Diagram

pulse, the normal data-available pulse cannot be created. However, a test-data-available pulse is created as described below.

The 1 output of FF 2 combines with the test-trols circuit in AND 1. (During normal operation, the test-write-selected-field level is not present, so that the GT 4 output cannot operate FF's 3 and 4.) AND 1 conducts, placing a conditioning level at GT 4 that passes the next OD 2 pulse from the timing circuit. The gated timing pulse forms the test-data-available pulse, which substitutes for the data-available pulse normally received from the Input System. The test-data-available pulse, like the normal data-available pulse, sets FF 3, causing a 1 to be written in the CD status channel when the timing circuits develop a status-write-sample pulse.

The test-data-available pulse also sets FF 4 to condition GT's 5 and 6. At the next OD 3 input to the OD-status-control circuit, GT 5 produces a write pulse

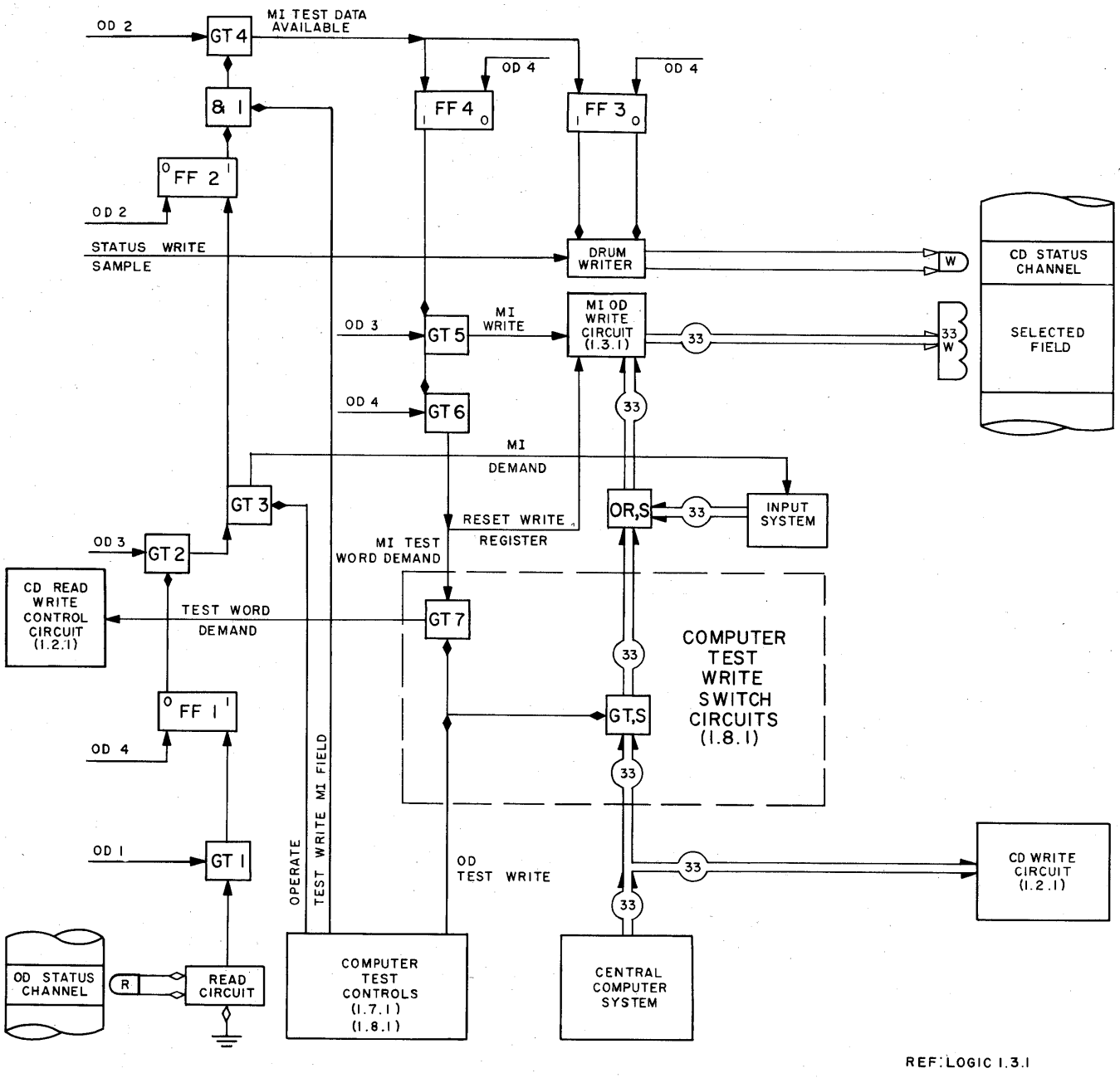


Figure 2–75. Input-Fields-Status-Control Circuit in Computer Test, Simplified Logic Diagram

which causes the selected OD-write circuit to write the write register contents onto the drum. At the next OD 4 pulse, GT 6 produces a test-word-demand pulse. The test-word-demand pulse is applied to GT 7 in the computer-test-write switch. If the test-write-select-drum-OD level from the computer-test-control circuit is still present, the test-word-demand pulse is gated to the CD-read-write-control circuit. From the CD-read-write-control circuit it goes to the Central Computer System to request another word.

The test-word-demand pulse at the output of GT 6 is also used to produce a reset-write-register pulse. The reset-write-register pulse clears the OD write circuits, readying it to receive the word from the Central Computer System. The path of this new word can be traced in figure 2–75. When the test-word-demand pulse is received by the Central Computer System, it places the word in the CD write circuit and in the 33 data gates in the computer-test-write-switch circuits. For as long as the test-write-select-drum-OD level from the computer-test-controls circuit remains present, the data gates are conditioned to pass the Central Computer System word to the data OR circuits. The data OR circuits receive inputs from the Input System during normal operation

but, during test operation, receive the test word from the computer-write-switch circuits. The OR circuits place the test word in the manual-input-OD-write circuit so that it may be written the next time a 0 bit is detected in the OD status channel.

From here on, the input-fields-computer-test circuit operates as a normal status-controlled circuit (refer to Ch 5). Writing is continued until the Central Computer System has written the programmed number of words. A computer-disconnect pulse from the Central Computer System then clears FF's 1 and 3 in the computer-test-control circuit (shown in fig. 2–74) and the write registers, ending the OD writing.

If a 1 is read in the OD status channel of the selected status-control circuit (shown in fig. 2–75), indicating a full register, the read circuit output will pass the OD 1 pulse through GT 1 to set FF 1. As a result, GT 2 will not be conditioned in time to pass the OD 3 pulse that starts the writing operation described above, and no writing will take place. Flip-flop 3, which has been cleared by an OD 4 pulse, remains cleared and causes a 0 to be written on the CD status channel, indicating that no word has been written.

The information written on the drum in this manner is read from the CD side of the drum by the normal-status identification-controlled reading operation. In the Central Computer System, comparison of the word written on the OD side of the drum with the word read on the CD side of the drum is made to ascertain whether the information has been correctly transferred.

Writing on the CD side of the drum during computer-test OD writing is stopped by lack of write pulses to the CD write register. Although the CD write register is full, the word cannot be transferred to the CD write heads.

9.1.3 Output Buffer Fields Computer Test

Output buffer (OB) field computer-test circuits permit reading of the OD side of the OB fields by the Central Computer System. Words previously written on the CD side of these fields by the Central Computer are compared in the Central Computer System with those read from the OD side to determine whether the word content has changed in the transfer.

The circuits of the OB fields of the Drum System normally read the OB fields to the Output System from the OD side of the drum. For computer tests on the output fields, a test signal path is provided which allows the Central Computer System to read the OD side of the drum fields. In the performance of computer tests on the OB fields, the computer-test-control circuit is conditioned by a d-c test level from the manual test circuits (fig. 2–76). To start a reading operation on the OD side of the drums, the Central Computer System sends a deselect pulse to the CD-read-write-control circuit. The deselect pulse forms a read-write-reset pulse which clears flip-flops in the computer-test-control circuit. The computer test signal path for OD reading is ready for programmed operating instructions from the Central Computer System.

A Central Computer System instruction, in the form of six index-interval pulses, goes to the CD-selection circuits, producing a select-OB-odd-or-select-OB-even level. This level enters the OB-field-selection circuits, where it develops a select-OB level. The select-OB level is sent to the computer-test-controls circuit, which it conditions to perform the OB computer test.

Before the actual test of the fields begins, the computer-test-controls circuit enters a pretest phase. The pretest phase is initiated when a test-OD level is received from the OB-field-selection circuits. This level is produced when the OB-field-selection circuits have connected the read heads for field 3 to the OB-OD-read circuits. Switching of the heads is performed by applying an OB-OD-field-select level to selected heads via the OB-OD-diode-switching circuit.

When counters in the OB-field-selection circuits determine that the next field (field 1) should be switched into the read circuit, an OB-switch-field pulse is developed. This pulse, in addition to enabling the selection of field 1, also goes to the computer-test-controls circuit. In the computer-test-controls circuit, it ends the pretest phase and begins the test phase of operation.

The test phase of operation is marked by the production of an OB-test level from the computer-test-controls circuit. The OB-test level goes to the OB-field-selection circuits, conditioning the transmission of a select-OB-OD-selected level to the selected OB-OD-status-control circuit.

The OB-test level also goes to the computer-test-read-switch circuits to open gates and to the OB-OD-diode-switching circuits to enable operation during test procedures.

In the selected OB-OD-status-control circuit that receives the select-OB-OD level, the presence of a word in a register of the selected OB field causes an OB-read-sample pulse to be generated. The OB-read-sample pulse is sent to the OB-OD-read circuit, where it is used to transfer data from the OB-OD-diode-switching circuit to the Central Computer System, via the OB-OD-read circuit, the computer-test read switch, 33 data OR circuits, and the CD-read-bus-output circuits. Simultaneous reading of the CD side of the OB fields is prevented by lack of read-sample pulses to the CD-read circuit.

The same read-sample pulse that produces OD reading branches in the OB-OD-read circuit and goes to the computer-test-read switch, where, in conjunction with the OB-test level from the computer-test-control

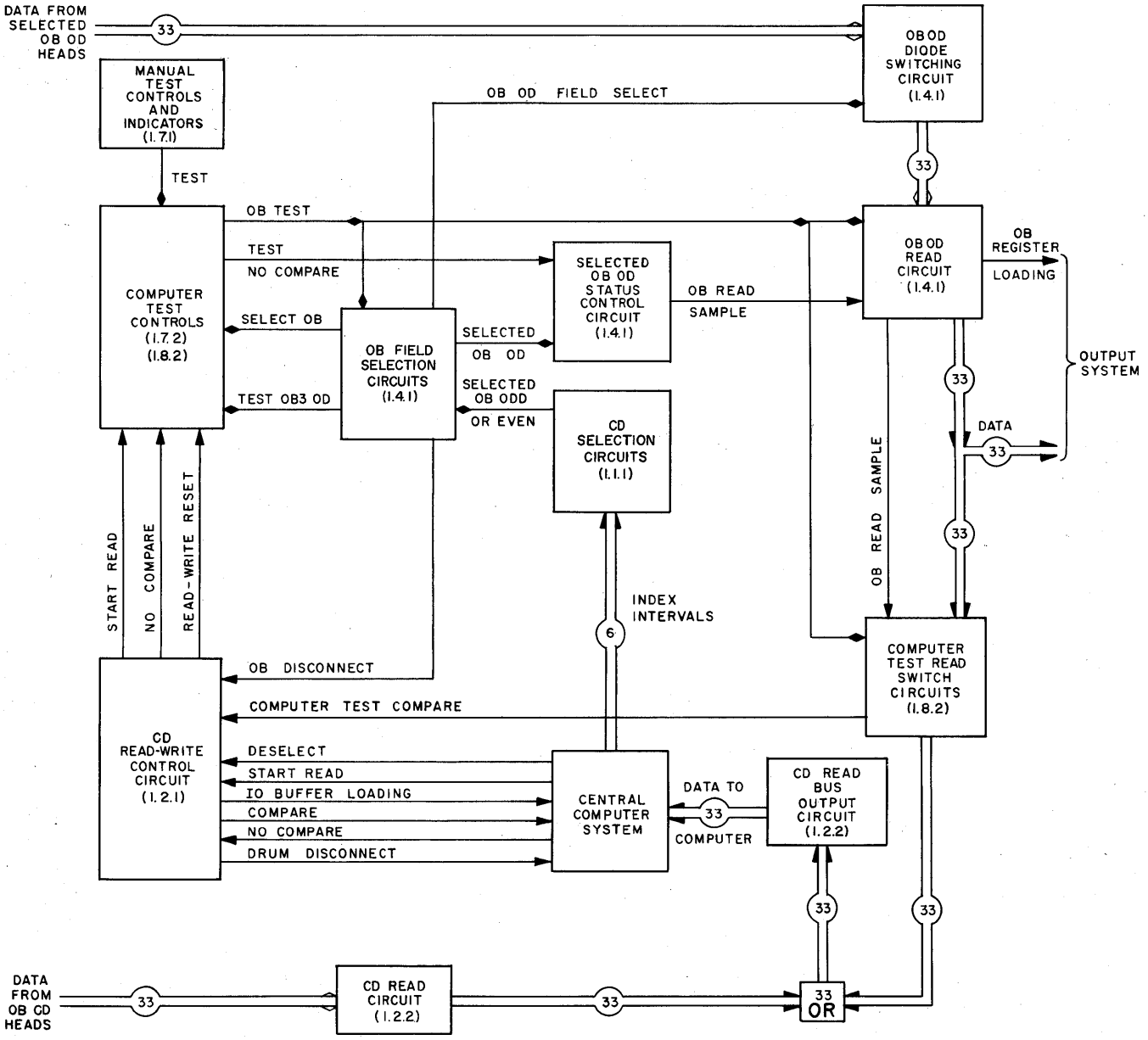


Figure 2–76. Output Buffer Fields Computer Test, OD Read, Block Diagram

circuit, it forms a computer-test-compare pulse. The computer-test-compare pulse goes to the CD-read-write-control circuit. There it is converted into IO-buffer-loading and compare pulses, which inform the Central Computer System that a word has been read that should be compared with the word previously written. Data also goes to the Output System, but it is not accepted there because the OB-register-loading pulse is absent during computer tests. No-compare pulses from the Central Computer System are fed to the computer-test-controls circuit, causing the production of the test-no-compare signal. The test-no-compare pulses enter the selected OB-OD-status control circuit and prevent the writing of other data in the registers read. This preserves the data written on the drum.

When the 2,048 registers of OB field 1 (the first field selected) have been sampled, OB-switch-field pulses transfer operations to OB fields 2 and 3 in turn. The reading operations for the latter two fields are the same as for field 1. After all programmed information has been read, a disconnect pulse is received from the Central Computer System. This pulse goes to the CD-

read-write-control circuit and is converted into a read-write-reset pulse. The read-write-reset pulse accomplishes the disconnecting operation by clearing the computer-test-controls circuit. Clearing the computer-test-controls circuit removes the OB-test level, preventing the production of field selection levels for use in the OD-status-control circuits.

9.1.4 Output Buffer Fields Computer Test, Circuit Analysis

During normal operation, the circuits of the OB fields of the Drum System read data from the OD side of OB fields to the Output System. During computer testing, a signal path is provided to read this data into the Central Computer System.

Before computer tests can be made on the output fields, a d-c test level must be supplied to the computer-test-controls circuit. This level is produced as described in 9.1.2. The test circuits are now ready to act on programmed instructions from the Central Computer System.

A deselect pulse from the Central Computer System is sent to the CD-read-write-control circuit, where it is converted into a read-write-reset pulse (fig. 2—77). The read-write-reset pulse clears FF's 1 and 2 in the computer-test-controls circuits.

A select-OB-odd or select-OB-even d-c level is produced in the CD-selection circuit as the result of decoding the selection indicated by the six index-interval-pulse signals from the Central Computer System. The selection level produced in this manner goes to the OB-CD-field-and register-switch-control circuit, developing a select-OB level which goes to AND's 1 and 2 in the computer-test-controls circuit.

A start-read pulse from the Central Computer System, via the CD-read-write-control circuit, sets FF 1, producing a test-read level, which goes to AND 1. Four of five conditions necessary to conduction in AND 2 are present in the test, select-OB, 0-side-sync-flip-flop (from FF 2), and test-read levels. The fifth level, the test-OB-3-OD level, is produced in the manner described below.

The OB-field switch counter (OB and CD) counts 12 CD 1 timing pulses after each CD index pulse from the LOG-timing circuit. At the 12th pulse counted, a CD-OB operate level is developed which goes to the OB-OD-field-switch circuit. In the OB-OD-field-switch circuit, the CD-OB operate level causes the production of an OB field selection level which goes to the center taps of the read heads of the selected OB field via the OB-OD-diode switching circuit. At each occurrence of the CD-OB operate level, the field selection changes to the next highest numbered OB field. When the OB-OD-field 3-select level is produced, the test-OB-3-OD level is also produced and sent to AND 1. The operation of the OB-OD field switch circuit is described in detail in Chapter 6.

Conduction in AND 1 of the computer-test-controls circuit produces an OB-pretest conditioning level at GT 1. At the next index pulse received by the OB-field-switch counter (OD and CD), an OB-switch-field pulse is developed which changes the selection level produced by the OB-OD-field-switch circuit to select-OB field 1. The OB-switch-field pulse also goes to GT 1 in the computer-test-controls circuit. It is passed by the OB-pretest level to set FF 2. With FF 2 in the 1 state, a 1-side-sync-flip-flop level is added to the select-OB level (from the OB-field-and-register-switch-control circuit) and to the test level at AND 2. This produces an OB-test level at the output of AND 2. The OB-test level goes to GT 2, to the OB-OD-read circuit, to the gates in the computer-test-read-switch circuit, and to the OB-OD-field-switch circuit.

In the OB-OD-field-switch circuit, the OB-test level substitutes for the operate level produced by INVERTER 1 when the Drum System is in normal operation. The OB-test level, therefore, enables the OB-OD-field-switch circuit to produce a select-OB-OD level, which is sent to the selected-OB-OD- status-control circuit (in this case, for OB field 1) when an OB-operate level from the OB-field-switch counter is present. The OB-operate level is present during the reading of each field. Its absence for 120 usec after field switching is necessary to provide sufficient delay for transients to die out.

The select-OB-OD level, sent to the selected OB-OD-status control circuit, enables that circuit to function as though operation is normal. When a full register is sensed, a read-sample pulse is sent to the OB-OD-read circuit. In the OB-OD-read circuit, the read-sample pulse is used in the gating of data from the OB-OD-diode-switching circuit to the computer-test-read-switch circuits and is itself sent to GT3 in the computer-test-read-switch circuits.

In the computer-test-read-switch circuits, the OB-test level conditions GT 3 to pass the read-sample pulse as a computer-test-compare pulse. The computer-test-compare pulse goes to the CD-read-write-control circuit. In the CD-read-write-control circuit, the computer-test-compare pulse branches and is sent to the Central Computer System as an IO-buffer-loading pulse, which informs the Central Computer System of the word transfer, and as a compare pulse, which requests the Central Computer System to compare the identification bits of the words read with those of the words previously written.

Data pulses entering the computer-test-read-switch circuits pass through 33 data gates which are conditioned by the OB-test level. After being passed through the computer-test-read-switch circuits, the data goes to

the CD-read-bus-output circuit via 33 data OR circuits and is sent to the Central Computer System. Data is also read to the Output System but cannot be accepted there because the OB-register-loading pulse, formed from the read-sample pulse in normal operation, is not developed. This OB-register-loading pulse is formed when the operate level from INVERTER 1 in the computer-test-control circuit is present.

To prevent the writing of new words on the registers being read, the Central Computer System sends a no-compare signal to the CD-read-write-control circuit. From this circuit, the pulse goes to the computer-test-controls circuit, where it is passed through GT 2 by the OB-test level as the test-no-compare pulse. The test-no-compare pulse is applied to the selected OB-OD-status-control circuit, where it causes a 1 to be written in the CD-status channel. This prevents the writing of a new word in the register involved. As a result, the information written on the OB fields during computer tests is preserved and can be used again.

In this way, reading proceeds through each of the three OB fields in the sequence of field 1, field 2, and field 3. When all the programmed information in the three fields has been read, the Central Computer System produces a disconnect pulse which goes to the CD-read-write-control circuit, forming a read-write-reset pulse. This read-write-reset pulse clears FF's 1 and 2 in the computer-test-control circuit to end the test.

Information read to the computer from the OD side of the OB drum fields is compared with information previously written on the CD side of these fields to ascertain whether the information has been correctly transferred. Comparison is made by means of identification bits inserted into the programmed words.

Transfer of words read on the CD side of the drum to the Central Computer System is prevented by lack of read-sample pulses from the CD-read-write-control circuit.

9.1.5 Display Field Computer Test

Display field computer test circuits permit the Central Computer System to read the OD side of the display fields (TD, RD, and DD). Test words previously written on the CD side of these fields by the Central Computer are compared in the Central Computer System with the test words read from the OD side to make certain that they have not changed during the transfer.

The circuits of the display fields of the Drum System normally read the display fields from the OD side of the drums during normal operation and transfer the display data to the Display System. During computer tests on the display element, a test signal path is provided which allows the Central Computer System to read the OD side of the display fields. For performance of computer tests on the display fields, the computer-test-controls circuit is conditioned by a test d-c level from the manual test circuits (fig. 2–78). To start a reading operation on the OD side of the drums, the Central Computer System sends a deselect pulse to the CD-read-write-control circuit. In the CD-read-write-control circuit, the deselect pulse is converted into a read-write-reset pulse, which clears the flip-flops of the computer-test-controls circuit. Clearing the computer-test-control circuit prepares the computer test signal path to accept programmed operating instructions from the Central Computer System.

A Central Computer System selection, in the form of six index-interval pulses, enters the CD-selection circuits and, depending on the coding of these pulses, produces d-c levels which are used to select the test. Two selections are available in display element testing: one for the DD field, called the DD-test-select level; and another for the SD (RD and TD) fields, called the SD-test-select level. The selection level enters the computer-test-controls circuit, where it is used in conjunction with a start-read pulse from the computer via the CD-read-write control circuit to form a test-read d-c level. These same conditions produce the SD-test level and computer-test-start-TD pulse, for SD testing, and the DD-test level and start-DD-test pulse, for DD testing. The test-read level conditions the computer-test-read switch to pass data from the OD-read circuit to the Central Computer System via the OR circuit and the CD-read-bus-output circuit. In normal operation, the data goes from the CD-read circuit to the Central Computer System via the OR circuit and CD-read-output circuit. When SD testing has been selected, the resulting computer-test-start-TD pulse and the SD-test d-c level start the SD (TD and RD) OD-read-control circuits. The read-control circuits provide read-sample pulses in the normal OD reading patterns of these fields. Similarly, selection of the DD test provides the start-DD-test pulse and the DD-test d-c level, which start the DD-OD-read-control circuit, thus providing read-sample pulses in the normal OD reading pattern of the DD field. The read-sample pulses are used in the OD-read circuits to transfer data to the computer-test-OD-read switch. The read-sample pulse also goes to the computer-test-read-switch circuit, where it is converted into the computer-test-compare signal. This computer-test-compare signal goes to the CD-read-write control circuit, where it is converted into both an IO-buffer-loading pulse and a compare pulse. The IO-buffer-loading pulse notifies the Central Computer System that a word is being transferred to it. A compare pulse requests the Central Computer System to compare the word read on the OD side of the drum with the word previously written on the CD side.

When all information programmed into the DD field or the SD (TD and RD) fields has been read, the

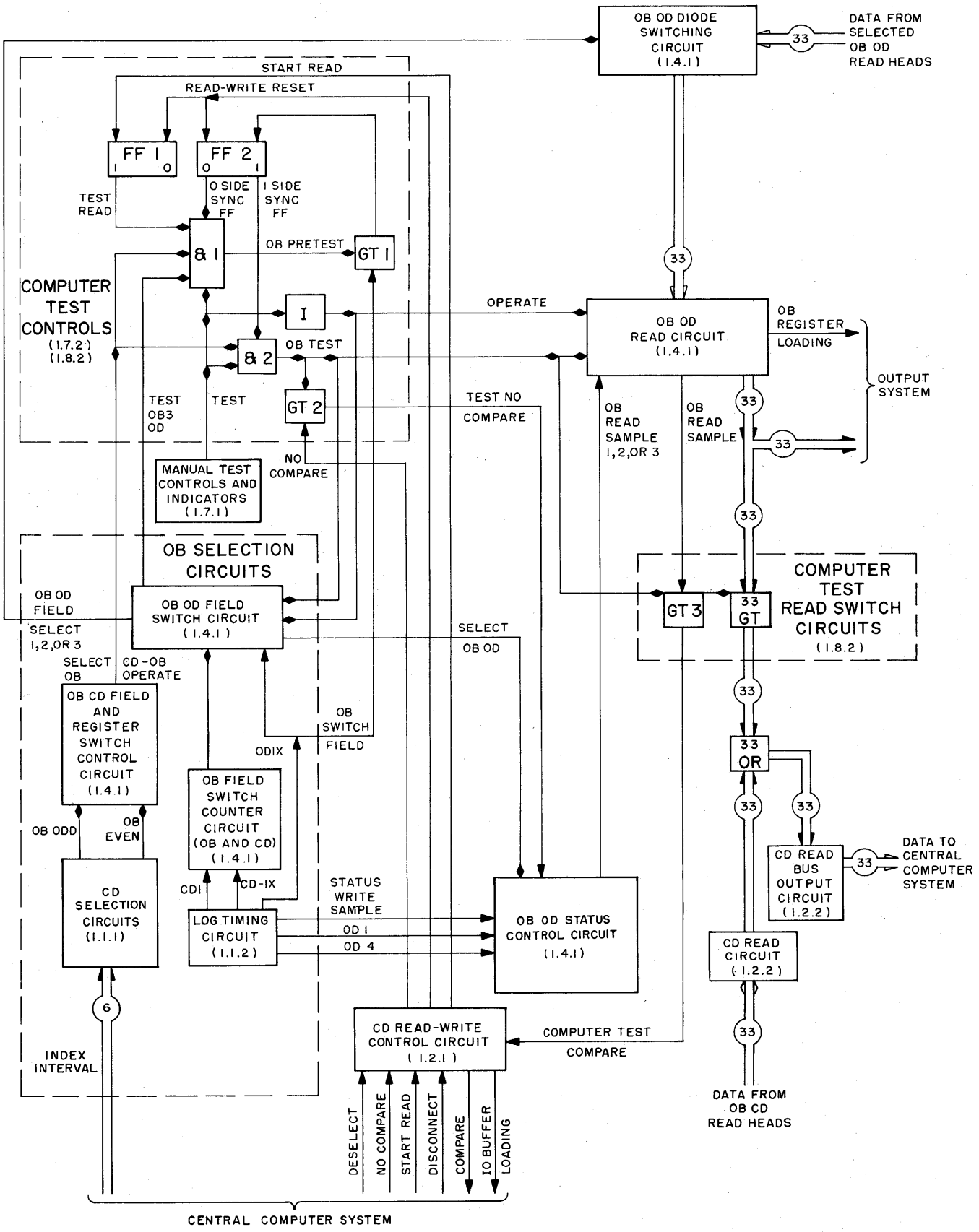


Figure 2–77. Computer Test for OB Fields, Simplified Logic Diagram

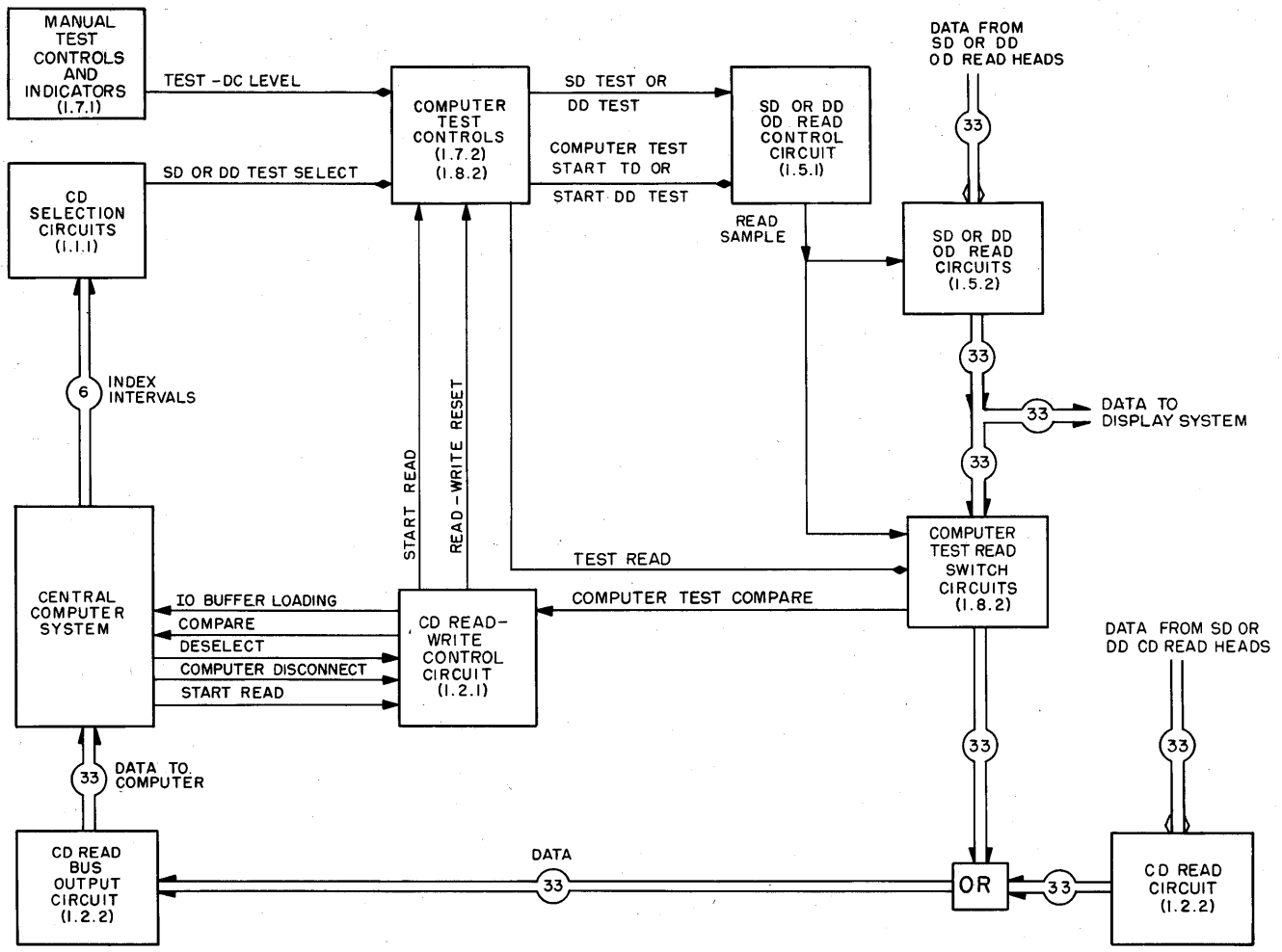


Figure 2–78. Display Fields Computer Test, OD Read, Block Diagram

Central Computer System sends a computer-disconnect pulse to the CD-read-write-control circuit. The computer-disconnect signal is converted into a read-write-reset pulse, which clears the computer-test-controls circuit, ending the test.

During these tests, the data from the OD side is read to the Display System as well as to the Central Computer System. No data is read on the CD side of the fields.

The information read from the OD side of the display drum fields is compared with the information previously written on the CD side of the drums to ascertain that no changes have occurred in the transfer. Comparison is made by means of identification bits inserted into the programmed words.

9.1.6 Display Fields Computer Test, Circuit Analysis

The circuits of the display fields of the Drum System are normally used to read data to the Display System from the OD side of the SD (TD and RD) and DD fields. When computer tests are to be performed on the display fields, a test signal path is established to read this data into the Central Computer System. Operation of the SD and DD-computer-test circuits is described in the paragraphs that follow.

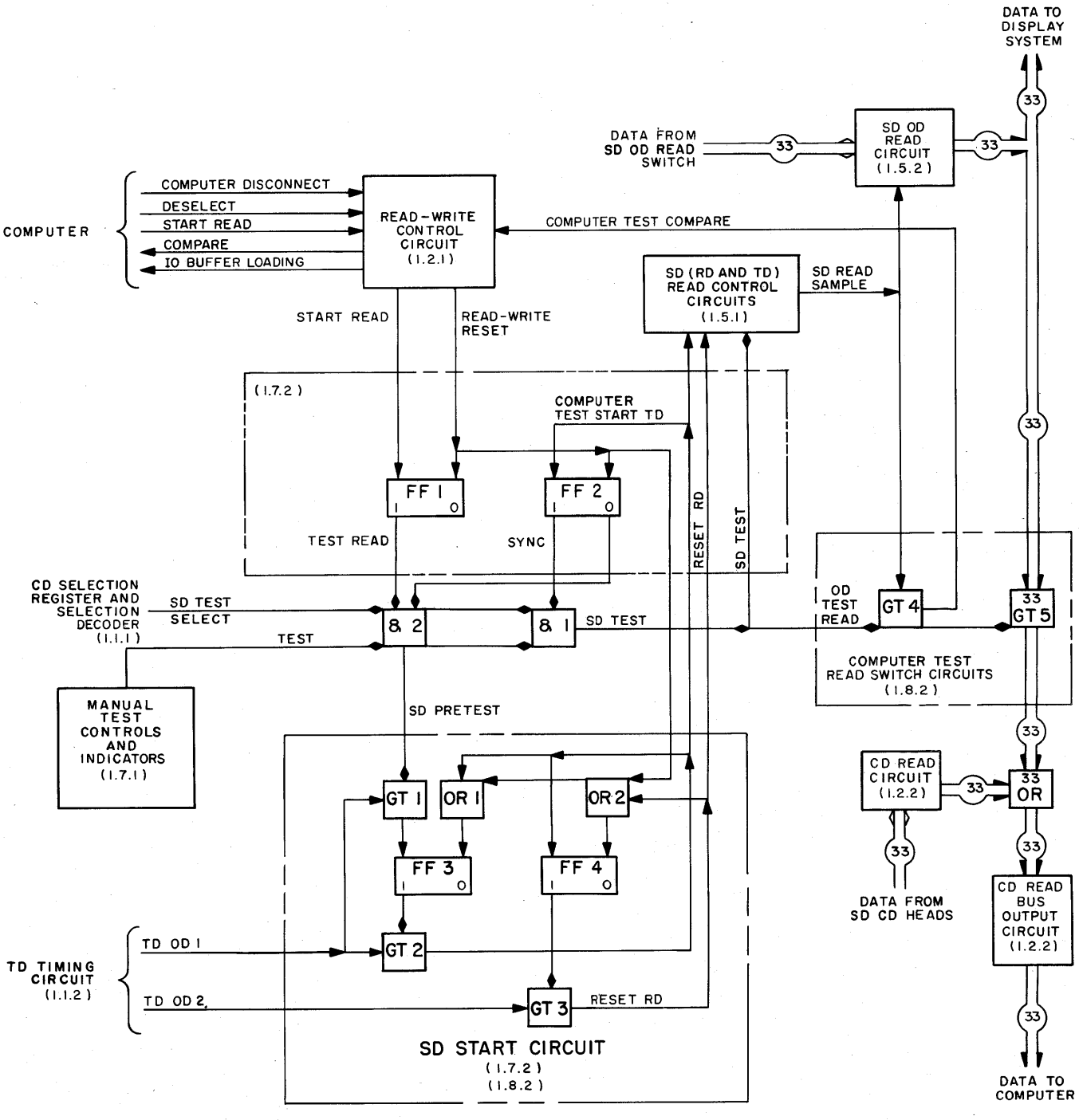
9.1.6.1 Situation Display Computer Test

As in other computer tests performed by the computer test circuits, a +10-volt test level must be supplied to the computer-test-controls circuit. This is accomplished as described in 9.1.2.

A deselect pulse from the Central Computer System is sent to the CD-read-write-control circuit, where it is converted into a read-write-reset pulse (fig. 2–79). The read-write-reset pulse is used in the computer-test-controls circuit to clear FF's 1 (test read), 2 (sync), and 3 and 4 (SD-start circuit). This conditions the control circuits to accept operational instructions from the Central Computer System.

Selection of SD testing by commands from the Central Computer System causes an SD-test-select level to be generated in the CD-selection circuits and sent to the computer-test-controls circuit. A start-read pulse is

then received from the Central Computer System via the CD-read-write-control circuit. The start-read pulse creates a 1 output at FF 1 which combines with the SD-test-select level, the 0 level of FF 2, and the test d-c level in AND 2 to produce SD-pretest level. The SD-pretest level activates GT 1 in the SD-start circuit, passing an OD 1 timing pulse to set FF 3 to the 1 side. The 1 output of FF 3 conditions GT 2 to pass the second OD 1 pulse for use as the computer-test-start-TD pulse. This same OD 1 timing pulse is also used to clear FF 3 and set FF 4 to the 1 side, thus activating GT 3. Gate 3 passes the OD 2 timing pulse following



REF: LOGIC 1.8.2

Figure 2–79. Display Fields Computer Test, SD Read, Simplified Logic Diagram

the second OD 1 pulse. This gated OD 2 pulse is used to clear FF 4 and, as a reset-RD pulse, to clear the RD-read-control circuit to prepare it for operation.

The computer-test-start-TD pulse (OD 1) starts the TD-OD-read-control circuit in its precessed reading operation. At the same time, this pulse sets FF 2 to the 1 side. The output of FF 2, combined with the SD-test-select level and the test d-c level in AND 1, produces the SD-test level. This SD-test level activates the SD (RD and TD) read-control circuit to produce SD-read-sample pulses which go to the SD-OD-read circuit. There, the read-sample pulses are used to transfer data to the computer-test-read-switch circuits. The SD-read-sample pulses also branch off and go to the computer-test-read-switch circuit. Read-sample pulses are produced according to the precession pattern for TD OD reading. Thus 12 slots of 8 consecutive registers each are skipped, and the 13th read. This process continues for 13 revolutions per field in order to read all the field registers. After all six TD fields are read, eight of the nine RD fields are read by the precession scheme for these fields. In this pattern, one register is read and five consecutive registers are skipped. This action goes on until all registers in a field are read, which occurs in six revolutions. The other seven fields are then read in order.

The SD-test d-c level also goes to the computer-test-read-switch circuits as the OD-test-read level. The OD-test-read level conditions GT 5 (one of 33 similar gates) in the computer-test-read-switch circuits to pass data from the SD-OD-read circuit to the Central Computer System via OR 3 and the CD-read-bus-output circuit. In addition, the OD-test-read level activates GT 4 in the computer-test-read-switch circuits to pass SD-read-sample pulses from the SD (TD and RD) read-control circuits. These gated read-sample pulses are sent to the CD-read-write control circuit as computer-test-compare pulses. A computer-test-compare pulse is converted in the CD-read-write-control circuit into an IO-buffer-loading pulse and a compare pulse.

During SD computer tests, the information read is also sent to the Display System. No reading is done on the CD side of the selected fields at this time because of the absence of a selection level.

When all the programmed information on the SD (TD and RD) fields has been read, the Central Computer System sends a computer-disconnect pulse to the CD-read-write-control circuit. This signal forms a read-write-reset pulse which clears the computer-test-control circuit flip-flops, thus stopping the test.

The words read from the OD side of the display drum fields are compared in the Central Computer System with the words previously written on the CD side of the drums to make certain that no changes have occurred in the transfer. Word comparison is made by means of identification bits inserted into the words originally written on the drums by the Central Computer System.

9.1.6.2 Digital Display Computer Test

In computer tests of the DD fields, a +10-volt d-c test level is first supplied as described in 9.1.2.

A deselect pulse from the Central Computer System is sent to the CD-read-write-control circuit, where it is converted into a read-write-reset pulse (fig. 2–80). The read-write-reset pulse is used in the computer-test-controls circuit to clear FF's 1 and 2. The computer-test-controls circuit is now conditioned to accept operational instructions from the Central Computer System.

Selection of DD testing by commands from the Central Computer System causes a DD-test-select level to be generated in the CD-selection circuits and sent to the computer-test-control circuit. In the same manner as that described in 9.1.6.1 for the SD-pretest level, the DD-pretest level is produced at AND 4. The DD-pretest level conditions GT 6 to pass MIXD-drum-OD-index pulses to form start-DD-test pulses. The start-DD-test pulse goes to the DD-OD-read-control circuit to start its precession reading operation. In addition, the start-DD-test pulse is sent to FF 2 to set the flip-flop to the 1 side. The 1 output of FF 2 combines with the test d-c level and the DD-test-select level in AND 3 to form the DD-test level. This DD-test level then activates the DD-OD-read-control circuit to produce DD-read-sample pulses which go to the DD-OD-read circuit. There the DD-read-sample pulses are used to transfer data to the computer-test-read-switch circuits. The DD-read-sample pulse also branches off and goes to the computer-test-read-switch circuits as the DD-test level.

Digital-display-read-sample pulses are produced according to the precession pattern for DD-OD reading. Thus 63 registers are skipped, and the 64th is read. This pattern is continued for a total of 64 drum revolutions in order to read all registers on the DD field.

The DD-test level branches off and is sent to the DD-OD-read circuit. The remainder of the DD computer test is the same as the SD computer test described in 9.1.6.1.

9.2 MANUAL TESTS

This paragraph describes test circuits in the Drum System which enable maintenance personnel to perform checks and tests on Drum System functions using Drum System circuitry only. These tests, known as manual tests, provide a way of localizing most malfunctions to a specific circuit, channel, pluggable unit, or component. The tests are conducted from the test door on unit 21 (fig. 2–81). The manual controls and test circuitry are shown in detail on logics 1.7.1 and 1.7.2.

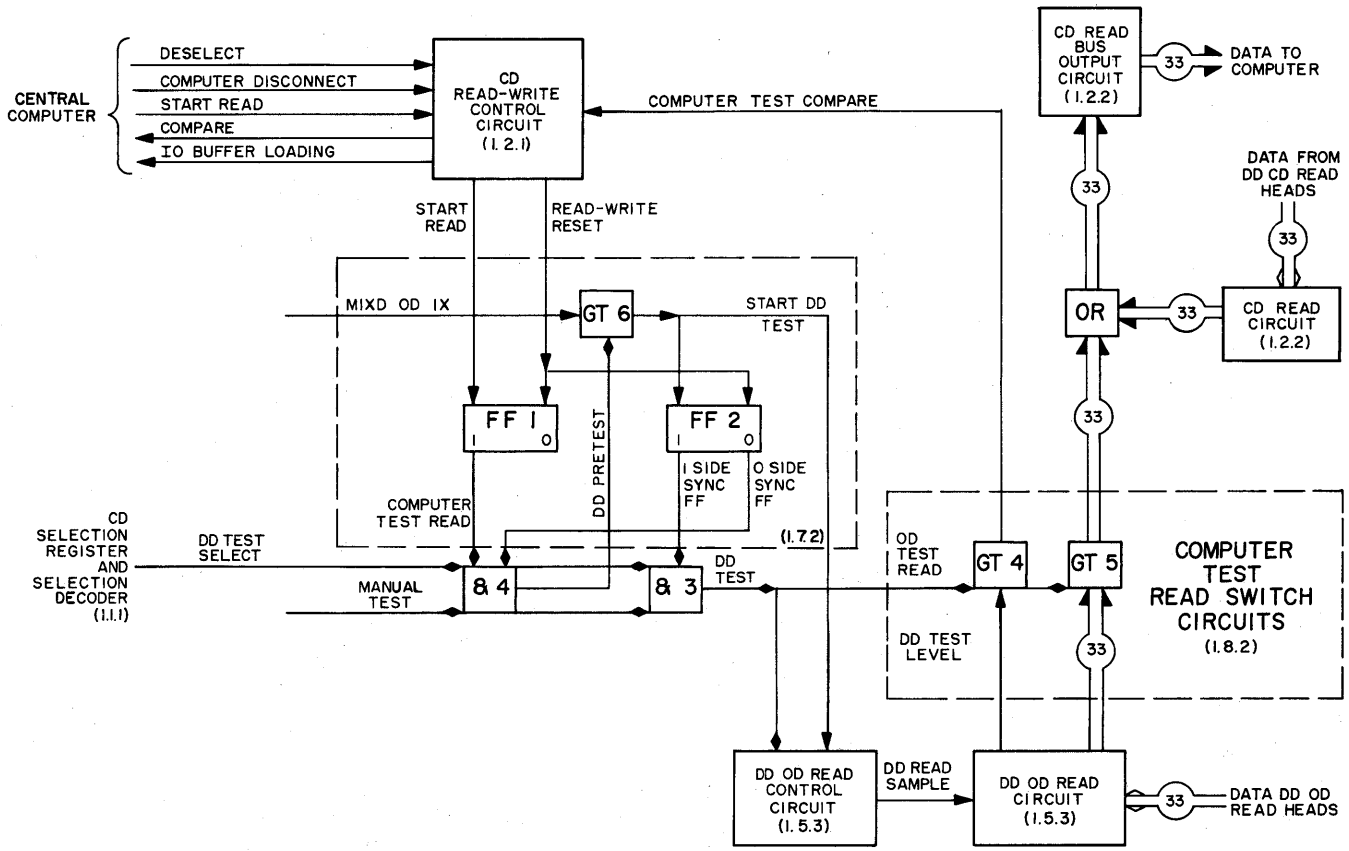


Figure 2–80. Digital Display Field Computer Test, Simplified Logic Diagram

9.2.1 Begin-Manual-Test Circuit

All manual tests on the Drum System must start with the operation of controls related to the begin-manual-test circuit (fig. 2–82). A —48-volt level is transmitted from the maintenance console to the begin-manual-test circuit when the TEST-OPERATE switch in module E of the maintenance console is in the TEST position. When TEST MODE SELECTION switch S2 on the test door of module 21L is set to the DRUMS IN MANUAL TEST position, the —48-volt level energizes the coil of relay K6. When K6 is energized, its 1 and 2 contacts close and energize K4, thus completing the circuit to the computer-test-control circuit, where the +10 volts serve as a test level. The +10-volt level also passes through the closed 3 and 4 contacts of K6 to several manual-test circuits, where it is used as a manual-test level.

Simultaneously with the formation of the test and manual-test levels, a d-c ground level is brought through closed relay K4 contacts 5 and 6 to the normally open SINGLE PULSE pushbutton, S35. This button is located on the test door of module 21L (fig. 2–81). When S35 is depressed, the d-c ground is applied to the pulse generator, causing the production of a single 0.1-usec pulse. This pulse appears at the SINGLE PULSE jack, J8, for use in test procedures requiring a single standard pulse.

9.2.2 Manual-Test-Field-Selection Circuit

Whenever a manual test begins with the operation of switch S2 in the begin-manual-test circuit (refer to 9.2.1), it is necessary to select the field to be tested. This is done by the operation of controls in the manual-test-field-selection circuit (fig. 2–83).

Initially, DESELECT pushbutton S24 is depressed, applying a test ground level to the input of the pulse generator through the normally open contact of S24 unit 1. Switch S24 is on the module 21L test door. When the pulse generator input is grounded, the generator produces one 0.1-usec pulse. This pulse is conducted through the closed, normally open, contacts of switch unit 2 to the CD selection register as a manual-deselect pulse. The manual-deselect pulse substitutes for the deselect pulse normally produced by the Central Computer System by providing an alternate input to OR 1. The deselect pulse clears the selection register and is sent to the CD-read-write-control circuit to prepare the latter to receive a drum operation instruction.

With the deselect operation completed, it is neces-

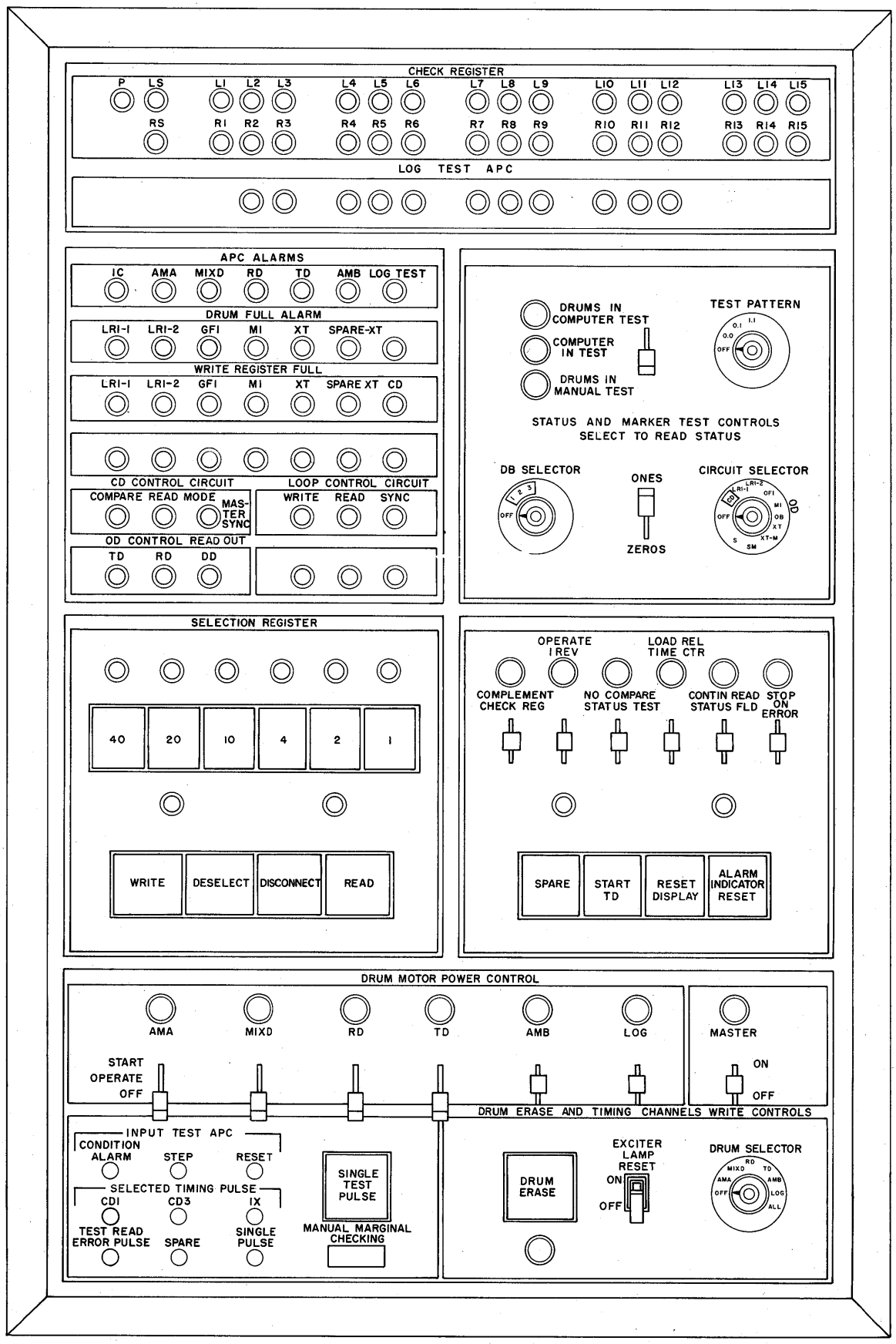


Figure 2–81. Unit 21, Module L, Test Door

sary to substitute manually a drum field selection for the drum field selection that normally comes from the Central Computer System in the form of index-interval pulses. Pushbuttons S16 through S21, labeled, 1, 2, 4, 10, 20, and 40 (on the test door), provide substitutes for the six index-interval pulses from the Central Computer System. Depressing the pushbuttons produces 1 bits for the associated index intervals. The resulting configuration of 1 and 0 bits in index-interval pulses 1, 2, and 4 determines the value of the units column in the drum field selection code; the resulting configuration of 1 and 0 bits in index intervals 10, 20, and 40 determines the value of the tens column in the drum field selection code.

Table 2–5 shows the code of the field or test selection and the pushbuttons that must be depressed to produce it. Each pushbutton that is depressed in accordance with this table applies ground to the pulse generator. The pulse generator output (0.1-usec pulse) is conducted through the closed switch unit 2 pushbutton contacts of the OR circuit associated with the index-interval pulse represented by the individual pushbuttons. The OR circuits normally get index-interval pulse inputs from the Central Computer System. The pulses pass through the OR circuits and set the associated flip-flops in the CD selection register. On the basis of the setting of the CD selection register, the CD selection decoder determines the drum that has been selected and sends a drum-select level to the timing-pulse-distributor circuit. The CD selection encoder also determines the selected field and sends a select-drum-field level to the selected drum field driver. The selected drum field driver applies this level to the center taps of the drum heads associated with the selected fields, thereby enabling them to read or write.

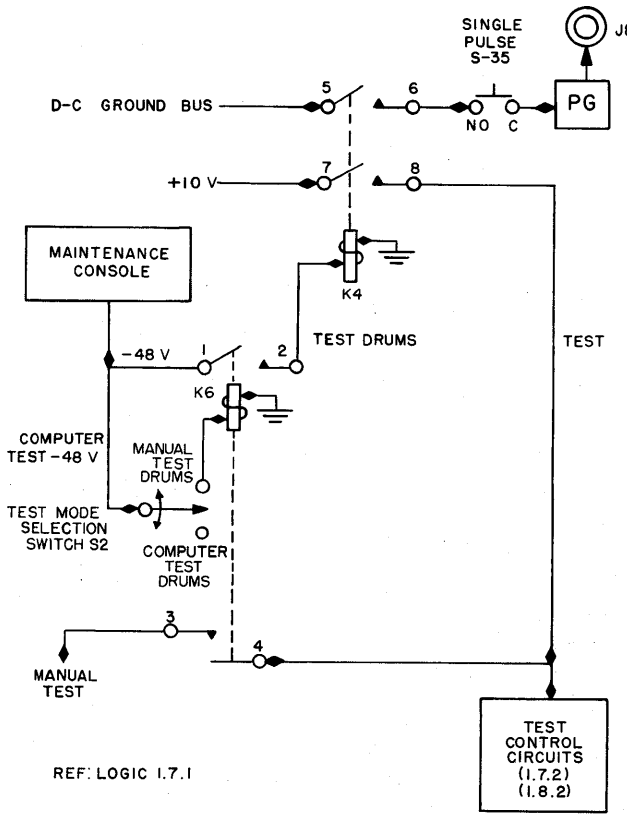


Figure 2–82. Manual Test Circuit, Simplified Logic Diagram

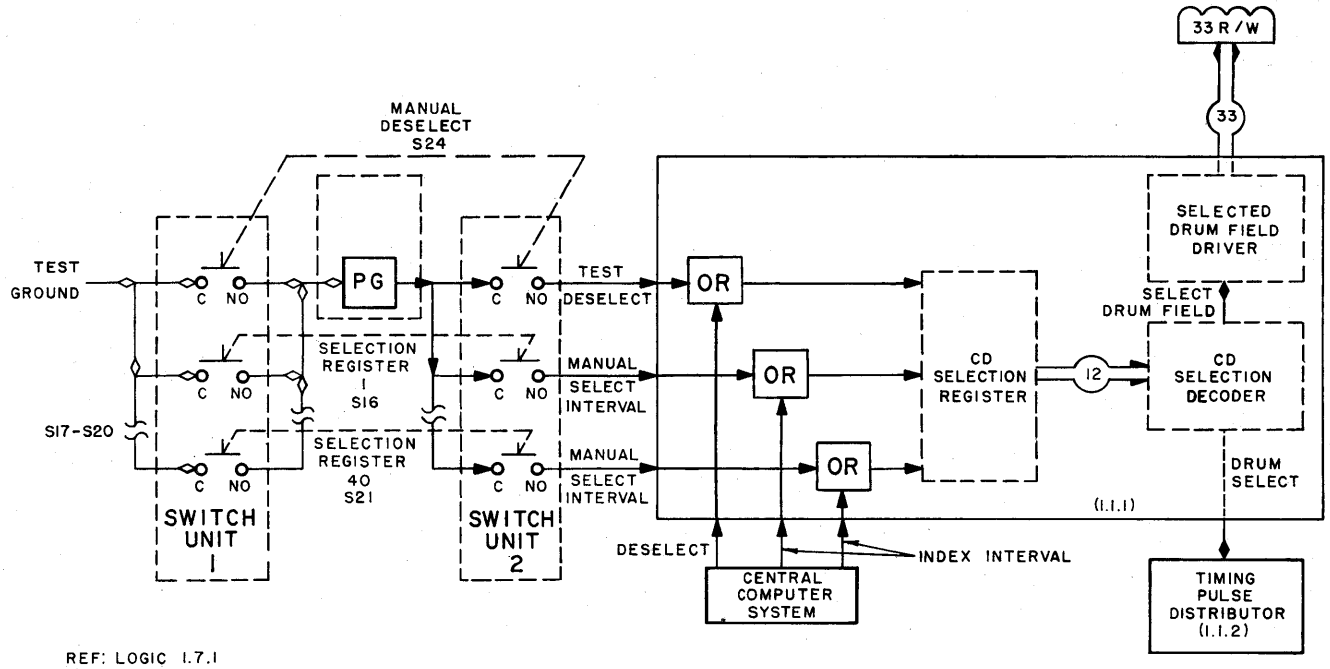


Figure 2–83. Manual Test Field Selection, Simplified Logic Diagram

9.2.3 Select-Manual-Read-or-Write-Drum-Operation Circuit

If the manual test that is to be performed requires a reading or writing operation by the field (or test) that has been selected, it is necessary to develop a manual substitute for the *Read* or *Write* instructions that normally come from the Central Computer System. The necessary substitution is made by the operation of controls in the select-manual-read-or-write-drum-operation circuit (fig. 2–84).

When a manual test involving a reading operation is to be performed on a selected field, the READ pushbutton is depressed. This applies a test ground to the pulse generator, producing a 0.1-usec pulse. The pulse serves as a manual-start-read pulse for use in the manual-test-pattern-control circuits, discussed in 9.2.4. It also serves as a substitute for the normal Central Computer System instruction to the CD-read-write control circuit and computer-test-control circuits.

TABLE 2–5. MANUAL TEST PANEL SELECTION REGISTER PUSHBUTTON CODE

FIELD OR TEST	CODE	PUSH-BUTTONS
DATA FIELDS		
MI basic status (test)	22	20, 2
MI status identification	23	20, 2, 1
XTL basic status (test)	24	20, 4
XTL status identification	25	20, 4, 1
XTL marker	40	40
LRI basic status (test) 1	34	20, 10, 4
LRI basic status (test) 2	36	20, 10, 4, 2
LRI 1 status identification	35	20, 10, 4, 1
LRI 2 status identification	37	20, 10, 4, 2, 1
GFI 1 basic status (test)	32	20, 10, 2
GFI 1 status identification	33	20, 10, 2, 1
AUXILIARY DRUMS FIELDS		
Auxiliary memory A-1	02	2
Auxiliary memory A-2	03	2, 1
Auxiliary memory A-3	04	4
Auxiliary memory A-4	05	4, 1
Auxiliary memory A-5	06	4, 2
Auxiliary memory A-6	07	4, 2, 1
Auxiliary memory B-7	10	10
Auxiliary memory B-8	11	10, 1
Auxiliary memory B-9	12	10, 2
Auxiliary memory B-10	13	10, 2, 1

TABLE 2–5. MANUAL TEST PANEL SELECTION REGISTER PUSHBUTTON CODE (cont'd)

FIELD OR TEST	CODE	PUSH-BUTTONS
Auxiliary memory B-11	14	10, 4
Auxiliary memory B-12	15	10, 4, 1
Spare 1	20	20
Spare 2	21	20, 1
OUTPUT DATA FIELDS		
Output buffer odd	30	20, 10
Output buffer even	31	20, 10, 1
INTERCOMMUNICATION OD ELEMENT		
Intercommunication other	16	10, 4, 2
Intercommunication own	26	20, 4, 2
DISPLAY DATA FIELDS		
Digital display test	17	10, 4, 2, 1
Digital display	27	20, 4, 2, 1
Track display 1	41	40, 1
Track display 2	42	40, 2
Track display 3	43	40, 2, 1
Track display 4	44	40, 4
Track display 5	45	40, 4, 1
Track display 6	46	40, 4, 2
Situation display test	47	40, 4, 2, 1
Radar data 1	60	40, 20
Radar data 2	61	40, 20, 1
Radar data 3	62	40, 20, 2
Radar data 4	63	40, 20, 2, 1
Radar data 5	64	40, 20, 4
Radar data 6	65	40, 20, 4, 1
Radar data 7	66	40, 20, 4, 2
Radar data 8	67	40, 20, 4, 2, 1
Radar data 9	70	40, 20, 10

If the TD or RD fields are to be read, it is necessary to depress the RESET DISPLAY and START TD pushbuttons. Operation of these two pushbuttons also applies ground to the pulse generator, sending manual-

reset-display and manual-start-TD pulses which go to the TD-OD-read-control circuit. These pulses substitute for the power-on-reset pulse developed when the equipment is initially energized, or for the end-RD-start-TD pulse produced during normal operation. When a manual test involving a writing operation is to be performed, the WRITE pushbutton is depressed. The action of this pushbutton is similar to that of the READ pushbutton. Manual-start-write pulses go to the CD read-write control circuit and to the computer-test-control circuit in place of the normal Central Computer System pulse inputs. An automatic manual-start-write pulse is provided for the manual-test pattern control circuit by gating the test-APC-carry pulse through the manual-read-write control circuit.

If the operation of the relative time counter for the GFI fields is to be tested, it is necessary to operate the LOAD REL. TIME CTR. switch. This allows the begin-manual-test circuit to be sent to the GFI-relative-time-counter-step circuit. In the relative-time-counter-step circuit, this level conditions a gate which provides a test source for the relative-time-counter-reset pulse which clears the flip-flops in the counter.

9.2.4 Manual-Test-Pattern-Control Circuit

During manual tests that require a known pattern to be written and read on the drum fields, the pattern to be used is selected by operating a control in the manual-test-pattern-control circuit. The complement of this pattern can also be developed by operating a control in the complement-test-pattern circuit. OR 1, in the manual-test-pattern-control circuit (fig. 2–85), conducts upon receipt of either a manual-start-read or a manual-start-write pulse, thereby setting the pattern flip-flop. Although the beginning of every test causes the flip-flop to be set, a complement-test-pattern pulse can be manually produced, which at first application clears the pattern flip-flop and at second application sets it again.

The output of the pattern flip-flop go to the contacts of TEST PATTERN switch S1. When the flip-flop side connected to any given contact is up, +10 volts are seen at the contact. When the flip-flop side is down,—30 volts are applied to the contact. Table 2–6 outlines the voltage present at the two wiper arms of the TEST PATTERN switch when the flip-flop is set and cleared for each position of the switch.

The output of the RC wiper arm is the odd-pattern-gate level; the output of the LC wiper arm is the even-pattern-gate level. The odd- or even-pattern-gate levels are logically present only when they are positive. The odd-pattern gate, when present, conditions GT 1. The even-pattern gate, when present, conditions GT 2. Gates

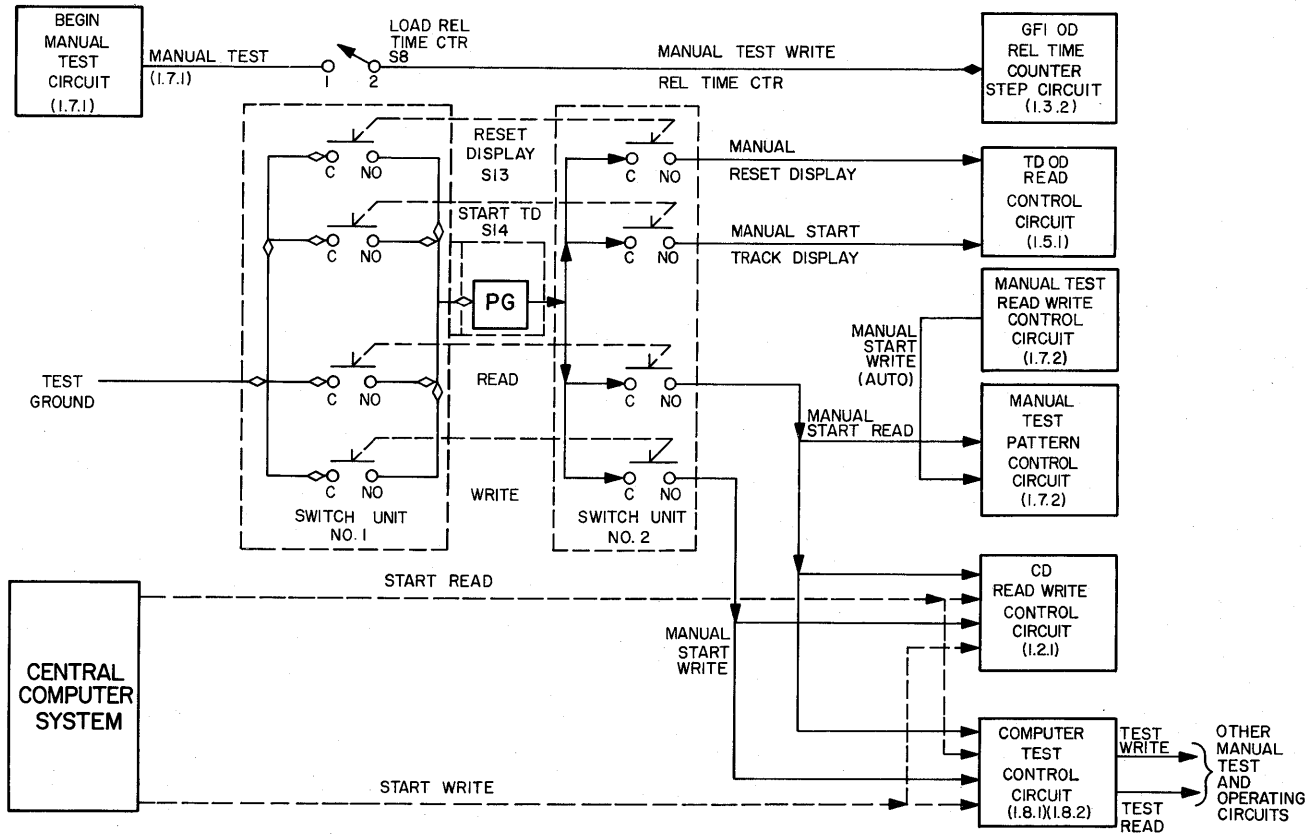


Figure 2–84. Select Manual Read or Write Drum, Simplified Logic Diagram

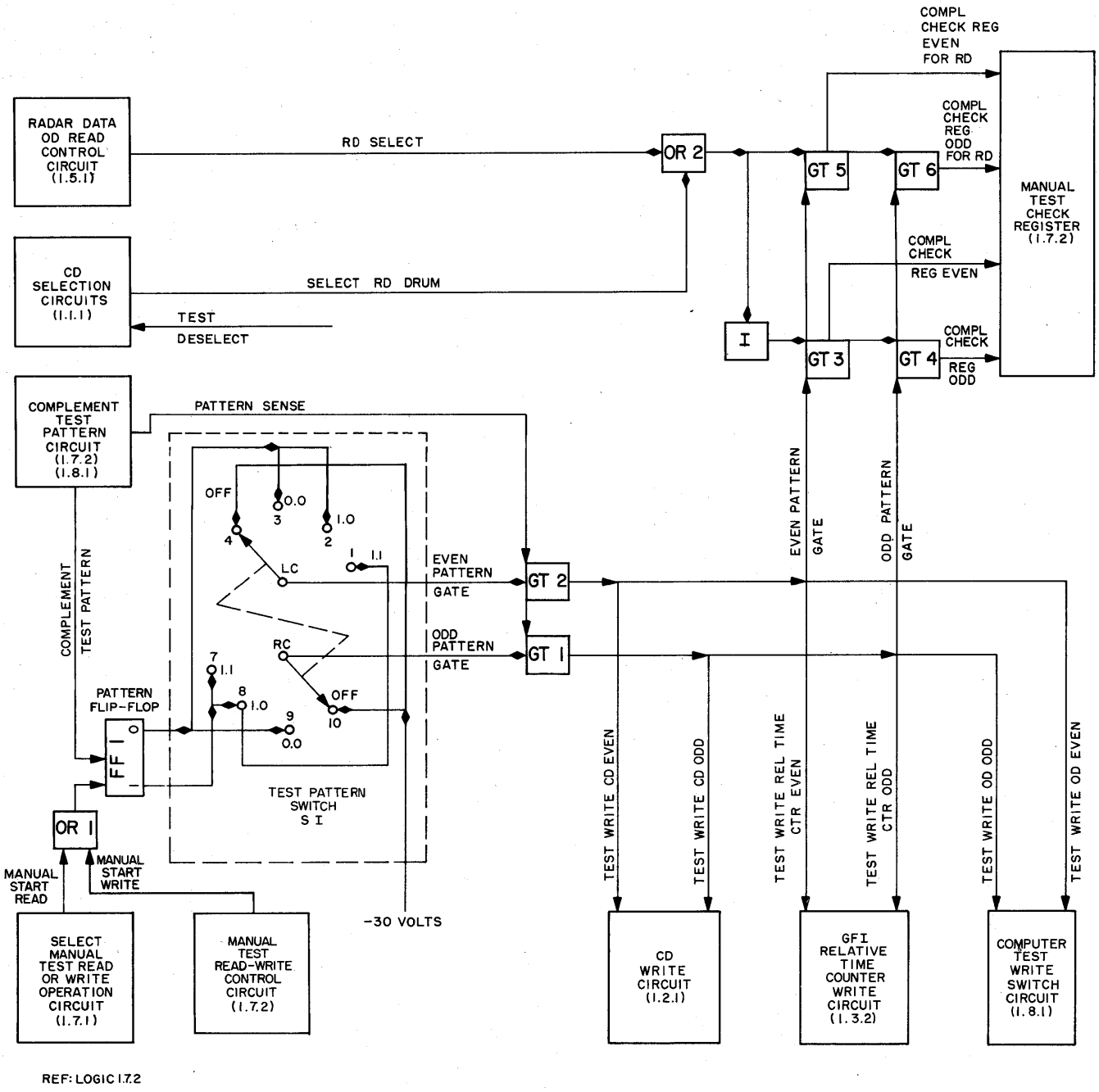


Figure 2–85. Manual Test Pattern Selection and Control Circuits, Simplified Logic Diagram

1 and 2 receive a pattern-sense pulse from the complement test pattern circuits. (Refer to 9.2.5.) The pattern-sense pulses will go through the gates (either or both) whenever they are conditioned. The GT 1 output goes to the CD-write circuit as a test-write-CD-odd pulse, to the GFI-relative-time-counter-write circuit as a relative-time-counter-odd pulse, to the computer-test-write-switch as a test-write-OD-odd pulse, and to GT's 4 and 6 as an odd-pattern-gate pulse.

Gate 6 is conditioned to pass the odd-pattern-gate pulse if an RD-select level from the RD-OD-read-control circuit or a select-RD-drum level from the CD selection circuits is present at OR 2. Gate 4 passes the odd-pattern-gate pulse if both levels are absent from OR 2 since, at this time, the INVERTER-tube circuit produces a positive output which conditions the gate. The output of GT 6 is a complement-check-register-odd-for-RD pulse. The output of GT 4 is a complement-

TABLE 2–6. TEST PATTERN SWITCH OUTPUT VOLTAGES

SWITCH POSITION	SWITCH CONTACT	WIPER ARM	VOLTAGE WITH FLIP-FLOP SET (VOLTS)	VOLTAGE WITH FLIP-FLOP CLEARED (VOLTS)
OFF	4	LC	−30	−30
	10	RC	−30	−30
0.0	3	LC	−30	+10
	9	RC	−30	+10
1.0	2	LC	−30	+10
	8	RC	+10	−30
1.1	1	LC	+10	−30
	7	RC	+10	−30

check-register-odd pulse. The complement-check-register odd and complement-check-register-odd-for-RD pulses go to the manual-test-check register.

The output of GT 2 duplicates the functions of the output of GT 1, but as even pulses. Thus, the GT 2 output produces a test-write-CD-even pulse, an even-pattern-gate pulse, and so on. Whenever an output of GT 1 or 2 is present, it causes the placing of 1's in the associated write circuit to which the odd or even output goes. Thus, if the GT 1 output is present, 1's are passed to the odd-numbered channels (L1, L3, . . . R1, R3 . . . and so on) of the write circuits to which it is applied. In the same way, the GT 2 output causes 1's to be passed in the even-numbered channels (L2, L4, . . . R2, R4, . . . and so on) of the write circuits to which it is applied.

A distinction is made between the odd- and even-complement-check-register pulses that are sent during an RD field selection because the RD fields contain only 24 bits each. Complement-check-register-for-RD pulses, whether odd or even, are applied to only 24 bits of the manual check register.

9.2.5 Complement-Test-Pattern Circuit

The complement-test-pattern circuit (fig. 2–86) is employed in the production of the pattern-sense pulse, which senses the condition of the pattern flip-flop and TEST PATTERN switch for the varied write circuits involved in manual tests. The pattern-sense pulse is produced during manual test procedures. A manual test

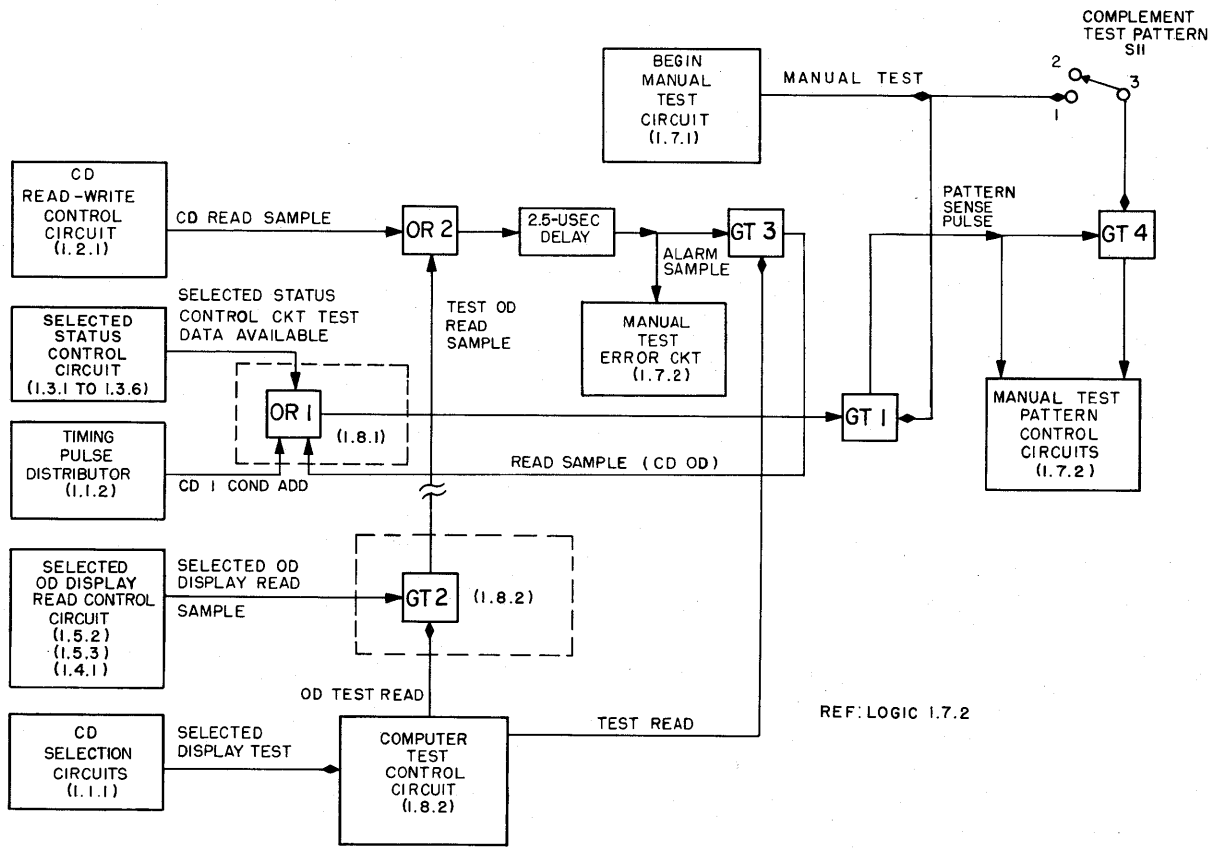


Figure 2–86. Complement Test Pattern Circuit, Simplified Logic Diagram

level conditions GT 1, which will then pass the output of OR 1 (fig. 2–86). Conduction in OR 1 is caused either by a selected-status-control-circuit-test-data-available pulse from the selected-status-control circuit, by a CD-1-conditioned-add pulse from the timing pulse distributor, or by a CD-OD-read-sample pulse from the CD read-write control or the computer test control circuits.

During manual test read operation, the computer-test-control circuit sends a test-read level to GT 3, conditioning the gate. The pulse input to GT 3 is obtained from OR 2, which, in turn, receives pulses from either the CD-read-write-control circuit or from the selected-OB-OD-display-read-control circuit via GT 2. When the pulse is obtained from the CD-read-write-control circuit, the CD-read sample is applied directly to OR 2. When the pulse is obtained from the selected-OB-OD-display-read-control circuit, a selected display-test level (either SD or DD) is transmitted to the computer-test-control circuit. The control circuit then transmits an OD-test-read level to GT 2 if a manual read test is being performed as described in 9.2.3. With GT 2 conditioned, selected SD-OD-read sample pulses from the selected-SD-OD-display-read-control circuit pass through GT 1 to OR 2.

The output of OR 2 is delayed 2.5 usec and applied to GT 3, which has previously been conditioned by the test-read level from the computer-test-control circuit (as described above), and the output of GT 3 is applied to OR 1. The delayed OR 2 output also goes to the manual-test-error circuit as an alarm sample.

The pattern-sense pulse at the output of GT 1 is also used to produce the complement-test-pattern pulse, which is sent to the manual-test-pattern-control circuits. This pulse is developed by operating the COMPLEMENT TEST PATTERN switch, S11. This applies a level to GT 4, gating the pattern-sense pulse to form the complement-test-pattern pulses.

9.2.6 Manual-Test-Check-Register-and-Control Circuit

The manual-test-check-register and control circuit (shown in fig. 2–87) provides a means of checking the contents of words written by the manual-test-pattern-control circuits. As was indicated in 9.2.4 and 9.2.5, during manual test write operations, a pattern-sense pulse is developed which causes the manual-test-pattern-control circuit to send complement-check-register pulses to the manual-test-check register. The complement-check-register pulses may appear as odd- and/or even-complement pulses for RD field or as odd- and/or even-complement pulses for all other drum fields. Complement-check-system-odd-for-RD pulses go to the even-numbered flip-flops from 2 to 10 and from 16 to 26. Complement-check-register-odd pulses for all other fields go to all the even-numbered flip-flops.

Complement-check-register-even-for-RD pulses go to all odd-numbered flip-flops from 1 to 11 and from 15 to 27. Complement-check-register-even pulses for all other fields go to all the odd-numbered flip-flops.

In this manner, selection of an RD field for manual test purposes allows only those flip-flops in the manual-check-register circuit that correspond to the RD drum word bits to be affected.

Each flip-flop in the manual check-system control circuit has both its 1 and 0 sides connected to neon indicator lamps on the manual test panel. Since complement pulses sent to the manual-check-register circuit correspond to the pattern pulses sent to the various write circuits during the manual test write procedures, the flip-flops of the manual-check register which are set by the reading of 1 bits are cleared by the complement pulses.

When manual test writing is completed, a manual test read operation checks the pattern that has been written. The manual-test-check register and control circuit is initially cleared by a reset-check-register pulse from the manual control circuit if an error was indicated. As seen in 9.2.10, the reset-check-register pulse is produced by manually operating a control on the test panel of the drum unit. After the initial clearing of the manual-test-check register the contents of the drum register being read at CD 1 time are sent to the flip-flops in the manual-test-check register from the CD-read-bus-output circuit. At any bit in the drum register where a 1 is read, that 1 sets the associated flip-flop in the check register. At CD 2 time, 2.5 usec later, the complement-check-register pulse is sent to the manual-test-check register. All flip-flops that should have 1 bits receive a complement pulse. If the pattern that should have been written is read, all flip-flops in the manual-test-check register are cleared. If, however, a flip-flop that should have a 1 bit has a 0 bit instead, the complement pulse sets that flip-flop. This causes an error indication.

To sum up the operation of the manual-test-check register and control circuit, the presence of a 1 bit in any flip-flop after CD 2 time indicates an error. This 1 bit is sent to the manual-test-error circuit and produces an error indication which stops drum operations. The neon lamps connected to the flip-flops then indicate which drum bit is being incorrectly transferred.

9.2.7 Status-Control-Channel-Manual-Test Circuits

The paragraphs that follow describe the manual test operations which are used to check the status control function. In order to check the status control chan-

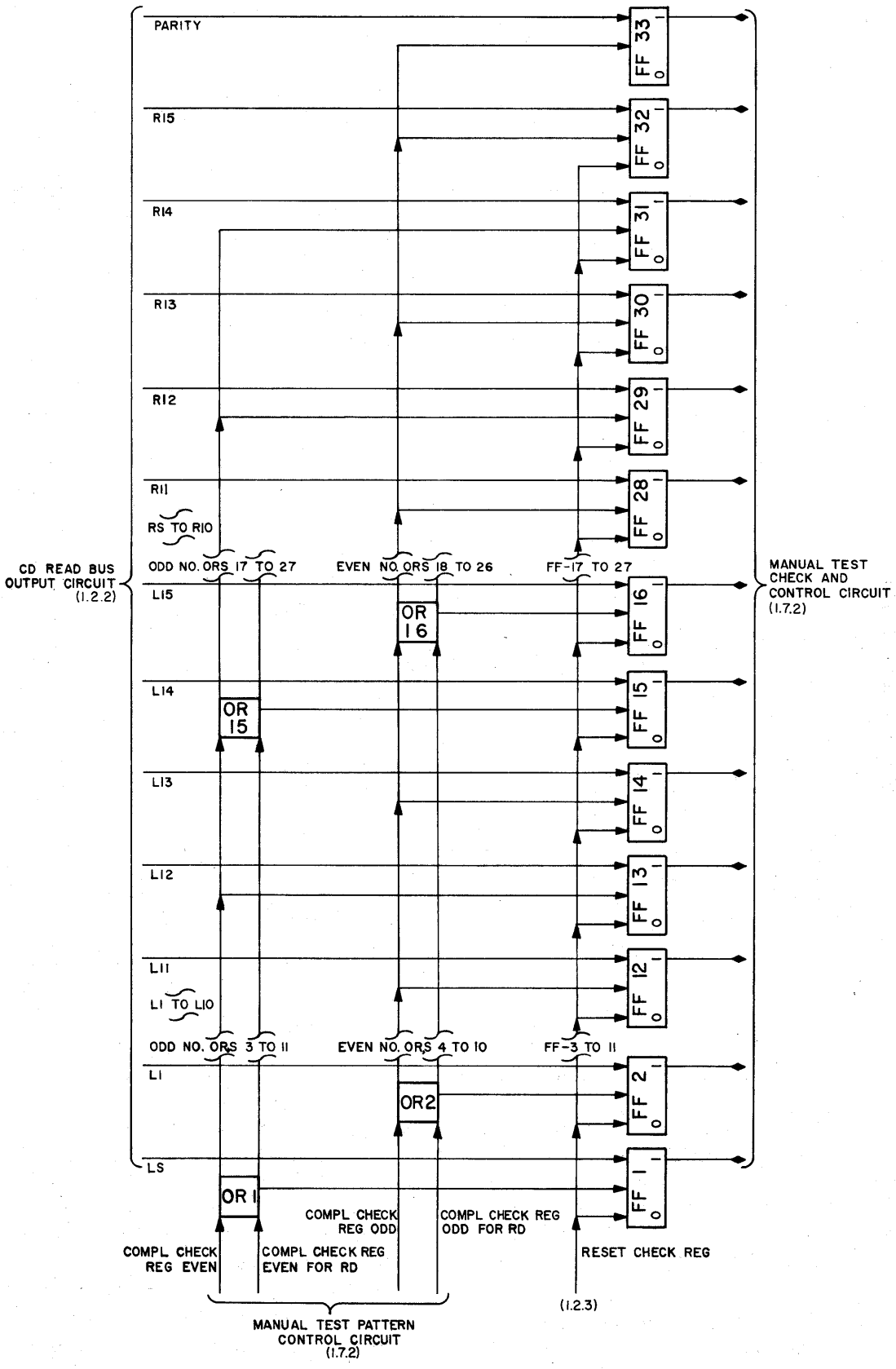


Figure 2–87. Manual Test Check Register and Control Circuit, Simplified Logic Diagram

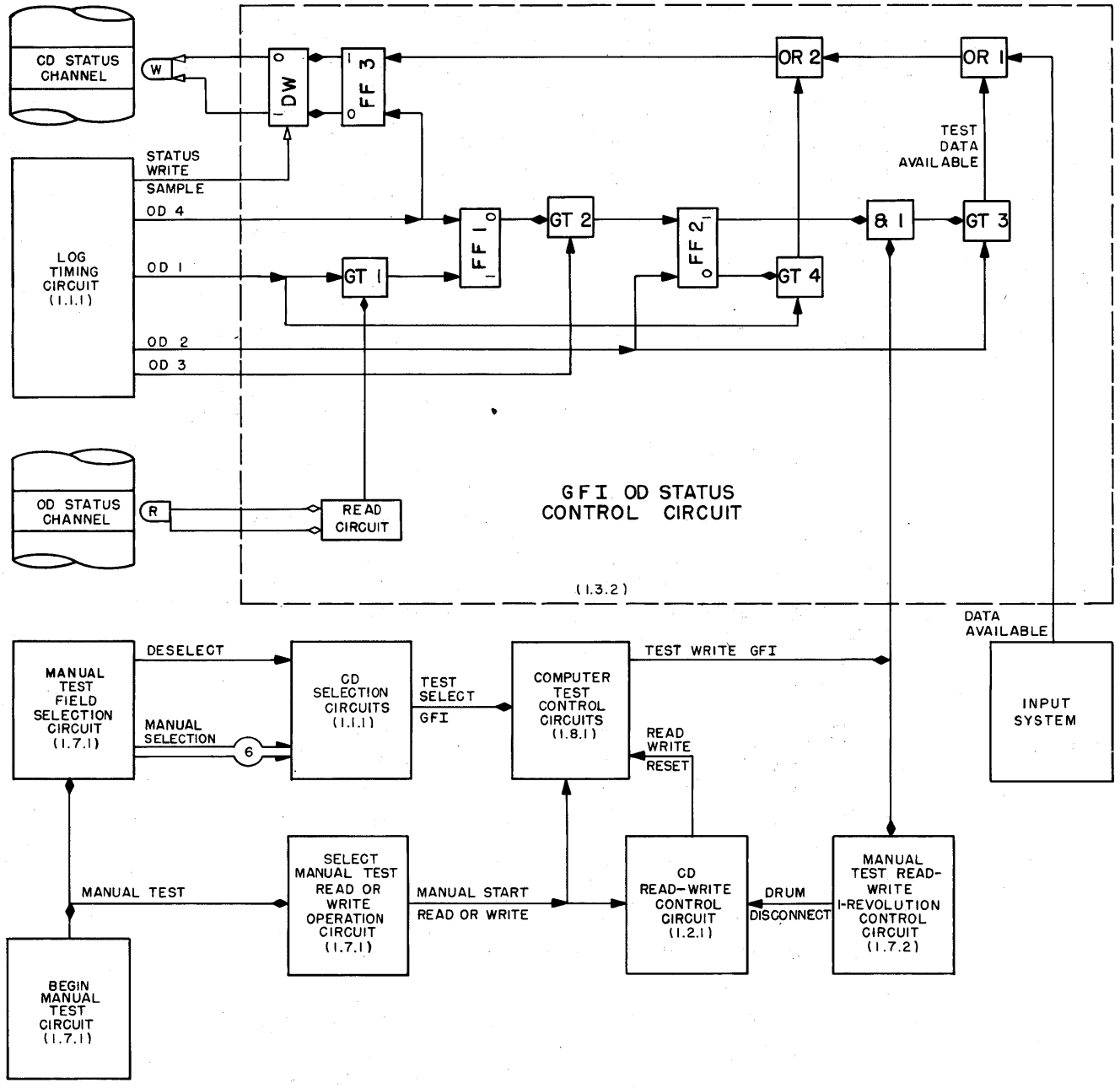


Figure 2–88. Writing CD Status Channel for Manual Test, Simplified Logic Diagram

nels of the fields that read and write by status control, 1 or 0 bits are written in the OD and the CD status channels and are read back to make certain that no errors have occurred. The manner in which the status channels are manually written and later checked to detect possible error is described in 9.2.7.1 through 9.2.7.6.

9.2.7.1 Writing the Status Channels for Manual Test

The circuits employed to write 1's or 0's manually in the status channels of the status-controlled fields are shown in figures 2–88 and 2–89. If it is desired to fill the status channels for a given field with 1 or 0 bits, a manual-test level is produced in the begin-manual-test circuit (fig. 2–88). The manual-test level is sent to the select-manual-test-read-or-write operation circuit and to the manual-test-field selection circuit. The field whose status channels are to be written is manually selected in the manual-test-field-selection circuit by producing a deselect pulse and the necessary combination of manual-selection pulses. The deselect pulse and the selected combination of manual selection pulses go to the CD

selection circuits, where they produce a test-select-input field level. In figure 2–88, the GFI field is shown as an example. The same operations will be true for the other three input data and three OB data status control circuits. The select GFI input level, in this case, goes to the computer-test-control circuit.

If it is desired to write 1 bits in the status channel of the selected field, a manual-start-write pulse is developed in the select-manual-test-read-or-write-operation circuit. If it is desired to write 0 bits in the status channel, a manual-start-read pulse is produced.

During the writing of 1 bits, the manual-start-write pulse goes to the computer-test-control circuit and the CD-read-write-control circuit. The combination of the select-GFI level from the CD selection circuits and the manual-start-write pulse in the computer-test-control circuit produces a test-write-GFI level which goes to AND 1 in the GFI-OD-status-control circuit and to the manual-test-read-write-1-revolution-control circuit. The manual-test-read-write-1-revolution-control circuit is manually adjusted to produce a drum-disconnect pulse at the end of one revolution of the selected field. (Refer to 9.2.8 for a discussion of the manual-test-read-write-1-revolution-control circuit.) The drum-disconnect pulse goes to the CD-read-write-control circuit and produces a read-write-reset pulse. The read-write-reset pulse goes to the computer-test-control circuit and removes the test-write-GFI level.

AND 1, which is fed by the test-write-GFI level during the writing of 1 bits, conducts when it also receives a +10-volt level from the 1 side of FF 2. Flip-flop 2 is set to the 1 side by the presence of a 0 bit in the OD status channel. A 0 bit in the status channel produces a read circuit output too late to condition GT 1 to pass an OD 1 pulse from the LOG-drum-timing circuit. Flip-flop 1 therefore remains in the cleared state that resulted from the arrival of the previous OD 4 pulse. The 0 side level from FF 1 conditions GT 2 to pass the next OD 3 pulse. The gated OD 3 pulse sets FF 2. The FF 2 output joins the test-write-GFI level at AND 1. The resulting output of AND 1 conditions GT 3 to pass an OD 2 pulse which forms a test-data-available pulse input to OR 1. Normally, OR 1 gets data-available pulses from the Input System element with which the GFI-OD-status-control circuit is associated. Thus, OR 1 conducts upon receipt of the test-data-available pulse and, in turn, causes conduction in OR 2. OR 2 will also conduct as a result of detection of a 1 bit in the OD status channel. In this circumstance, FF 1 is set, but FF 2 remains in the cleared state in which it was placed by the previous OD 2 pulse. The 0-state-output level of FF 2 conditions GT 4 to pass an OD 1 pulse to OR 2. When OR 2 conducts, its output sets

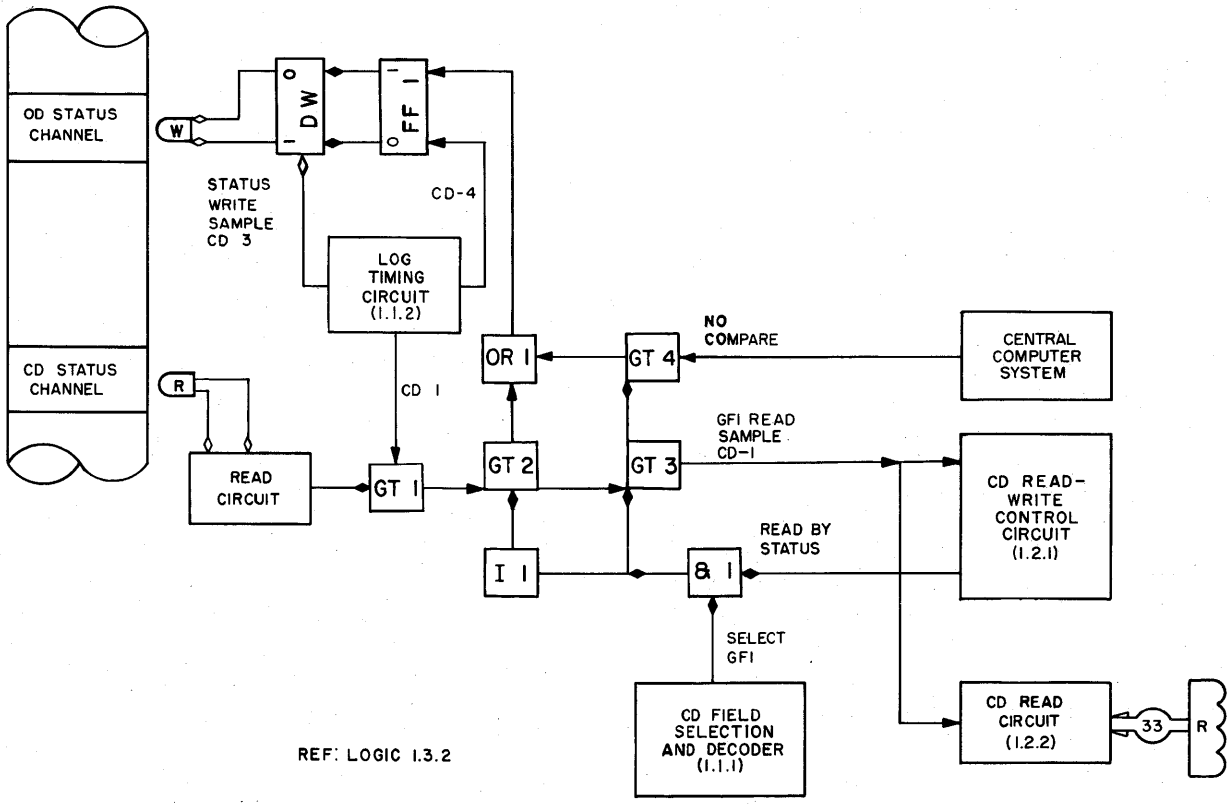


Figure 2–89. Writing OD Status Channel for Manual Test, Simplified Logic Diagram

FF 3, causing a 1 bit to be written in the CD status channel when the status-write-sample pulse is received.

It can be seen that, when a 1 bit is already present in the OD status channel, a 1 bit is automatically placed in the CD status channel. If a 0 bit is detected, a test-data-available pulse is produced because of the presence of the test-write-GFI level from the computer-test-control circuit. The test-data-available pulse substitutes for the data-available pulse produced during normal operation and causes the writing of a 1 bit in the CD status channel. Therefore, 1 bits are written in the CD status channel irrespective of whether a 0 or 1 is read in the OD status channel.

At the same time that 1 bits are being written in the CD status channel, 1 bits are also being written in the OD status channel. This operation is accomplished as follows: after the 1 bits have been written in the CD status channel, the individual bits pass under the CD status channel read head as the drum rotates (fig. 2–89). The read head is located in the CD-status-control circuit. The 1 bits are detected by the read circuit so that GT 1 is conditioned to pass one CD 1 pulse from the LOG-drum-timing circuit for each 1 bit on the channel. The GT 1 output goes to GT 2. Gate 2, in turn, is conditioned to pass the CD 1 pulses in the following manner: since a manual-test-write pulse is produced during the writing of 1 bits, the read-by-status level from the CD read-write-control circuit is absent at AND 1. With this level absent, AND 1 cannot conduct, thereby causing INVERTER 1 to produce an output level which conditions GT 2 to pass the CD 1 pulses from GT 1. The GT 2 output sets FF 1 via OR 1. The 1-state level of FF 1 causes the drum writer to write 1 bits in the OD status channel on receipt of status-write-sample pulses. This operation stops at the end of one revolution of the selected field. While the operation is in progress, however, 1 bits are written in every space on both the OD and CD status channels.

When it is desired to write 0 bits in the status channels, a manual-start-read pulse is produced by the select-manual-test-read-or-write-operation circuits. The manual-start-read pulse goes to the CD-read-write-control circuit, enabling the CD-read-write-control circuit to produce a read-by-status level. The read-by-status level goes to AND 1 in the CD-status-control circuit (shown in fig. 2–89). At this time, AND 1 conducts, cutting off INVERTER 1 and conditioning GT 3. If a 1 bit is detected in the CD status channel, GT 1 passes a CD 1 pulse, not only to GT 2, but also to GT 3. The latter produces a read-sample pulse which goes to the CD-read-write-control circuit. Since the Drum and Central Computer Systems are both in test operation, the no-compare pulse (normally returned when a word is to remain on a drum register) is not produced. Gate 4 receives no pulse input, and, therefore, no pulse appears at its output to produce conduction in OR 1. With no input to OR 1 and with GT 2 deconditioned, FF 1 remains in the 0 state in which it is placed by each CD 4 pulse from the LOG-drum-timing circuit. When a status-write-sample pulse is received, the drum writer places a 0 in the OD status channel.

After the bits are written in the OD status channel by the write head in the CD-status-control circuit, the drum rotates until the bits come under the read head in the OD-status-control circuit (shown in fig. 2–88). The absence of a manual-start-write pulse prevents the production of the test-write-GFI level. With no test-write-GFI level present in the GFI-OD-status-control circuit, the test-data-available pulse is not produced. Therefore, OR 1 does not conduct. Since only 0 bits have been written on the OD status channel by the OD-status-control circuit, all bits detected by the read head on the CD side are 0 bits. Flip-flop 1 is cleared throughout the drum revolution. Gate 2 thus passes every OD 3 pulse around the drum to set FF 2. Since FF 2 is always set at OD 3 time, an OD 1 pulse cannot be passed in GT 4 to produce conduction in OR 2. With the two input sources of OR 2 removed, FF 3 remains in the cleared state in which it is placed by each OD 4 pulse. Each status-write-sample pulse entering the drum writer from the LOG-drum-timing circuit thus causes the writing of a 0 bit. In this manner, the two status channels on each field can be filled with all 0 bits or all 1 bits.

9.2.7.2 Circuit Selection for Status-Control Manual Test

Selection of status control testing is accomplished by means of OB SELECTOR switch S5, ONES-ZEROS switch S4, and CIRCUIT SELECTOR switch S3. Figure 2–90 shows in diagram form the interrelation of these controls. A manual-test level from the begin-manual-test circuit is applied to ONES-ZEROS switch S4 and OB SELECTOR switch S5. The position of switch S4 determines whether ONES or ZEROS are on the status-control channel to be checked. In the ONES position, the manual-test level is applied to the pole of the A wafer of CIRCUIT SELECTOR switch S3. In the ZEROS position, the manual-test level is applied to the pole of the B wafer of CIRCUIT SELECTOR switch S3. The position of this switch determines which of the two status-control channels of a field is to be checked.

It can be seen that, with S4 in the ONES position and S3 in the OD-MI position, the manual-test level is applied to contact 3 of S3A, producing a check-manual-input-OD-1's-output level. This level goes to the manual-input-OD-status-control circuit to check the OD-status-control channel. In the same way, a check 1's or check 0's level can be sent to the status-control circuit for any field employing status control. When the CD status-control channel of any of the fields is to be

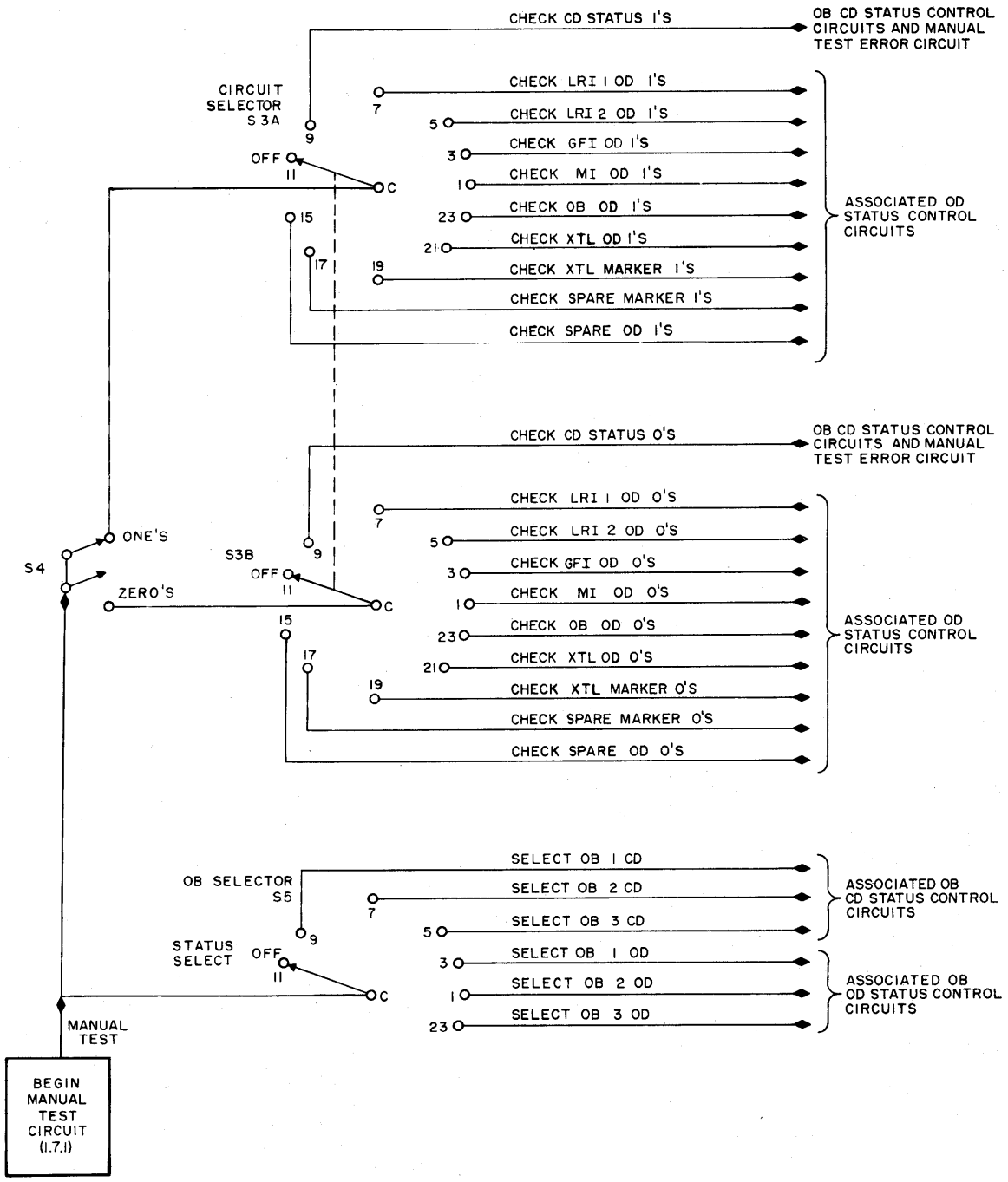


Figure 2–90. Field Selection Circuits for Status Control Channel Tests

checked, switch S3 is operated to the CD position.

An additional condition is imposed upon the status-control channel test for the OB fields. In addition to the setting of switch S4 to select a check of 1's or 0's and the setting of switch S3 to select OB OD or CD status-control channels, OB SELECTOR switch S5 must be operated to select the specific OB field to be checked. To test for 1's in the OD status-control channel for OB field 2, for instance, switch S4 has to be operated to the ONES position, switch S3 has to be operated to the OD-OB position, and switch S5 has to be operated to the OB2 OD position.

9.2.7.3 Manual Test for Input Fields OD Status Channels

The portions of the OD-status-control circuits that are used to check 1's or 0's after they have been written are shown in figure 2–91. During either check, the check-selected-status-circuit-OD-1's level is produced by setting the switches in the manual-test-for-status-control-selection circuits to the desired positions. When

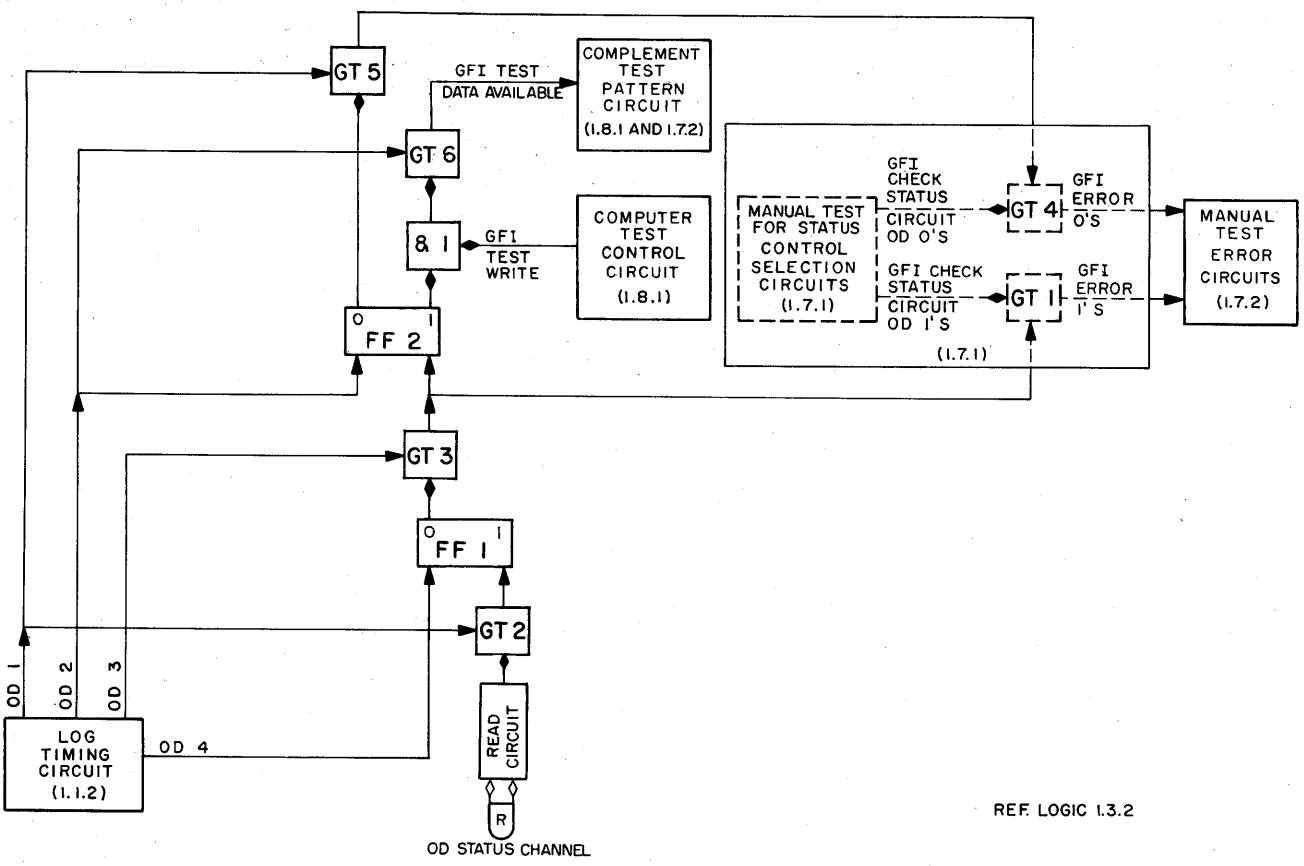


Figure 2–91. Manual Test Components of a GFI-OD-Status-Control Circuit, Simplified Logic Diagram

1's are being checked, the check-selected-status-circuit-OD-1's level is sent to GT 1. (In fig. 2–91, the GFI field is chosen as an example.) If one of the bits in the OD status channel is a 0 instead of a 1, FF 1 remains in the 0 state in which it has been placed by the last OD 4 pulse. The 0 state output of FF 1 conditions GT 3 to pass an OD 3 pulse to GT 1. Since GT 1 is conditioned by the GFI-check-status-circuit-OD-1's level, the OD 3 pulse is passed to the manual-test-error circuit as an error-1's pulse. In the manual-test-error circuit (discussed in 9.2.10), the error-1's pulse stops drum operation.

When 0's are being checked, the GFI-check-status-circuit-OD-0's level is sent to GT 4. If one of the bits in the OD status channel is a 1 instead of a 0, FF 1 is set. Gate 3 is therefore not conditioned in time to pass an OD 3 pulse. As a result, FF 2 remains in the 0 state in which it has been placed by the previous OD 2 pulse. The 0-state output of FF 2 conditions GT 5 to pass an OD 1 pulse. The gated OD 1 pulse is sent to GT 4. Since GT 4 is conditioned by the GFI-check-status-circuit-OD-0's level, the GT 5 output is passed to the manual-test-error circuit as an error-0's pulse. The error-0's pulse also stops drum operations.

During manual test write procedure for the selected field, the presence of a 0 in the OD status channel also produces an error-0's pulse. At such time, FF 1 again remains cleared long enough to pass an OD 3 pulse in GT 3. The GT 3 output sets FF 2. The 1-state output of FF 2 is added in AND 1 with the GFI-test-write level produced in the computer-test-control circuit when a manual test is selected. The resulting conduction in AND 1 conditions GT 6 to pass an OD 2 pulse which forms a test-data-available pulse. The test-data-available pulse goes to the complement-test-pattern circuit to produce the pattern-sense pulse (as described in 9.2.5).

9.2.7.4 Manual Test for Marker Status Channels

The check status channel OD 1's and 0's procedures are modified when the marker-status-control circuits are being examined. Figure 2–92 is the diagram of the XTL-OD-marker-status-control circuit. If a check is made for 1's in the OD status channel, the presence of a 0 in the OD channel permits FF 1 to remain cleared. The FF 1 output is added in AND 1 to the output of FF 2 (present when a 1 is read in the marker status channels). The output of AND 1 goes to GT 3 to condition the gating of an OD 3 pulse. The GT 3 output is passed by the XTL-status-check-for-1's level

at GT 1. The GT 1 output is the error-1's pulse which goes to the manual-test-error circuit. Thus, the only modification of the 1's check for the OD status channel in the marker-status-control circuits is the added condition of the presence of a 1 in the marker status channel when the OD status channel is read.

The check for 0's in the marker-status-control circuit is identical with the check for 0's in the normal-status-control circuit. If a 1 is present in the OD status channel, FF 3 remains cleared. Gate 6 is conditioned to pass an OD 1 pulse to GT 5. This pulse is gated by the XTL-status-check-for-0's level to form an error-0's pulse, which goes to the manual-test-error circuit.

Additional facilities are provided to check the contents of the marker status channel. If the marker status channel has been written to contain all 0's, the check-select-marker-for-0's level is produced in the manual-test-for-status-control circuits. This level conditions GT 9 to pass an output from GT 8. Gate 8 has an output only when a 1 is read in the marker status channel. The output of GT 9 produces conduction in OR 1. The pulse output of OR 1 is the XTL-marker-error pulse which goes to the manual-test-error circuit and stops drum operations.

When all the bits in the marker status channel have been written as 1's, the check-XTL-marker-for-1's level is produced in the manual-test-for-status-control selection circuits. This level provides an input to AND 2, which conducts only if FF 2 remains cleared at the OD 1 pulse following the OD 4 pulse which clears it. Flip-flop 2 remains cleared only when the channel contains a 0 bit and GT 8 does not pass a setting pulse to FF 2. When AND 2 does conduct, GT 10 is conditioned to pass an OD 3 pulse to OR 1, and the XTL-marker-error pulse is produced. (The test-data-available-pulse circuit has been described in 9.2.7.3.)

9.2.7.5 Manual Test for Input Fields, CD Status Channels, and OB OD Status Channels

One portion of the manual test element circuits is

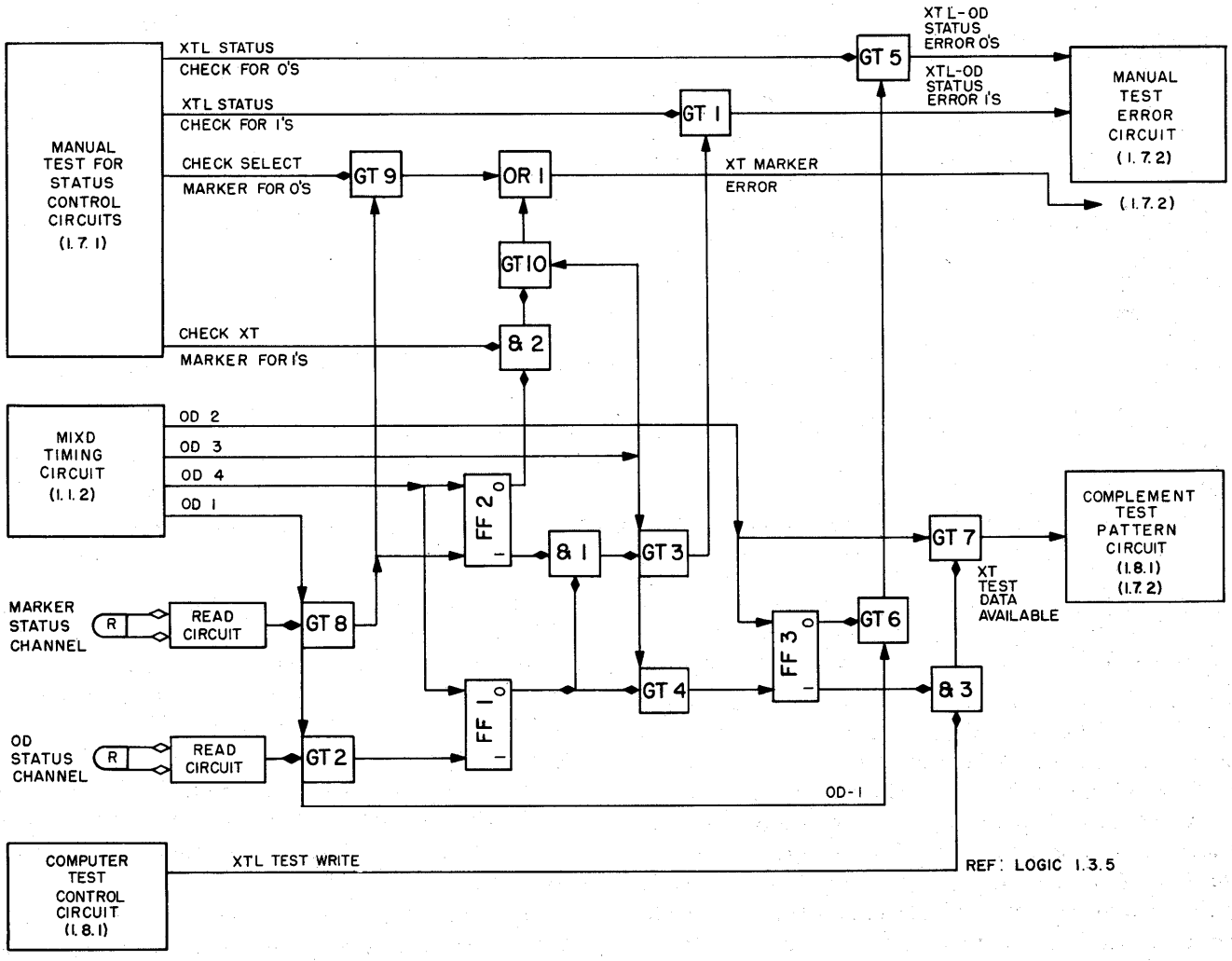


Figure 2–92. Manual Test Components of XTL-OD-Status-Control Circuit, Simplified Logic Diagram

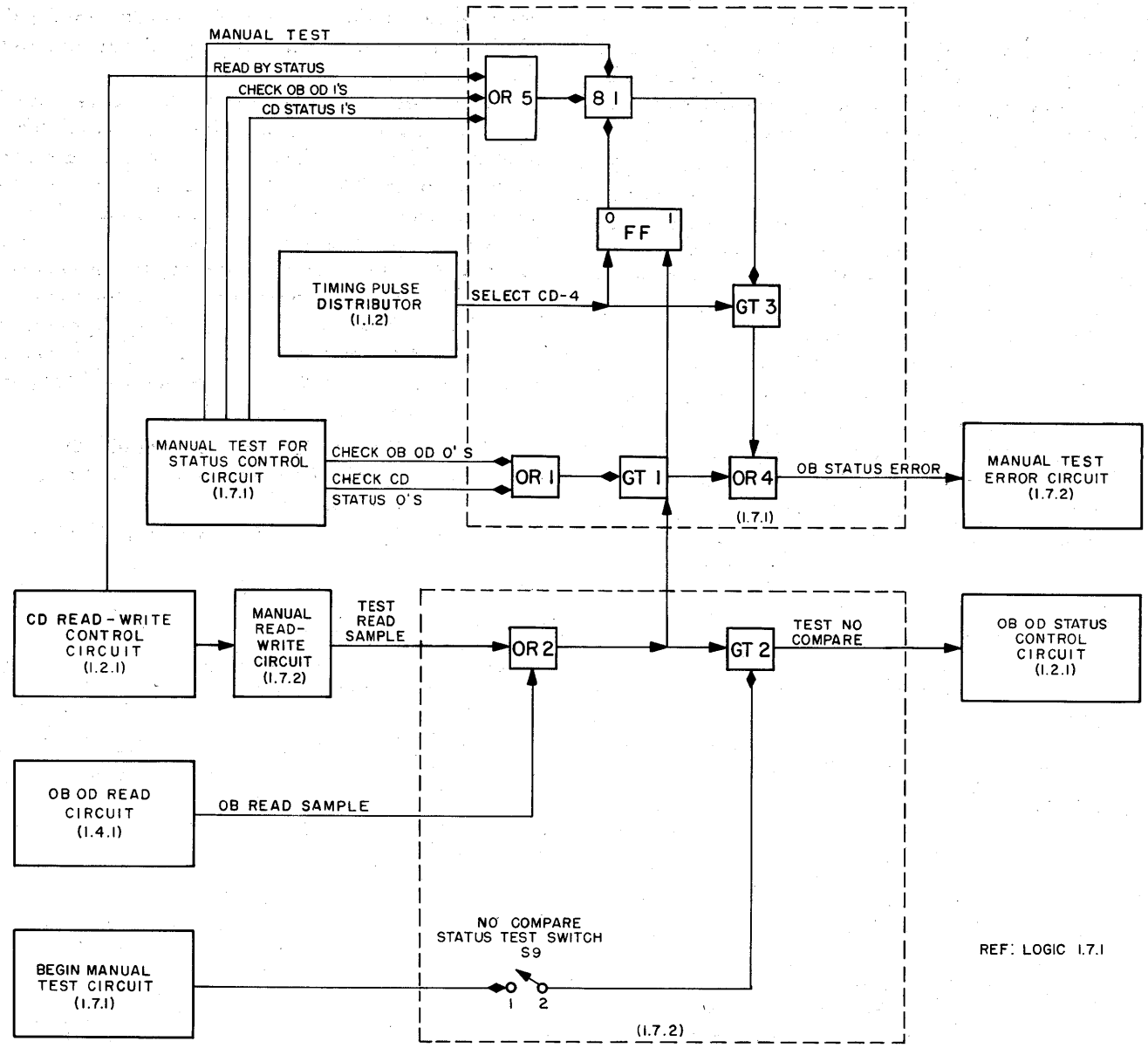


Figure 2–93. Manual-CD-Status-and-OB-CD-Status-Test-Control Circuit, Simplified Logic Diagram

devoted specifically to performing 1's and 0's checks on the CD status channels of the input fields and the OD status channel of the three OB fields (fig. 2–93).

During a check for 0's in any of the above-mentioned fields, a check-OB-OD-0's or a check-CD-status-0's level, as the case may be, is fed to OR 1. Thus, OR 1 conducts, sending a conditioning level to GT 1. Gate 1 receives a pulse input if the selection of any status control circuit for the check results in the production of a read-sample pulse (an OB-read-sample pulse from the OB-OD-read circuit, or a test-read-sample pulse from the CD-read-write-control circuit). A read-sample pulse can be developed by one of these circuits only when a 1 bit is detected in the respective CD status channel or OD status channel of the OB field that is being tested. The read-sample pulse from any of the possible sources provides the necessary input to GT 1. The resulting GT 1 output goes to OR 4, forming an OB-status-error pulse which goes to the manual-test-error circuit and stops drum operations.

The principle that read-sample pulses are produced only when a 1 bit is read in the selected-status-control circuit is employed in the check for 1's in the status channels.

The check-CD-status-1's level, the check OB-OD-1's level, and the read-by-status level are brought into OR 5. The output of OR 5 is added to the manual-test level from the manual-test-for-status-control circuit and

the 0-state level of the flip-flop in AND 1. If either read-sample pulse is present at OR 2, the flip-flop is set. If, however, there is a zero in the status channels, the read-sample pulses are not produced, and the flip-flop remains in the cleared state produced by a select-CD 4 pulse from the timing pulse distributor. AND 1, when conductive, produces the operating level for GT 3, which then passes the next select —CD 4 pulse. If the flip-flop had remained set, the rise time of the 0 side of the flip-flop would have exceeded the select-CD 4 pulse time. With GT 3 conditioned in time to pass the select-CD 4 pulse, however, an input is sent to OR 4. The OR 4 output is the OB-status-error pulse.

Should it be desired to perform a test requiring the use of a test-no-compare pulse, switch S9, the NO COMPARE STATUS TEST switch, is closed. This applies a manual-test level from the begin-manual-test circuit to GT 2. Should a read-sample pulse be produced, it is passed at GT 2 to form a test-no-compare pulse which goes to the OB-OD-status-control circuit.

9.2.7.6 Manual Test for OB CD Status Channel

The portion of the CD-OB-status-control circuit used during a manual test check for the contents of the OB CD status channel is shown in figure 2–94. In order to check 0's or 1's, the select-OB-1-CD-manual level must be produced in addition to the check levels. When checking for the presence of 0's in the channel (1's are errors), the select-OB-1-CD-manual level is added with the check-CD-status-0's level in AND 1. The output of AND 1 conditions GT 1. Gate 1 receives an input only if an error is present; that is, a 1 in the status channel. The resulting output of GT 1 is the select-OB-CD-error-0's pulse.

When checking for 1's in the channel (0's are errors), the select-OB-1-CD-manual level is added with the check-CD-status-1's level in AND 2. The output of AND 2 goes to AND 3, which conducts only if it gets another input from the 0 side of FF 1. Flip-flop 1 is cleared by each CD 4 pulse. If a 1 is read in the channel, FF 1 is set, and AND 3 can have no input. Flip-flop 1 remains cleared when a 0 (error) is detected in the CD status channel. The output of AND 3 produces conduction in OR 1, which also conducts if it receives a similar output from either of the other two OB-CD-status-control circuits. The OR 1 output goes to AND 4, which is also fed by the check-CD-status-1's level from the manual-test-for-status-control circuits. With both inputs present, AND 4 conditions GT 3 to pass the OB-write pulse from the CD-read-write-control circuit. The write pulse which is passed forms the OB-CD-error-status-1's pulse, which goes to the manual-test-error circuit and stops drum operations.

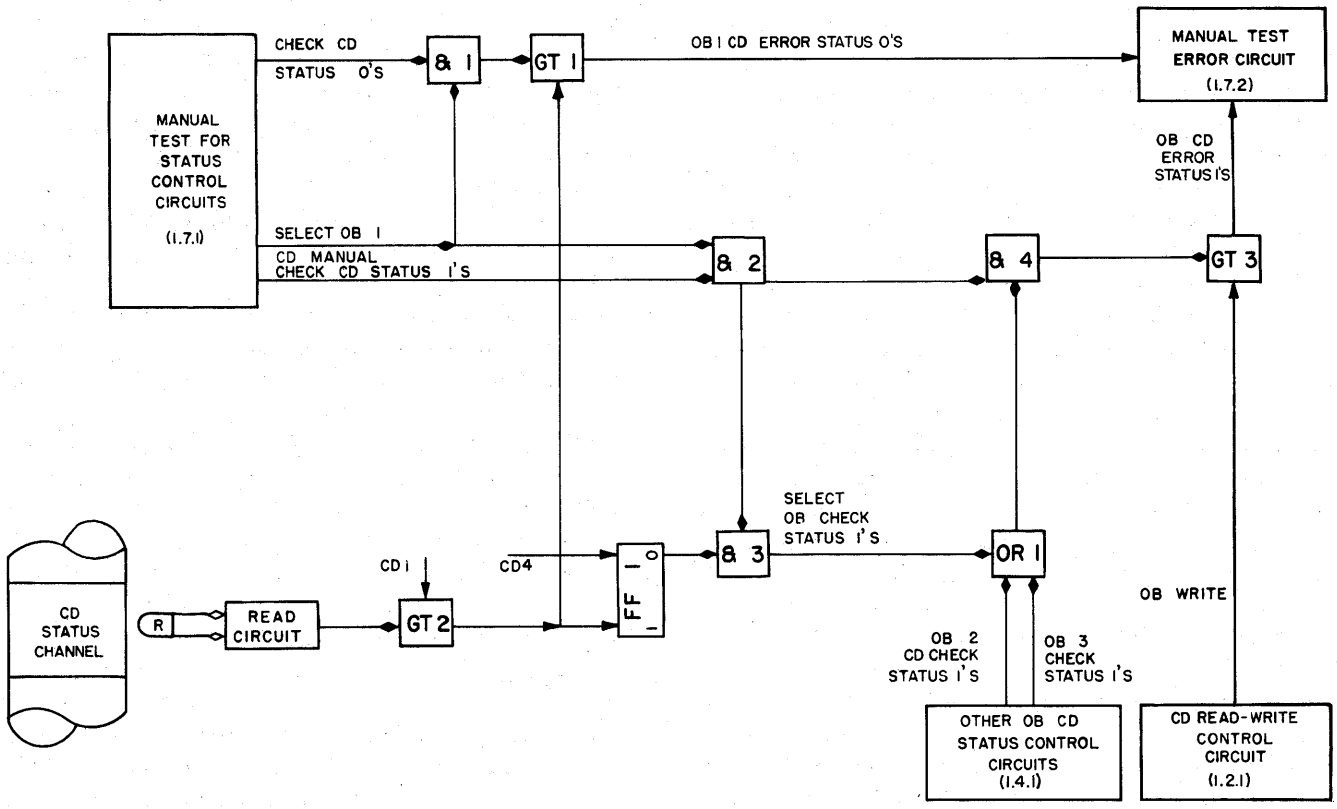


Figure 2–94. Test Components of OB 1 OD-Status-Control Circuit, Simplified Logic Diagram

9.2.8 Manual-Test-Read-Write-1-Revolution-Control Circuit

During most of the tests performed on the fields that read and write by status control or a modification of status control, it is desirable to test drum operations for only one drum revolution or its equivalent. The test read or write operation can be stopped at the end of one revolution of a drum field or at the end of the number of revolutions it takes to complete the read or write operation. The controls that stop the operation at the end of one revolution are shown in figure 2–95.

When OPERATE 1 REV switch S10 is closed, the manual-test level from the begin-manual-test circuit is applied to AND's 1, 2, 3, and 4. Of the four, AND 1 is associated with the display fields, AND 2 with the fields on the LOG drum (with the exception of the OB fields), AND 3 with fields on the MIXD drum (with the exception of the DD field), and AND 4 with the OB fields. The production of the CD-read-compare or CD-write-compare level (depending upon which operation is to be performed) by the CD-read-write-control circuit causes conduction in AND 1. This occurs after the first test-angular-position-counter-carry pulse. The output of AND 1 conditions GT 1 to pass the second test-angular-position-counter-carry pulse from the manual-test-angular-position-counter-alarm circuit. The second test-angular-position-counter-end-carry pulse is produced after all the registers of the field selected for test have had either a read or write operation performed on them. (Refer to 9.2.9 for a discussion of the manual-test-angular-position-counter-and-alarm circuit.) The output of GT 1 goes to OR 3, producing a LOG-disconnect-1-revolution pulse. The LOG-disconnect-1-revolution pulse goes to the CD-read-write-control circuit and stops the read or write operation that is in progress.

When the GFI or LRI-test-write level is sent to OR 2 by the computer-test-control circuit, AND 2 conducts. The output of AND 2 conditions the passing of a LOG-index pulse from the LOG-timing circuit in GT 2. The GT 2 provides a second source of the LOG-disconnect-1-revolution pulse at OR 3. Since the test-write levels at the input to OR 2 are formed when the index pulse from the LOG-timing circuit is received in the computer-test-control circuit, the test write operation lasts from the index pulse that forms the test-write level to the index pulse that causes the disconnect (one drum revolution).

Similarly, AND 3 conducts when an XTL, manual-input, or spare-test-write level is produced, causing conduction in OR 4, which then feeds AND 3. The AND 3 output conditions GT 3 to pass the following MIXD-index pulse to OR 5. The resulting OR 5 output is the MIXD-disconnect-1-revolution pulse, which stops the writing operation.

Conduction is produced in AND 4 when it receives both the OB-test level (formed when the reading of the first OB field begins) and the select-OB-3-OD level (formed when reading of the third OB field begins). The output of AND 4 conditions GT 4 to pass the next OB-field-switch pulse from the CD-OB-field-switching circuit. The only time GT 4 is conditioned to pass an OB-field-switch pulse is when all three OB fields have been read. At this time, the OB-field-switch pulse that is gated is the same pulse that causes a switch to OB field 1 from field 3. The output of GT 4 goes to OR 5, producing an all MIXD-disconnect-1-revolution pulse which stops the test-read operation.

9.2.9 Manual-Test-Angular-Position-Counter-and-Alarm-Control Circuit

The manual-test-angular-position-counter-and-alarm-control circuit (fig. 2–96) is used to provide a means of indicating the drum register being read or written when an error is detected during manual tests. This circuit is also used to check the precessed reading patterns used in the OD display element and to check the operation of the drum timing circuits.

The circuit controlling the operation of the manual-test-angular-position-counter-and-alarm circuit is shown in figure 2–96. The test select CD-index pulse is sent to OR 1 and causes it to conduct. The output of OR 1 goes to GT 1 and is passed to the 11-stage-angular-position counter as a clear-angular-position-counter pulse. The clear-angular-position-counter pulse clears the flip-flops in the 11-stage-angular-position counter, which is a standard serial-counting circuit. In tests on the manual-test-angular-position counter itself, the selected CD-index pulse is substituted by a reset-test-angular-position-counter pulse. The reset-test-angular-position-counter pulse is produced by applying a single pulse input to RESET jack J2 on the test door (fig. 2–81). In order for either pulse to be passed to the angular-position counter by GT 2, a not-error level from the manual-test-error circuit must be present at the gate. This level is always present except for the time at which an error is detected.

During all tests, except those on fields employing a precessed reading pattern, test-select-CD 3 pulses from the timing pulse distributor are fed to OR 2, which conducts, sending a pulse to GT 2. As with GT 1, GT 2 passes the output of its associated OR circuit only when a not-error level from the manual-test-error circuit is present. The output of GT 2 is the test-angular-position-counter-step pulse which goes to the 11-stage-angular-position counter. At the 2,048th select-CD 3 pulse, the angular-position counter forms a test-angular-position-counter-carry pulse which clears FF 1. (Flip-flop 1 is initially set by applying a single pulse to CONDITION ALARM jack J4.) At CD 1 time of the next register, a test-select-CD-index pulse from the timing

pulse distributor is fed to OR 1, causing the production of a clear-angular-position-counter pulse. The clear-angular-position-counter pulse clears the flip-flops of the 11-stage-angular-position counter and goes to GT 3. If a malfunction is present in the 11-stage-angular-position counter, the selected-drum-timing circuit, or the timing pulse distributor, the test-angular-position-counter-carry pulse is not developed in time to clear FF 1 before receipt of the clear-angular-position-counter pulse. The resulting 1-state level from FF 1 conditions the passing of the clear pulse by GT 3 to produce a test-angular-position-counter-error pulse. This pulse goes to the manual-test-error circuit and indicates an error in the counting operation. It also sets FF 3, causing neon lamp I48 to light and thereby providing visual indication of the presence of an error. In the manual-test-error circuit, the test-angular-position-error pulse causes the not-error-conditioning level to be removed from

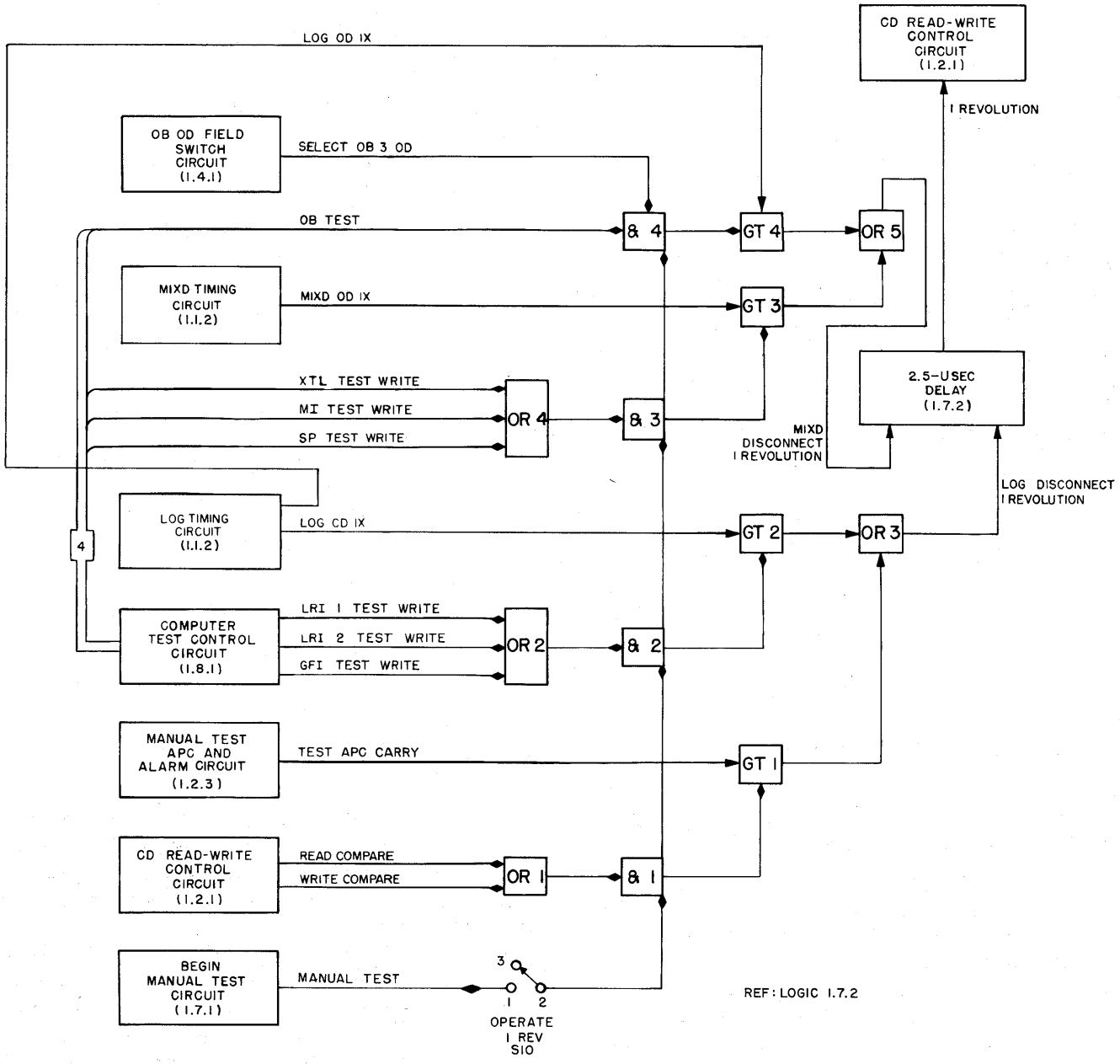


Figure 2–95. Manual-Test-Read-Write-1-Revolution-Control Circuit, Simplified Logic Diagram

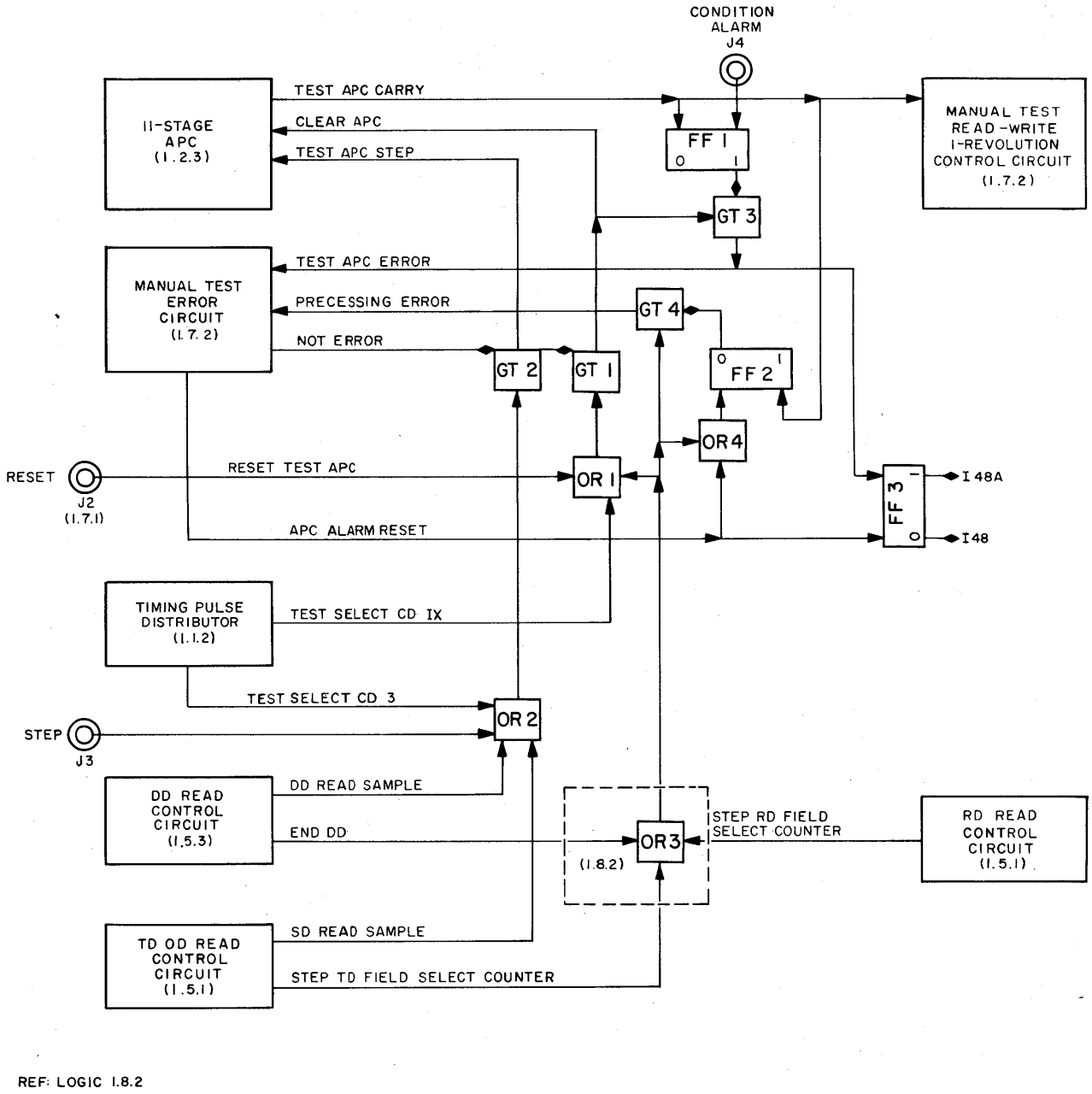


Figure 2–96. Manual-Angular-Position-Counter-and-Alarm-Control Circuit, Simplified Logic Diagram

GT's 1 and 2. Counting in the 11-stage counter is therefore stopped and cannot be resumed until the not-error level is returned.

If an error is detected at any time during a test on other circuits, the presence of that error in the manual-test-error circuit causes also the removal of the not-error level. Should this error occur during the middle of a drum revolution, the removal of the not-error level from GT's 1 and 2 will stop the counter. Neon indicating lamps are connected to the flip-flops in the 11-stage counter and indicate the setting of the counter at the time counting is stopped.

During tests on fields employing precessed reading patterns, it is necessary that all registers be read even though register reading is not sequential. To check this operation, the manual-test-angular-position-counter-and-alarm circuit counts the number of read-sample pulses produced during the reading of a field without respect to the number of drum revolutions required. Thus, when the DD field is being tested, DD-read-sample pulses from the DD-read-control circuit are received at OR 2. They are passed in GT 2 to form test-angular-position-counter-step pulses. The 2,048th DD-read-sample pulse counted forms a test-angular-posi-

tion-counter-carry pulse which sets FF 2. Setting FF 2 removes the 0-state level from GT 4. At the OD 3 time which follows 5 usec after the 2,048th DD-read-sample pulse, an end-DD pulse from the DD-read-control circuit arrives at OR 3 and is conducted to GT 4. In addition, it causes conduction in OR's 1 and 4, clearing FF 2 and causing the production of a clear-angular-position-counter pulse at GT 1. If the number of DD-read-sample pulses produced was insufficient to produce a test-angular-position-counter-carry pulse, FF 2 is cleared before the end-DD pulse arrives, and GT 4 is conditioned in time to pass the end-DD pulse from OR 3 to the manual-test-error circuit. The GT 4 output is the precessing-error pulse. During tests on the RD and TD fields, operation is the same as in the case of the DD field. Situation-display-read-sample pulses from the TD OD-read-control circuit replace the DD-read-sample pulses at OR 2. Step-TD-field-selector-counter pulses from the TD-OD-read-control circuit (or step-RD-field-selector-counter pulses from the RD-read-control circuit) replace end-DD pulses.

Test-angular-position-counter-carry pulses are sent to the manual-test-read-write-1-revolution-control circuit whenever they are produced, to be employed by the latter circuit as a means of stopping manual tests at the end of one drum revolution or its equivalent. This operation is described in 9.2.8.

9.2.10 Manual-Test-Error Circuit

The manual-test-error circuit (shown in fig. 2–97) provides a means of stopping drum operations when errors are detected during manual test and some normal operating procedures.

The presence of a 1 bit in the left-half word of

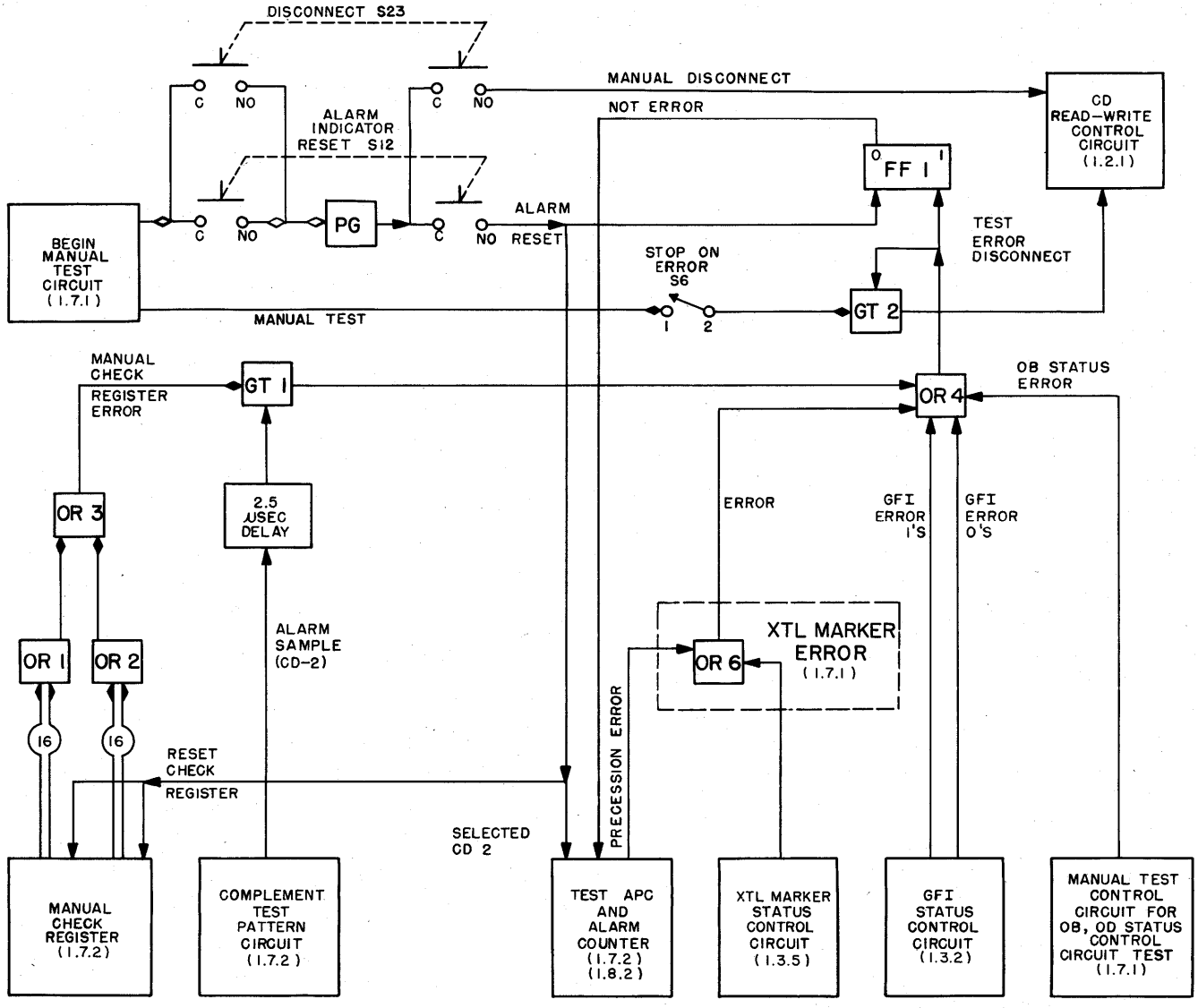


Figure 2–97. Manual-Test-Error Circuit, Simplified Logic Diagram

the manual-check-register circuit following a complement of the register flip-flops indicates an error in a pattern test. The 1 bit causes conduction in OR 1. In the same way, an error in the right half of the check register word is indicated by a 1 bit that causes conduction in OR 2. If OR 1 or 2, or both, have an input, the resulting output produces conduction in OR 3. The output level produced by OR 3 (manual-check-register-error level) conditions GT 1 to pass an alarm-sample pulse from the complement-test-pattern circuit (refer to 9.2.5) to OR 4, which produces an output pulse, setting FF 1, the not-error flip-flop. Inputs other than the GT 1 output cause conduction in OR 4. These inputs are error-1's or error-0's pulses from a status control circuit that has been selected for a status control channel check, an OB-status-error pulse from the manual-CD-status-and-OB-OD-status-tests-control circuit, or an output from OR 6. An OR 6 output is developed when a precession-error is received from the test-angular-position-counter-and-alarm circuits, or an XTL-marker-error pulse from the XTL-marker-status-control circuit. When FF 1 is set, the 0-state-output level, known as the not-error level, is removed from the test-angular-position counter and stops the counting operation. Neon indicators associated with the test-angular-position counter are lighted to indicate the drum register on which the error occurred. If STOP ON ERROR switch S6 has been operated, GT 2 is conditioned to pass the output of OR 4 to the CD-read-write-control circuit as a test-error-disconnect pulse. The test-error-disconnect pulse stops the test at the point at which the error is detected.

A manual-disconnect pulse, which has the same effect as the test-error-disconnect pulse, the Central-Computer-System-disconnect pulse, the status-disconnect pulse, or the OB disconnect pulse, is generated by depressing the DISCONNECT pushbutton.

In order to resume operations on the field being tested or on a new field, it is necessary to depress the ALARM INDICATOR RESET pushbutton. The ALARM INDICATOR RESET pushbutton, like the DISCONNECT pushbutton, applies a level to the pulse generator, causing a single pulse to be produced across the second pair of pushbutton contacts. This pulse goes to FF 1 as an alarm-reset pulse which clears the flip-flop and brings the not-error level up again. The pulse goes to the test-angular-position-counter-and-alarm circuit as an angular-position-error-reset pulse. In the test-angular-position-counter-and-alarm circuit, the angular-position-counter-error-reset pulse returns the counting circuits to the 0 state. The alarm-reset pulse also produces a reset-check-register pulse, which clears both halves of the manual check register.

9.3 TIMING REWRITE AND ERASE CONTROLS

The magnetic flux patterns on the drums which represent binary data are normally changed only by being written over or by accidental introduction of spurious fields. In certain cases, such as periods following maintenance or during installation, it is desirable to clear all information from the drum surface. This is accomplished by an erasing operation.

When a drum is erased, its surface is cleared of all magnetic flux patterns, including any random fields that might have been established by noise in the drum writing head. The timing and index channels are automatically rewritten after each erasure. The erase-rewrite circuits and components are described in the paragraphs that follow and are shown in detail on logic 1.7.3.

Demagnetization of the drums is performed by passing an alternating current of gradually decreasing magnitude through the coils on the drum erase bar. A view of a drum erase coil is shown in figure 2–98. The erase bar consists of a metal channel with a centerpiece which serves as an electromagnetic core for four coil windings. The coils are electrically connected in series-parallel, as shown in figure 2–98.

One assembled drum erase bar is mounted on each of the drums. The erase bars are placed between read-write bar 1 and the drum casting (fig. 2–99). It should be remembered that, although the erase bars are physically fixed on the drums, erasing (and automatic rewriting of the timing channels) is not a continuous operation. Manual controls on the unit 21 test door or on the maintenance console must be operated to erase any of the main drums and to write the timing and index channels for that drum.

9.3.1 Erase Circuitry

The circuit employed to apply an alternating current of gradually decreasing magnitude is shown in figure 2–100. Relay K4 is energized by moving TEST MODE SELECTION switch S2 on the module 21L test door (fig. 2–81) to the MANUAL TEST position. The drum to be erased is selected by rotating DRUM SELECTOR switch S33 to the appropriate position.

Contacts 16 and 17 of the relay apply 115-volt, 60-cycle power to the erase circuit. To apply power to the erase motor, either one of two switch circuits is used. With DRUM ERASE pushbutton S34 depressed and held down, and with DRUM SELECTOR switch S1 on the maintenance console turned to the OFF position, the 60-cycle erase supply voltage is applied to the erase motor. This voltage may also be applied through the OFF position of DRUM SELECTOR switch S33 on the module 21L test door when ERASE AND TIMING WRITE switch S4 on the maintenance console is depressed and held down. In this event, drum selection is made by means of DRUM SELECTOR switch S1 on

the maintenance console. Either DRUM SELECTOR switch S1 or DRUM SELECTOR switch S33 may be used to activate the drum selector relays.

The erase motor is a 2-revolution-per-minute motor which drives the voltage output amplitude control on the variable transformer. As the drum erase motor turns, it drives a cam which closes the contacts of switch S1. When S1 closes, it bypasses the circuits containing the erase pushbuttons and applies power to the motor and the variable transformer. Resistance-capacitance networks R1 and C1, and R2 and C2, are in parallel with S1 to protect the switch contact from arcing. When S1 closes, neon bulb X111 on the test door of module 21L (shown in fig. 2–100) lights, indicating that the erase pushbutton can be released. Switch S1 remains closed for 30 seconds, during which time the variable transformer is slowly turned until its output voltage is reduced to zero. At the end of 30 seconds, the motor-driven cam reopens the switch contacts, and the a-c source is removed.

The output of the variable transformer is applied through the contacts of the drum selection relays to any or all of the erase heads. During erasure, the selected drum rotates at normal speed.

9.3.2 Drum-Timing-and-Index-Channel-Write Circuits

Whenever a drum is erased, the timing and index channels of that drum are automatically rewritten. Both channels are rewritten at the same time by means of the component circuits shown in block form in figure 2–101. These circuits are arranged in logical order to show the transfer of signals from one circuit to another during a timing-and-index-write operation. The drum selection relays and the timing-and-index-channels-write circuits are described in the paragraphs that follow. The optical transducer, the optical frequency generator, and the timing pulse generator are described in Part 4.

9.3.2.1 Timing-and-Index-Channel-Write Circuit, Circuit Analysis

Only one of the six optical transducers and frequency generator assemblies can be operated at a given time. The assembly to be used is chosen by means of DRUM SELECTOR switch S33 on the unit 21 test door or switch S1 on the maintenance console. The timing-and-index write operation follows automatically the erase operation described in 9.3.1.1. In the event that all six drums are selected for erasure, each of the six

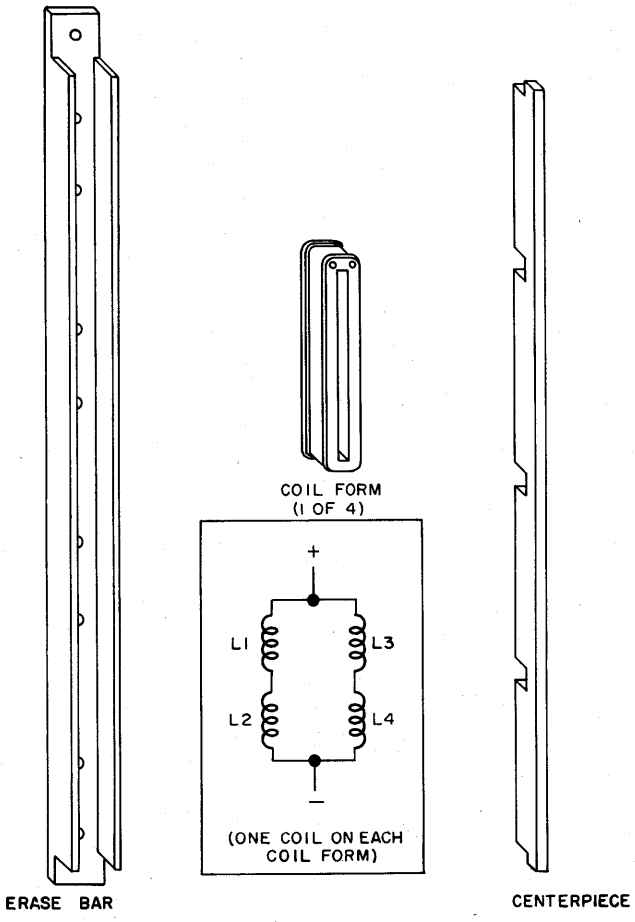


Figure 2–98. Erase Bar Components

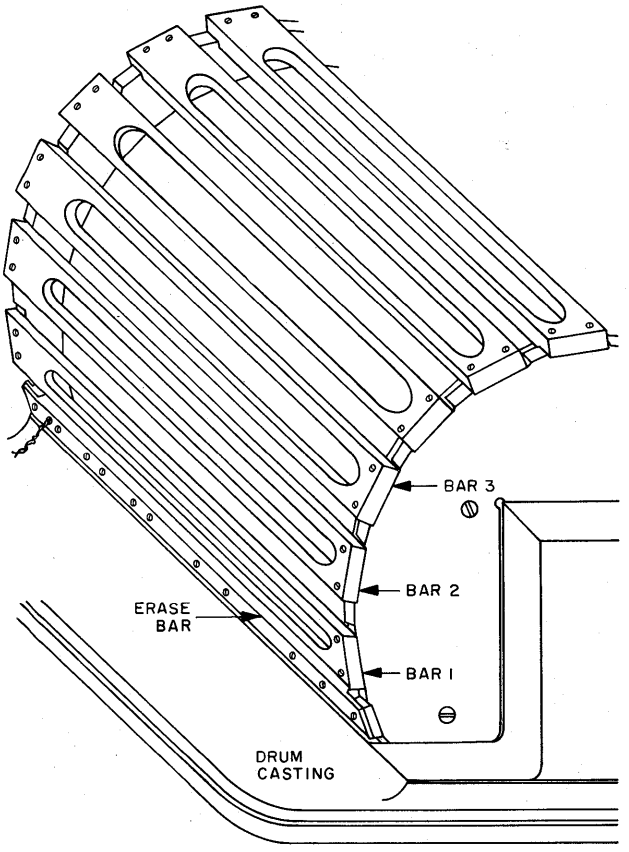


Figure 2–99. Erase Bar Shown in Position on Drum

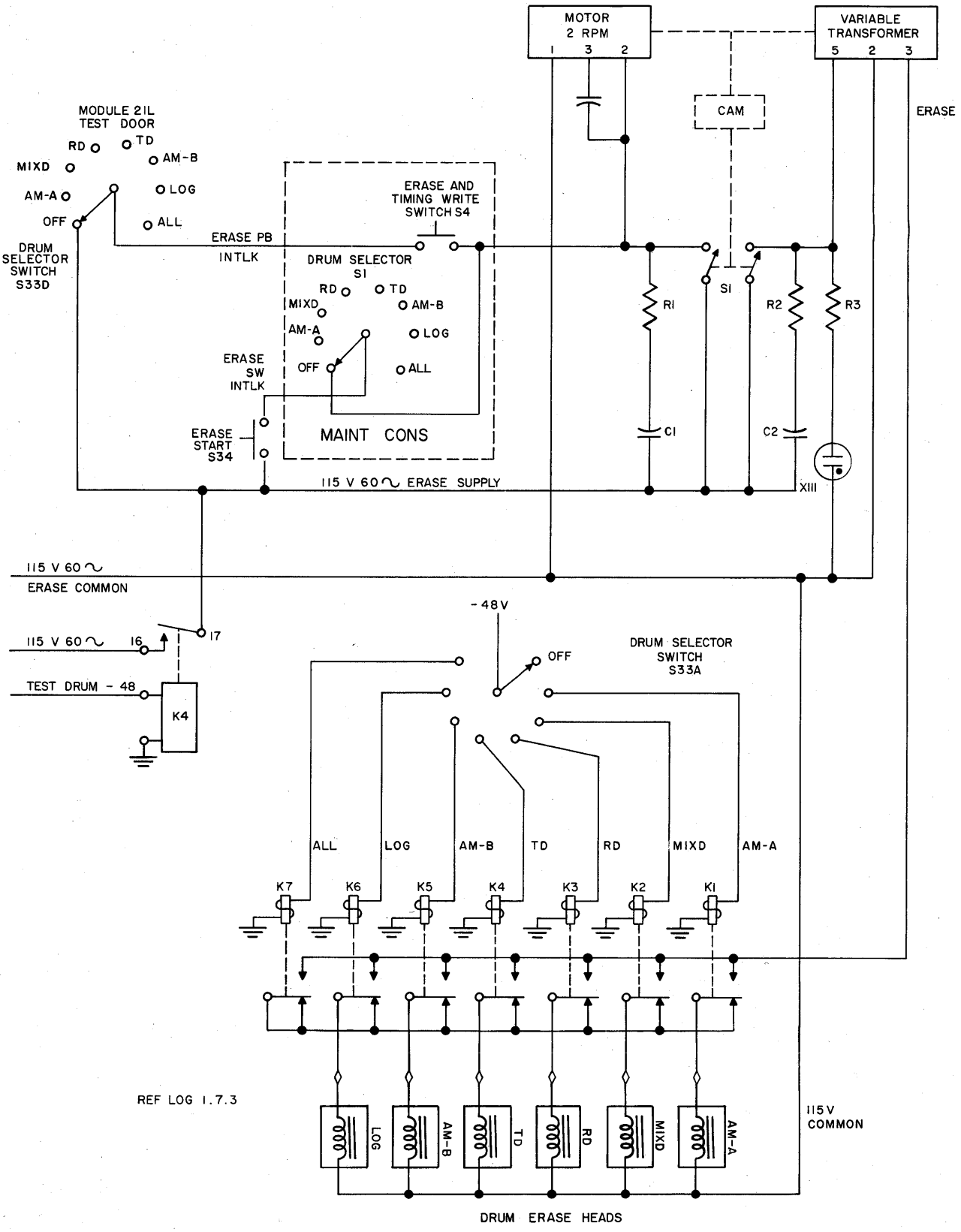


Figure 2–100. Erase-Rewrite-Start Circuit, Simplified Schematic Diagram

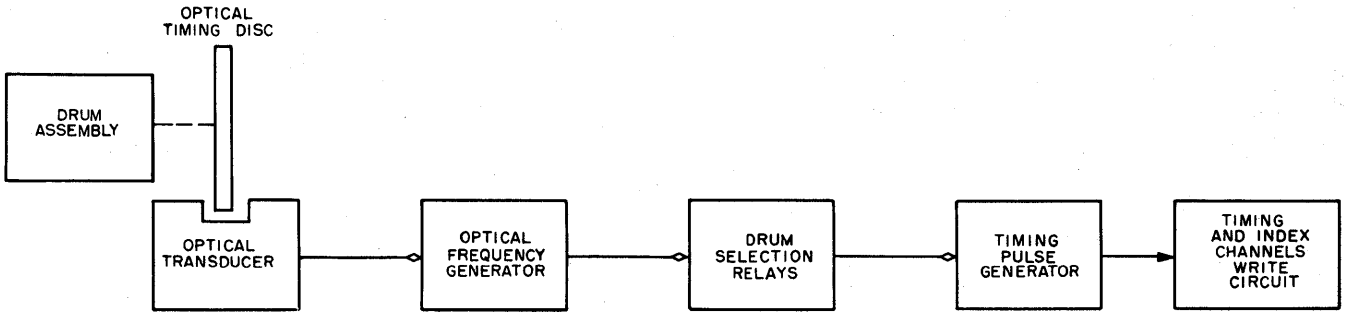


Figure 2–101. Writing of Timing and Index Channels, Block Diagram

drums will be erased at the same time; however, the automatic writing of the timing and index channels for these drums will be performed sequentially, beginning as soon as the erasure is completed. (The automatic sequential selection of the drums for the timing-and-index-channel write operation is described in 9.3.2.2.)

Operation of one of the drum selector switches, say DRUM SELECTOR switch S33, determines which optical frequency generator has operating voltages applied to its circuits.. Operation of S33 to the LOG position applies —48 volts to LOG drum selection relay K6. Contacts 1—2 and 3—4 of K6 close, applying a +250-volt level and a —300-volt level to the LOG optical frequency generator (fig. 2—102). Energizing the drum selection relays of a drum applies the 100-kc sine wave from the output of the optical frequency generator to the timing pulse generator through one pair of the relay contacts. Energizing the drum selection relays also

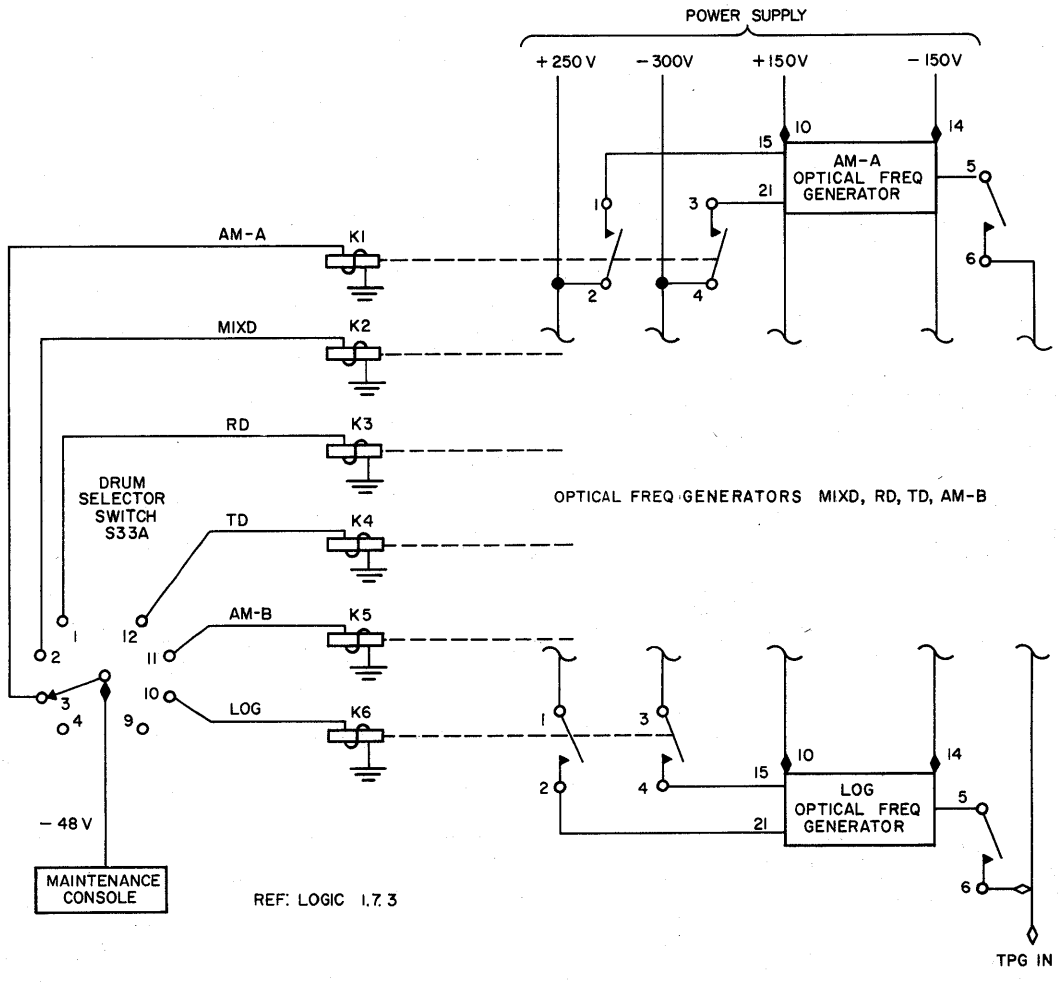


Figure 2–102. Drum Timing and Index Channel Writing, Selection Switches, Simplified Schematic Diagram

applies the output of the drum writers to the writing heads on the timing and index channels of the selected drum. The writing heads are fed through contacts of the appropriate drum selection relay (fig. 2–103). It should be noted that the test-drums level from the maintenance console reaches the drum selection relays only if TEST MODE SELECTION switch S2 on the test door of module 21L is in the MANUAL TEST position.

When the erasure operation is completed, a drums-erased level (fig. 2–103) is applied to control relay

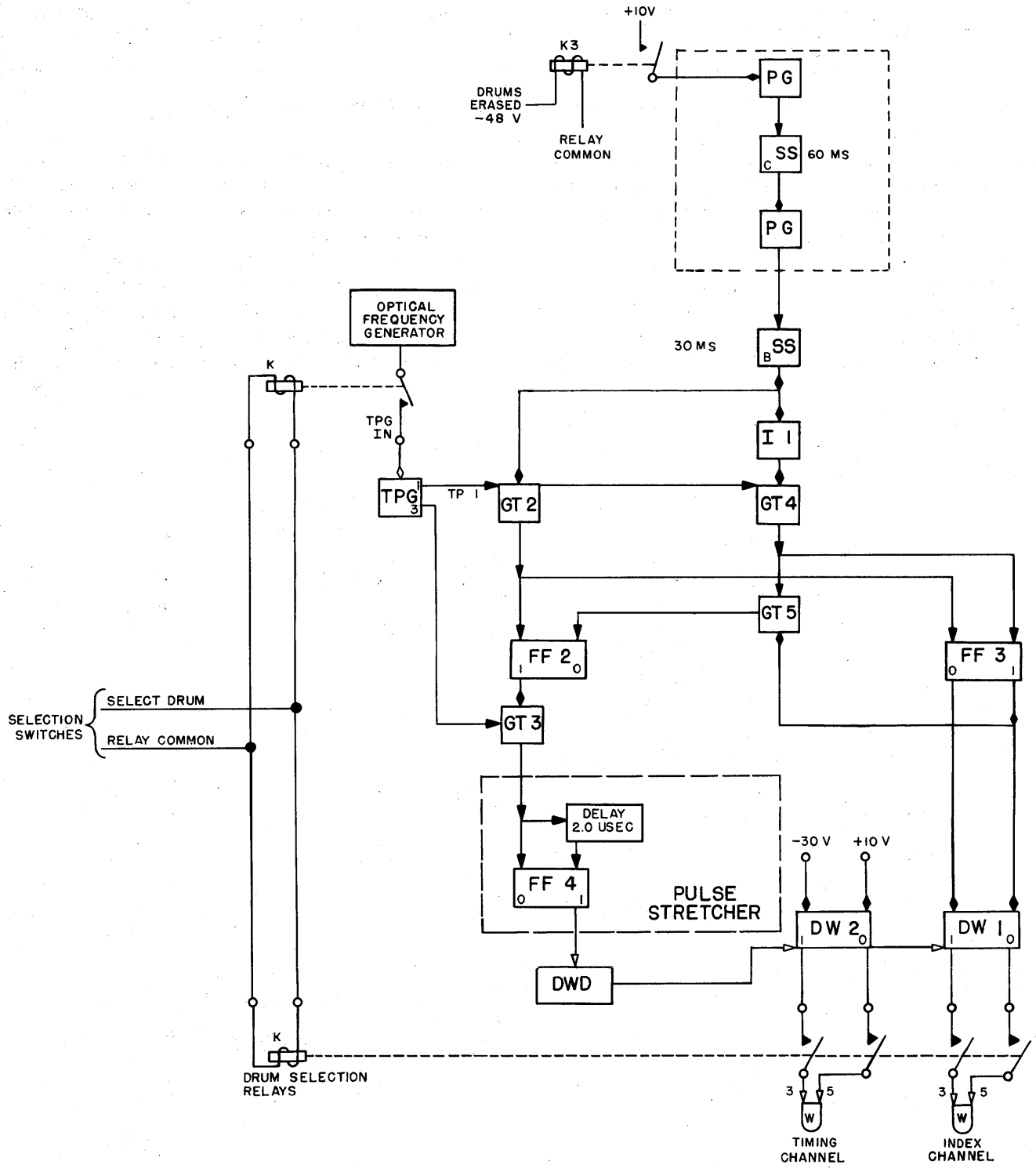


Figure 2–103. Timing-and-Index-Channel-Write Circuit, Simplified Logic Diagram

K3. The contacts of K3 close, causing +10 volts to be applied to pulse generator (PG) 1, which thereupon generates a single 0.1-usec pulse.

The output of PG 1 triggers single-shot multivibrator ₐSS. The single-shot multivibrator triggers PG 2, which cannot be triggered again until the 60-ms delay of ₐSS has expired. The output of PG 2 triggers the ₙSS single-shot multivibrator, whose waveform persists for 30 ms. The output of the ₙSS goes to GT 2 to operate as a conditioning level and to INVERTER 1 to prevent conduction in GT 4.

During the 30 ms that GT 2 is conditioned, TP 1 pulses from the timing pulse generator are passed to set FF 2 and clear FF 3. The 0-state output of FF 3 goes to drum writer 2. The 1-state output of FF 2 conditions GT 3 to pass the TP 3 pulses from the timing pulse generator. Each TP 3 pulse passed in this manner goes to the pulse stretcher. In the pulse stretcher, the TP 3 pulse clears FF 4 and sets it 2.0 usec later via the action of the delay line. During the 2.0 usec when FF 4 is in the 0 state, the drum write driver conducts, transferring the contents of the drum writers to the drum heads. The contents of the drum writer for the timing channel will always be 1 bits. During the 30 ms that GT 2 is conditioned, the contents of the index drum writer will be 0's. In this manner, 1 bits are placed in the timing channel once every TP 3 time for 1-½ drum revolutions. Since the sine-wave etching on the optical timing disc is continuous, having no distinguishable beginning or end, and since the sine waves on this disc cause the generation of TP 3 pulses, 1 bits written during the first half of the second drum revolution are written directly over those written during the first drum revolution.

During the time that the timing channel head is writing 1 bits, drum writer 1 feeds 0 bits to the write head on the index channel.

When the 30 ms are over, the output of the single-shot multivibrator goes negative. Gate 2 is no longer conditioned, and INVERTER 1 conducts, conditioning GT 4. Gate 4 passes TP 1 pulses to set FF 3. Flip-flop 3 now places a 1-state level in drum writer 1. At the next TP 3 pulse, therefore, a single 1 bit is written in the index channel by another TP 3 pulse, a TP 1 pulse in the index channel by another TP pulse, a TP 1 pulse is passed by GT 5, which has been conditioned by the 1-state output of FF 3. The passed TP 1 pulse clears FF 2, preventing further production of 2.0-usec pulses by the drum write driver. Thus, operation of the timing-write circuit causes the writing of 2,048 (or 2,060 in the case of the RD and TD drums) 1 bits in the timing channel and a single 1 bit in the index channel of the selected drum.

9.3.2.2 Timing-and-Index-Channel-Write Sequencing, Circuit Analysis

In the event that all drums are selected for erasure, they are all erased simultaneously. The writing of the timing and index channels of the drums starts automatically after the erasing operation. This operation is performed on one drum at a time, the drums being automatically selected in sequence.

Figure 2–104 illustrates the drum sequential selection circuitry. At the start of the drum erasing operation (described in 9.3.1.1), relay K1 is energized by 115 volts from the erase motor cam switch. Stepping

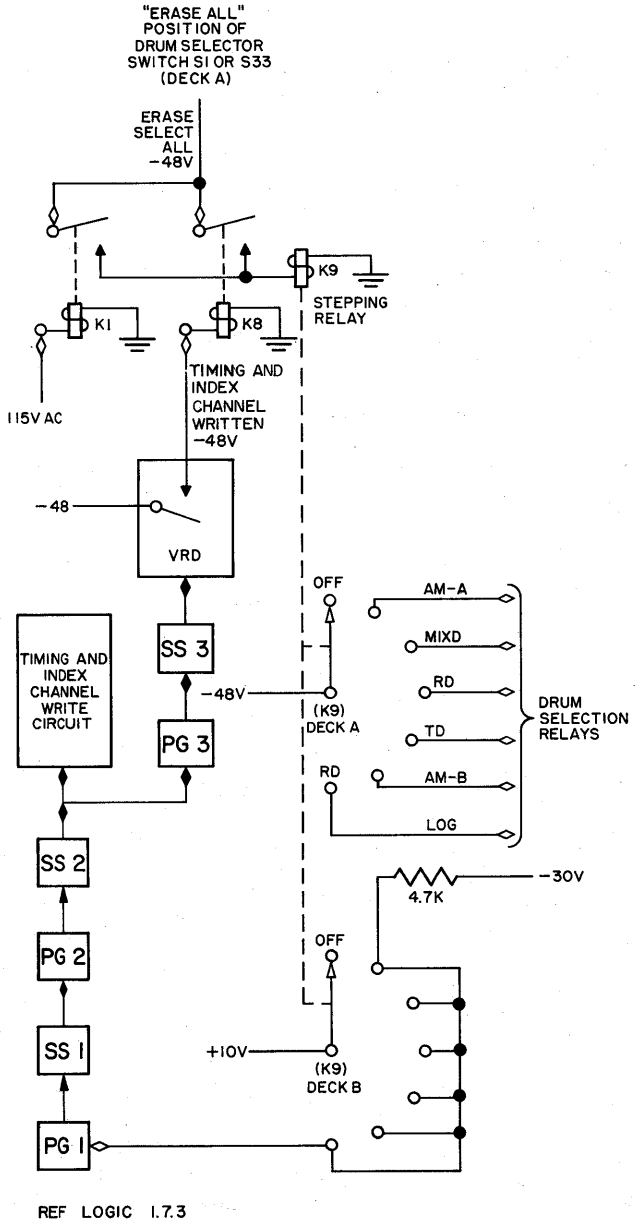


Figure 2–104. Timing-and-Index-Channel-Write Sequencing, Simplified Schematic Diagram

relay K9 is energized via the contacts of relay K1. When stepping relay K9 is energized, its stepping mechanism is cocked. At the conclusion of the drum erasing operation, relay K1 and stepping relay K9 are de-energized. When stepping relay K9 is de-energized, its stepping mechanism is tripped, causing the contact arm of deck A to move from the OFF position to the first position (AM-A). In the AM-A position, the AM-A drum selection relay (K1, fig. 2,—102) is energized, selecting the AM-A drum for the timing-and-index-channel write operation.

At this time, +10 volts from deck B of stepping relay K9 is applied to PG 1, which thereupon generates a single 0.1-usec pulse. This pulse triggers single-shot circuit 1, producing a positive level of 60-ms duration, which conditions PG 2. The output of PG 2 triggers single-shot circuit 2, producing a positive level of 30-ms duration. The output of single-shot circuit 2 is applied to the timing-and-index-channel write circuit to initiate the writing of the timing and index channels. (Refer to 9.3.2.1 for a description of the timing-and-index-channel-write operation.)

The output of single-shot circuit 2 is also applied to PG 3, whose output triggers single-shot circuit 3. The output of single-shot circuit 3 persists for 60 ms, during which time the vacuum-tube relay driver contacts are closed, generating the timing-and-index-channel-written level. This level energizes relay K8. Actuation of K8 causes the erase-select-all level from selector switch S1 to re-energize stepping relay K9, thereby cocking the stepping mechanism. The timing-and-index-channel-written level persists for 60 ms; at the end of this time, K8 and K9 are de-energized. When K9 is de-energized, its stepping mechanism is tripped, causing the contact arm to move from the first position (AM-A) to the second position (MIXD). In the MIXD position, the MIXD drum selector relay is energized, selecting the MIXD drum for the timing-and-index-channel write operation.

The foregoing operation is repeated until the timing and index channels of the six drums are written. At the completion of writing on the last drum, the stepping relay contact arm will have progressed to the OFF position in preparation for a new erase-rewrite operation.

9.4 DRUM-MOTOR-CONTROL CIRCUITRY

In previous discussions of the operation of the components of the Drum System, it was assumed that the six drums were rotating. This section describes the operation of the drum-motor-control unit, which contains the controls and circuits that control drum rotation.

9.4.1 Drum-Motor Circuit, Circuit Analysis

Each of the drums in the Drum System is rotated by a toothed pulley, which is driven by a ½-horsepower motor. The pulley arrangement between a typical drum and drum motor is shown in figure 2—105. The drum motors are synchronous a-c motors operating on 3-phase, 60-cycle power at 208 volts. Power control circuits for these motors are shown in figure 2—106.

The drum motors are numbered 1 through 6: motor 1 drives the AM-B drum; motor 2, the LOG drum; motor 3, the RD drum; motor 4, the TD drum; motor 5, the AM-A drum; and motor 6, the MIXD drum.

The a-c power necessary to operate each drum motor is applied through manually operated circuit breakers in the starting circuit. The circuit breakers are numbered to correspond to the numbers of their respective motors: circuit breaker (CB) 1 is in the circuit of motor 1, CB2 is in the circuit of motor 2, and so on. Each circuit breaker is provided with a thermal and a magnetic overload device that protects the motor windings from short circuits and prolonged overload conditions in the power supply. An auxiliary switch is connected to the poles of each of the circuit breakers. This switch contains one normally closed set of contacts (contacts B) and one normally open set of contacts (contacts A). The functions of these switches are described in 9.4.2.

When the circuit breaker is closed, auxiliary switch A contacts close and the B contacts open. Should an overload or short circuit occur during motor operations, the circuit breakers are thrown to the TRIP position. The circuit breaker contacts open, and the auxiliary switch contacts reverse their status. After a circuit breaker trips, it is necessary to operate the switch to the RESET position to resume service. The fourth position, the OFF position, opens the circuit breaker and auxiliary switch A contacts but closes the auxiliary switch B contacts.

The voltages applied through any circuit breaker must be conducted through the contacts of an associated magnetic contactor in order to start the drum motor. Magnetic-contactor contacts M1 through M6 are closed by the drum-motor-control circuit (refer to 9.4.2). Other magnetic-contactor circuits (described later) control MOTOR ON and MOTOR OFF lights.

An additional protective device, an overload relay (OLR) with saturating shunts, is connected directly in series with the phase 3 and phase 1 windings of the motor. The overload relay coils energize in cases of rapid current change, such as would be produced by a short circuit. Power is removed from the motor when the coil opens the overload relay contacts, which are connected in the drum-motor control circuits (shown in fig. 2—107). Other overload relay contacts are connected in the circuit of control relay CR10 and in each

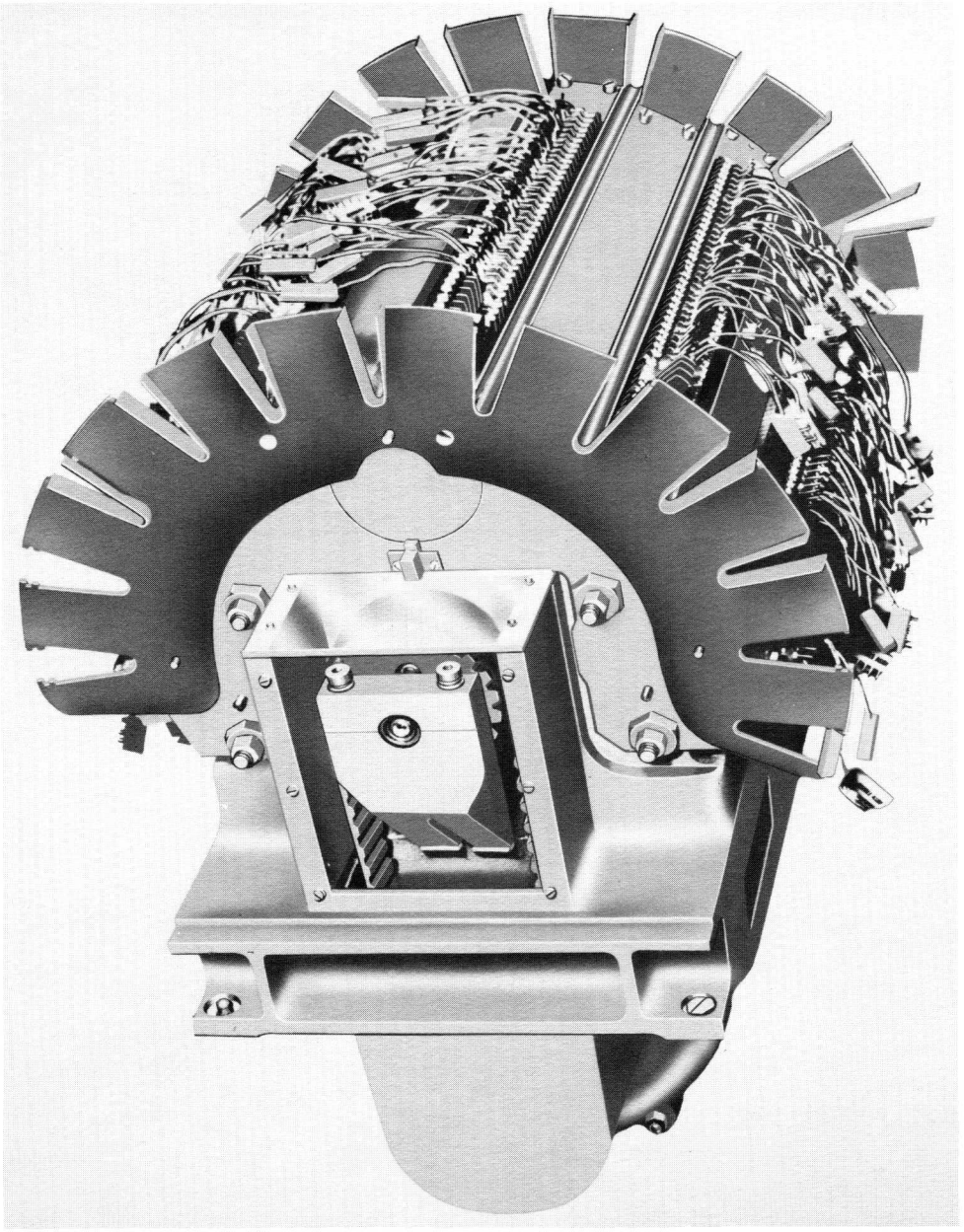


Figure 2–105. Drum Assembly Showing Drum Motor and Pulley Drive

motor-control circuit. Each overload relay also has a thermal protective device which operates when the coil has been overheated by persistent, small overload currents of short-circuit current magnitude. The circuit breaker protective device operates in a similar manner.

Circuit breaker 7 operates from phases 2 and 3 of the power system (fig. 2–106). This circuit breaker is identical with the others except that it has only two poles. It is used to protect the coil of time delay relay TR7, which is energized through the contacts of CB7. Time delay relay TR7 is an undervoltage relay whose contacts (shown in fig. 2–107) open, stopping motor operation, when the voltage applied to the motors remains below a selected value for a set period of time. This period is adjustable between 1 and 10 seconds. For example, if the delay is set for 8 seconds, the undervoltage condition must persist for 8 seconds before the relay contacts open.

9.4.2 Drum-Motor-Control Circuit, Circuit Analysis

The components of the drum-motor-control circuit (shown in fig. 2–106) control the operation of the six magnetic contactors, M1 through M6, described in

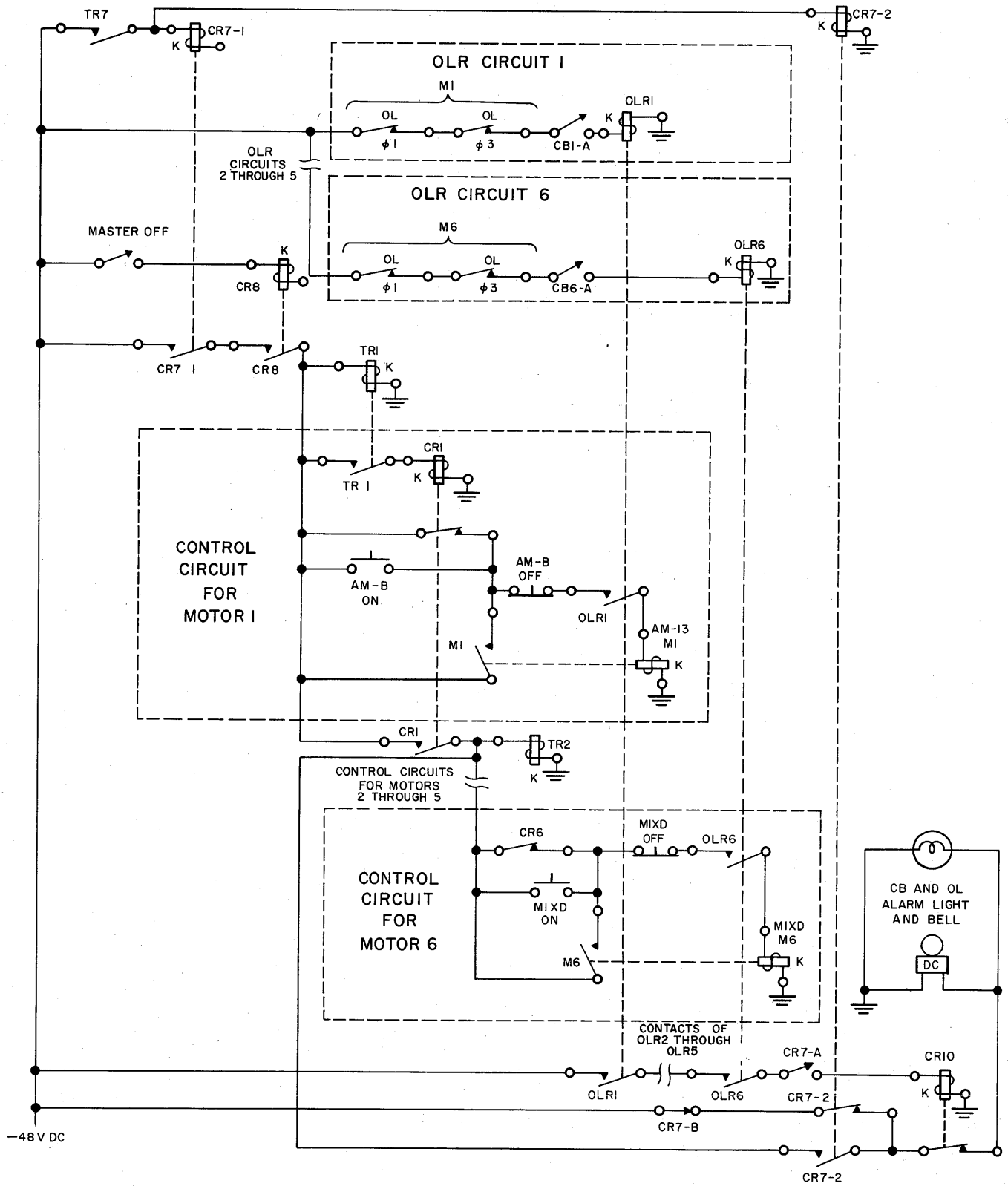


Figure 2–106. Drum-Motor Circuit, Simplified Schematic Diagram

9.4.1. When CB7 in the drum motor circuits (shown in fig. 2–107) is placed in the ON or RESET position, TR7 is energized. The contacts of this relay in the drum-motor control circuit close, applying a potential of −48 volts to the windings of control relays CR7-1 and CR7-2.

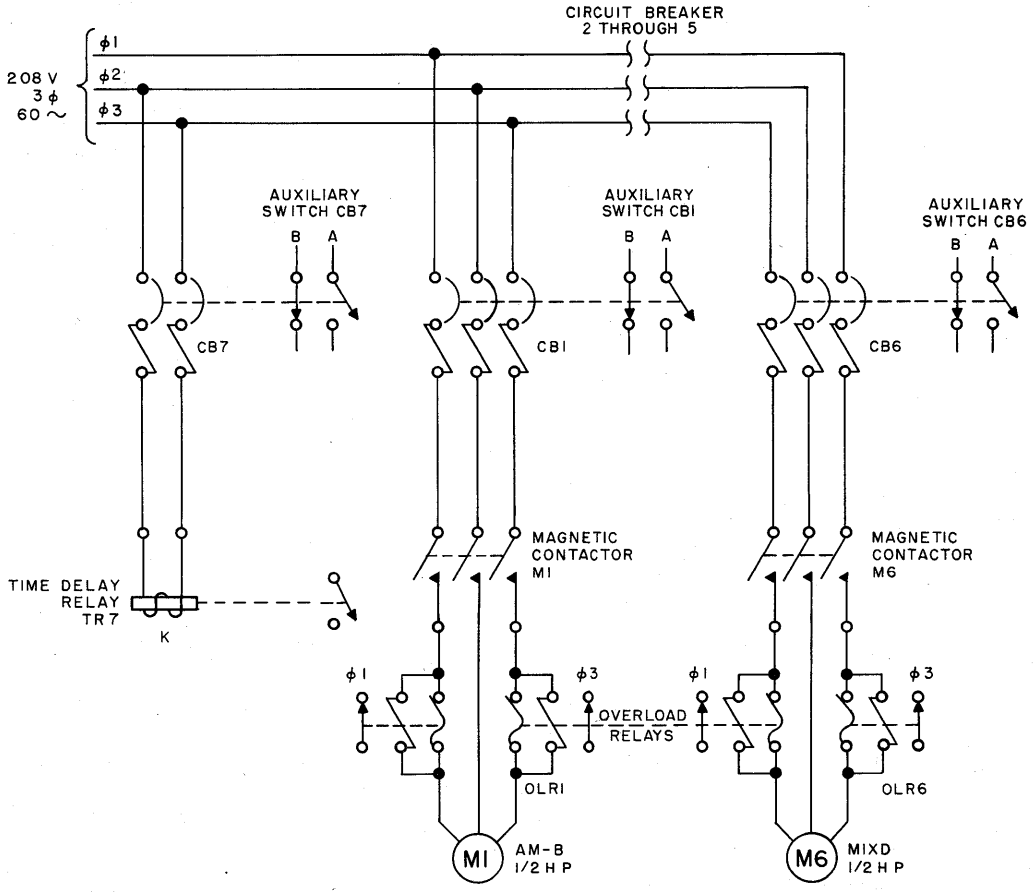


Figure 2–107. Drum-Motor-Control Circuit, Simplified Schematic Diagram

When CB1 through CB6 are placed in the ON or RESET position, the A contacts of their auxiliary switches close, applying a —48-volt potential through the closed contacts of the overload relays to the coil of the associated OLR relay. During operation, the OLR relays are de-energized only when an overload condition opens the contacts of the overload relay.

The drum motors are now ready to be energized. The MASTER OFF switch is operated, and CR8 is energized. Since CR7-1 has also been energized (by operating CB7), —48 volts are applied to TR1 and to the control circuit for motor 1. In the control circuit, the —48 volts find a path to ground through the normally closed contacts of CR1, the AM-B OFF switch, overload relay 1 contacts (which are now closed), and the coil of magnetic contactor M1. Energizing the coil of magnetic contactor M1 closes one set of contacts that apply power to the windings of motor 1, starting the motor (fig. 2–107). Energizing the magnetic contactor also closes an additional set of M1 contacts in the control circuit of motor 1. The latter contacts act as holding contacts for the coil of magnetic contactor M1.

Time delay relay TR1, whose coil is energized at the same time as the coil of M1, requires 1 to 10 seconds for its contacts to close. The total time depends on the setting of an adjustment on the relay. When TR1 contacts close, CR1 is energized. The normally closed contact pair of CR1 in the control circuit for motor 1 opens, leaving the holding contacts of M1 as the only d-c path for the coil of M1. Another CR1 contact pair at the input to the control circuit for motor 2 is closed. The latter contacts control application of —48 volts to the control circuit for motor 2 in the same way that CR7 and CR8 apply —48 volts to the control circuit for motor 1. With the closing of the CR1 contacts, M2 is operated, starting motor 2. It should be remembered that there is an adjustable delay of from 1 to 10 seconds between the starting of motors 1 and 2.

The control circuits for the remaining motors are identical. The motors are sequentially started with a predetermined time delay between the startings of successive motors.

If it should become necessary to stop the operation of any drum motor for maintenance, the operation of the other motors need not be disturbed. The OFF switch in the control circuit for the motor to be stopped is operated. This removes —48 volts from the coil of the magnetic contactor. When the magnetic-

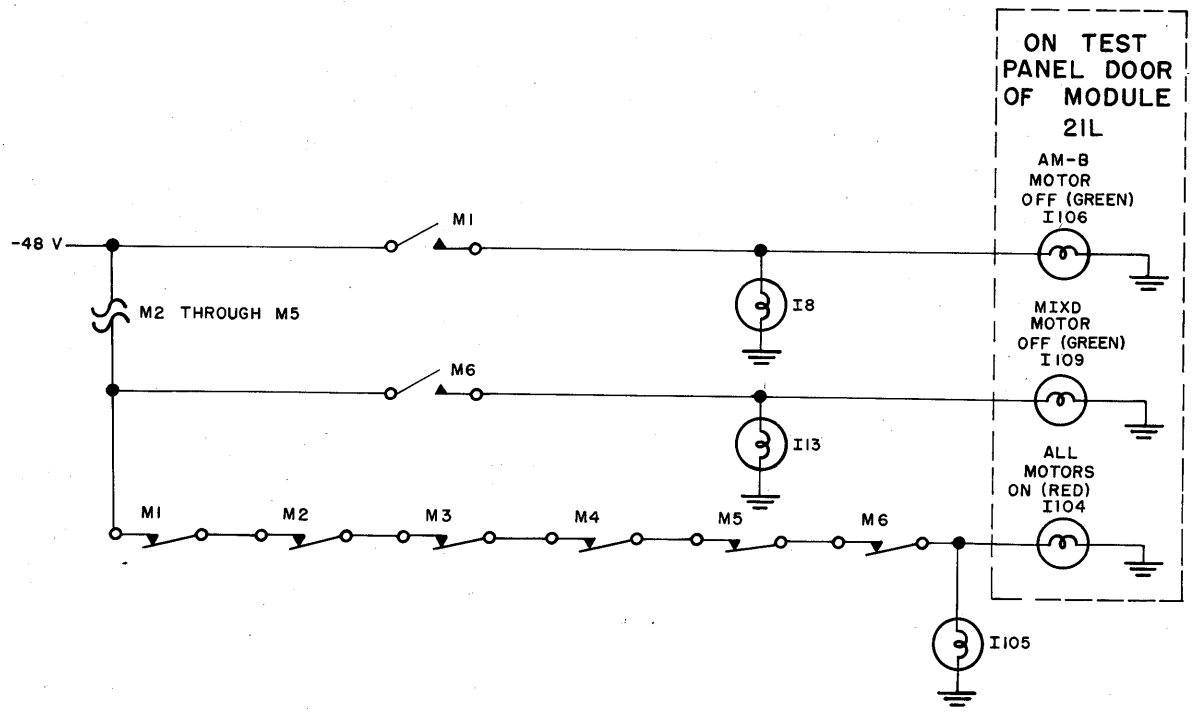


Figure 2–108. Drum-Motor-Control Circuit, Indicator Lamps Simplified Schematic Diagram

contactor contacts open, the motor stops and the holding contacts of the magnetic contactor are opened. The motor can be restarted by closing the ON switch. Closing the ON switch allows a restart without repeating the complete procedure for energizing all motors.

An alarm circuit included in the drum-motor-control circuit indicates the tripping of a circuit breaker, the opening of an overload relay, or an all-motors-off condition. Before CB7 is closed, —48 volts are applied through the normally closed auxiliary switch contacts (CB7B), through the normally closed CR7-2 contacts of CR7, and CR10 contacts to the CB and OL alarm light and bell. When CB 7 is closed, the CB7B contacts open, removing —48 volts from the bell and light. As each motor is energized in turn, the operation of its circuit breaker energizes the associated OLR relays, causing the OLR relay contacts to close. When all OLR relay contacts are closed, CR10 is energized. When CR10 is energized, its contacts open, removing —48 volts from the bell and light.

At the time that the contacts of TR7 are closed, CR7-2 is energized. The open and closed contact pairs of CR7-2 reverse their states. At the end of the delay between the starting of the first and the second drum motors, the open contacts of CR1 close. If CR10 is de-energized, a path for —48 volts is opened through the contacts of CR1, CR7-2, and CR10 to the bell and light. Relay CR10 is de-energized if CB 7 is tripped or if one of the overload relays opens.

9.4.3 Drum-Motor-Control Circuit Indicator Lamps, Circuit Analysis

Indicator lamps that indicate the operating condition of the drum motors are located on the test door of module 21L (shown in fig. 2–81) and in the drum-motor-control circuit. Figure 2–108 is a simplified schematic diagram of these lamp circuits. If any magnetic contactor opens during operation, its normally open and closed contact pairs reverse their states, and a d-c path is completed between the —48-volt power supply and the MOTOR OFF lamps associated with the motor which has stopped. When all motors are running, a pair of MOTOR ON lamps is lighted to indciate this fact.

PART 3

DETAILED THEORY OF OPERATION OF AUXILIARY DRUMS

CHAPTER 1

INTRODUCTION

The auxiliary drums are contained entirely in unit 20. There are six auxiliary drums, separately designated by the letters C through H (AM-C, AM-D, AM-E, AM-F, AM-G, AM-H).

The function of the auxiliary drums is to supply additional memory space for Central Computer System programs. These programs are too extensive to be stored in the Central Computer System core memory in their entirety. Therefore, large quantities of program data are stored in the auxiliary memory fields of the auxiliary drums until requested by the Central Computer System. When requested, the data is transferred back to the Central Computer System.

The auxiliary drums exchange information with the Central Computer System only. These information exchanges are accomplished via the computer-auxiliary-drum (ACD) circuits.

The Central Computer System must be able rapidly to select specific data stored on the auxiliary drums. This rapid selection is accomplished by the address-controlled method of reading and writing. This method enables the Central Computer System to read or write in a specific register.

Auxiliary drum and field selection circuitry is activated by programmed instructions from the Central Computer System. The instructions designate the auxiliary drum and field on which reading or writing will take place. The drum selection operation actuates the timing circuits associated with the selected drum. The timing circuits time the operations of the auxiliary drums. Since the drums do not rotate in synchronism, each selected drum must generate the timing pulses that time the data transfers between its own circuits and the Central Computer System.

Chapter 2 of this part discusses the function and formation of the AXD timing pulses, as well as their distribution.

Chapter 3 explains the function of field selection and describes the field selection and switching circuits required.

Chapter 4 discusses the function and source of the signals that control ACD writing and reading. Descriptions of the flow path of ACD data, and of the circuitry required for ACD writing and reading, are included.

Chapter 5 describes the manual tests that can be performed on the auxiliary drums circuits, together with the test circuits used for the performance of these tests. Included in this chapter are descriptions of the manually initiated timing rewrite and erase controls and of the drum-motor-control circuits.

A number of circuits used in the auxiliary drums are duplicates of those found in the main drums. In such cases, detailed discussions are not presented, but reference is made to the appropriate chapters or sections of Part 2.

CHAPTER 2

AUXILIARY DRUM TIMING GENERATION AND DISTRIBUTION

The auxiliary drum timing system times the operations of the auxiliary drums. Timing pulses are produced which affect reading or writing on the drum field. The timing pulses are also used to step the counting circuits of the auxiliary drums.

The drums do not rotate in synchronism, since each drum is driven by a separate motor. It is necessary, therefore, for each drum to generate the timing pulses that time and control its own operations and the operations of its associated circuits.

2.1 AUXILIARY DRUM TIMING PULSE GENERATION

The auxiliary drum timing system, unlike the timing system of the main drums, generates two timing pulses instead of four. These timing pulses are obtained from a timing channel recorded on each drum. Timing channels on all drums contain a flux pattern, which, when read, produces a series of sine waves. During the operation of each drum, each sine wave cycle is read from the timing channel and is converted into two standard pulses, 5.0 usec apart. These two pulses, known as auxiliary drum timing pulses (ACD's) 1 and 3, together represent a 10-usec operational cycle of the drum circuits. The ACD 1 and ACD 3 pulses are produced directly from the timing channel; their repetition rate is a direct function of drum speed.

Drum timing pulses are formed from the closed sine wave series recorded on each drum. In a closed series, there is no method of distinguishing any two sine wave cycles. One cycle must be arbitrarily selected to represent the beginning or ending of a drum revolution. This selection is performed by recording an additional channel, known as an index channel, on each drum. Each index channel contains a single 1 bit which establishes a reference register in drum rotations. The remainder of the index channel contains 0 bits.

2.1.1 Writing of Timing and Index Channels

The timing and index channels are written before Drum System operations are begun, or following maintenance procedures in which timing and index channels are erased. Timing and index channel writing on the auxiliary drums is identical with that on the main drums described in Part 2, Chapter 2. In this case, however, all the timing channels contain 2,048 bits. The circuits involved are shown on logic drawing 1–2.3.3.

2.1.2 Reading of Timing and Index Channels

The timing and index channels of each drum are read continuously. (See fig. 3–1.) The flux pattern on the timing channel of a drum causes a series of sine waves to be induced in the timing channel read head. (These sine waves are similar to the sine waves developed by the optical frequency generator.) The induced sine waves are applied to a timing pulse generator. The generator converts the sine waves into two fundamental timing pulses, ACD's 1 and 3, used to time the circuits of the drum. The 5.0-usec interval between each pulse results in a pulse cycle of 10 usec. This corresponds to the time required for one register on the drum surface to pass a read or write head during normal rotation of the drum. Within the auxiliary drum circuits, ACD 1 pulses are used for reading, and ACD 3 pulses for writing.

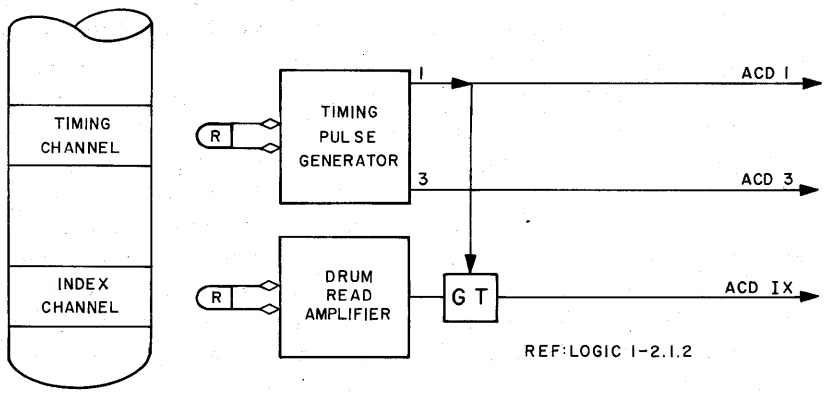


Figure 3–1. Auxiliary Drums, Timing and Index Channel Reading, Simplified Logic Diagram

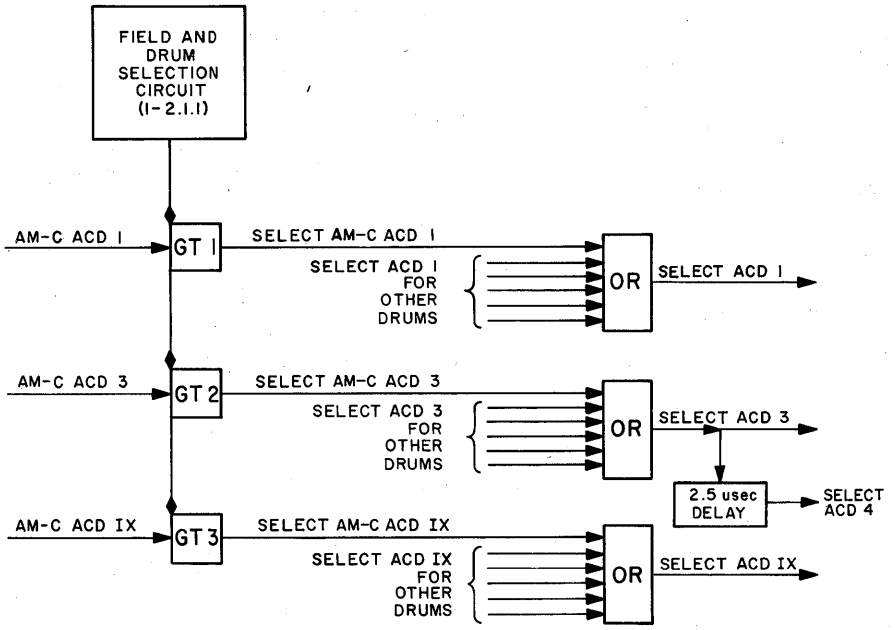


Figure 3–2. Auxiliary Drum Timing Pulse Distributor, Simplified Logic Diagram

The index-channel read head sends the sine wave caused by the index bit to the index-channel drum read amplifier. The drum read amplifier conditions a gate to pass the ACD 1 pulse occurring at that time. This gated ACD 1 pulse, the ACD-index pulse, is a reference point that indicates the first register of a drum revolution during information transfers between the auxiliary drums and the Central Computer System.

2.1.3 Formation of Special Purpose Timing Pulses and Levels

The application of drum timing pulses to key points in the transfer control circuits of the auxiliary drums is dependent on the drum involved in the transfer. This dependence is effected by feeding the required timing pulse into gates. (See fig. 3–2.) In order to conduct, the gates must be conditioned by a select-drum level. The select-drum level is present whenever a field on a drum is selected by the Central Computer for an information exchange. The array of gates, and the subsequent OR circuits into which the timing pulses are fed, is called the timing pulse distributor. The output of each gate is called a selected-drum timing pulse (it is present only when that drum is selected). The timing pulse distributor produces a selected ACD-index-pulse, a selected ACD 1 pulse, and a selected ACD 3 pulse for each drum. The gated timing pulses (ACD 1, 3, or IX) of the selected drum go to the data transfer control circuits of the auxiliary drum via three OR circuits. The selected ACD 3 pulse is delayed 2.5 usec to form the selected ADC 4 pulse. (Logic drawing 1–2.1.2 shows complete details.)

2.2 TIMING PULSE DISTRIBUTION

Within the auxiliary drum circuits, the drum ACD 1 pulses have their primary application in the read circuits, where they are passed through, conditioned to act as read-sample pulses. The ACD 3 pulses have their primary application in the write circuits, where they initiate the write-on-drums operation. The ACD 3 pulses are also used to step angular position counters associated with each drum. The ACD 4 pulse is used to set the master sync flip-flop in the read-write control circuit.

The ACD-index pulses have their primary application in the various counter and synchronizing circuits, where they perform the resetting function required at the completion of one or more drum revolutions.

2.3 AUXILIARY DRUM SYSTEM AND CENTRAL COMPUTER SYSTEM, TIMING RELATIONSHIP

The Central Computer System is a faster operating system than the Drum System. It employs a 6-usec timing cycle of 12 timing pulses, as distinguished from the 10-usec timing cycle of the Drum System. Data transfers occur at the maximum speed permitted by the drum timing. Any individual word is transferred within the 10-usec period of the drum timing cycle. The Central Computer interrupts its other operations to receive or transmit a word whenever the auxiliary drums are ready to transmit or receive the word.

CHAPTER 3

AUXILIARY DRUM FIELD AND DRUM SELECTION

Exchanges of information between the Central Computer System and the auxiliary memory fields (ACD exchanges) are initiated by programmed instructions from the Central Computer. One part of these instructions designates the drum field with which the Central Computer desires to exchange information. The field designation, in the form of parallel pulses, activates the Drum System field selection circuitry. The Drum System selection circuitry performs two operations required in an information transfer between the Drum System and the Central Computer System. These operations involve selecting the designated drum field and the drum in which the field is located.

The purpose of the first operation is to activate that drum field with which the information exchange is to take place and no other field; this operation must also condition the control circuits directly associated with the designated field. The drum selection operation is required to activate the timing circuits of the drum on which the selected field is located. The selected field and its associated circuits could not be correctly timed using the timing channel of any other drum, because of the synchronous operation of the drums.

The function and detailed operation of the ACD field selection circuits are shown on logic drawing 1–2.1.1 and described in the paragraphs that follow.

3.1 AUXILIARY MEMORY FIELD DESIGNATION

Field selection instructions from the Central Computer are transferred to the auxiliary Drum System by index-interval pulses which represent the six bits, L10 through L15, of a programmed instruction word. These bits, called index-interval bits, contain the field designation for the selected field. The octal code for each field is shown in figure 3–3.

Three of the Central Computer System instruction word bits represent the tens-column digit; the other three, the units-column digit. For example, if the 42nd auxiliary memory field, which is located on AM-G, is selected by the Central Computer System, the instruction word bits are 000111, in that order, representing code number 07_8. If the 28th auxiliary memory field is chosen, the instruction word bits are 110100, in the same order, representing code number 64_8. In the same manner, any one of the 36 fields listed in the octal field code chart of figure 3–3 can be selected.

3.2 AUXILIARY MEMORY FIELD SELECTION

The index-interval bits designate a field selected by the Central Computer System. The field selection circuitry performs two functions required for an information exchange between the selected drum field and the Central Computer: the activation of the designated field, and that field only; and the selection of the timing and control circuits of the drum on which the field is located.

The above functions are accomplished by means of decoding circuits and diode switching circuits. The decoding circuits transform the positive levels representing the two groups of three binary instruction bits into positive levels representing an equivalent 2-place octal number. These levels are applied to the read-write heads of the field designated by the octal code number, and through the read-write heads to the diode switching circuits.

The diode switching circuits are the means by which information transfer is limited to the designated field. In order for information to be read from, or written on, a designated drum field, the diode switch associated with that field must be conditioned by the field-selection level.

3.2.1 Field Selection Decoding Circuits

The decoding circuits used for auxiliary memory CD field and drum selection are similar to those used for the main drums, which are described in detail in 3.2.1 of Part 2. The tens-decoder, however, consists of only six AND circuits. Each AND circuit represents a numeral of the following group: 0, 1, 4, 5, 6, and 7. The numerals 2 and 3 are not used in the tens-decoder, since no auxiliary memory fields are represented by an octal number beginning with 2 or 3 (fig. 3–3).

3.2.2 Drum Field Driver Array

The auxiliary drum field drivers operate in the same manner as the main drum field drivers, described in 3.2.2 of Part 2.

3.3 AUXILIARY MEMORY FIELDS DIODE SWITCHING

Diode switching in the auxiliary memory fields is identical with that of the main drum fields. Refer to 3.3 of Part 2.

TENS \ UNITS	0	1	2	3	4	5	6	7
0			AUXILIARY MEMORY-G 37	AUXILIARY MEMORY-G 38	AUXILIARY MEMORY-G 39	AUXILIARY MEMORY-G 40	AUXILIARY MEMORY-G 41	AUXILIARY MEMORY-G 42
1	AUXILIARY MEMORY-H 43	AUXILIARY MEMORY-H 44	AUXILIARY MEMORY-H 45	AUXILIARY MEMORY-H 46	AUXILIARY MEMORY-H 47	AUXILIARY MEMORY-H 48		
2								
3								
4		AUXILIARY MEMORY-C 13	AUXILIARY MEMORY-C 14	AUXILIARY MEMORY-C 15	AUXILIARY MEMORY-C 16	AUXILIARY MEMORY-C 17	AUXILIARY MEMORY-C 18	
5		AUXILIARY MEMORY-D 19	AUXILIARY MEMORY-D 20	AUXILIARY MEMORY-D 21	AUXILIARY MEMORY-D 22	AUXILIARY MEMORY-D 23	AUXILIARY MEMORY-D 24	
6		AUXILIARY MEMORY-E 25	AUXILIARY MEMORY-E 26	AUXILIARY MEMORY-E 27	AUXILIARY MEMORY-E 28	AUXILIARY MEMORY-E 29	AUXILIARY MEMORY-E 30	
7		AUXILIARY MEMORY-F 31	AUXILIARY MEMORY-F 32	AUXILIARY MEMORY-F 33	AUXILIARY MEMORY-F 34	AUXILIARY MEMORY-F 35	AUXILIARY MEMORY-F 36	

REF: LOGIC 1-2.1.1

Figure 3–3. Octal Code for ACD Field Selection

3.4 AUXILIARY MEMORY DRUM SELECTION

Within the Drum System itself there is no fixed time relationship between individual drums, since each drum is rotated by a separate motor. Each drum generates the timing pulses which time and control its own operations and the operations of the system (or systems) with which it is associated. It is necessary, therefore, for the Drum System to select and condition the timing circuitry of the particular drum which contains the field designated by the Central Computer System.

When a particular field is designated by the index-interval pulses, the tens-selection-register-and-decoder produces a select-drum level which conditions the gates of the ACD-timing-pulse distributor. (Refer to Ch 2 for a discussion of drum timing and associated circuitry.)

The output of the tens-selection decoder may be used as the select-drum level because all fields on any one drum, and only the fields on that drum, are designated by code numbers having the same tens digit (see fig. 3–3).

3.5 SELECTION OF OCTAL CODE NUMBERS FOR NONEXISTING FIELDS

The field selection decoders are capable of producing a tens and a units output that does not designate an existing field. For example, 01_8 and 67_8 are octal code numbers for which no fields exist (see fig. 3–3).

A tens and a unit number produced in this category will be deleted in a separate decoder and OR circuit, the output of which prevents reading or writing (see Ch 4). The operation of this decoder is identical with that of the field selection decoder discussed in 3.2.1.

CHAPTER 4

COMPUTER-AUXILIARY DRUM DATA TRANSFER

The six auxiliary drums of unit 20 are used to store Central Computer program data. This data is transferred to the Central Computer as necessary and is used to control Central Computer operations. All transfers of data between the auxiliary drums and the Central Computer are controlled by the address method. The data transfer process and the circuits that control the data transfer are essentially the same as those used in the main drums. Detailed discussions of the operation of these circuits may be found in Part 2, Chapter 4, of this manual.

The data stored on the auxiliary drums must be used repeatedly by the Central Computer. It is very important, therefore, that this data not be destroyed or altered in any way. The auxiliary drum control circuits include a write interlock to prevent accidental writing on the auxiliary drums. Such accidental writing would alter parts of the program and seriously affect computer operation. The write interlock may be removed only by manual control for program loading or modifying.

The auxiliary drum write interlock consists of a relay network (write interlock relays) which serves to disconnect the drum writers from the write heads and to disable the address-control circuit if a writing operation is programmed.

4.1 ACD WRITE INTERLOCK CIRCUIT

Figure 3–4 shows the compare-addressable flip-flop in the address-control circuitry. This flip-flop is set by a compare-addressable pulse, which is passed by a gate. The setting of the flip-flop, therefore, will depend upon the gates being conditioned to pass compare-addressable pulses.

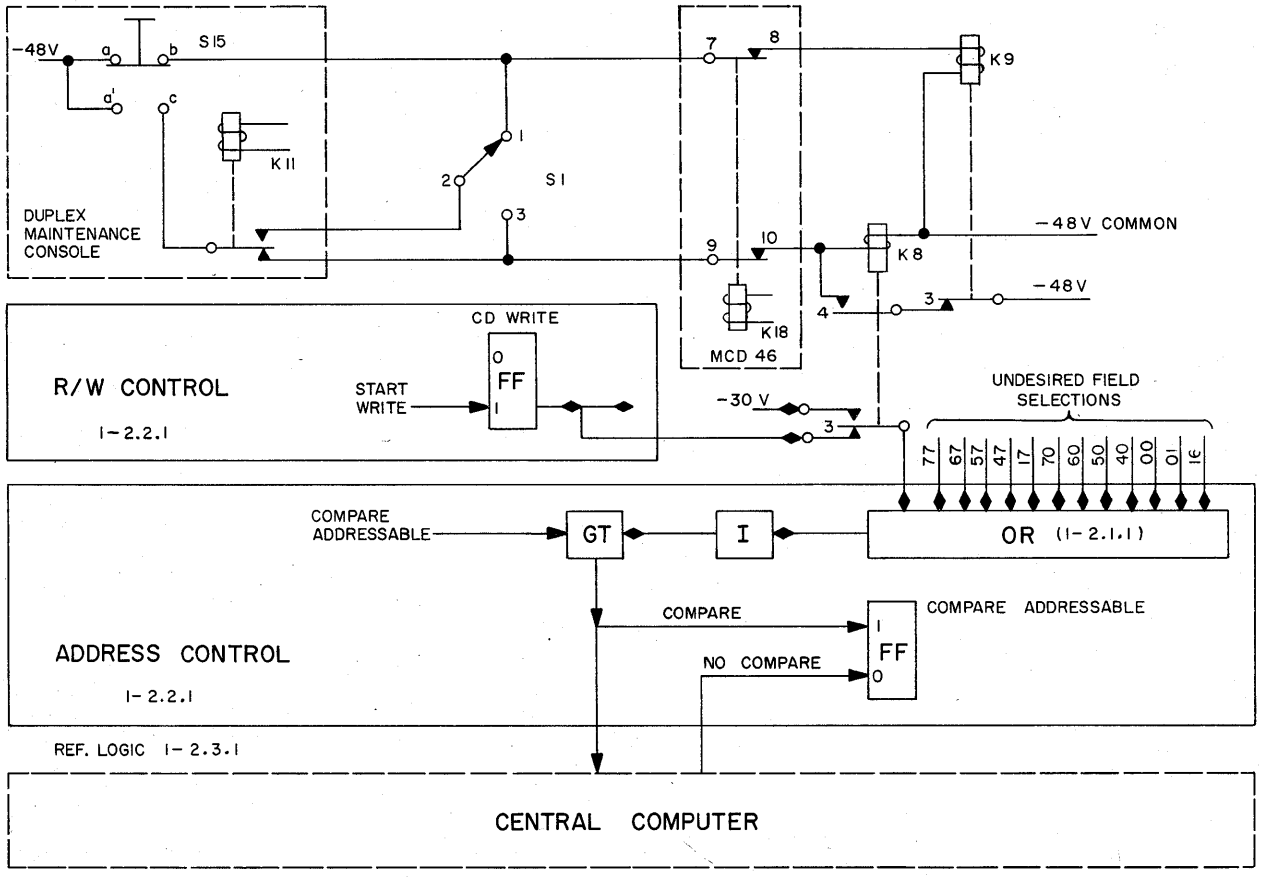


Figure 3–4. Auxiliary Drum Write Interlock Circuit

With the write interlock active, the +10-volt level from the CD write flip-flop in the read-write control goes through the normally closed contacts (3) of relay K8 to the OR circuit (logic 1–2.1.1). The +10-volt level at the output of the OR circuit is applied to the inverter which produces a negative output, deconditioning the gate. Thus, when the write interlock is active, the gate does not pass compare-addressable pulses to set the compare-addressable flip-flop.

When the write interlock is removed, K8 is energized. In this condition, contacts (3) of this relay apply −30 volts to the OR circuit, whose negative output is applied, in turn, to the inverter. The inverter output thus becomes positive and serves to condition the gate to pass compare-addressable pulses.

Another set of contacts (not shown in fig. 3–4) on K8 applies power to the write interlock relays. When the interlock is active, these contacts are open, and the write interlock relays are energized and disconnect the drum writers from the write heads of the selected field, thereby making writing impossible.

The other inputs to the OR circuit (shown in fig. 3–4) are select levels representing nonexisting fields. The selection of nonexisting fields blocks the compare-addressable pulse and prevents either reading or writing. (See 3.5 for a discussion of nonexisting fields selected.)

4.2 WRITE INTERLOCK OPERATION, OVERALL DESCRIPTION

To preserve the data written on the auxiliary drums as an accurate source of reference, elaborate precautions have been taken so that writing operations are performed only when strictly required. New writing on the auxiliary drums then becomes an accurate source of reference which supersedes obsolete information previously stored.

In the operate mode, preparation for writing involves two distinct steps: first turning on key-operated write interlock switch S15 on the lower section of module E of the duplex maintenance console; second, momentarily turning off the DC POWER switch at the power control door in unit 20. There is also a key-operated write interlock switch, S1, in the test door of unit 20. In the operate mode, however, this switch is disabled.

Upon completion of the writing operation, the key-operated write interlock switch, S15, at the duplex maintenance console is turned off, and the DC POWER switch is again turned off momentarily. From this time, no further writing can be performed until the two steps described have been taken.

In the test mode, the preparation for writing involves four distinct steps: first, turning on the key-operated write interlock switch, S15, at the duplex maintenance console; second, placing the OPERATE-MANUAL TEST switch (S14), also at the maintenance console, in the MANUAL TEST position; third, turning on the key-operated write interlock switch, S1, at the test door; and fourth, momentarily turning off the DC POWER switch at the power control door in unit 20. Upon completion of the writing operation, write interlock switches S15 and S1 are turned off, and the DC POWER switch is momentarily turned off. No further writing can be performed unless the preparatory steps described have been taken in accordance with the operate or the test mode in progress.

4.3 WRITE INTERLOCK, OPERATION ANALYSIS

Refer to figure 3–4. Key-operated switches S1 and S15 appear on the figure in the off position (key removed), and relays are shown in the de-energized state. To perform writing in the auxiliary drums, the main objective is the energizing of K8.

In the operate mode, when write interlock switch S15 is turned on, −48-volt control power is applied to K8 through the contacts of de-energized relays K11 and K18. Since K11 is de-energized during the operate mode, and K18 is energized when power is applied, it follows that d-c power must be removed (at the DC POWER switch in the power control door of unit 20) so that K18 is de-energized and, through its normally closed contacts, completes the −48-volt line to K8.

When d-c power is reapplied and K8 is energized, K8 is held energized through the contacts of K9. Relay K9 is energized only when the interlock switch, S15, is turned off and d-c power is removed. In this condition, contacts (3) of this relay open and −48-volt power is disconnected from the holding contacts (4) of K8. At all other times, K9 is de-energized. To energize K8, therefore, S15 is operated and d-c power removed. When d-c power is restored (upon momentary switching), K8 is held energized through its own contacts and those of de-energized K9. This condition will prevail for the duration of the writing operation, at the end of which S15 is turned off and the DC POWER switch is momentarily operated off and on.

In the test mode, to prepare for writing on the auxiliary drums, both write interlock switches, S15 at the maintenance console and S1 at the test door, must be operated, and the DC POWER switch at the power control door must be momentarily operated off and on. During the test mode, K11 at the maintenance console is energized as a result of setting the OPERATE-MANUAL TEST switch (S14) in the MANUAL TEST position. Through the transfer contacts of K11, the −48-volt control power from S15 appears at the center arm of S1. When interlock switch S1 is off, the −48-volts energize K9 through the contacts of K18 (when d-c power is removed). However, if write interlock switch S1 is operated, K8 will be energized when d-c power is removed

and will remain energized through its own contacts and those of K9 when d-c power is again applied.

At the end of each write operation, interlock switches S15 and S1 should be turned off, and the d-c power should be momentarily switched off to restore the normal write interlock condition.

CHAPTER 5
AUXILIARY DRUM TESTING

This chapter describes the theory of operation of the manual auxiliary drum test circuits, the manually initiated timing rewrite and erase controls, and the drum-motor-control circuitry.

Special circuits in the auxiliary Drum System enable maintenance personnel to perform manual checks and tests on Drum System circuits. The manual test provide a way of localizing a great majority of malfunctions to a specific circuit, channel, pluggable unit, or circuit component. The tests are conducted from the test door on unit 20D (see fig. 3–5) and involve Drum System circuitry only. Every circuit in each of the drum operating elements and some circuits of the computer test element can be checked.

The drum timing-rewrite-and-erase circuits are manually activated circuits which erase all magnetic flux on any auxiliary drum and automatically rewrite the timing and index channels of that drum.

The drum-motor-control circuits control the manual starting and stopping of any or all of the six auxiliary drums.

5.1 MANUAL TEST CIRCUITS, CIRCUIT ANALYSIS

This paragraph describes test circuits in the auxiliary Drum System which enable maintenance personnel to check and test all normally operated auxiliary drum circuits. The manual tests provide a way of localizing a great majority of malfunctions to a specific circuit, channel, pluggable unit, or circuit component. The tests are performed manually and do not use circuits of any of the other systems of the equipment. For this reason, the tests offer excellent means of checking the Drum System during installation. Checks on every circuit in each of the operating elements can be performed.

The manual control and test circuitry used by the auxiliary drums are shown in detail on logic drawings 1–2.3.1, 1–2.3.2, and 1–2.3.3.

5.1.1 Begin-Manual-Test Circuit

All manual tests on the Drum System must start with the operation of controls in the ACD begin-manual-test circuit (shown in fig. 3–6). A -48-volt level is transmitted from the maintenance console to the ACD begin-manual-test circuit when the TEST-OPERATE switch on the console is in the TEST position. When TEST MODE SELECTION switch S2 on the test panel of module 20D (fig. 3–5) is set to the DRUMS IN MANUAL TEST position, the –48-volt level is applied to the coil of relay K6, energizing it. When K6 is energized, its 1 and 2 contacts close and energize relay K4. When K4 is energized, its 7 and 8 contacts close and complete the +10-volt interlock circuit through the closed 3 and 4 contacts of K6 to several manual-test circuits, where it is used as a drum-in-manual-test level.

5.1.2 Manual-Test-Field-Selection Circuit

When a manual test begins with the operation of switch S2 in the begin-manual-test circuit (refer to 5.1.1), it is necessary to select the field to be tested. This is done by the operation of controls in the ACD manual-test-field-selection circuit. (See fig. 3–7.)

Initially, DESELECT pushbutton S16 is depressed, applying a test-ground level to the input of the pulse generator through the normally open contacts of S16 switch unit 1. Switch S16 is on the module 20D test panel. When the pulse generator input is grounded, the generator produces one 0.1-usec pulse. This pulse is conducted through closed contacts C and NO of S16 switch unit 2 to the CD selection register as a test-deselect pulse. This pulse substitutes for the deselect pulse normally produced by the Central Computer System by providing an alternate input to OR 1. The deselect pulse clears the CD selection register and is sent to the CD-read-write-control circuit to prepare the latter to receive a drum operation instruction.

With the deselect operation completed, it is necessary to manually substitute a drum field selection for the drum field selection that normally comes from the Central Computer in the form of index-interval pulses. Pushbuttons S10 through S15, labelled 1, 2, 4, 10, 20, and 40, provide substitutes for the six index-interval pulses from the Central Computer System. Depressing the pushbuttons produces 1 bits for the associated index intervals. The resulting configuration of 1 and 0 bits in index-interval pulses 1, 2, and 4 determines the value of the units column in the drum field selection code. The resulting configuration of 1 and 0 bits in index intervals 10, 20, and 40 determines the value of the tens column in the drum field selection code.

Table 3–1 shows the code of the field or test selection and the pushbuttons that must be depressed to produce the code. Each pushbutton that is depressed in accordance with this table applies ground to the pulse generator. The pulse generator output (0.1-usec pulse) is conducted through the closed switch unit 2 pushbutton

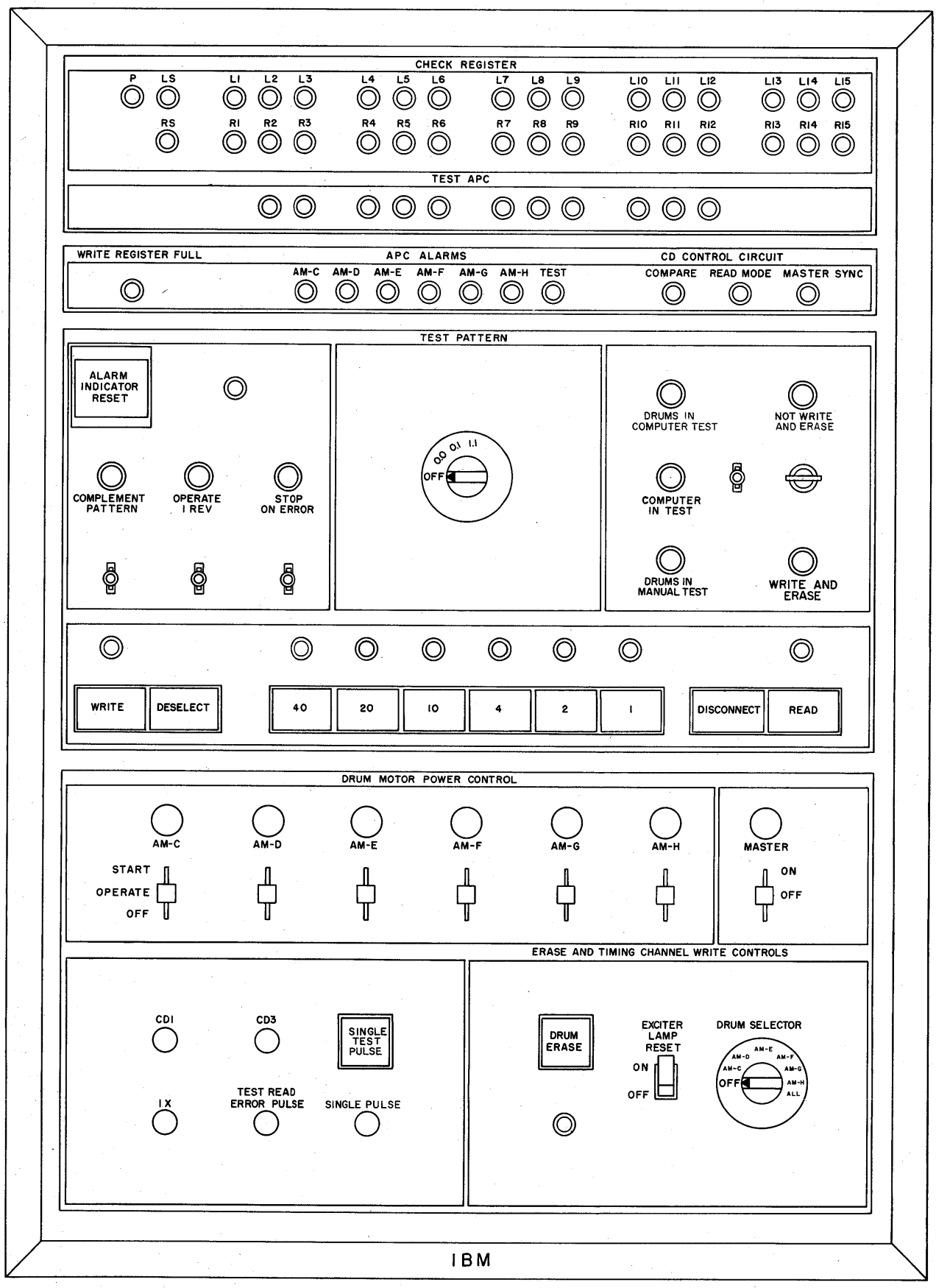


Figure 3–5. Unit 20, Module D, Test Door

TABLE 3–1. MANUAL TEST PANEL SELECTION REGISTER PUSHBUTTON CODE (AUXILIARY DRUMS)

FIELD OR TEST	CODE	PUSHBUTTONS
AM-C 13	41	40, 1
AM-C 14	42	40, 2
AM-C 15	43	40, 2, 1
AM-C 16	44	40, 4
AM-C 17	45	40, 4, 1
AM-C 18	46	40, 4, 2
AM-D 19	51	40, 10, 1
AM-D 20	52	40, 10, 2
AM-D 21	53	40, 10, 2, 1
AM-D 22	54	40, 10, 4
AM-D 23	55	40, 10, 4, 1
AM-D 24	56	40, 10, 4, 2
AM-E 25	61	40, 20, 1
AM-E 26	62	40, 20, 2
AM-E 27	63	40, 20, 2, 1
AM-E 28	64	40, 20, 4
AM-E 29	65	40, 20, 4, 1
AM-E 30	66	40, 20, 4, 2
AM-F 31	71	40, 20, 10, 1
AM-F 32	72	40, 20, 10, 2
AM-F 33	73	40, 20, 10, 2, 1
AM-F 34	74	40, 20, 10, 4
AM-F 35	75	40, 20, 10, 4, 1
AM-F 36	76	40, 20, 10, 4, 2
AM-G 37	02	2
AM-G 38	03	2, 1
AM-G 39	04	4
AM-G 40	05	4, 1
AM-G 41	06	4, 2
AM-G 42	07	4, 2, 1
AM-H 43	10	10
AM-H 44	11	10, 1
AM-H 45	12	10, 2
AM-H 46	13	10, 2, 1
AM-H 47	14	10, 4
AM-H 48	15	10, 4, 1

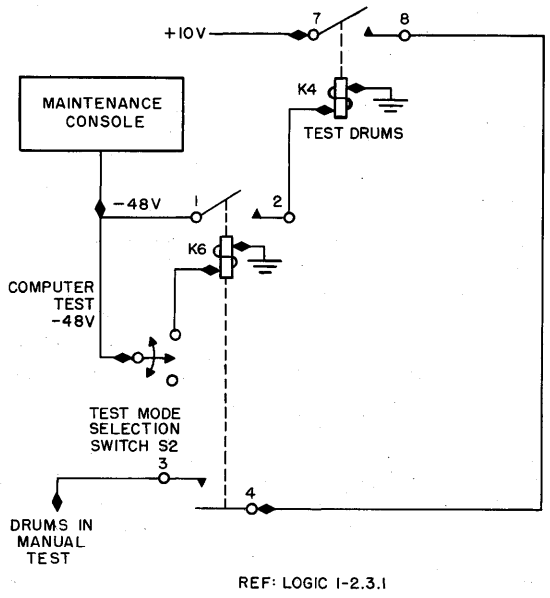


Figure 3–6. ACD Begin-Manual-Test Circuit, Simplified Logic Diagram

contacts to the OR circuit associated with the index-interval pulse represented by the individual pushbuttons. The OR circuits normally get index-interval pulse inputs from the Central Computer. The OR circuits that conduct set associated flip-flops in the CD selection register. On the basis of the setting of the CD selection register, the CD selection decoder determines the drum that has been selected and sends a drum-select level to the timing-pulse-distributor circuit. The CD selection decoder also determines the selection field and sends a select-drum-field level to the selected drum field driver. The selected drum field driver applies this level to the center taps of the drum heads associated with the selected field, thereby enabling them to read or write.

5.1.3 Select-Manual-Read-or-Write-Drum-Operation Circuit

If the manual test to be performed requires a reading or writing operation by the field (or test) selected, it is necessary to develop a manual substitute for the *Read* or *Write* instructions that normally come from the Central Computer. The necessary substitution is made by the operation of controls in the ACD select-manual-read-or-write-drum-operation circuit (shown in fig. 3–8).

When a manual test involving a reading operation is to be performed on a selected field, READ push-button S8 is depressed. This applies a test ground to the pulse generator, producing a 0.1-usec pulse. The pulse serves as a manual-start-read pulse to the manual-test-pattern-control circuits, discussed in 5.1.4 It also

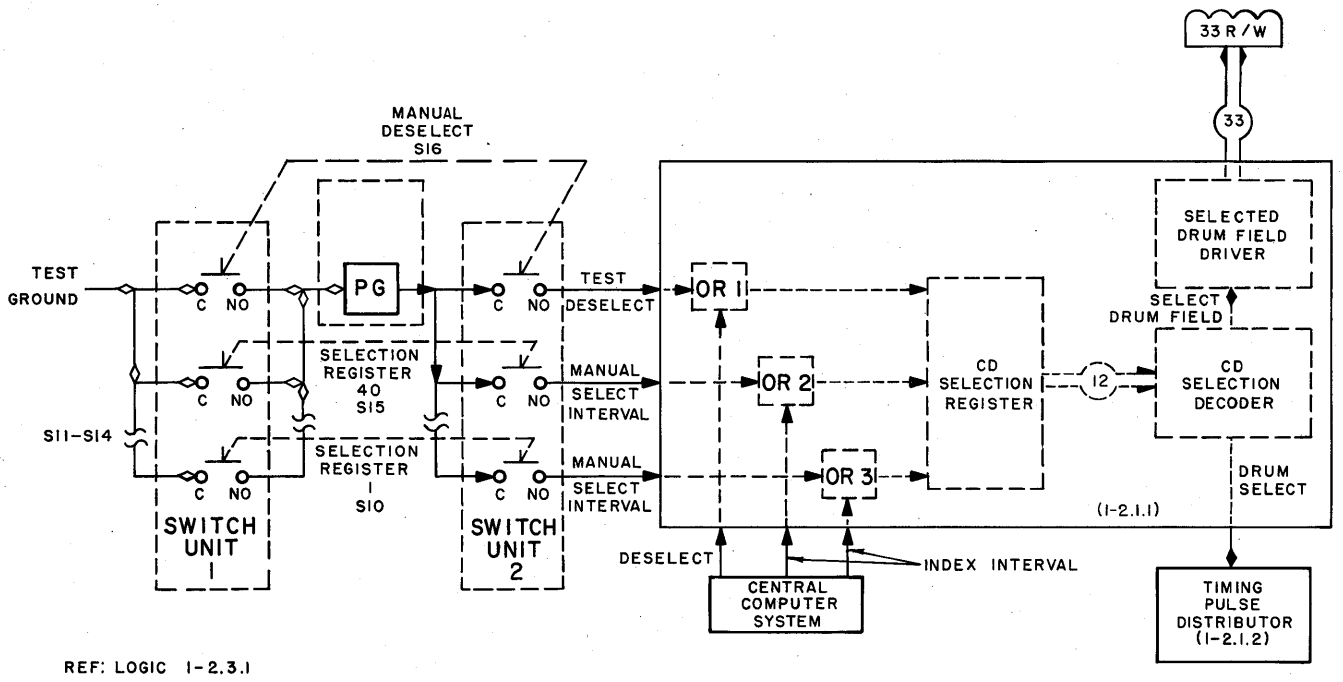


Figure 3–7. ACD Manual Test Field Selection, Simplified Logic Diagram

serves as a substitute for the normal Central Computer instruction to the CD-read-write-control circuit.

When a manual test involving a writing operation is to be performed, WRITE pushbutton S17 is depressed. The action of this pushbutton is similar to that of the READ pushbutton. Manual-start-write pulses go to the CD-read-write-control circuit in place of the normal Central Computer pulse inputs.

5.1.4 Manual-Test-Pattern-Control Circuit

During manual tests that require a known pattern to be written and read on the drum fields, the pattern to be used is selected by operating a control in the manual-test-pattern-control circuit. The complement of this pattern can also be developed by operating a control in the complement-test-pattern circuit.

With either a manual-start-read or manual-start--write operation chosen in the select-manual-test-read-or write-operation circuit, OR 1 in the ACD manual-test-pattern-selector-and-control circuits (fig. 3–9) conducts, setting FF 1, the pattern flip-flop. Although the beginning of every manual start causes the flip-flop to be set, a complement-test-pattern pulse can be manually produced which, at first application, clears the pattern flip-flop and, at second application, sets it again.

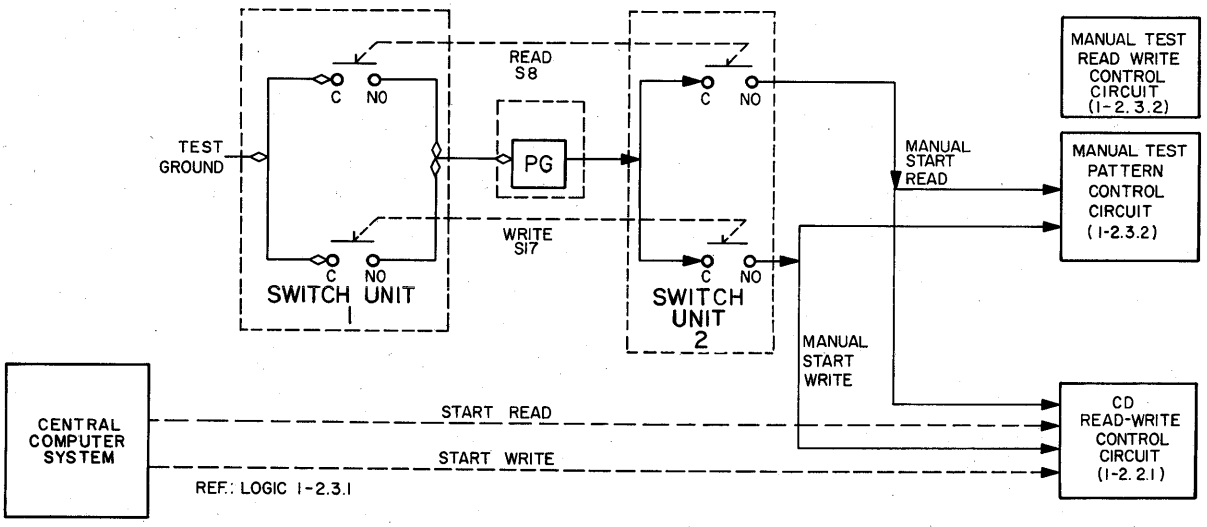


Figure 3–8. ACD Select Manual Read-or-Write Drum Operation, Simplified Logic Diagram

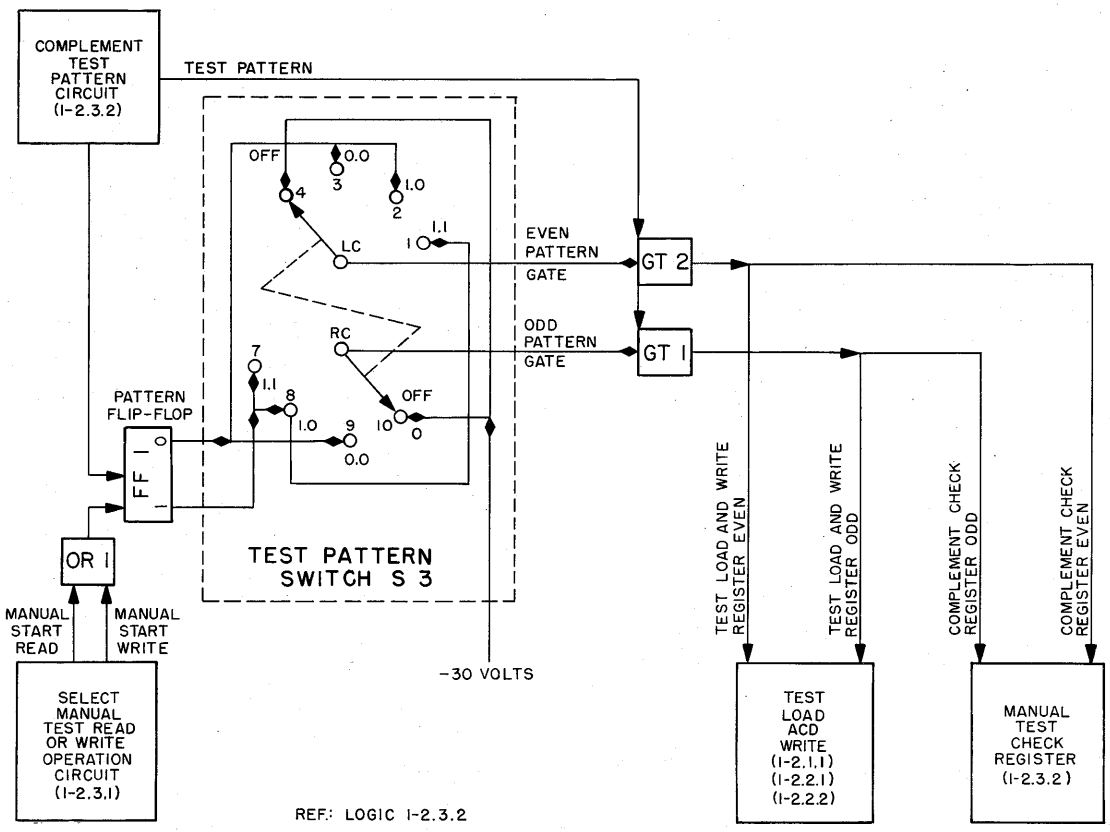


Figure 3–9. ACD Manual-Test-Pattern-Selection-and-Control Circuits, Simplified Logic Diagram

The outputs of the pattern flip-flop go to the contacts of TEST PATTERN switch S3. When the flip-flop side connected to any given contact is up, +10 volts are seen at the contact. When the flip-flop side is down, −30 volts are applied to the contact. Table 3–2 outlines the voltages present at the two wiper arms of the TEST PATTERN switch when the flip-flop is set and cleared for each position of the switch.

TABLE 3–2. TEST PATTERN SWITCH OUTPUT VOLTAGES (AUXILIARY DRUMS)

SWITCH POSITION	SWITCH CONTACT	WIPER ARM	VOLTAGE WITH FLIP-FLOP SET (VOLTS)	VOLTAGE WITH FLIP-FLOP CLEARED (VOLTS)
OFF	4	LC	−30	−30
	10	RC	−30	−30
0.0	3	LC	−30	+10
	9	RC	−30	+10
1.0	2	LC	−30	+10
	8	RC	+10	−30
1.1	1	LC	+10	−30
	7	RC	+10	−30

The output of the RC wiper arm is the odd-pattern-gate level; the output of the LC wiper arm is the even-pattern-gate level. The odd- or even-pattern-gate levels are logically present only when they are positive. The odd-pattern-gate level, when present, conditions GT 1. The even-pattern gate level, when present, conditions GT 2. Gates 1 and 2 receive a test pattern pulse from the complement-test-pattern circuit (refer to 5.1.5). Whichever gate (or gates) is conditioned passes the pulse. The GT 1 output goes to the test-load-CD-write circuit as a test load-ACD-write-register-odd pulse and to the manual-test-check-register circuit as a complement-check-register-odd pulse.

The output of GT 2 duplicates the functions of the output of GT 1, but as even pulses. Thus, the GT 2 output produces a load ACD-write-register-even pulse and a complement check-register-even pulse. Whenever an output of GT 1 or 2 is present, it causes the writing of 1 bits in the associated register location of the write circuit. Thus, if the GT 1 output is present, 1's are written in the odd-numbered bits (L1, L3, ... R1, R3, ... and so on) of the write circuits to which it is applied. In the same

way, the GT 2 output causes 1's to be written in the even-numbered register locations (L2, L4, ... R2, R4 . . . . and so on) of the write circuits to which it is applied.

5.1.5 Complement-Test-Pattern Circuit

The operation of the ACD complement-test-pattern circuit (fig. 3–10) is closely allied to the operation of the ACD manual test-pattern-selection-and-control circuit, described in 5.1.4. The ACD complement-test-pattern circuit is employed in the production of the test-pattern pulse, which senses the condition of the pattern flip-flop and TEST PATTERN switch for the various write circuits involved in manual tests. In addition, the ACD complement-test-pattern circuit produces the complement-test-pattern pulse, which complements the pattern flip-flop in the manual-test-pattern-selection circuits.

The test-pattern pulse is produced during both manual test read and manual test write procedures. During manual test write, the manual-test-control circuit produces a test-write pulse which passes GT 1 (fig. 3–10). The production of a manual-test level from the begin-manual-test circuit is sent to GT 1, which passes the test-write pulse to OR 1. The OR 1 output is the test-pattern pulse.

During manual test read operation, the manual-test-control circuit sends a test-read level to GT 3, conditioning the gate. The pulse input to GT 3 is obtained from the CD-read-write-control circuit. The pulse obtained from this circuit, a CD-write-sample, is delayed 2.5 usec and applied to GT 3, which has previously been conditioned by the test-read level from the manual-test-control circuit, as described above. The output of GT 3 is applied to OR 1. The delayed read-sample pulse also goes to the manual-test-error circuit as an alarm sample. Thus, it can be seen that, during manual test write operations, the test-pattern pulse is produced at CD 1 time; during manual test read, the test pattern pulse and the alarm pulse are produced at CD 2 time.

The test-pattern pulse may also be used in the production of the complement-test-pattern pulse, which is sent to the manual-test-pattern-control circuits. In these circuits, the complement-test-pattern pulse reverses the state of the pattern flip-flop. The pulse is developed by operating COMPLEMENT TEST PATTERN switch S7. This applies a d-c level to GT 4, passing the test-pattern pulse to form the complement-test-pattern pulse.

5.1.6 Manual-Test-Check-Register Circuit

The ACD manual-test-check-register-and-control circuit (fig. 3–11) provides a means of checking the contents of words written by the manual-test-pattern-control and complement-test-pattern circuits. As was indicated in 5.1.4 and 5.1.5, a test-pattern pulse is developed during manual test write operations, which causes the manual-test-pattern-control circuit to send a test-write pulse to the write register. The test-write pulse may to the odd, even, or all flip-flops of the write register, as determined by the manual-test-pattern-control circuit.

When manual test writing is completed, a manual test read operation checks the pattern that has been written. All flip-flops in the manual-test-check register are cleared at the start of a test. All flip-flops that should have 1 bits after reading receive at CD 2 time a complement pulse. If the pattern that should have been written is read, all flip-flops in the manual-test-check register are cleared. If, however, a flip-flop that should have a 1 bit

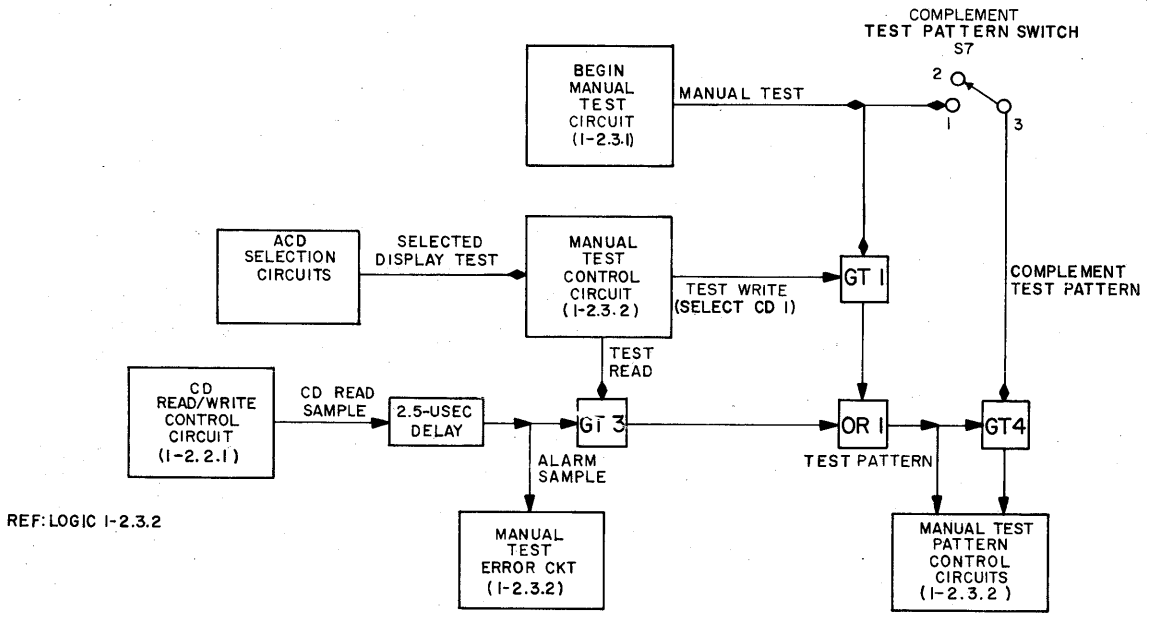


Figure 3–10. ACD Complement-Test-Pattern Circuit, Simplified Logic Diagram

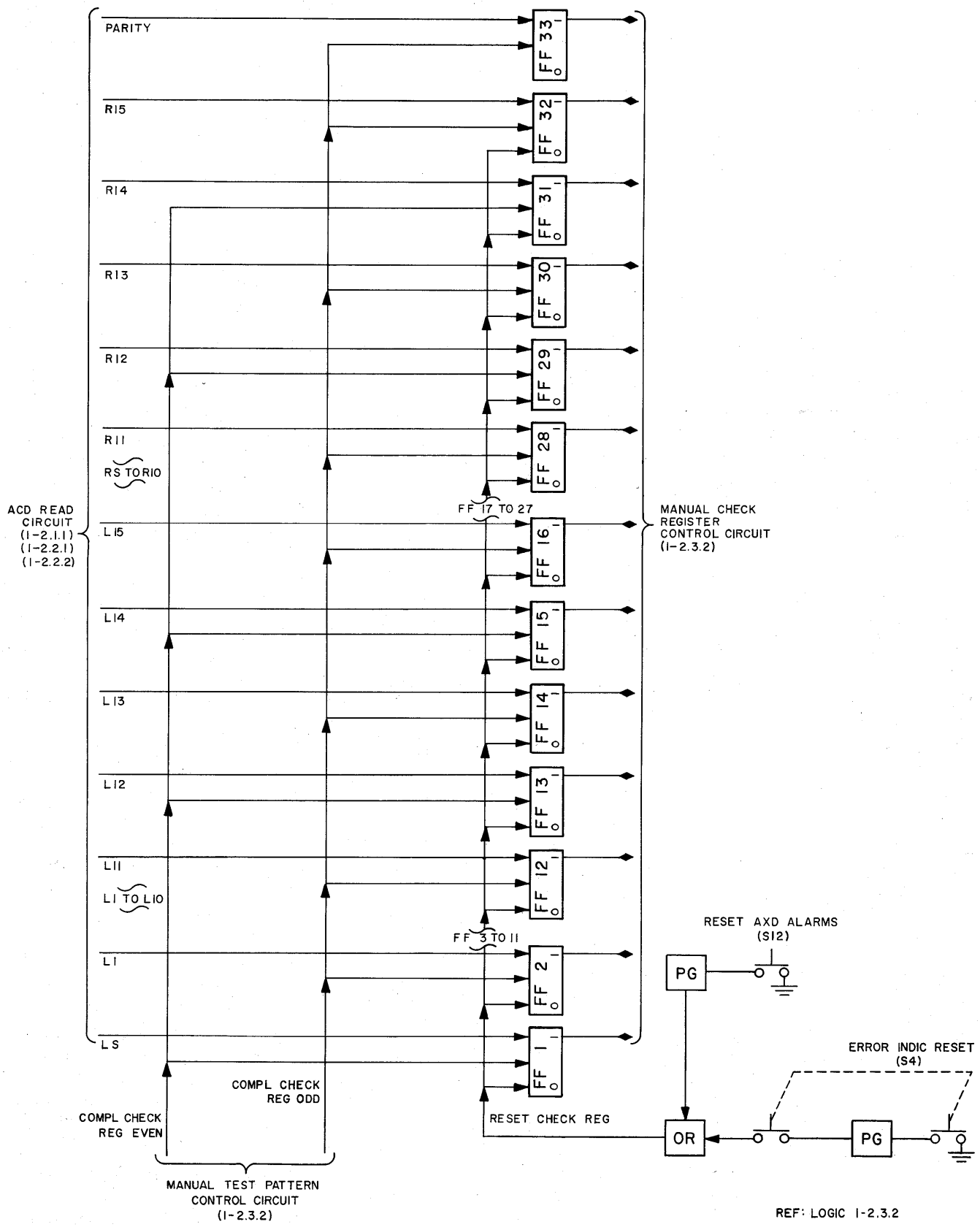


Figure 3–11. ACD Manual-Test-Check-Register-and-Control Circuit, Simplified Logic Diagram

has a 0 bit instead, the complement pulse sets that flip-flop, causing an error indication. If the STOP ON ERROR switch is in the STOP ON ERROR position, the test is stopped, and the bit in which the error occurred is indicated by the check register indicator lamps. The check register is cleared by switch S4 or S12, which develops the reset-check-register pulse.

To sum up the operation of the manual-test-check-register, the presence of a 1 bit in any flip-flop after CD 2 time indicates an error. The 1 bit is sent to the manual-test-error circuit and produces an error indication there that stops drum operations. The neon lamps connected to the flip-flops then indicate which drum bit is being incorrectly transferred.

5.1.7 Manual-Test-Read-Write-1-Revolution-Control Circuit

During most of the tests performed, it is desirable to test drum operations for only one drum revolution, or its equivalent. The test read or write operations can be stopped at the end of one revolution of a drum field or at the end of the number of revolutions it takes to complete the read or write operation. The controls that stop the operation at the end of one revolution are shown in figure 3–12.

When OPERATE 1 REV switch S6 is closed, the manual-test level from the begin-manual-test circuit is applied to AND 1. The production of the ACD -read-compare or ACD-write-compare pulse (depending upon which operation is to be performed) by the ACD-read-write-control circuit causes conduction in AND 1. The output of AND 1 conditions GT 1 to pass a test-angular-position-counter-end-carry pulse from the manual-test-angular-position-counter-and-alarm circuit. The test-angular-position-counter-end-carry pulse is produced when all the registers of the field selected for test have had either a read or write operation performed on them. (Refer to 5.1.8 for a discussion of the manual-test-angular-position-counter-and-alarm circuit.) The output of GT 1 is delayed 2.5 usec to produce a disconnect-1-revolution pulse. The disconnect-1-revolution pulse goes to the ACD-read-write-control circuit and stops the read or write operation that is in progress.

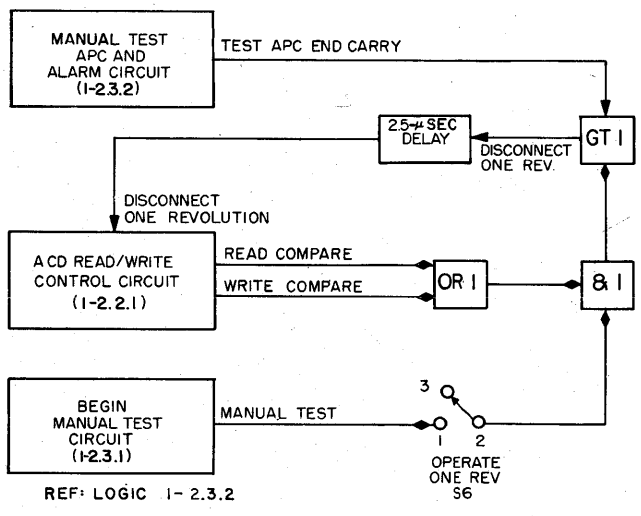


Figure 3–12. ACD Manual Test Read-Write-1-Revolution-Control Circuit, Simplified Logic Diagram

5.1.8 ACD Manual-Test-Angular-Position-Counter-and-Alarm Circuit

The ACD manual-test-angular-position-counter-and-alarm circuit in the manual drum test circuits is employed to provide a means of indicating the drum register being read or written when an error is detected during manual test.

The circuit controlling the operation of the ACD manual-angular-position-counter-and-alarm circuit is shown in figure 3–13. At the beginning of a manual test, the first APC-end-carry pulse causes the reading or writing operation to begin. The second APC-end-carry pulse causes the operation to discontinue. After each APC-end-carry pulse, the test-select index pulse goes to GT 1 and is passed to the 11-stage-angular-position counter as a clear-angular-position-counter pulse. This pulse clears the flip-flops in the 11-stage-angular-position counter, which is a standard serial-counting circuit.

During all tests, select-ACD 3 pulses from the timing pulse distributors are fed to GT 2. As in the case of GT 1, GT 2 is conditioned by AND 1. AND 1 receives two levels, a test-APC-operate level from the manual-test-read-write-1-revolution-control circuit and a +10-volt level. The output of GT 2 is the test-angular-position-counter step pulse, which goes to the 11-stage-angular-position. At the 2,048th select-CD 3 pulse, the angular-position counter forms a test-angular-position-counter-carry pulse which clears FF 1. (Flip-flop 1 is initially set by the test-select-ACD 1 pulse from the timing pulse distributor.) At CD 1 time of the next register, a select-CD-index pulse from the timing pulse distributor causes the production of a clear-angular-position-counter pulse, which clears the flip-flops of the 11-stage-angular-position counter and goes to GT 3. If a malfunction is present in the 11-stage-angular-position counter, the test angular-position-counter-end-carry pulse is not developed in time to clear FF 1 before receipt of the clear-angular-position-counter pulse. The resulting 1-state level from FF 1 conditions the passing of the clear pulse by GT 3 to produce a test-angular-position-counter-error pulse, which goes to FF 3. As a result, neon lamp I43 is lighted, indicating the presence of an error.

If an error is detected at any time during a test, the presence of that error in the manual-test-read-write-1-revolution control causes the removal of the test-APC-operate level. Should this error occur during the middle of a drum revolution, the removal of the test-APC-

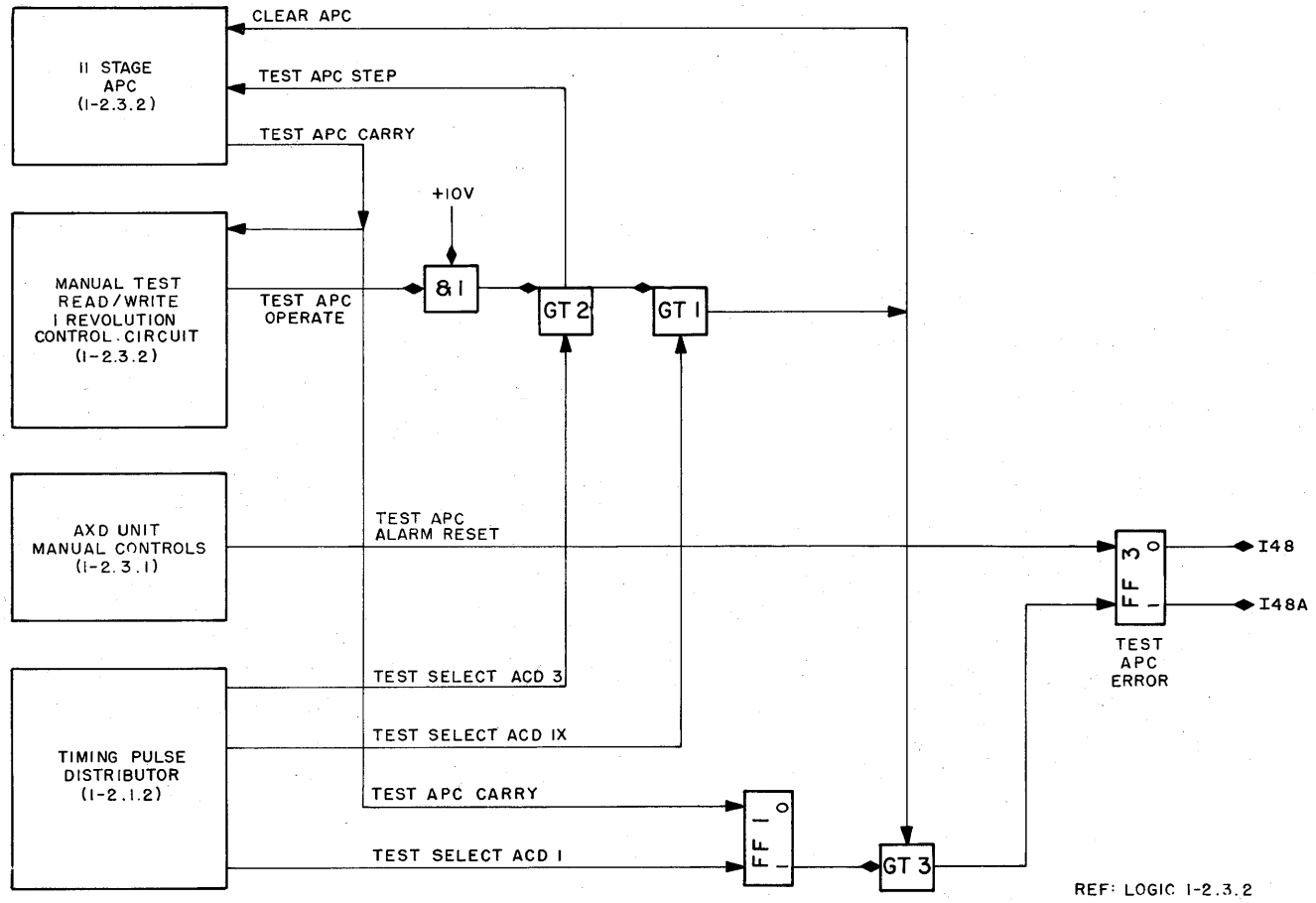


Figure 3–13. ACD Manual Angular-Position-Counter-and-Alarm Circuit, Simplified Logic Diagram

operate level from GT's 1 and 2 stops the counter. Neon indicating lamps are connected to the flip-flops in the 11-stage counter and indicate the setting of the counter at the time counting is stopped.

Test-angular-position-counter-carry pulses are sent to the manual-test-read-write-1-revolution-control circuit whenever they are produced, to be employed as a means of starting manual tests and then stopping them at the end of one drum revolution.

5.1.9 ACD Manual-Test-Error Circuit

The ACD manual-test-error circuit, shown in figure 3–14, provides a means of stopping drum operations when errors are detected during manual test.

The presence of a 1 bit in the left half-word of the manual-check-register circuit, following a complement of the register flip-flops, indicates an error in a pattern test. The 1 bit causes conduction in OR 1. In the same way, an error in the right half of the check register word is indicated by a 1 bit that causes conduction in OR 2. If OR 1 or 2, or both, have an input, the resulting output produces conduction in OR 3. The output level produced by OR 3 (manual-check-register-error level) conditions GT 1 to pass an alarm-sample pulse from the complement-test-pattern circuit (refer to 5.1.5) to FF 1, the not-error flip-flop. When FF 1 is cleared, the 0-state-output level goes to I58 and ACD manual-test-read-write-control circuit. If STOP ON ERROR switch S5 has been operated, GT 2 is conditioned to pass the output of GT 1 to the CD-read-write-control circuit. This pulse stops the test at the point at which the error is detected.

A manual-disconnect pulse, which has the same effect as the test-error-disconnect pulse or the Central-Computer-System-disconnect pulse, is generated by depressing DISCONNECT pushbutton S9.

In order to resume operations on the field being tested or on a new field, it is necessary to depress ALARM INDICATOR RESET pushbutton S4. The ALARM INDICATOR RESET pushbutton, like the DISCONNECT pushbutton, applies a d-c level to the pulse generator, causing a single pulse to be produced across the second pair of pushbutton contacts. This pulse goes to FF 1 as an alarm-reset pulse which clears the flip-flop. This pulse also goes to I58 and the manual-test-read-write-control circuit.

5.2 ERASE-REWRITE CONTROL

The erase and timing-rewrite circuits for the auxili-

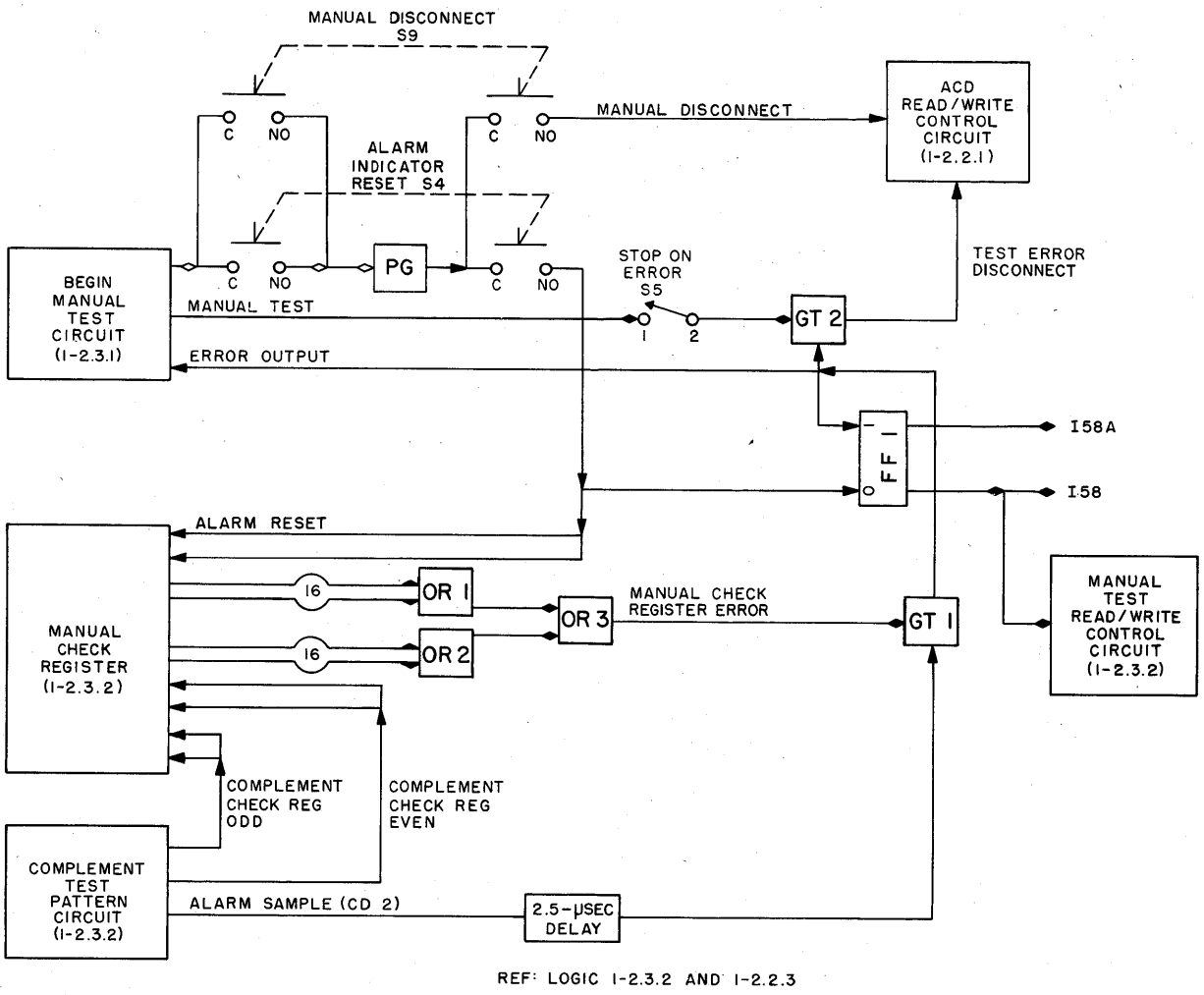


Figure 3–14. ACD Manual-Test-Error Circuit, Simplified Logic Diagram

ary drums are identical with those used in the main drums (compare logic drawings 1.2.3.3 and 1.7.3). The manual erase controls are located on the test door on unit 20D (see fig. 3–5). (For a detailed discussion of these circuits, refer to 9.3 in Part 2.)

5.3 DRUM-MOTOR-CONTROL CIRCUITRY

The motor-control circuits for the auxiliary drums are identical with those used in the main drums. The manual controls are on the test door on unit 20D. (For a detailed discussion of these circuits, refer to 9.4 in Part 2.)

PART 4
SPECIAL CIRCUITS

CHAPTER 1
INTRODUCTION

The Drum System employs a number of special circuits in addition to the basic circuits used throughout AN/FSQ-7 Combat Direction Central. These special circuits permit the performance of operations that would be less reliable, less economical, extremely difficult, or impossible, using basic circuits. Special circuits used only in the Drum System include drum write drivers, drum writers, drum read amplifiers, drum field drivers, drum read drivers, and timing pulse generators. There are special applications in the Drum System of certain devices and circuits which are used to perform different functions in other systems. Included among the latter are magnetic drum assemblies, diode-switching networks, and model G power cathode followers.

Magnetic drum assemblies, which contain magnetic drums and drum heads, provide a means of organizing and storing binary information. Drum write drivers and drum writers are used to transfer information into magnetic drum assembly storage; drum read amplifiers are used to transfer information out of magnetic drum assembly storage. Drum field drivers, drum read drivers, power cathode followers, and diode switching networks provide a means of switching Drum System operations in a manner that avoids parts duplication. Timing pulse generators are used to generate timing pulses that time and control system operations.

Analyses of the special circuits used in the Drum System are approached from a purely electronic view, rather than a logical one. The special circuits are analyzed in two stages: (1) a block diagram analysis which is intended to convey to the reader a general understanding of the special circuit and (2) a detailed, stage-by-stage circuit analysis describing the action on a signal from input to output.

The special circuits of the Drum System are discussed in detail in Chapters 2 through 11. Chapter 2 discusses the theory, physical construction, and arrangement of drums and drum heads. Chapters 3 through 11 discuss the drum write driver, drum writer, drum read driver, drum read amplifier, drum field driver, model G power cathode follower, diode switches, optical frequency generator, and the timing pulse generator, respectively.

CHAPTER 2
MAGNETIC DRUM ASSEMBLY

2.1 THEORY OF READING, WRITING, AND ERASING

2.1.1 Magnetic Drum Reading and Writing

Words and numbers are written on the surface of a drum by the use of coils wound on magnetic cores which are split by small transverse air gaps. Each air gap is placed adjacent to the magnetic surface of the drum.

The coil and core are combined in an assembly called a drum head. The magnetic surface of the drum is a thin, nickel-cobalt plating.

If direct current flows through the drum head, fringing flux at the gap magnetizes the spot on the magnetic drum surface that is adjacent to the gap. This process of inducing flux in the magnetic drum surface is called writing. If the magnetic drum is set in rotation, the magnetized spot remains on the drum, and a voltage is developed across the coil in the head every time the magnetized spot (bit) passes under the air gap. The process of inducing voltage across the coil by moving the bit past the head is called reading. Since the magnetized spot is not affected by reading, this type of reading is called nondestructive.

The relationship of the flux distribution pattern written on the drum surface and the read voltage induced in the head with respect to time is illustrated in figure 4–1. Before the bit reaches the gap at time 1, flux (and, therefore, induced voltage) is zero. From time 1 to time 2, fringe flux is small and induces a small voltage. From time 2 to time 3, flux increases more rapidly, inducing a larger voltage. Time 3 to 4 represents the greatest area of flux change (maximum positive slope) and consequently the period of maximum induced voltage. From time 4 to time 5 the rate of flux change is smaller, although the amount of flux continues to increase until it reaches a maximum value at time 5. Since the rate of flux change from time 4 to time 5 is approximately similar to that from time 2 to time 3 (although in the opposite direction), the voltage induced is approximately equal.

Preceding time 5, the maximum flux point on the bit approaches the center of the air gap; at time 5, it is exactly under the gap. The rate of flux change is zero (zero slope) at time 5. Therefore, the voltage induced in the head is also zero. Time 5 is also the voltage polarity crossover point. From time 5 to time 9 (as the magnetized bit recedes from the gap) flux decreases, producing a voltage similar to that produced from time 1 through time 5, but opposite in polarity.

If the direction of current flow through the writing head is reversed during writing, the direction of magnetizing flux is reversed and the direction of bit magnetization is also reversed. Thus, during reading, the polarity of induced voltage at all points is the reverse of that shown in figure 4–1.

In the Drum System, both reading and writing are accomplished while the drum rotates at constant speed. However, with direct current flowing through the drum head while the drum rotates, a complete strip (channel) passing around the drum circumference under the drum head would be magnetized by fringing flux. Use of brief current pulses (which produce magnetization of only a small area) instead of direct current prevents this total magnetization of a channel. Maximum information storage is approached in the Drum System by using an optimum pulse width of 1.5 usec.

In addition to pulse width and drum speed, bit length is also determined by the width of the air gap in the head and by the distance between the drum head core and the magnetized drum surface. The gap width is usually set at 0.001 inch. Core-to-drum spacing is also set at 0.001 inch to permit optimum flux density and to

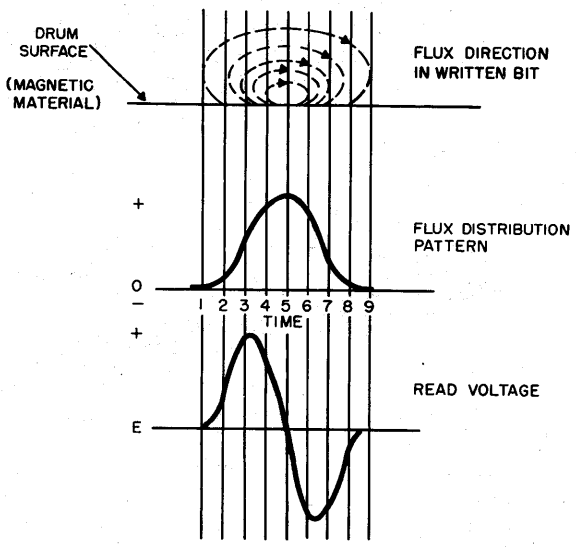


Figure 4–1. Flux Distribution Pattern and Read Output Voltage Produced by Writing on a Stationary Drum

maintain a safety factor that prevents the drum head from touching the rotating drum. The 0.001-inch spacing represents a compromise between close and safe spacing. The magnitude of the write circuit pulse determines the amount of flux induced on the drum surface.

Since bits are written with sufficient magnitude to produce maximum flux density in the magnetized bit area, a bit of opposite polarity can be written over an existing bit by sending a current pulse of the same magnitude but opposite polarity through the drum head. A write current of 110 milliamperes (ma) produces bit saturation but is not high enough to spread flux into adjacent areas.

2.1.2 Theory of Erasing

The entire drum surface is erased by first saturating the drum surface with an a-c field and then slowly reducing the field strength to zero. At the beginning of the erasing procedure, the a-c field produces flux densities at the drum surface that are stronger than the flux densities produced by the write pulses. The varying polarity of the a-c field causes a varying polarity of the flux induced on the drum surface. As the strength of the a-c field is reduced, each reversal of the a-c field polarity produces an induced flux density that is lower than that of the previous cycle. When the a-c field is finally reduced to zero, the residual magnetism in the drum produced during writing is also zero, resulting in the drum being completely erased. Erasing is usually employed in abnormal operation to rid the drum surface of noise. It is not necessary to erase the drum to change the information in its register; the register may be changed by writing the desired word over the old one.

2.2 MAGNETIC DRUM ASSEMBLY DESCRIPTION

2.2.1 Magnetic Drum

The magnetic drum shown in figure 4–2 is a monel cylinder that has been coated with copper and then plated with nickel-cobalt to a depth of 0.0005 inch. The magnetic drum is 10.7 inches in diameter and 12.5 inches long.

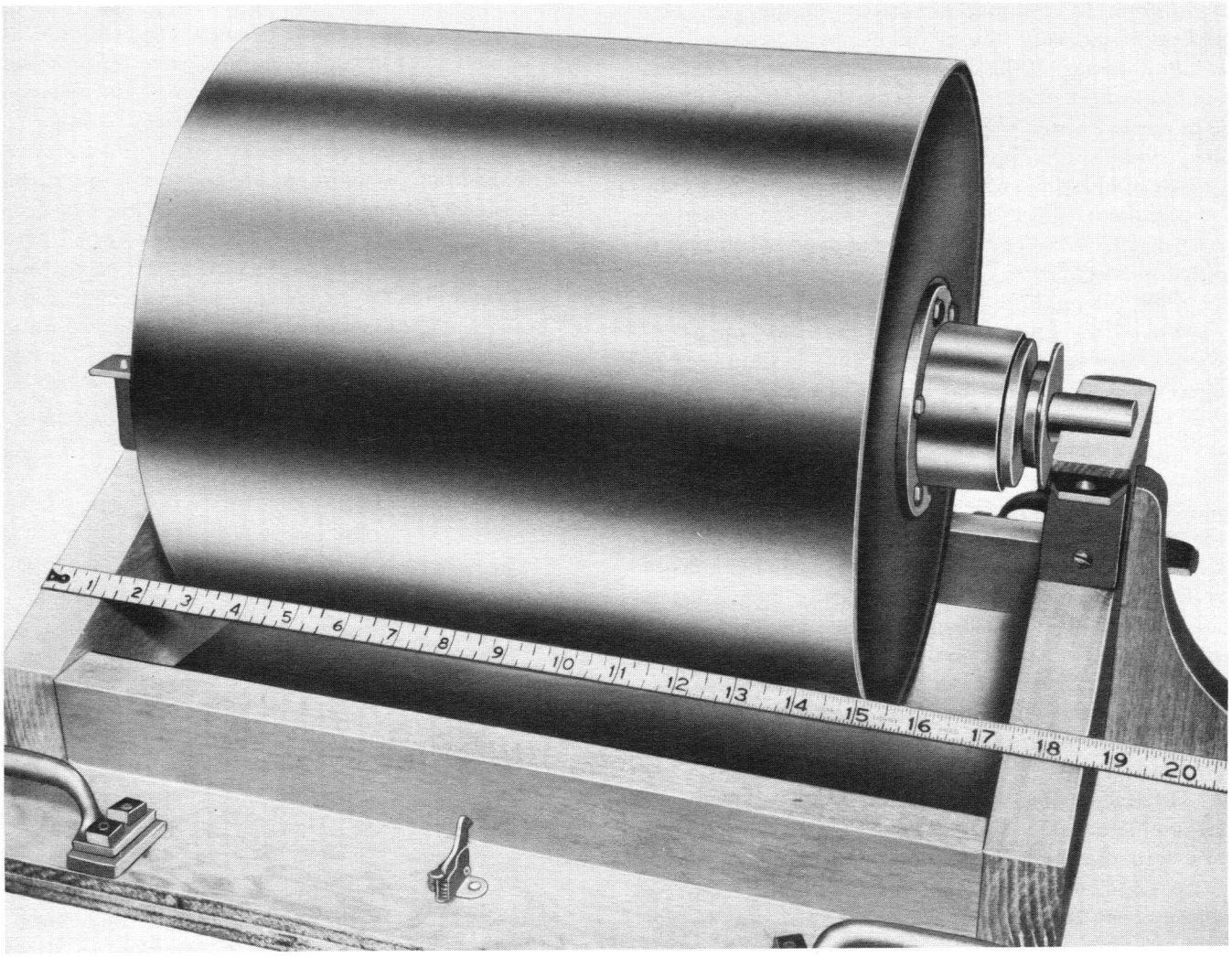


Figure 4–2. Magnetic Drum

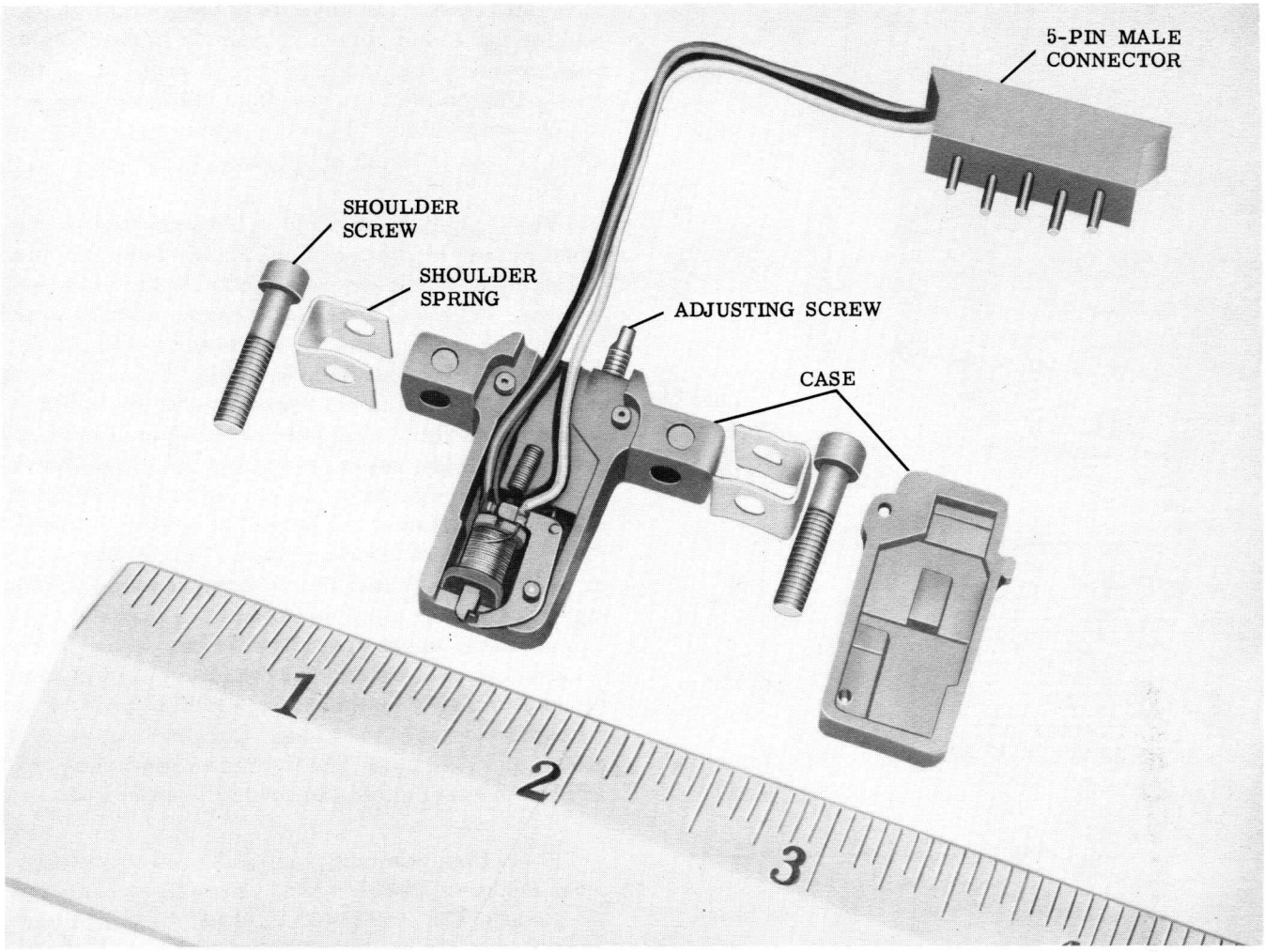


Figure 4–3. Disassembled View of Drum Head

2.2.2 Drum Read-Write Heads

All drum heads in the Drum System are identical. The same head-type is used for both reading and writing, but, in some cases, individual heads are connected to perform only one operation. Figure 4–3 shows a typical drum head. Drum head cores consist of nine insulated laminations, 0.002 inch thick. A 0.001-inch thick copper shim is soldered into place in the air gap to keep its size constant. A bobbin is slipped over the core. (See fig. 4–4.) The read-write coil on the bobbin is center-tapped and is used during both reading and writing.

The coil and core assembly are contained inside a 2-piece, open-bottomed case which is mounted in a fixed position over the magnetic drum. The case contains a compression spring and a tapered, core-adjusting screw. The compression spring presses down on one side of the core, rotating the core around a pivot. This turns the air gap closer to the magnetic drum surface and changes the angle which the air gap makes with the magnetic drum surface. A stud attached to the core presses against the side of the tapered, core-adjusting screw. This stud limits rotation of the core by the compression spring. As the screw is turned deeper into the case, the core rotates around the pivot in a direction opposite to that produced by the compression spring. The rotation produced by the tapered, core-adjusting screw, therefore, moves the air gap away from the drum. Two shoulder screws passing through mounting ears on the drum head case and two U-shaped shoulder springs fasten each complete drum head to a mounting bar which has its longitudinal axis parallel to the drum surface. Varying the depth to which each of the shoulder screws is turned provides a fine adjustment of the angle between the air gap and magnetic drum surface and of the distance between them.

2.2.3 Drum Head Arrangement Related to Logical Arrangement

As has been indicated, a short-duration current pulse is applied to a drum head coil to produce a flux pattern

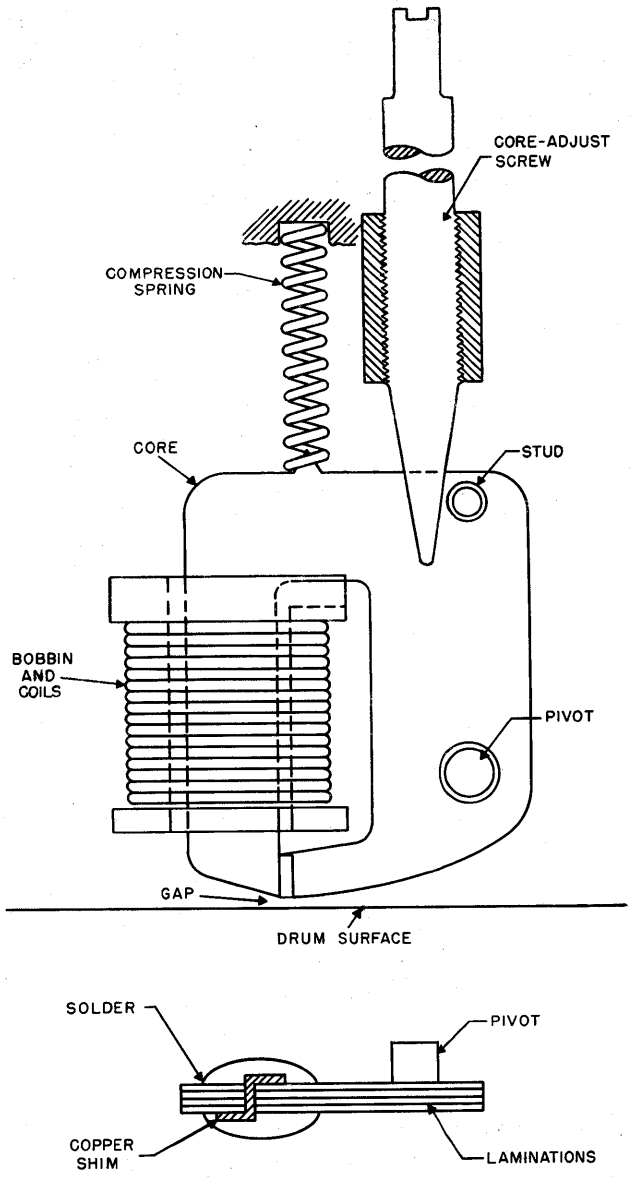


Figure 4–4. Details of Drum Head Assembly

that represents a 1 bit or a 0 bit on the magnetic drum surface. As the magnetic drum rotates, bits are continously written on the area that passes under the mechanically fixed drum head.

Drum heads are mechanically fixed by mounting them on six pairs of horizontal drum mounting bars axially arranged around the drum in an arc of 216 degrees. Figure 4–5 shows one pair of drum mounting bars on the drum casing. Forty heads can be mounted on each head mounting bar, making it possible to mount a total of 480 drum heads on each magnetic drum assembly. One drum head mounting bar in each pair of bars contains the drum heads used in CD operations on one type of data. The other head mounting bar of the same pair contains the drum heads used in OD operations, on the same data type. In addition to the 12 drum head mounting bars, an erase bar is mounted on the drum casing between the first drum head mounting bar and the drum casing. The erase bar extends over the entire horizontal length of the drum surface.

The physical arrangement of magnetic bits on the drum surface is illustrated in figure 4–6. The bits written by each read-write head encircle the drum and constitute a channel. A channel is the same width as an individual bit. Thirty-two of the channels available for drum heads on any one drum mounting bar usually store data bits. A 33rd channel stores a parity bit which is used by the Central Computer and Output Systems to perform reliability checks on the data being transferred. During system operation, the 32 information channels and the parity channel can be read or written simultaneously during each 10-usec period. The 33 bits in 33 channels written or read at one instant comprise a drum register. There are 2,048 operational registers about the circumference of the drum. The 33 bits stored in the drum register at any given time comprise a word. A number of words that constitutes an organized piece of information is known as a message. One drum register or a group of consecutive drum registers containing the word or words of a complete message is called a slot.

It has been seen that as the drum rotates the maximum number of heads mounted on any single bar covers 40 channels. The 40 channels store one drum field; each drum field stores only one type of data. For example, the long-range radar field stores only long-range radar data. Since 33-bit words are usually used, 33 channels are usually used for each field. There are two exceptions to this rule; radar data fields have 24-bit words, and gap-filler input fields have 26-bit words. In addition to the channels used to store words, each magnetic drum uses one channel to store timing information and one channel to store indexing information. On most drums, additional channels store information used by specialized control circuits.

The large physical size of drum head assemblies in relation to the width of the channel written by the drum head is shown in figure 4–7. Since the drum head assemblies are adjacently mounted on the mounting bars, there is an area of unused space between channels. This unused space is wide enough to contain five additional channels. In order to utilize this space, the heads in each pair of mounting bars are displaced laterally with respect to the heads in the preceding mounting bar. The amount of displacement is one-sixth of the distance between any two adjacent heads. The CD and OD drum heads on any one field are not displaced but are aligned

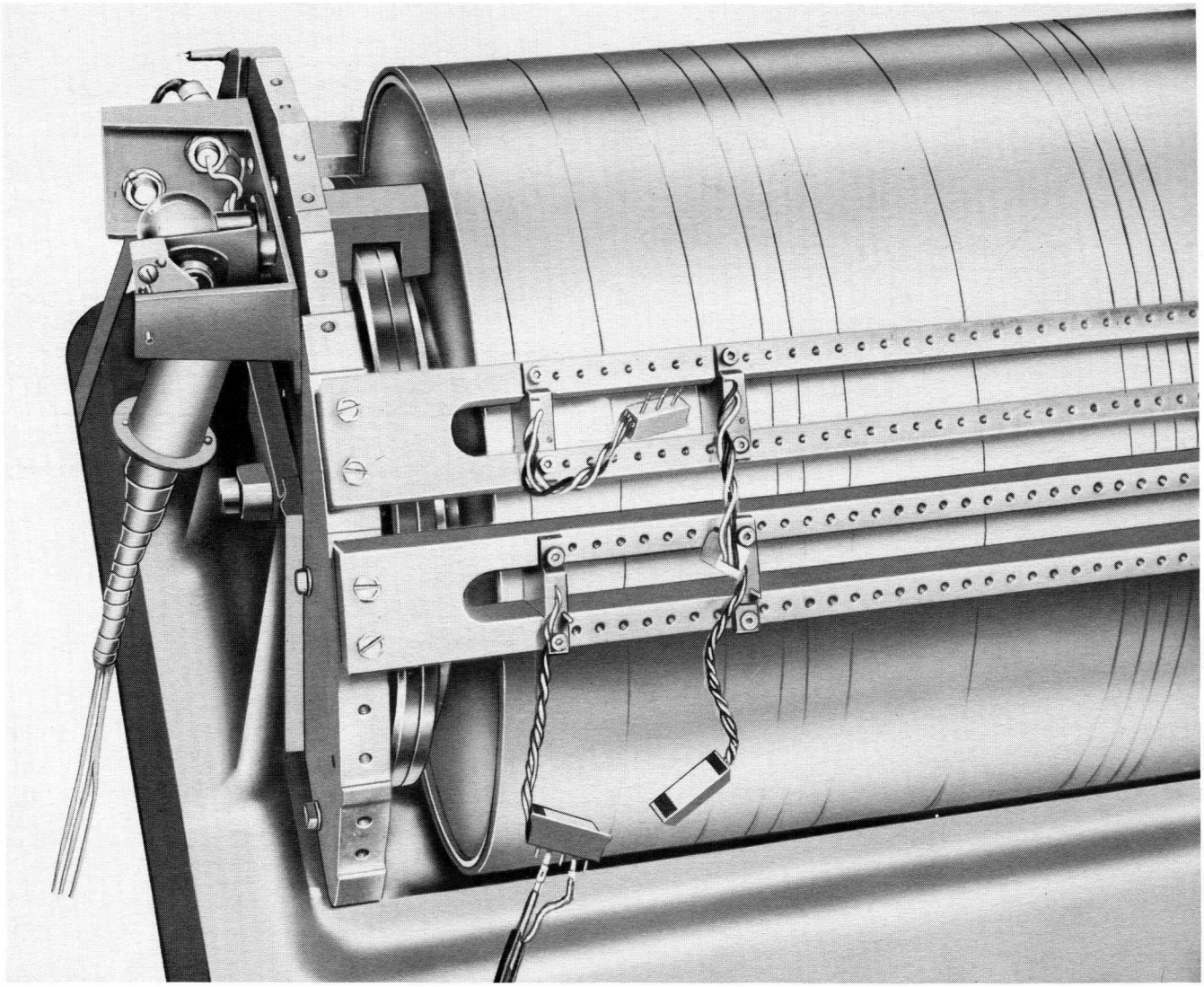


Figure 4–5. Mounting Bar Pair on Drum Casing

to cover the same channels. In some control circuit applications, two heads on different mounting bar pairs are aligned to cover the same channel.

Figure 4–8 illustrates how bits 1 and 2 of six difference fields are displaced with respect to each other in order to cover the entire drum surface.

Six fields of information are stored on all of the drums except the radar data drum. The radar data drum, which stores 24-bit words, has nine fields. Figure 4–9 shows the bit arrangement on the RD drum.

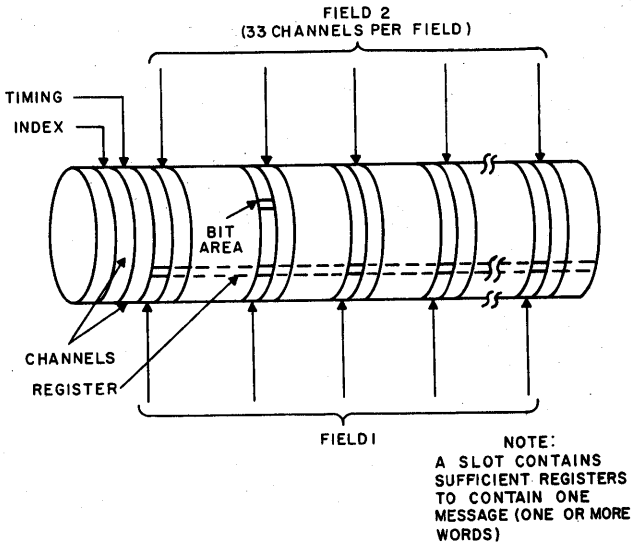


Figure 4–6. Relationship of Drum Terms

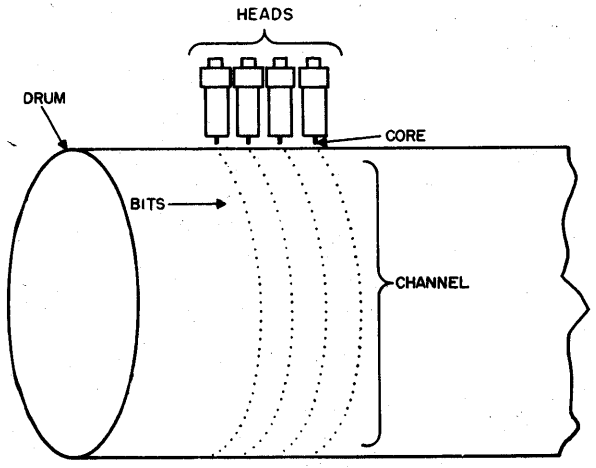


Figure 4–7. Relationship of Drum Head Assembly Size to Channel Width

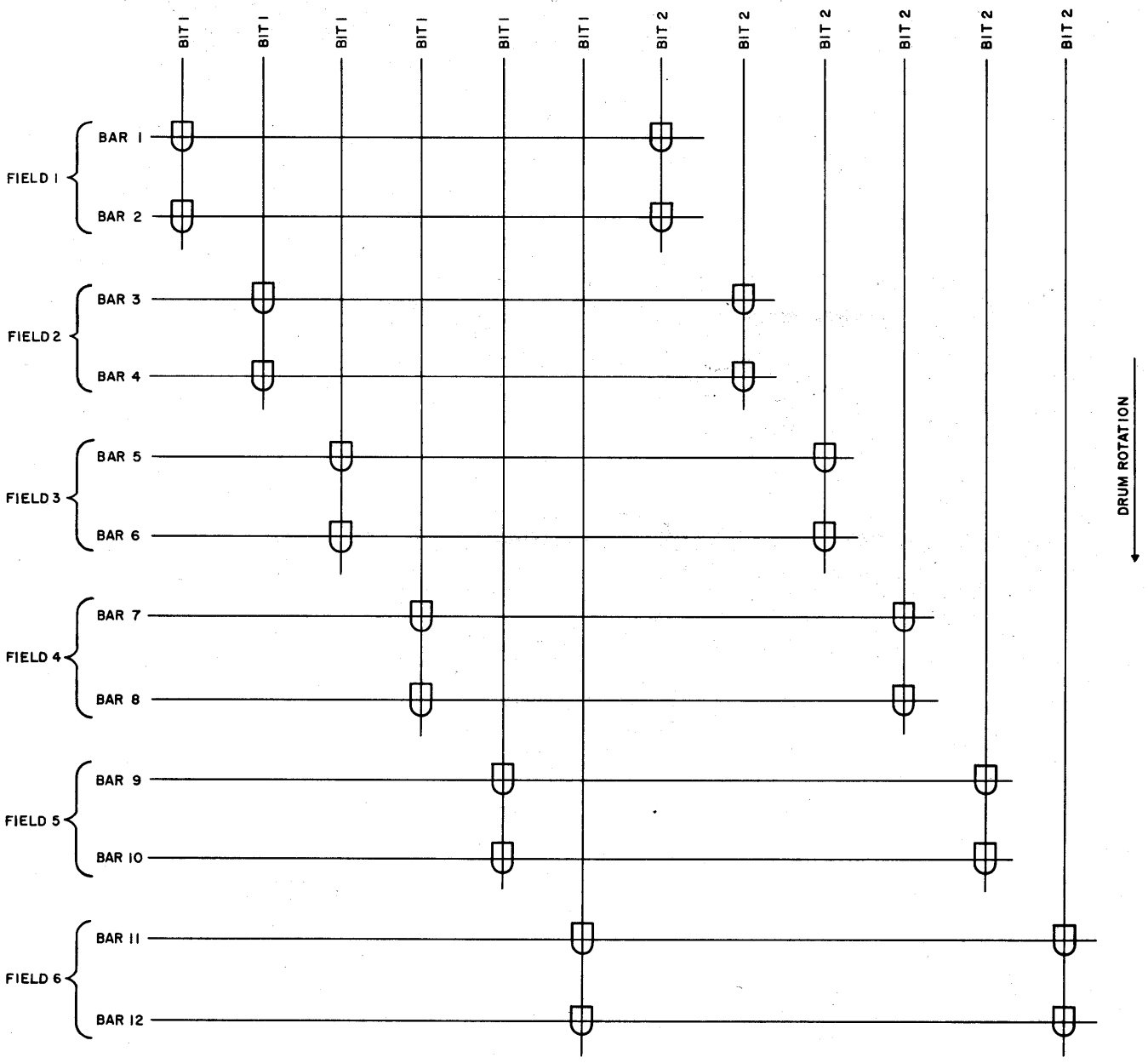


Figure 4–8. Magnetic Heads Arrangement of Mounting Bars

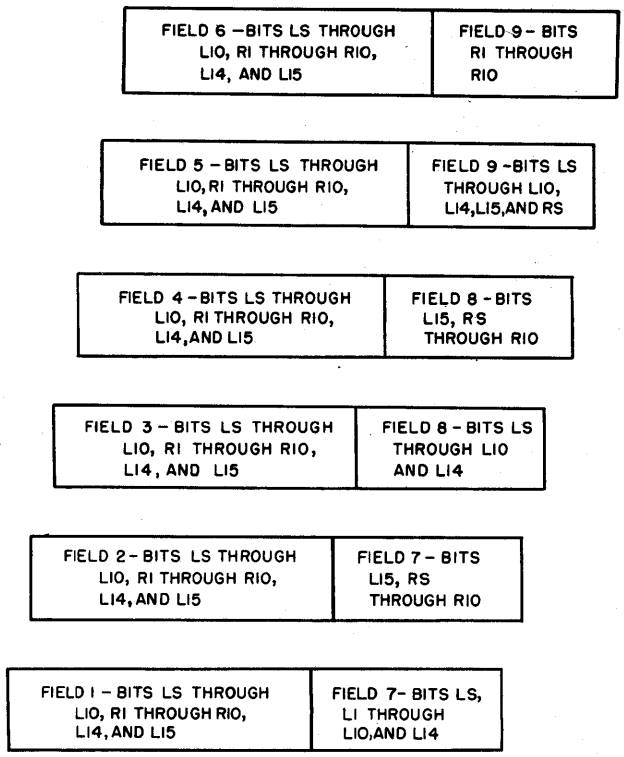


Figure 4–9. Bit Arrangement on Radar Data Drum for Nine Fields

CHAPTER 3

DRUM WRITE DRIVERS, MODELS A AND B

The drum write driver is a power amplifier which inverts a d-c command signal and applies it to the drum writers, causing them to generate write pulses for their associated drum heads. Two models of drum write drivers are used in the Drum System, model A and model B.

The model A drum write driver is used for applications in which the drum heads are driven through diode switching networks which transfer operations from reading to writing or vice-versa, upon the application of the proper command signals. The model B drum write driver is used for applications requiring direct drum head drive where only writing operations are to be performed.

3.1 DRUM WRITE DRIVER, BLOCK DIAGRAM ANALYSIS

Figure 4–10 is a block diagram of a drum write driver circuit. A negative-going square wave developed by a pulse stretcher flip-flop in the write circuit is applied to the input amplifier V1 and V2. In the input amplifier stage, the negative-going input is amplified and inverted. The amplified signal is then sent to a cathode follower stage. This cathode follower stage develops the power necessary to drive 12 drum writers if a model B drum write driver is being considered or 33 drum writers if a model A drum write driver is being considered.

3.2 MODEL A DRUM WRITE DRIVER, CIRCUIT ANALYSIS

A schematic diagram of a model A drum write driver is illustrated in figure 4–11. The input signal to a model A drum write driver is the —30-volt pulse that is generated on the 0 side of a model A flip-flop when the flip-flop is set for 1.8 usec. This negative pulse is applied to paralleled input amplifiers V1 and V2. Amplifiers V1 and V2 operate as a single amplifier stage. (See fig. 4–12.) Resistor R6 and capacitor C2 at the input form a decoupling network which serves to isolate the drum write driver from the flip-flop.

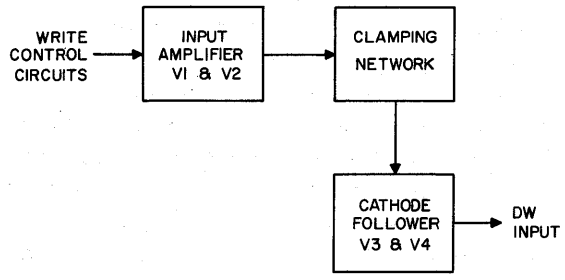


Figure 4–10. Drum Write Driver, Block Diagram

The negative input at the control grids of tubes V1 and V2 causes a positive pulse to be developed in the plate circuit. (See fig. 4–11.) Inductor L1 in the plate circuit produces a shorter rise time in this pulse by presenting a higher impedance to high-frequency components of the pulse. Crystal CR5 in the cathode circuit of the two tubes prevents cathode voltages from dropping below ground potential. The RC networks made up of resistor R5 and capacitor C1 and resistor R13 and capacitor C7 form decoupling networks for the power supply voltages. The 47-ohm resistors in the grid circuits suppress parasitic oscillations. The positive output of tubes V1 and V2 is coupled by capacitor C3 to the parallel-connected grids of tubes V3 and V4.

In the grid circuit of tubes V3 and V4, crystals CR1, CR2, CR3, and CR4 clamp input signals to the cathode follower between —105 volts and +10 volts. (See fig. 4–12.) In a quiescent state, crystals CR1 and CR2 are cut off and potentials developed between points A and B cause crystals CR3 and CR4 to conduct. Points A and B are effectively short-circuited. A —105-volt potential is developed at point A by the applied voltages. When a positive signal is applied to point A of the clamper circuit, point A becomes more positive than point B and crystals CR3 and CR4 stop conducting. Therefore, resistor R11 and resistors R18 and R19, which are paralleled by the back resistance of CR3 and CR4, form the input grid resistance for V3 and V4. Crystals CR1 and CR2 conduct when the input signal rises above +10 volts, clamping point A at +10 volts.

The output of the cathode follower is taken from the junction of resistor R28 and the combined resistance presented by 33 externally connected drum writers. When the —105-volts, no-signal level is present on the cathode follower grids, tubes V3 and V4 are cut off. The output voltage at the junction of R28 and cathode resistors R21, R22, R23, and R24, under no signal conditions, is —45 volts. When the +10-volt input is present at the cathode follower grid, it produces a +10-volt output at the cathode because of the bias developed at the junction of R28 and the cathode of tubes V3 and V4. Crystals CR6

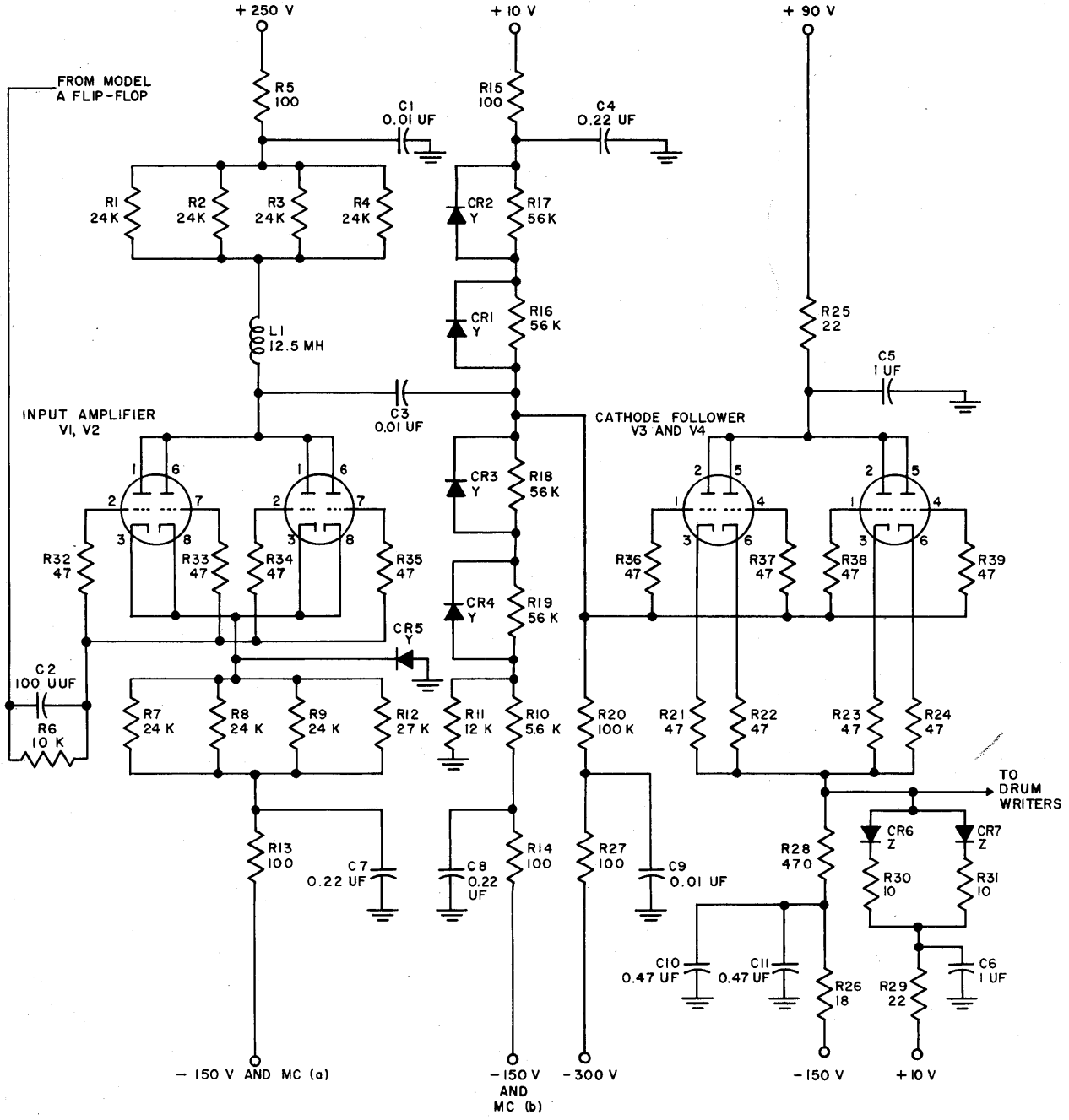


Figure 4–11. Model A Drum Write Driver, Schematic Diagram

and CR7 in the output circuit provide additional clamping of the +10-volt level. The positive pulse output shown in *B* of figure 4–13 is used to drive the drum writers. Figure 4–13, part *C*, shows two complete output pulses of the drum write driver.

The RC networks of resistor R29 and capacitor C6, resistor R26 and capacitor C10 and C11 and resistor R25 and capacitor C5 form decoupling networks for the power supply voltages. The 47-ohm resistors in the grid and cathode circuits suppress parasitic oscillations. (See fig. 4–11.)

When the flip-flop driving the drum write driver has been cleared, a positive level is present at the input amplifier and the cathode follower is cut off. An a-c coupling which reacts only to a change in the input signal is employed between the input amplifier and the cathode follower, in order to keep the cathode follower cut off until the next write pulse sets the drum read driver flip-flop.

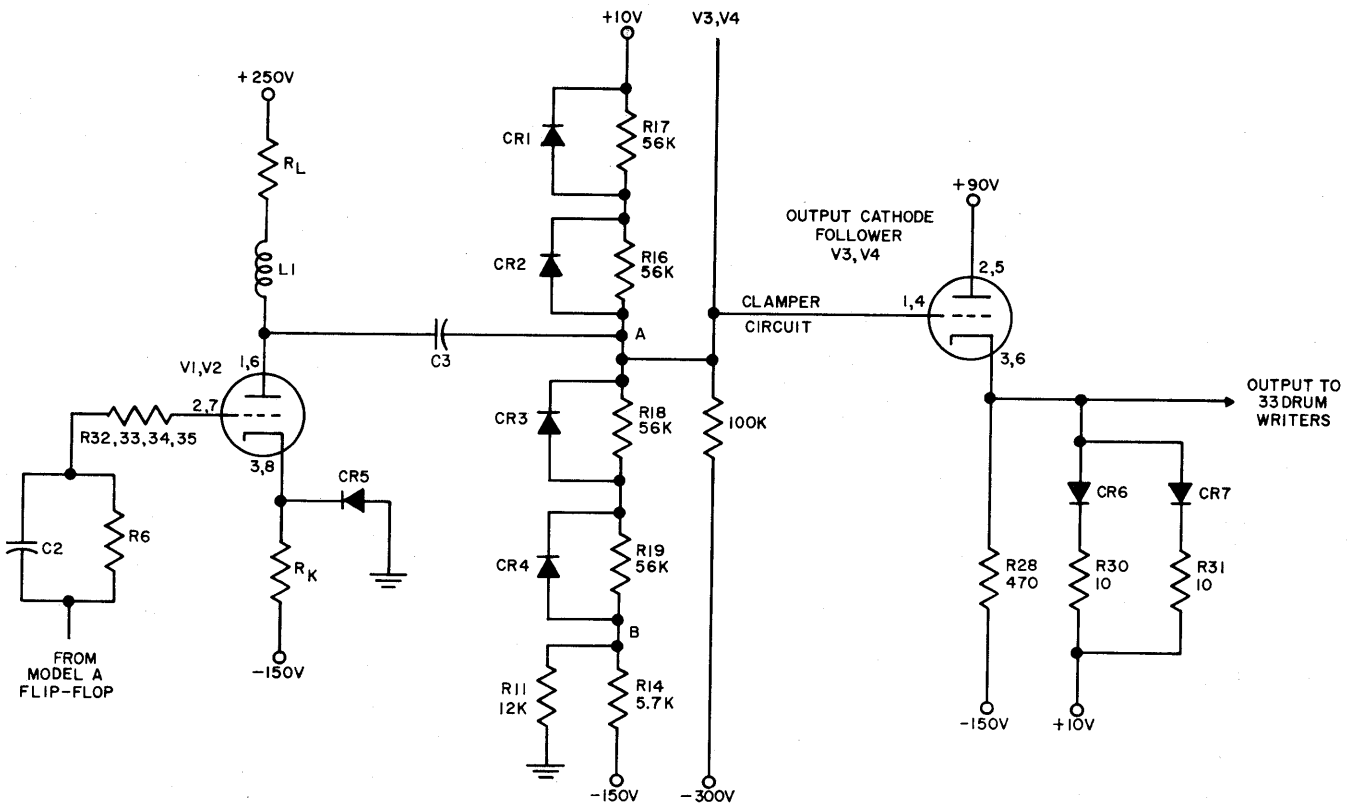


Figure 4–12. Drum Write Driver, Simplified Schematic Diagram

3.3 MODEL B DRUM WRITE DRIVER, CIRCUIT ANALYSIS

A partial schematic diagram illustrating the cathode follower circuit used with a model B drum write driver is presented in figure 4–14.

The input to a model B drum write driver is the —30-volt-square-wave pulse that is generated on the 0 side of a model A flip-flop when the flip-flop is set for 1.7 usec. Model B drum write driver circuits differ from the circuits of model A drum write drivers only in the cathode follower circuitry. The circuit analysis for model B drum write drivers is essentially the same, with the reservations noted above, as the circuit analysis of model A drum write drivers.

Load simulation is required in applications where fewer drum writers are to be driven by the drum write driver than are normally driven. Load simulation provides the necessary resistive output loading for the drum write drivers. The networks that provide model B drum write driver load simulation are shown in figure 4–15.

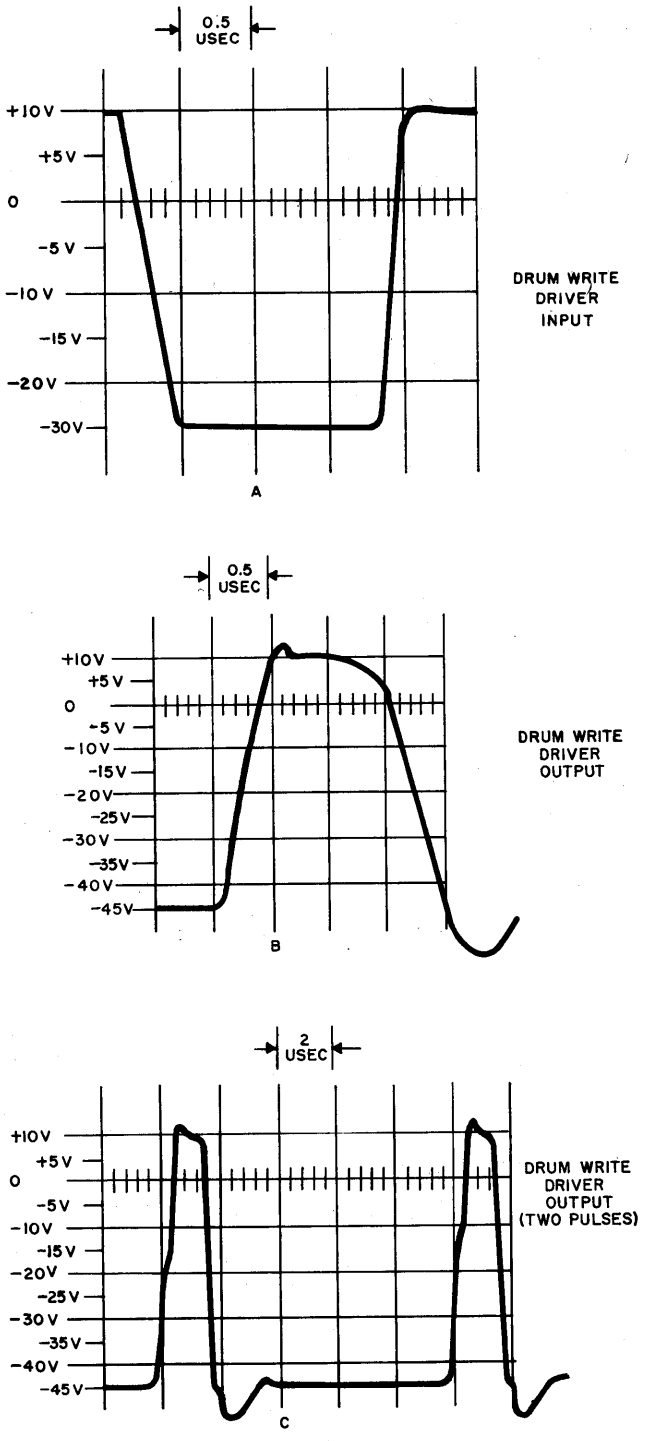


Figure 4–13. Model A Drum Write Driver, Input and Output Waveforms

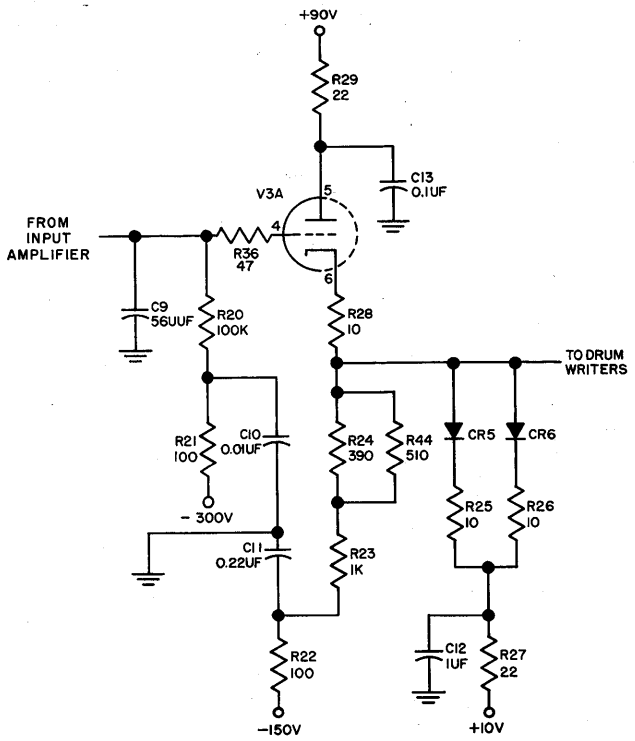


Figure 4–14. Cathode Follower Circuits for Model B Drum Write Drivers, Schematic Diagram

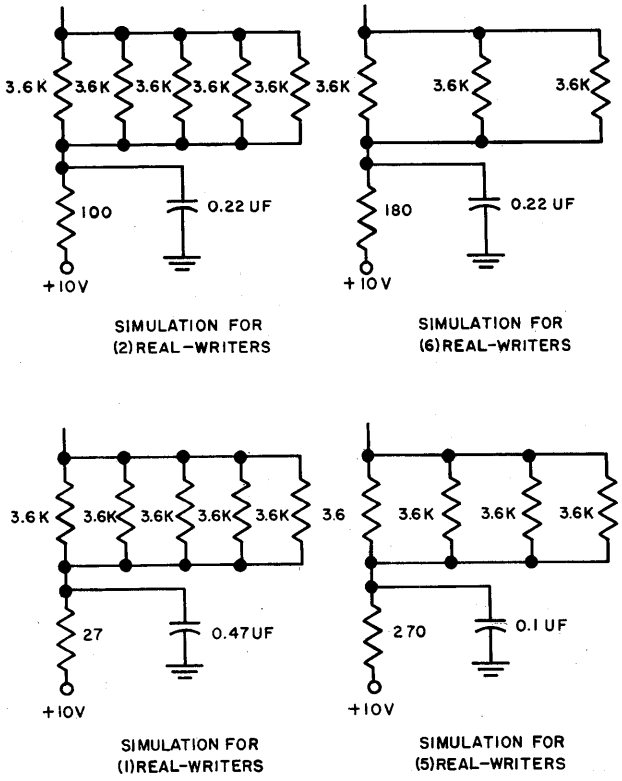


Figure 4–15. Model B Drum Write Driver Simulation, Schematic Diagram

CHAPTER 4
DRUM WRITER

The purpose of the drum writer is to provide write pulses to its associated drum head. The Drum System uses two models, A and B. The operational difference between the two models is that the model A drum writer (conditioned by a model-A-drum-write-driver-output pulse) operates a drum head through a diode switch network, whereas, the model B drum writer (conditioned by a model-B-drum-write-driver-output pulse) operates a drum head directly. The following discussion describes both models.

4.1 DRUM WRITER, BLOCK DIAGRAM ANALYSIS

Figure 4–16 is a block diagram of a drum writer. The input to the drum writer, applied at input amplifier stage V1A and V2B, is a 1- or 0-state d-c level from the output of an associated flip-flop in the write register. If the write register flip-flop is set, a positive voltage appears at the input to the V1B stage and negative voltage appears at the input of the V1A stage. If the write register flip-flop is cleared, the positive voltage appears at the input to the V1A stage, and the negative voltage appears at the input to the V1B stage. The input amplifier stage receiving the positive input conducts, and the other input amplifier is cut off. The output of the nonconducting input amplifier stage produces conduction in the associated output amplifier stage (tube V2A or tube V2B) when combined with a positive input from the drum write driver. Conduction in one of the output amplifier stages produces current flow through the write head coil connected to the drum writer. The direction of current flow is determined by the output amplifier stage that conducts. If stage V2A conducts, the direction of current flow through the coil produces a flux polarity that represents binary 1. If stage V2B conducts, the direction of current flow through the coil produces a flux polarity that represents binary 0.

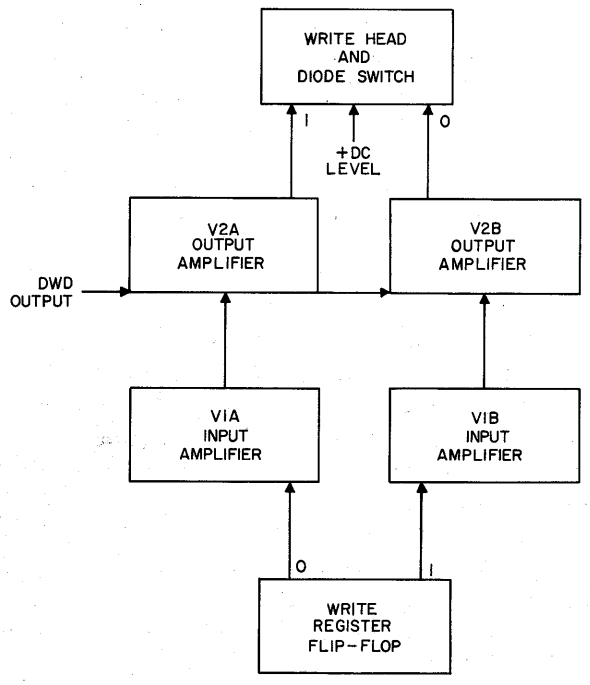
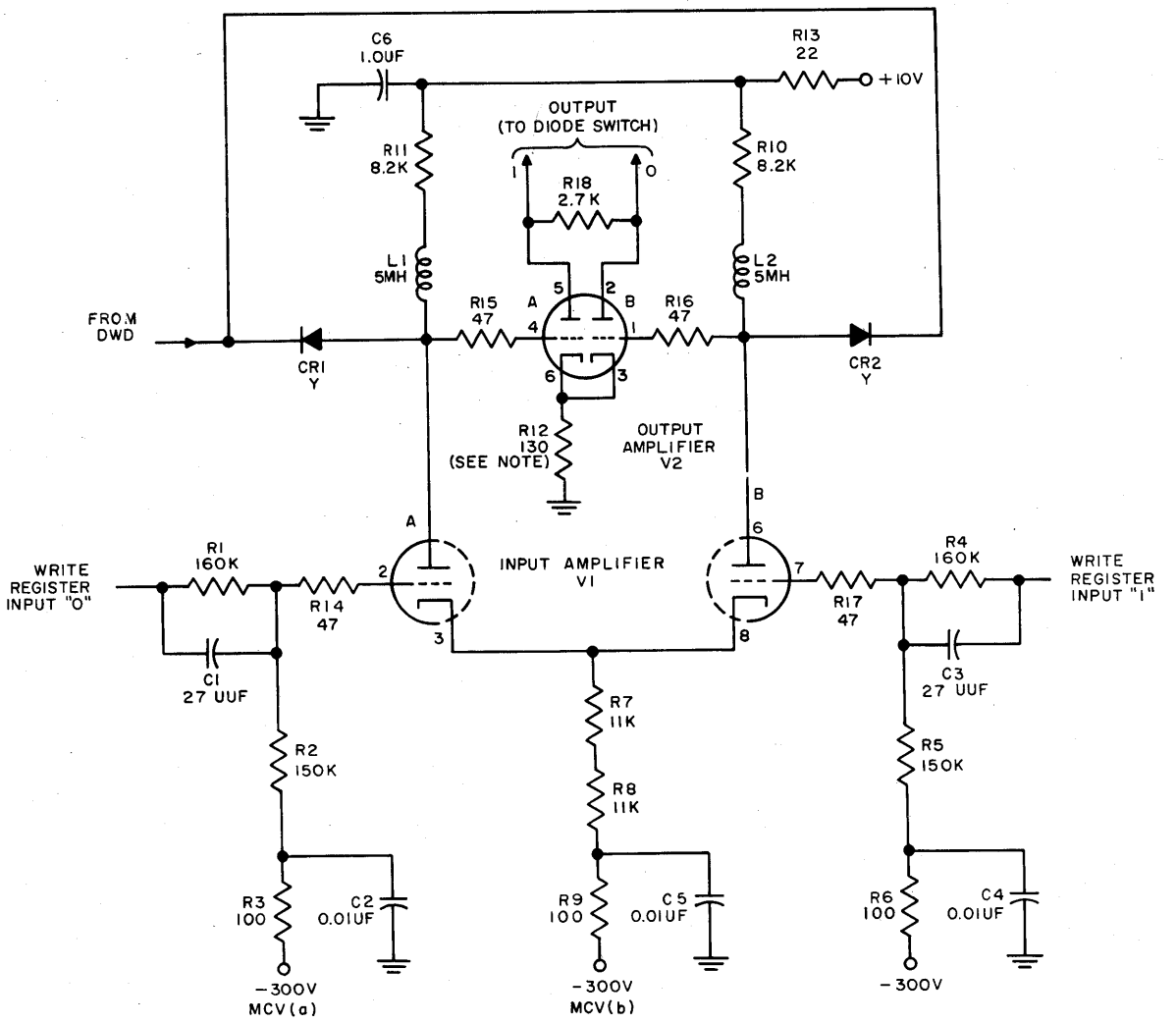


Figure 4–16. Drum Writer, Block Diagram

4.2 DRUM WRITER, CIRCUIT ANALYSIS

Stage V1B is connected to the 1 side of a write register flip-flop, and stage V1A is connected to the 0 side of the flip-flop. (See fig. 4–17.) The RC networks consisting of resistor R1 and capacitor C1, and resistor R4 and capacitor C3 in V1's grid circuits isolate the drum writer from the flip-flop. Inductors L1 and L2 peak the leading edge of voltage in the plate circuit. If the flip-flop is set, V1B has a +10-volt level at its control grid and V1A has a −30-volt level at its control grid. Consequently, the plate voltage of V1B decreases and the plate voltage of V1A increases. The plate voltage drop at the plate of V1B develops a large negative voltage at the control grid of tubes V2B, and V2B is cut off. The simultaneous plate voltage rise at the V1A plate places a positive voltage at the control grid of V2A. This positive voltage is sufficient to produce conduction in V2A when the input signal from the drum write driver goes positive. However, until the time at which the drum write driver receives a write pulse input, its output is −45 volts. This negative voltage appears at the cathodes of crystals CR1 and CR2. Current now flows through crystal CR1 because of the positive voltage present on the plate of V1A. In the conducting state, crystal CR1 is effectively a short circuit, and practically all of the −45 volts from the drum write driver is applied to the control grid of V2A. The algebraic sum of the voltages present on the grid of V2A is negative; in this condition the tube is cut off.

When the write pulse is received, the drum write driver produces a pulse of +10-volt magnitude. The positive voltage present at the cathode of CR1 now prevents conduction through the crystal and +10 volts is applied to the control grid of V2A during the duration of the



NOTE

RESISTOR R12 IN THE MODEL A DRUM WRITER IS 130 OHMS. IN THE MODEL B DRUM WRITER RESISTOR R12 IS 180 OHMS.

Figure 4–17. Model A Drum Writer, Schematic Diagram

drum write positive output. This +10-volt pulse is sufficient to cause heavy conduction in V2A. Output amplifier stage V2B cannot conduct because of the negative voltage placed at its control grid by the voltage drop in the plate circuit of V1B.

The heavy conduction of V2A saturates the write head coil in the plate circuit of the tube. The current pulse through the coil places a flux on the drum in a direction which indicates that binary 1 is written on the drum.

When the write register flip-flop is cleared, +10 volts are applied to tube section V1A. Consequently, when the drum write driver output goes positive, output amplifier V2B develops a current pulse that drives the write head. The heavy conduction in V2B saturates the write head coil in the plate circuit of the tube. The current pulse through the write coil places a flux pattern on the drum in a direction which indicates that binary 0 has been written. Sharp rises and decays of voltages applied to the write heads may shock the head winding into oscillation; resistor R18 damps these oscillations. The RC networks composed of resistor R9 and capacitor C5, resistor R3 and capacitor C2, resistor R13 and capacitor C6, and resistor R6 and capacitor C4 are decoupling networks for the drum writer power supply voltages.

Model A and model B drum writers are essentially the same, differing primarily in their useage. The model A drum writer is used in write circuits which are switched

from field to field. The model B drum writer is used on the OD side of the drum when field switching is not required. The model A drum writer input is a 1.8-usec pulse. The model B drum writer input is a 1.7-usec pulse. The 1.7- or 1.8-usec pulses are applied to realize an effective 1.5-usec pulse of current in the drum head. The line capacity and head inductance delay the effective minimum write current level of 35 ma for 0.2 or 0.3 usec.

This accounts for the 1.7- or 1.8-usec pulse length used to produce a 1.5-usec write pulse at the head. Model A drum writers receive their plate voltage (125 volts) from a drum field driver that has been selected by field selection circuits. This plate voltage is applied via the center taps of the write magnetic heads. A +150-volt line connected to the center taps of the write heads supplies plate voltage for the model B drum writer. The difference in pulse widths of drum write driver outputs compensates for the difference in plate voltages used for model A and model B drum writers. Therefore, the average current amplitude of pulses applied to the write heads is essentially the same for both models of drum writers. The cathode resistors provide additional compensation for plate voltages differences by developing different bias levels. Model A drum write cathode resistor R12 is 130 ohms; model B drum write cathode resistor R12 is 180 ohms. Resistor R12 is the only component that changes from a model A drum writer to a model B drum writer. The output current pulses for both model A and model B drum writers are shown in figure 4–18.

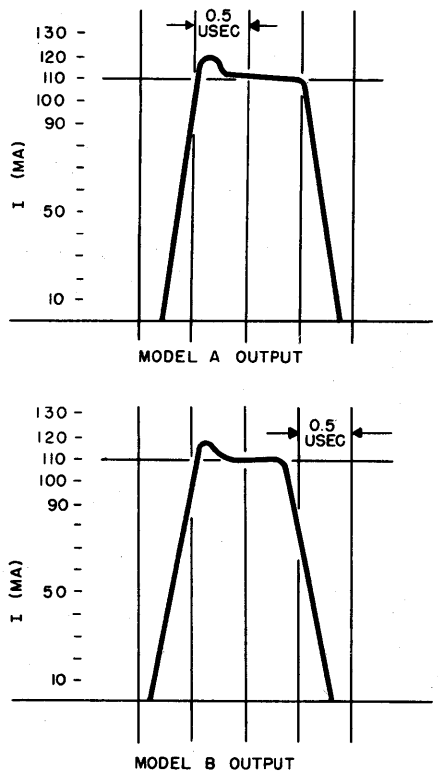


Figure 4–18. Models A and B Drum Writer Output Waveforms

CHAPTER 5
DRUM READ DRIVER

The drum read driver isolates the drum read heads from the drum read amplifiers when writing operations are performed by providing a d-c blocking voltage across the read diodes. The drum read driver connects the drum read heads to the drum read amplifiers during reading by providing a closed path, through the read diodes, for the incoming information. Controlled switching by the drum read driver from writing to reading operations prevents blocking of the drum read amplifiers. The drum read driver drives 33 drum read amplifiers.

5.1 DRUM READ DRIVER, BLOCK DIAGRAM ANALYSIS

Figure 4–19 is a block diagram of the drum read driver. The input to the inverter stage is a 0- or 1-state level from a flip-flop. When writing operations are performed, the flip-flop is cleared and a negative output level is applied to the inverter stage V1A, which provides amplification and inversion of the d-c level. A positive output of the inverter stage is sent to the cathode follower stage V1B, which acts as a buffer stage to isolate input V1A from output V2. The positive level from V1B is applied to output cathode follower V2 which in turn also produces a positive output. This cuts off the switching diodes connected to the read heads and isolates the drum read heads from the drum read amplifiers during writing operations. When reading operations are performed, the flip-flop at the input of the drum read driver is set. The positive-input level to V1A produces a negative level from the inverter. The negative-output level is fed through V1B to output cathode follower V2. The negative input level to V2 decreases the output level of V2. The switching diodes connected to the drum read heads conduct, permitting transmission of information from the drum read heads to their respective drum read amplifiers.

5.2 DRUM READ DRIVER, CIRCUIT ANALYSIS

The schematic diagram of a drum read driver is shown in figure 4–20. A model C flip-flop at the input of the drum read driver is cleared when drum writing is performed. This applies a −30-volt level to the control grid of V1A. (See fig. 4–21, part A.) Resistor R1 provides grid limiting and isolates the input of V1A from the flip-flop. Tube V1A functions as an overdriven amplifier. Therefore, the −30-volt input cuts off V1A, and plate voltage rises to equal the plate supply voltage. The output of V1A is d-c coupled to the control grid of isolating cathode follower V1B. The positive output of V1B is applied to the parallel-connected control grids of output cathode followers V2, V3, and V4. The output of the cathode followers is a +150-volt level. (See fig. 4–21, part A.) This +150-volt level is applied to the cathodes of switching diodes connected between the drum read amplifiers and drum write circuit. Since the cathodes are positive with respect to the plates (diode plate potentials are +125-volts which are supplied by the drum field drivers), the diodes appear as an open circuit. This presents a high-impedance input to the drum read amplifier, thus isolating the drum read amplifiers from the write circuit during writing operations. The flip-flop, at the input of the drum read driver, is set at a +10-volt level when reading is performed. This voltage is then sent to

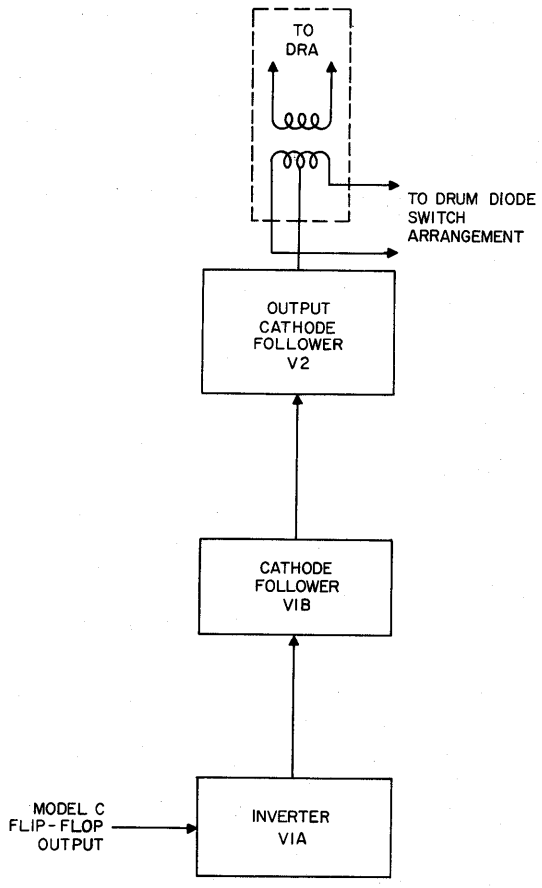


Figure 4–19. Drum Read Driver, Block Diagram

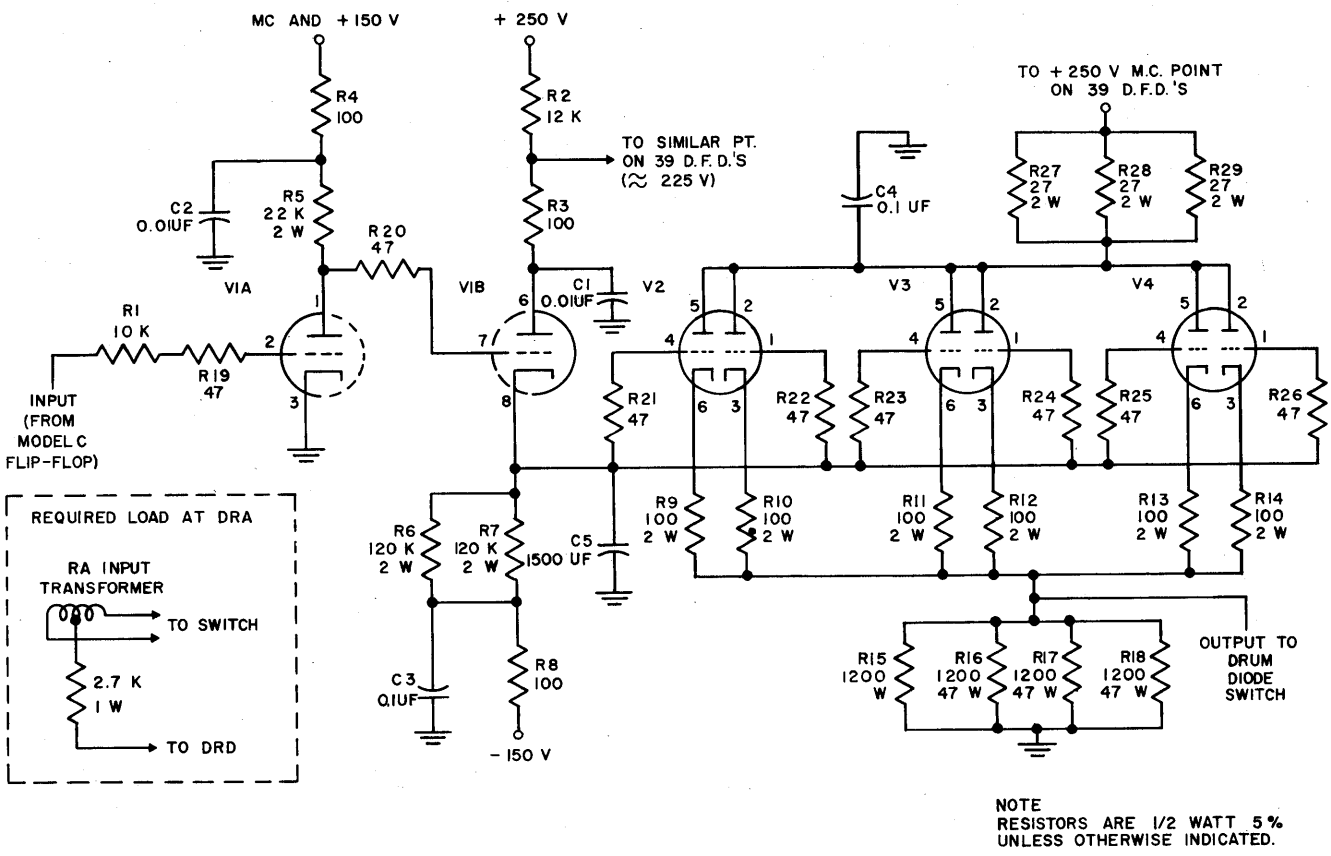


Figure 4–20. Drum Read Driver, Schematic Diagram

the inverter tube V1A. The +10-volt input level on the control grid of V1A (fig. 4–21, part B) causes the plate voltage of V1A to drop. The output of V1A is at a negative level and is coupled through V1B to V2, V3, and V4. The negative input to the control grids of V2, V3, and V4 produces a +100-volt level output.

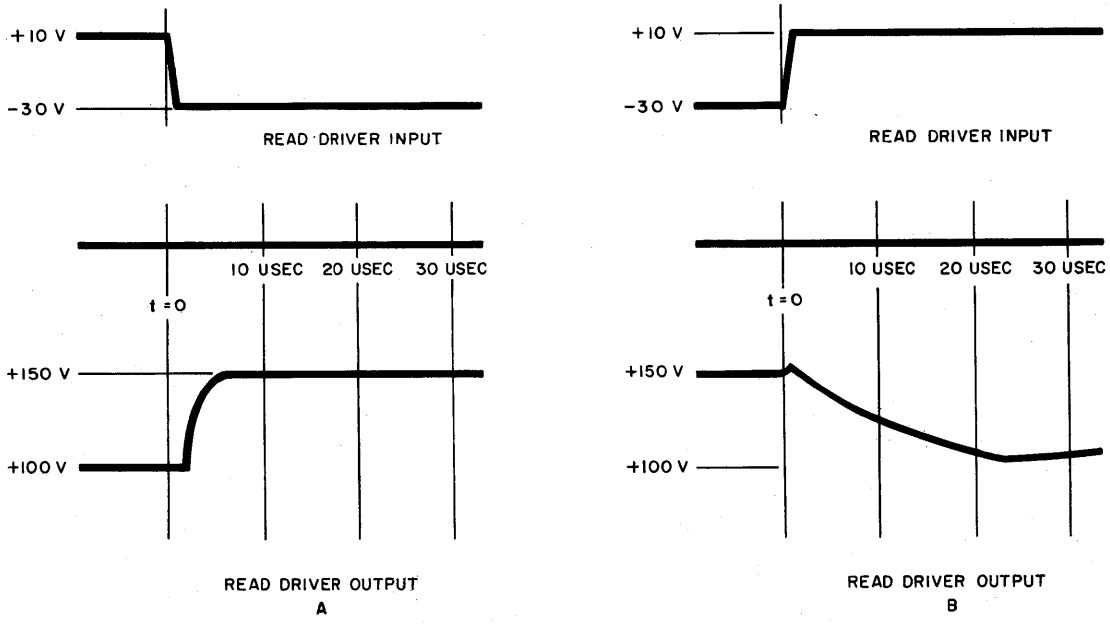


Figure 4–21. Drum Read Driver Read-Write Operation Waveforms

If the output of the drum read driver is allowed to drop suddenly when switching from writing operations to reading operations, transients develop and block the read amplifiers. If this blocking lasts more than the 120 usec, provided for switching by the drum read write controls, then the blocking voltages will override the drum read head signals. Capacitor C5 in the grid circuit of V2 prevents blocking of the drum read amplifiers by producing a relatively slow fall-time of 20 microseconds. (See fig. 4–21, part B.) The discharge path of C5 through parallel resistors R6 and R7 provides the necessary RC time constant to produce this 20-usec fall-time.

The RC networks of resistor R4 and capacitor C2, resistor R3 and capacitor C1, resistor R8 and capacitor C3, and resistors R27, R28, and R29 and capacitor C4 form decoupling networks for the supply voltages. The 47-ohm resistors in the control grid circuits suppress parasitic oscillations.

CHAPTER 6
DRUM READ AMPLIFIER

Drum read amplifiers are used in the reading of information stored on a magnetic drum. One drum read amplifier is associated with each channel of information bits. Information bits are represented by magnetized areas on the drum surface. When magnetized areas on a drum surface pass under drum read heads, the changing fields of magnetic flux induce voltages in the drum read head windings. These voltages form the input signals to the drum read amplifier. The input signal from one read head is converted by a drum read amplifier into a d-c level that conditions a gate at the output of the drum read amplifier. When magnetized areas on a drum surface represent 1 bits, drum read amplifier outputs condition the gate to pass a standard pulse. When magnetized areas represent 0 bits, drum read amplifier outputs cut off the gate.

6.1 DRUM READ AMPLIFIER, BLOCK DIAGRAM ANALYSIS

The drum read amplifier is a transformer input, 5-stage circuit. (See fig. 4–22.) The input transformer has a flat frequency response for a variable range of input information frequencies. The transformer, together with amplifier stage V1A, forms a high gain input stage. Cathode follower stage V2A provides isolation and impedance-matching between amplifier stage V1A and differentiator stage V3A. Differentiator stage V3A has maximum outputs at the zero crossing of input signals. Amplifier-limiter V4A amplifies and shapes the differentiator output into a square wave which is fed to output cathode follower stage V5A. The output of the drum read amplifier is positive (+10 volts) at read-sample time when a 1 bit is being read. The output is negative (—30 volts) at read-sample time when a 0 bit is being read. The positive output is of sufficient magnitude to condition the passing of a standard pulse by a gate.

6.2 DRUM READ AMPLIFIER, CIRCUIT ANALYSIS

6.2.1 Input Transformer TI

A schematic diagram of the drum read amplifier is shown in figure 4–23. The input circuit of the read amplifier is a transformer with a center-tapped primary. The primary winding of the transformer (terminals 3 and 5) is connected to the terminals of an associated drum read head. A positive voltage (+100 or +150) for diode switching is applied to the center tap (terminal 4) of the primary winding. The signal amplitude of either all 1's or all 0's is the same at the transformer. The read circuit differentiates between 1's and 0's at the gate whose suppressor grid is conditioned by the drum read amplifier. When consecutive information bits are all 1's or all 0's, the information repetition frequency is 100 kilocycles (kc). When consecutive bits are alternate 1's and 0's, the transformer input signal has a 50-kc fundamental repetition frequency with a 150-kc third-harmonic component. Since the amplitude and frequency of the input signal vary greatly, the input transformer is designed to have flat gain and minimum phase shift over the repetition frequency region of the input signal. There is a 1:5 gain in signal amplitude through the transformer.

Transient voltages are introduced at the input to the drum read amplifier by switching between drum fields or by a switch of operations. There is a +70-volt d-c level at the center tap of the magnetic heads when the drum read circuit is not reading. When a reading operation is to be performed, the d-c voltage at the center of the drum read head is raised to +130 volts. This positive-going voltage induces a negative voltage at the grid of amplifier V1A, and cuts it off. The read amplifier recovers from these transient effects in less than 100 usec.

6.2.2 Amplifier Stage V1A

Amplifier stage V1A uses a triode with low input capacitance to prevent large amounts of phase shift and

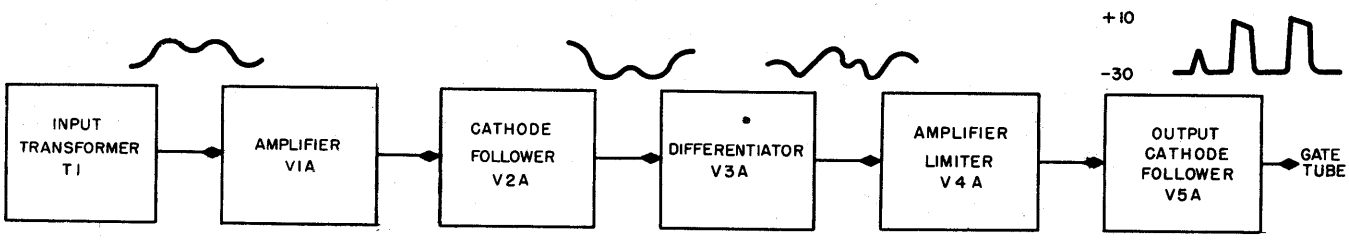


Figure 4–22. Read Amplifier, Block Diagram

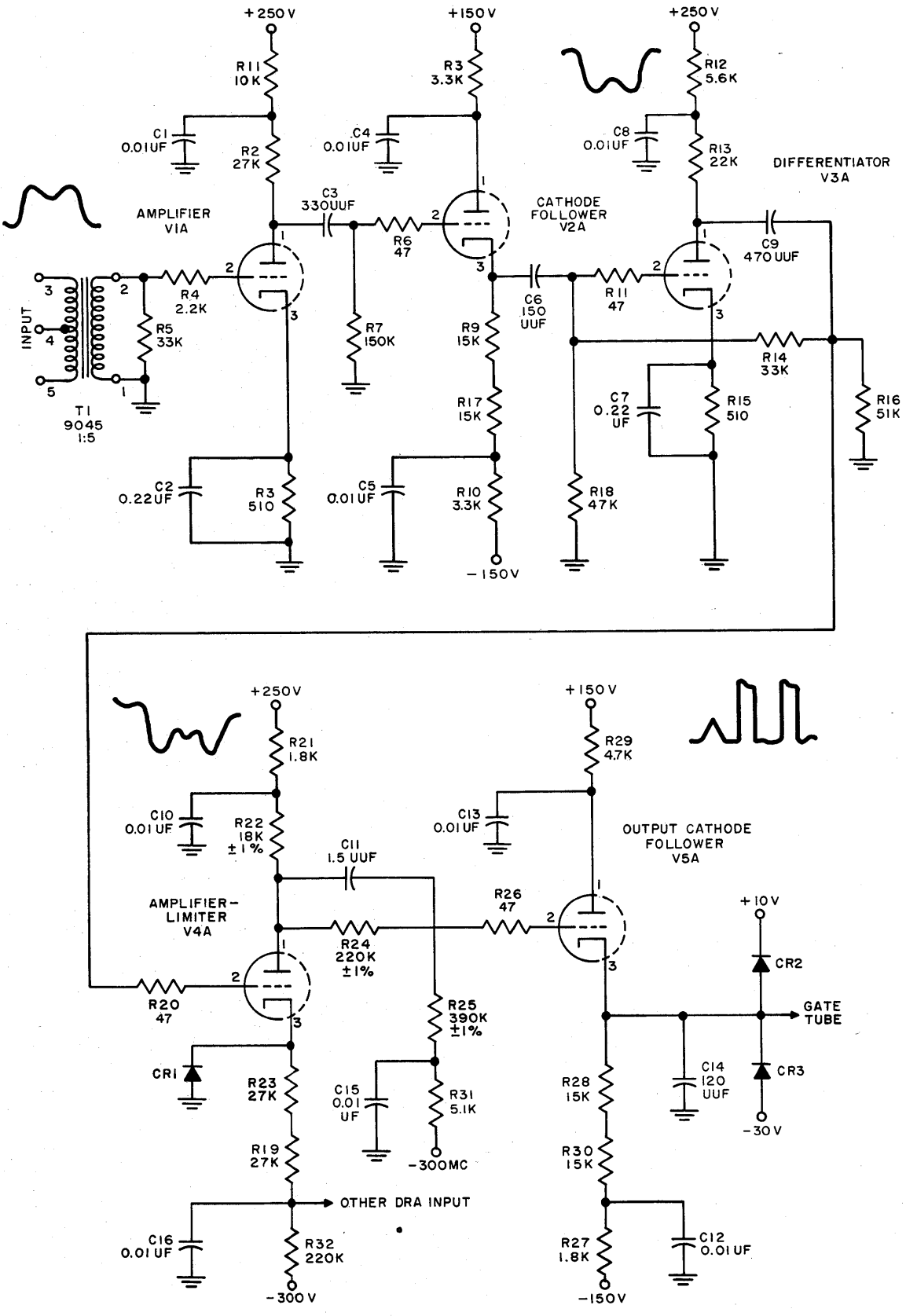


Figure 4–23. Read Amplifier, Schematic Diagram

phase distortion. The small input capacitance of the tube, together with other input stage considerations, forms an optimum load for the secondary of the transformer. This load causes only a 0.1-usec phase shift of the zero crossing of input signals in the transformer. Resistor R4 provides grid limiting which prevents overdriving the input stage when input signal voltages exceed 300 millivolts (mv), peak-to-peak. Resistor R4 also acts as a parasitic suppressor.

6.2.3 Cathode Follower Stage V2A

Cathode follower stage V2A is used as a buffer amplifier between the input stage and the differentiator. It isolates the output of V1A from the input of the differentiator stage V3A. Thus, V2A is a high-impedance load for V1A, and a low-impedance source for V3A. Cathode resistors R9 and R17 have resistances that are large enough so that very little amplitude distortion takes place with maximum signal input to the cathode follower V2A.

6.2.4 Differentiator Stage V3A

Voltages generated in the drum head coils by the varying fields of magnetic flux on the drum surface, form the input signals of the drum-read amplifier. Since the rate of change of flux is zero at the peak of the magnetized areas representing bits (fig. 4–24, part A) the voltage induced in the drum read head coils at the flux peak is zero. (See fig. 4–24, part B.) In order to obtain correct timing for drum-read-amplifier-output pulses, the differentiator which has maximum output at the zero crossing of the input signal is incorporated in the drum read amplifier. (See fig. 4–25.) Differentiator inputs are amplified and fed from the plate back to the grid through a feedback network composed of capacitor C9 and resistors R14 and R18. This feedback voltage effectively reduces the input resistance (equivalent R_g) of V3A. (See fig. 4–25.) The time constant of capacitor C6 and the equivalent input resistance is approximately 1/10th the period of the input frequency. Thus, the feedback network causes differentiation of input voltages. If input bits are all 1's or all 0's, the input is a sine wave. Differentiation of a sine wave results in a 90-degree phase shift.

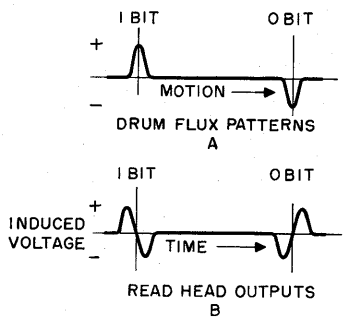


Figure 4–24. Flux Pattern on Drum Surface and Resulting Induced Voltages in Read Head Coil

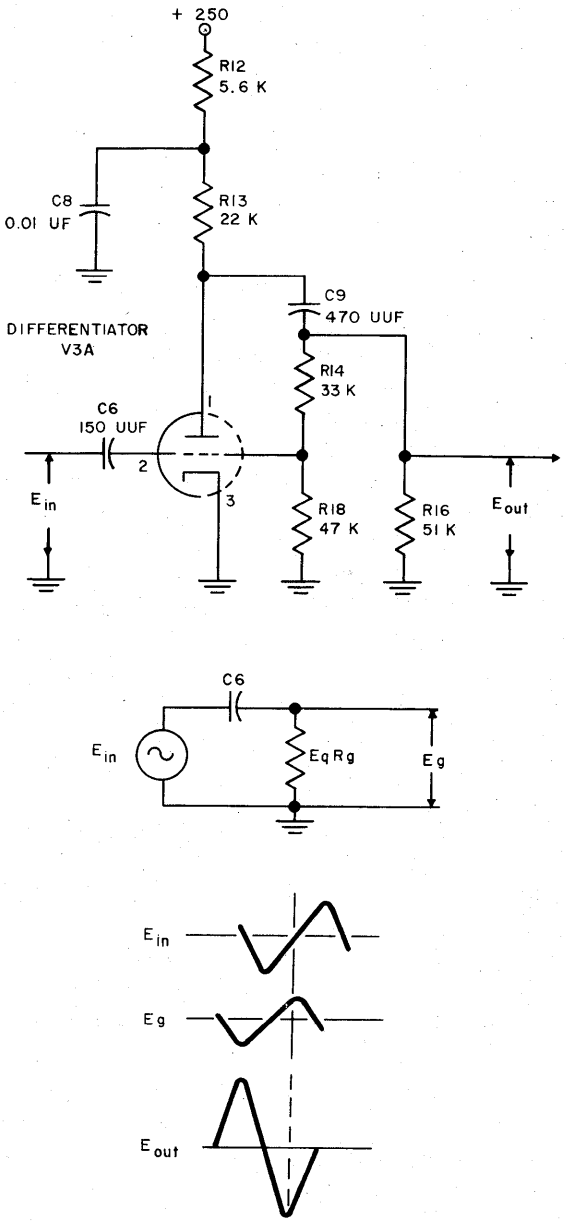


Figure 4–25. Read Amplifier Differentiator Stage, Simplified Schematic Diagram and Waveforms

When information bits are composed of alternate 1's and 0's, the input is a complex waveform made up of a sine wave with a fundamental frequency of 50 kc and a third harmonic sine wave of 150 kc. The sine wave components of the complex wave also are shifted in phase by approximately 90 degrees. Shifting input voltages 90 degrees produces maximum outputs when drum read amplifier input voltages are crossing zero.

6.2.5 Amplifier Limiter Stage V4A

Amplifier limiter stage V4A forms the drum read amplifier output waveshape. Tube V4A is an overdriven amplifier that operates in the following manner. Positive

driving voltages at the grid saturate the tube, limiting the positive portion of input signals. When grid driving voltage goes negative, cathode voltage tends to decrease. However, the cathode is clamped at ground by crystal CR1. Grid voltage continues to go negative, and the tube is cut off. Plate voltage rises, and the tube output is a positive square wave. The square wave is applied to the output cathode follower.

6.2.6 Output Cathode Follower Stage V5A

Output cathode follower stage V5A forms standard +10- and −30-volt conditioning levels at its output. With no input to the drum read amplifier, the voltage at the grid of V5A is set at −36 volts by the grid voltage divider consisting of resistors R24, R25, and R31. Resistor R24 and capacitor C11 are a high-frequency compensation network that maintains a fast rise-time in the leading edge of the limiter output. The output of V5A is −30 volts as a result of clamping by crystal CR3.

With a 1-bit input to the drum read amplifier (50 to 300 mv), the input to V5A is large enough to cause the cathode voltage to rise to +10 volts. The cathode voltage tends to go higher, but is clamped at the +10-volt level by crystal CR2. The +10-volt level enables the gate at the drum read amplifier output to pass a standard pulse. The output of V5A rises to +10 volts when the input voltage at tube V4A reaches approximately −4.5 volts. This rise ensures gating of the standard pulse.

When the bit at the input to the read amplifier is a 1, the rising cathode voltage at V5A causes capacitor C14 to charge. Capacitor C14 aids gate conduction by helping to supply current required during pulse time. When the gate conducts, its suppressor grid draws current and tends to drop the voltage output of V5A. However, capacitor C14 in the cathode circuit continually charges to the +10-volt level, substituting for some of the current drawn by the suppressor grid. This prevents the drum read amplifier output voltage from dropping more than 3 volts during pulse time.

Figure 4–26 shows ideal waveforms, peak-to-peak voltages, and time relationships of information bits in the read amplifier.

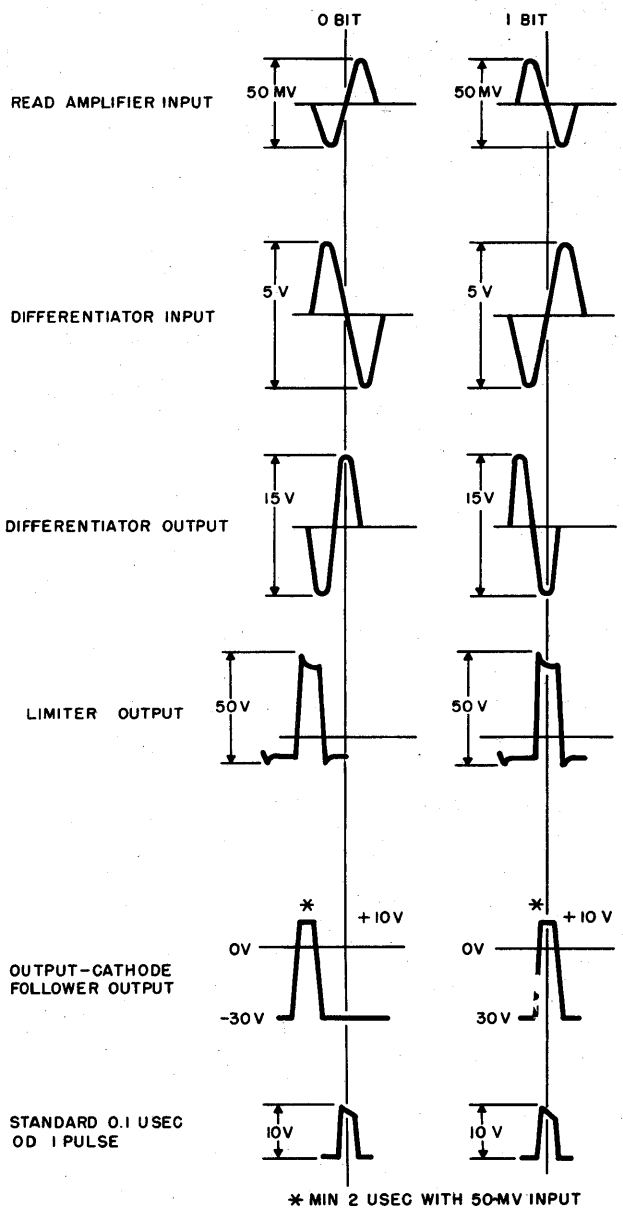


Figure 4–26. Read Amplifier Ideal Waveforms and Time Relationships

CHAPTER 7
DRUM FIELD DRIVER

The drum field driver amplifies field selection circuit outputs to voltage levels that either cut off drum heads in the associated field or allow those heads to conduct during CD reading or writing operations. One drum field driver is capable of driving the write circuits of one complete field. These circuits include 33 drum heads and 33 drum writers.

7.1 DRUM FIELD DRIVER, BLOCK DIAGRAM ANALYSIS

The drum field driver is composed of three stages: an amplifier, cathode follower, and output cathode follower stage. (See fig. 4–27.) The amplifier V1A stage receives either a +10- or a −30-volt level from the field selection circuits. It amplifies the input level received and produces a positive level whose amplitude is dependent upon the input level. This output is fed to the cathode follower stage V1B. The cathode follower is employed primarily as a shaping stage. It produces a relatively fast rise time or slow fall time (see fig. 4–27) in the waveshape sent to the output cathode follower stages V2 to V7 inclusive.

The output cathode follower stages develop the select-field or nonselect-field level which is sent to the center taps of the magnetic drum heads in the field connected to the drum field driver. In addition, the select-field level is utilized as plate voltage by each of the drum writers in the selected field.

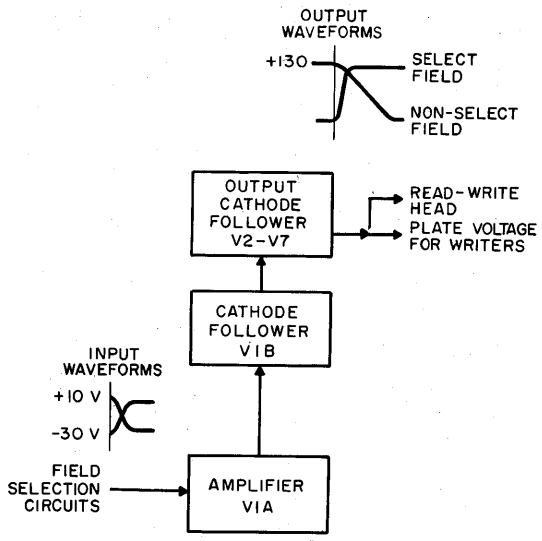


Figure 4–27. Drum Field Driver, Block Diagram

7.2 DRUM FIELD DRIVER, CIRCUIT ANALYSIS

7.2.1 Amplifier Stage V1A

The schematic diagram of the drum field driver is shown in figure 4–28. An input level of +10 volts or −30 volts from the output of the field selection circuit is applied to the cathode of amplifier V1A across resistor R6. Stage V1A conducts. A +10-volt input results in a positive d-c level at the plate of the tube. (An increase of voltage at the cathode increases tube bias and decreases plate current, resulting in a voltage rise at the plate.) A −30-volt input also produces a positive d-c level, but of a smaller amplitude. Resistors R1 and R2 form a voltage divider for the grid. Resistor-capacitor networks consisting of R5 and C3 and R4 and C2 are decoupling filters. Resistor R2 serves both as part of the grid-biasing voltage divider and as a decoupling filter in conjunction with capacitor C1.

7.2.2 Cathode Follower Stage V1B

Cathode follower V1B couples the output of the power amplifier to the output cathode follower stage. (See fig. 4–29.) The input to the cathode follower has a high-frequency compensation network that keeps a fast rise time in the leading edge of the input waveshape. This network is composed of resistor R8 and capacitor C4. A fast rise time and a relatively slow fall time in the output waveshape of the drum field driver are formed in this stage. This ensures slow application of back voltage to the field switching diodes and a minimum of blocking in the drum read amplifier circuit. The period of the fall time is approximately eight times longer than the period of the rise time; this is due to the different time constants of the charge and discharge paths of capacitor C8. With a +10-volt input to the drum field driver, a positive d-c level is applied to the grid of V1B. The resulting rise of cathode voltage causes capacitor C8 to charge through the path indicated on the figure 4–29. Capacitor C8 remains charged until the field selection circuits switch to another field. When the field selection changes, the input to the drum field driver drops to −30 volts. The cathode of V1B becomes less positive, causing capacitor C8 to discharge through resistors R14 and R15.

The plates of the cathode follower stages in all 39 drum field drivers and the drum read drivers are connected to a common decoupling network. (See fig. 4–28.)

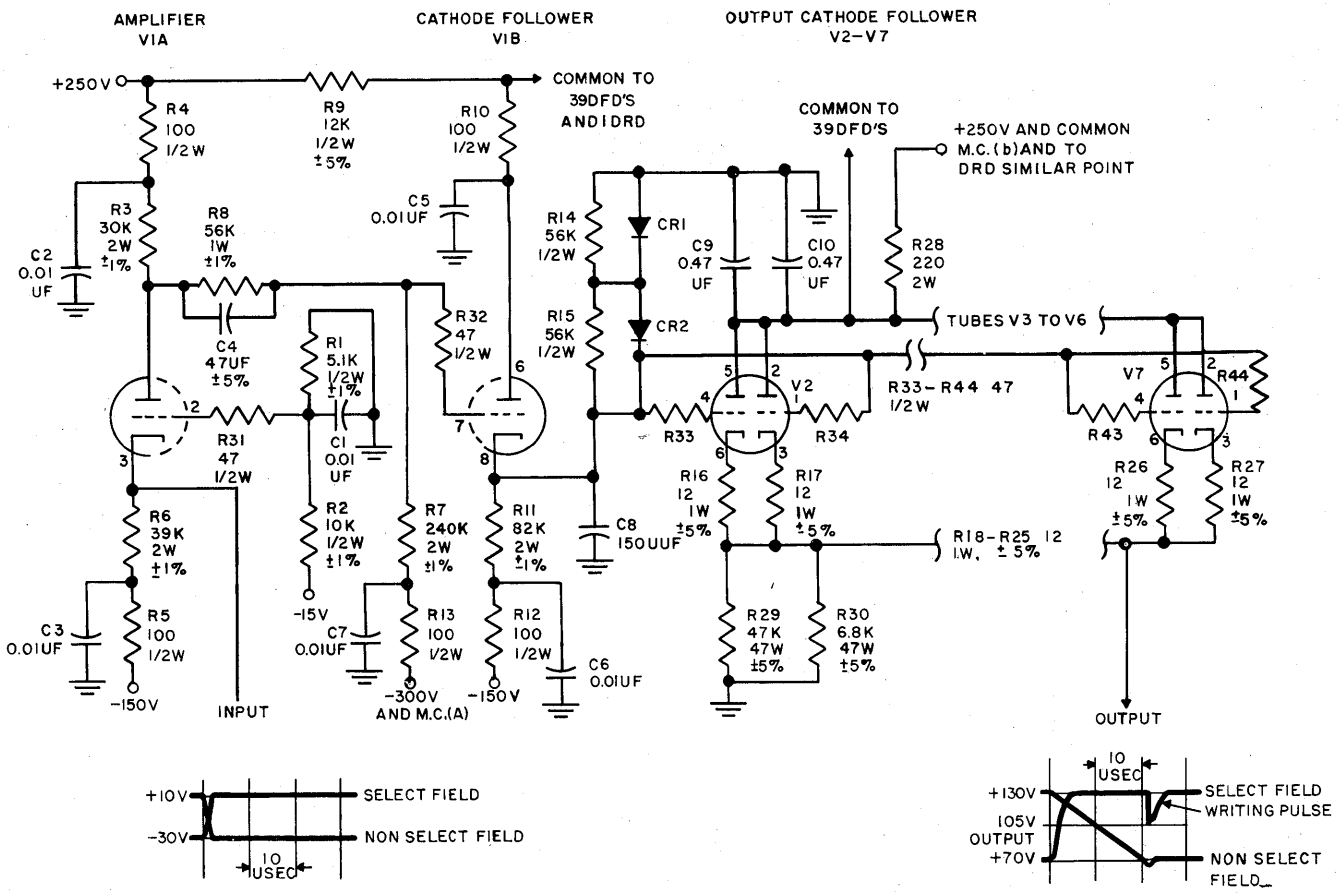


Figure 4–28. Drum Field Driver, Schematic Diagram

7.2.3 Output Cathode Follower Stage V2-V8

The output cathode follower stage is composed of six duotriodes in parallel so that approximately 4 amperes of writing current can be developed. (See fig. 4–29.) The output of the drum field driver is taken from the cathode of this stage, and goes to the center tap of the drum heads in the associated field.

Crystals CR1 and CR2 are used to clamp the grid voltages of the output cathode follower at ground. This prevents high back voltages produced by failures in the

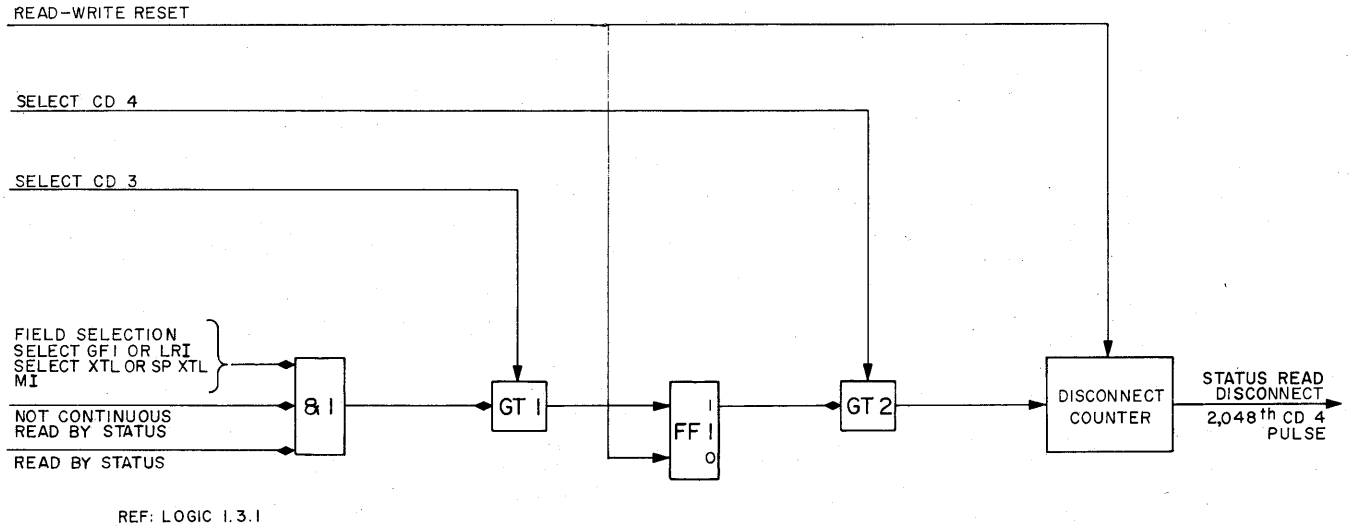


Figure 4–29. Drum Field Driver, Simplified Schematic Diagram

stage preceding the output cathode follower from overdriving the field switching diodes in the selected field. The need to decouple the plate supply is due to the large current pulse drain of the drum field drivers during writing. To decouple these circuits a very small resistor and a very large capacitor must be used due to the 4-amp current drain. Available physical mounting space dictates that the capacitor be composed of a number of small capacitors in parallel. The most expedient way of connecting the capacitors together is the manner indicated in the circuit schematic. The plate supply for all 39 drum field drivers and the drum read driver is common. If each of these circuits were decoupled separately, the failure of one would damage diodes in the switching matrix. Resistors R14 and R15 effectively equalize the back resistances of crystals CR1 and CR2.

There is a 20-volt dip in the select-field level during the period of the write pulse produced when writing. This dip is due to additional loading when the drum writers draw current.

CHAPTER 8

MODEL G POWER CATHODE FOLLOWER

Model G power cathode followers are used in special applications in which certain fields are selected for reading operations only. Two model G power cathode followers develop the power necessary to drive 33 drum heads in much the same way that one drum field driver develops power to drive 33 drum heads. One power cathode follower drives even-numbered heads in selected fields and the other power cathode follower drives odd-numbered heads. Eighteen pairs of model G power cathode followers are used to drive 18 fields of read heads.

8.1 MODEL G POWER CATHODE FOLLOWER, BLOCK DIAGRAM ANALYSIS

The input cathode follower stage V1A of the model G power cathode follower receives command signals from field selection circuits. (See fig. 4–30.) The input cathode follower has two functions; it isolates the field selection circuits from the remaining stages in the model G cathode follower and matches the impedance looking back towards the field selection circuits and the input impedance of differential amplifier V1B. Output from V1A is sent to the differential amplifier V1B. The differential amplifier also receives a second input, a feedback signal from the output cathode follower V2 and V3. The purpose of the feedback signal is to maintain a constant level from the output cathode follower. The differential amplifier compares the two signals and increases or decreases the drive to the output cathode follower, as necessary, to maintain a constant output level.

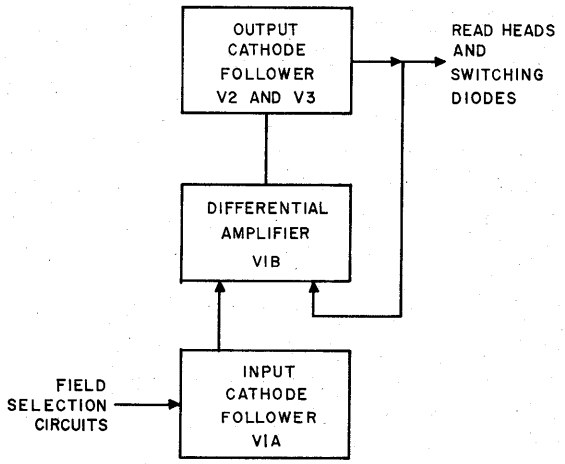


Figure 4–30. Model G Power Cathode Follower, Block Diagram

When the field selection circuits select a field associated with a model G power cathode follower, a select level is received. The output level of the power cathode follower permits conduction through switching diodes connected to the associated read heads. In the conducting state the switching diodes present a low-impedance path between the drum read heads and the drum read amplifiers. When the field selection circuits select fields other than ones associated with model G power cathode followers, a nonselect level is received by the power cathode follower, and its output level cuts off the switching diodes, disconnecting the associated drum read heads from the drum read amplifiers.

8.2 MODEL G POWER CATHODE FOLLOWER, CIRCUIT ANALYSIS

A schematic diagram of a model G power cathode follower is shown in figure 4–31; a simplified schematic diagram is shown in figure 4–32. When the field selection circuits select a field associated with the power cathode follower, a +10-volt level is applied to the control grid of input cathode follower stage V1A. This +10-volt input establishes approximately +11 volts at the cathodes of the input cathode follower and the differential amplifier stage V1B. A fraction of the output voltage from output cathode followers V2 and V3 is fed back to the grid of V1B. Assuming a +13.2-volt output from V2 and V3, feedback through the voltage divider network of resistors R13, R14, and R15 applies +7 volts to the control grid of V1B. The difference between the +7 volts feedback and the +11 volts at the cathode of V1B and V1A produces a −4-volt bias on V1B; V1B conducts slightly and plate voltage rises to +180 volts. The rise in plate voltage is coupled through the voltage divider network of resistors R4 and R5 to the control grids of V2 and V3.

The +180-volt potential at the plate of V1B places +5 volts on the control grids of V2 and V3. A positive voltage on the control grids of V2 and V3 produces heavy plate current. Tubes V2 and V3 have large current-handling capabilities which result in a high order of power amplification. The positive output of the output cathode follower (+13.2 volts) is applied to the center taps of the drum read heads in the selected field. The associated switching diodes conduct, and the drum read heads are electrically connected to the associated drum read amplifiers.

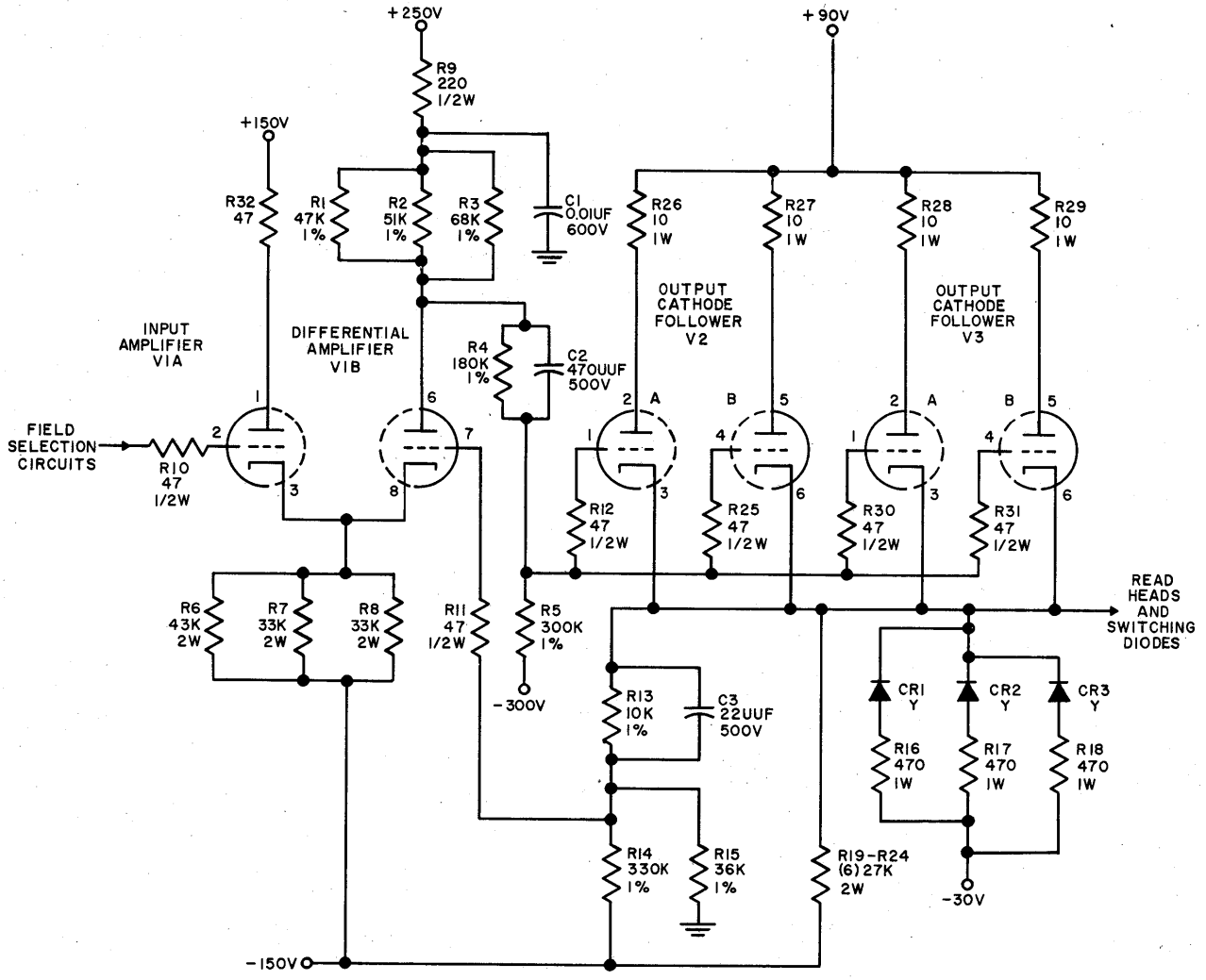


Figure 4–31. Model G Power Cathode Follower, Schematic Diagram

Capacitor C2 in the grid circuit of V2 and V3 is a high-frequency compensator which produces steep rise and fall times. Capacitor C3 in the feedback network is a high-frequency compensator which eliminates positive and negative overshoots. When the output voltages of V2 and V3 rise above +13.2 volts, a more positive voltage is fed back to the control grid of V1B. This increases conduction and reduces the plate voltage of V1B. Thus, the positive grid voltage applied to V2 and V3 decreases. Tubes V2 and V3 conduct less heavily, returning their cathode voltage to +13.2 volts. When the output voltage decreases to below +13.2 volts, a less positive voltage is fed back to the control grid of V1B. Tube V1B plate voltage rises, causing V2 and V3 to conduct more heavily, and the output voltage is raised to +13.2 volts.

When the field selection circuits select other fields for reading, a nonselect, —30-volt level is applied to the input cathode follower. This —30-volt input places the cathodes of V1A and V1B at —26.5 volts. Assuming a —32-volt output from the output cathode follower, feedback through the feedback voltage divider network produces a —28-volt level at the control grid of V1B. Tube V1B conducts heavily, and plate voltage drop is coupled through the voltage divider, thus producing —50-volt bias on the control grids of V2 and V3. Tubes V2 and V3 conduct very little. A —32-volt output of the output cathode follower is applied to the center tap of the drum read heads. The associated switching diodes are cut off, thereby disconnecting the drum heads from the drum read amplifiers.

When a —32-volt output of the output cathode follower goes more negative, the feedback voltage applied to the differential amplifier V1B cause tubes V2 and V3 to conduct more heavily. This heavy conduction returns the output cathode follower output voltage back to a normal —32-volt level. When the output voltage decreases, the action of the feedback network and tube V1B reduces conduction in V2 and V3. The drop in conduction increases the negative output of V2 and V3 and returns the output to the normal —32-volt level.

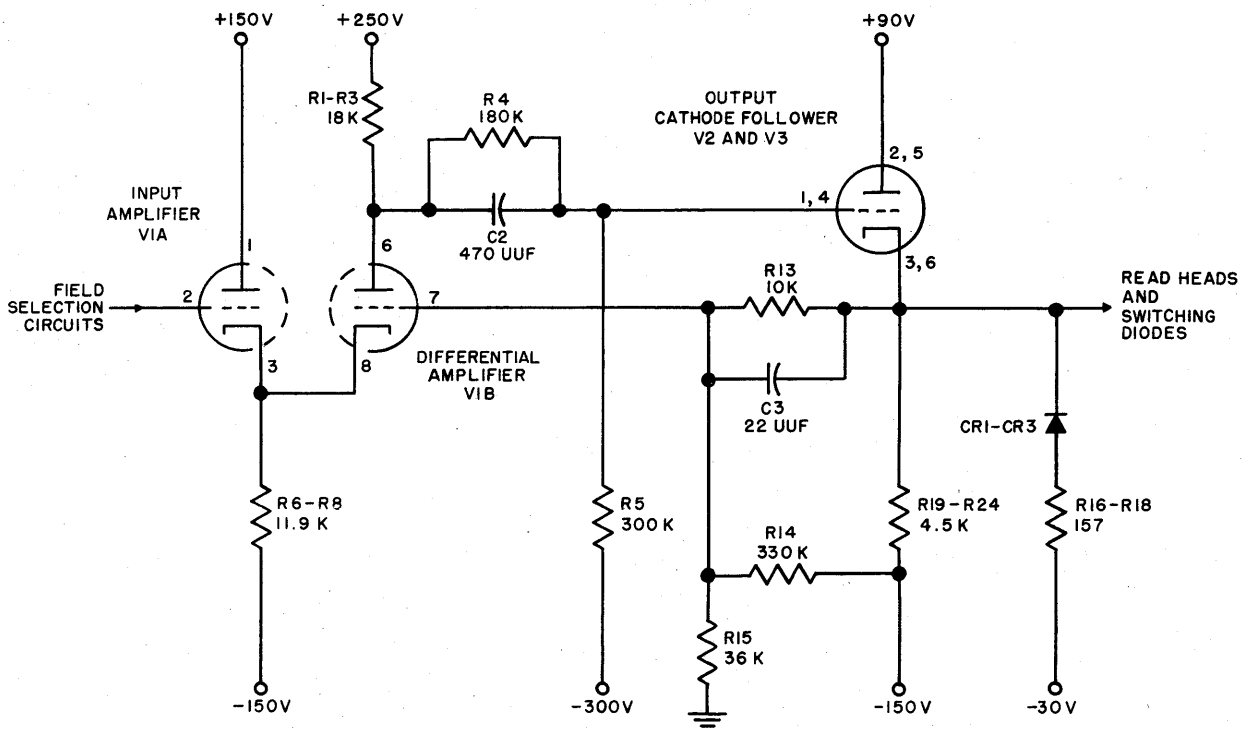


Figure 4–32. Model G Power Cathode Follower, Simplified Schematic Diagram

Crystal diodes CR1, CR2, and CR3 protect the read head and switching diode circuits against failure of the +90-volt power supply to V2 and V3. The crystal diodes clamp at —40 volts. Resistors R16, R17, and R18 reduce the delay in rise-time at the output of the power cathode follower. Assuming that resistors R16, R17, and R18 are absent, the diodes tend to clamp at —30 volts. This level is 2 volts less than the normal V2 and V3 output. The resulting feedback section tends to increase the negative bias on V2 and V3, cutting them off in an attempt to compensate for the lowered output level. Resistors R16, R17, and R18 limit current and equalize the load on the clamping diodes.

The RC network of resistor R9 and capacitor C1 (fig. 4–31) form a decoupling network for the power supply voltages. The 47-ohm and 10-ohm resistors employed in the grid and plate circuits of the power cathode follower suppress parasitic oscillations.

CHAPTER 9

DIODE SWITCH, MODELS A, B, C, AND D

For the sake of convenience, the diodes forming the read-write switching matrix are arranged in groups designated models A, B, C, and D. These models or a combination thereof are built into pluggable cans. The combination used in a can is dependent solely on the switching application. Taken alone, no function is performed by a diode switch since each is an integral part of the switching matrix. The diode switch, regardless of models used, serves merely as a passive transfer element and its behavior is contingent upon such input and output considerations as impedances and driving requirements. They are used to perform switching functions because they can pass current in only one direction. A detailed analysis of the logical operation of the diode switches, which is beyond the scope of this chapter, may be found

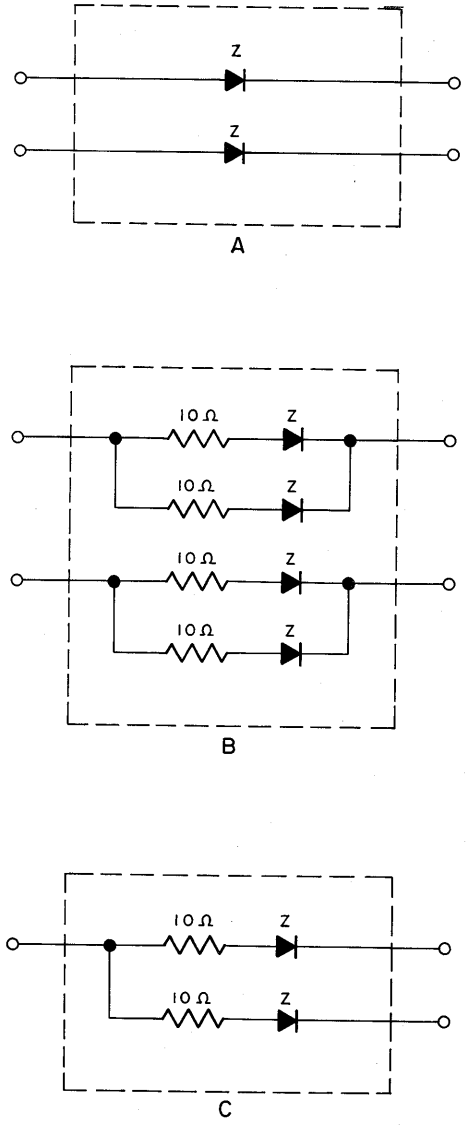


Figure 4–33. Diode Switch, Models A, B, and C

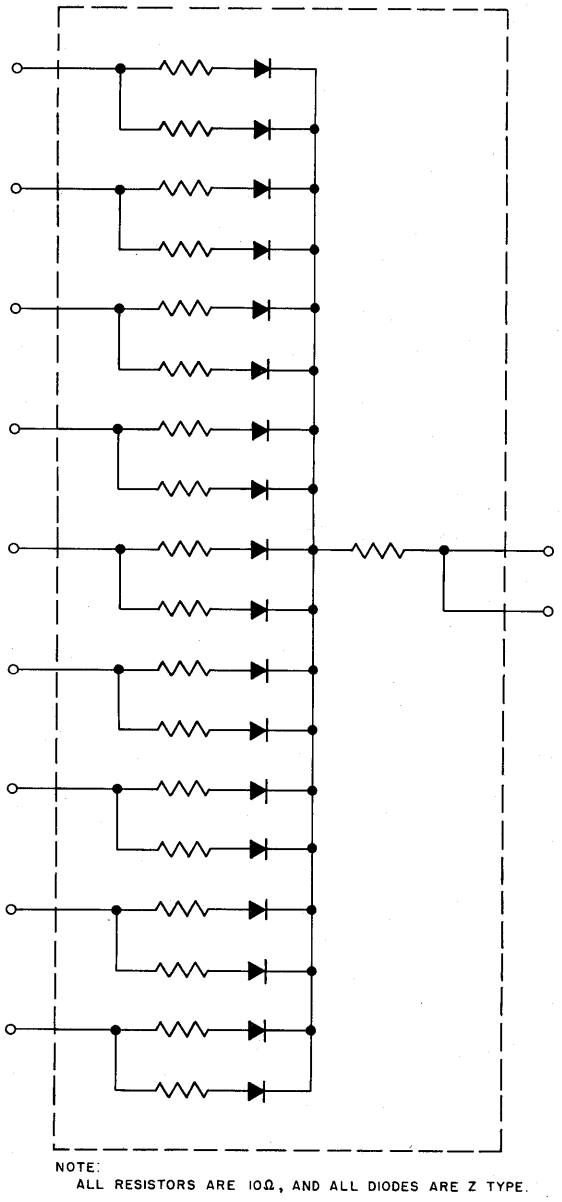


Figure 4–34. Diode Switch, Model D

in Chapter 3, Part 2, Drum and Field Selection. This chapter then will concern itself with the applications of the various models.

9.1 DIODE SWITCH, MODEL A

The model A diode switch, shown in figure 4–33, part A, is used as follows:

a. In the drum head diode switching matrix, it is used in conjunction with the drum read driver to disconnect the drum read amplifiers from the drum writers during writing operations and provides a magnetic drum heads of a selected field to the drum read amplifiers during reading.

b. Where there is more than one OD drum field associated with one group of read amplifiers, it is used in conjunction with a model G power cathode follower to switch between these fields, providing a path from the drum heads of one field to the read amplifiers, and blocking the heads of the remaining fields from the read amplifiers.

9.2 DIODE SWITCH, MODELS B AND C

Diode switches, models B and C, shown in figure 4–33, parts B and C, are switching devices between the CD drum fields and are used in conjunction with a drum field driver to switch between the various CD fields of the Drum System, enabling reading or writing on only one field at a time.

9.3 DIODE SWITCH, MODEL D

The model D diode switch, shown in figure 4–34, is used as a dummy load on drum writers for certain CD drum fields having fewer than 33 drum heads.

CHAPTER 10

OPTICAL FREQUENCY GENERATOR

10.1 OPTICAL FREQUENCY GENERATOR, BLOCK DIAGRAM ANALYSIS

A block diagram of the optical frequency generator is shown in figure 4–35. An optical timing disc mounted on the drum shaft rotates with the drum. The optical transducer forms a narrow beam of light which is directed through a transparent area on the optical timing disc. As the timing disc rotates, varying amounts of light pass

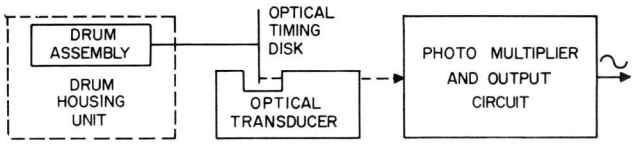


Figure 4–35. Optical Frequency Generator, Block Diagram

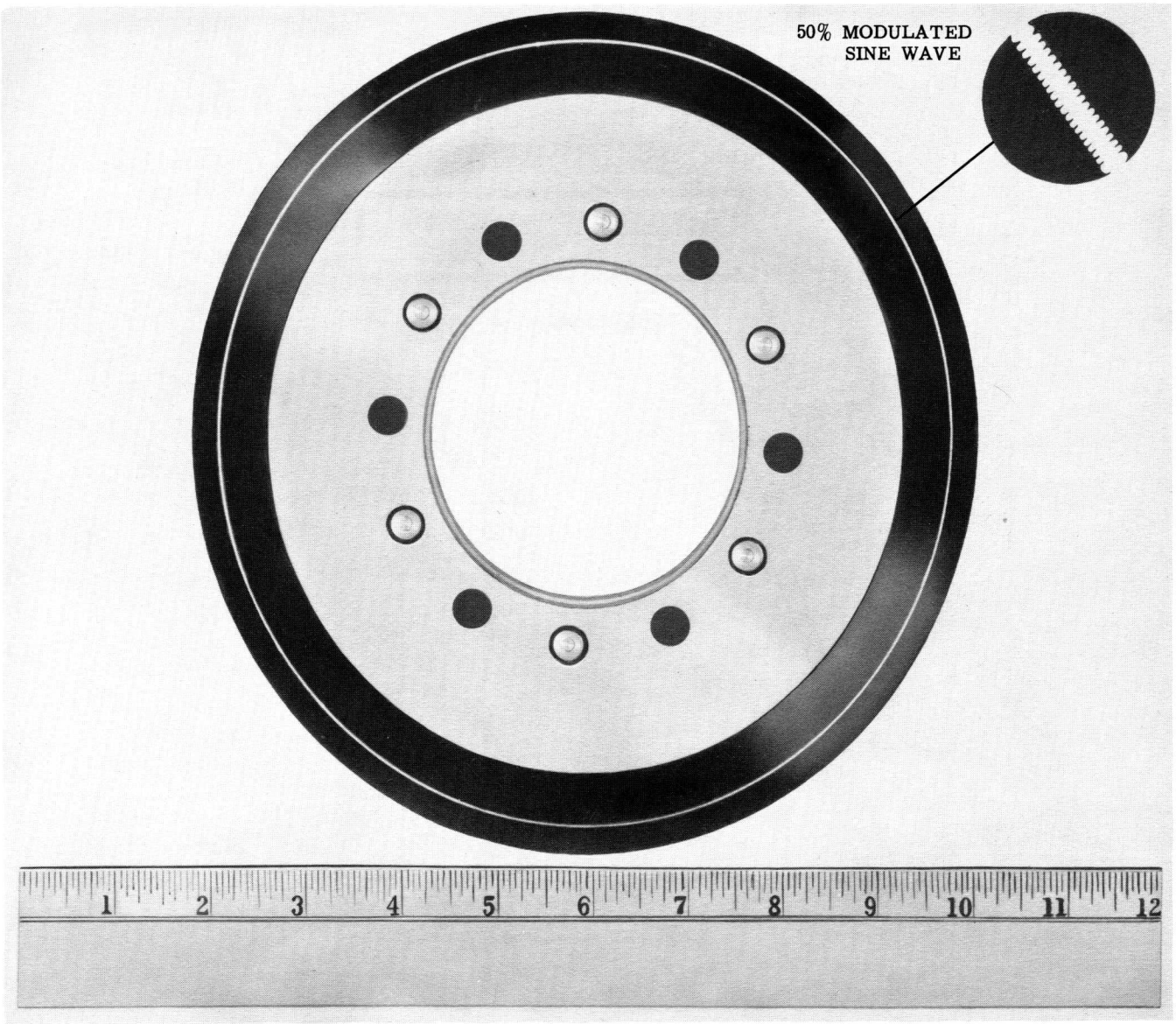


Figure 4–36. Optical Timing Disc

through the optical timing disc. This varying light is applied to a photomultiplier-and-output circuit. The photomultiplier converts the light energy to electrical energy. The output circuit acts as a buffer which feeds the output signal to a timing pulse generator.

10.2 OPTICAL FREQUENCY GENERATOR, CIRCUIT ANALYSIS

10.2.1 Optical Transducer

As the drum rotates, an optical timing disc mounted on the drum shaft turns with the drum. The optical timing disc is composed of two plates of glass, laminated with a photographic plate inserted between them. The photographic plate is opaque except for a transparent area that is etched around the outer periphery of the plate. The transparent area is in the shape of a 50 percent modulated sine wave pattern. (See fig. 4–36.)

The optical timing disc is mounted so that the transparent area cuts a light path in the optical transducer. A cross-sectional view of the optical transducer mounted on the drum assembly is shown in figure 4–37. Light from a lamp in the optical transducer passes through lenses 1, 2, 3, and 4 and is reflected by mirror 1. The reflected light passes through lens 5, and is reflected by mirror 2. The light is then projected through the transparent area of the optical timing disc. The amount of light passing through the optical timing disc is varied at a sinusoidal rate by the pattern of the transparent area. The varying

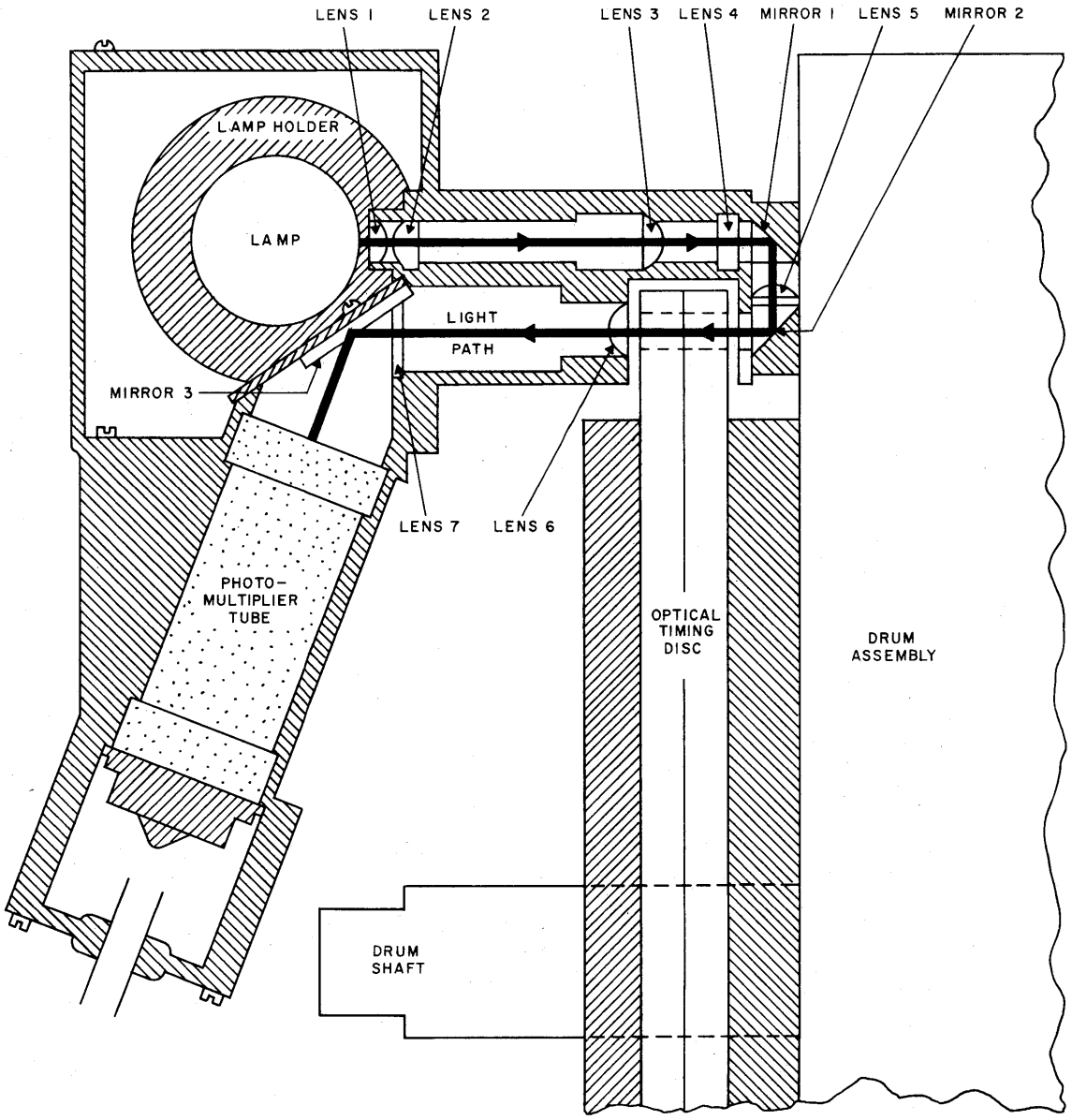


Figure 4–37. Optical Transducer and Drum Assembly, Cross-Sectional View

light passes through lenses 6 and 7 to mirror 3. Mirror 3 reflects the sinusoidally varying light into the window of a photomultiplier tube.

10.2.2 Photomultiplier and Output Circuit

The photomultiplier tube converts light energy to electrical energy. A schematic diagram of the photomultiplier and output circuit is shown in figure 4–38. A photomultiplier tube consists of a cathode, a number of dynodes, and an anode. A dynode is a metal plate, the surface of which is treated to produce high secondary emission. The cathode of photomultiplier tube V1 emits electrons proportional to the amount of light incident to it. These electrons are attracted to the first dynode (pin 1) by the d-c potential applied to it and by the proximity of the dynode to the cathode. For each electron that strikes the dynode, several secondary electrons are released. These secondary electrons from the second dynode (pin 7) are attracted in turn to the third dynode (pin 2). This process is repeated by the 3rd, 4th, 5th, and 6th dynodes (pins 6, 3, and 5, respectively). The secondary electrons from the sixth dynode are attracted to the anode (pin 4). Thus, for each electron emitted by the cathode, a large number of electrons are attracted to the plate. Since the amount of light striking the cathode varies at a sinusoidal rate, the amount of electrons attracted to the plate also varies at a sinusoidal rate. The output of the photomultiplier tube, V1, is a 100-kc sine wave. This signal is applied to the grid of V2. A low-Q resonant circuit from grid to ground acts as a bandpass filter. Cathode follower V2 feeds the signal to a timing pulse generator, isolating the photomultiplier tube from the timing pulse generator.

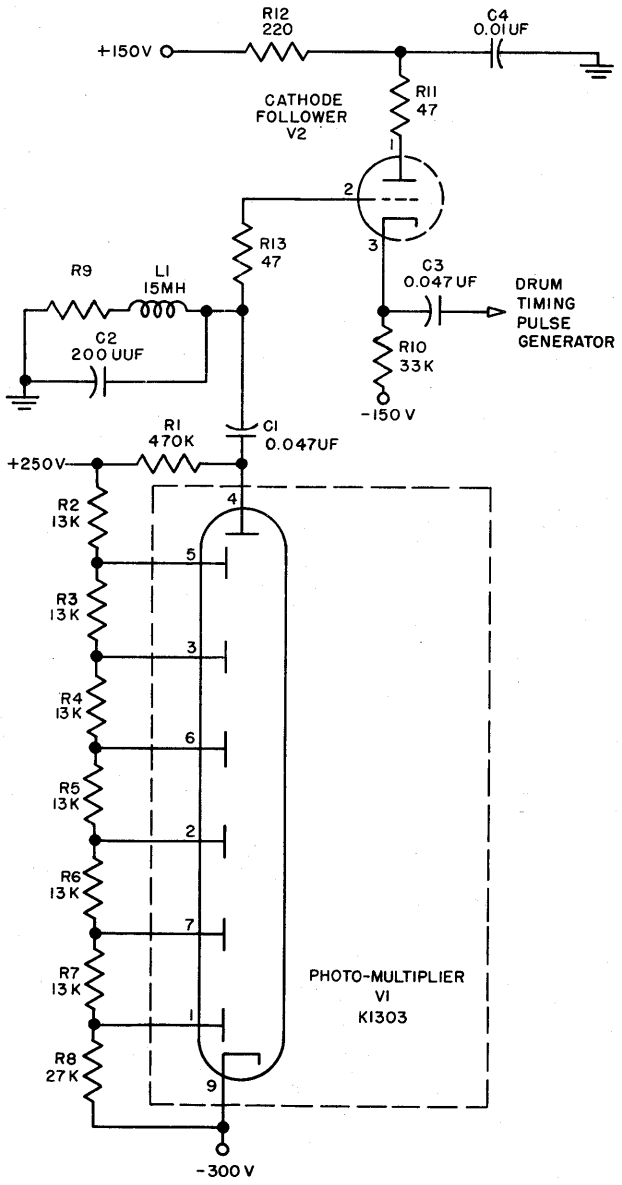


Figure 4–38. Photomultiplier and Output Circuit, Simplified Schematic Diagram

CHAPTER 11
TIMING PULSE GENERATOR

The timing pulse generator is employed both in the reading and writing of Drum System timing pulses. During the writing operation, the timing pulse generator receives sine wave inputs from the optical frequency generator. During the reading operation, the timing pulse generator receives sine wave inputs from the timing channel drum read head. In both instances, the timing pulse generator converts each sine wave cycle to two standard pulses, each occurring at one zero crossing point of the input sine wave. The two pulses are drum timing pulses DTP 1 and DTP 3, respectively.

11.1 TIMING PULSE GENERATOR, BLOCK DIAGRAM ANALYSIS

A block diagram of the timing pulse generator is shown in figure 4–39. Timing signals (100-kc sine waves) from the optical frequency generator or the read head on a drum timing channel are applied to the first push-pull amplifier stage, via a center-tapped transformer. The sine waves are amplified by the first and second push-pull amplifier stages V1 and V2. The amplified sine waves are applied to peaker limiter stages V3A and V3B. The peaker limiter stages convert the 100-kc input signal to 0.5-usec positive pulses.

The peaker limiters produce positive-pulse outputs at each negative-going zero crossing of the input sine wave. Since the input signal to V3A is 180 degrees out of phase with the input signal to V3B, the outputs of these two tubes are ½-cycle apart. Since the frequency of the timing pulse generator input signal is 100-kc, the two signals are 5 usec apart. The output of V3A is peaked, shaped, and amplified by the first, second, and third pulse shaping amplifier stages, V4A, V5, and V6. The output of V6 is a standard DTP 1 pulse. The output of V3B is peaked, shaped, and amplified by the first, second and third pulse shaping amplifier stages, V4B, V7, and V8. The output of V8 is a standard DTP 3 pulse.

11.2 TIMING PULSE GENERATOR, CIRCUIT ANALYSIS

Input signals from an optical frequency generator or a drum read head on a drum timing channel are applied to the primary of input transformer T7. (See fig. 4–40.) The secondary of T7 drives the control grids of the first push-pull amplifier stage V1A and V1B through parasitic suppressor resistors R3 and R4.

The first push-pull amplifier stage V1 is a conventional class A push-pull amplifier, except for the cathode circuit. The cathode of V1A is capacitively coupled to the cathode of V1B. This capacitor maintains the two cathodes at the same a-c potential. If the input signal at the grid of one of the tubes is reduced or missing, that tube acts as a grounded grid amplifier driven by the signal coupled to its cathode from the other cathode. Bias for the first push-pull amplifier stage is applied through resistor R10 returned to —150 volts. The use of separate

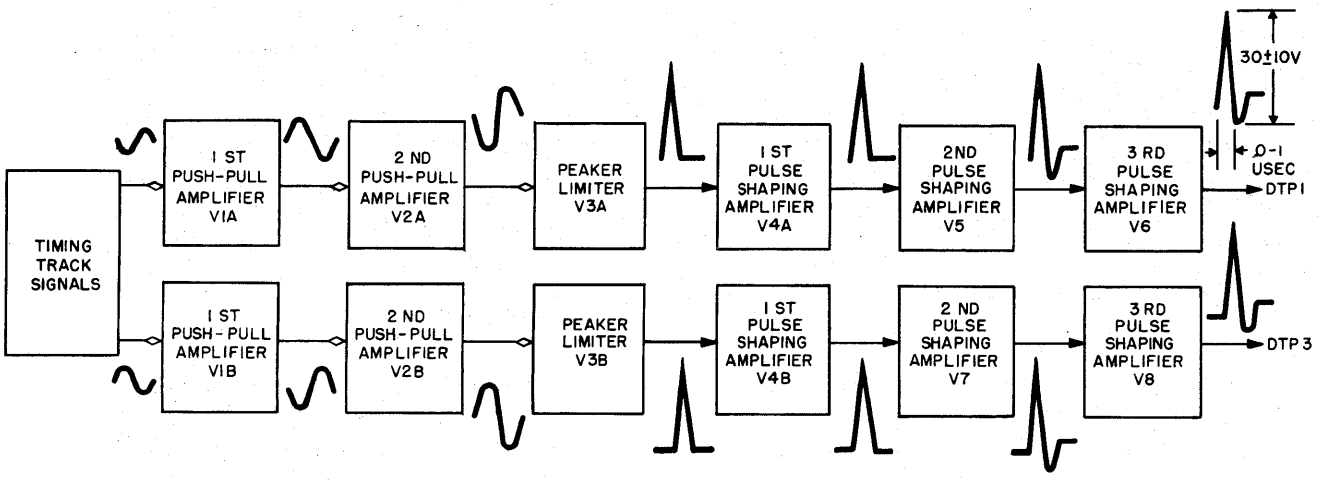


Figure 4–39. Timing Pulse Generator, Block Diagram

cathode resistors enables each section of the tube to establish its own d-c bias, compensating for differences in the conduction of the sections.

Resistor R9 is used as a common voltage source for both plates of V1. This is shown in figure 4—40, by indicating R9 with a solid line in the A section and a dashed line in the B section. Other circuit components serving as common sources for two sections of a tube are indicated in a similar manner.

The output signals of V1A and V1B are RC coupled to the second push-pull amplifier stage V2A and V2B. This stage operates in the same manner as the first push-pull amplifier stage. The output signals of V2A and V2B are RC coupled to peaker limiter stage V3A and V3B. The sine wave signal applied to the grid of V3A is much greater than the bias developed across cathode resistors R31 and R33. Therefore, the positive half of the input signal drives plate current to saturation and the negative half of the input signal causes plate current to be cut off.

During the time the input signal changes from positive to negative, plate current changes rapidly from a saturation to a cutoff level. Inductor L1 in the plate circuit of V3A resonates with the distributed capacitance of the circuit at approximately 1 mc. The rapid change of plate current shock excites the resonant circuit, tending to produce a damped waved train. The plate voltage forms a positive half-cycle at the resonant frequency and then tends to form the negative half-cycle. When plate voltage becomes less positive than the supply voltage, crystal diode CR1 draws current, damping the oscillation and clipping the negative half-cycle. When the input signal changes from negative to positive, plate current changes rapidly from cutoff to saturation. The rapid change of plate current tends to cause the plate voltage to become less positive. This causes crystal diode CR1 to draw current. The crystal shorts out inductor L1, causing plate voltage to equal the supply voltage. Therefore, the output of V3A is a positive pulse of approximately 0.5-usec duration, which occurs at the negative-going zero crossing of the input signal. Since V3B is identical to tube V3A, they produce similar outputs. The signal applied to V3B is 180 degrees out of phase with the signal applied to V3A. Therefore, the negative-going zero crossing of the signal applied to V3B occurs one half-cycle (5 usec for 100-kc inputs) later. Thus V3A and V3B alternately produce positive pulses.

A capacitor (C10) couples the cathode of V3A with the cathode of V3B (as was the case in the first and second push-pull amplifiers). In addition to functioning as described in the previous two stages, C10 also preserves the zero crossing point of the input sine waves despite distortion in previous stages. Assume that the signal of V3A changes from negative to positive, while the signal to V3B tends to remain positive. The change of signal to V3A causes the cathode voltage of V3A to increase. This increase has the same effect as a decrease in grid voltage. Therefore, as V3A changes conduction from cutoff to saturation, V3B changes from saturation to cutoff.

The signal output of V3A is coupled to the first pulse-shaping amplifier stage, V4A. V4A is normally cut off due to the bias applied through voltage divider R29 and R35. The applied pulse has sufficient amplitude to cause grid current to flow in V4A, thereby developing grid-leak bias. Grid-leak bias effectively clamps the positive peaks of the applied signal to ground potential. Only a small portion of the applied positive pulse to V4A causes plate current to flow. The plate circuit of V4A is similar in operation to the plate circuit of V3A. The rapid change of plate current from cutoff to saturation excites inductor L3. Inductor L3 is connected across the secondary of pulse transformer T1. Thus, the positive pulse applied to the grid of V4A causes V4A plate voltage to decrease. Inductor L3 tends to oscillate, but this oscillation is damped by crystal diode CR3. The output pulse of V4A is approximately 0.2 usec in duration.

Transformer T1 inverts the negative pulse from the plate of V4A to a positive pulse and applies it to the second pulse-shaping amplifier stage. Tube V5 is normally cut off by the —15-volt bleeder bias. Tube V5 operates in the same manner as tube V4A except that resistor R67 damps oscillations. Pulse transformer T3 couples the signal from the plate of V5 to the grid of V6. The signal at the grid of V6 is positive. The third pulse-shaping amplifier stage, V6, is biased below cutoff by the —30-volt bleeder bias. This bias voltage prevents ringing in the previous stage from producing an output. The large bias also reduces (as compared to V5) the conduction time of V6. This reduction causes the output pulse of V6 to be a standard DTP 1 pulse. The first, second, and third pulse-shaping amplifier stages, V4B, V7, and V8, operate exactly as do stages V4A, V5, and V6. The output of V8, a standard DTP 3 pulse, occurs 5 usec later than the output of V6.

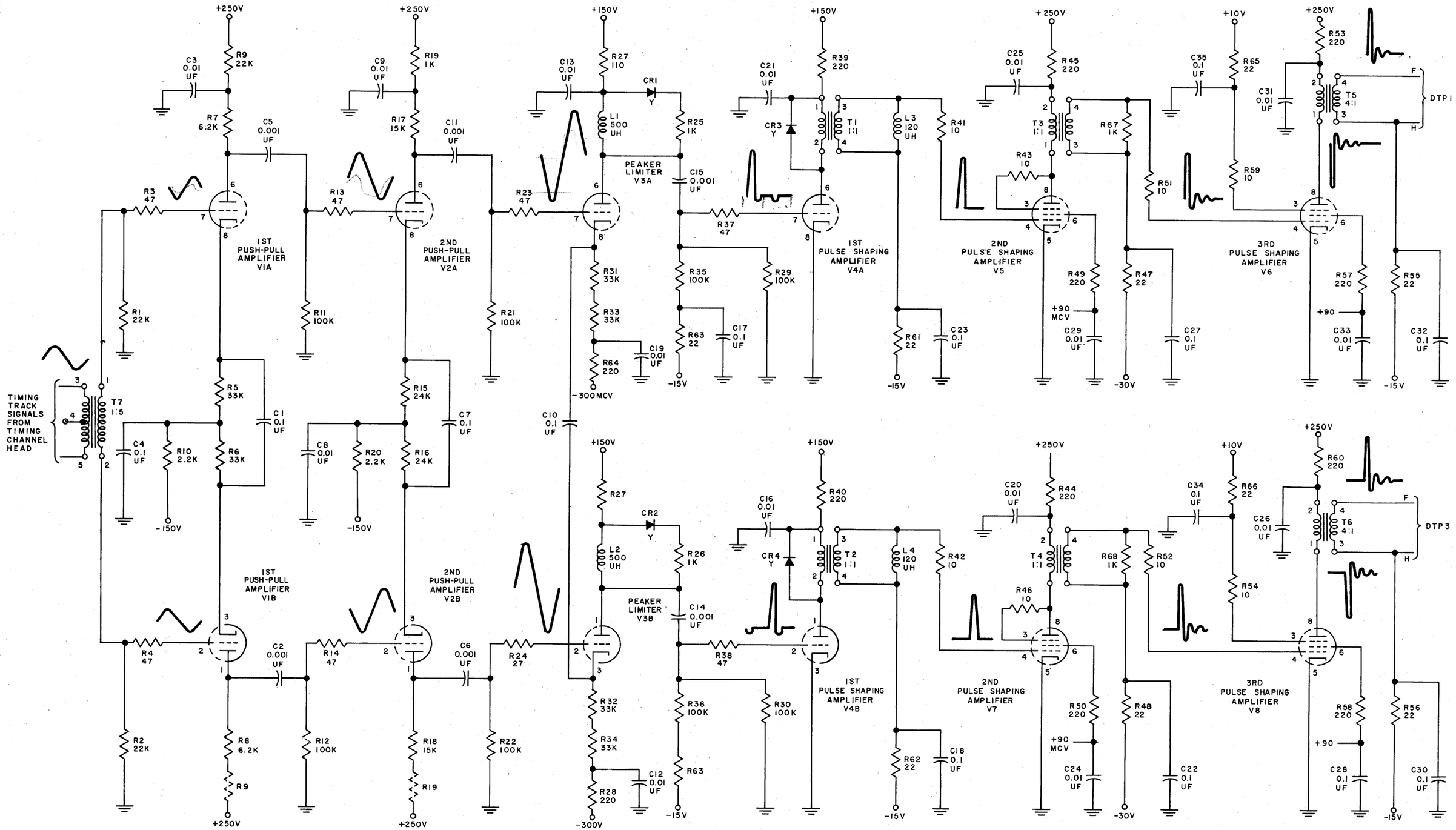


Figure 4-40. Timing Pulse Generator, Schematic Diagram

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