SAGE

3-42-0

THEORY OF OPERATION

OF

DRUM SYSTEM

FOR

AN/FSQ-7
COMBAT DIRECTION CENTRAL

AND

AN/FSQ-8
COMBAT CONTROL CENTRAL

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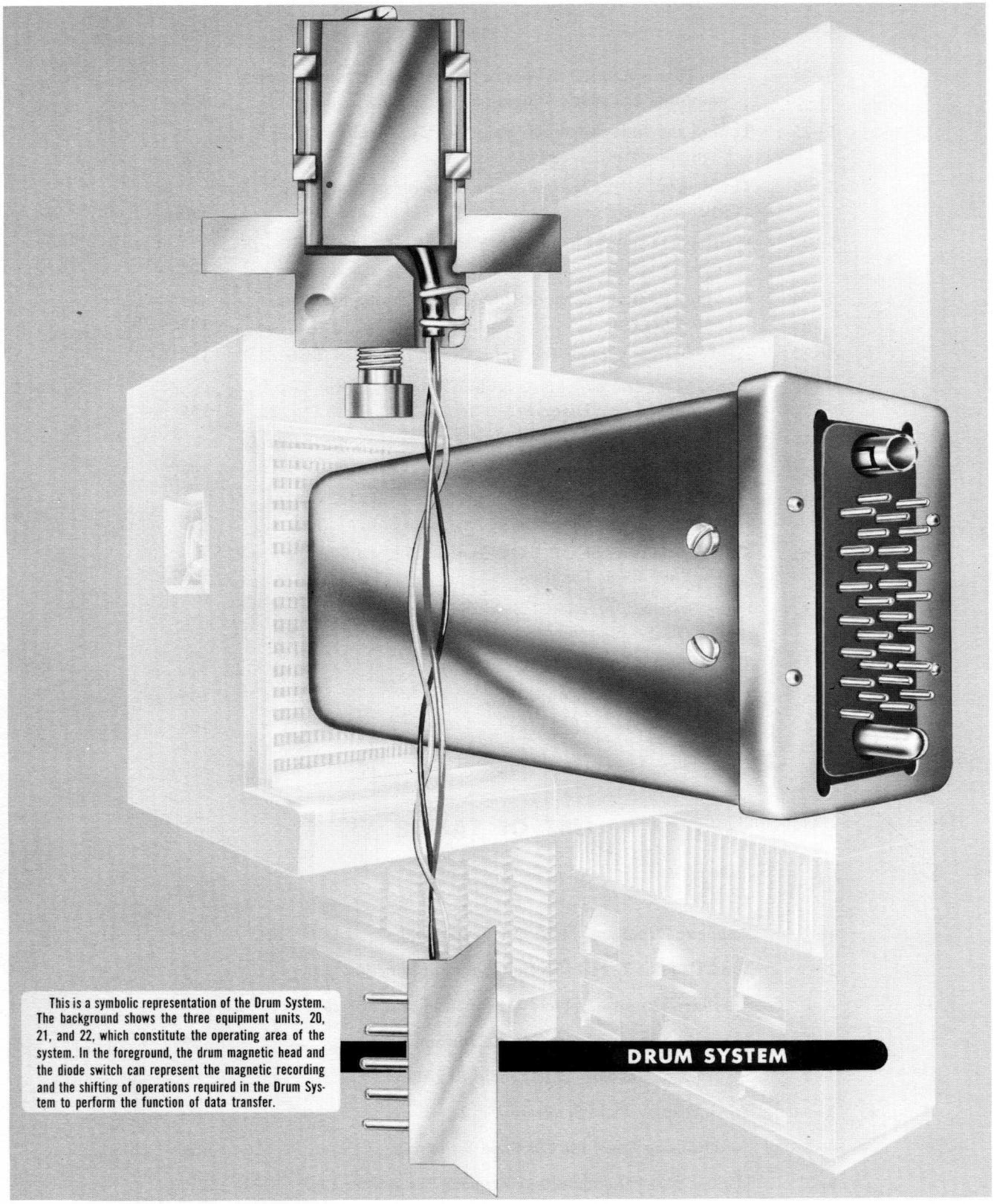


This is a symbolic representation of the Drum System. The background shows the three equipment units, 20, 21, and 22, which constitute the operating area of the system. In the foreground, the drum magnetic head and the diode switch can represent the magnetic recording and the shifting of operations required in the Drum System to perform the function of data transfer.

DRUM SYSTEM

CONTENTS (cont'd)

PART 1
INTRODUCTION

CHAPTER 1
PURPOSE AND SCOPE

1.1 PURPOSE

The primary purpose of this manual is to explain Drum System circuit operation to systems, displays, and IO IBM field engineers. The manual also serves as a reference source for IBM field engineers and other personnel assigned to technical duties at Air Defense Sites.

1.2 SCOPE

The manual has been divided so that field engineers receive adequate coverage of the Drum System in accordance with their assignments. Thus, the entire content applies to systems men; Parts 1, 2, 3, and Chapter 2 of Part 5 apply to displays men; Parts 1, 2, 4, and Chapter 3 of Part 5 apply to IO men. A detailed description of each part in the manual follows.

Chapter 1 of Part 1 covers the introductory matter. Chapter 2 presents physical details of the system; e.g., unit floor layout, configuration, and component descriptions. Chapter 3 discusses the overall characteristics of Drum System performance, its relationships with other systems of the AN/FSQ-7 equipment, and its most peculiar differences in the AN/FSQ-8 equipment.

Part 2 contains the most significant information concerning Drum System operation. The basic functions described in this part apply, in one way or another, to performance of all drum logic divisions, with particular emphasis on the interrelationship existing between the Drum and the Central Computer Systems.

The descriptions of addressable fields in Part 3 are based on the fundamental discussions of Part 2. This is particularly true in the case of auxiliary memory fields which are addressable and which are related to the Central Computer only. All other addressable fields are individually described and their relationship to the Display System and to the alternate Drum System in the equipment is pointed out in this part.

The descriptions of status fields in Part 4 also are based on the fundamental discussions of Part 2. The circuit in each of the status fields is analyzed and the modifications applicable to each case are described in detail along with their interrelationship with the Input and Output Systems.

Part 5 contains descriptions of circuits specifically assigned to test operation of the Drum System. Some of these test circuits serve to establish test loops with the Central Computer; the rest of the test circuits serve to isolate the Drum System from its interrelated systems to perform local tests. Chapter 1 of this part presents an overall discussion of test circuits. Chapter 2 describes addressable field loop tests with the Central Computer, thus establishing a correlation with the text in Part 3. Chapter 3 describes status field loop tests with the Central Computer to establish a correlation with the text in Part 4. Chapter 4 describes the circuit operation of manual test facilities and the method of analyzing individually the various functions of the system.

Part 6 describes the Drum System operating with AN/FSQ-8 equipment. These descriptions take the Drum System operating with the AN/FSQ-7 equipment as a reference and list all applicable physical and functional differences.

1.3 RELATIONSHIP TO OTHER MANUALS

The circuit descriptions and simplified diagrams presented in this manual have been based on the logic diagrams contained in 3-222-0, *Schematics for Drum System of AN/FSQ-7 Combat Direction Central and AN/FSQ-8 Combat Control Central.* Therefore, the closest relationship exists between this theory of operation manual and the Schematics manual. Relationships to a lesser degree also exist between this manual and the Theory of Operation manuals prepared for systems interrelated with the Drum System. These manuals are:

a. 3-3-0 *Special Circuits for AN/FSQ-7 Combat Direction Central and AN/FSQ-8 Combat Control Central* (refers to all systems)

b. 3-32-0 *Theory of Operation of Central Computer System for AN/FSQ-7 Combat Direction Central and AN/FSQ-8 Combat Control Central*

c. 3-52-0 *Theory of Operation of Input System for*

AN/FSQ-7 Combat Direction Central and AN/FSQ-8 Combat Control Central

d. 3-62-0 *Theory of Operation of Display System for AN/FSQ-7 Combat Direction Central and AN/FSQ-8 Combat Control Central*

e. 3-72-0 *Theory of Operation of Output System for AN/FSQ-7 Combat Direction Central and AN/FSQ-8 Combat Control Central*

f. 3-82-0 *Theory of Operation of Power Supply System for AN/FSQ-7 Combat Direction Central and AN/FSQ-8 Combat Control Central*

CHAPTER 2

DRUM SYSTEM PHYSICAL DESCRIPTION

2.1 GENERAL

The original design requirements of the AN/FSQ-7 equipment indicated that magnetic storage needs could be satisified by four data transfer drums (MIXD, LOG, TD, and RD) and two computer data auxiliary drums (AM-A, and AM-B). However, in time, equipment demands determined the need for additional auxiliary magnetic storage space. These demands were satisfied with the incorporation of six computer data auxiliary drums (AM-C through AM-H). Presently, the original six magnetic drums are referred to as the main drum group, and the additional six as the auxiliary drum group.

The Drum System is thereby divided into two physical areas, main drums and auxiliary drums. These areas are contained within units 21, 22, and 20. Figure 1–1 shows the unit layout on the equipment floor at the site. Units 20, 21, 22 as well as module E of the duplex maintenance console have been shaded in the figure to indicate their respective location on the floor. Notice that the Drum System is fully duplexed; therefore, the above components are found in areas A and B of the equipment. The main-drums control circuits are located in unit 21, while the main drum assemblies and their transfer circuits are housed in unit 22. The auxiliary drum assemblies and their control and transfer circuits occupy unit 20.

Drum System performance may be monitored locally at the system units or remotely at the duplex maintenance console. Module E of this console contains the various controls and indicators necessary for such monitoring.

Power for the three Drum System units is obtained from marginal checking and distribution (MCD) units 29 and 46. Unit 29 services the main drums and unit 46 the auxiliary drums.

2.2 UNIT 21

The main-drums control circuits are located in unit 21, which is composed of 15 nine-tube modules, labeled A through R (excluding I, O, and Q). In addition, a Z module is provided for power control and distribution. The circuits contained within this unit are intended to effect information transfers. Discussions pertinent to their operation are provided in the text. The main components of the unit, such as the test door, the power control panel, and the circuit breaker panel, are described in paragraphs 2.2.1 through 2.2.3.

2.2.1 Test Door

The main-drums test door (fig. 1–2), module 21L, serves to provide test switches and neon indicators which enable manual local testing. The test switches provide for the local generation of each Drum System function, such as selection, writing, reading, etc. The neon lamps furnish visual indications useful in localizing control and distortion errors to specific parts of the system. Reference is made to manuals 3-152-0, *Maintenance Techniques and Procedures of Drum System* and 3-292-0, *Fundamentals of Maintenance for AN/FSQ-7 Combat Direction Central and AN/FSQ-8 Combat Control Central,* which provide test door operation procedures.

The test door is divided into several panel sections, each of which is concerned with either the initiation of a test operation or the indication of a malfunction. Most of the panel sections contain a combination of switches and neon indicators; each switch and associated indicator are labeled in accordance with the operation they reflect.

Two panel sections are provided with neon indicators only. The neons in each of these panel sections are mounted in duly labeled rows. In addition, the lamps in each row are labeled, to associate them with a specific drum, bit, or signal.

2.2.2 Power Control Panel

The power control panel (fig. 1–3) is mounted on the Z module back panel. This panel is composed of two rows containing lever switches, pushbars, and incandescent lamp indicators. The lever switches and pushbars exercise control over power application to unit 21 and may be operated manually. However, in the event of excessive power fluctuations in associated circuit breaker lines, the lever switches and pushbars are automatically operated. The two lever switches control the individual application of a-c and d-c power to the unit. Corresponding ON-OFF lamps indicate the presence or absence of a-c and d-c power. Also, incandescent lamps enclosed within each pushbar serve to indicate the overall state of the unit.

Three incandescent lamp indicators in the upper row of the panel serve to reflect any power disturbance

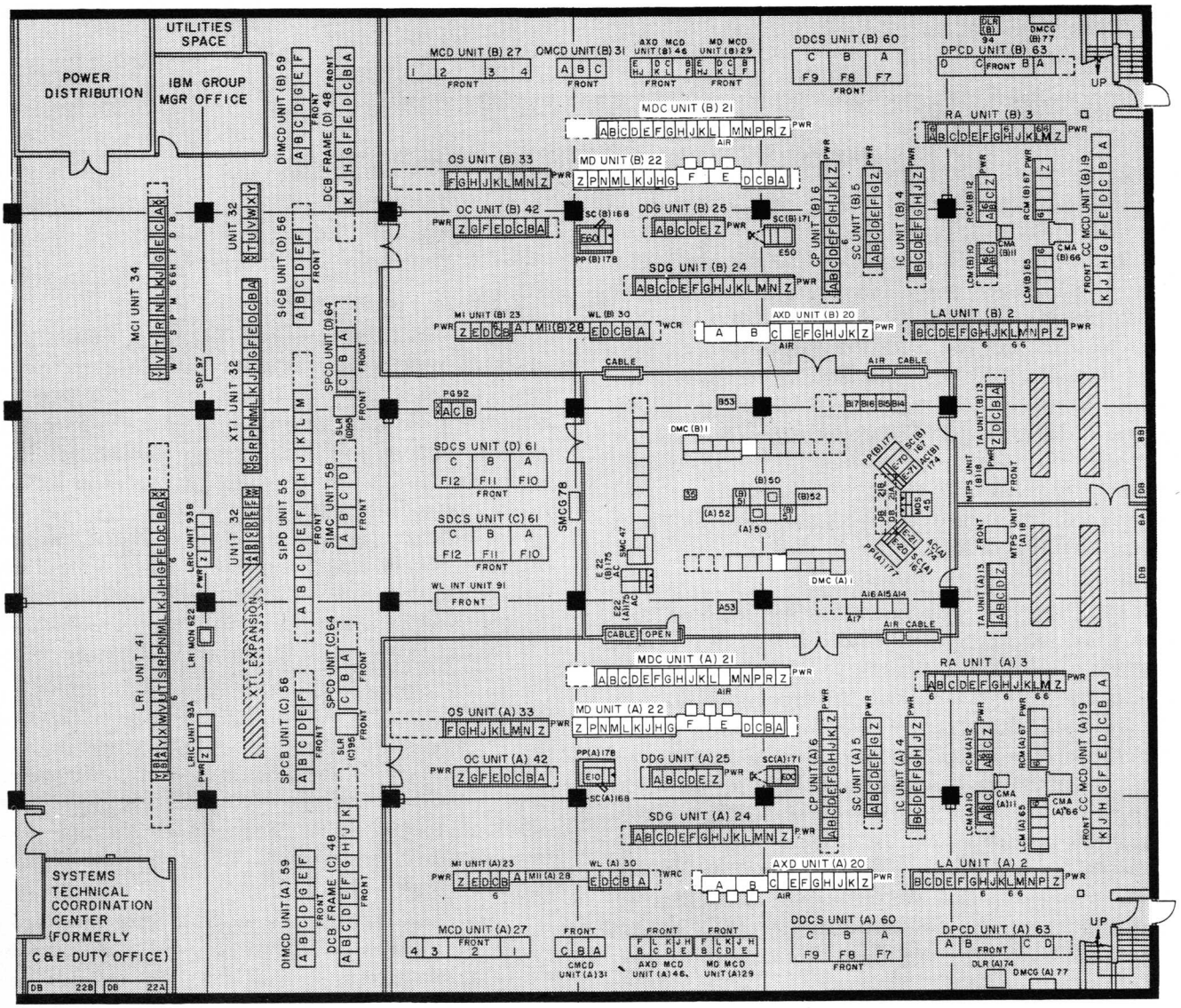


Figure 1–1. Equipment Floor Layout; Drum System Unit Location

in each of the three areas of the corresponding circuit breaker panel (refer to par. 2.2.3).

2.2.3 Circuit Breaker Panel

The circuit breaker panel (see fig. 1–4) is mounted on the Z module front panel. Circuit breakers are protective devices that automatically disconnect power when power surges occur. The panel is divided horizontally into three major sections, which are labeled, top to bottom, as follows: AC FILAMENT, NON-MARGINAL CHECK, and MARGINAL CHECK.

2.3 UNIT 22

Unit 22 contains the Drum System transfer circuits and also serves as the main-drum assemblies housing facility. The unit is composed of 12 nine-tube modules, labeled A through P. Modules E and F are mounted horizontally over the drum housings. The other modules are of the standard vertical type. The operation of transfer circuits is presented with the corresponding logic description in the text. Paragraphs 2.3.1 through 2.3.3.9 describe the significant components of the unit; these include the power control panel, the circuit breaker panel, and the magnetic drum assembly.

2.3.1 Power Control Panel

The power control panel is identical to that found on unit 21 (refer to par. 2.2.2).

2.3.2 Circuit Breaker Panel

The circuit breaker panel is identical to that found on unit 21 (refer to par. 2.2.3).

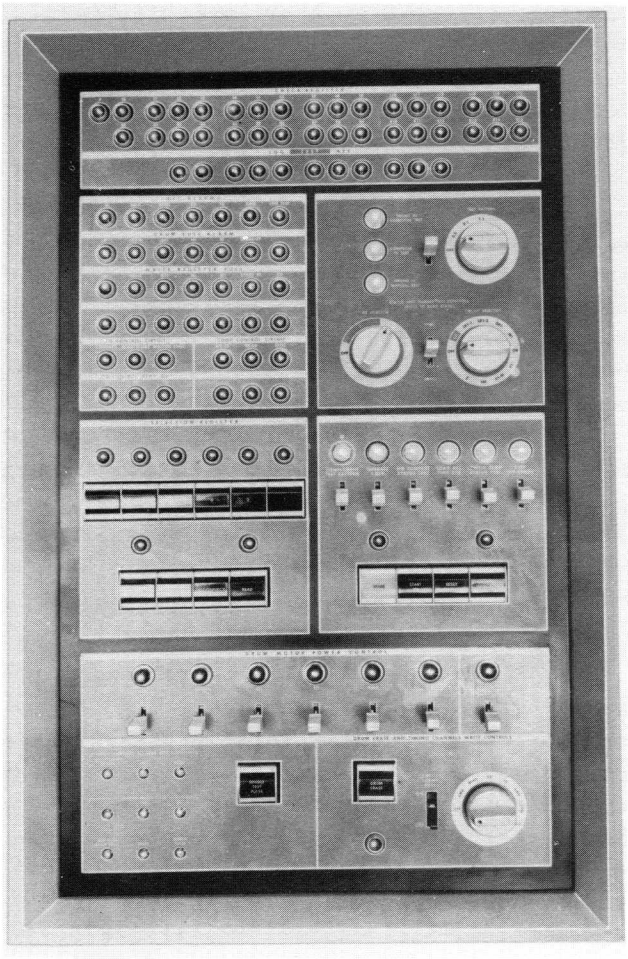


Figure 1–2. Main Drums Test Door

Figure 1–3. Power Control Panel

2.3.3 Magnetic Drum Assembly

2.3.3.1 Overall Description

The magnetic drum assembly (figs. 1–5 and 1–6) is mounted on the drum cradle, a hinged casting which pivots in and out of the drum unit structure. This arrangement enables the drum assembly to be swung out from its housing, thus furnishing ready access to assembly components. The following constitute the characteristic components of the drum assembly: the drum rotor, the drum motor, diode switch cans, drum bars, and write-read heads. One complete drum assembly weighs approximately 450 pounds.

The magnetic drum assembly is protected by a transparent plastic dome. Filtered 60-degree air is fed into the dome to cool the drum assembly.

2.3.3.2 Drum Rotor

The magnetic drum rotor (figs. 1–5 and 1–6) is a Monel metal cylinder, coated with copper and plated with nickel-cobalt. The 0.01-inch copper coating fills the porosity of the Monel metal and provides a diamond polished surface. The 0.0005-inch nickel cobalt plating is a dia-magnetic alloy characterized by high remanence. This plating provides the magnetic storage capabilities of the drum surface. The rotor is 10.7 inches in diameter, 12.5 inches long, and weighs 105 pounds. Its shaft is mounted on ball bearings and has a toothed pulley connected by a belt to the drum motor pulley.

2.3.3.3 Drum Motor

The drum motor (fig. 1–5) is a synchronous, 3-phase, 3600-rpm motor operating at 208V. It is rated at ½ hp and requires a large starting current of 125 amp/phase to develop the high starting torque (16.8 lb-ft) necessary to bring the drum rotor quickly up to speed. The motor is approximately 14-⅛ inches long (shaft included) and 9 inches wide. It is mounted on the cradle beneath the drum rotor. A toothed pulley on the drum motor and a drive belt connect the motor with the rotor of the drum.

2.3.3.4 Diode Switch Cans

Pluggable cans containing diode switches serve as a convenient means of accommodating the numerous diodes required for field switching in each drum refer to Ch 6, Part 2). Several diodes may be contained within

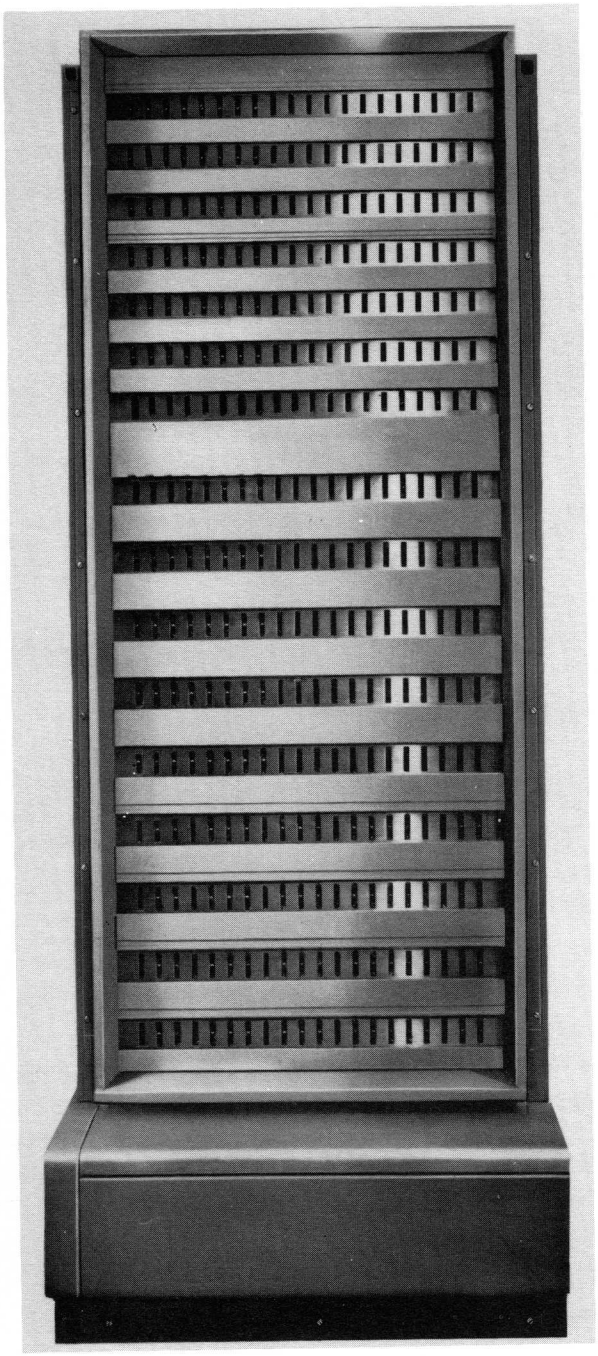


Figure 1–4. Circuit Breaker Panel

each can (figs. 1–5 and 1–6). Field switch diode cans are mounted on apron-type shelves on both sides of the drum assembly. CD drum and read switch cans are mounted on panels located in the drum housing structure to the right of each drum. Each can is provided with guide pins at one end and a pull ring at the other to facilitate insertion and removal.

2.3.3.5 Drum Bars

Each drum contains provisions to accommodate 13 bars (figs. 1–5 and 1–6) in an arc of 216 degrees. In the MIXD, LOG, TD, and RD drums, six pairs of these bars are used to mount read-write heads; the 13th bar is the erase bar. In the auxiliary drums, AM-A through AM-H, alternate spaces occupy read-write head bars, leaving the 13th space for the erase bar.

To enable read-write head mounting, the center of each bar is cut out lengthwise and screw mounting holes are provided along the inside edges. A maximum of 40 heads can be mounted on each bar (actually, 33 heads are commonly used for data and two or three additional heads for purposes of circuit control). Each drum bar weighs approximately 8 pounds.

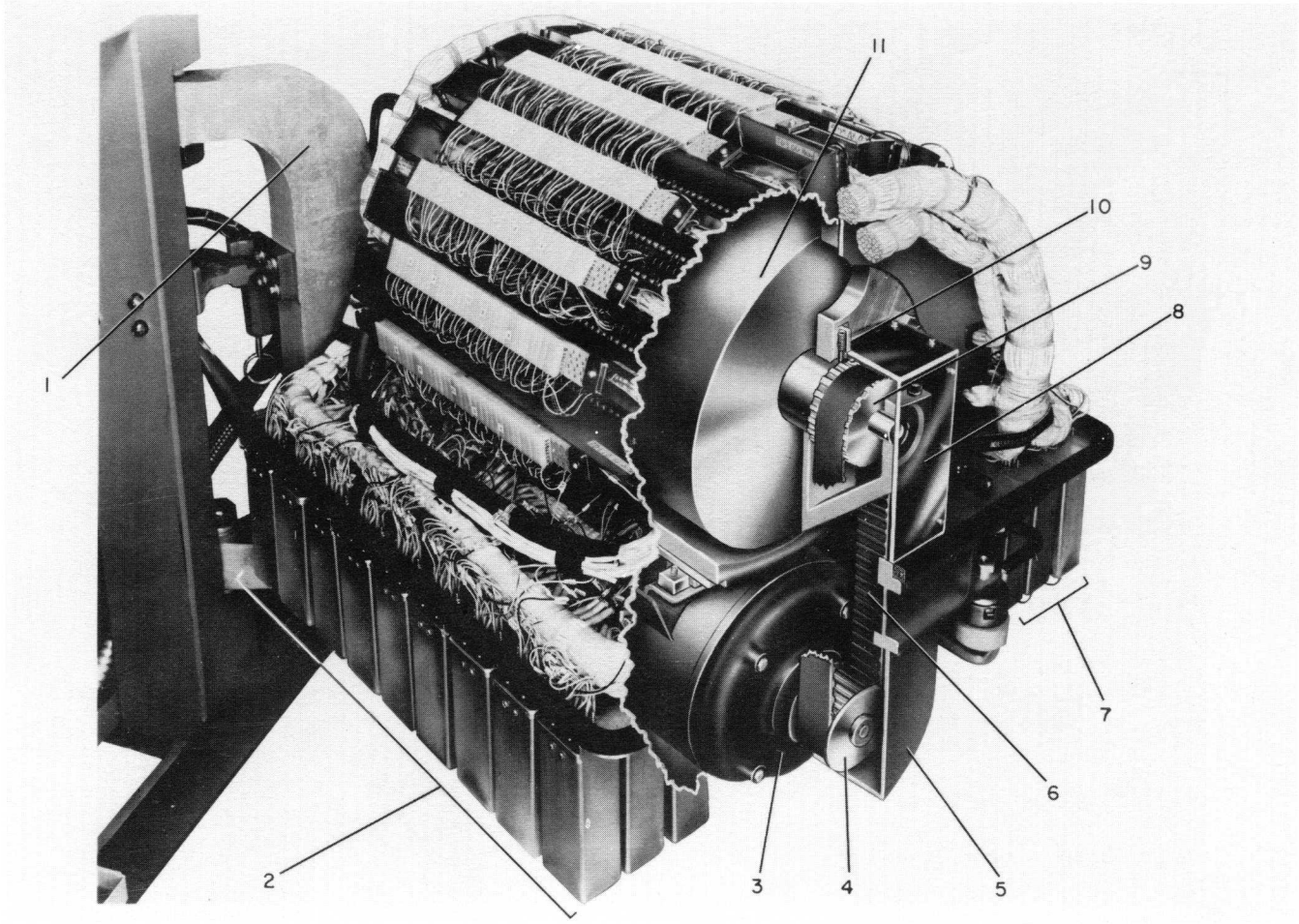
The erase bar (fig. 1–7), which is mounted between the first read-write head bar and the drum casing, permits demagnetization of the corresponding drum. This bar consists of a metal channel with a centerpiece which serves as an electromagnetic core for four coil windings.

2.3.3.6 Write-Read Heads

The Drum System presently utilizes aluminum heads (fig. 1- 8) which are used for both writing and/or reading. The component parts of an aluminum head, illustrated in the figure, follow: the open-bottom case, amplitude adjust screw, carriage-retract spring, core-buffer spring, head assembly clip, carriage, core-tracking spring, core assembly wire clip, shoulder screws, and male connector. When assembled, the head is held together by the head assembly clip. The core assembly consists of nine insulated laminations, 0.002 inch thick. A 0.001-inch silver shim is inserted in the core-recording gap and soldered into place to keep its size constant. A coil wound around the core magnetizes the core during both writing and reading.

The operation of the components inside the assembled head (see fig. 1–9) is as follows. The core-buffer spring is anchored to the carriage roof; it places a constant downward pressure on the core assembly, causing the core-recording gap to be moved toward the drum surface. The carriage-retract spring is anchored to the case at one end and presses against the carriage roof at the other end. Thus, upward pressure is produced on the carriage roof. This pressure is opposed by the setting of the amplitude adjust screw. In other words, as the screw is turned clockwise, the carriage is moved downward, moving the core-recording gap toward the drum surface. Notice that the core assembly does not swing around a pivot; rather it moves up and down with the carriage as it slides on the case. Also notice that there is no interaction between the core-buffer spring and the carriage-retract spring.

A core-tracking spring is mounted between the case and the core assembly to prevent any possible chatter of the core assembly within the head assembly.



1 Drum Cradle
2 CD Field Diode Switch Cans
3 Drum Motor
4 Drum Motor Pulley
5 Drum Motor Pulley Guard
6 Drum Belt
7 OD Field Diode Switch Cans
8 Transparent Drum Rotor Pulley Guard
9 Drum Rotor Pulley
10 Static Grounding Brush, Sectional View
11 Drum Rotor

Figure 1–5. Magnetic Drum Assembly, Pulley End

Two shoulder screws passing through mounting shoulders on the drum-head case secure each drum head to the drum bar (refer to par. 2.3.3.5). Each head may be moved laterally in its mounting to determine the proper location of the corresponding channel. Each head may also be moved forwards and backwards to adjust for timing and register co-ordination.

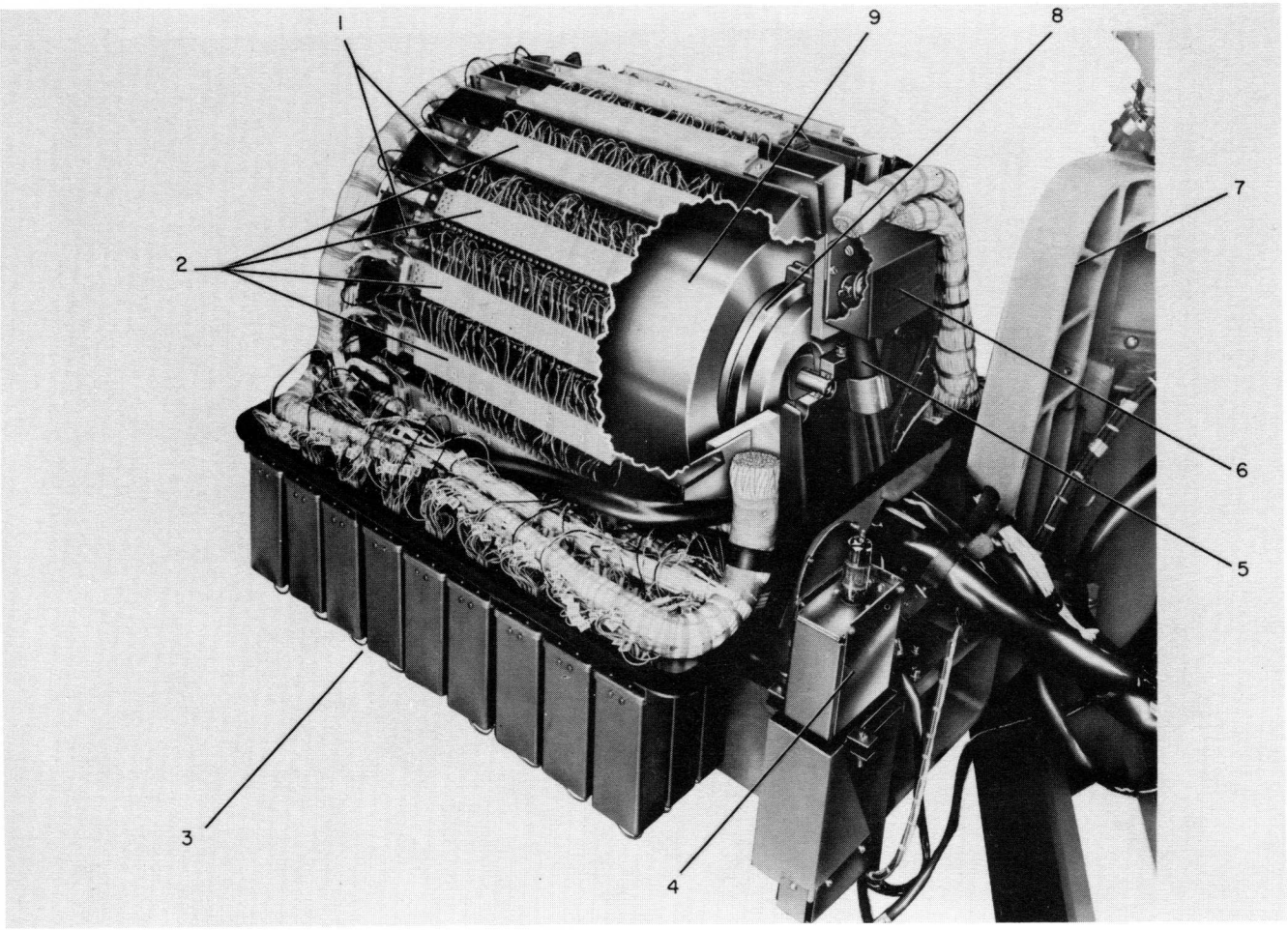
The wire clip anchors the connecting wires to the case, preventing undue strain on the core assembly connections. The 5-pin male connector plugs into a female receptacle located on the drum assembly. Male connectors from the heads on a drum bar are inserted into adjacent female receptacle bars.

2.3.3.7 Optical Timing Disc

The optical timing disc (fig. 1–10) is approximately 8 inches in diameter and 0.5 inch wide. It is mounted on the drum rotor shaft at the nonpulley end of the drum assembly. The disc comprises two plates of glass laminated with a photographic plate between them. The photographic plate is opaque except for a transparent area. This area, shown magnified in the figure, has the shape of a 50 percent modulated wave envelope. There are 2,048 wave variations in the optical timing disc of all drums except the TD and RD drums. The disc mounted on the TD and RD drums has 2,060 variations. Refer to Part 2, paragraph 4.2.3, for a description of timing disc operation.

2.3.3.8 Optical Transducer

The optical transducer (fig. 1–11) comprises one exciter lamp, seven lenses, three prismatic mirrors, and a photomultiplier tube. The transducer is mounted on the non-pulley end of the drum above the drum motor shaft. Refer to paragraph 4.2.1.2 of Part 2 for the functional description of the transducer.



1 Drum Bars
2 Head Connectors
3 Field Diode Switch Cans
4 Power Cathode Follower PU
5 Photomultiplier
6 Transducer Housing
7 Drum Assembly Cradle
8 Optical Timing Disc
9 Drum Rotor

Figure 1–6. Magnetic Drum Assembly, Nonpulley End

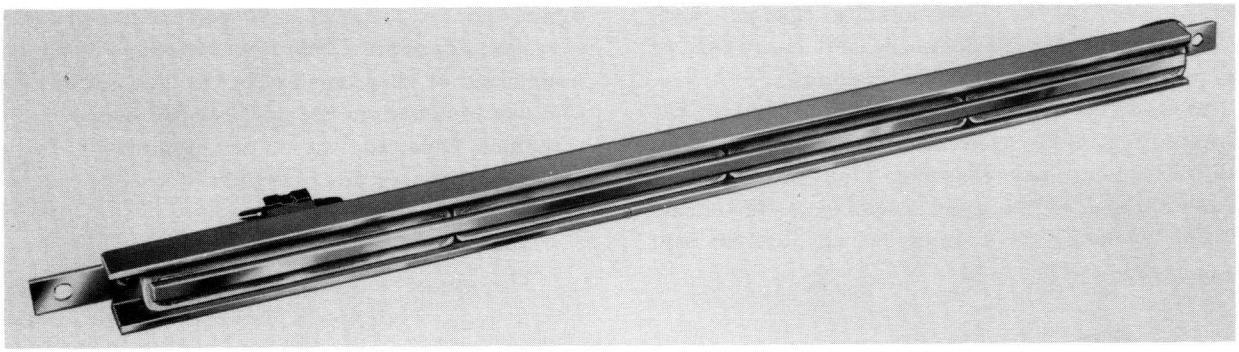
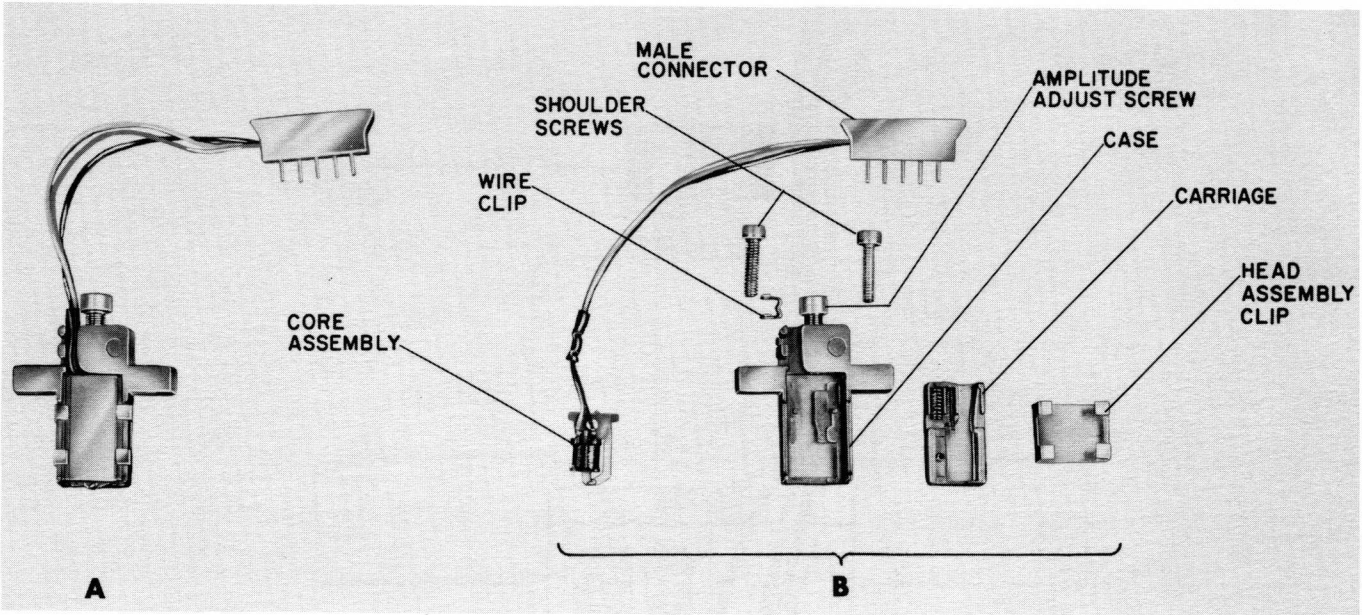


Figure 1–7. Erase Bar



A — Head Assembly
B — Head Components
Figure 1—8. Write-Read Aluminum Drum Head

2.3.3.9 Etched Timing Disc

The etched timing disc to be installed in all Drum Systems starting with site 17 has the same diameter as the drum rotor (approximately 10.7 inches) and 0.75 inch wide. It is mounted on the drum rotor shaft at the nonpulley end of the drum assembly. The disc recording surface (fig. 1—12) is treated identically to that of the drum rotor (par. 2.3.3.2). Upon this surface, shown magnified in the figure, the index and the timing channels signals are etched to form ridges and valleys. The ridges correspond to the disc surface, while the valleys are cut through the nickel-cobalt plating baring the copper coating. There is one etching in the index channel on the etched timing disc of all drums: there are 2,048 etchings in the timing channel of all the drums except the TD and RD drums. The timing channel of these drums contains 2,060 etchings. Paragraph 4.2.2 of Part 2 describes the etched timing disc circuit.

2.4 UNIT 20

The auxiliary drum assemblies and control and transfer circuits are housed in unit 20. The unit contains 10 nine-tube modules, A through K and a Z module for power distribution. The circuits occupying this unit effect all auxiliary drum operations. Related circuit operation discussions are provided in the text. Paragraphs 2.4.1 through 2.4.4 deal with the chief components of the unit.

2.4.1 Test Door

The auxiliary drums test door (fig. 1—13) mounted on module F provides the switches and indicators necessary for local testing. This test door is simpler than the main drums test door, because auxiliary drums are only connected for CD operation. However, the layout of controls and indicators is similar in both doors (par. 2.2.1).

2.4.2 Power Control Panel

The power control panel is identical to that found on unit 21 (par. 2.2.2).

2.4.3 Circuit Breaker Panel

The circuit breaker panel is identical to that found on unit 21 (par. 2.2.3).

2.4.4 Magnetic Drum Assembly

The auxiliary magnetic drum assembly is identical to that of the main drums (par. 2.3.3), excepting that only seven drum bars are utilized instead of 13. This is because only CD operations are accommodated; therefore the six bars which accommodate OD transfers are omitted.

2.5 MODULE E, DUPLEX MAINTENANCE CONSOLE

Module E of the duplex maintenance console (fig. 1—14) is directly related to Drum System operation. This module is divided into an upper and a lower sec-

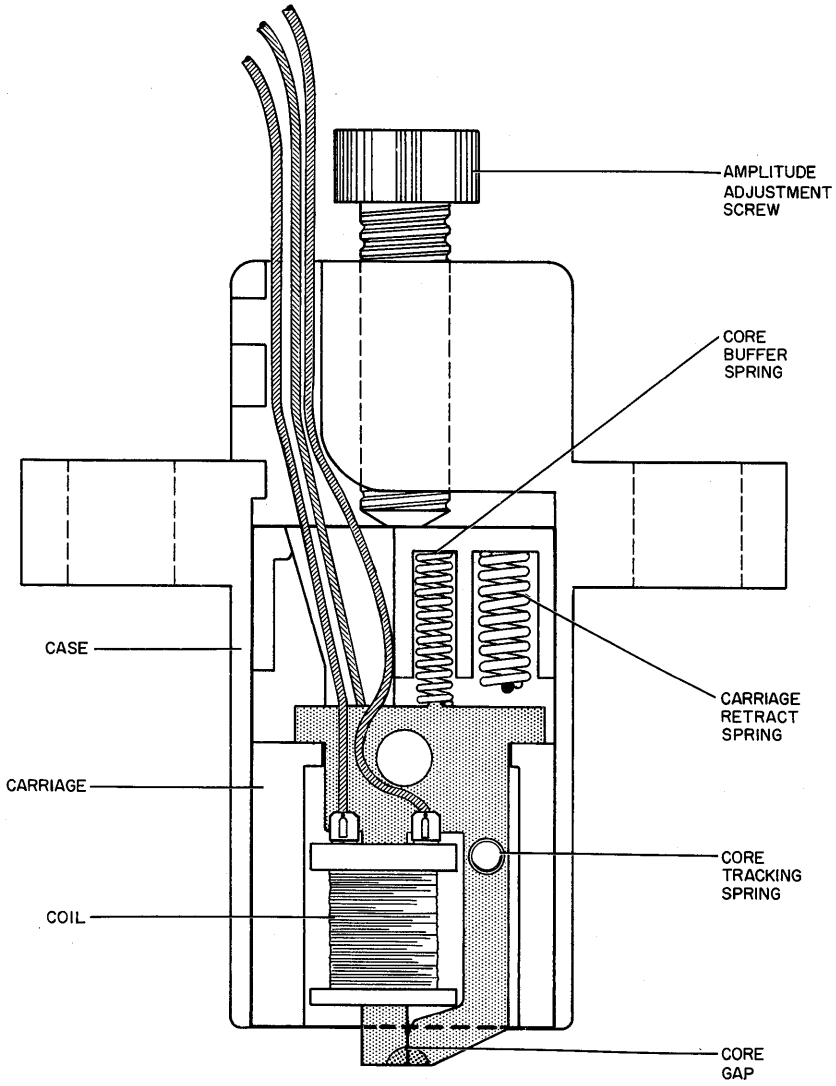


Figure 1–9. Aluminum Head Assembly, Component Location

tion. The upper section reflects main drum (MIXD, LOG, TD, RD, AM-A, and AM-B) operations, and the lower section reflects auxiliary drum (AM-C through AM-AM-H) operations. Each section, in turn, consists of several panel sections which contain various neon and incandescent lamp indicators, a selector knob, pushbuttons, and lever mode switches. Labels on each panel section indicate the functions of controls and indicators therein contained. Discussions pertaining to each control and indicator on this module may be found in 3-152-0, *Maintenance Techniques and Procedures for Drum System of* AN/FSQ-7 *Combat Direction Central and AN/FSQ-8 Combat Control Central.*

2.6 UNITS 29 and 46

The MCD units 29 and 46 contain all the relay networks required to supply power to the electronic and electric circuits (motors) of the Drum System. Unit 29 is directly connected to the main drums and unit 46 to the auxiliary drums. Though these units form part of the Power System, their direct relationship with the Drum System, particularly with the drum motor control circuits, points the need for coverage thereof in this manual (Part 2, Ch 1). Other descriptions of these units appear in 3-82-0, *Theory of Operation of Power Supply System for AN/FSQ-7 Combat Direction Central and AN/FSQ-8 Combat Control Central.*

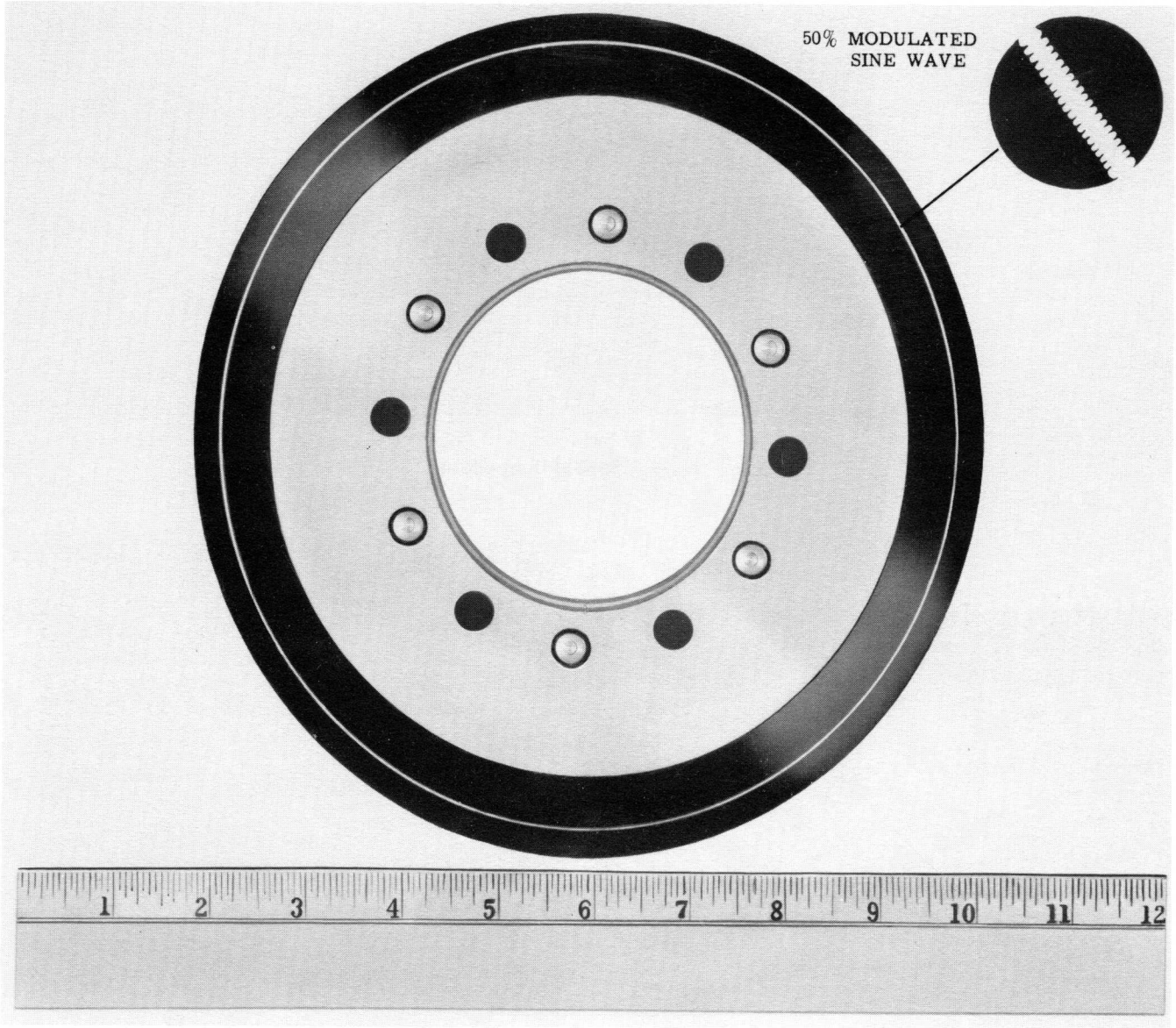


Figure 1–10. Optical Timing Disc

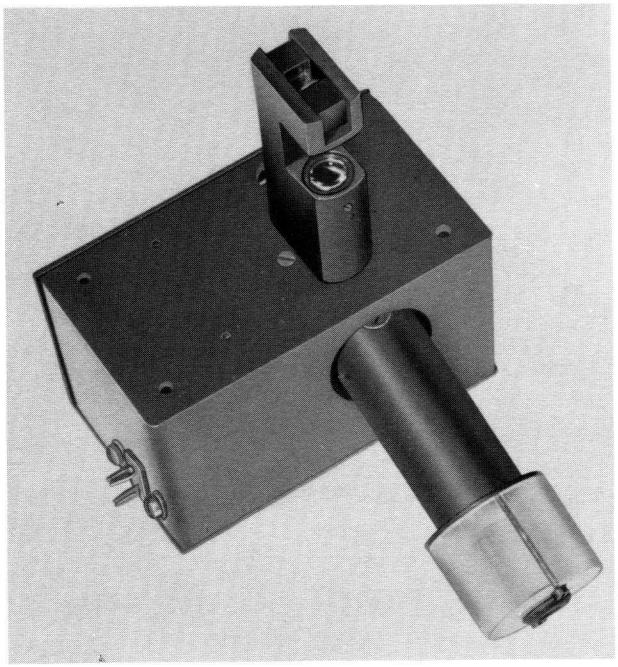


Figure 1–11. Optical Transducer

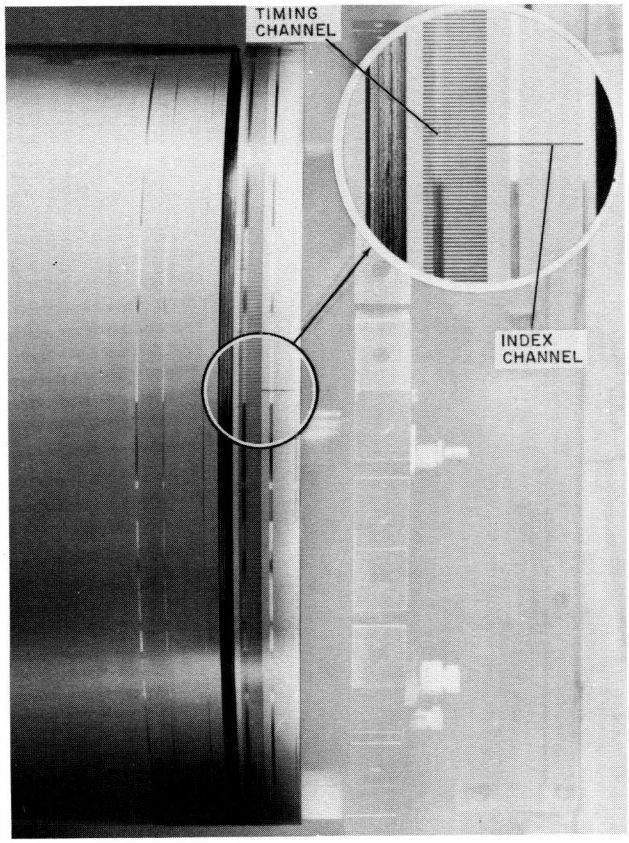


Figure 1–12. Etched Timing Disc

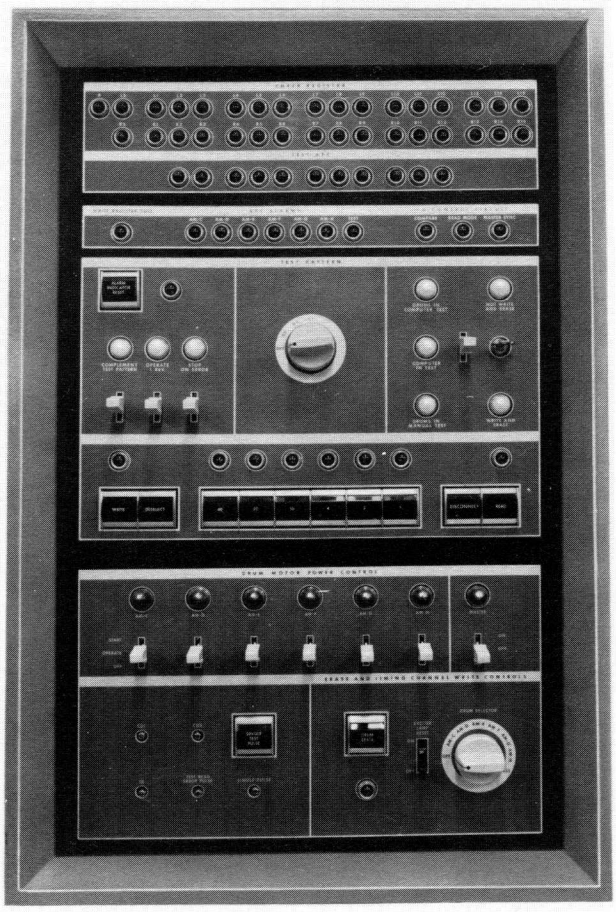
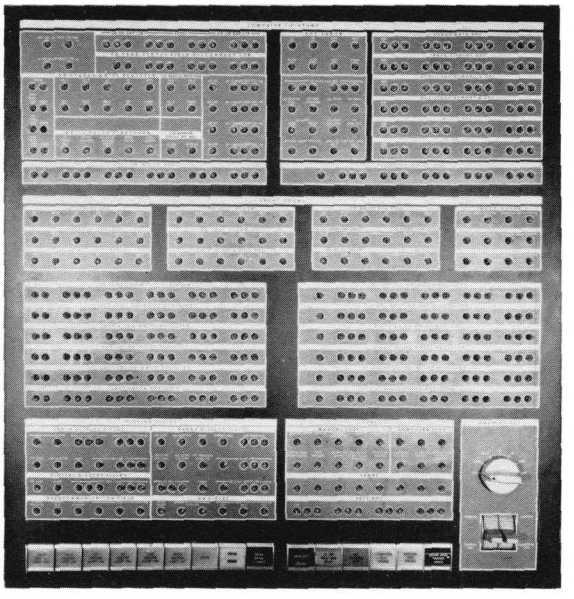
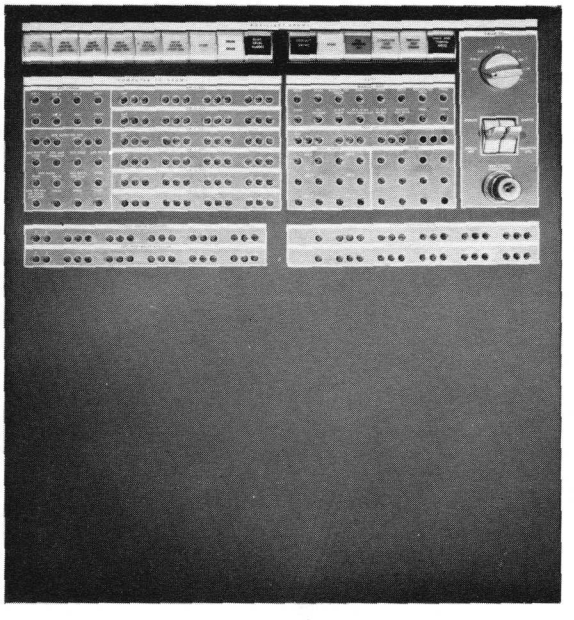


Figure 1–13. Auxiliary Drums Test Door



UPPER PANEL SECTION – MAIN DRUMS



LOWER PANEL SECTION – AUXILIARY DRUMS

Figure 1–14. Module E, Duplex Maintenance Console

CHAPTER 3
DRUM SYSTEM FUNCTIONAL DESCRIPTION

3.1 GENERAL

This chapter defines the purpose of the Drum System, its overall function, and its interrelationship with the Input, Output, Display, and Central Computer Systems. This introductory presentation is equally suitable for the AN/FSQ-7 Combat Direction Central or the AN/FSQ-8 Combat Control Central because the Drum System in either of the two equipments performs upon the same technical principles. Nevertheless, the two equipments differ in tactical application and the difference is reflected in the Drum System. Specifically, the Q-8 equipment does not process radar data; this means that the LRI, GFI, and RD fields are not operative in the Drum System installed in Combat Control (CC) sites. Consequently, functional description of the Drum System will be undertaken through three different clarifying aspects: first, basic purpose and overall function; second, system interrelationship in the AN/FSQ-7 equipment; third, system interrelationship in the AN/FSQ-8 equipment. The basic purpose and overall function is covered in paragraph 3.2 and AN/FSQ-7 Drum System interrelationships in paragraph 3.3. Drum System interrelationships in the AN/FSQ-8 equipment are covered in Part 6.

3.2 OVERALL DESCRIPTION

The purpose of the Drum System is to store tactical data being transferred from the Input System to the Central Computer, or from the Central Computer to the Output or Display Systems. In addition, the Drum System provides auxiliary memory space for tabular data and program information from the Central Computer. In the process of data transfers, the Drum System acts as a time buffer stage which allows the system of destination to receive the data at its own pace. For example, tactical data from the Input System arrives in large quantities and at random times. The drums store this data in an orderly manner and have it available for rapid transfer to the Central Computer. Data processed by the Central Computer is stored in the drums at a rapid pace and is delivered to the Output or the Display System at a slower pace compatible with the operation of these systems. The Drum System being a time buffer, storage device performs no computations; i.e., data enters and leaves the system without alteration.

The time required to obtain information stored, or access time of a drum, averages about 10 ms. This means that information desired may be found on a rotating drum either immediately or it may take up to 20 ms (one full drum revolution) to be found. The average access time is, thus, 10 ms. Taking various storage devices in the equipment on a comparative basis, the Central Computer core memory access time of 6 usec is shorter than the drum access time. However, drum access time is considerably short considering the access time of other IO (input-output) devices such as card and tape machines.

Another important function of the Drum System is the generation of timing information used by the Input, Output, and Display Systems. This timing information provides the systems with the synchronization required for their internal operations and for the respective data transfer to or from the Drum System. The Central Computer and Drum Systems have their own independent timing control. Through timing control, each drum rotating at the normal speed of 2,914 rpm can accept successive data transfers at the rate of one transfer every 10 usec.

Drum System circuits are classified in two major groups: circuits related to data transfers from the Central Computer are CD (computer-drum) circuits; and circuits related to transfers with the Input, Output, and Display Systems are OD (other-than-computer-drum) circuits. These two groups of circuits constitute the CD and OD sides of each drum and the operations performed are accordingly called CD and OD operations.

Each of the 12 drums in a system is divided into logical divisions known as fields. Each field, except track display (TD) and radar data (RD) fields, contains 2,048 axially oriented registers, which are numbered consecutively about the circumference of the drum. One 33-bit information word can be stored in each register. All but one of the magnetic drums contain six fields named for the type of data they store. The RD drum has nine fields.

Magnetic drums are named for the fields they contain. (Refer to table 1–1.) The LOG and MIXD drums are the only magnetic drums which contain more than one type of field. The names LOG and MIXD were evolved in the following manner: The letter L is the first letter of the long-range radar input field name; O is the first letter of the output buffer field name; and G is the first letter of the gap-filler input field name. Simi-

larly, M in MIXD is the first letter of the manual input field name; I is the first letter of the intercommunication field name; X is the first letter in the abbreviation of the crosstelling field name; and D is the first letter in the digital display field name. All other magnetic drums contain only one type of field; each drum is named for the particular type field that it contains.

Circuits are built into the Drum System to provide for rapid detection of Drum System malfunctions by allowing automatic testing by Central Computer System programs. Additional circuits permit testing to be performed under manual control. These circuits allow Drum System tests to be performed with the Drum System disconnected from the other systems of the Combat Direction Central. As a result, they serve as a valuable aid in installation as well as to maintenance.

Drum System operations are performed to rigorous reliability standards. Many self-checking circuits are included which reduce the time required to isolate the cause of faulty operation. Should faulty operation be produced by component failure, alarms and indicating circuits distributed throughout the Drum System would facilitate rapid detection and location of the failure.

Every Q-7 (or Q-8) equipment contains two Drum Systems and two Central Computer Systems (duplex system). One Drum and Central Computer System combination actively processes and transfers data. The other combination is in a standby state. When maintenance is to be performed on the active combination, the functions of the active Drum and Central Computer Systems are switched to the standby systems. In order to shorten the data-transfer time, intercommunication is maintained between active and standby equipment at all times. Intercommunication between Central Computer Systems is also used to enable the standby Central Computer System to check the operation of the active Central Computer System. The active Central Computer System constantly generates intercommunication data for transfer to the standby system. The circuits between computer and drums (CD) in the active Drum System

TABLE 1–1. MAGNETIC DRUM AND FIELD DESIGNATIONS

DRUM DESIGNATION	DRUM ABBREVIATION	FIELD TYPE AND QUANTITY	FIELD ABBREVIATION
LOG	None	Long-range radar input (2)	LRI 1 and 2
		Output buffer (3)	OB 1, 2, 3
		Gap-filler input (1)	GFI
MIXD	None	Manual input (1)	MI
		Intercommunication (1)	IC
		Crosstelling (1)	XTL
		Spare crosstelling (1)	SP XTL
		Digital display (1)	DD
		Spare aux memory (1)	SP AM
Aux memory A	AM-A	Aux memory (6)	AM-A 1 to 6
Aux memory B	AM-B	Aux memory (6)	AM-B 7 to 12
Aux memory C	AM-C	Aux memory (6)	AM-C 13 to 18
Aux memory D	AM-D	Aux memory (6)	AM-D 19 to 24
Aux memory E	AM-E	Aux memory (6)	AM-E 25 to 30
Aux memory F	AM-F	Aux memory (6)	AM-F 31 to 36
Aux memory G	AM-G	Aux memory (6)	AM-G 37 to 42
Aux memory H	AM-H	Aux memory (6)	AM-H 43 to 48
Radar data	RD	Radar data (9)	RD 1 to 9
Track display	TD	Track display	TD 1 to 6

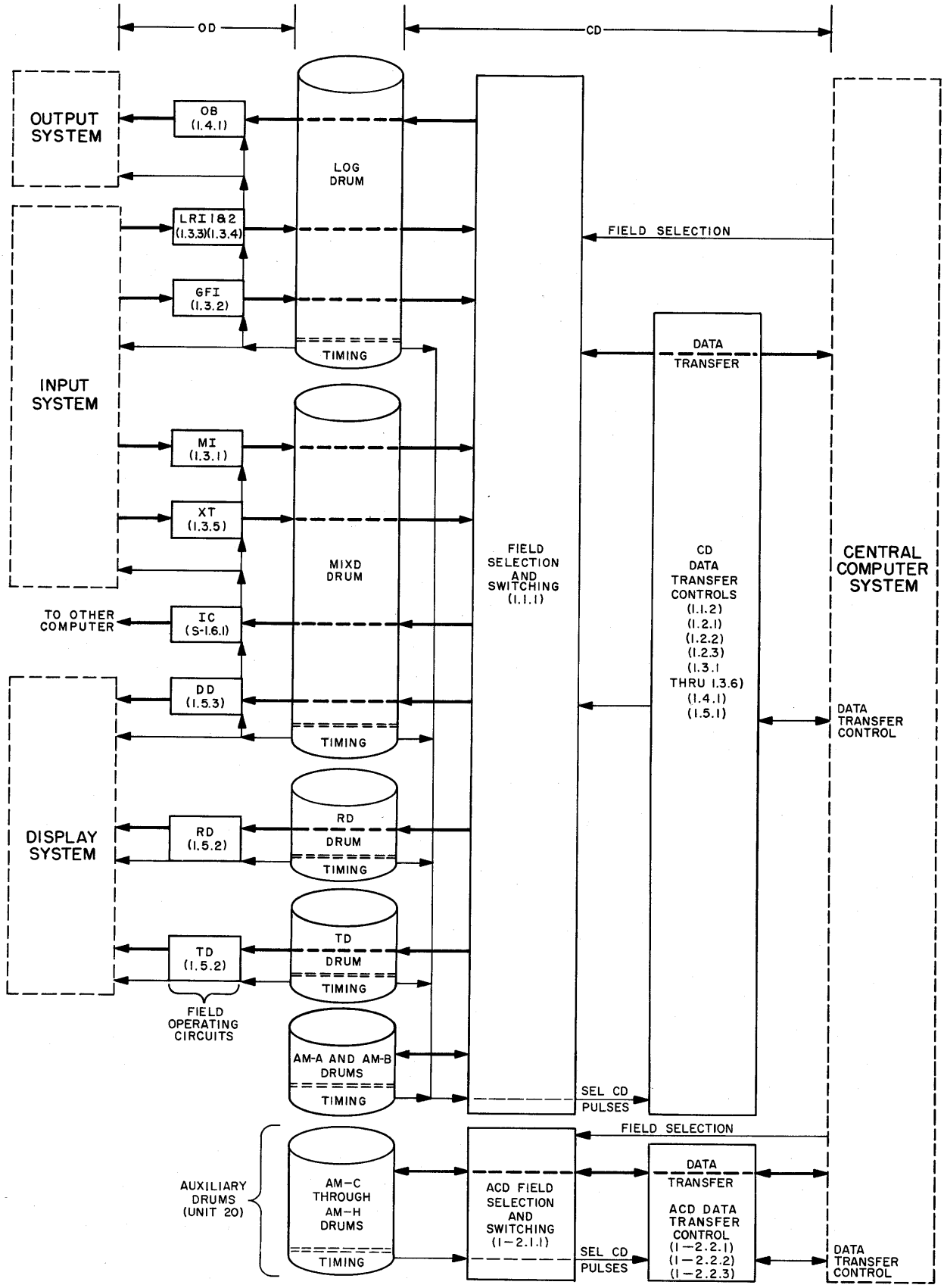


Figure 1–15. Drum System Operational Block Diagram

transfer this intercommunication data from the active Central Computer System to the magnetic drums so that it may be stored and transferred to the standby Central Computer System. The transfer from the magnetic drum to the standby Central Computer System is through the CD circuits of the standby Drum System.

3.3 THE DRUM SYSTEM IN A COMBAT DIRECTION CENTRAL

The AN/FSQ-7 Combat Direction Central equipment contains all facilities to receive, calculate, and display radar data as well as other tactical data required for air defense. Since the Drum System serves as an operating link between all other data-handling systems of the equipment, all types of raw and processed data flow through the drums. This transfer function interrelates the Drum System with the Central Computer, Input, Output, and Display Systems as indicated in figure 1–15. An effort has been made in this illustration to indicate the individual data paths on the OD side of the drums, as opposed to a common path for all transfers on the CD side. This condition allows the drums to effect data transfers with the Input, Output, and Display Systems simultaneously and at times suitable to the operation of these systems. On the other hand, transfers to and from drums and Central Computer must be scheduled by a control program so that only one transfer can take place at any given time. Intercommunication (IC) transfers between Drum System in areas A and B are also subject to program scheduling in the area effecting the transfer.

Paragraphs 3.3.1 through 3.3.10 contain brief descriptions of the various circuit areas of the Drum System operating in an AN/FSQ-7 Combat Direction Central.

3.3.1 CD Field Selection and Switching Circuits

The field-selection and switching circuits (figs. 1–5, logic drawings 1.1.1 and 1-2.1.1) perform two functions required for an information exchange between the drum fields and the Central Computer. It activates the field designated by the Central Computer and that field only, and it conditions the timing and control circuits of the drum in which the field is located. These functions are accomplished by the decoding circuits and the diode switching circuits.

3.3.2 Drum Timing Circuits

The drum timing circuits, logic drawings 1.1.2 and 1-2.1.2, time the operations of the Drum System and of all other systems of the AN/FSQ-7 with which the drums exchange information, except the Central Computer. Each drum generates timing pulses for itself. The timing pulses are used to initiate and to effect the operations which cause the Drum System circuits to write and to read. They are also used to step the various counters used in the Drum System circuits.

3.3.3 Read-Write Control Circuits

The key Drum System circuits in any information exchange with the Central Computer are the read-write control circuits, shown on logic drawings 1.2.1 and 1-2.2.1. The Central Computer sends transfer control instructions into this circuit, where they are combined with drum timing pulses and field-selection levels to produce drum-transfer-control levels. These levels activate the Drum System circuits which select the field registers to or from which information will be transferred, and also control the transfer.

3.3.4 Angular-Position-Counter Circuits

The angular-position-counter (APC) circuits, logic drawings 1.2.3 and 1-2.2.3, are used in conjunction with the read-write control circuits to determine explicitly the field registers to or from which data is to be transferred. When the Central Computer designates, by number, the register or registers with which the data exchange is required, the angular position counter counts the drum registers passing under the read-write heads. When the number so counted compares with the Central Computer designation, the data transfer is performed. This method of register selection, known as address control, is used in CD writing and reading from the auxiliary memory fields, from the intercommunication field, and from the display field.

3.3.5 Read-Write Circuits

The read-write circuit consists of two separate groups of circuits: the read circuits (shown on logic 1.2.2) and the write circuits (logic 1.2.1). The write circuit is capable of placing, at one instant of time, a complete information word (33 bits) on the drum surface. Only one write circuit is employed on the CD side of the drums. A separate write circuit for each of the input fields is employed on the OD side of the drums. The read circuits are the means by which a complete information word (33 bits) is read at one instant of time from the drums. Only one read circuit is employed on the CD side of the drums. On the OD side of the drums, separate read circuits are employed for the OB fields circuits and for the intercommunication field circuits. Two read circuits are used in the display field circuit.

3.3.6 Input-Fields Operate Circuits

Four data types (LRI, MI, GFI, and XTL) comprise the input to the Combat Direction Central. Information is received by the input-fields operate circuits, logic drawings 1.3.1 through 1.3.6, at different rates and at random intervals. The input-fields operate circuits store this data on the drums for later transfer to the Central Computer. The transfer from the Drum

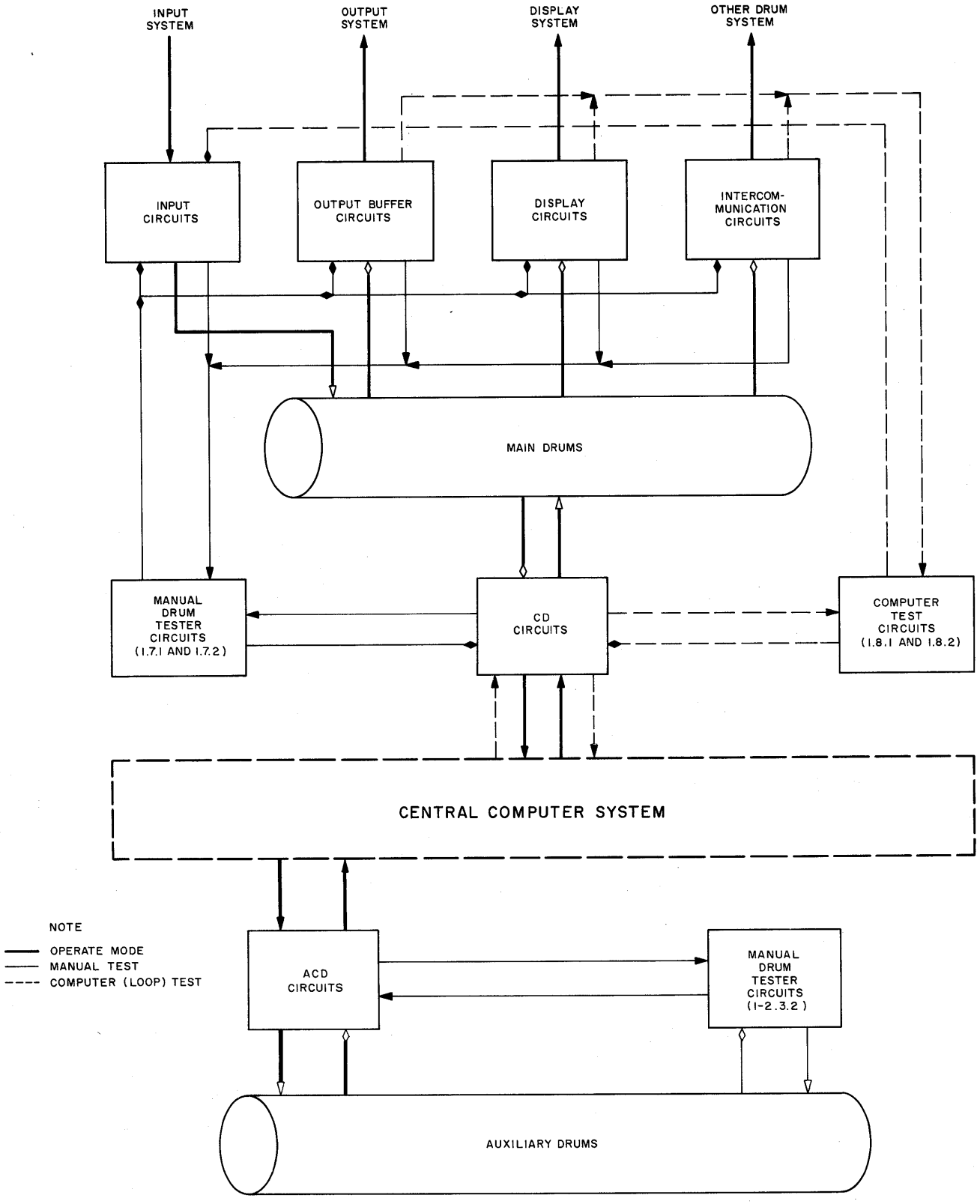


Figure 1–16. Drum System Test Operation, Block Diagram

System to the Central Computer System is performed at Central Computer System command.

These circuits employ a method of register selection, the criterion for which is the full or empty status of the register. Under appropriate control conditions, information is automatically transferred into empty registers by the Input System and is removed from full registers. Upon removal, the data is sent to the Central Computer circuits. This method of transfer, known as status-controlled transfer, is used by all input-fields operate circuits.

There are six separate input-fields operate circuits, each handling a particular type of input data and associated with one of the six input fields on the main drums. These fields, in summary, are: the MI, the GFI, LRI 1, LRI 2, the XTL, and SP XTL fields (table 1–1).

3.3.7 Output-Buffer-Fields Operate Circuits

The Central Computer System develops large quantities of tactical data for transfer to the Output System. This transfer is performed by the OB-fields operate circuits, logic drawing 1.4.1, using the status transfer method outlines in 2.2.7. Since the operations of the Central Computer are considerably faster than the operation of the Output System, the transfer of tactical data is regulated by the OB-fields operate circuits to provide data for the Output System at a rate compatible with Output System operations.

3.3.8 Display-Fields Operate Circuits

The display-fields operate circuits, logic drawings 1.5.2 and 1.5.3, take display data stored on the magnetic drums by the CD circuits and transfer it to the Display System. Like output data, display data is generated at speeds that are too great to be handled in the Display System. The Drum System, therefore, reduces the rate of transfer of display data to the Display System.

The display-fields operate circuit consists of three distinct areas. The first is used for reading digital display information from the drums and into the Display System. The second and third are used for consecutively reading track display information and radar display information from the drums into the Display System.

3.3.9 Intercommunication Field Circuits

The intercommunication field circuits, logic drawings S-1.6.1, take intercommunication data stored on the magnetic drums by the CD circuits in one Drum System and transfer it to the alternate Drum System. This transfer takes place under the control of the alternate Drum System. The intercommunication field thus provides mutual contact between areas A and B of the duplex equipment.

3.3.10 Test Circuits

Drum System test circuits are of two types: loop test and manual test. The computer (loop) test circuit (fig. 1–16 logic drawings 1.8.1 and 1.8.2) provide the Central Computer System with a means of performing tests on the Drum System to detect alteration of data. When the Drum System is in an operate mode, the Central Computer System exchanges information with the magnetic drums via the CD circuits only. However, when the Drum System is in a computer-test mode, the computer-test circuits provide the Central Computer System with access to OD circuits. The additional data paths made possible are shown by dashed lines on the figure.

The manual-test circuits (logic drawing 1.7.2) enable maintenance personnel to exercise control over Drum System performance in isolation from other associated systems. Manual-test circuits have facilities for individual checking of the storage and control operations of the CD and OD circuits (shown by the light lines of fig. 1–16). In addition, the manual-test circuits contain manually operated controls that energize and de-energize the Drum System and lamps that indicate the condition of various Drum System circuits.

PART 2
DRUM SYSTEM BASIC FUNCTIONS

CHAPTER 1
INTRODUCTION

To transfer data from source to destination, the Drum System performs three sequential actions. It RECEIVES – STORES – DELIVERS. These actions are associated with all data transfers regardless of the points of source and destination.

On the other hand, considering source and destination, the following cases of data transfer result:

a. The Central Computer is both the point of source and destination. These transfers are handled by the eight auxiliary drums.

b. The Input System is the source and the Central Computer System is the point of destination. These transfers are handled by the LRI and GFI fields of the LOG drum, and the MI and XTL fields of the MIXD drum.

c. The Central Computer System is the source and the Output System is the point of destination. These transfers are handled by the OB fields in the LOG drum.

d. The Central Computer System is the source and the Display System is the point of destination. These transfers are handled by the TD and RD drums as well as by the DD field of the MIXD drum.

e. The Central Computer System in the active area of the equipment is the source and the Central Computer System in the standby area is the point of destination. These data transfers are handled by the IC field of the MIXD drum.

Receiving, storing, and delivering from a specific source to a specific destination involve six basic functions of the Drum System: power control; magnetic writing, reading, and erasing; timing; field selection; field switching; and CD data transfer control. These functions are briefly reviewed in the following paragraphs.

The characteristics of a drum rotor demand considerable initial torque from the driving motor. To develop initial torque, a motor places heavy drain upon line current which, in turn, rules out the practicability of simultaneous starts. Chapter 2 discusses the relay network controlling sequential starting of the motors in the Drum System.

The 12 drums in the Drum System are magnetic storage devices. Storage facilities thereby provided imply that information received is recorded and is made available for delivery to destination at the proper time. The recording process is called magnetic writing; making data available is the process of magnetic reading. Eliminating, or cleaning, magnetic storage from a drum constitutes the process of magnetic erasing. This subject is presented in Chapter 3.

Each of the drums in the system generates its own timing signals. In the auxiliary drums, the use of timing signals is restricted to the control of local operations of each drum. However, timing from each of the other drums serves to control, not only local operation of the drum, but also the operations of the system or systems (Input, Output, and Display) related to the drum. The Central Computer and Drum Systems have individual and isolated timing control.

Examining the different cases of data transfer through the Drum System, it will be noticed that, in each case, the Central Computer System is the source or destination of each transfer. This condition indicates that computer-drum (CD) exchanges represent the entire traffic of data through the system. Such concentrated activity requires that CD transfers in either direction be made one at a time. Field selection (Ch 5) is initiated by the Central Computer to isolate one drum field from the 75 drum fields available. The field selected is properly energized to write on or read from the drum, according to the direction of the transfer.

Field switching is an allied function of field selection. Diode switches acting in check-valve fashion place the selected field in direct communication with the circuits which control the write or read operation.

Also allied to field selection is the control of data

transfer from drums to Central Computer or vice-versa. This function includes the reception of the Central Computer instruction to start writing or reading, the activation of address control or status control which determines the method of transfer, and the release of data to be written on or to be read from the selected drum field. Chapter 7 describes CD data transfer control.

CHAPTER 2
DRUM MOTOR POWER CONTROL

2.1 GENERAL

The operations of the Drum System discussed in this manual are based on the assumption that each corresponding drum is rotating. This chapter describes the operation of the drum motor circuits supplying power to the drum motors that drive the drum rotors. The mounting of drum motors and the supply circuits which energize them are identical in all drum assemblies.

Drum motors may be energized in either of two ways: by means of automatic sequential cycling or individually. In either case, there is a need for an understanding of the manual operation of associated switches to implement the discussion of circuit performance.

Drum motors are numbered 1 through 6 in accordance with the order in which they are energized during sequential cycling. For the main drums, the order is as follows: motor 1, AM-B drum; motor 2, LOG drum; motor 3, RD drum; motor 4, TD drum; motor 5, AM-A drum; motor 6, MIXD drum. For the auxiliary drum, the order is as follows: motor 1, AM-G drum; motor 2, AM-H drum; motor 3, AM-E drum; motor 4, AM-F drum; motor 5, AM-C drum; motor 6, AM-D drum. Note that in Combat Control Centrals utilizing a second TD drum in place of the R_{rl} drum, this second TD drum is energized in the order normally assigned to the RD drum.

Whether the drum motors are energized automatically, by means of sequential cycling, or individually by means of test door switch manipulation, the effects of large current surges have been considered. To minimize these effects, relay networks have been employed which provide for the gradual activation of each drum motor. The same relay networks furnish the sequential cycling pattern utilized during automatic energizing. This pattern is accomplished through the use of time delay relays, which are adjustable from 1 to 10 seconds. The normal time involved in the sequential cycling of drum motors is approximately 6 seconds per drum.

2.2 DRUM-MOTOR START CIRCUIT

Energizing of the drum motors is determined by the presence of 208V, 3-phase, 60-cps power in the start circuits of units 29 and 46 (fig. 2–1). This is effected by the manual setting of circuit breakers (CB) CB1 through CB7. The CB's are numbered to correspond with the number of their respective drum motors. For instance, CB1 is in the circuit of motor 1, CB2 is in the circuit of motor 2, and so on. CB7 is used to initiate the energizing of the motor control circuit (par. 2.3). Each CB is provided with a thermal and a magnetic overload device that protects the motor windings from short circuits and prolonged overload conditions in the power supply.

When CB7 is closed, time delay relay coil TR7 becomes energized and the corresponding contacts close. This initiates the activation of the drum-motor control circuit. With the closing of each of the drum motor CB's, line power is advanced to the magnetic contactors. Operation of the magnetic contactors is dependent upon the state of the corresponding control circuit. When this circuit is energized, the contactors are closed and power is applied to the drum motors.

An auxiliary switch is connected to the poles of each of the CB's. This switch contains one normally open set of contacts (contacts A). When a CB is closed, the corresponding auxiliary switch A contacts also close. Should an overload or a short circuit occur during motor operations, the CB automatically springs to the OFF position; the auxiliary switch A contacts open. These conditions are reflected in the control circuit, and the associated drum motor is de-energized. After a CB opens, it is necessary to manually reset the CB to establish power connection.

2.3 SEQUENTIAL ENERGIZING, CONTROL CIRCUIT ANALYSIS

The drum-motor control circuit (fig. 2–2) serves to provide the required voltage cycling for energizing each drum motor. The —48V needed to activate the circuit is furnished through the contacts of time-delay relay TR7, which is energized by the activation of CB7 in the corresponding drum-motor start circuit (par. 2.2). The following circuit analysis is based on the assumption that TR7 is energized. Because TR7 is an undervoltage relay, its contacts will open, stopping motor operation when the line voltage applied to the motors decreases below a selected value for a set period of time. This period is adjustable between 1 and 10 seconds. For example, if the delay is for 8 seconds, the undervoltage condition must remain for 8 continuous seconds before the relay contacts open.

The sequential energizing process is initiated by placing the individual drum motor power control

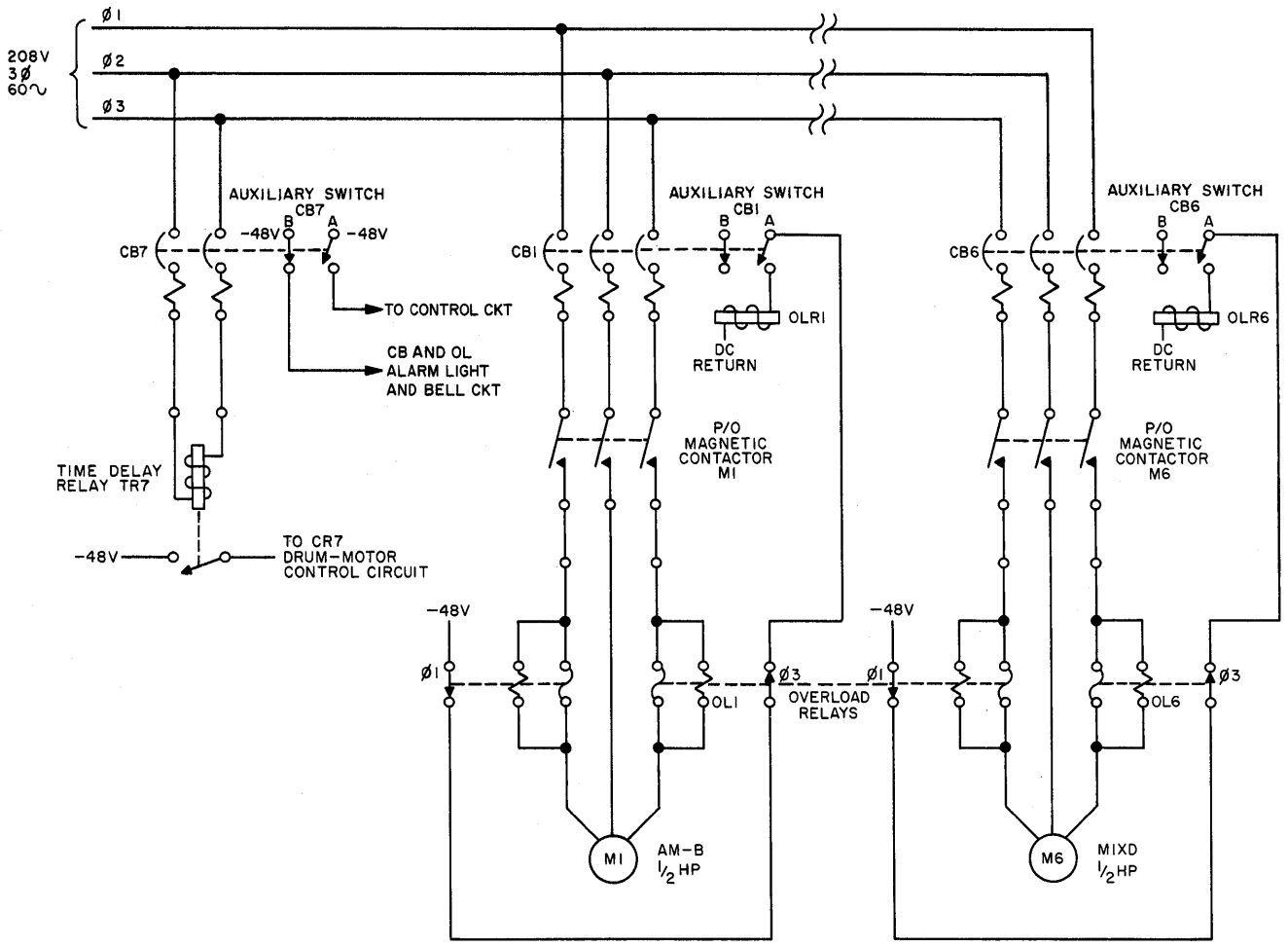


Figure 2–1. Drum-Motor Start Circuit, Simplified Schematic Diagram

switches to the OPERATE position, and the MASTER ON-OFF switch, S26, on module 21L (module 20F for auxiliary drums) to the ON position. With TR7 energized —48V energize control relays CR7-1 and CR7-2; with S26 closed, —48V energize control relay CR8. Through the closed contacts of relays CR7-1 and CR8, a path is completed to energize relay AM-B M1, which causes the magnetic contactor to close and energize motor 1. The above —48V path is formed through the following: closed contacts of energized CR7-1 and CR8 relays; closed contacts of de-energized CR1; closed contacts of AM-B OFF switch; closed contacts of overload relay OLR1.

The closing of relay contacts CR7-1 and CR8 contributes to automatic motor sequencing in other respects. Through these contacts, —48V is applied to TR1. Time-delay relay TR1 is similar in operation to TR7 in that its coil requires from 1 to 10 seconds to become energized. When TR1 becomes energized, the corresponding contacts close, applying —48V to relay CR1.

Control relay CR1 has two sets of contacts, one normally closed (A contacts), and one normally open (B contacts). When CR1 is energized, the A contacts open, thus interrupting the original —48V path to relay AM-B M1. However, figure 2–2 indicates that the energizing of AM-B M1, in addition to causing the drum motor to start, serves to close auxiliary contacts in the control circuit. These contacts also carry —48V power. Therefore, the relay is held energized through its own contacts.

Closed CR1 B contacts determine the energizing of the motor 2 control circuit. Consequently, the time between the energizing of motor 1 and the energizing of motor 2 is identical to the time setting of TR1. This is because —48V reach CR1 only after TR1 has been energized. This energizing process is repeated until all six motors have been energized.

The drum-motor control circuits contain overload relays which serve as additional protective devices. These relays, OLR1 through OLR6, are connected in series with each respective set of Ø1 and 3 a-c overload

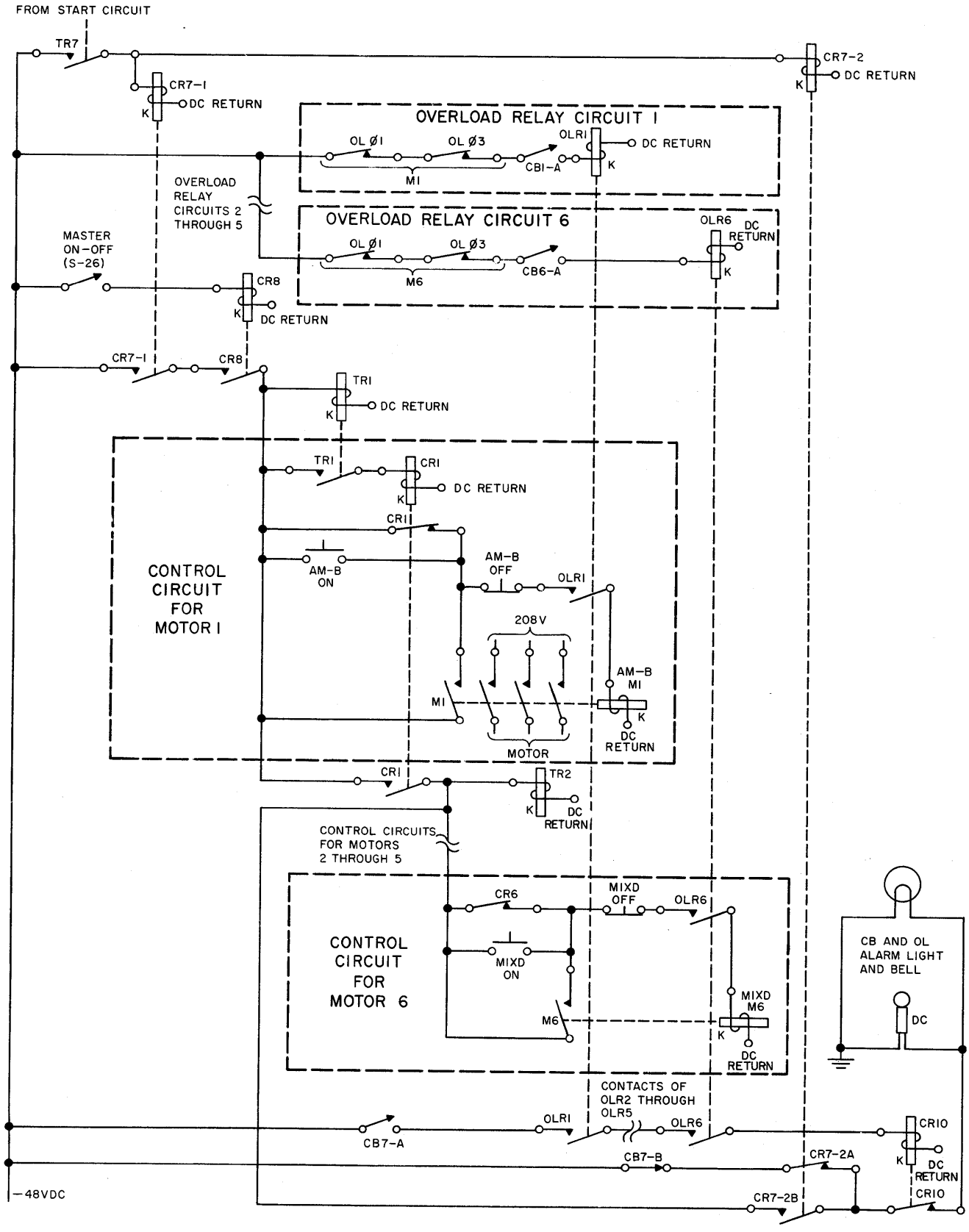


Figure 2–2. Drum-Motor Control Circuit, Simplified Schematic Diagram

relay contacts. The Ø1 and Ø3 relay coils, which are physically connected in the drum-motor power lines, are energized in cases of rapid current changes (such as would be produced by a short circuit). These radical changes are reflected in the control circuit by the opening of contacts Ø1 and Ø3. This, in turn, de-energizes overload relay R1, thus, removing energizing voltage from AM-B M1. At this time magnetic contactors M1 are opened and power is removed from the drum motor.

An alarm circuit included in the drum-motor control circuit indicates the opening of a circuit breaker, de-energizing of an overload relay, or an all-motors off condition. Before CB7 is closed, —48V are applied to the CB and OL alarm light and bell through auxiliary switch B contacts and normally closed CR7-2A and CR10 contacts. When CB7 is closed, these contacts open, removing —48V from the bell and light.

When TR7 contacts are closed, CR7-2 is energized; the A contacts open and the B contacts close. At the end of the delay between the starting of the first and second drum motors, CR1 contacts close. If CR10 is de-energized at that time, the alarm light and bell receive —48V. Relay CR10 is de-energized only when CB7 is open or if one of the overload relays becomes de-energized.

2.4 INDIVIDUAL ENERGIZING, CONTROL CIRCUIT ANALYSIS

The operation of the drum-motor control circuits (fig. 2–2) also allows each drum to be individually energized.

This is accomplished through the manipulation of each corresponding START-OFF switch on the test door of module L (module 20F for auxiliary drums). This switch is a 3-position lever switch containing an upper (START) position, a middle (OPERATE) position, and a lower (OFF) position. In the OPERATE position (automatic start), the OFF contacts are closed and the START contacts are open. When the switch is set to the START position from the OPERATE position, both the START and OFF contacts are closed. Conversely, when the switch is set from the OPERATE position to the OFF position, both the START and OFF contacts are open.

Initially, the START-OFF switch must be in the OFF position so as to allow the —48V power to be present without activating the drum-motor control circuit. This supply voltage is made available by setting the MASTER ON-OFF switch to the lower (ON) position. After a predetermined period of time (approximately 6 seconds per drum) the START-OFF switch may be placed to the upper (START) position. Activation of the corresponding control circuit is immediate and takes place as described in paragraph 2.2. It should be noted that all drums can be manually started at one time. This action, however, results in excessive current drain and will cause associated circuit breakers to trip,

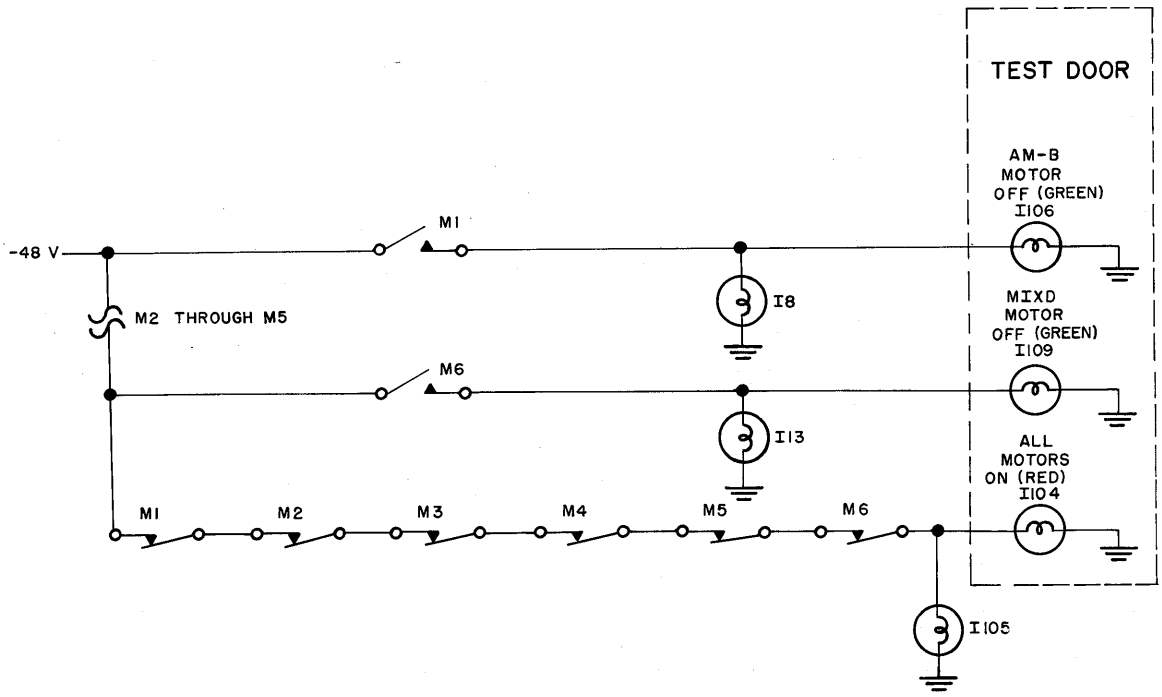


Figure 2–3. Main-Drum Motor Control Indicator Circuit, Simplified Diagram

thereby de-energizing the motors. Therefore, a pause is required between successive activations of START-OFF switches.

2.5 DRUM MOTOR INDICATOR LAMPS, CIRCUIT ANALYSIS

Indicator lamps that display the operating condition of the drum motors are located on the test door, module 21L (fig. 1–3) and in the drum-motor control circuit. Figure 2–3 is a simplified schematic diagram of the indicator lamp circuits. If any magnetic contactor opens during operation, its normally open and normally closed contacts reverse their states, and a d-c path is completed between the —48V power supply and the MOTOR OFF lamps associated with the motor which has stopped. When all motors are energized, the MASTER lamp on module 21L lights.

CHAPTER 3

THEORY OF DRUM WRITING, READING, AND ERASING

This chapter describes the magnetic process of writing, reading, and erasing on the nickel-cobalt surface of a drum. A description is also given of the manner in which the drum surface is divided, for purposes of writing and reading, into fields and registers which yield a total capacity of approximately one-half million bits of information.

3.1 MAGNETIC WRITING

The fundamental block in the magnetic write, as well as read, processes is the drum head (fig. 1–9). A drum head consists mainly of a coil wound on an inverted U-shaped laminated core. The ends of this core are held in close proximity to each other so that they form a narrow (0.0027 inch) gap. When current is applied to the coil, the core becomes magnetized and a magnetic field is developed across the gap. The lines of force in this field not only follow a straight path between the ends of the core (or north and south ends of the magnet) but also form a bulge from one core end to the other. The lines of force in the bulge constitute fringe flux which is used to magnetize, or write, on a desired area of the drum surface.

Suitable pulse recording on the drum surface is obtained by allowing a drum head to remain magnetized for 1.7 usec. The fringe flux developed by the head during this period leaves on the nickel-cobalt coating a spot with lines of force arranged in the shape of a tiny permanent magnet. This magnetized spot is called a bit. In the Drum System, drum heads write 1 bits and 0 bits. Generation of 1 and 0 bits is based on the theory of electromagnets which dictates that the direction of current in a coil determines the north and south poles of the electromagnet (fig. 2–4). Drum write heads are generally connected to follow this theory. The power source is connected to a center tap in the coil and a vacuum tube is connected at either end of the coil. At any given time in a write operation, one of the two tubes is conducting and the other is nonconducting. For example, to write a 1 bit, tube A is conducting; this causes the right-hand side of the core to become the north pole of the electromagnet, while the other end is the south pole. Accordingly, lines of force flow from north to south. To write a 0 bit, tube A is nonconducting and tube B is conducting. North and south poles of the electromagnet switch places and the lines of force accordingly switch direction.

The flux density of a recorded bit can be controlled by manual adjustment. This adjustment consists of varying the distance between the core gap and the drum surface.

The magnitude of the write current determines the amount of fringe flux and, consequently, the physical

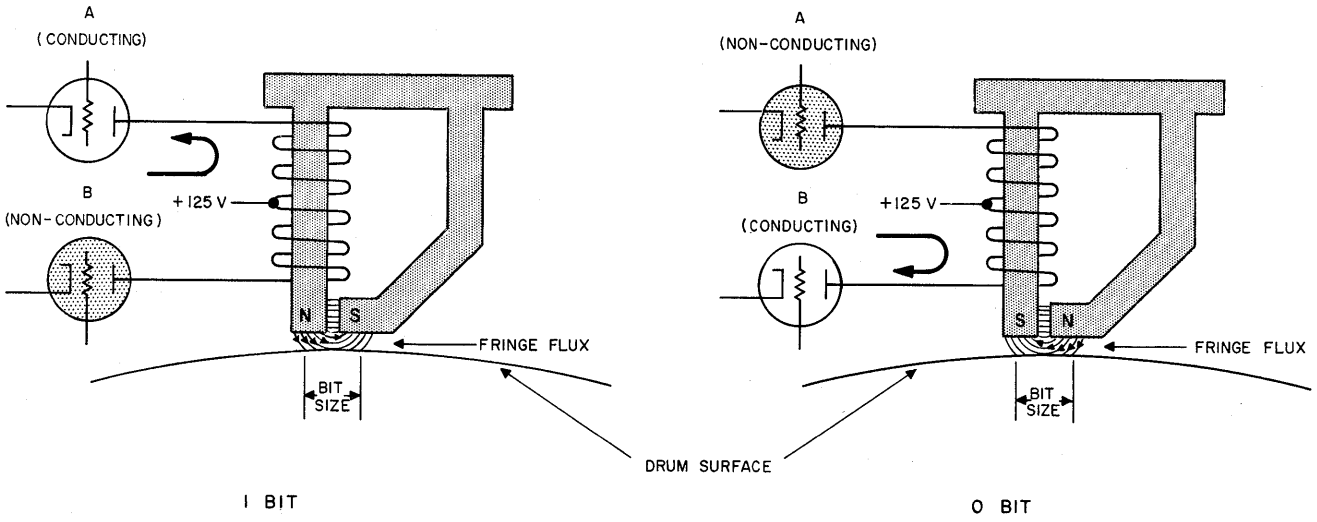


Figure 2–4. Drum-Head Write Operation

size of the recorded bit. A write current of 110 ma produces satisfactory bit saturation but is not excessively large to cause the bit to overlap with others recorded in adjacent areas. Another factor influencing bit size is the measurement of the core gap which is predetermined at the time of manufacture.

3.2 MAGNETIC READING

The magnetized spots, or bits, recorded on the drum surface during the write process serve to induce a voltage on the same drum head or any other head during the reading process. Thus, without variation to its flux density and physical size, a recorded bit can be read over and over at every drum revolution, as the bit passes under a core gap. This type of magnetic reading is called nondestructive reading.

The relationship between the flux distribution pattern written on the drum surface and the read voltage induced in the head with respect to time are illustrated in figure 2–5. Section A of the figure represents this relationship in a 1 bit; B, represents a 0 bit. Considering the 1 bit before reaching the gap at time 1, flux density and, consequently, induced voltage are zero. From time 1 to time 2, flux density and read voltage slowly build up. From time 2 to time 4, flux increases at a rapid rate; therefore, the induced voltage also undergoes a rapid increase. Between time 4 and time 6 the rate of flux change diminishes to almost no change as it goes past time 5. During this period, the read voltage induced in the head collapses and overshoots through the zero axis to its negative peak. From time 6 to time 8 flux changes rapidly and the voltage induced in the head also builds rapidly towards the zero axis. Between time 8 and time 9 the slow rate of change in the flux density is followed by a slow rate of change in the voltage induced in the head. At time 9, the magnetized spot has concluded its passage under the core gap. The process undergone by a 0 bit is identical and opposite to that of a 1 bit. This condition results from the reversal in magnetic polarity and flux direction as previously discussed. One- and 0-bit signals read by a drum head are applied to a drum amplifier (DA) circuit. For detailed description of DA performance refer to 3-3-0, *Special Circuits for AN/FSQ-7 Combat Direction Central and AN/FSQ-8 Combat Control Central.*

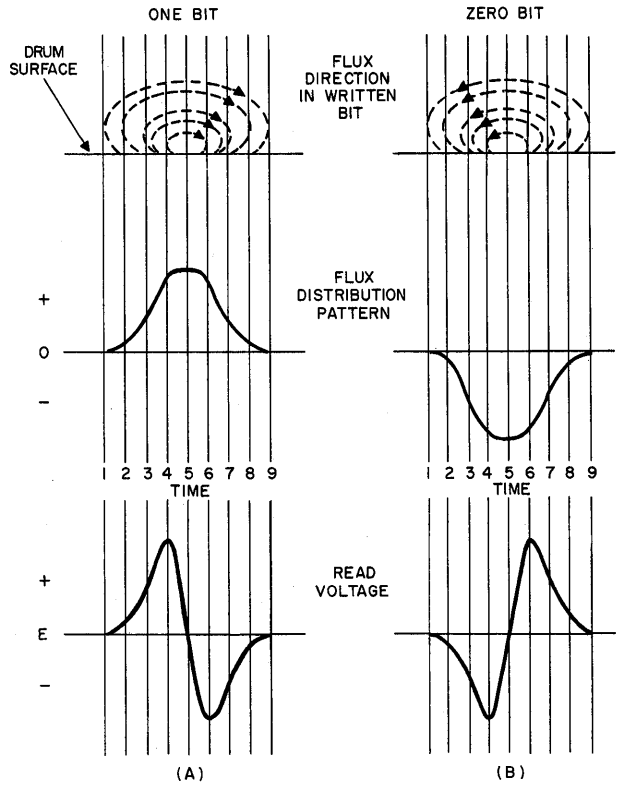


Figure 2–5. Flux Distribution – Read Waveforms Relationship

3.3 MAGNETIC ERASING

Erasing is the function of neutralizing all magnetized areas on the recording surface of drums. This function is performed to eliminate spurious signals, or magnetic noise, which appear on the drum surface as a result of such abnormal conditions as a write head touching the surface, dust, etc. There are no means of performing partial erasing on a drum. However, when information which has been recorded on a portion of the drum surface is not desired, the superimposed recording of new information effectively destroys the previous information.

Erasing of a drum is performed by recording a sinusoidal (115V, 60-cycle) signal of diminshing amplitude. This erasing signal is controlled so that its amplitude is maximum at the start of erasing and is gradually reduced until its becomes zero, or the equivalent of a d-c signal. Since the degree of magnetizing on the drum surface corresponds to the amplitude of the erasing signal, it follows that the magnetizing effect is fully neutralized when the erasing signal amplitude becomes zero.

In drums employing the optical timing disc and transducer unit, drum timing is magnetically recorded on the drum surface and is thereby eliminated at the time of erasing. Consequently, circuits are provided in these drums to cause automatic rewriting of the timing and index channels immediately after every erasing operation. However, in drums employing the new etched timing disc (par. 4.2.4), the timing and index channels are permanent and therefore not affected by erasing in the same manner. Because drum erasing can only be accomplished when the system is placed in the test mode, the

discussion of erase circuits appears in Part 5, Drum System Test Circuits.

3.4 DRUM SURFACE LAYOUT

If one were to consider the lateral surface of a drum extended over a flat surface, the area covered would be approximately 12.5 by 33.6 inches. These measurements correspond to the length and the circumference (π d) of a drum. A drum surface (fig. 2–6) is utilized so that the length of the drum axis is divided into six interleaved fields and the length of the drum circumference is divided into 2,048 registers. Paragraphs 3.3.1 and 3.3.2, which follow, respectively describe field and register layout of the drum surface.

3.4.1 Field Layout

One field on a drum is formed by the 33 adjacent information heads mounted on a drum bar. Because each head is contained within a case approximately 0.3 inch wide and the recording tip of each drum head falls directly in the center of its case, the spacing between the tips of adjacent heads is also 0.3 inch. Consequently, on a rotating drum, the 33 information heads on one drum bar originate 33 parallel tracks known as channels.

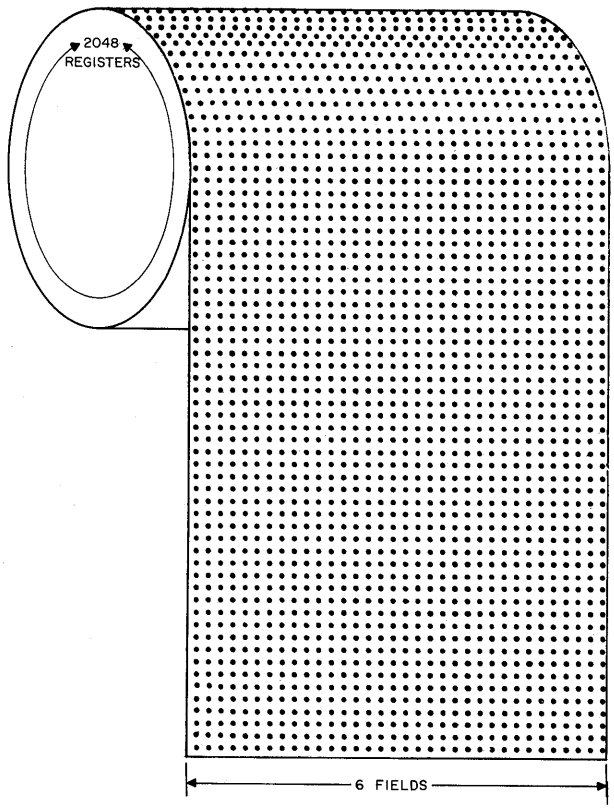


Figure 2–6. Drum Surface, Overall Layout

The aforementioned spacing between channels is utilized in the following manner. Assume a group of adjacent heads mounted on a drum (fig. 2–7) where the first of the heads is coincident with the left edge of the drum; this head formation is to be taken as a reference. If a second group of adjacent heads is mounted, displaced 0.050 inch to the right with reference to the first group, the heads in the second group will trace another set of channels. Each of these channels will fall 0.050 inch to the right of each channel from the first group of heads. The remaining spacing between channels can be utilized by the addition of head groups, each progressively displaced with respect to the preceding one. For example, if four additional head groups are mounted on the drum, each displaced to the right of the preceding one by 0.050 inch, the head-to-head space originally created by the reference group would be fully utilized. This, in turn, would result in the tracing of channels, each displaced 0.050 inch from the next.

The actual head displacement on bars 1, 3, and 5 on any drum is illustrated in figure 2–8. Notice that the length of the inside cut in each bar allows the entire group of 33 heads to be displaced. In other words, the heads in each field are progressively displaced from bar to bar.

Each drum having CD-OD operations employs 13 drum bars (fig. 2–9); namely, one erase bar and six pairs of information head bars to correspond with the six fields in the drum. Hence, each field utilizes a set of two drum bars; the drum heads on each bar in the set are mounted so they ride on the same channel. This arrangement facilitates the function of writing and reading. Therefore, one bar of heads is utilized to write information on the drum, while the other reads the written information from the drum. Such is the case for the LOG, MIXD, RD, and TD drums, which have CD and OD operations. The auxiliary memory drums, having only CD operations, require only one bar of heads per field for both writing and reading.

Although the assembly structure is the same for CD-OD and auxiliary drums, head bars in the latter occupy only the spaces allotted for bars 1, 3, 5, 7, 9, and 11. The space allotted for the remaining bars is covered with blank plates.

3.4.2 Register Layout

Once it has been established that 33 adjacent heads on a drum bar form the 33 channels of a field, it must be established that each of these channels is not a continuous line but a succession of magnetized spots or bits. It is equally significant to indicate that, at the time of writing, all 33 bits in an information word are re-

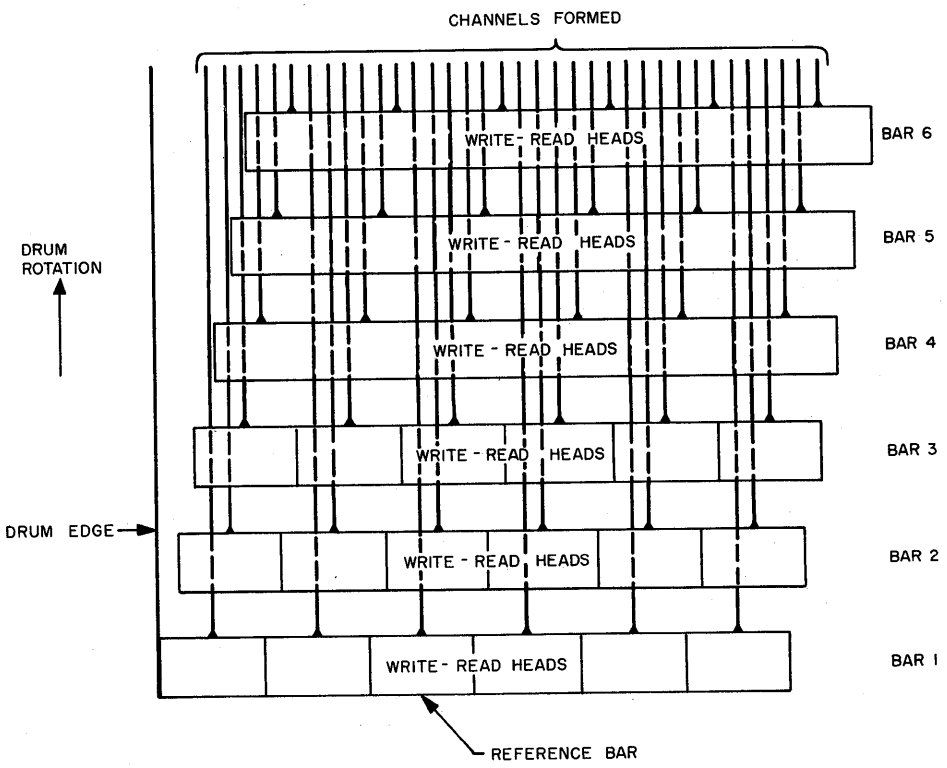


Figure 2–7. Drum Bars in Successive Field Displacement

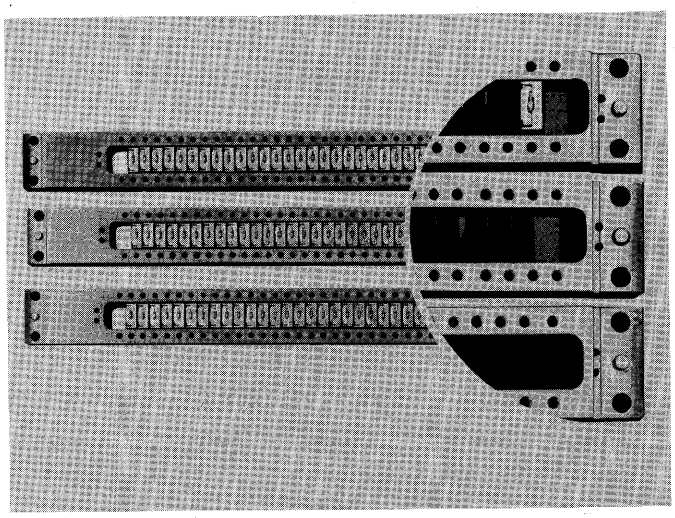


Figure 2–8. Typical Drum Head Bars 1, 3, and 5, Bottom View

corded at once on the drum surface. Furthermore, the writing operation can be repeated up to 2,048 times during each drum revolution.

In other words, the length of the drum circumference allows 2,048 equidistant spaces, or registers, each of which contains a 33-bit word. Calculated in time distance (2,048 registers in approximately 20-ms drum revolution), each register is 10 usec long. All registers on the drum surface are identified by count. This function is performed by the angular position counter (APC) associated with each drum (par. 7.4.2). The APC starts its count at index-pulse time and reports to the Central Computer, upon program request, the number of each drum register passing under the heads of a specific drum bar. The LOG drum APC circuits are applicable only during local test operations.

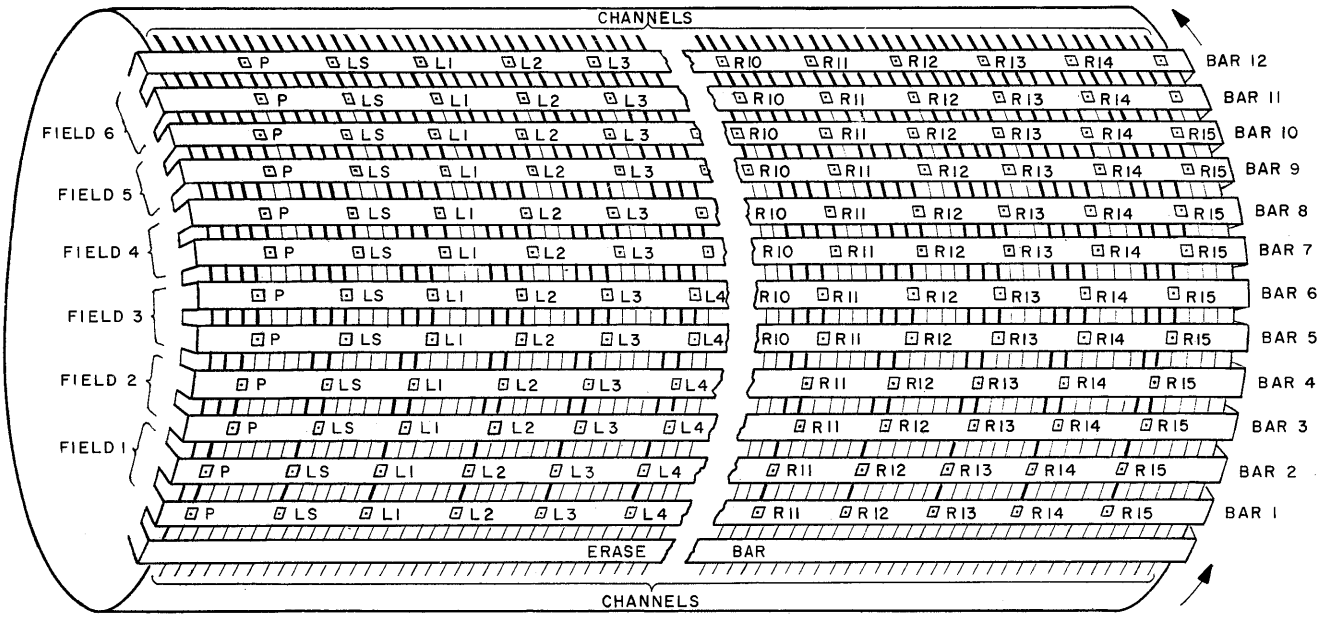


Figure 2–9. Drum Surface, Field Layout

CHAPTER 4
TIMING GENERATION AND DISTRIBUTION

4.1 GENERAL

Each of the 12 drums in the system develops its own timing independently from one another. Such timing is utilized by circuits within the Drum System and circuits of the related system, except the Central Computer. Thus, timing generated by the LOG drum controls the operations of the LRI and GFI elements in the Input System and the elements of the Output System. The MIXD drum generates timing for the MI and XTL elements of the Input System, the DD element of the Display System, and the IC circuits of the alternate Drum System in the duplex equipment. The TD and RD drums generate the timing employed by the SD element of the Display System. In the auxiliary drums, AM-A through AM-H, timing is utilized by the circuits of each auxiliary drum only.

Timing developed by each drum allows data transfers, into or out of the system, to take place at the rate of one transfer every 10 usec. The 10-usec periods come as a result of the 2,914-rpm rotational speed and the 2,048 circumferential divisions of all drums except the TD and RD drums. These two drums have 2,060 circumferential divisions each.

To accommodate the various steps involved in a data transfer, each 10-usec period is divided into four parts represented by four consecutive drum timing pulses (DTP's), namely DTP-1, DTP-2, DTP-3, and DTP-4. In successive periods, or registers, of a rotating drum, timing pulses occur in the sequence DTP-1, DTP-2, DTP-3, DTP-4, DTP-1, DTP-2, DTP-3, DTP-4, DTP-1, etc. The time distance between two consecutive timing pulses is 2.5 usec.

In addition to timing pulses, a synchronizing pulse called index pulse is produced once per drum revolution. Considering the rotational speed of the drum, consecutive index pulses occur at approximate time intervals of 20 ms.

The components and circuits employed in the Drum System for the generation and distribution of timing pulses form part of logics 1.1.2 and 1-2.1.2 and are described in 4.2 through 4.3.

4.2 TIMING GENERATOR

The Drum Systems in operation at the various sites employ one of two basic methods of timing generation: all systems installed in sites 1 through 16 employ the optical method described in 4.2.1; all other sites, starting with site 17, employ the etched timing disc method described in 4.2.2.

4.2.1 Optical Method of Timing Generation

The optical method of timing generation comprises the following operations:

a. Development of a basic timing signal with an optical frequency generator (OFG). Refer to 4.2.1.1 through 4.2.1.3.

b. Conversion of the basic timing signal to discrete timing pulses by means of a timing pulse generator (TPG). Refer to 4.2.1.4.

c. Writing of these pulses on two separate control channels of the drum; namely, the timing and index channels. Refer to 4.2.1.5.

d. Reading of basic timing and index signals. Refer to 4.2.1.6.

The OFG employed in this method of drum-timing generation develops the basic timing signal which causes standard write heads to magnetically record the basic timing pulses on the drum surface. Therefore, at the time of erasing (par. 3.2) not only the stored data but also the timing and index channels are completely eliminated from the drum surface. This condition requires the use of a special relay network which causes the automatic rewriting of timing and index channels immediately after each erase operation.

The OFG is composed of the optical timing disc, the optical transducer, and the power cathode follower (pars. 4.2.1.1 through 4.2.1.3). These three components are illustrated in block form in figure 2–10 to indicate how they operate in conjunction with each other to provide an input signal to the TPG (par. 4.2.1.4).

4.2.1.1 Optical Timing Disc

The optical timing disc (fig. 1–10) comprises two plates of glass laminated with a photographic plate between them. The photographic plate is opaque except for a transparent circular area which has the shape of a 50 percent modulated wave envelope. There are 2,048 wave variations in the optical timing disc of all drums except the TD and RD drums. The disc mounted on the TD and RD drums has 2,060 wave variations. The object of the wave variations in the transparent area of the disc is, first, to cause the light beam from the optical

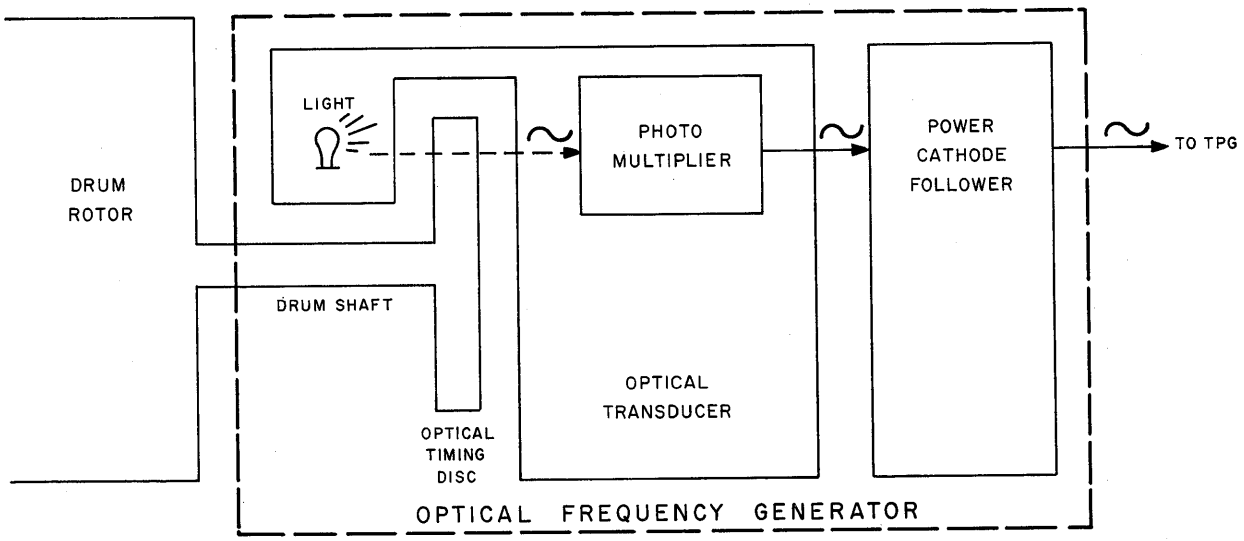


Figure 2–10. Optical Frequency Generator, Block Diagram

transducer to vary in intensity as the drum rotates (fig. 2–10); second to insure that, in spite of changes in drum rotational speed, the same number of variations (2,048 or 2,060) are produced at every drum revolution. The light variations are received by the photomultiplier tube in the optical transducer.

4.2.1.2 Optical Transducer

The cross-sectional view of the optical transducer as well as its mounting on the drum assembly with respect to the optical timing disc are shown in figure 2–11. The transducer unit contains one exciter lamp as the light source, seven lenses, three prismatic mirrors, and a photomultiplier tube. The lenses and mirrors are mounted in a protruding arm which wraps around the edge of the optical timing disc. The exciter lamp lights under control of the erase circuits to initiate the process of writing timing pulses on the drum surface after every erase operation. Light from the lamp passes through lenses 1, 2, 3, and 4 and is reflected by mirror 1. The reflected light passes through lens 5 and is reflected by mirror 2. The light is then projected through the transparent area of the optical timing disc. The amount of light passing through is varied in a sinusoidal pattern as described in 4.2.1.1. This pulsating light passes through lenses 6 and 7 and is reflected by mirror 3 into the window of the photomultiplier tube.

4.2.1.3 Photomultiplier and Cathode Follower Circuit

The photomultiplier tube converts the pulsating light energy into pulsating electrical energy. Although only the photomultiplier tube is mounted within the optical transducer unit, its entire circuit and the power cathode follower circuit are shown in the diagram of figure 2–12. The photomultiplier tube consists of a cathode, six dynodes, and an anode. Dynodes are metal plates the surface of which is treated to produce high emission. The cathode of the tube emits electrons proportional to the amount of light incident on it. These electrons are attracted to the first anode (pin 1) because of the d-c potential applied to it and by the proximity of the dynode to the cathode. For each electron that strikes the dynode, several secondary electrons are released. These secondary electrons are attracted by the second dynode (pin 7) and cause a greater number of secondary electrons to be released. This process is repeated by the other dynodes until the increasing secondary electrons reach the anode (pin 4). Thus, for each electron emitted by the cathode, a great number of electrons reach the anode or plate. Since the light reaching the cathode varies at a sinusoidal rate, the amount of electrons reaching the plate also varies at a sinusoidal rate. The output of the photomultiplier tube is approximately a 100-kc sinusoidal signal.

The circuit components which complete the photomultiplier circuit and the entire power cathode follower circuit are physically mounted within the power cathode follower pluggable unit mounted on the drum assembly (fig. 1–7). The output of the photomultiplier is connected to the power cathode follower. This circuit acts as a buffer stage between the photomultiplier tube and the timing pulse generator.

4.2.1.4 Timing Pulse Generator (TPG)

The TPG is a special circuit of the Drum System and is, therefore, covered in detail by the Special Circuits

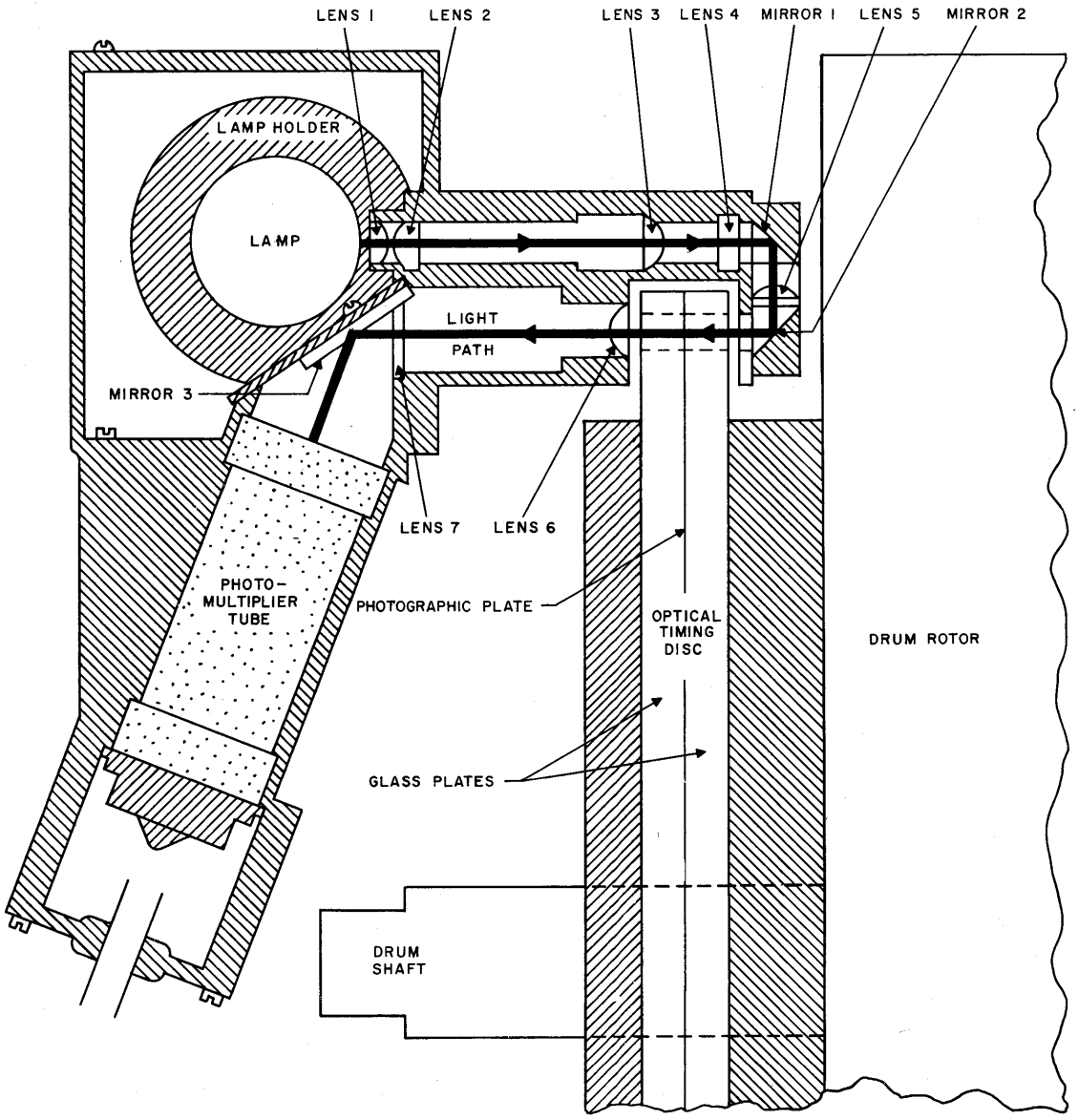


Figure 2–11. Optical Transducer Operation, Cross-Sectional View

manual (3-3-0). Logically described, the TPG receives the sinusoidal signal from the power cathode follower and converts each cycle of the signal into two discrete and equidistant pulses. These pulses are called TP 1 and TP 3, (fig. 2–13). The TP 1 pulses are formed at each negative-going zero crossing of the input sine wave; the TP 3 pulses are formed at each positive-going zero crossing of the input sine wave. At normal drum rotation speed, there are 5 usec between zero-crossing points. The same interval is therefore present between TP 1 and TP 3 pulses. Following the same reasoning, successive TP 1 pulses are produced at 10-usec intervals and successive TP 3 pulses are also produced at 10-usec intervals. The TP pulses are utilized by the timing and index-channel write circuit.

4.2.1.5 Timing and Index-Channel Write

The logic diagram of figure 2–14 shows the circuits intervening in timing generation from optical development to writing on the drum surface. Included are the OFG and TPG circuits described in preceding paragraphs and the indication of control exercised by the erase circuits. While such control enables erasing of one specific drum or of all drums simultaneously, the time and index channel rewrite operation following erase must be executed on a drum-by-drum basis because

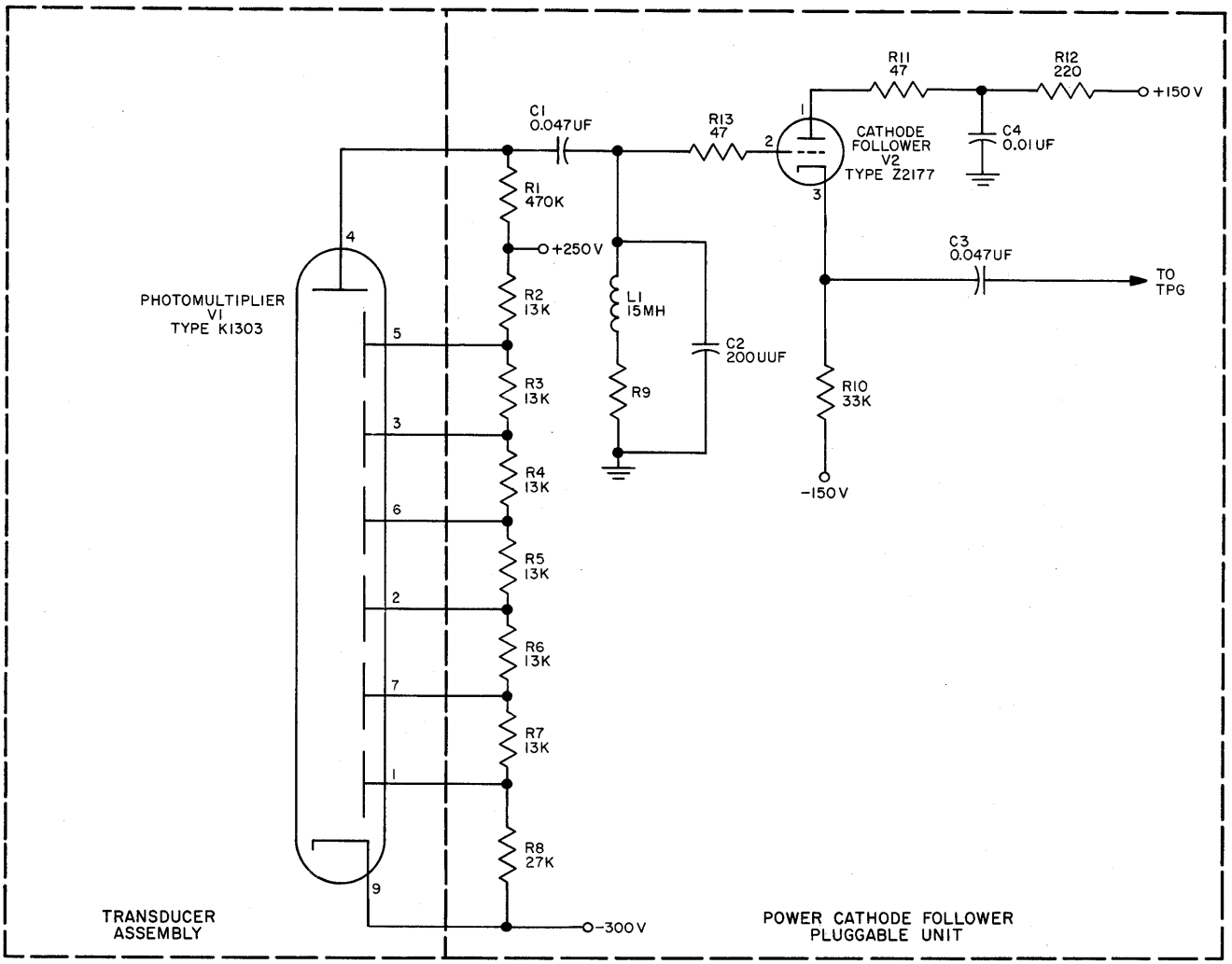


Figure 2–12. Photomultiplier and Power Cathode Follower Circuits, Simplified Schematic Diagram

there is only one TPG and one timing and index write circuit to serve the six main drums. (The six auxiliary drums have identical arrangements.) Through relay action, as shown in the figure, the input of this circuit is connected to the OFG of one specific drum and the output is connected to the timing and index write heads of the same drum.

At the start of an erase operation, the exciter lamp lights in the OFG of each of the six drums. However, only one OFG is relay-connected to the TPG which, in turn, produces DTP-1 and DTP-3 pulses. At the same time, the erase control circuits have produced a triggering level which is applied to the single-shot (SS) circuit. The negative output of the quiescent SS circuit becomes positive and remains in that state for 30 ms. This period is significant for it is the interval allowed the timing and index write circuit to record timing information of the drum surface. After this period, no further timing is written until the next erasing operation is performed.

During the 30-ms period following the triggering of the SS circuit (approximately 1-½ drum revolutions) the actions described below take place. Gate circuit GT 1 is conditioned. TP 1 pulses from the TPG are passed through GT 1 to set FF 1 and to clear FF 2. The 1 state of FF 1 conditions GT 2 to pass TP 3 from the TPG. Each TP 3 passed in this manner goes to the pulse stretcher. In the pulse stretcher, the TP 3 pulse clears FF 3 and enters the 1.7-usec delay. At the end of this delay, FF 3 is set. Therefore, for 1.7 usec following each TP 3 pulse, the 1 side of FF 3 is providing the drum write driver DWD with its required negative input, which results in the simultaneous conditioning of drum writer DW 1 and DW 2. Thus, the drum writers conduct, causing the timing and index channel heads to write. Under the above conditions, DW 1 is arranged by

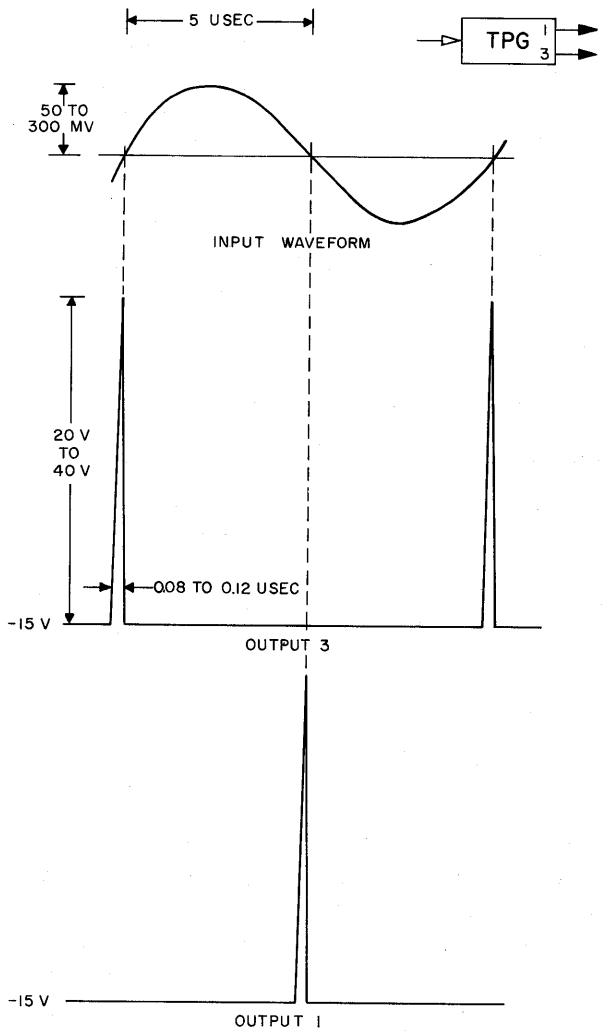


Figure 2—13. Timing Pulse Generator Input and Output Waveform Relationship

the output of FF 2 to write 0 bits, while DW 2 is arranged by the +10V and −30V inputs to permanently write 1 bits.

Immediately upon termination of the 30-ms period, the SS circuit output becomes negative. In this condition, GT 1 is no longer conditioned, but GT 3, in turn, is conditioned through the action of the inverter (I) circuit. The next TP 1 pulse goes through GT 3 and sets FF 2. With this flip-flop set, DW 1 causes the index head to write a 1 bit, and GT 4 receives a conditioning level. Meanwhile, the next TP 3 pulse goes through GT 2 and the pulse stretcher, causing the index channel head as well as the timing channel head to write a 1 bit. The next TP 1 pulse after this pulse writing goes to GT 4, clears FF 1, and, in the process, removes the conditioning level to GT 2. Thus, all successive TP 3 pulses are blocked at the GT 2 and the writing of index and timing pulses is discontinued until a new erase operation is performed.

4.2.1.6 Timing and Index-Channel Read

The timing and index channels of each drum are read continuously during operation of the Drum System (fig. 2—15). The flux pattern on the timing channel of a drum causes a series of sine waves to be induced in the timing channel read head. (These sine waves are similar to the sine waves developed by the OFG.) The induced sine waves are applied to a TPG, which converts them to two (DTP's 1 and 3) of the four standard timing pulses used to time the circuits of the drum.

In each drum timing circuit, the DTP 1's are sent to a 2.5-usec delay line. The output of this delay line is called a DTP 2 pulse. The DTP 3 pulses are also sent to a 2.5-usec delay line, the output of which is termed a DTP 4 pulse. The DTP pulses 1 through 4 comprise the standard timing pulses of each drum. The 2.5-usec interval between each pulse results in a pulse cycle of 10 usec. This corresponds to the time required for one register on the drum surface to pass a read or write head during normal rotation of the drum.

Drum-timing pulses which time drum operations during information exchanges between the Drum System and the Central Computer System are designated as CD 1, CD 2, CD 3, and CD 4. Drum-timing pulses which time drum operations during information exchanges with the Input, Output, and Display Systems as well as with the duplex Drum System are designated OD 1, OD 2, OD 3, and OD 4.

Within the Drum System, CD 1, and OD 1 pulses are used for reading, and CD 3 and OD 3 pulses are used for writing. The CD 2, CD 4, and the OD 2, OD 4 pulses are used for control operations which prepare the Drum System circuits to read or write.

The index channel is read by two index channel drum read heads, the CD index head and the OD index head (except in the AM drum, where there is only a CD index head). The CD index read heads sends the sine wave produced by the index bit to the index channel drum read amplifier. The drum read amplifier conditions a gate to pass the DTP 1 pulse occurring at that time. This gated DTP 1 pulse is called the CD-index pulse. The OD head sends its sine wave to another drum read amplifier, which conditions another gate to pass a DTP 3 pulse. This DTP 3 pulse is called the OD-index pulse. The CD-index pulse coincides with a DTP 1 timing pulse, and the OD-index pulse coincides with a DTP 3 timing pulse.

The CD-index pulse serves to indicate the beginning of a drum revolution during information transfers between the Drum System and the Central Computer System. The CD-index pulse is associated with the first of

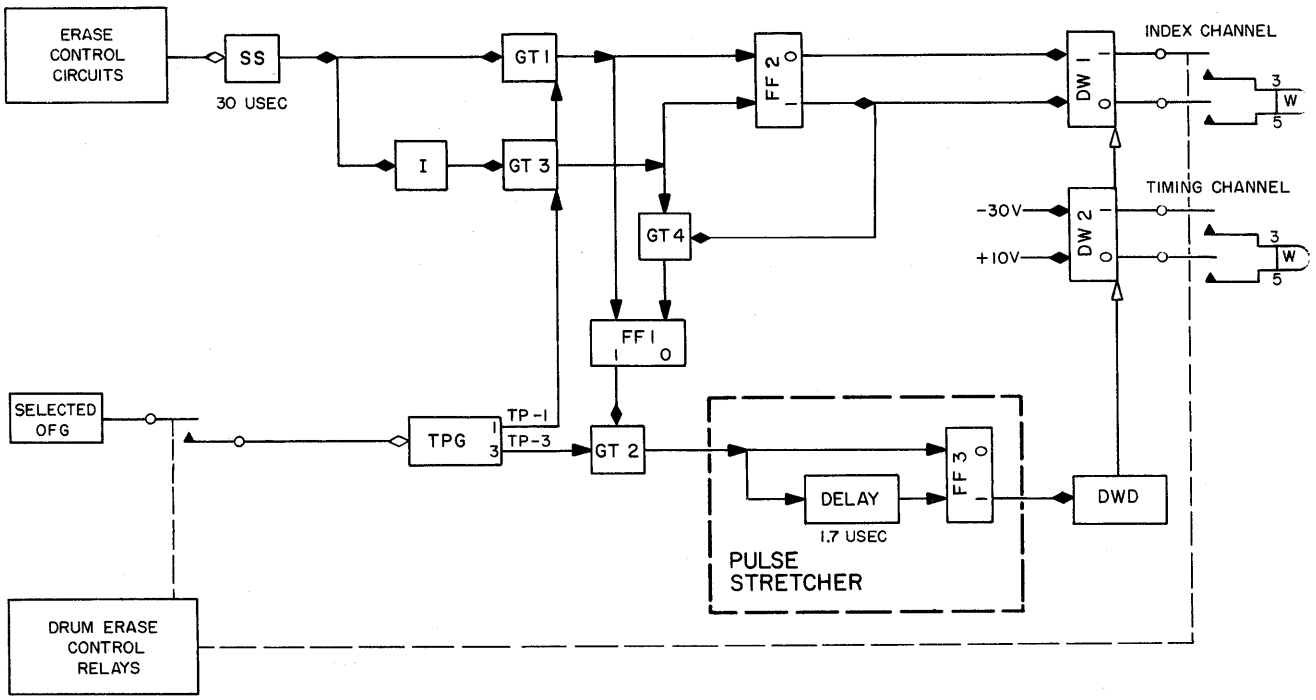


Figure 2–14. Timing-Channel and Index-Channel Write Circuit, Simplified Logic Diagram

the 2,048 registers. The OD-index pulse indicates the end of a drum revolution during information exchanges between the Drum system and the Input, Output, or Display Systems. The OD-index pulse will be associated with the last of the 2,048 registers.

4.2.2 Etched Timing Disc Method of Timing Generation

The etched timing disc method of timing generation is a simplified method which provides for timing and index signals permanently recorded. Consequently, the OFG components and the relay network for automatic timing and index channel rewrite are not required. Timing generation by this method is completed in one operation, namely, reading of the etched timing and index channels. This operation is performed in the manner described in the preceding paragraph.

The 2,048 circumferential divisions (2,060 in the RD and TD drums) are accurately determined by ridges and valleys on the magnetic surface of the etched timing disc (fig. 1–12). The ridges appear flush with the magnetic nickel-cobalt coating. In the valley areas, to expose the nonmagnetic copper plating of the disc, no nickel-cobalt coating is applied.

Erasing does neutralize the magnetized timing and index channels of the etched timing disc. However, two recording heads, one riding on the timing channel and the other on the index channel of each drum, continuously magnetize the two channels. The six timing heads and the six index heads in the main drums are series-connected in alternate order. The first head is connected to a source of +10V and the last head is connected to ground. The six auxiliary drums in unit 20 have identical operation for the timing and index channel heads when the system is equipped with etched timing discs.

4.2.3 RD and TD Drum Timing Pulses

The timing circuits of the TD and RD drums are modified slightly so as to delay the application of OD and CD pulses to the TD and RD circuits. A delay of 120 usec is required to allow time for switching transients, developed during RD and TD field switching operations, to subside. The modification is accomplished as follows.

The timing disc on the TD and RD drums is constructed to cause the writing of 2,060 timing cycles in the TD and RD timing channels, instead of the 2,048 timing cycles found on all other drums. The DTP 1 and DTP 3 pulses derived from these channels are fed into gap counters which cause the first 12 cycles during each revolution of the drums to be skipped. The counters prevent the DTP 1 pulses and DTP 3 pulses of the first 12 cycles of each revolution from being sent to the read and write circuits of the TD and RD drums, thereby delaying the RD and TD operations for 12 cycles (120 usec).

In the case of the RD and TD drums, a distinction is made between the DTP pulses and the equivalent OD or CD pulses. The DTP can be taken from any point on the 2,060-cycle timing channel; OD and CD signals are taken only from the 2,048 cycles that are present after 12 cycles are skipped. The OD and CD pulses represent the output of the gap counters. With 120 usec skipped at the beginning of each revolution, no register on any of the TD or RD fields is read before the required switching time has elapsed.

4.2.3.1 TD Timing, Circuit Analysis

The optical timing disc, employed in the writing of the timing channel of the RD and TD drums, contains 2,060 sinusoidal cycles. The TPG in the timing-channel read circuit for these drums (fig. 2–16) alternately generates two timing pulses, DTP 1 and DTP 3, for each sine-wave cycle detected by the timing channel read head. Both timing pulses are delayed 2.5 usec to produce DTP 2 and DTP 4.

The DTP 1 and DTP 3 pulses are passed by the output of the TD CD gap counter, to produce the TD CD 1 and TD CD 3 pulses used by the TD angular position counter. The DTP 2 pulse is passed by the TD OD gap counter to produce the TD OD 2 pulse and a TD timing level. The TD OD 2 pulse is used to step the TD register counter; the TD timing level is a necessary condition for the operation of the TD OD read circuits.

The TD CD gap counter is shown in figure 2–17. The counter is initially cleared by the index pulse. With FF's 3 and 4 at 0, OR circuit 1 conducts. The output of OR circuit 1 conditions gate 1 to pass DTP 1's to the counter. The 0 outputs of FF 3, FF 4, or of both flip-flops, maintain conduction in OR circuit 1 until 12 DTP 1's have been counted. At this time FF's 3 and 4 are both in the 1 state and OR circuit 1 conduction stops. With OR circuit 1 output level removed from GT counting stops until the next index pulse clears the counter and resumes conduction in the OR circuit. In the period before the index pulse arrives (from the 13th to the 2,060th DTP 1 pulse), FF's 3 and 4 are in the 1-state, and AND circuit 1 conducts, producing an output level. The level at the output of gap counter 1 passes the 13th through the 2,060th DTP 1 and DTP 3 pulses at gates 1 and 2 respectively of figure 2–16.

The TD OD gap counter uses the OD index pulse to clear its flip-flops and uses DTP 2 pulses for counting. In all other respects, the TD OD gap counter is identical with the TD CD gap counter. The output level of the TD OD gap counter passes the 13th through 2,060th DTP 2 pulses at GT 3 (fig. 2–16). In addition, the output level is used as a necessary condition for TD reading.

By skipping the first 12 pulses after every index, the TD-timing-circuit-and-gap counter produces a 120-usec period during which OD timing pulses are not available for reading, writing, or register counting purposes. At

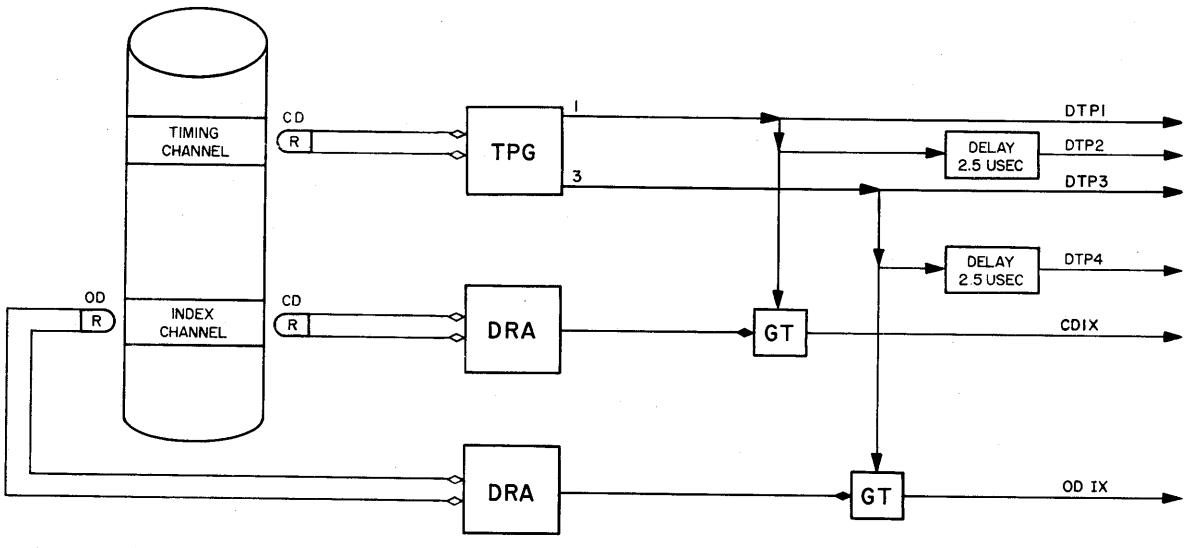


Figure 2–15. Timing-Channel and Index-Channel Read Circuit, Simplified Logic Diagram

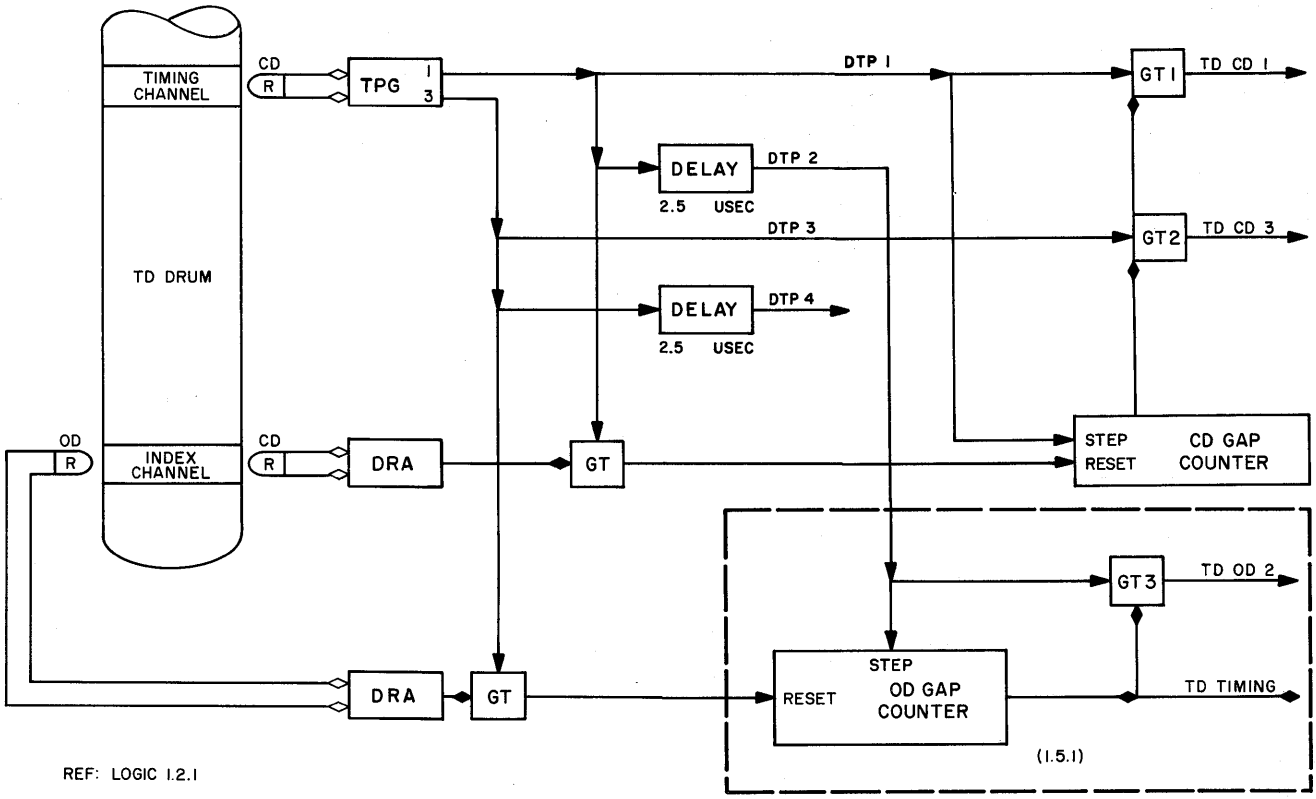


Figure 2–16. TD Timing Read Circuit, Simplified Logic Diagram

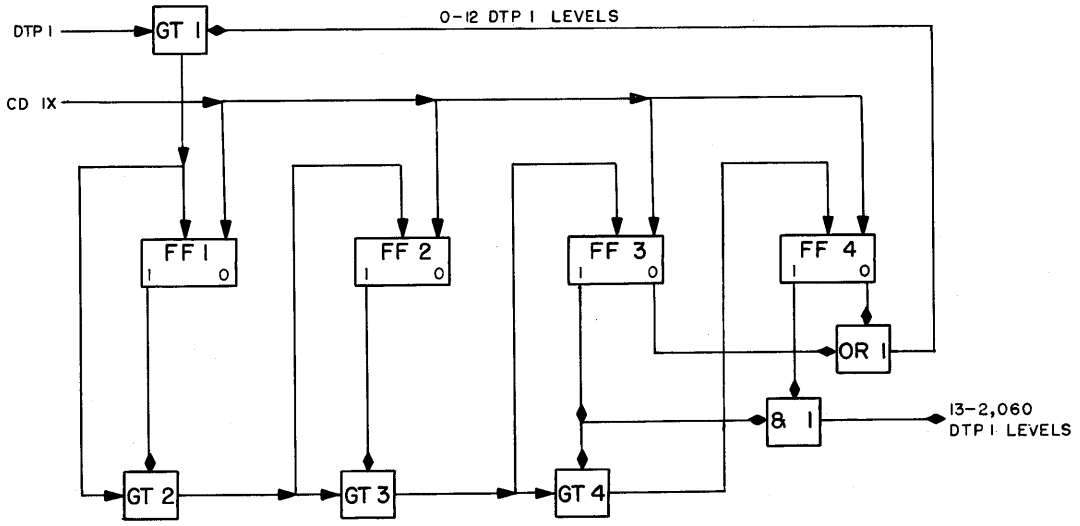


Figure 2–17. TD CD Gap Counter, Simplified Logic Diagram

the end of the delay, however, 2,048 timing cycles remain during which the drum can read and write the usual number of drum registers.

4.2.3.2 RD Timing, Circuit Analysis

The radar drum (RD) timing circuits are shown in figure 2–18. The generation of the DTP and CD pulses for the radar field circuits is identical to the generation described above for the corresponding pulses of the track drum. The RD CD gap counter is identical with the TD OD gap counter. The RD OD gap counter is

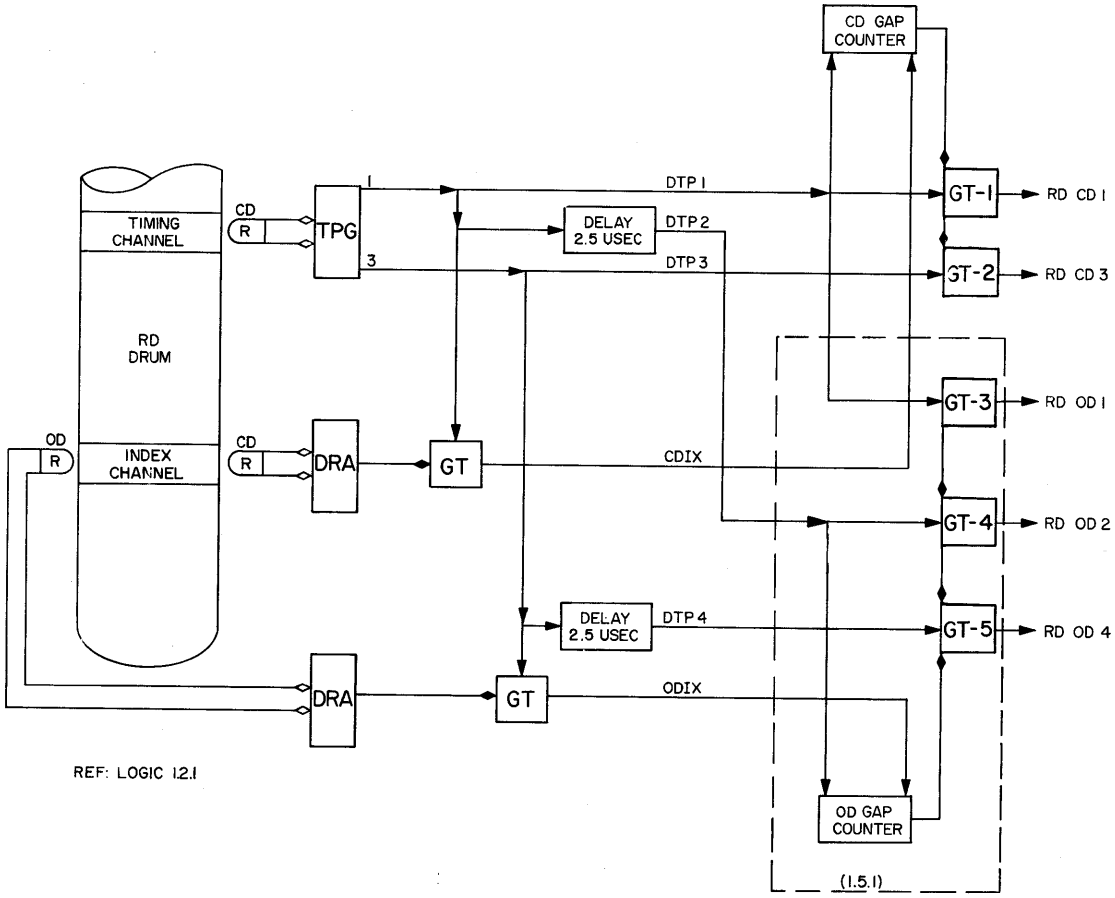


Figure 2–18. RD Timing Read Circuit, Simplified Logic Diagram

identical to the TD OD gap counter. The level generated by this counter conditions GT's 3, 4, and 5 to pass the 13th through 2,060th DTP 1, 2, and 4 pulses, respectively, thereby producing the RD OD 1, the RD OD 2, and the RD OD 4 pulses used for RD OD reading, writing, or counting purposes.

4.3 TIMING PULSE DISTRIBUTION

Although the function of timing in the Drum System has one fundamental principle, the six auxiliary drums in unit 20 have a distribution network which is independent from the distribution network used by the six main drums. Proceeding in order of complexity, the auxiliary drums present a more straightforward approach to discussions of timing distribution.

The application of timing pulses generated by the six auxiliary drums in unit 20 is generally devoted to one CD area of operation which includes the ACD read-write control logic 1-2.2.1 and the ACD manual test read-write control logic 1-2.3.2. This area is shared by the six auxiliary drums. Therefore, the drum containing the field selected (by the Central Computer or by manual field selection) at any given time supplies the timing required by the two logics involved.

However, main-drum timing pulses are generated for three specific areas of operation. The first area is identical in purpose with that of the auxiliary drums previously described and includes the CD read-write control logic 1.2.1, the manual test read-write control logic 1.7.2, and the manual control logic 1.7.1. The second area refers to CD-OD field operate logics (MI 1.3.1, GFI 1.3.2, LRI-1 1.3.3, LRI-2 1.3.4, XTL 1.3.5, SP XTL 1.3.6, OB 1.4.1, TD-RD 1.5.1 and 1.5.2, IC S-1.6.1). To these logics, each respective drum continuously applies CD and OD timing pulses as required, regardless of field selection. The third area consists of the systems (Input, Output, and Display) associated with the OD side of the Drum System. To these systems, also, each respective drum permanently applies OD timing pulses.

Since the CD read-write and manual test control logics in either the auxiliary or main drums are effectively activated by each selected field, timing pulses from the drums are brought to a point of release available in each drum group. Upon release, timing pulses

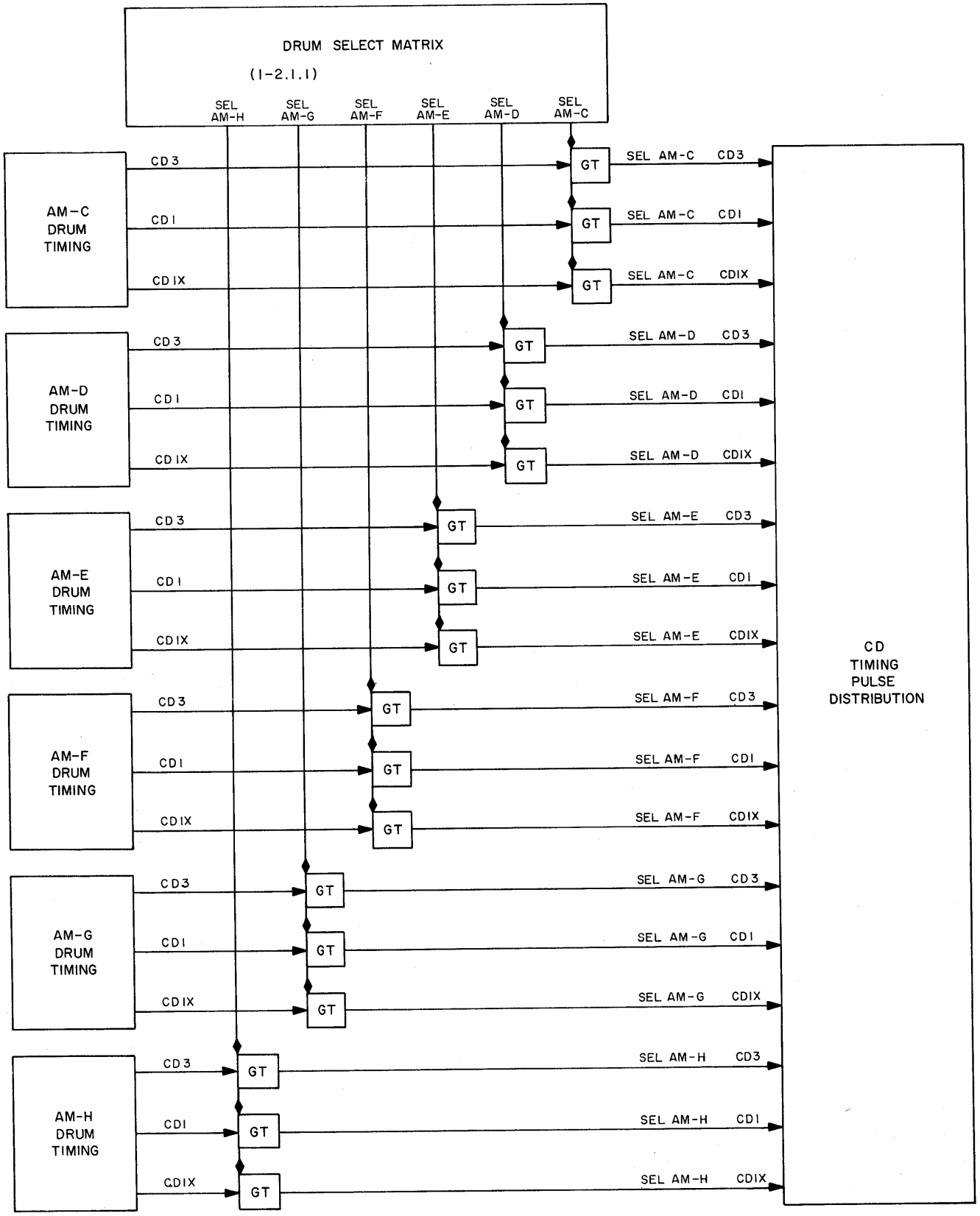


Figure 2–19. Auxiliary Drums Timing Pulse Distributor, Simplified Logic Diagram

are routed to the above logics in the form of SEL CD 1, SEL CD 3, SEL CD 4, and SEL CD IX pulses. The release of CD timing pulses is performed by the circuits of the TPD described in 4.3.1. The routing of SEL CD timing pulses to the various CD control logics is performed by the CD timing distribution circuits described in 4.3.2.

Continuous timing pulse distribution to field operate logics and associated systems is due to two important factors. First, OD data transfers may occur simultaneously and at random times; therefore, the respective field operate logics require continuous timing control. Second, OD timing pulses from each drum are utilized to control operations in the associated systems. Thus, Input System operations are timed by the LOG and the MIXD drums, Output System operations, by the LOG drum, and Display System operations, by the MIXD, TD, and RD drums. The detailed distribution of CD and OD timing pulses to each of the aforementioned field operate logics and systems is described in 4.3.3 through 4.3.5.

4.3.1 Timing Pulse Distributor

Figure 2–19 shows the groups of gate circuits which constitute the TPD in the auxiliary drums (AM-C through AM-H). SEL drum levels from the drum select logic (refer to par. 5.3.3) are applied to respective groups of gate circuits. Each group of gates continuously receives CD 1, CD 3, and CD IX pulses from the same drum which originates the SEL level. Therefore, when one of the SEL drum levels appears, the corresponding gates are conditioned to pass the timing pulses from the selected drum. The pulses at the output of the gates accordingly become SEL timing pulses. Pulses CD 1 CD 3, and CD IX are used for gating because they are the most significant in the control of data transfers. As such, they are the direct result of reading from the timing and index channels of the drum. CD 4 pulses, on the other hand, are obtained from CD 3 sources through a 2.5-usec delay line. CD 2 pulses are not generated.

The TPD in the main drums has the same purpose as in the auxiliary drums. The circuit layout for the RD, TD, AM-A, and AM-B drums is also identical to that of the auxiliary drums. However, the MIXD and LOG drums require special time pulse gating to accom-

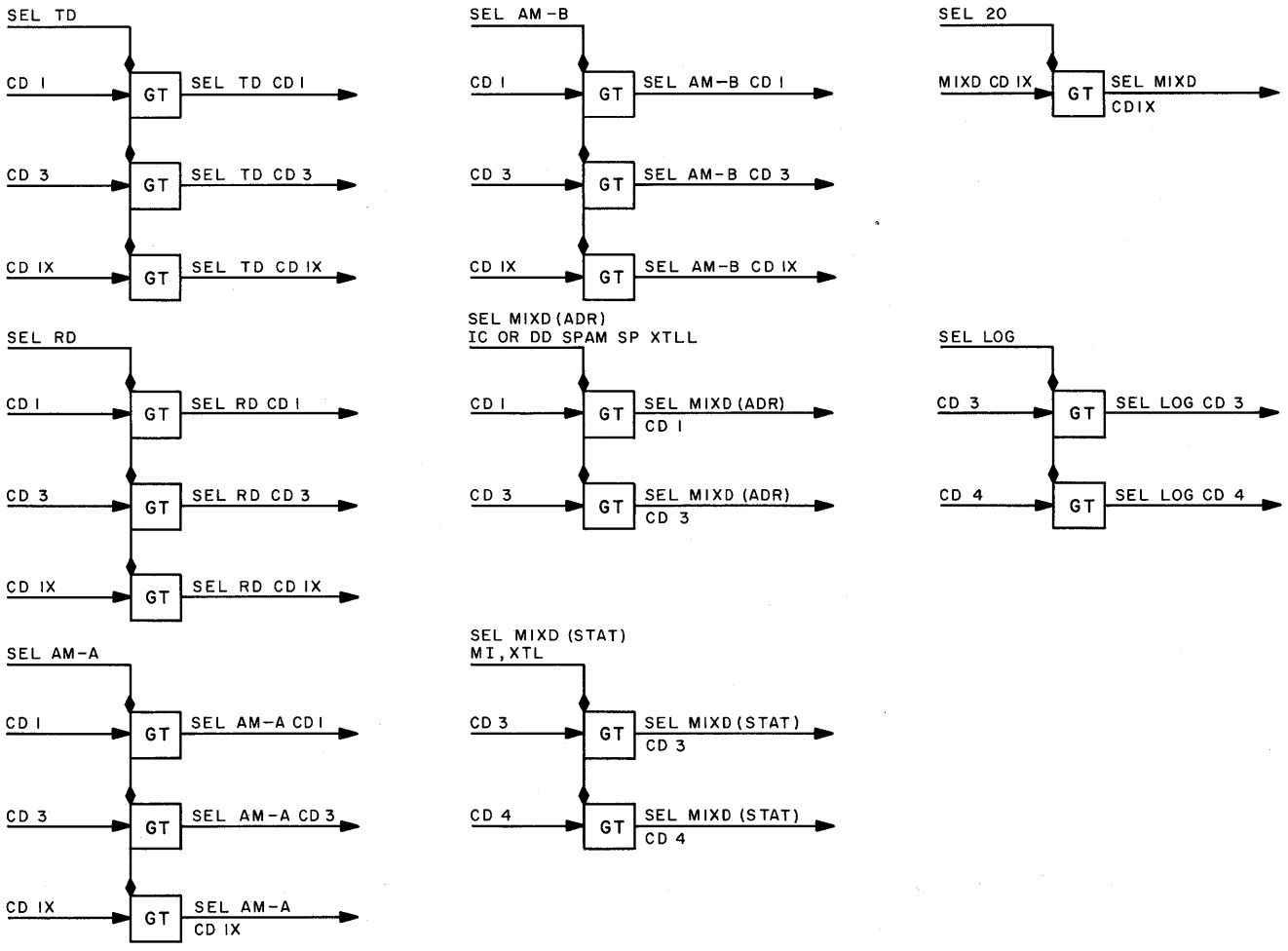


Figure 2–20. Main Drums Timing Pulse Distributor, Simplified Logic Diagram

modate the address and status requirements of their fields. Figure 2–20 shows a simplified diagram of the main drums TPD. The origin of the SEL drum levels is the drum select matrix, logic 1.1.1, the timing pulses are originated by each drum, and the destination of SEL timing pulses is the main drum CD timing pulse distribution circuits.

Refer to figure 2–20. Two different SEL MIXD drum levels are produced by logic 1.1.1. One, SEL MIXD (ADR), results when the SP XTL field or addressable fields IC, DD and SP AM, are selected; the other, SEL MIXD (STAT), is produced when status fields MI or XTL, are selected. The SEL MIXD (ADR) level allows distribution of CD 1 and CD 3 pulses, and the SEL MIXD (STAT) level allows distribution of CD 3 and CD 4 pulses. CD index pulses from the MIXD drum are distributed when any selection in the SDR 20 series is received from the Central Computer. The SEL LOG level is used in the TPD to release CD 3 and CD IX pulses only. CD 1 and CD 4 pulses from the LOG drum are applied to the CD timing pulse distribution circuits described in 4.3.2.

4.3.2 SEL CD Timing Pulse Distribution

The purpose of SEL CD time pulse distribution is to control CD read-write operations in the operate or test modes of Drum System performance. Since SEL CD timing pulses are produced upon field and drum selection, the CD read-write circuits are effectively activated to fulfill the needs of each field selected. Auxiliary drums SEL CD timing pulse distribution is illustrated in figure 2–21. Notice the destination of each of the SEL CD timing pulses when the system is in the operate mode. SEL CD 3 pulses from any one of the six auxiliary drums are connected to the write gate in logic 1-2.2.1 and are converted to SEL CD 4 pulses through a 2.5-usec delay; SEL CD 4 pulses are connected to the master sync gate in the same logic. SEL CD 1 pulses are also connected to logic 1-2.2.1 in two different ways. From each drum individually, these pulses are connected to start compare gates in the address control of logic 1-2.2.1 (par. 7.4.1). From any one of the six drums, a SEL CD 1 pulse connection is made to the read gate of the same logic. In addition to SEL CD timing pulses, CD 1, CD 3, and CD IX pulses are continuously being fed from the timing generation circuits of each drum to the APC and alarm circuits of logic 1-2.2.3.

The CD manual test read-write controls, logic 1-2.3.2, are activated in the test mode of the system and operate in conjunction with the CD read-write control. Logic 1-2.3.2 circuits receive SEL CD 3, and SEL CD IX from any one of the six auxiliary drums.

The main drum SEL CD timing pulse distribution is shown in figure 2–22. Detailed inspection of circuit layout will reveal that CD timing pulse distribution in the main drums generally resembles that of the auxiliary drums described above. This resemblance exists in the TD, RD, AM-A, and AM-B drums which contain all-addressable fields. The differences, then, are due to the methods of handling MI and XTL fields under status control and IC, DD, SP AM, and SP XTL fields under addressable control in the MIXD drum, as well as the all-status fields in the LOG drum. The origin of the SEL CD timing pulses is the TPD (4.3.1). Other timing pulses shown in the figure, such as LOG CD 1 and LOG CD 4, are taken directly from the timing circuits of the drum.

For better understanding, the following discussion contains an analysis of each SEL CD timing pulse reaching the CD control logics. Going from top to bottom in the figure, the APC and alarm circuits, logic 1.2.3, permanently receive CD 1, CD 3, and CD IX pulses from each of the six main drums. Also distributed to logic 1.2.3 are SEL CD 1 pulses connected to the LOG APC checkout circuit. These pulses come from OR 3 which, in turn, receives gated LOG CD 1 pulses from GT 1. LOG CD 1 pulses pass through GT 1 only when an OB field is selected (SEL OB level present). Other conditions affecting OR 3 refer to SEL CD 1 distribution to logic 1.7.2.

In the manual read-write circuits, logic 1.7.2, SEL CD 1 pulses are used to control write-by-address operations. The conditions for the production of SEL CD 1 pulses are those established at OR 3, namely, the presence of TEST SEL IC CD 1 pulses, a gated LOG CD 1 pulse, or any of the SEL CD 1's from OR 7. TEST CD IX pulses are received from OR 1. The various inputs to OR 1 can be traced to the TPD (fig. 2–20). TEST CD 3 pulses used to step the test APC are obtained from OR 2. Any of the six drums affected by addressable or status fields, at any time, will produce the CD 3 pulses applied to OR 2.

The status disconnect counter, logic 1.3.1, receives SEL CD 3 pulses from OR 2, as previously described, and also SEL CD 4 pulses from OR 5. There are three inputs to OR 5. First, a gated LOG CD 4 pulse from GT 2, which appears when both the SEL OB and the OB OPER levels are present, or when either an LRI or a GFI field is selected. Any one of these conditions present at OR 4 will open GT 2 to pass LOG CD 4 pulses. The second input to OR 5 is the SEL MIXD (STA) CD 4 pulse from the TPD. The third input to OR 5 comes from a 2.5-usec delay circuit which converts SEL CD 3 pulses into SEL CD 4 pulses.

The manual control, logic 1.7.1, receives SEL CD 4 pulses whose development was described above.

Timing for the CD read-write control, logic 1.2.1, is provided by SEL CD 4 pulses which control the

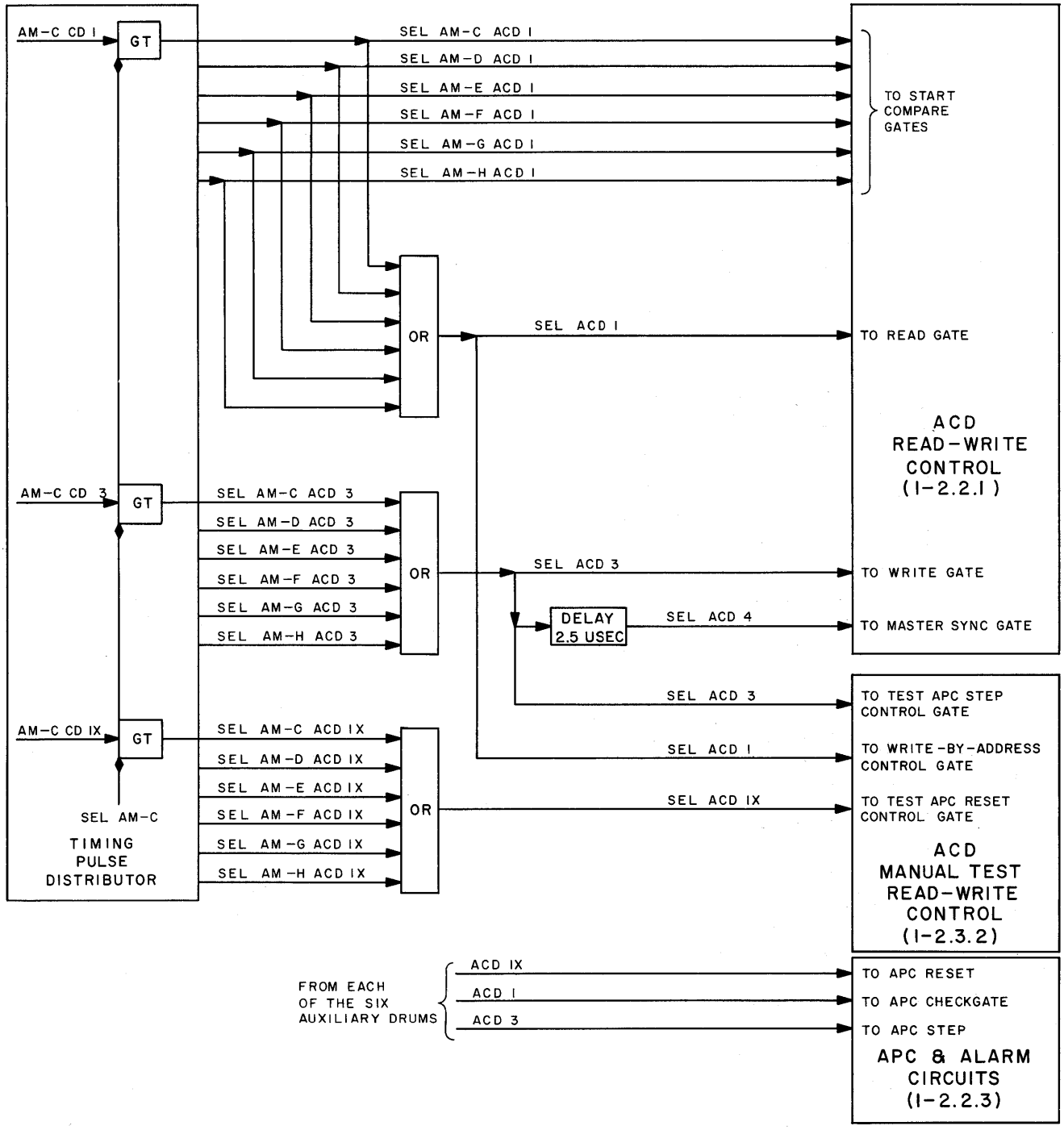


Figure 2–21. Auxiliary Drums SEL CD Timing Pulse Distribution, Simplified Logic Diagram

master sync gate, by SEL CD 3 pulses for the write gate, and by SEL CD 1 pulses for the read gate as well as the start-compare gates. SEL CD 4 pulses are originated at OR 5, as previously described; SEL CD 3 pulses originated at OR 6 are present whenever any of the drums containing addressable fields is selected. (Writing control of status OB fields is determined by the respective 1.4.1 logic.) SEL CD 1 pulses are connected in two different ways; one common SEL CD 1 originating at OR 7 and individual SEL CD 1's from each drum containing addressable fields. These pulses are passed by one of the start-compare gates with the ultimate purpose of

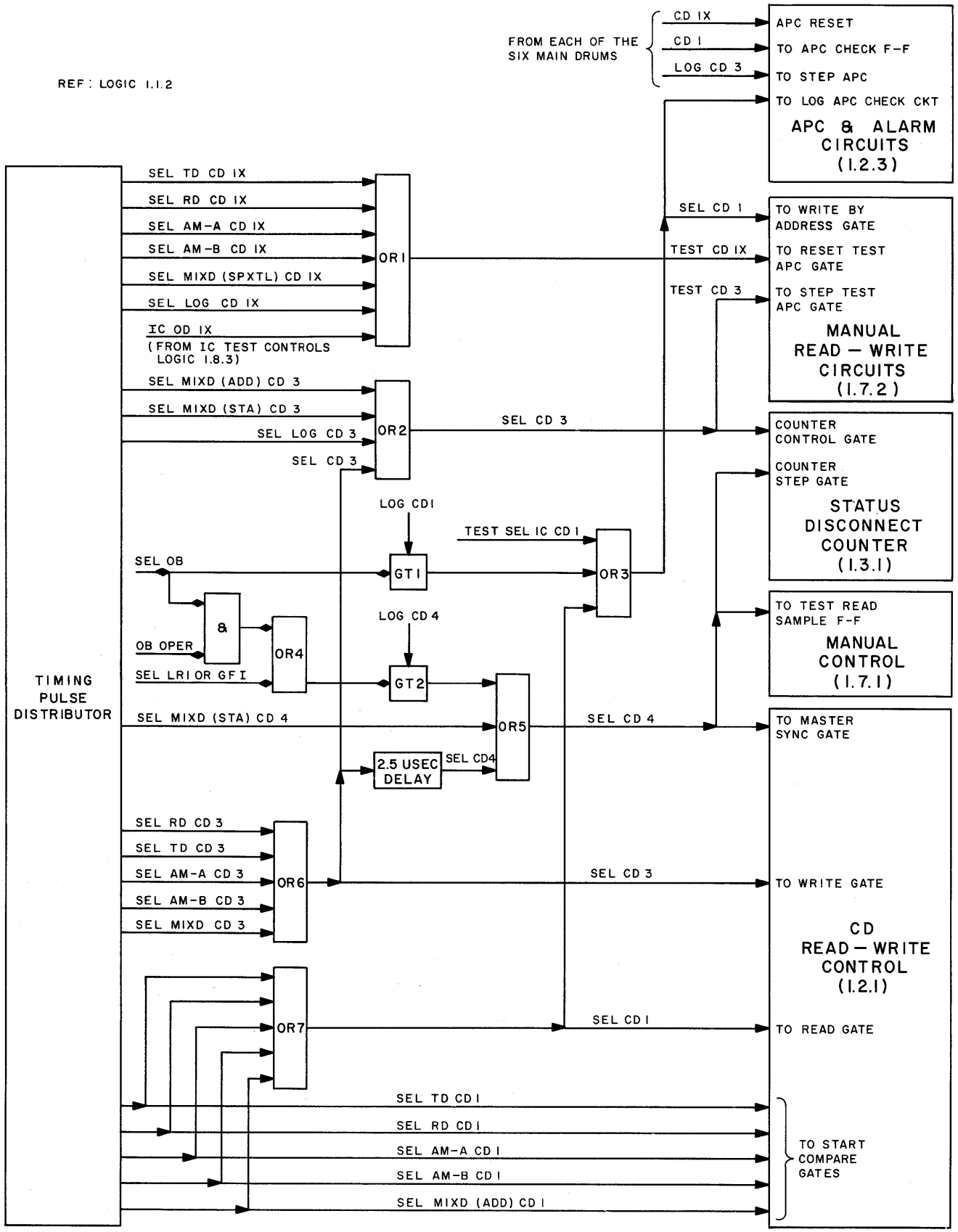


Figure 2–22. Main Drums SEL CD Timing Pulse Distribution, Simplified Logic Diagram

transferring to the Central Computer the contents of the APC in the selected drum.

4.3.3 LOG OD Timing Pulse Distribution

The overall distribution of LOG timing pulses is shown in figure 2–23. LOG-OD timing pulses are continuously distributed to time the six status field logics controlled by the LOG drum: the GFI field (logic 1.3.2), the two LRI fields (logics 1.3.3 and 1.3.4), and the three OB fields (logic 1.4.1). The LRI and GFI fields operate in conjunction with the Input System, and the OB fields with the Output System. LOG-OD pulses are continuously being sent to these systems to synchronize their operations with those of the LOG drums.

4.3.4 MIXD OD Timing Pulse Distribution

The distribution of the MIXD-drum timing pulses is shown in figure 2–24. These pulses time the operation of four CD-OD fields, namely, the MI field, the IC field, the XTL fields, and the DD field. Two spare auxiliary memory fields, the SPAM and SP XTL, are also under MIXD timing pulse control. The MIXD OD pulses are sent to the Display System, the Input System, and the CD circuits of the standby Drum System. These timing pulses are used in the equipment to synchronize information exchanges with the Drum System.

4.3.5 TD and RD OD Timing Pulse Distribution

The TD and RD drum timing pulse distribution is illustrated in figure 2–25. These pulses time the OD data transfers of the six TD fields and the nine RD fields of the TD and RD drums, respectively. The OD timing pulses of each drum are sent to the SD timing pulse switch (logic 1.5.2) in the SD OD field switching and read circuits. From these circuits the pulses are passed through a common OR circuit and sent to the situation display generator element (SDGE) as SD timing pulses. This action serves to synchronize the operation of the SDGE circuits with the TD and RD drum circuits.

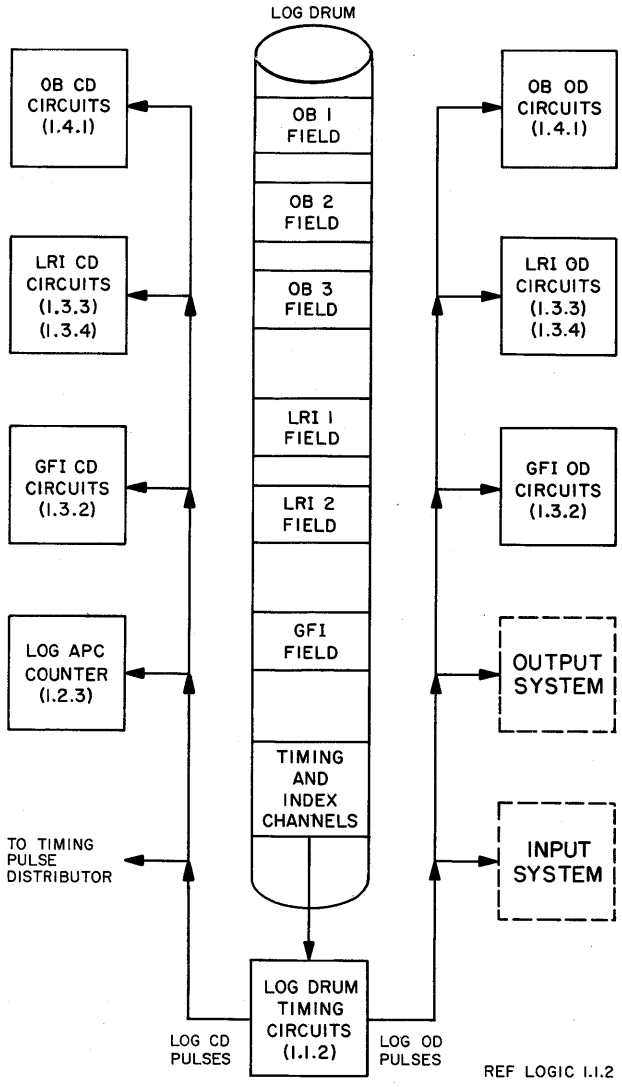


Figure 2–23. LOG Drum Timing Pulse Distribution, Block Diagram

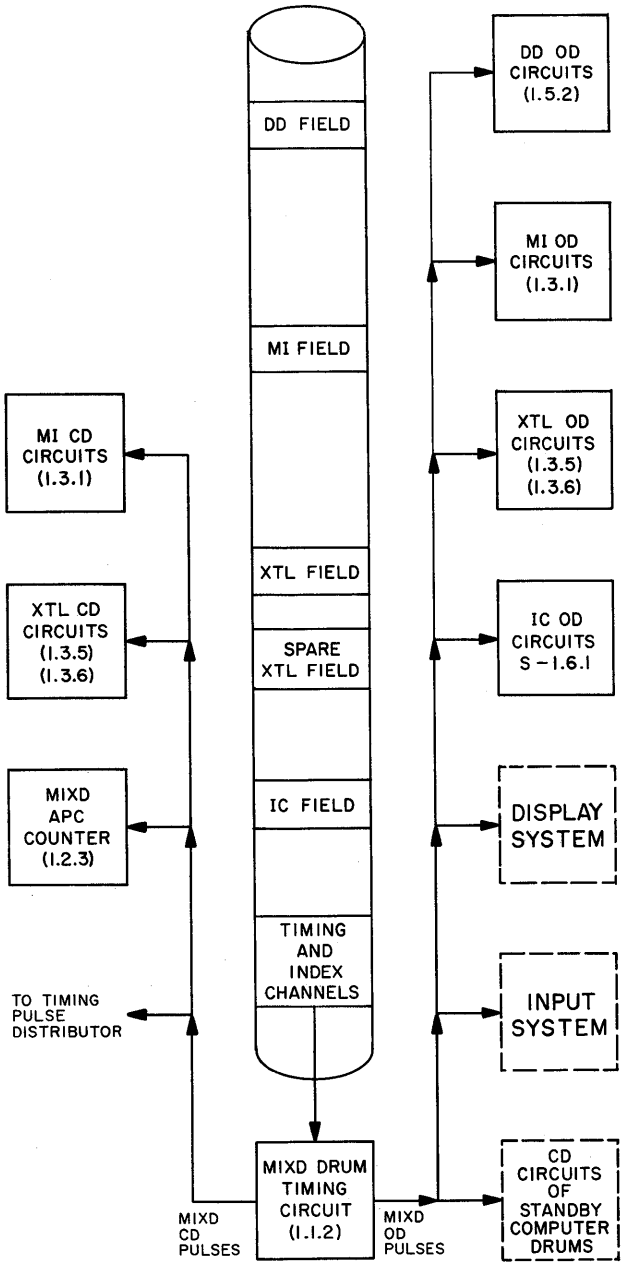


Figure 2–24. MIXD Drum Timing Pulse Distribution, Block Diagram

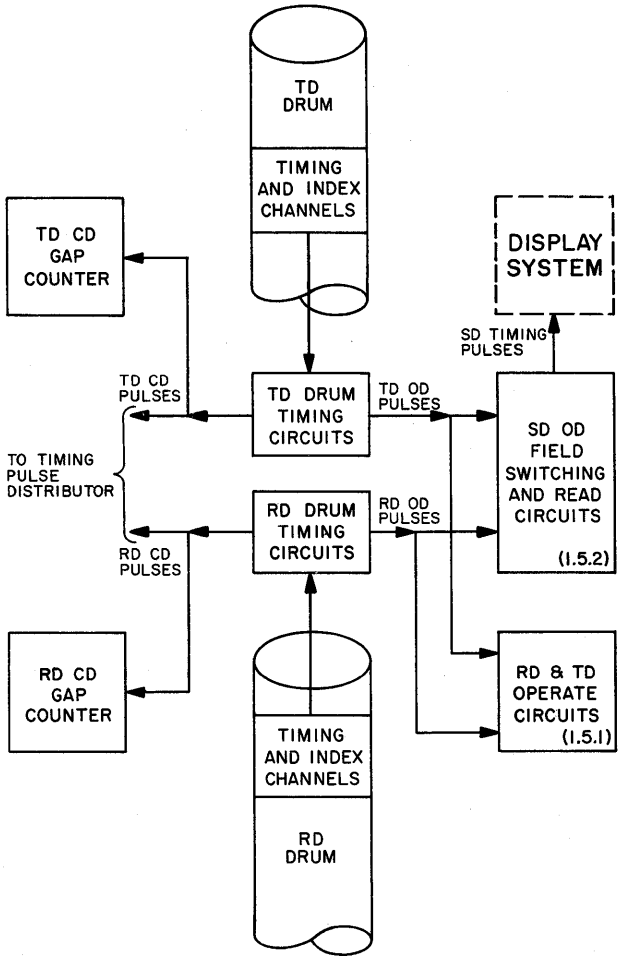


Figure 2–25. TD and RD Drums Timing Pulse Distribution, Block Diagram

CHAPTER 5
FIELD AND DRUM SELECTION

5.1 GENERAL

The intermediate location of the Drum System with respect to other data-handling systems of the equipment affects the transfer of data through the OD side and the CD side of the drums in a different manner. On the OD side, three systems, Input, Output, and Display, are independently connected to the Drum System so that data transfers to and from these systems can be performed simultaneously and at random times as required. However, on the CD side, the Central Computer, which receives and supplies all tactical data, is the only connection to the Drum System. Due to the latter condition, Central Computer programming schedules all CD transfers in such a manner that only one field of the 39 main drum or 36 auxiliary drum fields can be selected at any given time for one data transfer. An incoming CD data transfer implies a reading operation, and an outgoing CD data transfer implies a writing operation involving the field selected.

In addition to reaching all fields for writing or reading on the CD side of the drums as previously mentioned, the Central Computer may reach some of the same fields for writing or reading on the OD side. This operation is available when the computer is in the test mode to allow loop circulation of test data. For example, selecting an LRI test field allows the Central Computer to write LRI test data on the OD side and to read this data on the CD side in the normal manner. Similiarly, OB test data can be written on the CD side, as normally done, and an OB test field can be selected to read the test data on the OD side and return it for comparison to the Central Computer.

In scheduling data transfers with the Drum System, the Central Computer System is only concerned with a select drums *(SDR)* instruction and a field number designation. No individual drum designation is required from the Central Computer since each field selection reaching the Drum System serves to automatically activate the timing circuits in the corresponding drum. Selected drum timing is required to effect the CD transfer.

5.2 FIELD ENCODING

IO transfers to and from Central Computer and drums are initiated by an *SDR* program instruction which selects one of the Drum System fields as the IO transfer device. The *SDR* instruction causes a *deselect* command and a field selection to be applied to the main drums or the auxiliary drums. The *deselect* command appearing in the form of a deselect pulse clears the drum circuits of previous selections. Each new field selection is made through auxiliary bits, L10 through L15, of the computer instruction word.

Six physical lines from the Central Computer connect the auxiliary bits to the main-drum selection circuits (logic 1.1.1) and six other lines perform the same function with the auxiliary drums (logic 1-2, 1.1). Due to the independent auxiliary bit line connections, bit R1 of the instruction word is used at the Central Computer to determine main or auxiliary drums for the transfer. When bit R1 is a 0, the field selection is applied to the main drums; a 1 R 1 bit in the position causes field selection to be applied to auxiliary drums.

When a field is selected by the Central Computer, a pulse combination appears on the six auxiliary bit lines to form an octal expression in terms of octal tens and units. For example, a selection causing all six lines to carry a pulse would represent the octal expression 77 (binary 111 111).

Three of the auxiliary bit lines, L10, L11, and L12, carry the tens octal combination, whereas lines L13, L14, and L15 carry the units. Consequently, assuming that the Central Computer selects field 27, the DD field, a pulse will simultaneously appear on lines L11, L13, L14, and L15 to form the octal expression 27 (binary 010 111). Since lines L10 and L12 represent zeroes in this field selection, no pulse will appear on these lines.

5.2.1 CD Select Field Designation and Function

In the operate mode, Central Computer field selection is made for writing and/or reading on the CD side of the drums. Thus, 39 fields in the main drums and 36 fields in the auxiliary drums are available to the Central Computer for IO transfers with the Drum System. Tables 2–1 and 2–2 supply the listing of designated CD field numbers in the main and auxiliary drums, the write and/or read function performed, and the drum bar affected by each selection.

For better understanding of the following descriptions, refer to definitions of addressable and status fields in paragraph 7.1.

Note that the auxiliary memory fields and all other addressable fields have the dual function of writing

and reading. The status fields have only one function of either writing or reading according to the nature of the data being transferred.

Depending upon the requirements of the program, the Central Computer may select each of the status fields under basic status or identity. However, the drum field selected under either identity or status is physically the same. SDR GFI 32 (STATUS) and SDR GFI 33 (IDENTITY) are an example of two different selections affecting the same physical drum field.

In addition to basic status and identity designations, LRI drum fields are given the SDR LRI-1 50 and SDR LRI-2 51 designations by the Central Computer. Selections 50 and 51 allow the program to choose not only a specific site identity but also a specific message label (ML).

OB selections are normally made by the Central Computer as SDR OB ODD 30 and SDR OB EVEN 31, in alternate order. However, OB operate circuits logic 1.4.1, (Part 4 Chapter 3,) develop from these two selections a pattern which allows writing on drum fields OB-1, OB-2, and OB-3, in rotational order.

SDR IC OWN 26 and SDR IC OTHER 16 are both considered CD selections since they can be effected when the equipment is in the operate mode. SDR IC OWN 26 is the selection used by the Central Computer to read or write on the CD side of its own IC drum field. However, to provide intercommunication between the two computers in duplex equipment, both computers may select IC OTHER 16 to read the OD side of the other IC field.

XTL MARKER 40 is a CD selection made by the Central Computer to write the 1001001001 . . . pattern on the marker channel of XTL fields (Part 4, par. 2.5).

5.2.2 Test Selections, Designation and Function

There are three selections available to the Central Computer for test purposes only: TEST SDR DD 17, TEST SDR SD 47, and TEST SEL IO 76. These selections allow the Central Computer to examine data as it is normally transferred from the Drum System to the Display System or to the alternate duplex Drum System. OD circuit performance of the nine RD, six TD, the DD, and the IC fields is tested by means of these three OD selections.

OD circuit performance of the LRI, OB, GFI, MI, and XTL fields can be tested by the Central Computer without specific test selections. Basic status selections SDR MI 22, SDR XTL 24, SDR OB ODD 30, SDR OB EVEN 31, SDR GFI 32, SDR LRI-1 34, and SDR LRI-2 36, which are available to the Central Computer in the operate mode, can also be utilized in the test mode. When any of these selections is made simultaneously with a DRUMS-IN-COMPUTER-TEST condition, a loop is established to generate test data at the Central Computer, circulate it through the drum field circuit under test, and return it to the Central Computer for comparison.

5.3 FIELD SELECTION DECODING

The pulse pattern appearing at the six auxiliary bit lines at the time of each field selection is applied to selection circuits in logic 1.1.1 of the main drums or logic 1-2,1.1 of the auxiliary drums. The purpose and performance of circuits in either logic is the same; namely, to activate the timing circuits of a specific drum and to provide a driving output at one of 39 drum field drivers (DFD's) in the main drums or one of the 36 DFD's in the auxiliary drums. The DFD with the driving output serves to activate all the information heads mounted in the corresponding drum bar (refer to tables 2–1 and 2–2). The activated heads in the drum bar are thereby enabled to perform the operation of magnetic drum writing or reading.

It follows that the selection circuits function is one of decoding a desired field designation. This decoding function is performed by the following four matrix sections of each selection logic: tens and units decoder, CD field select, drum select, and OD test field select.

5.3.1 Tens and Units Decoder

A simplified diagram of the tens and units decoder section is shown in figure 2–26. This section contains the selection register, the tens decoder matrix, and the units decoder matrix. The selection register consists of six flip-flops which are reset or cleared by the deselect pulse that precedes each field selection. The set side, 1 side, of each flip-flop receives one of the six auxiliary bit lines from the Central Computer circuits.) (Index interval decoder logic 0.6.1 originates main drum selections and miscellaneous IO logic 0.7.7 originates auxiliary drum selections.)

Each new field selection causes the flipflops to be set in accordance with the octal ten and octal unit digits of the field designation. A group of three flip-flops forms the combination for the ten digit, while the other group of three flip-flops forms the combination for the unit digit. Therefore, all combinations possible from each group will fall between the limits of 0 and 7. These combinations are associated at eight AND circuits of the tens matrix and eight AND circuits of the units matrix. By careful tracing in the figure it can be seen that the AND associated with the tens 7 will produce an output level when the three corresponding flip-flops have been simultaneously set by index-interval pulses. Such would be the case in selecting any of the six fields in the AM-F drum (table 2–2). Similar tracing can be made in the case of the AND associated with the tens 4 where only the first flip-flop in the group (L10) is set and the other two (L11 and L12) remain cleared as

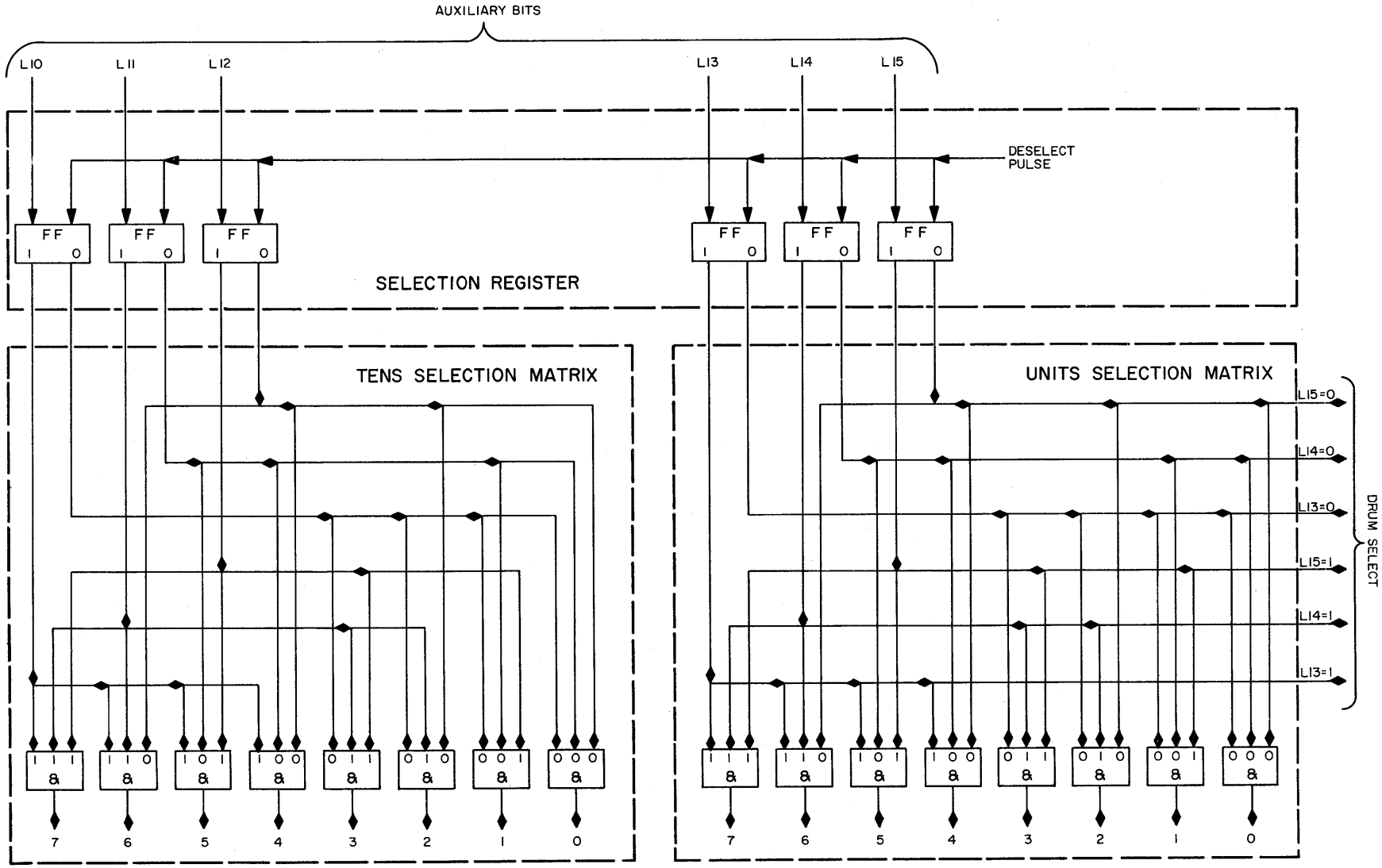


Figure 2–26. Tens and Units Decoder Matrix, Simplified Logic Diagram

determined by the deselect pulse. A tens 4 appears in selecting any of the six fields in the TD drum or the AM-C drum. (Refer to tables 2–1 and 2–2 respectively.)

The units decoder matrix and the group of three associated flip-flops operate in identical manner as described for the tens decoder matrix. In addition, the 0 and 1 outputs from the three flip-flops are connected to the drum select matrix section described in 5.3.3.

The eight outputs available from the tens decoder and the eight outputs from the units decoder constitute the basic decoding process. All other circuits in each drum selection logic are further applications which utilize AND and OR matrices to associate tens and units output levels to form all combinations required in the entire field and drum selection processes.

5.3.2 CD Field Select

The CD field selection section serves to provide an input level to one of the 39 DFD's connected to main drum CD fields (six CD fields per drum in the LOG, MIXD, TD, AM-A, and AM-B drums and nine CD fields in the RD drum). In the auxiliary drums, 36 DFD's are connected to the 36 CD fields available at six fields per drum.

The level appearing at a DFD input is dependent upon the coincidence of specific tens and units levels from the tens and units decoder. It is significant to reiterate that only one of the 75 fields contained in all drums of a system can be affected by CD selection at any one time. However, the same physical drum field may be selected under two different designations, in accordance with program requirements. This condition particularly applies to CD status field data transfers described in 7.1.

5.3.2.1 AM, TD, and RD Drums

Figure 2–27 supplies the example of typical CD field selection such as that affecting the AM-A drum. This drum has been chosen for the typical case because all CD field designations therein contained carry the same tens designation. Drums AM-B through AM-H, TD, and RD are similar to the typical example. The MIXD and LOG drums, however, are somewhat different (par. 5.3.2.2).

Referring to figure 2–27, whenever the tens 0 and units 2 levels are coincident at AND 1 (SEL AM-A1), a +10V level appears at the input of DFD 1. This DFD, in turn, produces the +125V driving output connected to all information heads in bar 1 of the AM-A drum. At the same time, the other 38 DFD's in the main drums and the 36 DFD's in the auxiliary drums receive a −30V input level. Therefore they all produce the quiescent output of +70V. (Refer to the Special Circuits manual, 3-3-0.)

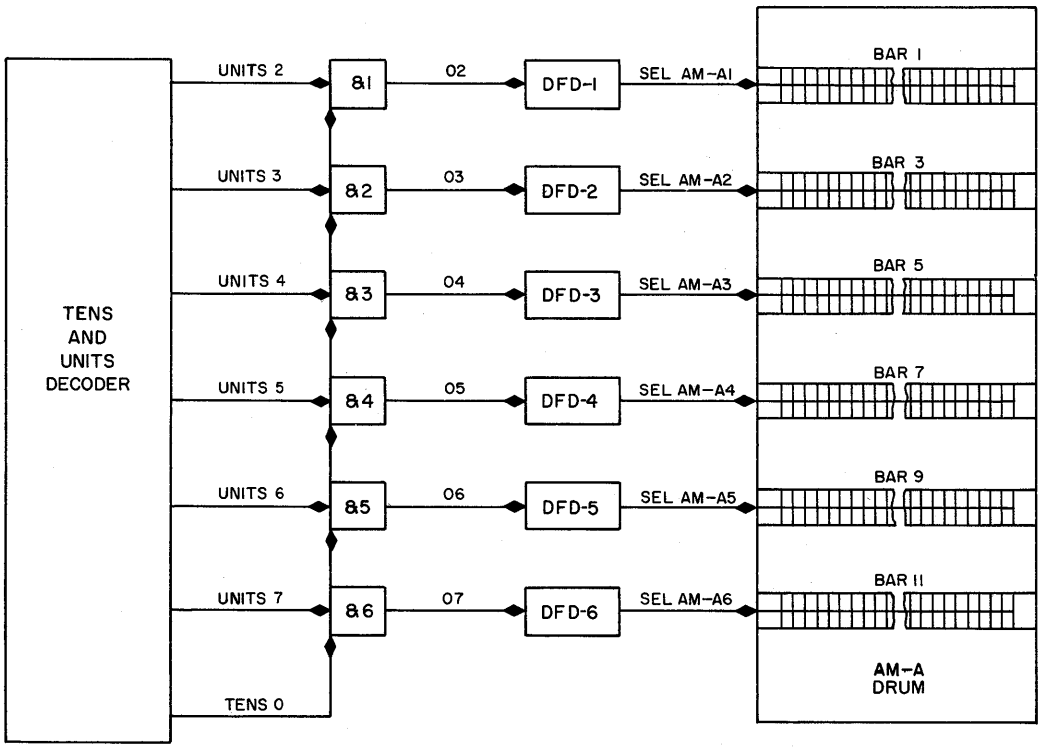


Figure 2–27. AM-A Drum CD Field Selection Circuit, Simplified Logic Diagram

TABLE 2–1. MAIN DRUMS CD FIELD DESIGNATION AND FUNCTION

FIELD NAME	FIELD OCTAL DESIGNATION	DRUM BAR NUMBER	FIELD FUNCTION
AM-A DRUM			
SEL AM-A1	02	1	Write-read
AM-A2	03	3	Write-read
AM-A3	04	5	Write-read
AM-A4	05	7	Write-read
AM-A5	06	9	Write-read
AM-A6	07	11	Write-read
AM-B DRUM			
SEL AM-B7	10	1	Write-read
AM-B8	11	3	Write-read
AM-B9	12	5	Write-read
AM-B10	13	7	Write-read
AM-B11	14	9	Write-read
AM-B12	15	11	Write-read
MIXD DRUM			
SEL SP XTL	20	11	Write-read
SP AM	21	2	Write-read
MI (STAT)	22	7	Read
MI (IDENT)	23	7	Read
XTL (STAT)	24	9	Read
XTL (IDENT)	25	9	Read
SEL XTL MARKER	40	9, 11	Write
IC OTHER	16	3	Read
IC OWN	26	1	Write-read
IC TEST	76	3	Read
DD TEST	17	6	Read
DD	27	5	Write-read
LOG DRUM			
SEL OB ODD	30	1	Write (OB-1)
OB EVEN	31	3	Write (OB-2)
		5	Write (OB-3)
GFI (STAT)	32	7	Read
GFI (IDENT)	33	7	Read
LRI-1 (STAT)	34	9	Read
LRI-1 (IDENT)	35	9	Read
LRI-1 (IDENT)	50	9	Read
LRI-2 (STAT)	36	11	Read
LRI-2 (IDENT)	37	11	Read
LRI-2 (IDENT)	51	11	Read
TD DRUM			
SEL TD-1	41	1	Write-read
TD-2	42	3	Write-read
TD-3	43	5	Write-read
TD-4	44	7	Write-read
TD-5	45	9	Write-read
TD-6	46	11	Write-read
RD DRUM			
SEL RD-1	60	1	Write-read
RD-2	61	3	Write-read
RD-3	62	5	Write-read
RD-4	63	7	Write-read
RD-5	64	9	Write-read
RD-6	65	11	Write-read
RD-7	66	3	Write-read
RD-8	67	7	Write-read
RD-9	70	11	Write-read
TEST SEL SD	47	All OD bars, TD and RD drums	Read

TABLE 2–2. AUXILIARY DRUMS, CD FIELD DESIGNATION AND FUNCTION

FIELD NAME	FIELD OCTAL DESIG-NATION	DRUM BAR NUMBER	FIELD FUNCTION
AM-C DRUM			
SEL AM-C13	41	1	Write-read
AM-C14	42	3	Write-read
AM-C15	43	5	Write-read
AM-C16	44	7	Write-read
AM-C17	45	9	Write-read
AM-C18	46	11	Write-read
AM-D DRUM			
SEL AM-D19	51	1	Write-read
AM-D20	52	3	Write-read
AM-D21	53	5	Write-read
AM-D22	54	7	Write-read
AM-D23	55	9	Write-read
AM-D24	56	11	Write-read
AM-E DRUM			
SEL AM-E25	61	1	Write-read
AM-E26	62	3	Write-read
AM-E27	63	5	Write-read
AM-E28	64	7	Write-read
AM-E29	65	9	Write-read
AM-E30	66	11	Write-read
AM-F DRUM			
SEL AM-F31	71	1	Write-read
AM-F32	72	3	Write-read
AM-F33	73	5	Write-read
AM-F34	74	7	Write-read
AM-F35	75	9	Write-read
AM-F36	76	11	Write-read
AM-G DRUM			
SEL AM-G37	02	1	Write-read
AM-G38	03	3	Write-read
AM-G39	04	5	Write-read
AM-G40	05	7	Write-read
AM-G41	06	9	Write-read
AM-G42	07	11	Write-read
AM-H DRUM			
SEL AM-H43	10	1	Write-read
AM-H44	11	3	Write-read
AM-H45	12	5	Write-read
AM-H46	13	7	Write-read
AM-H47	14	9	Write-read
AM-H48	15	11	Write-read

Similarly, the coincidence of tens 0 with units, 3, 4, 5, 6, or 7 produces an output from AND 2, 3, 4, 5, or 6, respectively. The DFD receiving the level from one of these AND circuits, in turn, produces the +125V driving output connected to the information heads in the corresponding bar of the AM-A drum.

5.3.2.2 MIXD and LOG Drums

CD field selection in the MIXD and LOG drums is somewhat different from the other drums in the system due to the transfer of data in two different directions and the address and status methods of data transfer. The LOG drum transfers LRI and GFI incoming status fields data, and OB outgoing status fields data. The MIXD drum transfers MI and XTL incoming status fields data and IC and DD outgoing addressable field data. For clarity, incoming data and outgoing data fields will be treated separately in the following discussions.

Figure 2–28 illustrates the CD field selection circuits related to incoming data in the MIXD and LOG drums. In addition to the tens-units combinations of preceding descriptions, the basic status CD selection of each of these fields carries with it the TEST SEL designation of the same field. In the operate mode, this TEST selection has no effect since the test circuits are fully deactivated. However, in the test mode, the test circuits

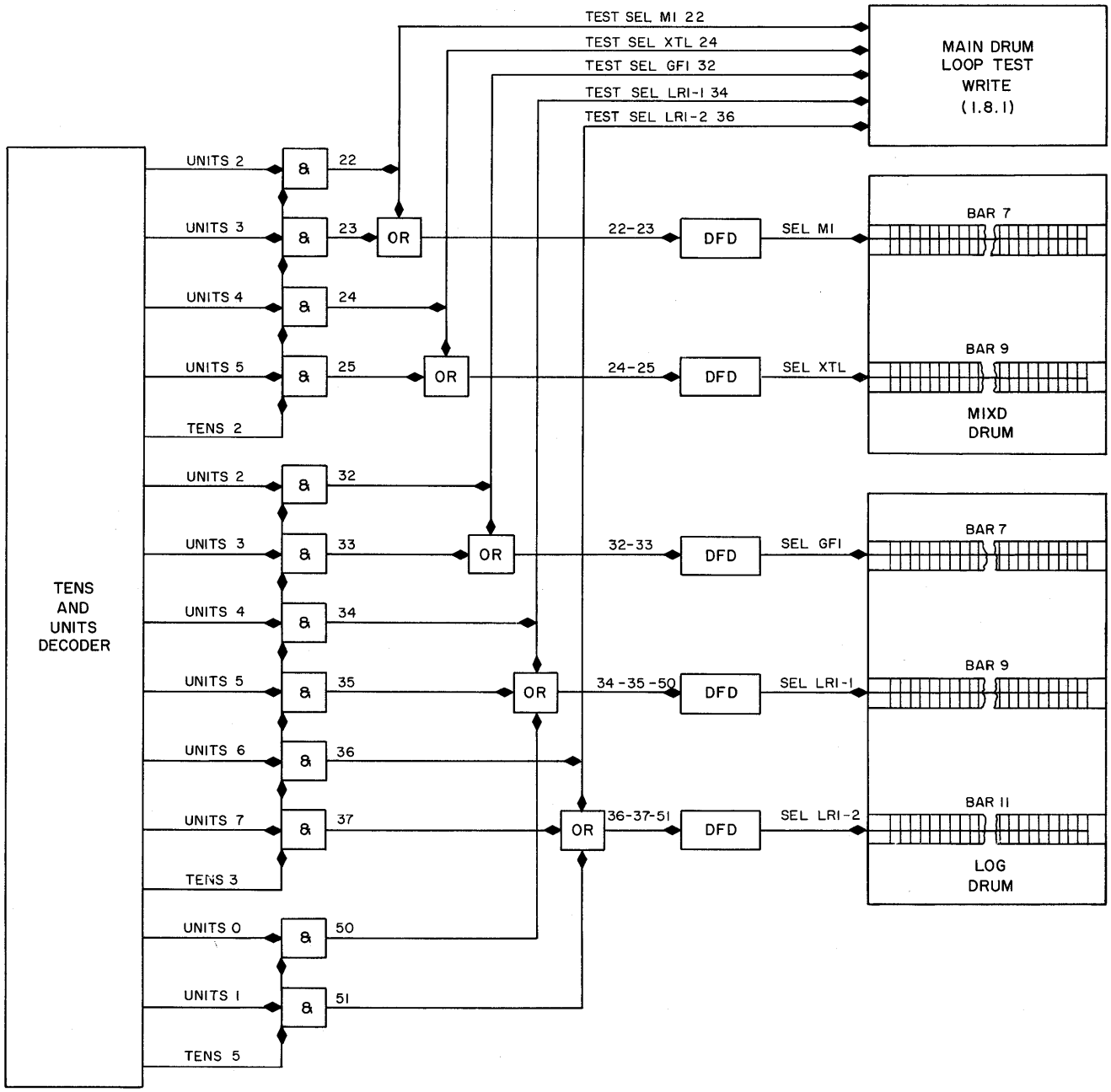


Figure 2–28. MIXD and LOG Drums Incoming Data CD Field Selection, Simplified Logic Diagram

become activated, effectively providing for a dual, CD-OD, selection of the same drum field. The dual field selection is necessary to the status-transfer control circuits which operate on a chain-reaction pattern affecting both the CD and OD sides of the field (par. 7.7.1).

MIXD and LOG drum fields transferring outgoing data are illustrated in figure 2–29. Notice that CD field selections of the OB fields automatically carry the TEST selection of the same fields in the identical manner described above for the incoming data status fields. Likewise, TEST selection of OB fields becomes active only in the test mode.

The IC and DD fields data-transfer control circuits perform independently for the CD and OD sides of each field. For this reason, the CD designation, SDR IC 26 – and SDR DD 27, of these fields do not automatically carry their counterparts on the OD side (TEST SEL IC 76 and TEST SEL DD 17).

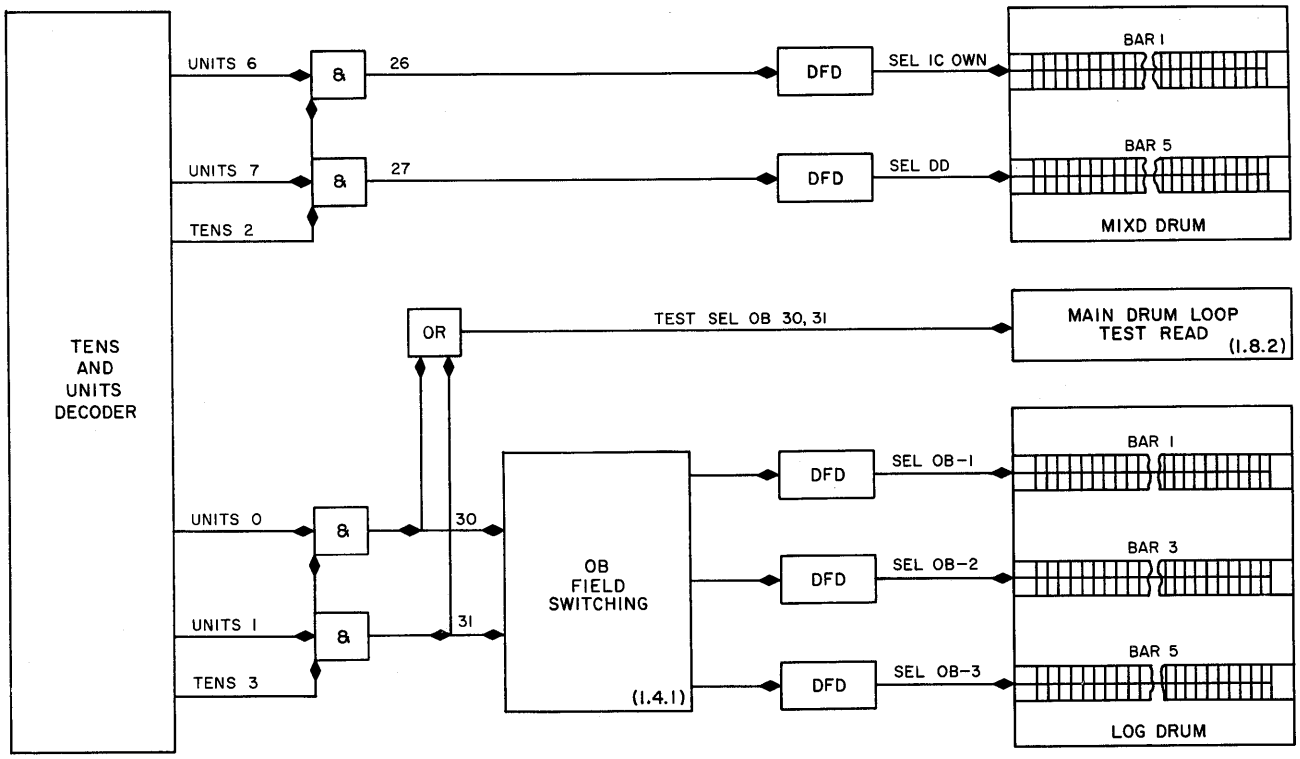


Figure 2–29. MIXD and LOG Drums Outgoing Data CD Field Selection, Simplified Logic Diagram

5.3.3 Drum Select

The purpose of drum select is to release drum timing pulses CD-IX, CD-1, and CD-3 to the corresponding field operate logic. Drum timing pulses are continuously generated by each rotating drum and are applied to gate circuit inputs in the pulse distributor, logics 1.1.2 and 1-2.1.2. However, drum timing pulses are released only when a drum-select level from the drum-select matrix section is present to condition the gates. Figure 2–30 shows the main-drum-select matrix section in its simplified form. This matrix section receives input levels from the flip-flops and the AND circuits in the tens and units decoder described in paragraph 5.3.1. The object of AND and OR circuits in the matrix is to insure that a select drum level is only produced when one of the fields contained in the drum is selected. For example, the CD fields contained in the RD drum are 60 through 67, and 70. Therefore, the 0 outputs from the three unit flip-flops are associated in an AND circuit whose output level is, in turn, associated with a tens 7 level at a second AND circuit. The output from this second AND circuit indicates the presence of SDR 70 from the Central Computer. A tens 6 level is present for any selection between SDR 60 and SDR 67. Consequently, the SDR 70 level and the tens 6 level are associated at an OR circuit which produces the SEL RD level whenever SDR 60 through 67 or SDR 70 have been made by the Central Computer.

The SEL MIXD level involves a larger AND and OR circuit combination because of different field designations affecting the MIXD drum. Tracing the level flow in the figure will lead to understanding the combinations which ultimately form the SEL MIXD level. Notice that field designations 20, 21, 26, 27, and 40 which produce this level apply to addressable fields. Therefore, the SEL MIXD level as shown in the figure serves to complete addressable field transfers in the MIXD drum (refer to par. 7.4). In addition to the above, two other drum select levels, not shown in the figure, affect the MIXD drum. One level is produced by the presence of status fields SDR MI 23 or SDR XTL 25; the other level serves to release CD IX pulses upon the presence of any selection in the 20's series (refer to 4.3.1).

The SEL TD, SEL LOG, SEL AM-A, and SEL AM-B levels are developed in a manner analogous to that described for the RD and MIXD drum select levels. AND and OR circuit combinations are needed due to the specific field designations involved in these drums.

Select drum level generation for the auxiliary drums AM-C through AM-H is somewhat simpler due to the uniform field designations in each drum. Thus, a select drum level is automatically generated by the tens level from each corresponding field selection. Reference to logic 1-2.1.1 and to table 2–2 reveals that a tens 0 generates a SEL AM-G; a tens 1 generates a SEL AM-H;

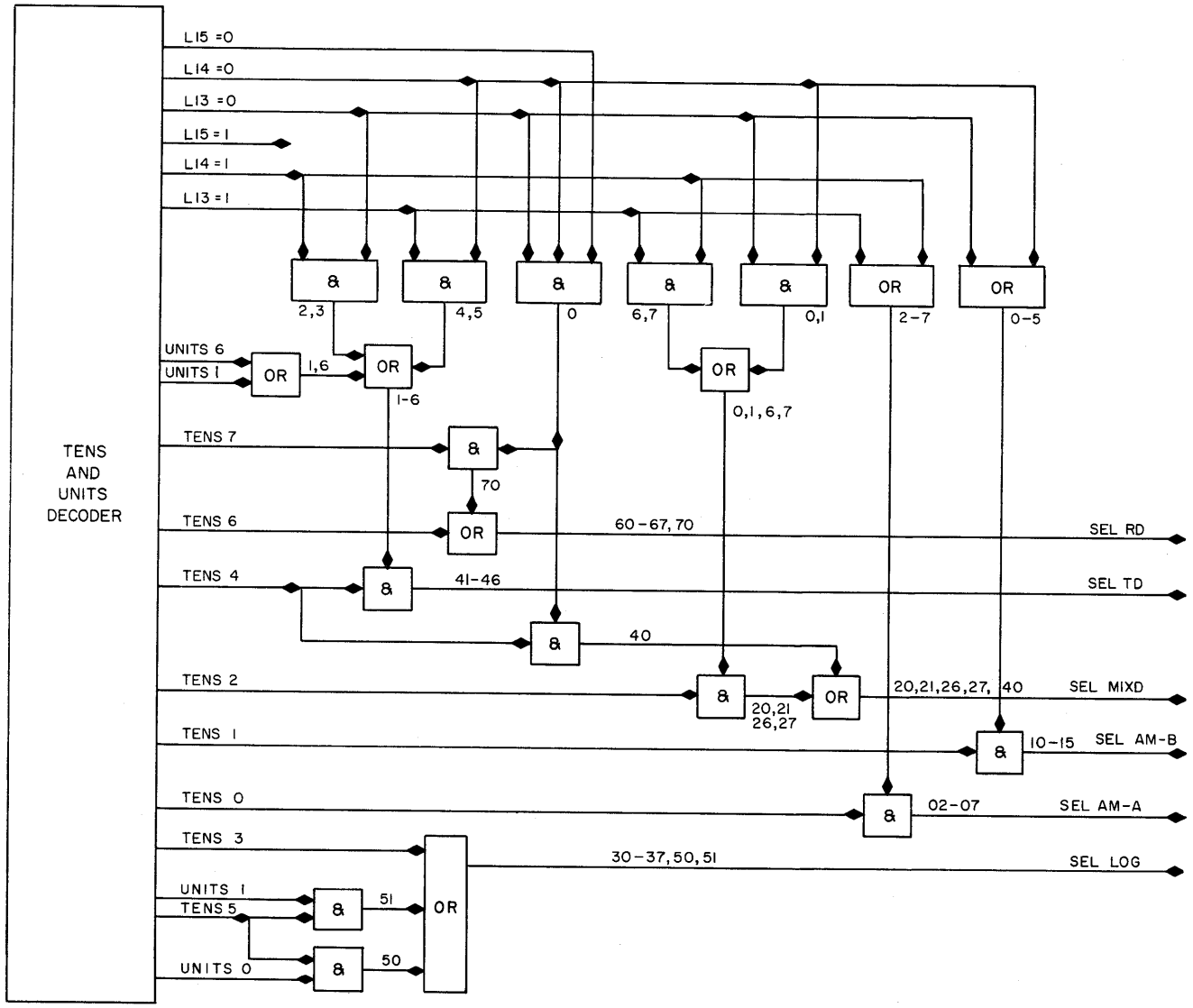


Figure 2-30. Main-Drum-Select Matrix, Simplified Logic Diagram

a tens 4 generates a SEL AM-C; a tens 5 generates a SEL AM-D; a tens 6 generates a SEL AM-E; and a tens 7 generates a SEL AM-F level.

5.3.4 Operation of Test Selections

Selections affecting the OD side of drums apply to the testing of all drum fields except auxiliary memory fields. Because auxiliary memory fields are only associated with the Central Computer, there is no OD operate logic to these fields. When test selections are made in the test mode, a connection is made automatically to the Central Computer from each OD bus line carrying messages into and out of the Drum System. Thus, under SDR 47, (TEST SEL SD), the six OD fields of the TD drum and the nine OD fields of the RD drum are selected and a connection is established from the SD bus line to the Central Computer. Since the 15 SD fields are read on the OD side, the operation involved becomes an OD test read operation (5.3.4.1). The same condition is true in the case of SDR 17 (TEST SEL DD), SDR 76 (TEST SEL IC) and SDR 30-31 which affect the OD side of the DD, IC, and OB fields, respectively.

A similar condition of CD field selection is present when testing status fields MI, XTL, GFI, LRI-1, and LRI-2. In these cases, basic status field selections are employed by the Central Computer so that test data can be consecutively written on, and read from, all registers of the drum field under test. A basic status selection activates the CD field to read and also allows for computer test data to be written on the OD side of

the same field when the drums are set to the DRUMS-IN-COMPUTER-TEST condition.

5.3.4.1 OD Select Test Reading

The normal transfer of DD intelligence from the Central Computer to the Display System illustrated in figure 2–31, has been chosen to describe the test selection operation involved in OD test reading. A permanent connection from the DD bus line as well as from the OB, SD, and IC OWN bus lines is brought to a common OR circuit leading to the test read gates.

In the operate mode, the absence of test selections and manual control levels result in no OD test read level to condition the test read gates. Therefore, even though each word transfer in the bus lines reaches the gates input, no return of data to the Central Computer is possible.

In the test mode, however, an OD test read level will be present at the test read gates provided that a test selection (SDR 17, 30-31, 47, or 76) is made and that the manual controls are set to, DRUMS-IN-COMPUTER-TEST (refer to par. 1–1 of Part 5). Each test selection serves to complete the requirements to produce the OD test read level to condition the corresponding field operate circuits and to activate the corresponding CD field. Other test selections shown have identical application.

5.3.4.2 OD Select Test Writing

The transfer of MI data from the Input System to the MI drum field has been depicted in figure 2–32 to describe test field selections in an OD test write operation. The information output from the MI status control, logic 1.3.1, is applied to the drum write heads through a set of 33 OR circuits. The second input to each OR comes from the output of the 33 test write gates. Notice that these gates receive test data from the Central Computer. However, the OD test write level is required to condition the gates to pass the test data. The OD test level is present only in the test mode, when a basic status field selection (22, 24, 32, 34, or 36) has been made and the manual controls are set to DRUMS-IN-COMPUTER-TEST. In a manner identical to that described in the paragraph above, each test selection

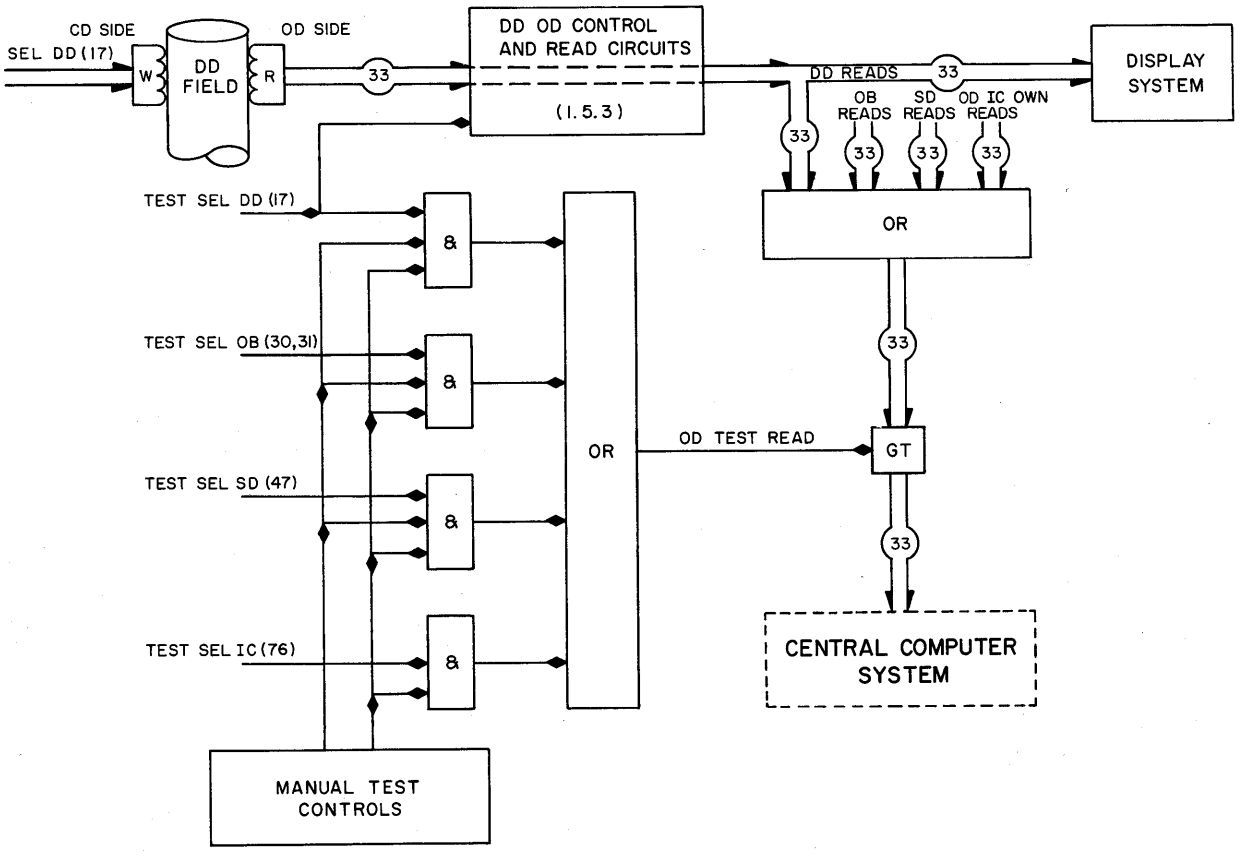


Figure 2–31. Test Field Selections for OD Test Read, Simplified Logic Diagram

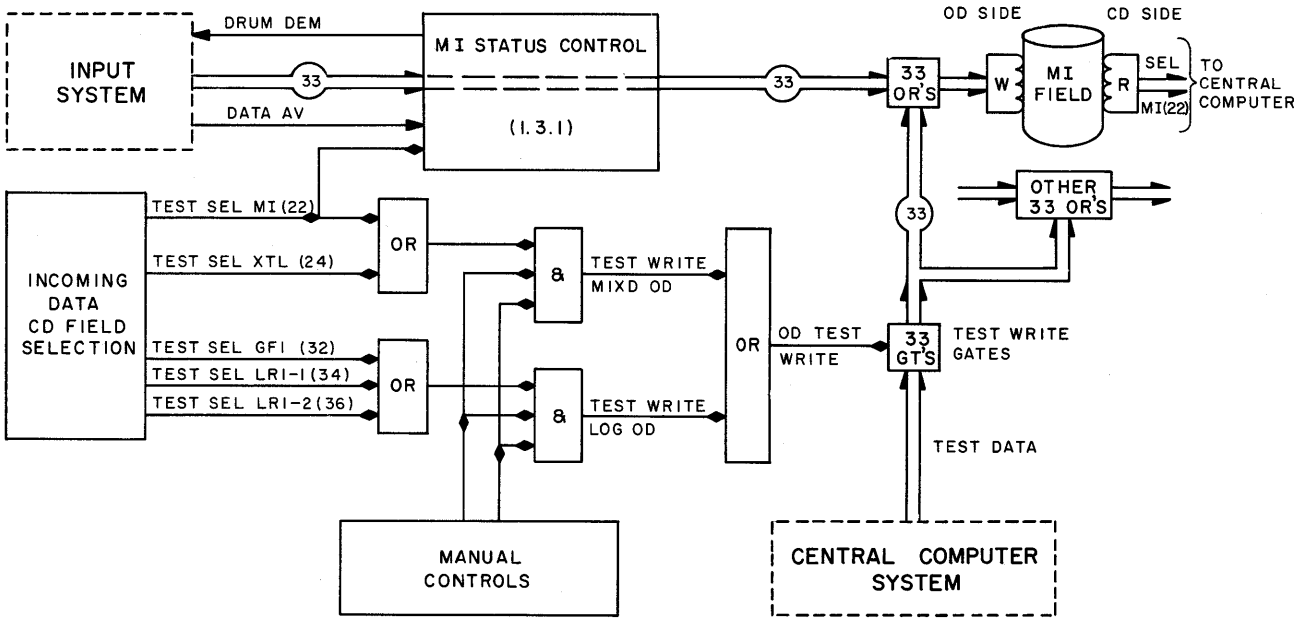


Figure 2–32. Test Field Selections for OD Test Write, Simplified Logic Diagram

level contributes to producing an OD test write level, to conditioning its corresponding operate circuits, and to activating the corresponding CD field.

Reference to the figure reveals that the output of the test write gates is simultaneously applied to other sets of 33 OR circuits. Each 33-OR set is connected to the input of the following status control logics: MI, 1.3.1; GFI, 1.3.2; LRI-1, 1.3.3; LR-2, 1.3.4.; and XTL, 1.3.5. The output of each 33-OR set goes to the OD side of the respective drum field.

CHAPTER 6

FIELD AND DRUM DIODE SWITCHING

6.1 GENERAL

Field and drum switching is a complementary action to field and drum selection. In fact, going from one field selection to another or exchanging write-read operations implies a switching action. Such action is reflected upon the selected field or, more concisely, upon the information heads mounted on one specific drum bar. The information heads in the CD field selected are enabled by the output (+125V) of one DFD, while the information heads in all other CD fields are fully disabled, also by the output (+70V) of their corresponding DFD's. Once the information heads of the selected field are enabled or energized, a concluding operation of storing (write) or withdrawing (read) information is to be performed by the heads.

To single out one CD field from 74 other CD fields and to cause writing or reading by this field, a complex diode switch network is employed as part of Drum System logics 1.1.1, 1.1.1-2, and 1-2.1.1.

Figure 2–33 serves two purposes. First, it shows how the 33 information heads in each field are connected to one 33-common line in each drum; the 33-common lines from the six main drums, in turn, are connected to one 33-main which goes directly to the write and read control circuits. Second, the figure indicates the location of diode switches at each field, at each drum, and at the 33-main connected to the read circuits. A diode symbol in the figure represents 66 actual diodes (each head has one diode in each of the two connecting wires).

The field and drum diode switches act as check valves to allow any one field selected to be placed in direct communication with the write or read circuits. During a write operation the read circuits are disconnected through the action of the read diode switch; information from the CD write bus is thereby applied to the heads in the selected field. When a CD READ level is present, the read diode switch becomes conductive. As a result, the heads of the selected field transmit information stored on the drum surface directly to the 33 drum read amplifiers (DRA's) and to the CD read bus.

6.2 DIODE SWITCH, DRUM LAYOUT

Even though the overall layout of field and drum switching was discussed in the preceding paragraph, a more detailed presentation will lead to better understanding of the entire diode network. Figure 2–34 is an expansion of the AM-A drum symbology shown in figure 2–33. Because of the multiplicity of identical operating items, such as 33 heads simultaneously energized from one DFD, a thorough schematic drawing becomes excessively large. Therefore, in figure 2–34 an attempt is made to present field diode switching and drum diode switching layout as apply to bits P, LS, L1, R13, R14, and R15 of the AM-A drum. Bits not shown follow identical configuration.

The diodes are classified into field switch and drum switch diodes. In the figure, the field switch diodes are all those connected to the head terminals. The drum switch diodes appear along the lower edge of the drawing. Since each bit employs two diodes, there are 66 diodes per field and 396 diodes in six fields, a total of 462 diodes, including drum switching, in the AM-A drum.

The field switch diodes are mounted in pluggable cans inserted in the right and left shelves of each drum assembly. The drum switch diodes are mounted in similar pluggable cans inserted in the inside frame of the drum housing unit. (Refer to 2.3.3.4 of Part 1.)

6.3 DIODE SWITCHING OPERATION

It was mentioned in previous paragraphs that diode switches perform the function of check valves which allow the 33 heads of a selected CD field to be in direct connection with 33 drum writer circuits (DR's) or 33 drum read amplifiers (DRA's). The so-called check-valve operation of each field and drum diode switch is based on the +125V output from the DFD in the selected field and the +70V output from all of the other 74 DFD's in the system. Thus, if +125V is applied to the plate and +70V to the cathode, the diode conducts. On the contrary, if the plate has +70V and the cathode +125V, the diode does not conduct.

In the case of the read diode switch, the condition is quite similar. The plates of these diodes will have +125V at each field selection. However, when the field has been selected for reading, the cathode of each diode receives +100V, which makes the diodes conductive, thereby placing 33 heads of the selected field in contact with 33 DRA's. When the field has been selected for writing, the plates again receive +125V but the cathodes

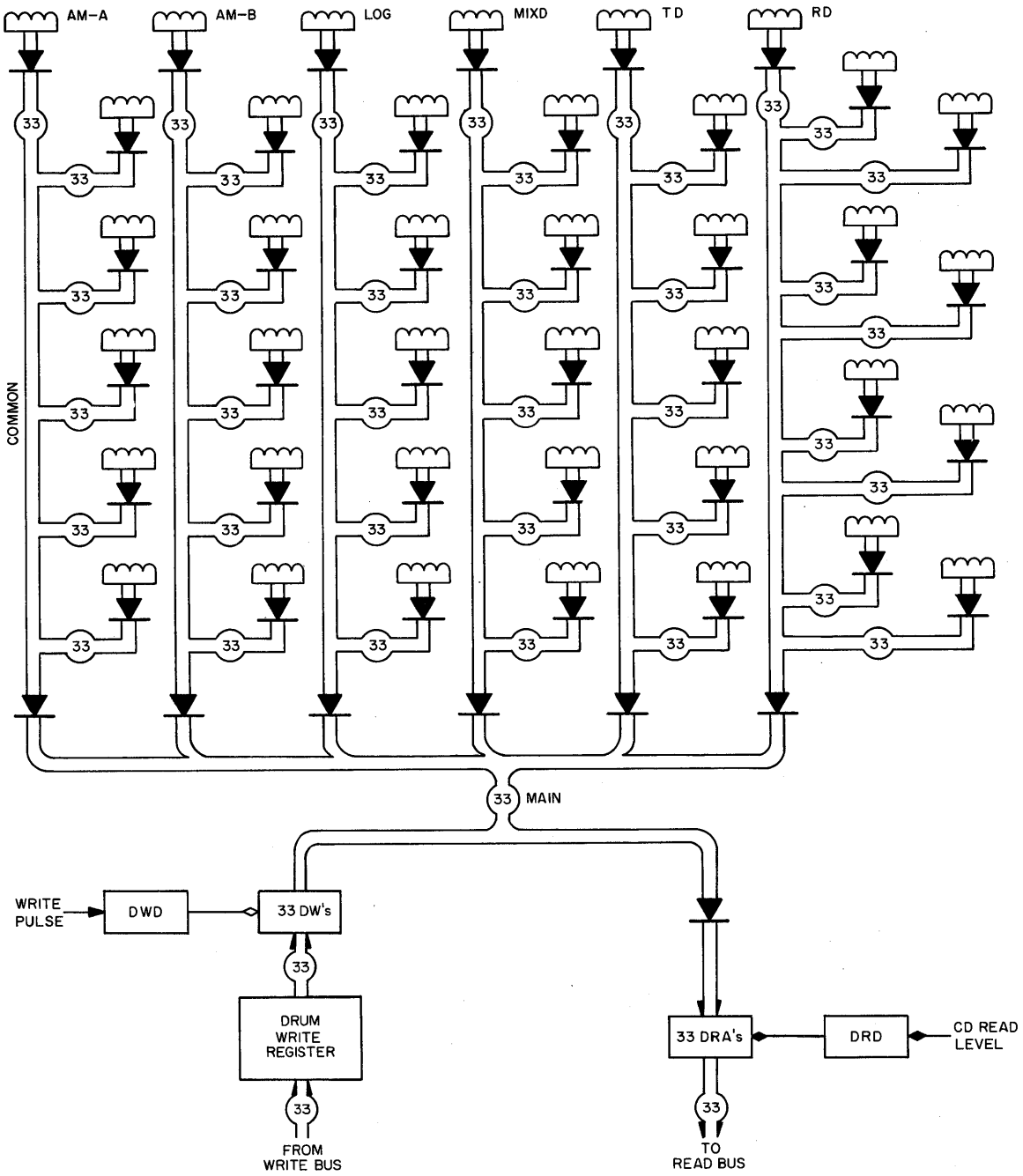


Figure 2–33. Diode Switching, Main Drum Network

receive +150V. This condition prevents conductivity through the diodes and effectively disconnects the DRA's from active operation.

The interrelated operation of diode switches has been summarized in the schematic diagram of figure 2–35. Two symbolic drums, A and B, with two fields each and one magnetic head in each field are shown for the purposes of this discussion.

Assume that field 1 in the figure has been selected. As a result, DFD-1 will produce a +125V output, while DFD's 2 through 4 will produce +70V. The +125V output is applied to terminal 4, center tap, and appears at terminals 3 and 5 of the head. From this point, the associated field switch and drum switch diodes lie in series with the plates of the two tubes in the drum writer (DW) and the plates of the read switch diodes.

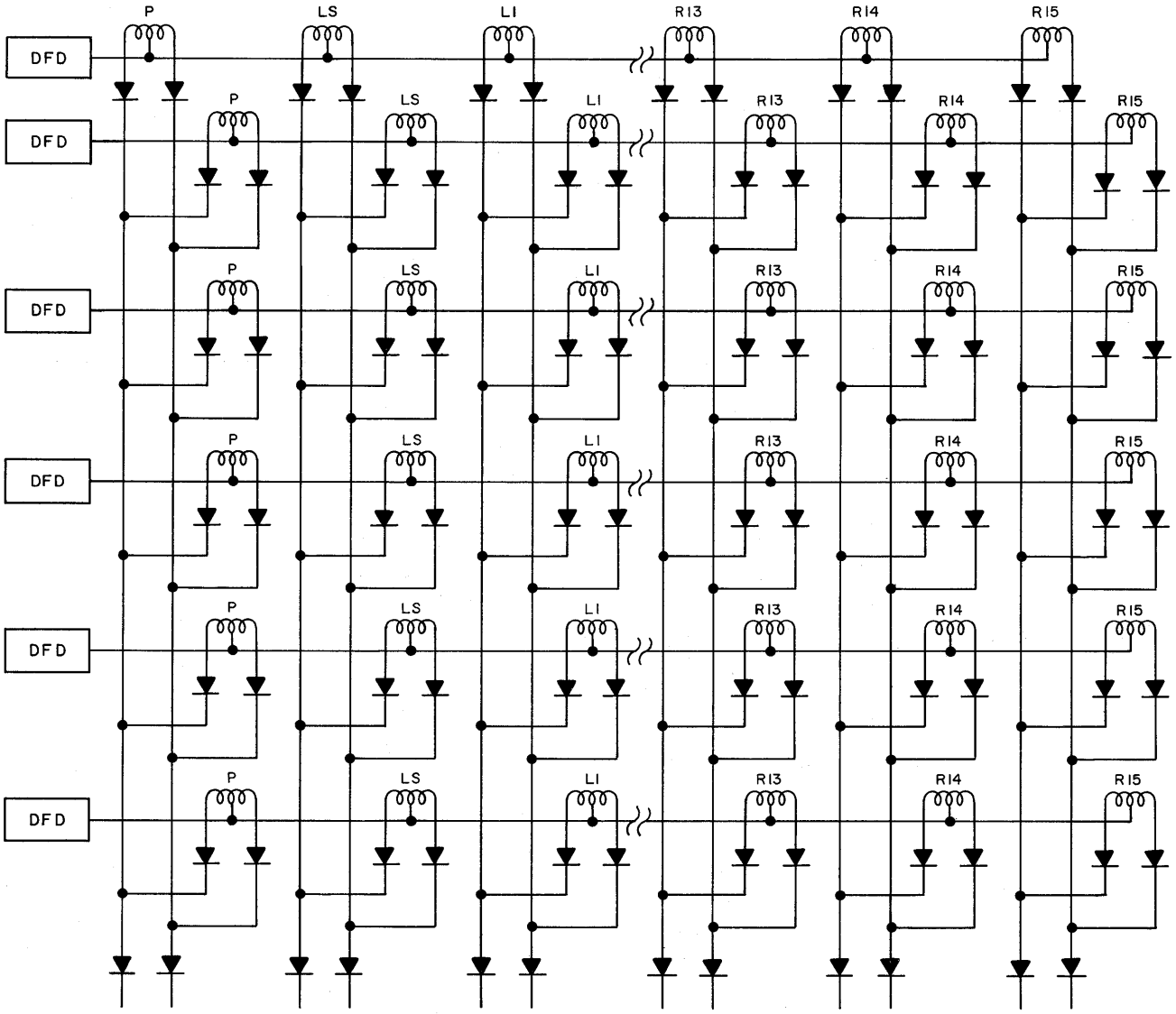


Figure 2–34. Field and Drum Diode Switch Layout in the AM-A Drum, Simplified Schematic

In other words, plate voltage for the vacuum tubes in the DW and the read switch diode plates comes from the DFD related to the selected field. Regarding the field 2 switch diodes in drum A, the plates receive +70V from DFD-2 and the cathodes receive +125V from the selected field head; therefore, field 2 is effectively disconnected. The two fields in drum B receive +70V from DFD's 3 and 4; therefore, +70V appear at the plates of the drum switch diodes. The cathodes of these diodes receive +125V from drum A; therefore, the entire drum B is effectively disconnected.

At this stage of the discussion, +125V from the selected field DFD is made available to the DW and the read diode switch. The write or read operation which may ensue is dependent upon the following conditions. For writing, a write pulse causes the drum write driver (DWD) to condition the DW so that the 0 or 1 state of the drum write register flip-flop can be recorded by the head as a 0 or 1 bit. Simultaneous with this operation, the absence of a CD read level causes the DRD to produce a +150V output applied to the center tap of the DRA input transformer. (Refer to special circuits manual 3-3-0.) This +150V appears at the cathode of the read switch diodes, effectively disconnecting the DRA during the write operation.

For reading, the CD read level is present during the entire operation; therefore, a +100V output from the DRD appears at the cathodes of the read switch. In this condition, +125V at the plates and +100V at the cathodes, the read switch diodes are conductive and the

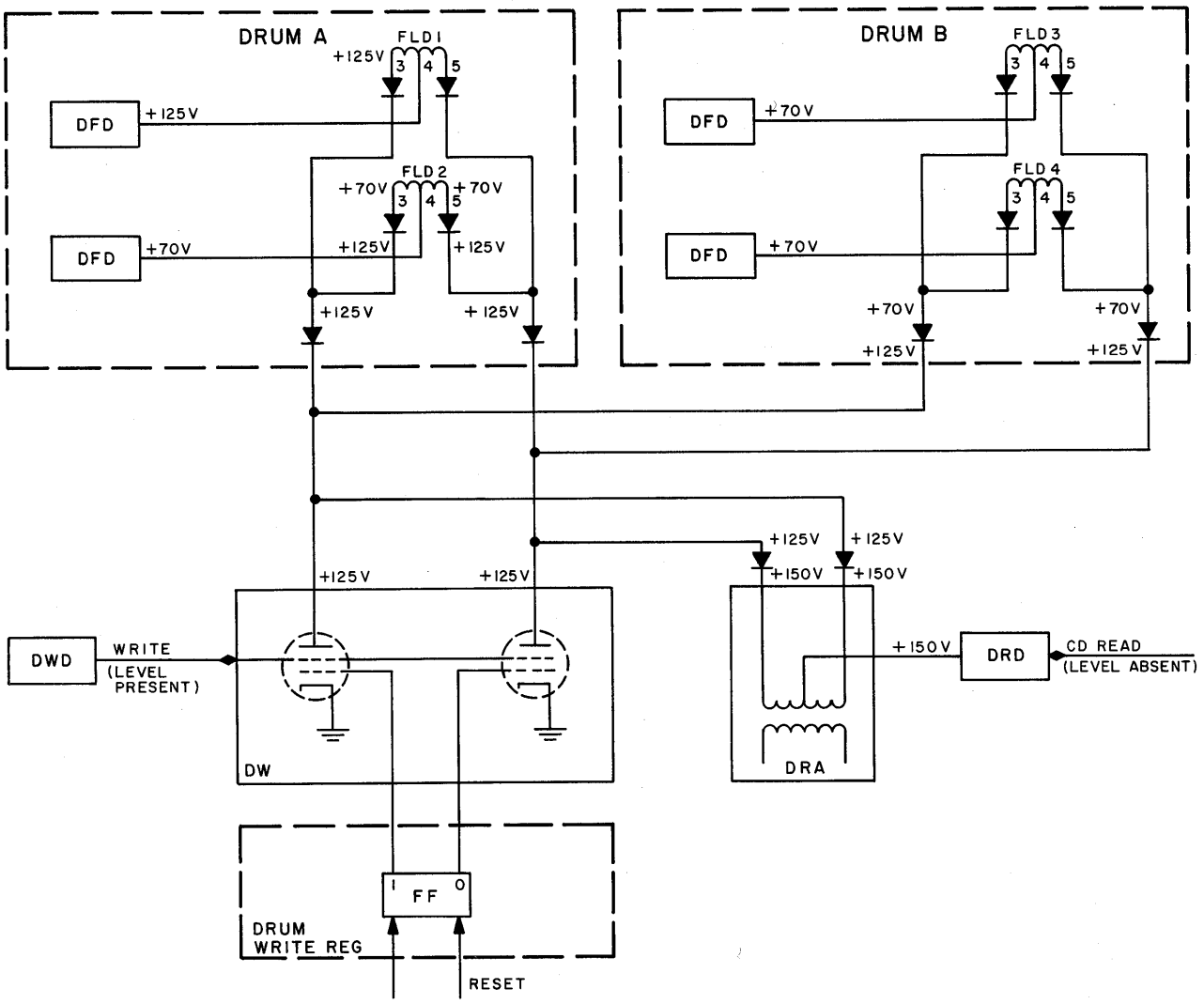


Figure 2–35. Typical Diode Switch Operation, Schematic Diagram

DRA receives the 0 or 1 bit signal previously recorded on the drum surface. Coincidentally, the write pulse is absent; therefore the DW is deconditioned and effectively disconnected during the read operation.

The understanding of diode switching achieved from the previous discussion can be directly applied to the actual diode network as found in the main and auxiliary drums of the system.

CHAPTER 7
COMPUTER-DRUM DATA TRANSFER CONTROL

7.1 GENERAL

The control of data transfers between the Central Computer and the Drum Systems is actually the second and concluding step to be observed in the overall performance of a data transfer. The previous step is selection of a drum field by the Central Computer, as described in Chapter 5. Therefore, the following discussions are based on the assumption that the field selection decode operation is complete. In other words, the information heads in the corresponding drum bar are energized with +125V.

To recapitulate, a field selection is the result of a *Select Drums* instruction in the Central Computer. This selection is preceded by a Central Computer deselect pulse which clears the field selection and CD data transfer control circuits in the Drum System. After field selection, a *Read* or *Write* instruction is given by the Central Computer and a corresponding start-read or start-write pulse is received by the Drum System.

When the above preparatory requirements are fulfilled, the Drum System activates the necessary control circuits to perform the transfer. Such transfer can be performed by one of two methods, namely, address or status. Under the address method, the Central Computer selects a block of address locations, or drum registers, and gives instructions to transfer the entire block to or from (write or read) the drum in consecutive order of registers. Under the status method, the Central Computer gives instructions for transfer to the drum (write) when a word request is issued by the drum as a result of an empty register or registers; or it gives instructions for transfer from the drum (read) of the information contained in any register of the field selected. Reading of status fields is performed by the Central Computer under one of two CD field selection designations. The first designation is basic status where the program allows information in all transfers to be accepted for further process. The second designation is status identity where the site identity of each incoming message (bits R11 through R15) is examined by the Central Computer. Acceptance of the message, in this case, depends upon favorable comparison with program requirements.

Each of the 75 operate fields available in the Drum System is assigned a specific method of CD transfer. Thus, all 36 fields in the auxiliary drums of unit 20 are addressable. In the main drums, all 27 fields in the AM-A, AM-B, TD, and RD drums are addressable fields. In the MIXD drum the IC, DD, SP AM, and SP XTL are addressable fields. Notice, however, that the SP XTL field is basically a status field presently being utilized for auxiliary memory purposes. The remaining two fields, MI and XTL, in the MIXD drum are status fields as are all six fields, LRI 1, LRI 2, OB 1, OB 2, OB 3, and GFI, in the LOG drum.

Figure 2–36 shows the interrelation of the read-write control, addressable control, read circuits, and write circuits of the auxiliary drums computer-drum data transfer control. This area of the Drum System is covered by logics 1-2.2.1 and 1-2.2.2. Figure 2–37 represents the equivalent area in the main drum group. This area is covered by logics 1.2.1 and 1.2.2. The similarity existing between these two illustrations denotes the identical operation of the circuit areas which are common to both. To clarify, the computer-drum data transfer control in the auxiliary drum group is identical in circuit layout to the addressable field transfer control in the main drum group. The fact that status field control is also exercised by the main drum group determines the difference. In view of the identical addressable field operation in the two drum groups, detailed descriptions given in 7.3 through 7.6 for the main drums apply equally to the auxiliary drums.

7.2 BLOCK DIAGRAM ANALYSIS

The circuits shown in figure 2–37 comprise the area which is shared by all six drums in the main drum group (par. 4.3). It follows, then, that timing pulses utilized in CD data transfer control are SEL CD timing pulses. Referring to the figure, the read-write control receives deselect, disconnect, start-read, start-write, and other pulses from the Central Computer and uses them to determine whether the selected field is to be read or written. The output of the read-write control consists of a read level or a write level, depending upon the operation to be performed. When reading is to be done, the read-write control also produces the CD-read-mode level which causes the drum read driver to produce the +100V output to enable the heads in the selected field to read.

The read or write level generated by the read-write control is applied to both address and status con-

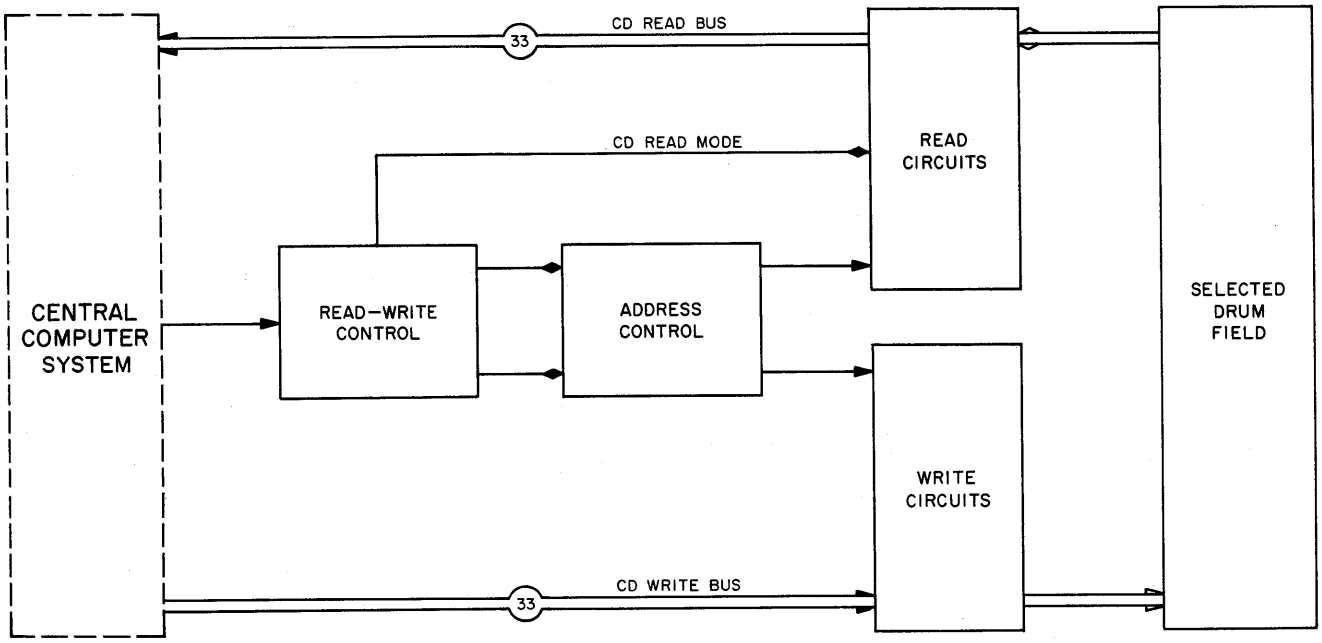


Figure 2–36. Auxiliary Drums Computer-Drum Data Transfer, Block Diagram

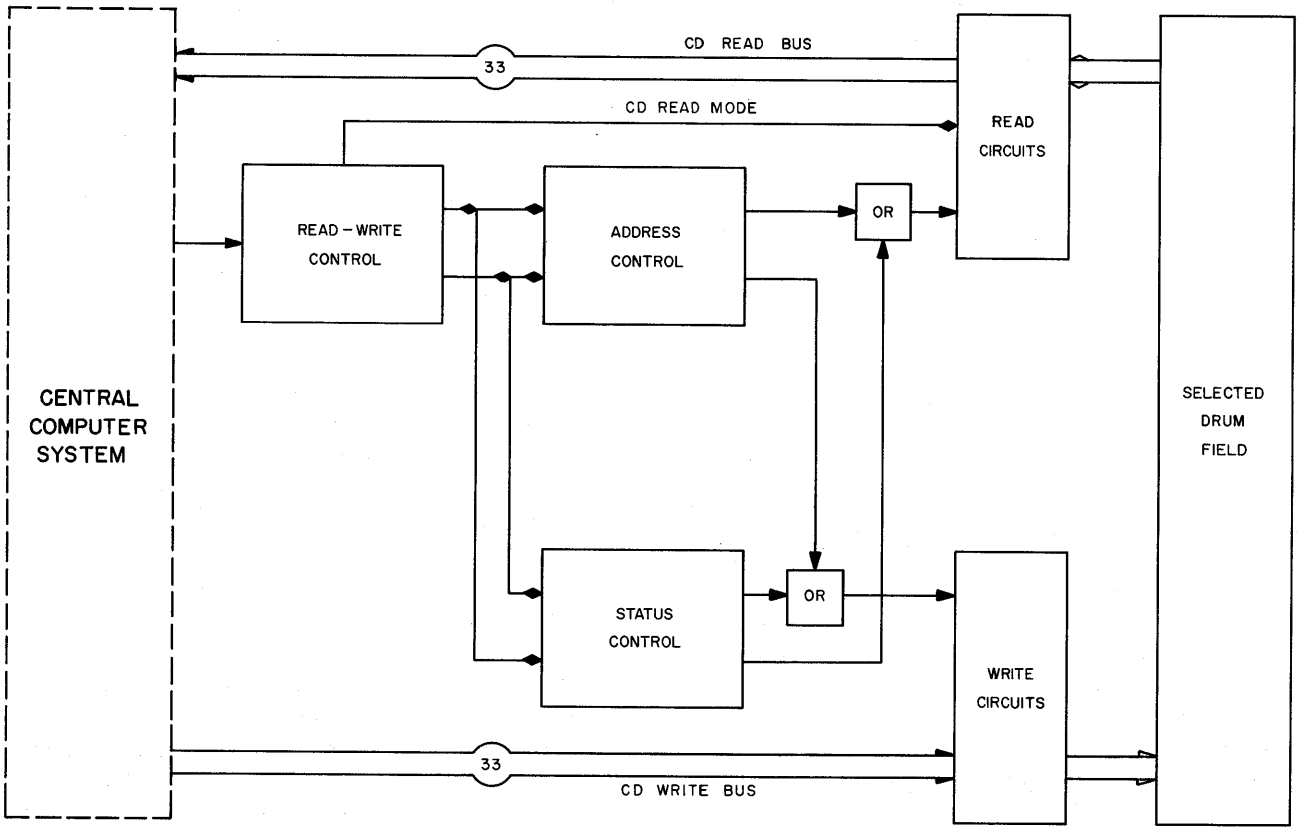


Figure 2–37. Main Drums Computer-Drum Data Transfer, Block Diagram

trol. However, only one control circuit will be activated, depending upon the nature of the selected field (address or status). Timing pulses from the AM-A, AM-B, TD, RD, or MIXD drum (whichever is selected) are supplied only to the address control circuit. Note that, with the exception of the MIXD drum, all of these drums contain only addressable fields. The MIXD drum, however, does not provide timing-to-address control if the operation involves the transfer of XTL or MI data. The LOG drum, which contains status fields only, and the MIXD drum, whenever an XTL or MI field is selected, supply timing pulses directly to the status control circuit. Since the address or the status control function is performed by timing pulses from the selected drum, address or status handling of a data transfer is dependent upon the nature of the field and the timing generated by its corresponding drum. (Refer to Ch 4 of this part for a detailed discussion of timing pulse generation and distribution.)

Under address control, data transfers from drum to computer (read operation) or from computer to drum (write operation) are controlled in the same manner. Timing pulses from the drum containing the selected field are utilized to step an angular position counter (APC). (Refer to 7.4.2.) The content of the counter is the address of the next register to come under the read-write heads. Successive APC counts are transferred to the Central Computer for comparison with the address specified for reading or writing by the program. Prior to a successful comparison, no-compare pulses are sent from the Central Computer to the drums, which then resume their compare request until the APC count equals the drum address specified by the program. Upon successful comparison, the address control circuits produce a read-compare or a write-compare level. The read-compare level conditions a gate which is sampled at CD 1 time and becomes a read-sample pulse applied to the read circuits. The write-compare level conditions another gate which is sampled at CD 3 time to produce a write pulse applied to the write circuits.

Under status control, a data transfer is dependent upon the condition of a drum register being either empty or full. A register is considered empty when it actually contains no word information or when it contains word information which has been used. A register is considered full when it contains information which has not been used. Fields that are read and written by status control are provided with two control channels called the OD status channel and the CD status channel. A 1 bit appearing in a status channel indicates that the register is full, and a 0 indicates that the register is empty. The status control circuits examine the status channels and use the status information found there to control the reading or writing operation. In this manner, word information writing is done only on empty registers and reading is done only from full registers.

Even though the principles of address control and status control are different, the completion of an operation by either method of control is based on successful comparison. In the handling of status data transfers from the drums to the Central Computer, input word data stored on the drum is read from the drum and transferred to the Central Computer upon selection of the input field by the Central Computer. Whenever the program does not call for the particular type of data transferred, the Central Computer discards the word and sends a no-compare pulse to the Drum System, causing the writing of a 1 bit on the OD status channel to indicate a full register. If comparison is successful, the Central Computer does not generate the no-compare pulse, causing the writing of a 0 on the OD status channel to indicate an empty register.

Similar methods are used in the status transfer of output data from the Central Computer to the LOG drum and thence to the Output System. For a detailed description of a typical status control circuit, refer to 7.7.

The read circuits transfer data from the drum to the Central Computer. To do reading, three conditions must be satisfied: field selection, generation of a read-sample pulse by either address or status control, and conditioning of the drum read driver by means of a CD-read-mode level from the read-write control circuits. The above conditions result in enabling the heads in the selected field to pick up the information recorded on the drum surface and releasing this information to the Central Computer through the CD read bus. Along with the word being released, the read circuits also send the Central Computer an IO-buffer-loading pulse. This pulse informs the Central Computer that a word is being transferred.

The write circuits transfer data from the Central Computer to the drum. To do writing, two conditions must be satisfied: field selection and a write pulse from either the address or status control. Upon completion of writing, the write circuits reset the drum write register and produce a word-demand pulse which is sent to the Central Computer to request another word.

7.3 READ-WRITE CONTROL

The read-write control (fig. 2–38) supplies the address and status controls with the read or write level necessary to their operation. It also generates the CD-read-mode level necessary for the operation of the read circuits. However, the read or write level can be produced only when the following conditions necessary to reading or writing have been met. First, at least 120 usec must have elapsed since any selection or other

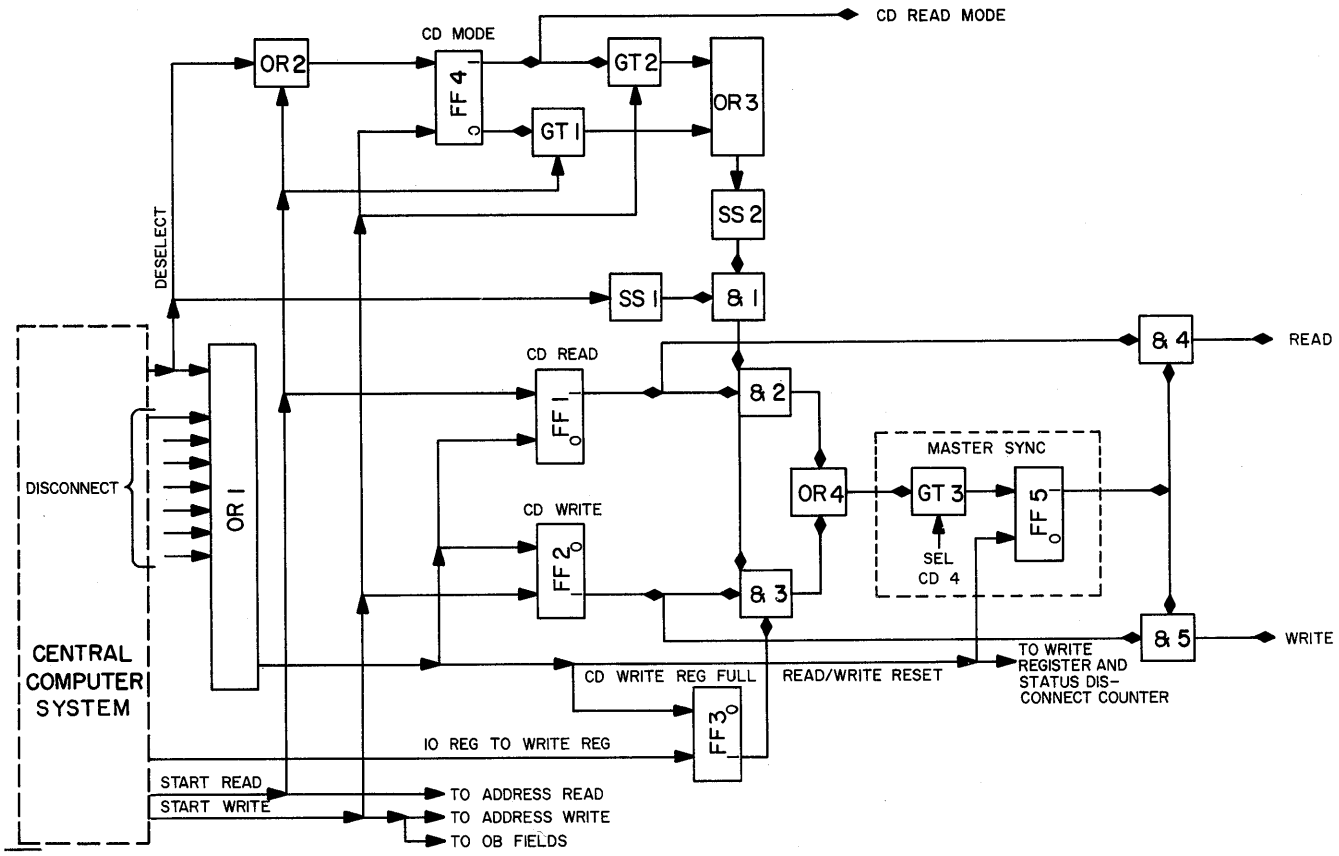


Figure 2–38. Read-Write Control Circuit, Simplified Logic Diagram

switching operation affecting the heads in the selected field has been performed; second, a start-read or start-write pulse must be received from the Central Computer; third, a field and its corresponding drum must have been selected. In addition, if writing is to be done, an IO-register-to-write-register pulse must be received from the Central Computer, indicating that the drum write register has been loaded with a word from the Central Computer.

7.3.1 Switching Delay

Switching operations affecting the selection circuits and the read switch introduce transient currents in the heads of the selected field, which interfere with the read or write operation. A delay circuit prevents the appearance of the read or write level for 120 usec after any of the switching operations.

The deselect pulse, which is part of the *Select Drums* instruction, appears immediately before any selection process. The deselect pulse triggers single-shot circuit SS 1 (fig. 2–38) which removes one of the inputs to AND 1 for 120 usec. With one of its inputs removed, AND 1 produces no output and a read or write level cannot be generated.

The status of the CD mode flip-flop, FF 4, determines the presence or absence of the CD-read-mode level which serves to activate the read switch. Whenever the status of FF 4 is changed by a start-read or start-write pulse, SS 2 is triggered through OR 3, thus removing one of the inputs to AND 1 and producing a delay of 120 usec before the read or write level can be generated. If FF 4 is cleared, a start-read pulse appears, and the flip-flop will be set and will produce the CD-read-mode level. The start-read pulse will also be passed by GT 1 and OR 3 to trigger SS 2. This action removes an input to AND 1, providing the necessary delay. A start-write pulse appearing when FF 4 is set will clear the flip-flop and will be passed by GT 2 and OR 3 to trigger SS 2.

As previously described, the action of SS 1 or SS 2 in removing one of the conditioning levels to AND 1 provides the delay necessary after any switching action to allow the heads in the selected field to operate effectively.

7.3.2 Generation of Read Level

Any reading or writing operation is initiated by a start-read or start-write pulse from the Central Com-

puter. However, before a reading or writing operation is started, FF's 1, 2, 3, and 5 will have already been cleared by either the disconnect pulse which terminated the previous read or write operation, or by the deselect pulse which is part of the *Select Drums* instruction.

The start-read pulse from the Central Computer sets CD read FF 1, the output of which supplies a conditioning level to AND's 2 and 4. AND 2 requires another conditioning level from AND 1. The AND 1 output is present at all times except when a switching delay is in progress. The output of AND 2 is applied through OR 4 to GT 3 as a conditioning level. Gate 3 passes SEL CD 4 pulses to set FF 5. The output of FF 5 supplies the second conditioning level to AND 4. AND 4, thus, has an output. This output is the read level which goes to the address and the status control circuits.

The start-read pulse also sets FF 4 which sends the CD-read-mode level to the read switch to prepare the read circuits for reading.

7.3.3 Generation of Write Level

When a writing operation is programmed, the start-write pulse sets FF 2. The output of this flip-flop supplies a conditioning level to AND's 3 and 5. When the Central Computer transfers the first word to be written to the drum write register, the IO-register-to-write-register pulse sets FF 3. The output of FF 3 supplies a second input to AND 3. The third input to AND 3 comes from AND 1 after recovery from switching delays. AND 3 thus has an output which is applied through OR 4 to GT 3. This gate passes SEL CD 4 pulses to set FF 5. The output of FF 5 supplies the second input to AND 5. The output of AND 5 is the write level which goes to both the address and status control circuits.

The start-write pulse clears FF 4 which removes the CD-read-mode level to disconnect the read amplifiers.

7.3.4 Operation Timing

The preceding discussions show that setting of master sync FF 5 must take place if a reading or writing operation is to be performed. The action of FF 5 insures that the reading or writing starts at the proper drum timing. Until GT 3 is conditioned, all actions in the read-write control are the result of pulses from the Central Computer and are independent of Drum System timing. Since each reading or writing cycle begins at CD 1 time, FF 5 is set at CD 4 time so that the read or write level can only appear immediately before the beginning of a full drum-timing cycle.

Flip-flop 5 also insures that the Drum System does not attempt to perform a reading or writing operation unless a drum field is selected. The SEL CD 4 pulse which sets FF 5 is generated only when a drum is selected. (Refer to 4.3.2 in Ch 4.)

7.3.5 Termination of Read or Write Operation

Reading or writing operations are stopped by means of a disconnect pulse. The disconnect pulse may originate at either the Central Computer System or the Drum System. When reading or writing by address, the Central Computer generates a disconnect pulse after the programmed number of words has been transferred. The Central Computer will also generate a disconnect pulse upon completion of writing of the programmed number of OB field words. When reading by status, the disconnect pulse is generated by the status disconnect counter (7.7.2) after all registers in the selected field have been examined.

The disconnect pulse clears FF's 1 and 5 to stop reading. It clears FF's 2, 3, and 5 to stop writing. With the control flip-flops cleared, the read or write levels are no longer generated and reading or writing stops.

7.4 ADDRESS CONTROL

The operation of the address control circuits (fig. 2–39) is dependent upon the selection of an addressable field, a read or write level, and a start-read or start-write pulse from the read-write control circuit. The generation of a read-sample pulse applied to the read circuits or a write-sample pulse applied to the write circuits is handled by address control in an identical manner.

7.4.1 Address Control Circuit Analysis

The start-read or the start-write pulse from the read-write control (fig. 2–39) clears compare addressable FF 1 through OR 3; this action results in a level being applied to one of the two inputs of AND 3. The read or the write level from the read-write control supplies the other level to AND 3. In this condition, AND 3 produces a start-compare level which simultaneously conditions GT's 1 through 5. One of these five gates passes SEL CD 1 pulses from whichever drum has been selected.

Note that the LOG drum does not supply pulses to these gates since it does not contain addressable fields. The MIXD drum contains two operating status fields (XTL and MI). However, selection of these fields inhibits the distribution of SEL MIXD CD 1 pulses to GT 2. (Refer to 4.3.2.) The SEL CD 1 pulse which passes through one of the five gates is used to transfer the contents of the APC corresponding to the selected drum to the Central Computer. Operation of these counters is described in 7.4.2. The same pulse which transfers the APC count is used to set compare-addressable FF 1 through OR 2. The level produced by

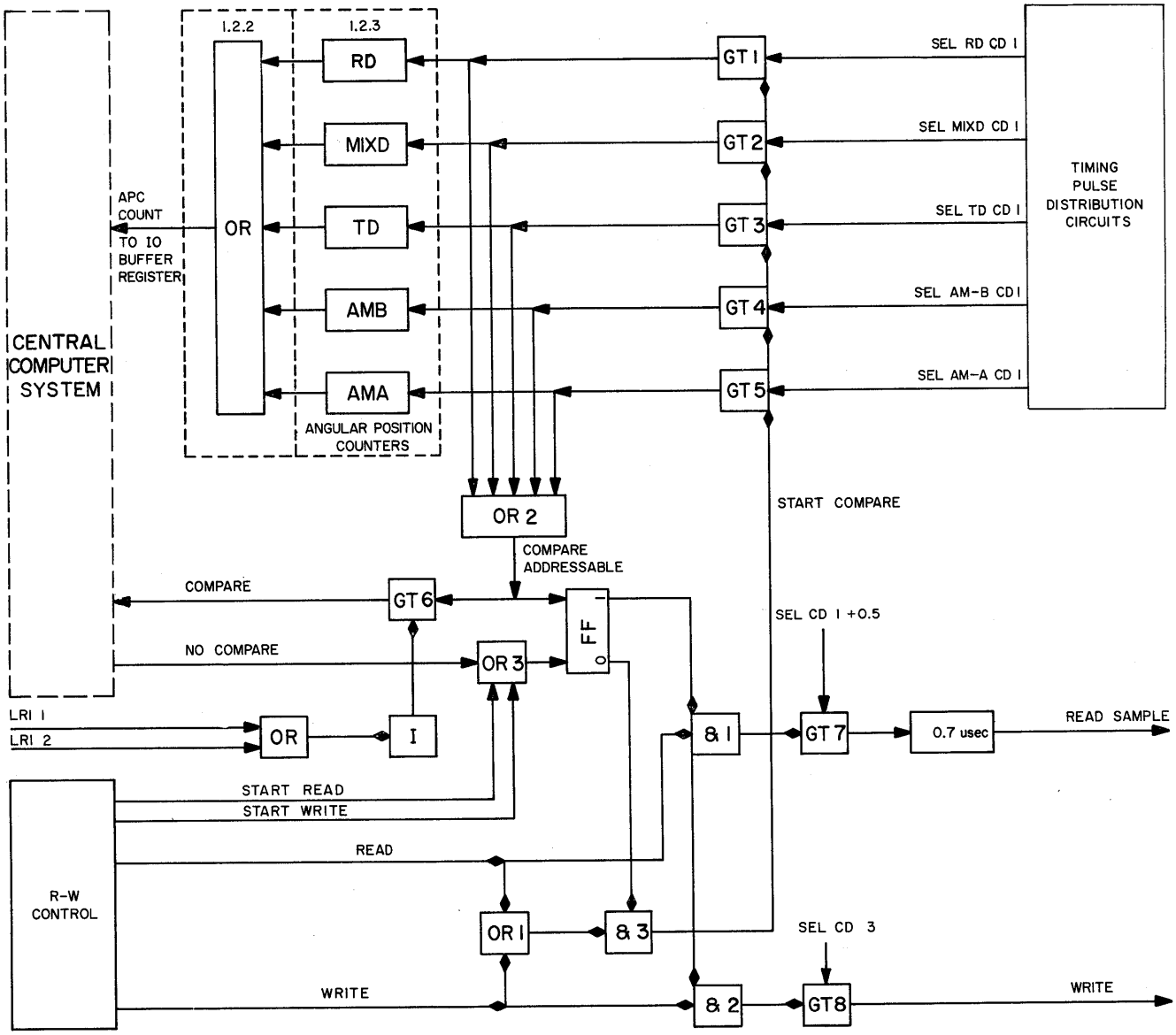


Figure 2–39. Address Control Circuit, Simplified Logic Diagram

FF 1 is applied to AND's 1 and 2. In the case of read by address, the read level from the read-write control provides AND 1 with its second input. AND 1 conditions GT 7. However, the same SEL CD 1 pulse which passes through one of the GT's 1 through 5 to set FF 1 cannot pass through GT 7. The first SEL CD 1 pulse passed through GT 7 must be in a later register of the drum.

The compare-addressable pulse from OR 2, in addition to setting FF 1, is applied to GT 6. This gate is conditioned at all times (except on every other register) during LRI data transfer. (Refer to 2.7 of Part 4.) The output of GT 6 is the compare pulse which is sent to the Central Computer along with each of the counts from the APC. For each unsuccessful comparison, the Central Computer returns a no-compare pulse in approximately 2 usec. The no-compare pulse clears compare-addressable FF 1, which results in the removal of one of the levels from AND 1, thereby removing the conditioning level from GT 7. Therefore, CD 1 pulses cannot pass GT 7 and read-sample pulses are not produced. Clearing FF 1 also results in the application of the second level to AND 3, which again produces the start-compare pulse to begin a new cycle of comparison. When the APC count compares successfully with the address in the program, the no-compare pulse is inhibited by the Central Computer. Therefore, GT 7 remains conditioned and SEL CD 1 pulses are passed

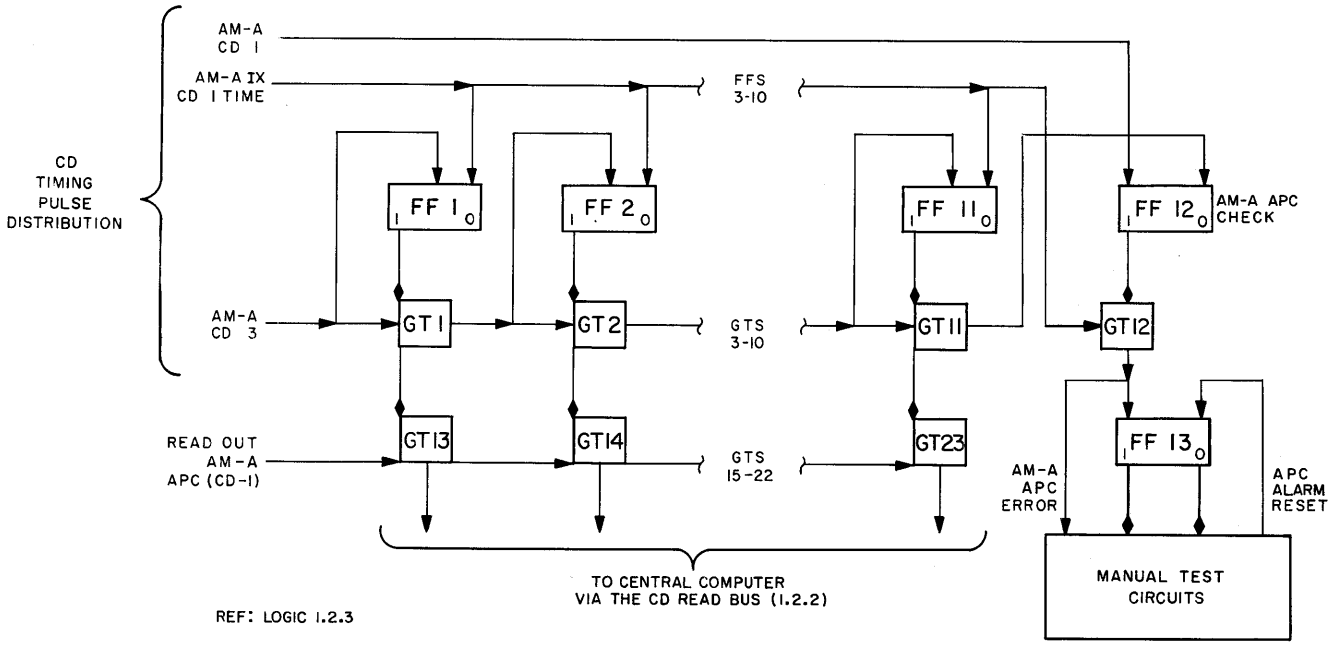


Figure 2—40. AM-A Drum Angular Position Counter, Simplified Logic Diagram

through GT 7 as CD read-sample pulses. These pulses are sent through the 0.7-usec delay to the read circuits.

In the case of write-by-address, the same process is employed except that AND 2 is conditioned by the write level and the output of FF 1 and produces the level to condition GT 8. Gate 8 passes SEL CD 3 pulses to produce write pulses.

Address-controlled reading or writing is terminated by a disconnect pulse from the Central Computer when the required number of words have been read or written. The disconnect pulse disables the read-write control which then removes the read or write level. With the read or write level absent, AND's 1 and 2 no longer condition GT 7 or 8 and no read-sample or write pulses can be produced.

7.4.2 Analysis of APC and Alarm Circuits

An APC is associated with each drum. A typical APC, the AM-A APC, is illustrated in figure 2—40. This is an 11-stage scale-of-2, 048 counter which operates in the following manner:

Assume that all of the counter flip-flops are in the 0 state. The first CD 3 pulse input complements FF 1 to the 1 state. The d-c output of the flip-flop conditions GT 1, but not in time to pass the same step pulse that complements the flip-flop. This is so because the flip-flop rise time exceeds the 0.1-usec period of the step pulse.

The second step pulse input complements FF 1 back to the 0 state. Since the decay time of the 1 side of the flip-flop also exceeds the step pulse width, the output level remains at GT 1 long enough to pass the second step pulse to FF 2.

The gated second-step pulse complements FF 2 to the 1 state. The 1 output of this flip-flop has a longer rise time than the step pulse width.

With FF 1 in the 0 state and FF 2 in the 1 state, the third step pulse complements FF 1 to the 1 side. As before, GT 1 is not conditioned in time to pass the step pulse input. At the next (fourth) step pulse, FF's 1 and 2 remain up long enough to pass the step pulse through GT's 1 and 2, to FF 3.

This operation continues, with every step pulse input complementing FF 2, every 4th pulse complementing FF 3, every 8th pulse complementing FF 4, and every 16th pulse complementing FF 5. The number of pulses counted in this manner can be determined at any time in the counting process by examining the outputs of the counter flip-flops. The FF 1 output (1 or 0 d-c level) represents the lowest order column of a binary number; the FF 2 output represents the second column of the binary number, etc. The maximum number of pulses that can be represented by the d-c output of the counter is expressed by the function 2^n-1, in which n represents the number of flip-flops in the counter.

The counter is initially cleared by an AM-A-CD-index pulse which occurs at CD 1 time of the first register on the drum (register number 0). Five usec later, an AM-A-CD 3 pulse steps the counter to 1. At

the CD 3 pulse of every register on the drum, the counter is stepped again. Since the first register on the drum is numbered 0, the counter setting (as represented by the states of its flip-flops) at any given time is one number higher than the number of the register under the read-write heads at that time.

Whenever one of the counter flip-flops from 1 to 11 is set, that flip-flop's output conditions the associated gate from among GT's 13 through 23. When the readout-AM-A-APC pulse is received, it pulses GT's 13 through 23. The gates that have 1-state levels pass the readout pulse to the CD-read bus. Information received by the CD read bus is transferred directly to the Central Computer System.

Reviewing the operation of the AM-A-CD-APC, note that the counter setting at any given time is a binary number which is greater by one than the actual number of the last register counted. However, the setting is transferred during the next register (at CD 1 time, before the counter is stepped again) so that the count transferred represents the actual address of the drum register which is available for reading or writing when the next read- or write-sample pulse occurs.

When the AM-A-CD APC has been stepped to 2,047, all the flip-flops are in the 1 state. The next CD 3 timing pulse (occurring during the last drum register) is passed through GT's 1 through 12, producing an end-carry pulse which clears FF 12, the APC check flip-flop.

Flip-flop 12 is normally set. It is cleared only by the APC end-carry pulse and then set again by the next CD 1 pulse. Normally, the index pulse occurs while FF 12 is cleared. At this time GT 12 is not conditioned and the index pulse is not passed. If there has been an error in counting, the end-carry pulse does not appear to clear FF 12 just before the index pulse appears. The index pulse, in this case, is passed by GT 12, producing an AM-A-APC-error pulse which is sent to the manual drum tester element, where the AM-A-APC-error pulse sets a flip-flop which produces an error indication at the maintenance console. Also, FF 13 is set by the gated-index pulse. The 1-state output of FF 13, goes to an error indicator on the drum unit test panel. Flip-flop 13 must be manually cleared after an error is indicated.

7.5 READ CIRCUIT ANALYSIS

The read circuits read words from the selected drum field and transmits them to the Central Computer. For a reading operation to take place, the read switch must be activated by the CD-read-mode level from the read-write control circuit (par. 7.3.2). When the read switch is activated, each read-sample pulse transmits a word to the Central Computer.

The read switch (fig. 2–41) consists of a pair of diodes connected in each line carrying signals from a read-write head to a drum read amplifier (DRA) from the read-write heads when a writing operation is in progress (par. 6.1). When reading is to be done, the diodes are used to connect the DRA's to the read-write heads. This is necessary because the same heads are used for both reading and writing.

Whenever a drum field is selected for either reading or writing, the +125V dc-select-field level from the drum field driver (DFD) is applied to the anodes of the read-switch diodes (par. 6.3). Except when a reading operation is to be performed, the CD-read-mode level is not present and the output of the drum read driver (DRD) is a +150Vdc level. This level is applied through the input transformers of the DRA's (only one transformer is shown on fig. 2–41) to the cathodes of the read-switch diodes. With the cathodes at a higher d-c voltage than the anodes, the diodes cannot conduct and no signals from the write circuits can reach the DRA's.

When a reading operation is to be performed, the read-write control circuit sends the CD-read-mode level to the DRD. Under this condition, the output of the DRD's is a +100Vdc level. This level applied to the cathodes of the read-switch diodes places the cathodes at a lower d-c voltage than the anodes and the diodes can conduct. This condition connects the DRA's to the read-write heads and reading can be done.

The information under each of the 33 read heads (a 1 bit or a 0 bit) is transferred through the read switch to the corresponding DRA. For each 1 bit read by the heads, the corresponding gates (1 through 33) will receive a conditioning level coincident with the read-sample pulse; the conditioning from 0 bits is not coincident with the read-sample pulse. Therefore, gates that produce an output represent 1 bits and gates with no output represent 0 bits.

Figure 2–41 shows that the gates connected to each of the 33 DRA's are divided into two groups: the first group consists of gates which provide their output to bits LS through L10 and L14 through R10; the gates of the second group provide their output to parity, L11, L12, L13, R11, R12, R13, R14, and R15 bits. The bits in the second gate group correspond to the unused bits in radar data words. This logic arrangement serves to ensure that when the RD fields are read during testing, false information is not produced by the unused gates and DRA. During marginal checking operations, the DRA's without an input will normally provide an output of 0 to 5V which is sufficient to condition the gates. This results in false information being transmitted to the Central Computer through the CD read bus.

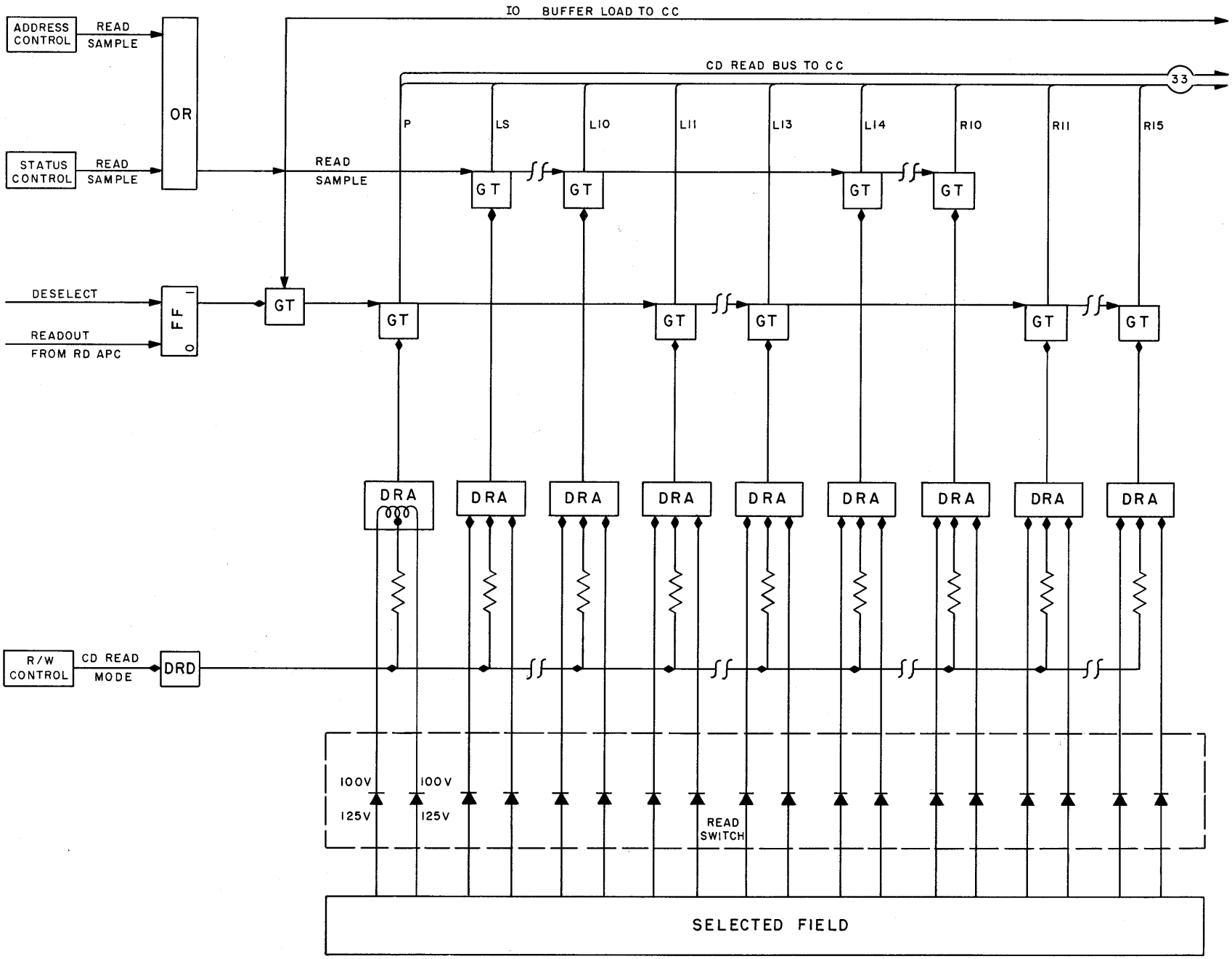


Figure 2–41. CD Read Circuit, Simplified Logic Diagram

When reading is done from any field, except RD fields, the deselect pulse sets the flip-flop to condition the control gate to pass read-sample pulses. In this condition, all 33 read gates will receive read-sample pulses and provide a correction word pattern through the CD read bus.

During reading of RD fields, the readout-RD-APC pulse will clear the flip-flop to remove the conditioning level to the control gate. In this condition, the read gates in the second group previously mentioned will not receive read-sample pulses and accordingly will not produce an output.

The read-sample pulse, which, in effect, releases the information word to the Central Computer, also becomes an IO-buffer-loading pulse which indicates to the Central Computer circuits that a word is being transferred.

7.6 WRITE CIRCUIT ANALYSIS

The write circuit operates upon receipt of a write pulse from either address or status control circuits (fig. 2–42). The write pulse received is applied to OR 1 and OR 2. From OR 1, the pulse causes the writing on the drum surface of the word stored by the Central Computer in the drum write register (DWR). From OR 2, the pulse is delayed to reset the flip-flops in the write register; it also forms the word-demand pulse to the Central Computer, after the word has been written on the drum.

The pulse stretcher connected to the output of OR 1 widens the write pulse sufficiently to cause a magnetized spot on the drum surface. The DWD produces an output which causes the drum writers to write when its input drops from +10V to −30V. The write pulse clearing the flip-flop applies the −30V level to the DWD. The same write pulse passes through the delay circuit and sets the flip-flop 1.7 usec later, removing the −30V input to the DWD. Thus, for 1.7 usec the output of the DWD conditions the 33 drum writers to transfer the contents of the DWR onto the drum surface.

The write pulse at the output of OR 2 is connected to another delay circuit which, after 2.4 usec, produces a pulse applied to OR 3. This 2.4-usec delay compared to the 1.7-usec delay at the pulse stretcher results in a time gap of 0.7 usec, which ensures the writing process to be fully accomplished before resetting the DWR and sending a word demand to the Central Computer. The write register reset originated by the write pulse and the read-write reset pulse originated at the read-write control are applied to the DWR through OR 3.

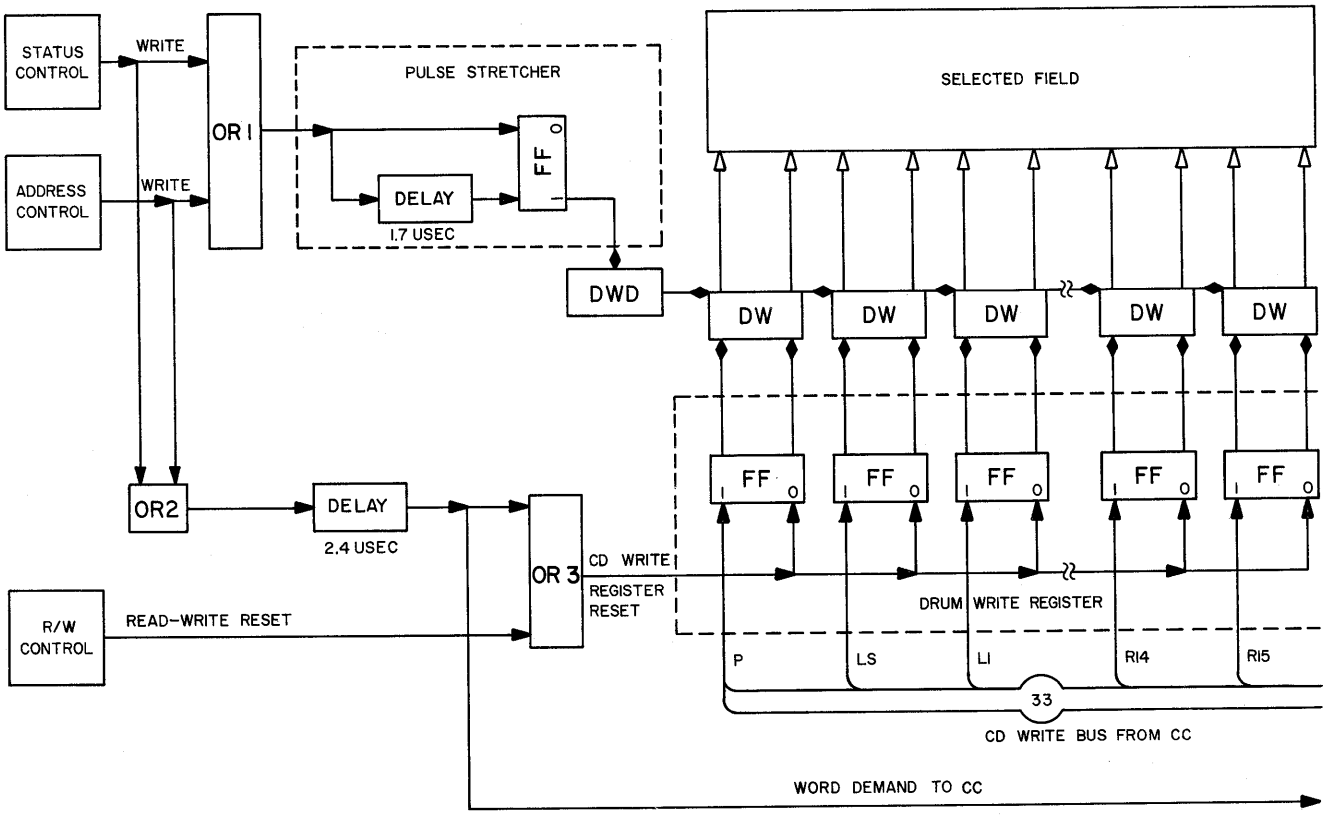


Figure 2–42. CD Write Circuit, Simplified Logic Diagram

7.7 STATUS CONTROL

The operation of the status-control circuits extends itself over the OD and CD sides of the drum in a chain reaction process. Therefore, to understand CD operation it is necessary to include OD operation as well. This is particularly true considering that there are status-controlled fields which carry incoming data (MI, XTL, LRI, and GFI fields) as well as status controlled fields which carry outgoing data (the three OB fields). The status control for all status fields is essentially identical and opposite in signal flow. The signal flow accommodates itself to the incoming or outgoing field.

Taking an incoming data field as a typical case, the chain-reaction process may be arbitrarily chosen to start at the OD status channel read head. When this head reads a 1, indicating a full register, no further action takes place. However, when the head reads a 0, indicating an empty register, a drum-demand pulse is generated by the OD status control and is applied to the Input System. The drum-demand pulse causes readout from the channel of the corresponding Input System element. Readout, in turn, causes a data-available pulse generated at the Input System and applied to the OD status control. The data-available pulse accompanies the transfer of the readout data to the status field and causes a 1 to be written on the CD status channel. Up to this point, the operations have been performed on the OD side of the drum; the rest of the operations in the chain-reaction process affect the CD side, as follows.

Assuming that a 1 was written on the CD status channel and that transfer of incoming data was made to the drum, the CD status channel head reads a 1 which results in a compare pulse being sent to the Central Computer System and a read-sample pulse which causes transfer of the incoming data to the Central Computer. Whenever the transferred data does not conform with the requirements of the program, the data is discarded by the Central Computer and a no-compare pulse is produced. The no-compare pulse causes the writing of a 1 on the OD status channel, indicating that the register involved is full. Whenever the data transferred agrees with the requirements of the program, the Central Computer utilizes the word and the no-compare pulse is inhibited. The absence of a no-compare pulse causes a 0 to be written on the OD status channel, which is interpreted by the OD status control as an empty register and the entire operation begins as previously indicated.

7.7.1 Typical Status Control Circuit

The diagram of figure 2–43 shows the logic circuits involved in the control of a typical incoming data transfer from the Input System to the Central Computer System. To establish a parallel with the overall description of the status control previously given, the following discussions will take as a point of departure the OD status channel read head as shown on the figure.

7.7.1.1 OD Status Control, Circuit Analysis

When a 1 is read by the OD status channel read head, the DRA connected to it produces an output pulse which conditions GT 1 to pass the next OD 1 pulse. The output of GT 1, in turn, sets FF 1, thereby removing the conditioning level from GT 2; OD 3 pulses are thus blocked at GT 2. This results in no sensing of GT 3 and, consequently, no drum-demand pulse applied to the Input System. Summarizing, the presence of a 1 on the OD status channel, which signifies a full register, prevents a drum-demand pulse from being produced.

When a 1 is read by the OD status channel read head, the output from the DRA does not condition GT 1 in time to pass the next OD 1 pulse, and FF 1 remains cleared as previously done by the OD 4 pulse. In this condition, FF 1 conditions GT 2 to pass the next OD 3 pulse. The output from GT 2 becomes a gated OD 3 pulse which is also passed by GT 3, provided that the system is in the operate mode. It is apparent that in the test mode of the system no drum-demand pulses can be produced from any of the OD status control circuits.

Six usec after sending a drum-demand pulse to the Input System, a data-available pulse appears in the OD status control circuit (provided that there is data ready for transfer in the Input System). Since the drum-demand pulse is produced at OD 3 time, the data-available pulse coincides with the OD 1 + 1 usec time of the next drum register (actually 11 usec after reading the OD status channel). The data-available pulse indirectly sets FF 4 through OR 1, and directly sets FF 5. When FF 4 is set, the DW circuit connected to this flip-flop causes the CD status head to write a 1 (meaning full register) on the CD status channel. Setting of FF 5 conditions GT 6 to pass the next OD 3 pulse. The pulse at the output of GT 6 is the write pulse applied to the pulse stretcher. The write pulse clears FF 6 which, in turn, causes a negative input to be applied to the DWD circuit. Since DWD's produce an output only when a negative input is present (refer to special circuits manual, 3-3-0), the 33 drum writer (DW) circuits will be conditioned by the output of the DWD to cause the input word to be written on the drum surface. Conditioning of the 33 DW's lasts for 1.7 usec. At the end of this period, the write pulse going through the 1.7-usec delay clears FF 6 and removes the negative input to the DWD.

Before concluding the OD status control description, three allied functions require clarification. One is the 15-usec period transferred from OD status channel reading to CD status channel writing, next is the pur-

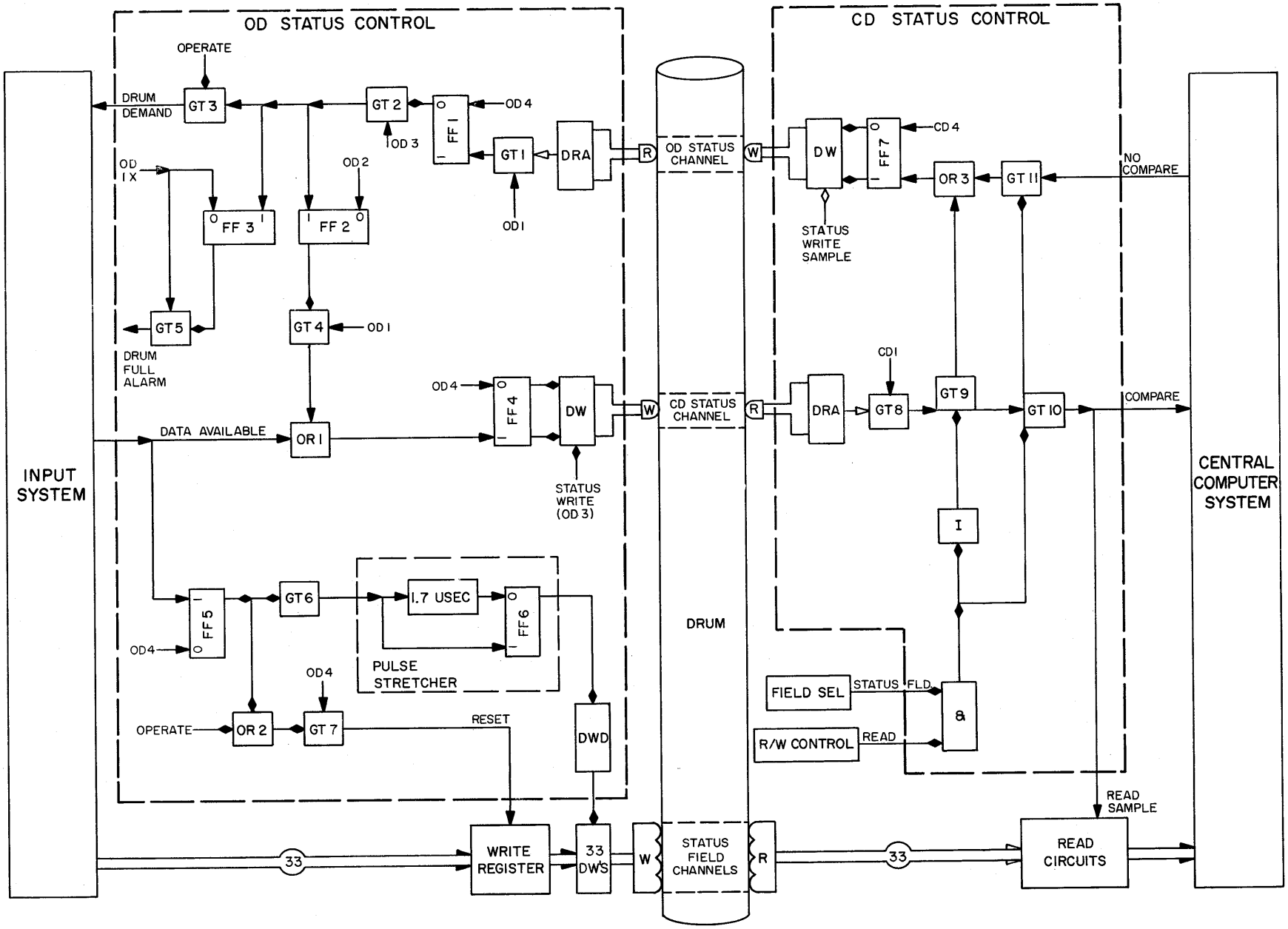


Figure 2–43. Typical Status Control Circuit, Simplified Logic Diagram

pose and performance of FF 2 and GT 4, and last is the operation of drum full alarms by FF 3 and GT 5, shown on figure 2–43. With regard to the first allied function, it was previously mentioned that the data-available pulse (OD 1 + 1), which precedes transfer of data from the Input System, is received 11 usec after reading the OD status channel. However, the actual OD writing of data takes place at OD 3 time, the time employed by these operations totals 15 usec. To allow for the time required for this process, all OD status channel read heads are manually preset to read 15 usec before the actual drum register passes under the information heads. Another aspect of the 15-usec period is related to the fact that successive periods overlap each other to allow data transfers to take place at the normal rate of one transfer every 10 usec. For a practical example assume that the OD status channel read head senses two 0 bits in succession, meaning two adjacent empty registers. While the drum-demand pulse resulting from the first 0 bit is going through the Input System, the second 0 bit is being sensed by the read head. In spite of the fact that the second 15-usec period starts before the first is concluded, there is no interaction between these successive periods.

Flip-flop 2 and GT 4 serve to insure that when a 1 is read from the OD status channel, a 1 also appears on the same register of the CD status channel. In this manner, a full register can be read by CD status control at each drum revolution until the respective word is accepted by the Central Computer. Notice that FF 2 is always cleared at OD 2 time and is set at the next OD 3 time only when drum-demand pulses are generated. Therefore, when a drum demand is not generated, meaning a full register, the preceding OD 2 pulse connected to FF 2 serves to condition GT 4. Such conditioning remains until the next OD 1 pulse senses GT 4. Thus, the pulse is passed by the gate and is applied to OR 1, causing the same effect as a data-available pulse; i.e., a 1 is written on the CD status channel. Without the operation of FF 2 and GT 4, OD 4 pulses applied to FF 4 would cause the writing of 0's on the CD status channel whenever data-available pulses are absent.

A drum-full alarm is generated whenever no drum-demand pulses are produced from a specific status field during a complete drum revolution. This condition indicates that all 2,048 registers in that particular field are full (fig. 2–43). The generation of a drum-full alarm is accomplished by FF 3 and GT 5 in the following manner. The space between two consecutive index pulses denotes one complete drum revolution. Therefore, each index pulse has been connected to clear FF 3 and sense GT 5 simultaneously. Assuming that FF 3 was set by a drum-demand pulse, the next index pulse will clear the flip-flop and sense the gate. As a result, the gate is conditioned, not in time, however, to pass the same index pulse. If a second index pulse appears before a drum demand is generated, GT 5 will be conditioned to pass this pulse and to produce a drum-full alarm. It follows that the appearance of one or more drum-demand pulse between two consecutive index pulses will prevent the generation of a drum-full-alarm pulse.

7.7.1.2 CD Status Control, Circuit Analysis

The CD status channel read head senses every passing register in the rotating drum. The DRA receives the signal from the read head and produces a conditioning pulse for GT 8. When the signal received is a 1 bit, GT 8 is conditioned in time to pass a CD 1 pulse. Zero bits condition the gate too late for CD 1 pulses. The output of GT 8 may take one of two different paths (through GT 9 or GT 10), depending upon the state of the AND circuit. When a field select level and/or a read level is absent, the output of the AND circuit is a negative level. This negative level applied to the inverter (I) circuit results in conditioning of GT 9. Therefore, GT 9 passes the pulse from GT 8 to OR 3. From OR 3 the pulse sets FF 7, which causes (through the DW) writing of a 1 bit on the OD status channel. This action prevents the generation of a drum-demand pulse by the OD status control.

The alternate path for the output of GT 8 is open when both the field select and read levels are present at the AND circuit. In this case, the output of the I circuit becomes negative, while GT 10 and GT 11 are conditioned by the AND circuit output. When GT 10 is so conditioned, the pulses at the output of GT 8 become the compare pulses that are sent to the Central Computer and the read-sample pulses that are sent to the read circuit (par. 7.6).

Summarizing CD status control to this point, in the absence of the respective status field selection and the read operation, each 1 bit appearing on the CD status channel causes a 1 bit also to appear on the OD status channel with the corresponding register. This action takes place through GT 8, GT 9, OR 3 and FF 7. When the respective status field has been selected and the read operation has been instituted, GT 10 is conditioned to generate compare and read-sample pulses, and GT 11 is open to pass the no-compare pulses from the Central Computer.

The compare pulse effectively requests the Central Computer to ascertain whether the data being transferred fulfills program requirements at that time. If not, the Central Computer sends the no-compare pulse applied to GT 11. Since this gate is open, as previously indicated, the pulse proceeds to OR 3 and causes a 1 to be written on the OD status channel. This action allows the data on that particular register to be trans-

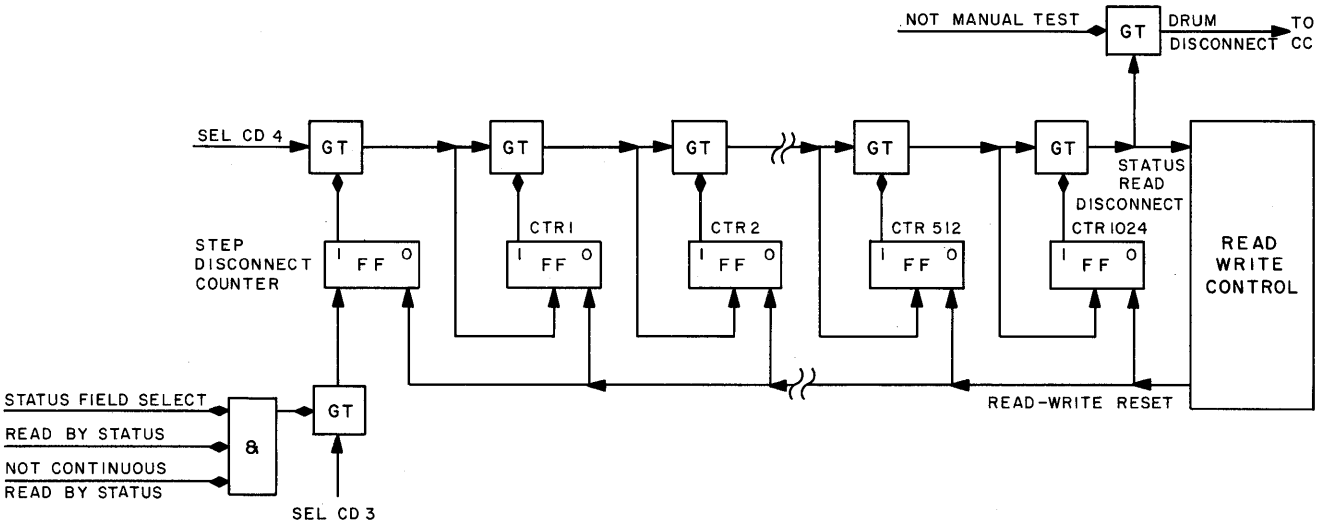


Figure 2–44. Status Disconnect Counter, Simplified Logic Diagram

ferred again and again, at every drum revolution, until it eventually compares favorably with program requirements. When a favorable comparison takes place, the no-compare pulse is inhibited from GT 11. In this condition, FF 7 remains cleared, as established by the preceding OD 4 pulse, and a 0 is written on the OD status channel. It is apparent that the absence of the no-compare pulse indicates that the word data in that particular register was utilized by the Central Computer. Therefore, the writing of a 0 implies that the register is available, or "empty", to accept another word to be transferred from the Input System.

7.7.2 Status Disconnect Counter, Circuit Analysis

The CD status disconnect counter allows CD reading to commence at CD 4 time of a specific drum register in the selected field, and produces a status-read-disconnect pulse, at CD 4 time, 2,048 registers later. In this manner, the read operation initiated by the Central Computer for any status field can only last for one complete drum revolution.

Figure 2–44 shows the logic operation of the counter. A fundamental requirement is the presence of three levels at the AND circuit: the status-field-select level from the selection logic, the read-by-status level from the read-write control circuit, and the not-continuous-read-by-status level from the test circuits. When these three levels appear in coincidence, the adjacent gate circuit passes the next SEL CD 3 pulse, which sets the step disconnect flip-flop. At SEL CD 4 time of the same register, the count begins.

The counter itself is a scale of 2,048, 11-stage, binary counter. The figure shows the first two and last two stages, and their respective counts. The seven stages not shown cover the following counts: 4, 8, 16, 32, 64, 128, and 256. The last two stages cover the 512 and 1,024 counts. This means that at the rate of count, the gate in the last stage will produce a pulse at the 2,048 count. Referring to figure 2–38, the status-read-disconnect pulse at the output of the counter is applied to one of the inputs to OR 1 in that figure. The output of OR 1 becomes a read-write reset pulse which is returned to the status disconnect counter to clear its entire circuit.

PART 3
ADDRESSABLE FIELDS

CHAPTER 1
INTRODUCTION

The Drum System contains 67 addressable fields, so designated because their circuit control performs data transfers, to and from the Central Computer, by the address method. Fifty of these fields serve as an expansion to the normal storage capacity provided by the Central Computer core memory. These are called auxiliary memory fields and are distributed in the following manner:

a. Main Drums

MIXD Drum	1 SP AM field
	1 SP XTL field
AM-A drum	6 fields
AM-B drum	6 fields

b. Auxiliary Drums

AM-C through AM-H drums	36 fields

Chapter 2 contains detailed descriptions of the auxiliary memory fields.

The other 17 addressable fields are the nine fields in the RD drum, the six fields in the TD drum, and the DD and the IC fields in the MIXD drum. In these 17 fields, as in any other addressable fields, information can be written and read by the Central Computer to satisfy program requirements. However, the primary purpose of the RD, TD, and DD fields is to carry on to the Display System the information stored by the Central Computer. A detailed analysis of these fields is given in Chapter 3.

The IC field is unique in that the information stored in this field is normally read and transferred to the alternate area under control of the alternate Drum System. IC field operation is described in Chapter 4.

CHAPTER 2
AUXILIARY MEMORY DRUM FIELDS

The 14 auxiliary memory drum fields contained in the main drums are used by the Central Computer primarily to store master program information. In the case of the active program (CDA or CCA), the space of 19 drum fields is required. However, up to 14 fields storage capacity is provided by the main drums while the rest of the master program is stored in core memory.

The process of data transfers to and from the Central Computer takes place in each of these fields as indicated in 7.4 of Part 2. The SP XTL field, basically a status field, is caused to operate as an addressable field when a select-drum level is produced upon receipt of field selection SEL SP XTL 20 (5.3.3 of Part 2).

The 36 auxiliary memory fields contained in the AM-C through AM-H drums are used by the Central Computer to store tabular information such as weather constants and mathematical ratios or statistical information such as flight histories. Data transfers in and out of these fields also take place in the manner described in 7.4 of Part 2. However, to preserve the accuracy of data stored therein, an illegal address decoder and write interlock circuits have been provided in unit 20. These circuits are described in 2.1 and 2.2.

2.1 ACD ILLEGAL FIELD SELECTIONS

The auxiliary drums CD field designations are listed in table 2–2. The associated field selection decoder (logic 1-2.1.1), however, is capable of producing units and tens outputs other than those designations listed in the table, thereby resulting in the selection of illegal auxiliary fields. For example, octal designations 01 and 67 would be illegal because no such fields exist.

A tens and units output (fig. 3–1) designating an illegal field is passed to the illegal field selection decoder. That decoder's output is applied to an OR circuit whose output, in turn, prevents the generation of compare pulses to the Central Computer (2.2.1). The operation of this decoder is identical with that of the field selection decoder discussed in 5.3.1 of Part 2.

2.2 ACD WRITE INTERLOCK

To preserve the data written on the auxiliary drums as an accurate source of reference, elaborate precautions have been taken so that writing operations are performed only when strictly required. New writing on the auxiliary drums then becomes an accurate source of reference which supersedes obsolete information previously stored.

In the operate mode, preparation for writing involves two distinct steps: first, turning on key-operated write interlock switch S15 on the lower section of module E of the duplex maintenance console; second, momentarily turning off the DC POWER switch at the power control door in unit 20. There is also a key-operated write interlock switch, S1, in the test door of unit 20. In the operate mode, however, this switch is disabled.

Upon completion of the writing operation, key-operated write interlock switch S15 at the duplex maintenance console is turned off, and the DC POWER

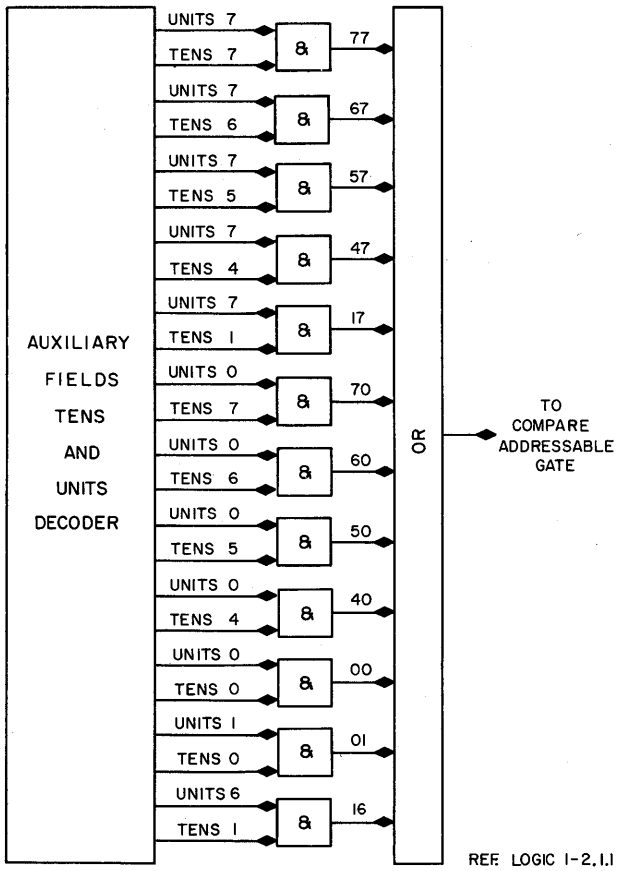


Figure 3–1. Auxiliary Drums Illegal Field Selection Decoder

switch is again turned off momentarily. From this time, no further writing can be performed until the two steps described have been taken.

In the test mode, the preparation for writing involved four distinct steps: first, turning on key-operated write interlock switch S15 at the duplex maintenance console; second, placing the OPERATE-MANUAL TEST switch (S14), also at the maintenance console, in the MANUAL TEST position; third, turning on key-operated write interlock switch S1 at the test door; and fourth, momentarily turning off the DC POWER switch at the power control door in unit 20. Upon completion of the writing operation, write interlock switches S15 and S1 are turned off, and the DC POWER switch is momentarily turned off. No further writing can be performed unless the preparatory steps described have been taken in accordance with the operate or the test mode in progress.

2.2.1 Circuit Analysis

Figure 3–2 shows the compare-addressable flip-flop in the address-control circuits. This flip-flop is set by a compare-addressable pulse, which is passed by a gate. The setting of the flip-flop, therefore, will depend upon the gate's being conditioned to pass the compare-addressable pulses.

With the write interlock active, the +10V level from the CD write flip-flop in the read-write control goes through the normally closed contacts (3) of relay K8 to the OR circuit (logic 1-2.1.1). The +10V level at the output of the OR circuit is applied to the inverter, which produces a negative output, deconditioning the gate. Thus, when the write interlock is active, the gate does not pass compare-addressable pulses to set the compare-addressable flip-flop.

When the write interlock is removed, K8 is energized. In this condition, contacts (3) of this relay apply −30V to the OR circuit, whose negative output is applied, in turn, to the inverter. The inverter output thus becomes positive and serves to condition the gate to pass compare-addressable pulses.

Another set of contacts (not shown in fig. 3–2) on K8 applies power to the write interlock relays. When the interlock is active, these contacts are open, and the write interlock relays are energized and disconnect the drum writers from the write heads of the selected field, thereby making writing impossible.

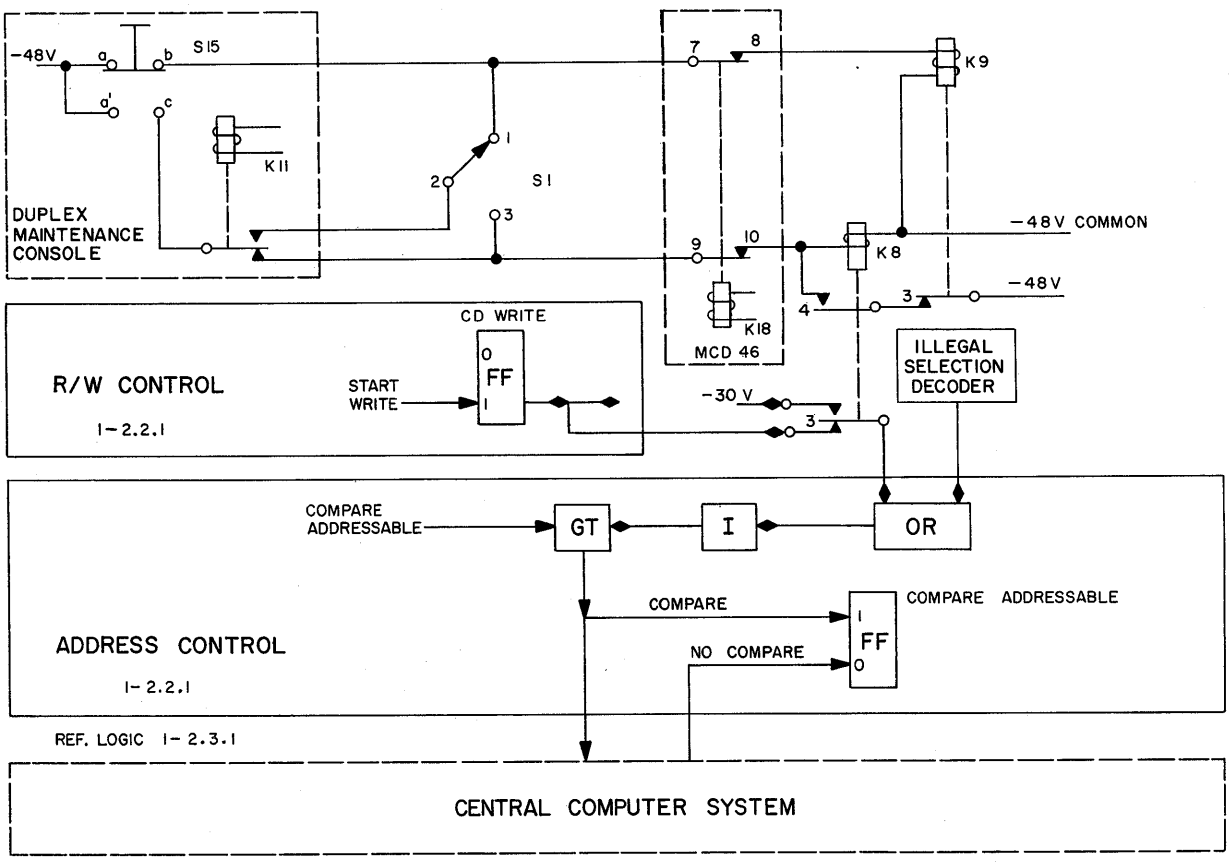


Figure 3–2. Auxiliary Memory Fields Write Interlock Circuit

The other inputs to the OR circuit are select levels representing illegal fields. The selection of illegal fields blocks the compare-addressable pulse and prevents either reading or writing. (Refer to 2.1 for a discussion of illegal field selections.)

2.2.2 Operation Analysis

See figure 3–2. Key-operated switches S1 and S15 appear in the figure in the off position (key removed), and relays are shown in the de-energized state. To perform writing in the auxiliary drums, the main objective is the energizing of K8.

In the operate mode, when write interlock switch S15 is turned on, —48V control power is applied to K8 through the contacts of de-energized relays K11 and K18. Since K11 is de-energized during the operate mode, and K18 is energized when power is applied, it follows that d-c power must be removed (at the DC POWER switch in the power control door of unit 20) so that K18 is de-energized and, through its normally closed contacts, completes the —48V line to K8.

When d-c power is reapplied and K8 is energized, K8 is held energized through the contacts of K9. Relay K9 is energized only when interlock switch S15 is turned off and d-c power is removed. In this condition, contacts (3) of this relay open and —48V power is disconnected from the holding contacts (4) of K8. At all other times, K9 is de-energized. To energize K8, therefore, S15 is operated and d-c power removed. When d-c power is restored (upon momentary switching), K8 is held energized through its own contacts and those of de-energized K9. This condition will prevail for the duration of the writing operation, at the end of which S15 is turned off and the DC POWER switch is momentarily operated off and on.

In the test mode, to prepare for writing on the auxiliary drums, both write interlock switches, S15 at the maintenance console and S1 at the test door, must be operated, and the DC POWER switch at the power control door must be momentarily operated off and on. During the test mode, K11 at the maintenance console is energized as a result of setting the OPERATE-MANUAL TEST switch (S14) in the MANUAL TEST position. Through the transfer contacts of K11, the —48V control power from S15 appears at the center arm of S1. When interlock switch S1 is off, the —48V energizes K9 through the contacts of K18 (when d-c power is removed). However, if write interlock switch S1 is operated, K8 will be energized when d-c power is removed and will remain energized through its own contacts and those of K9 when d-c power is again applied.

At the end of each write operation, interlock switches S15 and S1 should be turned off, and the d-c power should be momentarily switched off to restore the normal write interlock conditions.

CHAPTER 3
DISPLAY FIELDS

The Drum System display fields are a data storage link between the Central Computer System and the Display System. Display data from the Central Computer System is sent to the display fields for storage. The stored data is then transferred from the Drum System to the Display System.

Display data from the Central Computer System is sent to the Drum System at rates too rapid for use by the Display System. Consequently, the rate of data transfer to the Display System is reduced by interleaving the data written on the drum and employing a precessed reading pattern.

Display data is interleaved at the Central Computer System before it is written on the CD side of the drums. During OD reading, the interleaved message on the drums is transferred in the proper sequence by having the read circuits alternately skip and read in a pattern that corresponds to the programmed interleaving of the message. The skip-and-read pattern develops the necessary time delay between successive word transfers, resulting in a rate of data transfer compatible with Display System requirements.

Display data transfers are performed either automatically and continuously or at a programmed computer command, depending on the type of data being transferred. Two types of data are sent to the Display System: digital display (DD) and situation display (SD) data. Digital display data is sent to the DD element of the Display System in a programmed operation. Situation display data is subdivided into track display (TD) data and radar data (RD). Track display and radar data are fed in continuous alternation to the situation display generator element (SDGE) of the Display System.

The circuits that transfer the DD and the SD data from the Central Computer System to the Display System are shown in figure 3–3. The heavy lines in the figure indicate data flow; the lighter lines, control signal paths.

The CD-writing of display data is accomplished by address control (Ch 7 of Part 2); OD-reading is accomplished by the circuits on the OD side of the drums.

Digital display information is stored on one field of the MIXD drum. The DD read circuit reads the information on the drum field under the control of the DD-read-control circuit. The DD-read-control circuit employs a reading pattern that introduces a time delay between successive DD word transfers. The reading pattern is generated by the timing circuit of the MIXD drum and involves skipping a fixed number of drum registers between readings of the individual words of a DD message. During the last register of each drum revolution, the reading pattern is precessed so that the next word is read one register earlier during the following revolution. This procession of the pattern ensures that no DD field registers are unread and that none are read more than once during a fixed number of drum revolutions. As the registers are read by the DD read circuit, the data is sent to the digital display generator element (DDGE).

Situation display information is stored on 15 fields: nine fields on one drum (RD) store RD information; six fields on a second drum (TD) store TD information. The two drums are read alternately, sending a continuous stream of display information in the SDGE.

As the TD drum is read, the contents of its fields are sent to the TD-field switch. The TD-read-control circuit selects one field at a time to be read into the SD drum switch. The selection is made in a numerical sequence that begins with field 1.

When the reading of six TD fields is completed, eight of the nine radar fields are read. (The ninth field is written on the CD side at the same time that the eight fields are read by the OD side.) The fields are read through the RD-field switch under the control of the RD-read-control circuit, one field being read at a time. The field selection for RD as for TD data is consecutive but begins with a field selected by the Central Computer System. The selected field contents are sent to the SD drum switch. The RD field read first contains the oldest Central Computer System information. The RD field read last contains the most recent Central Computer System information. The RD field that is not read during the cycle is being written on by the Central Computer System.

The SD drum switch transfers the data from the selected field of the drum being read to the SD read circuit. During TD reading, the SD read circuit is controlled by the TD-read-control circuit. This circuit employs a reading pattern that introduces a time delay between message transfers. The reading pattern is timed

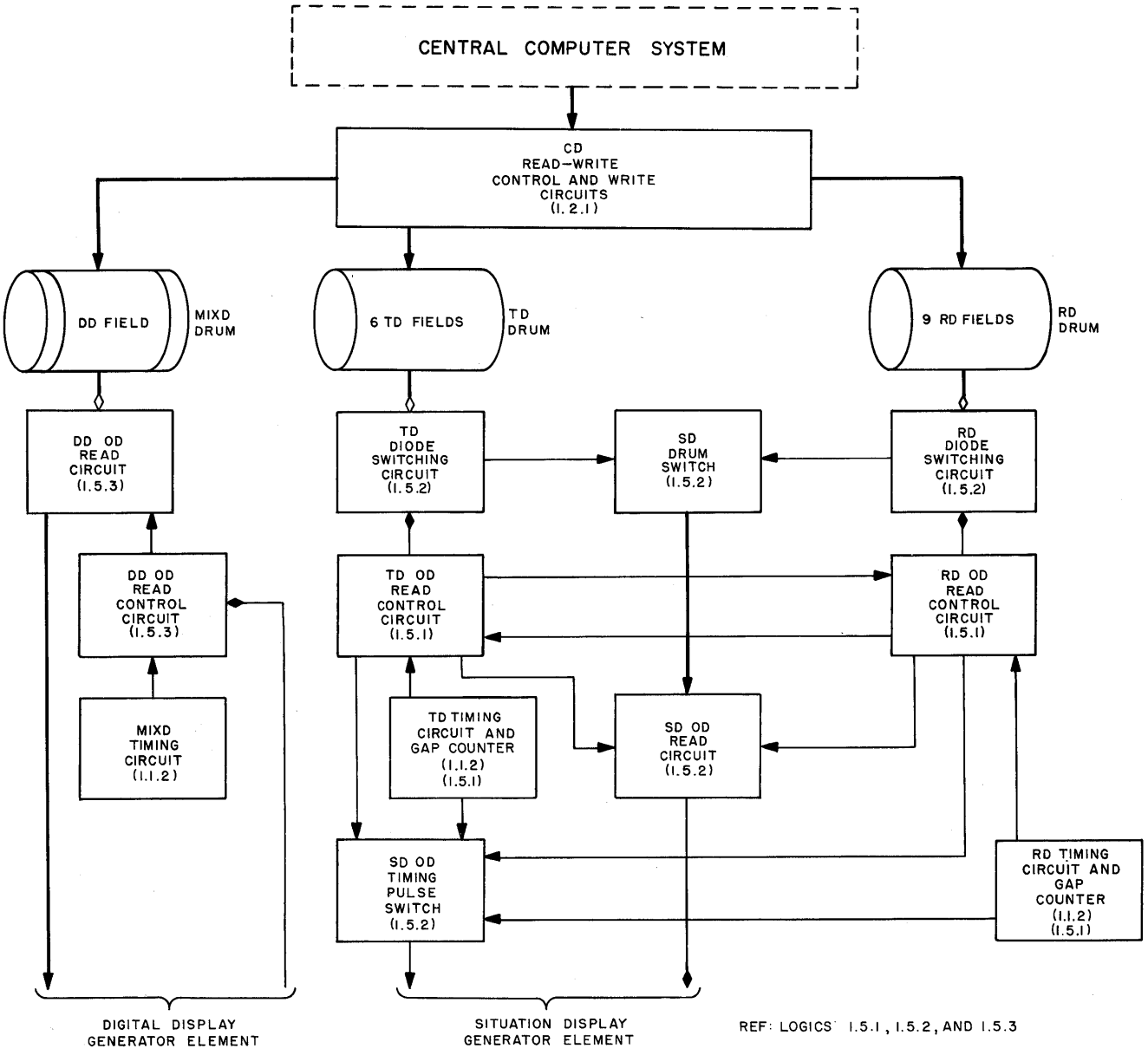


Figure 3–3. Transfer of Display Fields Data, Block Diagram

by the TD-timing-circuit-and-gap counter. The pattern involves skipping a fixed number of multiword slots before the reading of each multiword slot. As in DD reading, the read pattern is precessed at the end of each revolution.

During RD reading, the SD read circuit is controlled by the RD-read-control circuit. Like the other two display read-control circuits, the RD circuit has a precessed reading pattern that introduces a time delay between readings of successive slots.

When TD reading is completed, a signal from the TD-read-control circuit goes to the RD-read-control circuit and starts the RD reading operation. When reading of the RD fields is completed, the RD-read-control circuit sends a signal to the TD-read-control circuit, recommending the TD reading operation.

During the time each drum is being read, its associated timing circuit, gap counter, and read control circuit send control signals or timing pulses to the SD timing pulse switch. The signals from the drum being read are then switched to the SDGE. Two types of timing pulses are developed by the two timing circuits and gap counters: drum timing pulses which are developed during any of 2,060 timing cycles (RD or TD drum)

and OD pulses from the 2,048 cycles between the 13th and the 2,060th timing cycle.

3.1 TRANSFER OF DIGITAL DISPLAY DATA

Digital display information is interleaved by the Central Computer System before it is written on the CD side of the Drum System. Therefore, successive words of a message are not written in successive drum registers.

During OD reading, the message is transferred in the proper sequence by having the read circuits alternately skip and read in a pattern that results in six 40-usec intervals between the readings of consecutive message words. This pattern makes it necessary for the drum to turn through 64 revolutions before the entire DD field is read. At the end of each revolution, the reading pattern is stepped one number ahead of its normal count to ensure that all registers are read.

3.1.1 DD OD Reading, Functional Analysis

Digital display reading is initiated on the OD display circuits when the start-read portion of the DD-read-control circuit receives a control pulse from the DDGE. The start-DD-read pulse conditions the start-read circuit to gate OD 2 and index pulses to the register counter as step pulses.

Step pulses are counted in the register counter, producing an output level when 63 have been counted. The output level goes to the read-sample gate, causing the development of a read-sample pulse at the 64th OD 1 pulse.

Read-sample pulses go to the DD read gates and the DDGE. In the drum read amplifiers, the read-sample pulse causes the transfer of the information word in the 64th drum register to the generator element. In the DDGE, read-sample pulses step a timing counter that counts the number of DD words received from the DDGE.

During the same drum register that the OD 1 read-sample pulse is produced, but 2.5 usec later, the 64th OD 2 step pulse returns the register counter to 0. The counter restarts its cycle of 64 when it receives the 65th step pulse.

In this manner, 63 drum registers are skipped, the 64th is read, 63 skipped again, the 128th read, and so on in the same reading pattern. During the 2,048 registers of one MIXD drum revolution, 32 read samples are produced. To prevent the read samples of the second revolution from being produced at the same registers as the read samples of the first revolution, the register counter is precessed by counting the index as well as the OD 2 pulse during the 2,048th register. As a result, the second-revolution-read-sample pulses are generated at the 63rd register, the 127th register, and so on.

Index pulses continue to form additional step pulses once each revolution. Each time an additional step pulse is formed, the read-sample pulses produced during the following revolution appear one register earlier. In 64 revolutions of the MIXD drum, 64 additional step pulses are formed and every register on the drum field is read once.

At the end of the 64th revolution, the index pulse coincides with the register counter d-c output level. This produces an end-DD pulse, which stops DD reading until a new start-DD-reading pulse is sent by the DDGE.

3.1.2 DD OD Reading, Circuit Analysis

Digital display OD reading (fig. 3–4) begins with a start-DD-read pulse from the DDGE.

In the DD-OD-read-control circuit, the pulse sets FF 1 of the start-read circuit to the 1 side. The resulting level conditions gate 1 (GT 1) to pass OD 2 and index pulses from OR 1 to the register counter as step pulses.

During the first 2,047 registers of the drum, OD 2 pulses provide the only inputs to OR 1. At the 2,048th register, the OD 2 pulse produces conduction in the OR circuit; in addition, conduction is produced by the MIXD-index pulse at OD 3 time.

The register counter (fig. 3–5) counts the step pulse inputs from the start-read circuit. The counting process is the same as that described for the angular position counter (APC) in 4.4.1.

At the time of the 63rd step pulse, all flip-flops in the register counter are set, causing conduction in AND 1. The output of AND 1 conditions GT's 3 and 4 (fig. 3–4). Before the 64th OD 2 step pulse clears the counter, the 64th OD 1 pulse from the MIXD timing circuit is passed by GT 3. Except for the time when the DD field is being tested, an operate level from the computer-test-control circuit conditions GT 5 to pass the output of GT 3. The resulting pulse is the DD-read-sample pulse, which is sent to the DD read circuit to release a word to the DDGE.

In the DD read circuit, the read-sample pulse is gated to the DDGE by each of 32 drum read amplifiers, which detect 1 bits on the drum field. A 33rd drum read amplifier is present for the parity bit, but this bit is only for testing.

Although not indicated in figure 3–4, the read sample also goes directly to the DDGE as a load-DD pulse and to the test circuit as a DD-test-read-sample pulse. In the generator element, the load-DD pulses are counted to determine the number of words read by the DD read circuits.

This pattern of skipping 63 registers and producing a read-sample pulse every 64th register is continued for

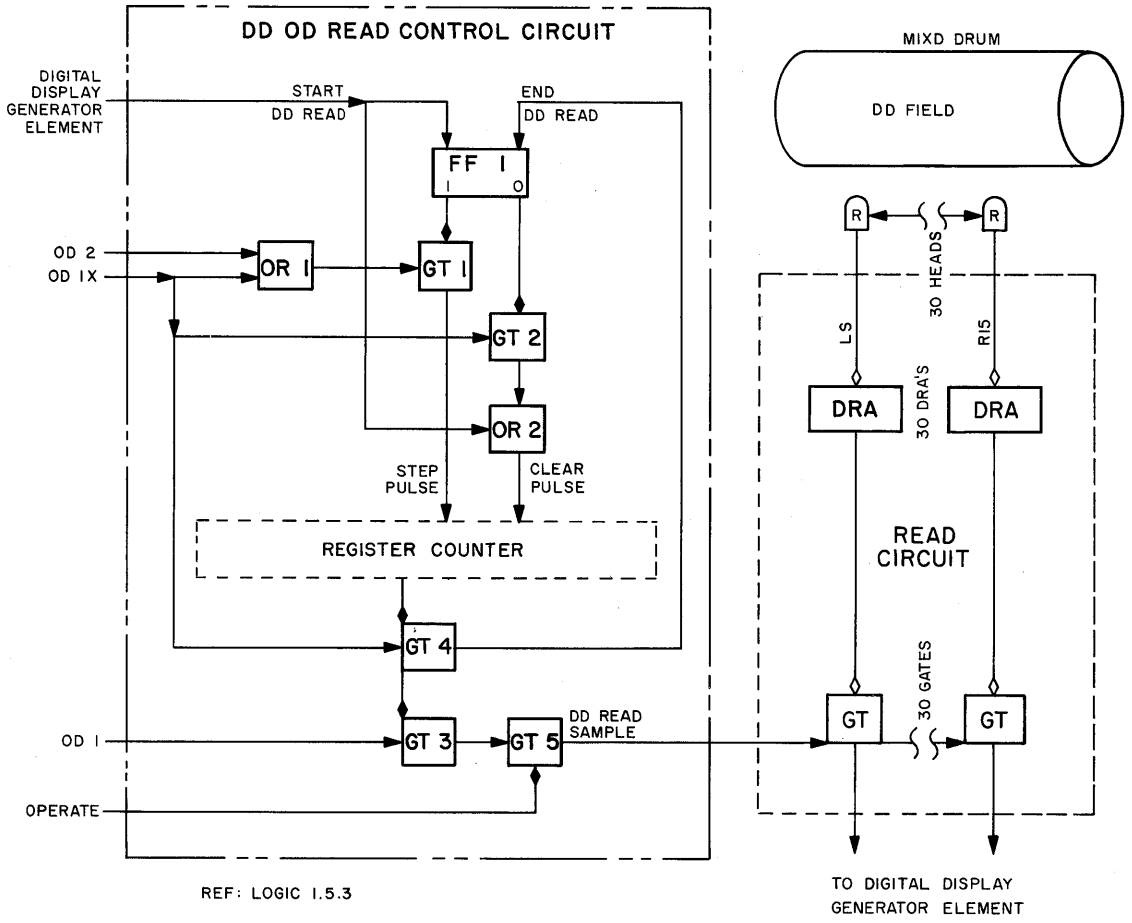


Figure 3–4. Digital Display OD Reading Operation, Simplified Logic Diagram

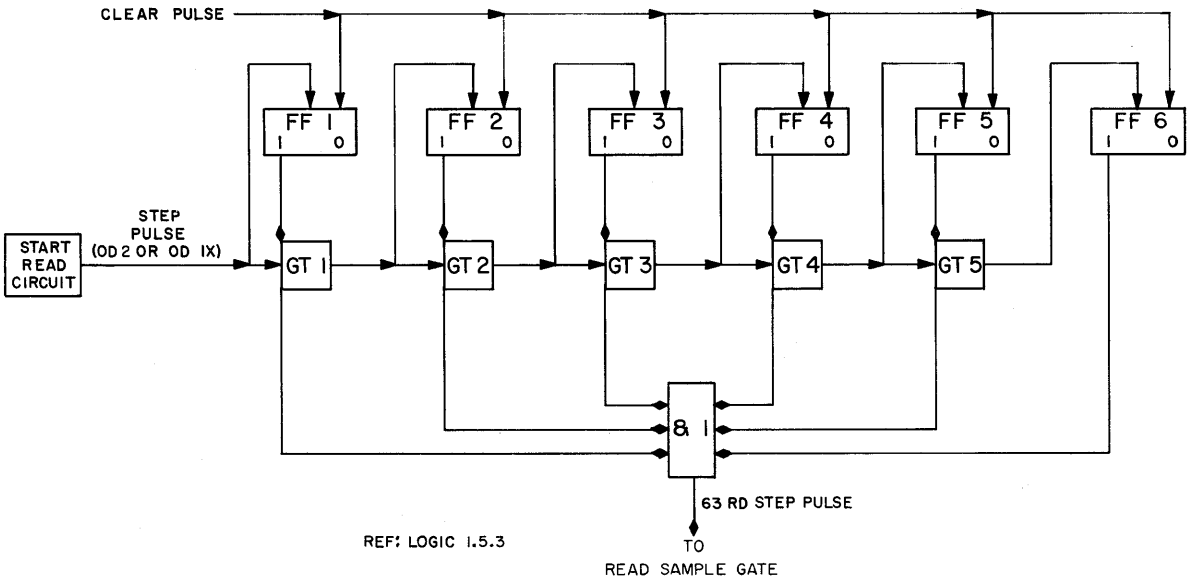


Figure 3–5. Digital Display Register Counter, Simplified Logic Diagram

a complete drum revolution. During the last register of the revolution, the OD-index pulse (at OD 3 time) serves as an alternate input to OR 1. The OR 1 output is passed by GT 1 to form a step pulse. This extra step pulse during the 2,048th register precesses the register counter so that the read-sample pulses produced by its outputs coincide with the 63rd, 127th, 191st, and so on, registers of the second revolution. At the end of the second revolution, precession causes a read-sample pulse to coincide with the 62nd register, then the 126th, 190th, and so on. At the end of the 64th revolution, all drum registers on the DD field are read, and the register counter output level coincides with an OD-index pulse. This coincidence in GT 4 forms an end-DD-read pulse (fig. 3–4).

The end-DD-read pulse goes to the start-read circuit, clearing FF 1. The rise time of the 0 output of the flip-flop is not fast enough to pass the same index pulse that is at GT 2; but, at the end of the following drum revolution, the next index pulse is passed. This gated index pulse clears the register counter flip-flops. No DD-read-sample pulses can be produced thereafter until another start-DD-read pulse sets FF 1.

Figure 3–6 indicates the DD registers for which read-sample pulses are produced during each revolution of the MIXD drum.

3.2 TRANSFER OF SITUATION DISPLAY DATA, FUNCTIONAL ANALYSIS

Situation display reading begins in the OD display circuits (logic 1.5.1) when the Drum System is energized. A power-on-reset signal from the manual control panel is sent to the TD-OD-read-control circuit (fig. 3–7), in which the power-on-reset pulse produces a field-select level. This level goes to the TD-diode-switching circuit to cause the contents of field 1 to be switched into the SD drum switch. The drum switch enables the OD display circuit to use one set of read circuits for both TD and RD words by transferring the contents of the selected field from the drum that is being read to the SD OD read circuits. At the end of every 13th TD drum revolution, the field-select level is changed, switching the contents of fields 1 through 6, in that order, into the read circuits. The TD OD gap counter develops a 120-usec delay at the beginning of each revolution, which provides for decay of switching transients when fields are being switched. (Refer to Ch 6 of Part 2.)

The field contents are passed through the read circuits to the SDGE when an SD-read-sample pulse is received by the read circuits from the TD-OD-read-control circuit. Read-sample pulses are produced in a regular pattern. While the first 128-word slots of a TD field pass under the read heads, no read-sample pulses are produced; however, eight read-sample pulses are

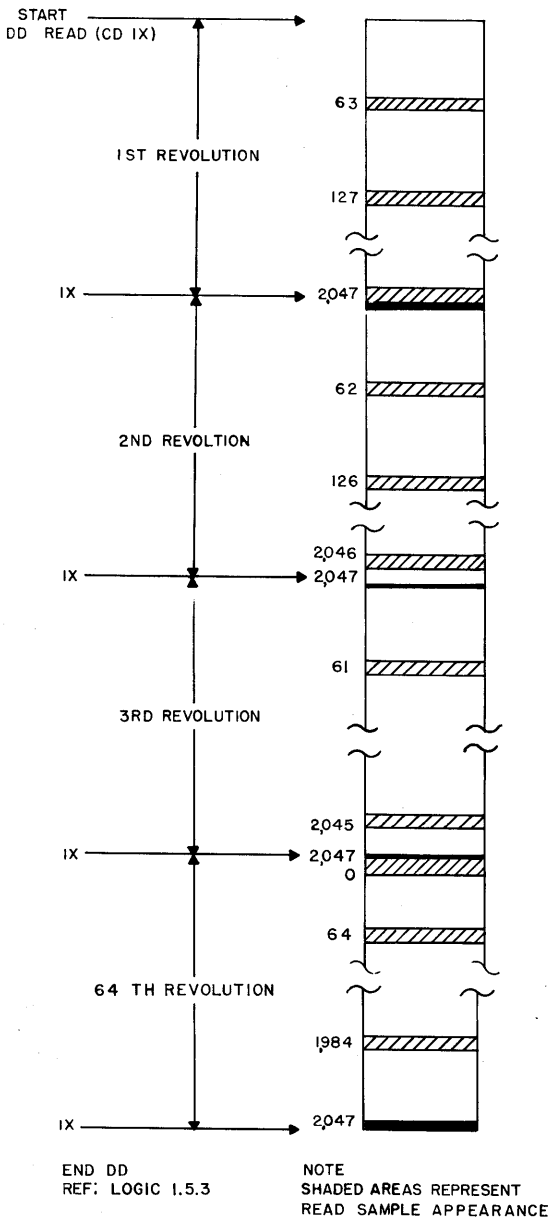


Figure 3–6. Sequence of Digital Display Reading

produced (one for each word) for the 13th slot. Twelve more slots are skipped, and one is read into the generator element. During the last drum register of each revolution, an index pulse from the TD timing circuit advances the slot count. By the end of 13 drum revolutions, all slots of the selected TD field are read.

Two and one-half usec before each read-sample pulse is produced, a TD-word-on-way (WOW) pulse is generated to inform the SDGE that a word is about to be read. The WOW pulses go to the SDGE via the SD timing pulse switch, which transfers them along with timing and index pulses from the TD timing circuit.

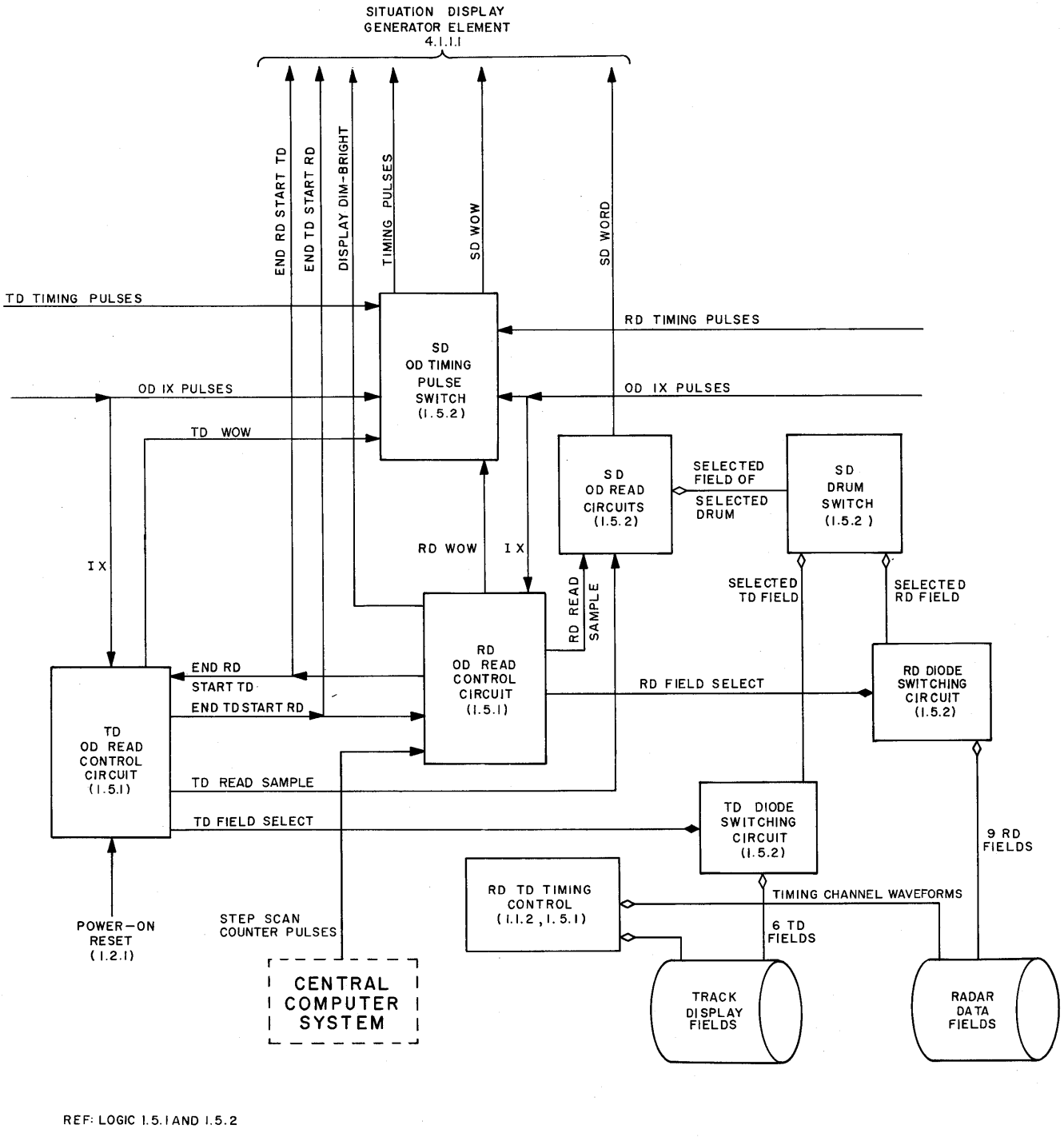


Figure 3–7. Situation Display Reading, Block Diagram

After the drum has rotated 78 times (13 times for each of the six fields), all registers of the TD drum have been read, and an end-TD-start-RD pulse is produced in the TD-OD-read-control circuit. This pulse stops TD reading and goes to the RD-read-control circuit to begin RD reading. It also goes to the SDGE to condition the element to present RD information.

At the start of RD reading, the RD-read-control circuit produces a field-select level which designates the first field to be read. The first field selection to be made

is computed by adding 1 to the number of step-scan-counter pulses that have been sent to the RD-read-control circuit by the Central Computer System. The total number of pulses received indicates which field is written on by the Central Computer System. By adding 1 to the number, RD selection circuits begin reading the earliest written information first. The next seven fields are selected for reading in numerical order. The field being written on by the Central Computer System is not read during the same read cycle as the other eight fields. The contents of the selected field are switched into the SD read circuits by the RD-diode-switching circuit and the SD drum switch. The RD gap counter provides the 120-usec delay required by the read circuits for switching time (4.2.3.1 of Part 2). Each time a read-sample pulse is produced by the RD-read-control circuit, the information at the SD read circuits is sent to the SDGE.

Read-sample pulses for RD reading are produced according to a pattern which provides for the skipping of five registers between the production of two successive read-sample pulses. This pattern of reading one register and skipping five is repetitive, continuing for three drum revolutions. At the end of the third revolution, all the odd registers will have been read. At this time, the reading pattern is precessed one register by an RD-index pulse, permitting reading of the even registers during the next three drum revolutions. Thus, by the end of six drum revolutions, all the registers of the selected RD field are read. Table 3–1 indicates the sequence in which the registers of the selected TD field are read. Only the registers of the first and last slot read during a given drum revolution are shown in the table. Similarly, table 3–2 indicates the sequence in

TABLE 3–2. SEQUENCE OF READING OF RD FIELD REGISTERS

RD DRUM REVOLUTION	FIRST REGISTER AT WHICH RD READ SAMPLE IS PRODUCED	LAST REGISTER AT WHICH RD READ SAMPLE IS PRODUCED
1	1	2047
2	5	2045
3	3	2043
4	0	2046
5	4	2044
6	2	2042

TABLE 3–1. TD FIELD SEQUENTIAL READING RELATIONSHIP

TD DRUM REVOLUTION	FIRST GROUP OF REGISTERS AT WHICH TD READ SAMPLES ARE PRODUCED	CORRESPONDING SLOT NUMBER	LAST GROUP OF REGISTERS AT WHICH TD READ SAMPLES ARE PRODUCED	CORRESPONDING SLOT NUMBER
1	96-103	13	1968-1975	247
2	16-23	3	1992-1999	250
3	40-47	6	2016-2023	253
4	64-71	9	2040-2047	256
5	88-95	12	1960-1967	246
6	8-15	2	1984-1991	249
7	32-39	5	2008-2015	252
8	56-63	8	2032-2039	255
9	80-87	11	1952-1959	245
10	0-7	1	1976-1983	248
11	24-31	4	2000-2007	251
12	48-55	7	2024-2031	254
13	72-79	10	1944-1951	244

which the registers of the selected RD field are read. Only the first register and the last register read during a given drum revolution are shown.

Two and one-half usec before the generation of each read-sample pulse, an RD WOW pulse (fig. 3–7) is produced to inform the generator element that a word is to be read. The WOW pulses go to the SD timing pulse switch. During RD reading, the RD WOW and RD timing and IX pulses (the latter from the RD timing circuit) are sent to the SDGE.

When the RD field containing the most recently written information is being read, the RD-read-control circuit sends display-bright pulses to the generator element. During the display of the other seven RD fields read during the same cycle, display-dim pulses are sent in place of the display-bright signal.

When all registers of eight RD fields are read, an end-RD-start-TD pulse is generated. This pulse is sent to the TD-read-control circuit and the SDGE. In the read-control circuit, it starts the TD reading operation. In the generator element, the start-TD pulse conditions the display circuits to present the data read out during the track data reading cycle.

3.3 TRACK DISPLAY OD READING, FUNCTIONAL ANALYSIS

Situation display OD operations begin with the reading of the TD drum. When the Drum System is energized, a power-on-reset pulse goes from the manual control panel to the TD-read-control circuit (fig. 3–8). In the start-read portion of the read-control circuit, the power-on-reset pulse produces a reset pulse, which clears the register, slot, and field counters.

The field counter, when cleared, produces a field-select level for TD field 1 in the field selection matrix. The field-select level is applied to the read heads of TD field 1 to prepare them for a reading operation.

The start-read circuit passes OD 2 pulses to the register counter as a register-counter-step pulse. The register counter is a scale-of-8 counter which produces a slot-counter-step pulse every time it counts eight register-counter-step pulses. The slot-counter-step pulses go to the slot counter, which is a scale-of-13 counter. The 12th slot-counter-step pulse counted produces a level which, in conjunction with the drum timing level from the TD OD gap counter, produces a read and step-field d-c level. (The TD OD gap counter provides the 120-usec delay necessary to permit decay of field switching transients.)

The read level passes timing pulses in the read-sample and WOW gates to send WOW pulses to the SD timing pulse switch and TD-read-sample pulses to the SD read circuits. A WOW pulse is sent to the SDGE to prepare the element to receive a TD word. The TD word is sent 2.5 usec later when the read-sample pulse samples the read gates in the SD OD read circuit. Eight read-sample pulses are produced, one for each of eight registers counted by the register counter. The eighth pulse counted produces the slot-step pulse, which clears the slot counter.

Twelve more slots are counted before another slot is read. The process of skipping 12 slots and reading one continues until one drum revolution is completed. The index pulse then acts as a slot-counter-step pulse and advances the slot counter. As a result, all groups of eight read-sample pulses are produced one slot earlier than if normal counting had continued in the slot counter. This continues for 13 revolutions. At the end of the 13th revolution, all registers in the field have been read and the step-field level at the output of the slot counter coincides with the index pulse. The output resulting from this coincidence is used to step the field counters. The changed field counter output goes to the field selection matrix and produces a field-select level that designates the next TD field.

3.4 TRACK DISPLAY OD READING, CIRCUIT ANALYSIS

Track display OD reading can be divided into two operations: development of the reading pattern and field switching. The circuits used to produce the precessed reading pattern employed for TD reading are described in 3.4.1; those used to switch from one TD field to another are described in 3.4.2.

3.4.1 TD Reading Pattern Development, Circuit Analysis

The SD OD circuits employed to develop the precessed reading pattern used for TD are shown in figure 3–9.

When the Drum System is first energized, a power-on-reset pulse is sent to the start-read portion of the TD-read-control circuit to initiate the SD reading operation. During subsequent SD reading cycles, end-RD-start-TD pulses from the RD-read-control circuit start the reading operation. Either pulse will produce at the output of OR 1 (fig. 3–9) a start-TD-and-reset pulse, which sets FF 1 and clears the register counter, the slot counter, and the field selection counter. The start-TD-and-reset pulse also clears FF 2 by producing conduction in OR 2. The 1 output of FF 1 conditions the passing of OD IX pulses at GT 1. The GT 1 output sets FF 2 to the 1 state. The level at the 1 output of FF 2 goes to the field-switching circuits as a TD-select level and passes OD 2 pulses from the TD timing circuit at GT 2. Gate 3 is also conditioned by the same level, but not in time to pass the index pulse that sets FF 2.

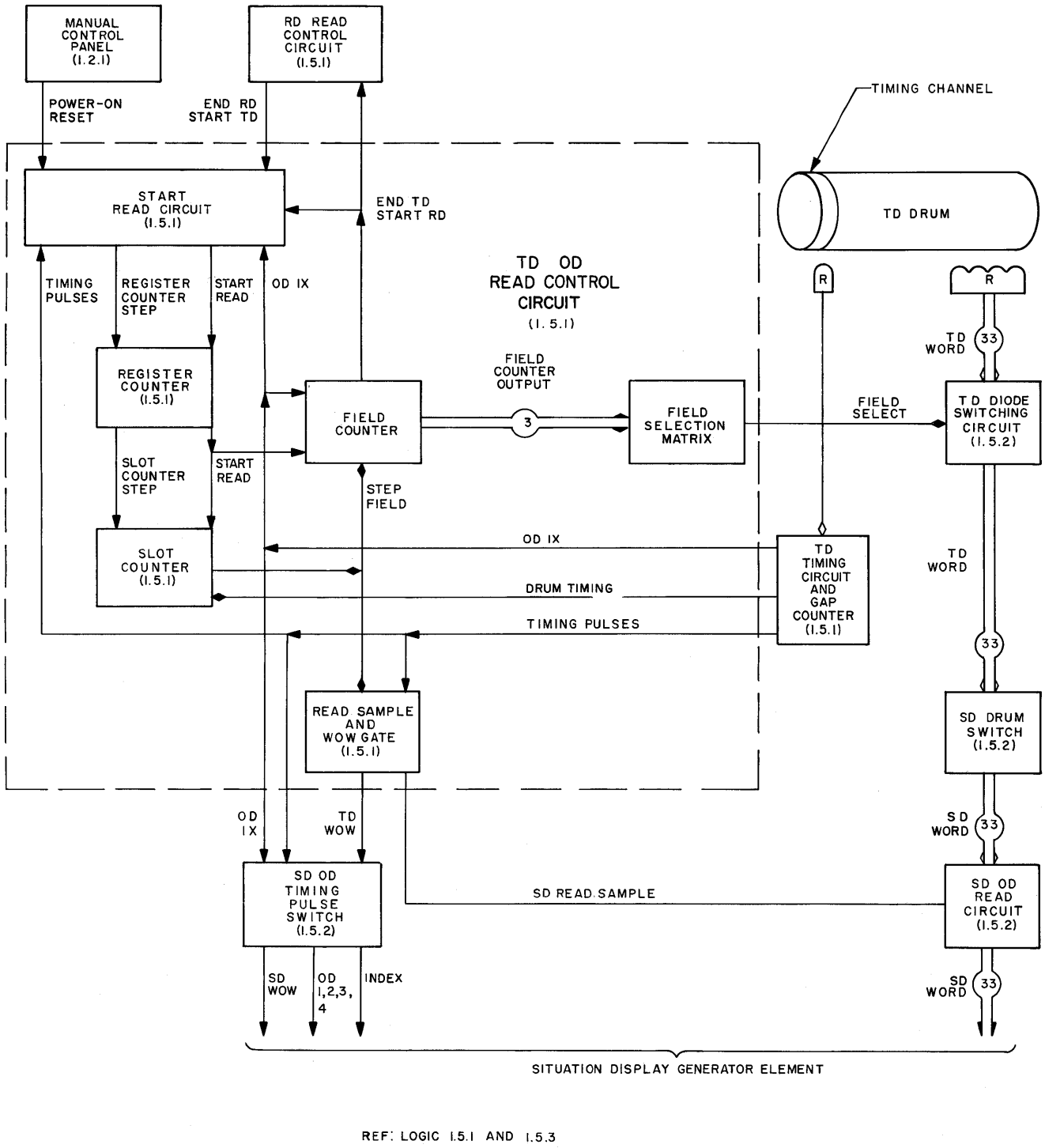


Figure 3–8. Track Display OD Reading, Block Diagram

The GT 2 output pulses form register-counter-step pulses, which clear FF 1 and step the register counter. The register counter is a scale-of-8 counter which operates on the principles described in 3.1.1. Every eighth step pulse counted by the register counter produces an end-carry-output pulse. Since the TD drum is written in 8-word slots by the Central Computer System, each register counter pulse output represents one slot.

The register counter output goes to OR 3, causing it to conduct. The pulses taken from the output side

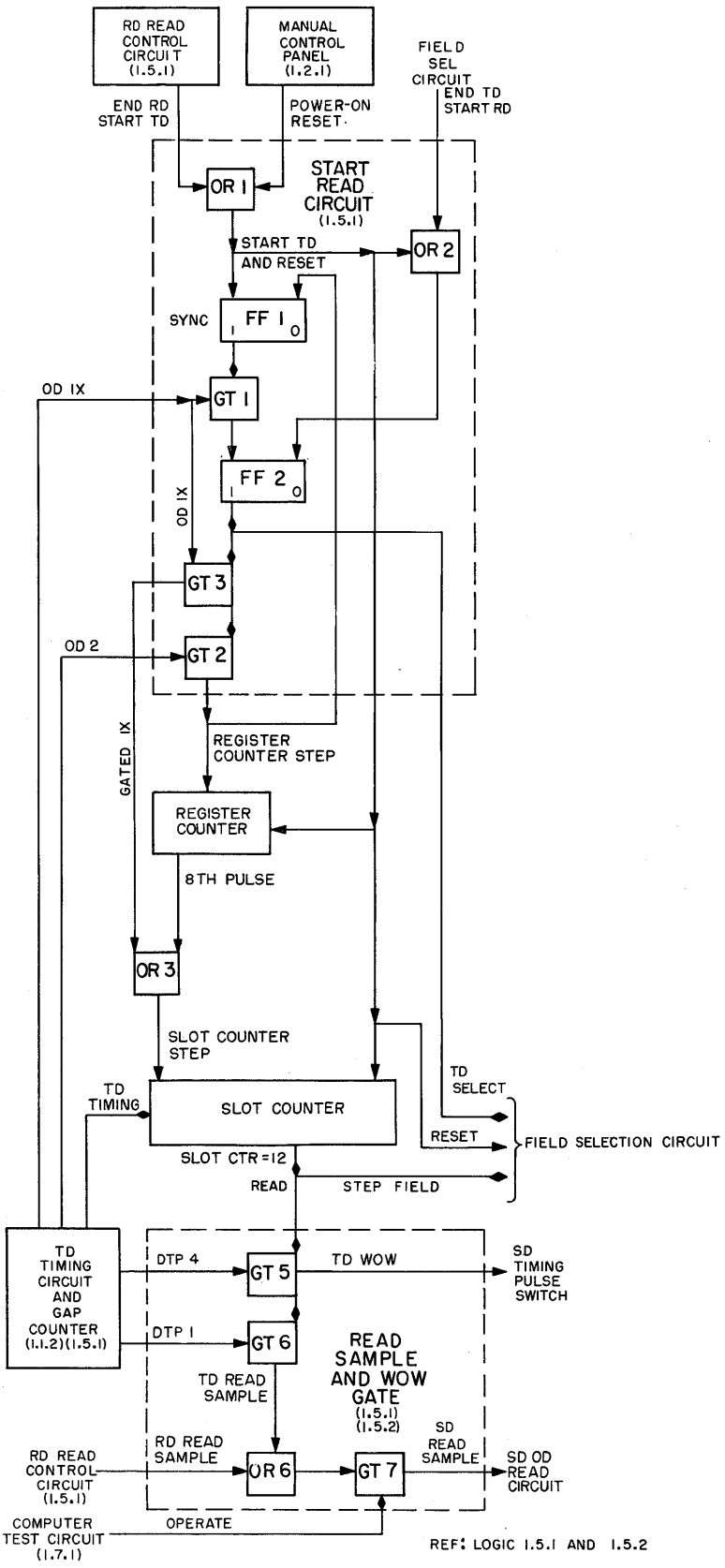


Figure 3–9. Track Display Reading Pattern Development, Simplified Logic Diagram

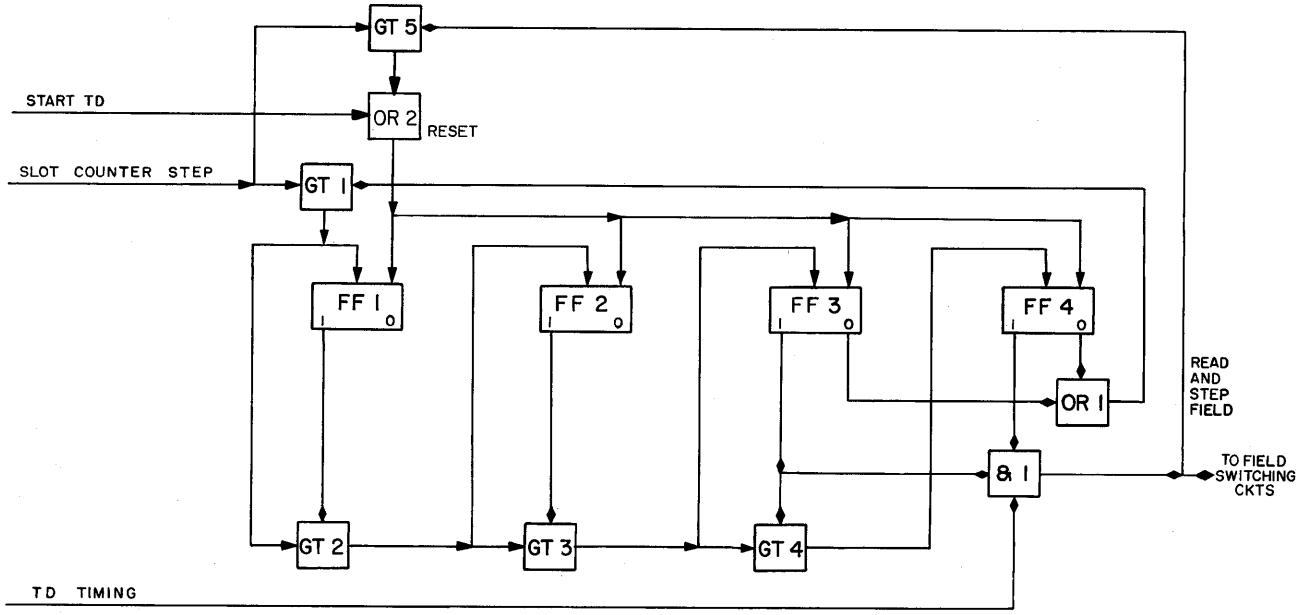


Figure 3—10. Track Display Slot Counter, Simplified Logic Diagram

of OR 3, called slot-counter-step pulses, are used to step the slot counter. The slot counter is a scale-of-13 counter, the operation of which follows (fig. 3—10). The counter is initially cleared by the start-TD pulse at OR 2. With FF 3 or 4 at 0, OR 1 conducts. The output of OR 1 conditions GT 1 to pass slot-counter-step pulses to the counter (3.1.1). The 0 output of either FF 3 or FF 4 or both maintains conduction in OR 1 until 12 slot-counter-step pulses have been counted. At this time, FF's 3 and 4 are in the 1 state. The 1 outputs of both flip-flops produce conduction in AND 1 when added to the TD timing level. The level at the output of AND 1 is called the read-and-step-field level. It remains at the output of AND 1 until the next slot-counter-step pulse arrives at GT 5, eight registers (one slot) later. The step-field level conditions the passing of this 13th slot-counter-step pulse at GT 5 or OR 2. (Since there are no 0 outputs from FF's 3 and 4 during the 12th slot-counter-step pulse, GT 1 will not be conditioned to pass the 13th slot-counter-step pulse.) The output of OR 2 clears the counter. At the next slot-counter-step pulse, counting begins again.

During the period between the 12th and the 13th slot-counter pulses, the read level (fig. 3—9) passes eight drum timing pulses in GT 5 to produce eight TD WOW pulses. The WOW pulses go to the OD timing pulse switch. They are then relayed to the SDGE to prepare to receive words from the drums. The words are produced 2.5 usec later by having the step-field level pass DTP 1 pulses in GT 6. The output of GT 6 is the TD-read-sample pulse, which produces conduction in OR 6. The output of OR 6 is passed by GT 7, which is conditioned by an operate level from the computer-test-control circuit. (The operate level is present during normal operation but absent during test procedures.) The TD-read-sample pulses thus become SD-read-sample pulses. They go to the SD read circuits and serve to transfer the TD word to the SDGE.

In this manner, 12 8-word slots are counted before one slot of 8 is read. At the end of the reading of that one slot, no read-sample pulses are developed until 12 more slots have been skipped.

The skip-12, read-1, skip-12 pattern continues until the first revolution of the drum is completed. At this time, an index pulse is passed through GT 3 to duplicate the functions of the slot-counter-step pulse. As a result, the slot counter is stepped ahead in its count. Each group of eight read-sample pulses is produced one slot earlier at each successive revolution of the drum. The first group of read-sample pulses is delayed 120 usec to allow for field switching by skipping the first 12 timing cycles at the beginning of each revolution. This is accomplished by means of the gap counter.

At the end of 13 drum revolutions, all registers on the selected TD field have been read. The TD-index pulse then clears the slot counter to prepare it to count for the next field.

3.4.2 TD Field Switching, Circuit Analysis

When the first TD reading operation begins (3.4.1), the start-TD-and-reset pulse which clears the counters in the read-pattern-development circuits also clears the field counter of the TD-field-switching circuits (fig. 3–11). Thereafter, the field counter is stepped by the output of GT 1. Gate 1 conducts when the step-field level from the slot counter (3.4.1) is coincident with the index pulse. This condition exists at the end of every 13th revolution of the drum. Thus, as soon as all registers of a field are read (after 13 revolutions), the field counter is stepped and the next field is selected.

The output of the field counter selects the next fields by establishing a combination of d-c levels at the input to the field selection matrix (fig. 3–11).

When the field counter is cleared, the combination of the 0 outputs from its three flip-flops and the TD-select level (produced by starting TD reading) provide the necessary conditions for conduction in AND 1. When AND 1 conducts, it produces a select-field-1 level, which goes to the center taps on the 33 read heads of the first TD field, enabling them to conduct.

When the field counter is stepped, levels at its output change, causing different AND circuits in the field selection matrix to conduct. The earlier field-select level decays, and a new one is produced. Table 3–3 shows the flip-flop output combinations that produce conduction in the different AND circuits in the matrix, and the field that is selected as a result.

At the sixth input (the 5th step-field pulse after the reset pulse) to the field counter, AND 7 conducts, conditioning GT 2. The sixth step-field pulse is passed to GT 2, forming an end-TD-start-RD pulse. This pulse is sent to the start-TD-read circuit (fig. 3–9), where it

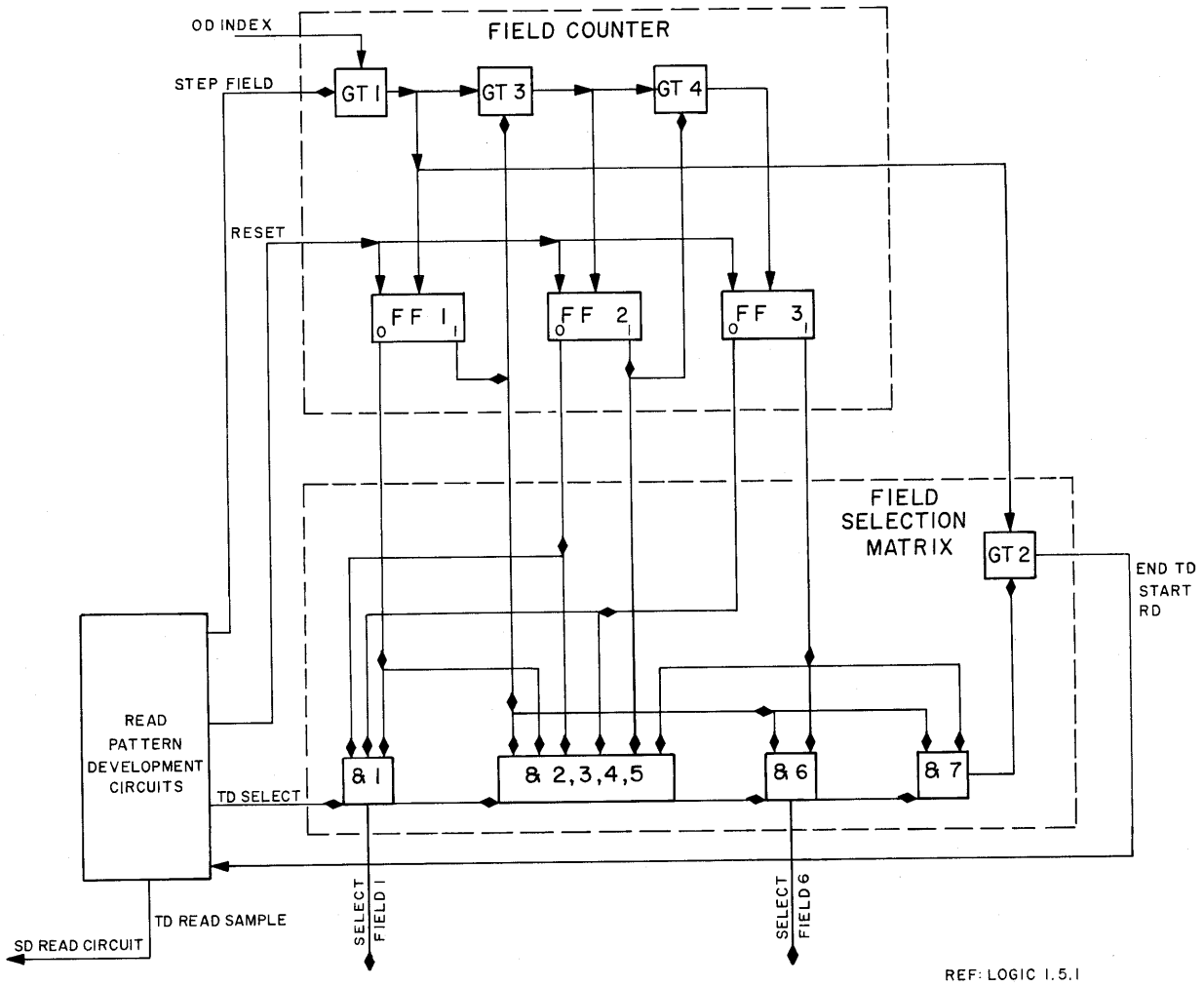


Figure 3–11. Track Display Field Selection Circuits, Simplified Logic Diagram

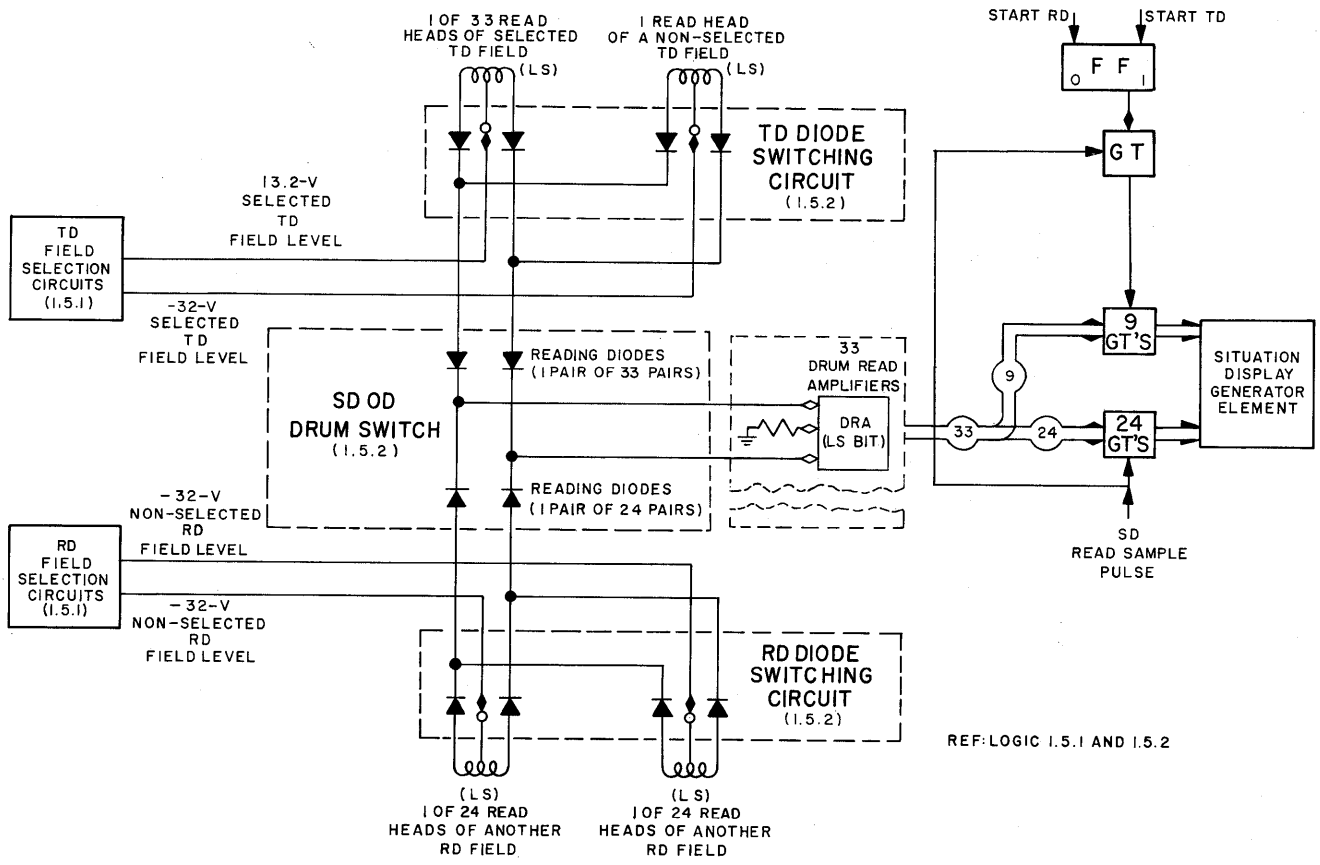


Figure 3–12. Track Display and Radar-Data-Field-Switching and Reading Circuit, Simplified Logic Diagram

TABLE 3–3. TRACK DISPLAY FIELD SELECTION

STEP FIELD GATED INDEX PULSES	COUNTER OUTPUTS FLIP-FLOP 1	FLIP-FLOP 2	FLIP-FLOP 3	AND CIRCUIT	FIELD SELECTED
Reset Pulse	0	0	0	1	1
1st	1	0	0	2	2
2nd	0	1		3	3
3rd	1	1		4	4
4th	0		1	5	5
5th	1		1	6	6

clears FF 2, thus stopping the development of the reading pattern.

The read heads for all TD fields are connected to the same 33 pairs of reading diodes in the SD drum switch, but only the heads of the selected field conduct (fig. 3–12). The TD-diode-switching circuit prevents conduction of the read heads in nonselected TD fields by isolating the selected TD-field level from these read heads.

Similarly, the SD OD drum switch permits the use of the same drum read amplifiers for reading of the TD or the RD drums. The reading diodes in the SD

OD drum switch isolate the selected field level of either drum from the circuits of the other. (Refer to Ch 5 of Part 2.)

3.5 RADAR DATA OD READING, FUNCTIONAL ANALYSIS

Radar data reading follows TD reading, beginning when the end-TD-start-RD pulse, from the TD-read-control circuit, enters the RD-start-read-control circuit (fig. 3–13). The start-read circuit is conditioned to pass OD 2 and index pulses to the register counter as step-register-counter pulses. The start-read circuit also forms an RD-select level which goes to the read-sample and WOW-gate circuit, field selection matrix, and SD OD timing pulse switch.

The register counter is a scale-of-6 counter. The first step-register-counter pulse counted in each counting cycle produces a read level of the register counter output. The step-field-read-counter level is sent to the read-sample-and-WOW-gate-and intensity control. In the latter circuit, it conditions the passing of an OD 4 pulse to form an RD WOW pulse. This pulse is sent to the SD timing pulse switch. From the timing pulse switch it is sent to the SDGE to inform the element that a word is about to be sent by the RD circuits.

Two and one-half usec after the production of the RD-WOW pulse, an OD 1 pulse is passed to produce an RD-read-sample pulse. The read-sample pulse is sent to the TD-read-sample-and-WOW gate to form an SD-read-sample pulse (fig. 3–9). The SD-read-sample pulse is passed by the 1 bits in the SD read circuits, thereby transferring the RD word into the SDGE.

During the second through the sixth-step-register-counter pulses in the register counter counting cycle, there is no counter output. Therefore, no WOW pulses or read-sample pulses are produced for five registers. This pattern of reading one register and skipping five is repetitive, continuing for three drum revolutions. At the end of the third revolution, all the odd registers will have been read. At this time, the reading pattern is precessed one register by an RD-index pulse, permitting reading of the even registers during the next three drum revolutions. At the end of six drum revolutions, all drum registers are read. An RD-OD-index pulse is gated by the read-sample-and-WOW-gate-and-intensity-control circuit and becomes a step-field-switching-counter pulse (fig. 3–13). This pulse is sent to the fields counter, the field-switching counter, and the register counter. The levels at the field-switching counters output go to the field selection matrix to produce select-field levels, which indicate the RD field to be read next. Reading is done by sending the select-field levels to the RD-diode-switching circuits, which transfer the contents of the selected RD field into the SD OD read circuit via the SD drum switch. Radar data information bits at the SD read circuit are transferred to the SDGE by SD-read-sample pulses. The SD-read-sample pulses, as indicated above, come from the RD-read-sample-and-WOW gate whenever RD-read-sample pulses are produced by the RD-read-control circuit.

The field-switching counter selects the first RD field to be read by adding 1 to the number of step-scan pulses sent to the scan counter synchronizer by the Central Computer System. The total number of pulses received from the Central Computer System indicates the RD field that is to be written on by the Central Computer System. Each time the Central Computer System begins writing on a new field, another step-scan pulse is sent.

The step-scan-counter pulses from the Central Computer System are synchronized with the RD timing pulses in the scan counter synchronizer. The synchronizer is initially cleared by the power-on-reset pulse, which initiates SD OD reading. The synchronized step-scan-counter pulses at the synchronizer output are sent to the scan counter, stepping it until it is set at the number of the field on which the Central Computer System is to write. During TD reading only, the contents of the scan counter (indicating the first field to be read) are transferred to the field selection counter by a transfer-scan-counter pulse. Thereafter, the field selection counter is stepped by step-field-selection-counter pulses from the read-sample-and-WOW-gate-and-intensity control.

The RD field read first contains the oldest data; the field read last, the most recent data. During the time that the first seven selected fields are read, the read-sample pulses are passed through a gate in the read-sample-and-WOW-gate-and-intensity control to produce display-dim pulses. During the reading of the eighth field, the read-sample pulses are gated to produce display-bright pulses. These pulses are sent to the SDGE. In the SDGE, these pulses cause either dimming of the presentation of those fields containing older data or brightening of the field containing the most recent data, depending on which pulse is present.

3.6 RADAR DATA OD READING, CIRCUIT ANALYSIS

Radar data OD reading can be divided into two separate operations, development of the reading pattern and field switching. The circuits used to produce the precessed reading pattern employed by the RD drums are described in 3.6.1. The circuits used to switch from one RD field to the next and the circuits that enable the Central Computer System to select the first RD field to be read during each SD reading cycle are described in 3.6.2.

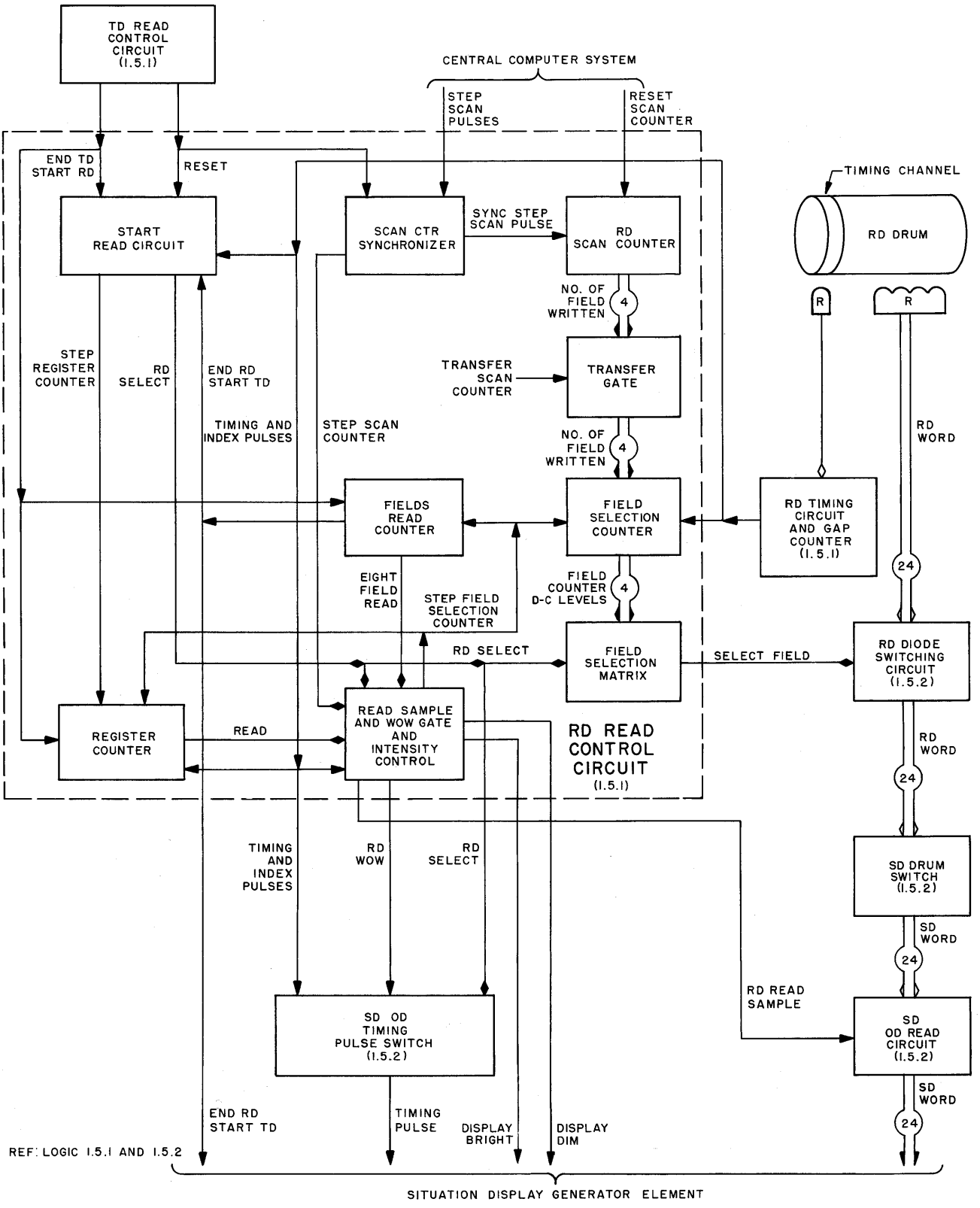


Figure 3–13. Radar Data OD Reading, Block Diagram

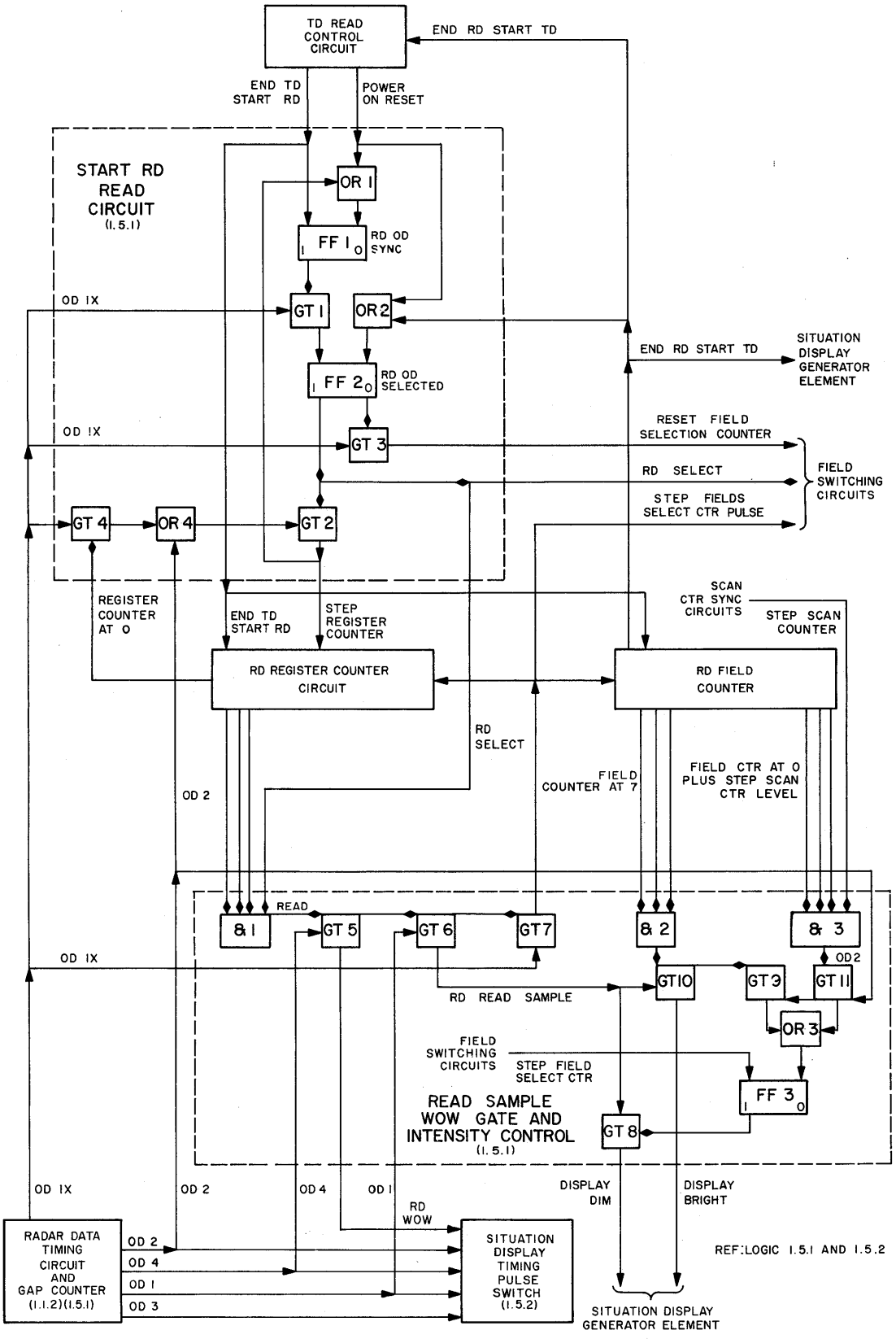


Figure 3–14. Radar Data Reading Pattern Development, Simplified Logic Diagram

3.6.1 RD Reading Pattern Development, Circuit Analysis

The OD display circuits employed to develop the precessed reading pattern used by the RD drum are shown in figure 3–14.

When the Drum System is energized, a power-on-reset pulse is sent through the TD-read-control circuit to the start-read portion of the RD-read-control circuit. This pulse causes conduction in OR's 1 and 2. The outputs of the two OR circuits clear FF's 1 and 2. The first OD-index pulse that occurs after the power-on-reset signal is passed in GT 3 by the 0 output of FF 2 to produce a reset-field-selection-counter pulse. The reset-field-selection-counter pulse clears the field selection counter (3.6.2).

The RD-read-control circuit components cleared by the power-on-reset-and-index pulse remain in the 0 condition during the period of TD reading and field switching. When reading of the TD drum is completed, the TD-read-control circuit produces an end-TD-start-RD pulse (3.4.2). This pulse sets FF 1 to the 1 side and clears the RD register counter and the RD field counter flip-flops. The 1 output of FF 1 passes the next index pulse from the RD timing circuit at GT 1 to set FF 2. The 1 output of FF 2 is the RD-select level, which goes to the field-switching circuits (3.6.2), the SD timing pulse switch (3.7), and to GT 2. Gate 2 is conditioned to pass OD 2 pulses from OR 4. (The first OD 2 pulse passed is the 13th in the timing channel. This is due to the fact that the first 12 cycles of OD pulses are skipped in the RD timing circuit.) The OR 4 outputs are called step-register-counter pulses, which go to the register counter.

The register counter is cleared by an end-TD-start-RD pulse (fig. 3–15). Gate 1 is conditioned by the output from OR 2. The first step-register-counter pulse is passed by GT 1 to set FF 1. Successive step pulses continue operating the counter in a manner similar to that of the counter explained in 3.1.1 (fig. 3–5). AND circuit 1 (fig. 3–13) conducts when the flip-flops are in a 1-0-1 state. The output from AND 1 conditions GT 2 to pass the sixth step-register-counter pulse. This pulse clears the flip-flops, causing AND 2 to conduct. The output from AND 2 is a register-counter-at-0 level.

AND 1 (fig. 3–14) will conduct when the three flip-flops of the register counter are simultaneously in the 1-0-0 state and the RD-select level is present. The output from AND 1 goes to GT's 5, 6, and 7. In GT's 5 and 6, the level conditions the passing of OD 4 and OD 1 pulses, respectively, to generate RD-WOW (OD 4) and read-sample (OD 1) pulses. The WOW pulse goes to the SD timing pulse switch to be transferred to the SDGE. Receipt of this signal informs the SDGE that a word will follow from the Drum System. Two and one-half usec later, the RD-read-sample pulse is developed and sent to the SD-read-sample-gate circuit (fig. 3–9 to produce an SD-read-sample pulse. The SD-read-sample pulse goes to the SD read circuit. In the SD read circuit,

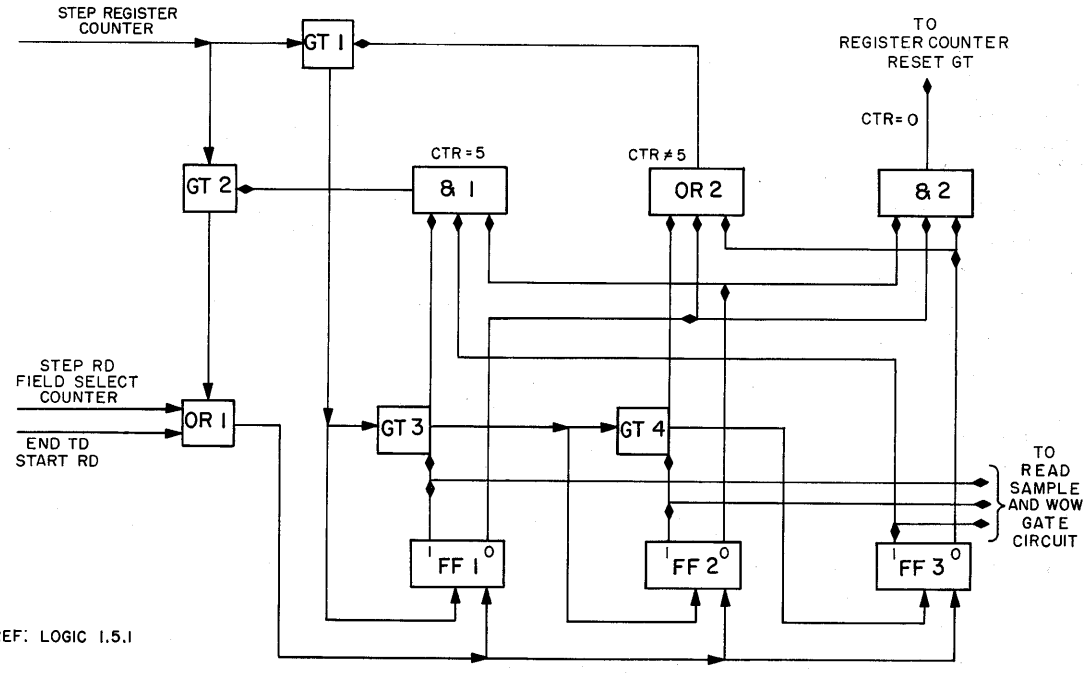


Figure 3–15. Radar Data OD Register Counter, Simplified Logic Diagram

it is passed to the SDGE by each 1 bit in the word that is switched by the SD drum switch at that time (3.4.2).

The RD-read-control, circuit produces a read-sample pulse at the second register (register 1; registers are numbered 0 through 2,047) and skips the next five registers (registers 2 through 6). Another read-sample pulse is produced at the eighth register (register 7). This pattern of reading one register and skipping five is repetitive, continuing for three drum revolutions. At the end of three drum revolutions, all odd-numbered registers on the field have been read. At this time, the OD-index pulse coincides with the register-counter-at-0 level in GT 4 (fig. 3–14). The resulting output goes to OR 4. Conduction in OR 4 produces a step-register-counter pulse at the output of GT 2. The additional step pulse generated at this time precesses the register counter. During the next three revolutions, all even-numbered registers are read. At the end of six revolutions, the step-fields-read-counter level is coincident with the index pulse in GT 7, to produce a step-field-select-counter pulse. The step-field-select-counter pulse clears the register counter and goes to the field-switching circuits.

In the read-pattern-development circuits (fig. 3–14), the step-field-select-counter pulse sets FF 3. The resulting 1 output passes the RD-read-sample pulses through GT 8, generating display-dim pulses, which go to the SDGE. While the display-dim pulse is present, RD information is dimmed on the CRT screens.

A branch of the step-field-select pulse goes to the field counter and steps the counter each time the pulse is produced. The counter is a 3-flip-flop, scale-of-8 circuit. At the seventh step-fields-select-counter input, reading of the eighth field begins and the counter flip-flops are all at 1. The three 1 outputs are combined in AND 2 to indicate that the counter is at 7 and the eighth field is being read. The output of AND 2 conditions GT's 9 and 10. Gate 9 passes an OD 2 pulse from the RD timing circuit to provide conduction in OR 3. Conduction in OR 3 clears FF 3 and prevents the generation of the display-dim pulse. Gate 10 passes read-sample pulses, producing display-bright pulses, which go to the SDGE during the reading of the eighth field. In the SDGE, the display-bright pulses cause brightening of the RD information being displayed. This action highlights the display of the information most recently written by the Central Computer System.

It is possible for the flow of information from the Central Computer System to get ahead of the display cycle. Were this to occur, the computer would select for writing the first field in the RD display cycle while it is being read. This would present new information to the Display System in a dim display, whereas new information should be displayed brightly.

To prevent confusion at the CRT screens if this occurs, the step-scan-counter level generated in the field selection circuits by the Central Computer System selection is sent to the read-sample-and-WOW-gate-and-intensity control. Occurring as it does when the three flip-flops in the field-read counter are all at 0, it produces conduction in AND 3 to develop a field-counter-at-0-step-scan-counter level. This level passes an OD 2 pulse in GT 11 to cause conduction in OR 3. This clears FF 3. With FF 3 cleared, no display-dim pulse is developed. Since the fields-read counter is not at 7, no display-bright pulse is developed either. Therefore, the SD CRT's do not present any information during the reading of that first field.

The eighth step-fields-select-counter pulse received by the field counter develops an end-RD-start-TD pulse output. This pulse clears FF 2, goes to the TD-read-control circuit to start reading there, and goes to the SDGE to inform it that TD reading is about to begin. Thus, only eight of the nine RD fields are read during any one SD reading cycle. The ninth field is written by the Central Computer System during this time.

3.6.2 RD Field Switching, Circuit Analysis

When SD reading is first started, the power-on-reset pulse is sent through the TD-read-control circuit to the RD-step-scan synchronizer (fig. 3–16). In this circuit, which is part of the RD-read-control circuit, OR's 1 and 2 conduct, clearing FF's 1 and 2.

At any time thereafter, the Central Computer System indicates that it intends to write on a new RD field by sending a step-scan-counter pulse to the 1 side of FF 1. The step-scan-counter pulse establishes a 1 level at the output of FF 1 which passes a DTP 1 from the RD timing circuit.

The passed DTP 1 pulse sets FF 2 to the 1 side, forming a step-scan-counter level. This level goes to the read-sample-and-WOW-gate-and-intensity control to make certain that no data is displayed if the step-scan-counter pulses from the Central Computer System arrive during the reading of the first selected RD field (3.6.1).

The step-scan-counter level also conditions GT 2 to pass an OD 2 pulse, producing a scan-counter-step pulse. This pulse represents the step-scan-counter pulse synchronized with the operations of the Drum System.

The scan-counter-step pulse is applied to OR's 1 and 2 to clear FF's 1 and 2. Therefore, only one scan-counter-step pulse is produced by the scan counter synchronizer for each step-scan-counter pulse input.

The scan-counter-step pulse is also applied to the scan counter. The scan counter is a scale-of-9 counter, whose basic operation is similar to that of counters previously discussed. When the Central Computer System selects RD field 1 for writing, a reset-scan-counter pulse

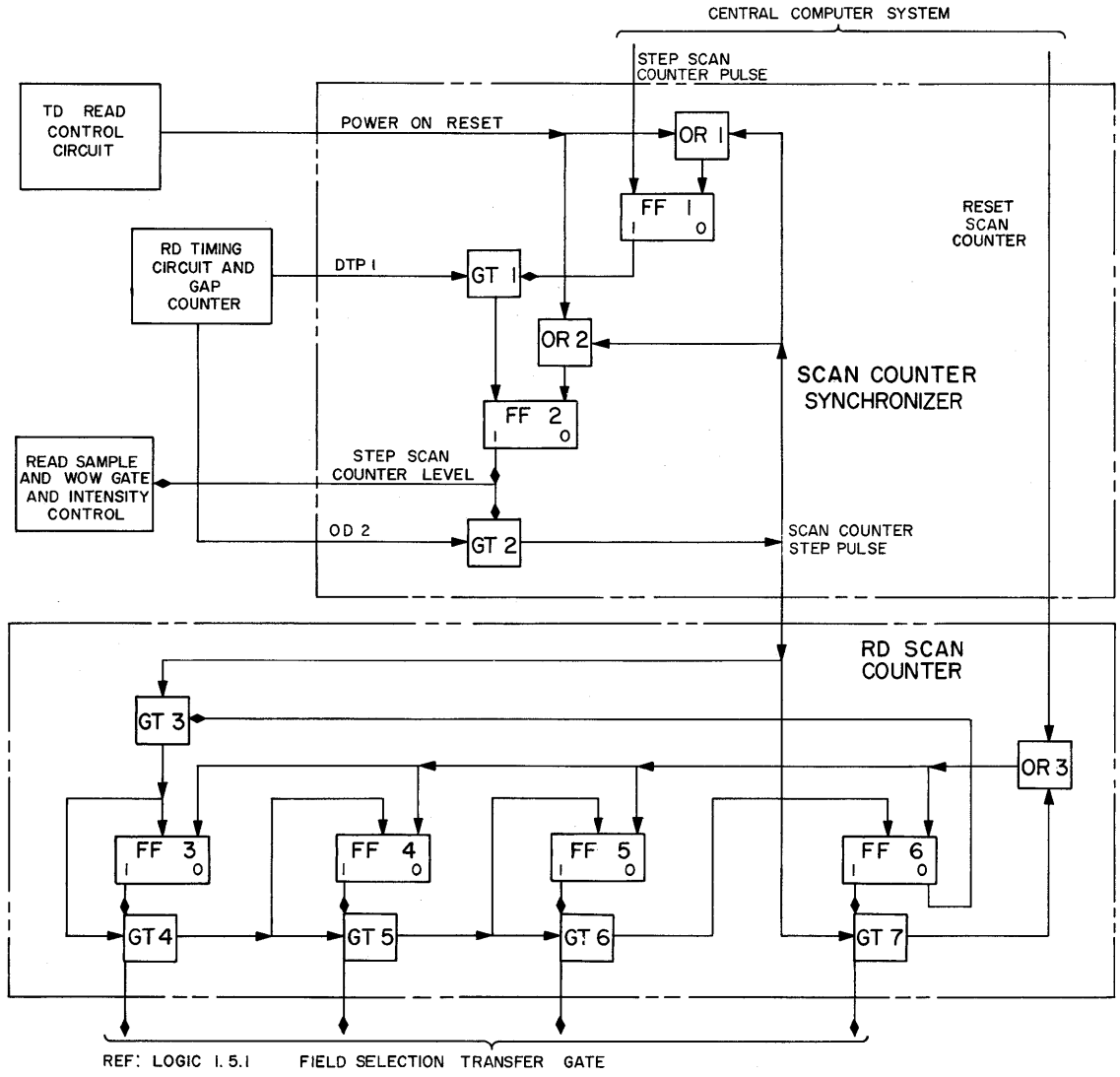


Figure 3–16. Radar Data Circuits for Selection of RD Field for OD Reading, Simplified Logic Diagram

is sent to the scan counter. In the scan counter, the reset-scan-counter pulse causes conduction in OR 3. Conduction in OR 3 clears all the scan-counter flip-flops. The output of FF 6 establishes a level at GT 3 which passes scan-counter-step pulses. Eight scan-counter-step pulses are counted in the normal fashion. The ninth scan-counter-step pulse is passed, not through GT 3, but through GT 7 by the 1-state level of FF 6 which is established by the eighth step pulse. The ninth pulse, when passed, goes to OR 3 and clears the counter. A cleared counter indicates that RD field 1 has once again been selected by the Central Computer System for a writing operation. The first scan-counter-step pulse counted represents field 2; the second, field 3; and so on. The d-c levels developed at the outputs of the flip-flops of the scan counter are sent to the transfer gates (fig. 3–17).

A reset-field-select-counter pulse produced in the RD read-pattern-development circuits during TD reading (3.4.1) sets FF 1 in the field selection counter (fig. 3–17) and clears the counter. The FF 1 output conditions GT 1 to pass a DTP 4 pulse. The timing pulse is a transfer-scan-counter pulse, which goes to GT's 3, 4, 5, and 6 of the transfer gate. Wherever a 1 level from the scan counter conditions one of these gates, a pulse is sent to an associated flip-flop in the field selection counter, setting it. Thus, the binary setting of the scan counter is transferred to the field selection counter in such a manner that the field selection counter indicates

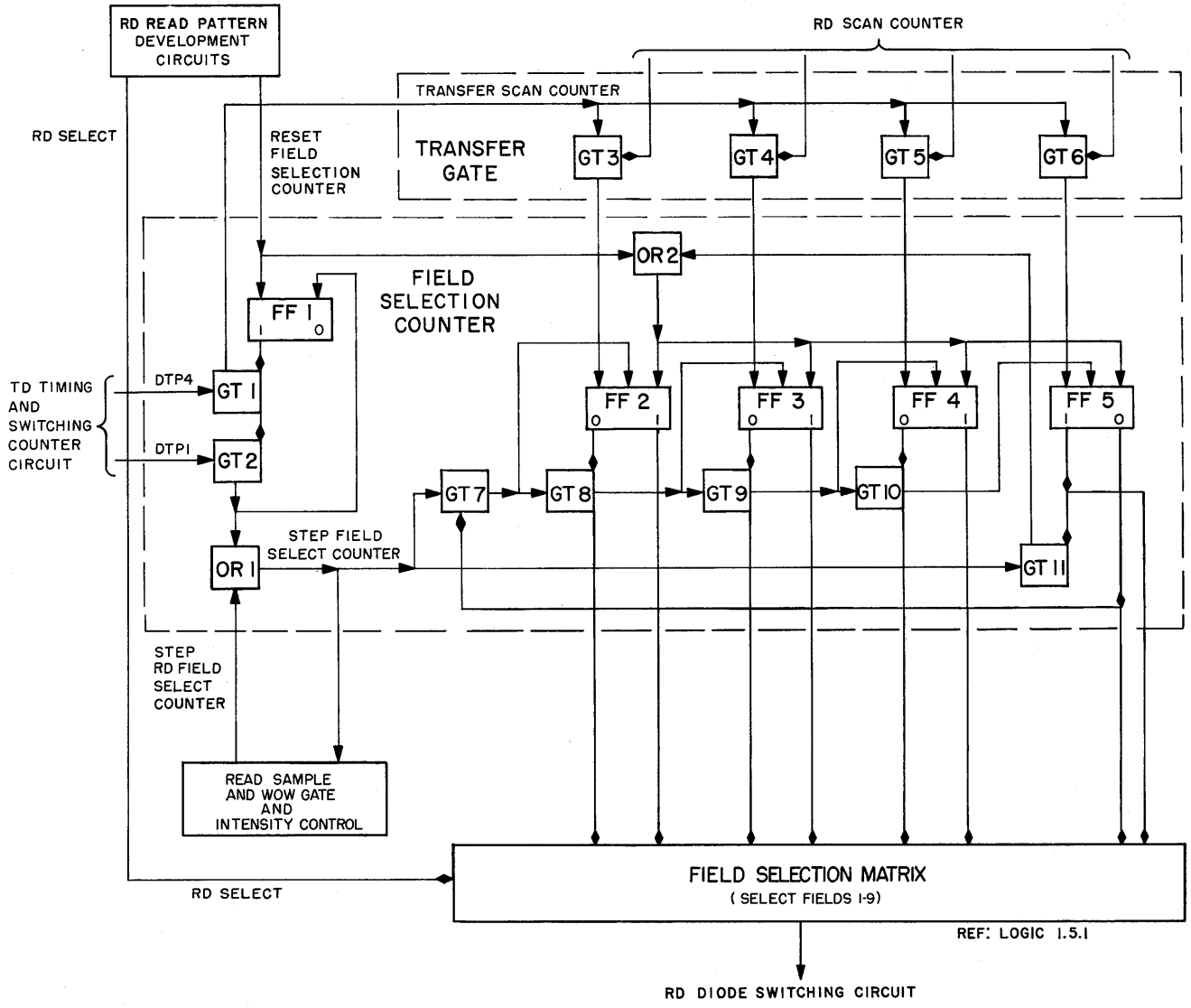


Figure 3—17. RD OD Field Selection Circuit, Simplified Logic Diagram

the field upon which the Central Computer System will write.

The level from FF 1 also conditions GT 2 to pass the first DTP 4. This DTP 1 clears FF 1, preventing further production of transfer-scan-counter pulses, and goes to OR 1. OR 1 conducts, developing a single step-selection-counter pulse for the field selection counter. As a result, the counter assumes a setting that represents a number that is 1 greater than the setting of the scan counter.

The field selection counter operates in a manner similar to that of the scan counter. After the initial setting of the field-switching counter by the transfer gate output and the DTP 1 step pulse, the counter is stepped by the output of the read-sample-and-WOW-gate-and-intensity control. Each time this control indicates the completion of the reading of a field, it sends a step-field-selection-counter pulse to OR 1 in the field selection counter. The output of OR 1, thereafter, steps the field-switching counter each time the reading of a field is completed.

The output of the field-selection-counter levels goes to the RD field selection matrix. This matrix operates in the same manner as the TD field selection matrix (3.4.2) except that levels are available for nine fields instead of six as in the latter matrix.

In order for any of the AND circuits of the field selection matrix to conduct, an RD-select level from the read-pattern circuits must be present. This signal indicates that the RD drum has been selected for SD reading. The output of the field selection matrix goes to the RD-diode-switching circuit. This circuit is identical in its

operation with the TD-diode-switching circuits, except that the d-c select field levels produce conduction in 24 read heads instead of in 33 (fig. 3–12).

As shown in figure 3–12, the RD field switch output supplies an alternate input to the SD drum switch, which in turn feeds the SD read circuit. The read-sample pulses produced by the read-pattern-development circuits described in 3.6.1 pass the selected RD field contents to the SDGE.

3.7 SITUATION DISPLAY TIMING PULSE SWITCH, CIRCUIT ANALYSIS

The SD timing pulse switch (fig. 3–18) of the OD display circuits is employed to alternately switch RD and TD timing, index, and WOW pulses to the SDGE.

The drum timing pulses from the TD timing circuit go to OR 1. The drum timing pulses from the RD timing circuit go to OR 2. OR's 1 and 2 conduct each time they receive one of the four drum timing pulses. The outputs of OR's 1 and 2 go to GT's 1 and 2, respectively. The drum (RD or TD) being read at a given time has a select level generated in its read-control circuit. This select level goes to the gate pulsed by the drum timing pulses of the selected drum. For example, if the TD drum is being read, the TD-select level goes from the TD-read-control circuit to GT 1.

The gate conditioned by a select level passes the drum-timing-pulse inputs to OR 3. The OR 3 outputs are thereafter referred to as SD-drum-timing pulses and are sent to the SDGE.

Each select-drum level (when present) conditions a gate which is pulsed by the index pulses of the associated timing circuit. Thus the TD-select level is established at GT 3 during TD reading and the RD-select level at GT 4 during RD reading. The index pulses go to OR 4. The OR 4 outputs are referred to as SD-index pulses and go to the SDGE.

The drum being read at any given time produces a WOW pulse before sending a word into the SDGE. The

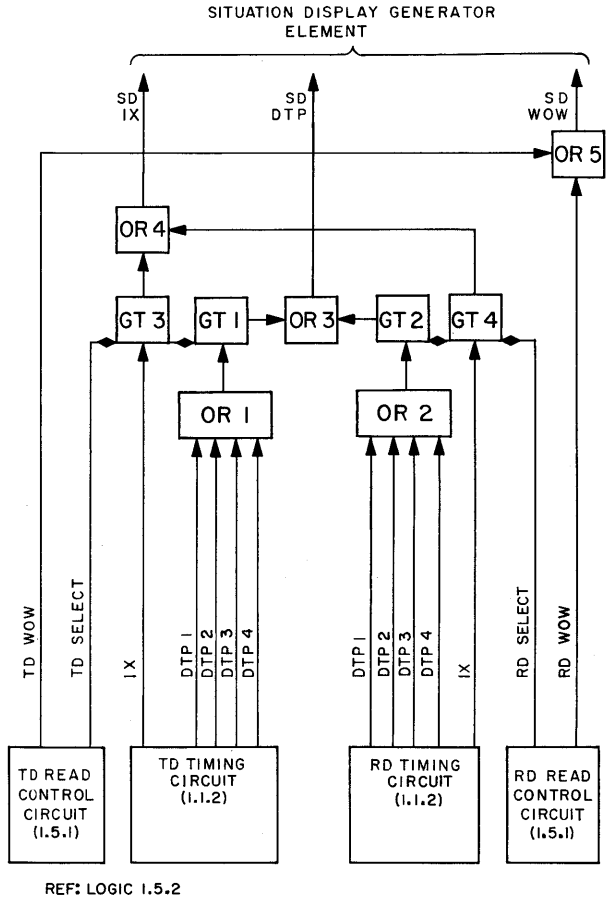


Figure 3–18. SD Timing Pulse Switch, Simplified Logic Diagram

TD or RD-WOW pulse, whichever is present, produces conduction in OR 5. The OR 5 output is referred to as an SD-WOW pulse and goes to the generator element.

The SD-timing-and-index pulses are used to time the operation of the generator element, and the WOW pulses prepare it to receive the words read from both drums.

CHAPTER 4
INTERCOMMUNICATION FIELD

Intercommunication between duplex areas A and B of the equipment enables the alternate standby area to keep abreast of the tactical developments and equipment performance in the active area. The two areas are related by means of data written by the active Central Computer System on the active Drum System IC field. This data is transferred to the standby Central Computer System under control of the standby Drum System.

Intercommunication field data transfers are accomplished as shown in figure 3–19. The active Central Computer System (assume either one) generates the data which is to be written by address control on the CD side of the associated IC field, IC Own. The data is written on the field by the active Drum System CD data transfer control circuits. The data is read on the OD side, IC OTHER, by the active Drum System OD field operating circuits under the control of the alternate area Drum System. The IC data read is then transferred to the standby Central Computer System via a bus line and the CD circuits of the standby Drum System.

Because of the addressable nature of the IC field, each Central Computer System may write and read on the CD side of the associated IC field. The OD reading operation, however, must be initiated by the alternate Central Computer System. Once this is done, the alternate Drum System assumes control of the operation.

4.1 IC FIELD CD WRITING

The CD circuits in the active Drum System transfer IC data from the active Central Computer System to the active IC field by address control. (Refer to Ch 7 of Part 2.) The use of address control in CD writing on the active IC field enables the standby Central Computer System to know exactly where pertinent data has been placed. This ensures the transfer of correct data from the active to the standby Central Computer System.

4.2 IC FIELD OD READING, BLOCK DIAGRAM ANALYSIS

Reading of the IC field in Drum System A is performed under the direction of Central Computer System B and Drum System B. Figure 3–20 is a block diagram of this reading operation.

A deselect pulse is sent by Central Computer System B to the CD-read-write-control circuit in Drum System B. Central Computer System B sends auxiliary bits to Drum System B field selection circuits, where they are decoded to produce the IC-other-select level. The CD-read-write-control circuit, in turn, sends a read-write-reset pulse to the IC-read-control circuit in Drum System B. The read-write-reset pulse and the IC-other-select level prepare the IC-read-control circuit to receive the start-read-other-IC pulse from Central Computer System B via the B Drum System CD-read-write-control circuit.

The start-read-other-IC pulse causes the B system IC-OD-read-control circuit to produce an APC-readout pulse. The APC-readout pulse gates the contents of the IC APC to the CD-read-output circuit (Drum System B), from which it goes to Central Computer System B. This information represents an address on the IC field of the A system MIXD drum. The contents of the IC APC are determined by the number of step-APC pulses received from the IC-read-control circuit, after the index pulse from the A system IC OD timing circuit has cleared the counter. The step-APC pulses are actually MIXD OD 1 pulses from the A system MIXD drum that pass through the B system read-control circuit. The APC circuit output is sent to the B system CD-read-output circuit. At the same time, the B system IC-read-control circuit sends an IC-compare pulse to Central Computer System B via the CD-read-write-control circuit in Drum System B.

The IC-compare pulse from the B system IC-read-control circuit causes Central Computer System B to compare the APC contents from Drum System A with 11 bits in the Central Computer System B comparison circuits. The comparison circuit bits represent the desired address on the drum in Drum System A. Until comparison is successful, Central Computer System B sends no-compare pulses back to the B system IC-read-control circuit.

When the no-compare pulse is not returned, IC-read-sample pulses are developed by the B system IC-read-control circuit. The read-sample pulses go to the A system IC OD read circuit, where they gate the IC word on the A system MIXD drum to the CD-read-output circuit of Drum System B. The IC-read-sample pulses continue to be developed until Central Computer System B produces a disconnect pulse, which enters the IC-read-control circuit as a read-write-reset pulse.

With each word read into Central Computer System B in this manner, the IC-read-control circuit sends

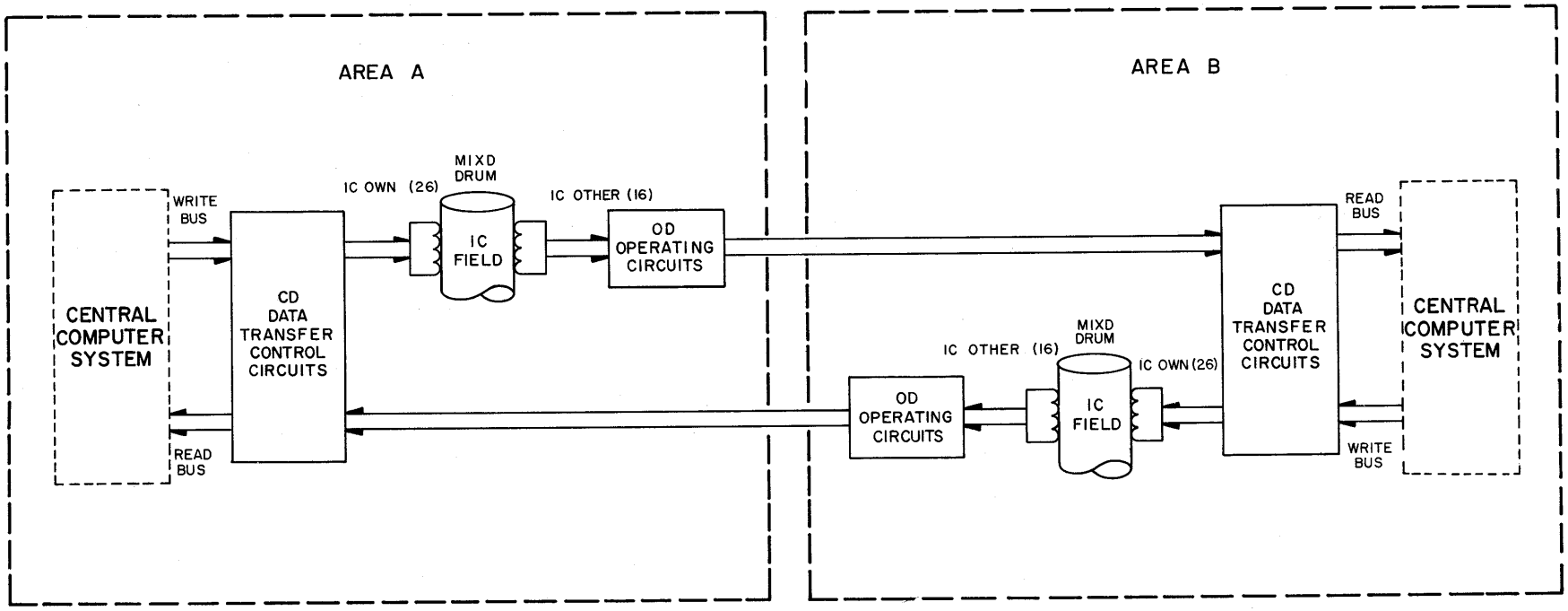


Figure 3–19. Intercommunication Field, Block Diagram

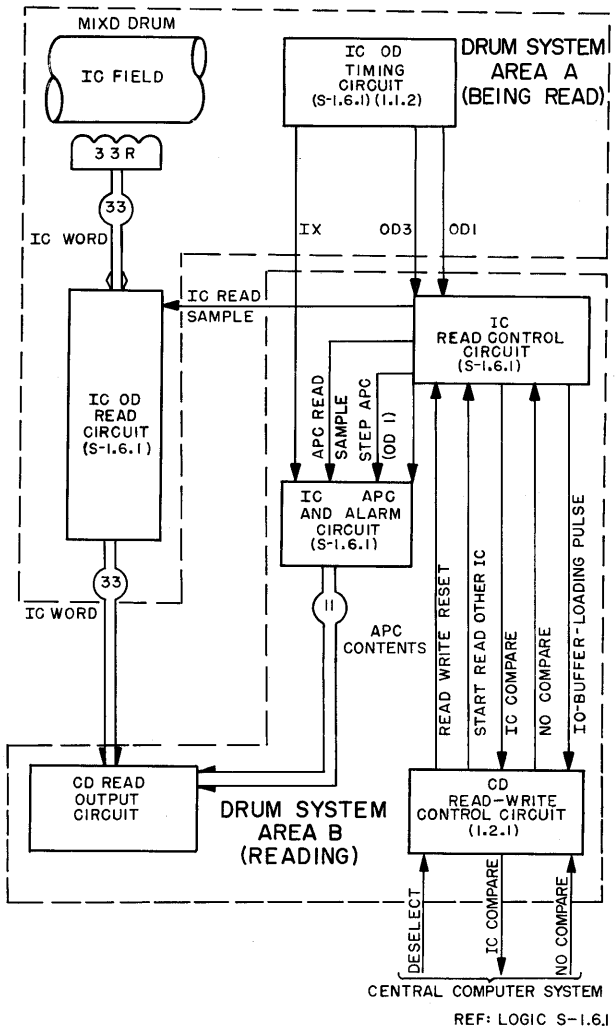


Figure 3–20. Intercommunication — OD Circuits, Block Diagram

an IO-buffer-loading pulse to the B system CD-read-write-control circuit for transfer to Central Computer System B. Central Computer System B counts the IO-buffer-loading pulses to determine when it has received the desired number of words. Timing and index pulses from Drum System A are used by the B system IC-read-control circuit to time and control reading operations. The IC-OD-index pulse is used in IC field reading only. The OD 1 and OD 3 pulses are standard pulses generated by the A system MIXD timing circuits.

4.3 IC OD TIMING CIRCUIT, FUNCTIONAL DESCRIPTION

Timing pulses from the MIXD drum of the active Drum System are used in the transfer of data from the active to the standby Drum System. Drum timing pulses are transmitted from the A system drum being read to the IC and the IC-APC control of Drum System B doing the reading (fig. 3–21). The read-sample pulse is generated in the IC read controls of Drum System B.

The timing pulses from Drum System A used in Drum System B in the transfer of IC data are the OD 1 and OD 3 pulses derived from the MIXD drum timing circuits, and an OD-index pulse generated for use with the IC field by the IC OD timing circuit (fig. 3–21). The OD-index pulse for the IC field is derived from an additional read head mounted on the index channel of the MIXD drum. The read head is energized by the 1 bit in the index channel and causes the drum read amplifier to produce a wide pulse at GT 1 that coincides with the OD 3 timing pulse from the MIXD timing circuit. The wide pulse, therefore, acts as a conditioning level and produces the OD-index pulse at OD 3 time.

In Drum System B, the index pulse clears the IC-APC-and-alarm circuit. The OD 1 and OD 3 timing pulses go to the IC-read-control circuits and the IC-APC-and-alarm circuit. The uses of both OD 1 and OD 3 pulses in the IC read control and IC read circuit are discussed in 4.4.

4.4 IC OD READING CIRCUITS, FUNCTIONAL DESCRIPTION

4.4.1 IC-OD-Read-Control Circuit

The OD reading of the IC field in Central Computer System A is performed under the control of Central Computer System B. The CD-read-write-control circuit in Drum System B sends a read-write-reset pulse to the B system IC-read-control circuit (fig. 3–22).

The read-write-reset pulse causes conduction in OR's 1, 2, and 3, clearing FF's 1, 2, and 3. Clearing the IC-read-control circuit flip-flops prepares the circuits

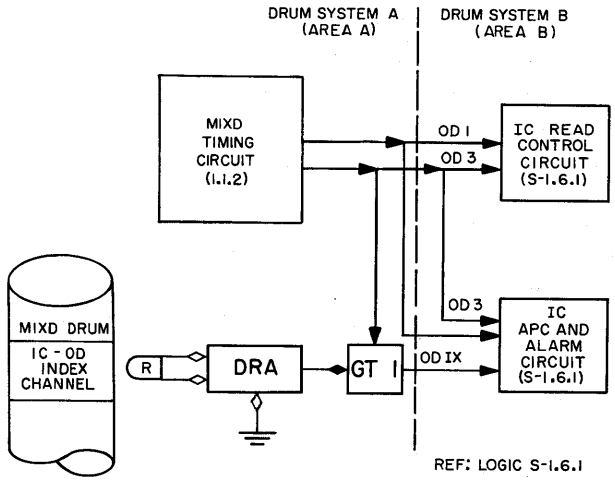


Figure 3–21. Intercommunication — OD Timing Circuit, Simplified Logic Diagram

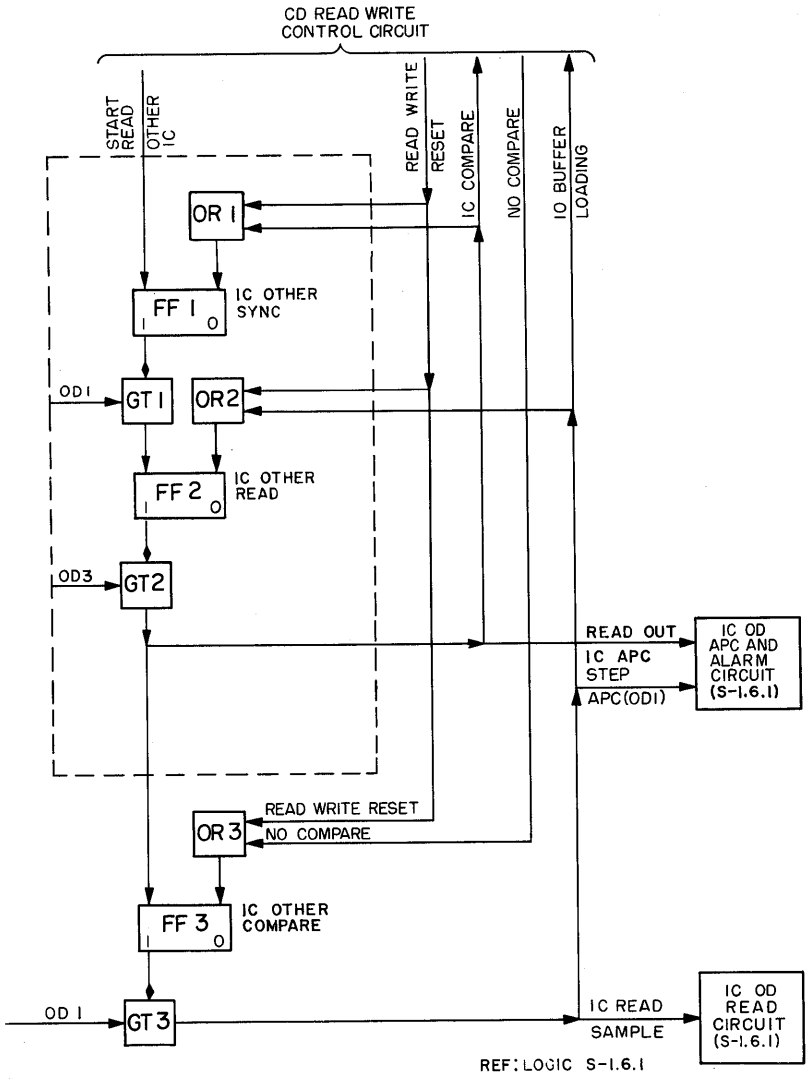


Figure 3—22. Intercommunication-Read-Control Circuit, Simplified Logic Diagram

to receive a programmed start-read-other-IC pulse from the CD-read-write control circuit of Drum System B.

The start-read-other-IC pulse sets FF 1 in the B system IC-read-control circuit. The 1-state output of FF 1 conditions GT 1 to pass an OD 1 pulse from the MIXD timing-circuit of Drum System A, synchronizing the instruction pulse from the B system with the timing cycle of the A system. The gated OD 1 pulse sets FF 2, and the resulting FF 2 output conditions GT 2 to pass an OD 3 pulse from the MIXD timing circuit of Drum System A.

The GT 2 output goes to the CD-read-write-control circuit of Drum System B as an IC-compare pulse and to the IC-APC-and-alarm circuit (4.4.2) as an APC-readout pulse.

The IC-compare pulse and the counter setting of the IC-APC-and-alarm circuit are sent to Central Computer System B. The counter setting is compared with a programmed address in the circuits of Central Computer System B. If the two addresses do not compare, Central Computer System B sends a no-compare pulse to the CD-read-write control of Drum System B within 1.1 usec. The CD-read-write-control circuit of system B immediately transfers the no-compare pulse to the IC-read-control circuit. The no-compare pulse produces conduction in OR 3, clearing FF 3.

Conversely, if the comparison is successful, the no-compare pulse is not developed and FF 3 remains in the 1 state, where it has been placed by the output of GT 2. With FF 3 in the 1 condition, GT 3 is still conditioned when the next OD 1 pulse arrives. The GT 3 output pulse goes to the A system IC OD read circuit as an IC-read-sample pulse and to the CD-read-write-control circuit of Drum System B as an IO-buffer-loading pulse.

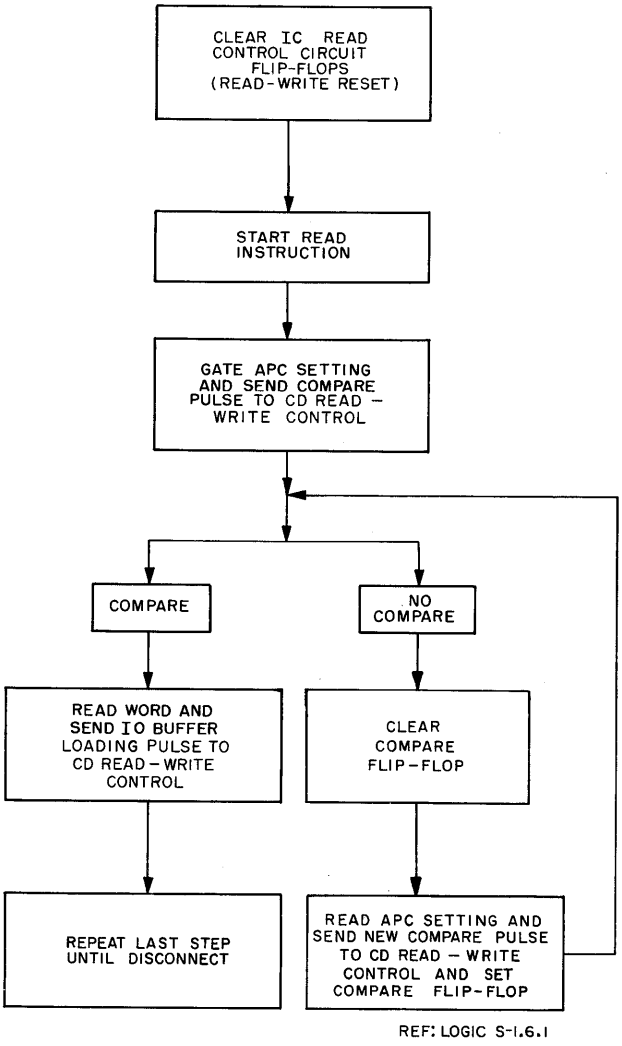


Figure 3–23. Sequence of IC Field Reading Operations

The IO-buffer-loading pulse also clears FF 2 in the IC-read-control circuit by producing conduction in OR 2. With FF 2 cleared, no further GT 2 outputs can be produced until the next start-read-other-IC pulse is received from the CD-read-write-control circuit of Drum System B.

The IO-buffer-loading pulses are transferred to Central Computer System B by the CD-read-write-control circuit of Drum System B to be counted. Counting the IO-buffer-loading pulses enables Central Computer System B to determine the number of IC-read-sample pulses and, therefore, the number of words transferred by the A system IC OD circuit. When the number of words received represents the total number of words specified by the Central Computer System B program, a read-write-reset pulse is produced which stops the IC OD reading operation by clearing FF 3.

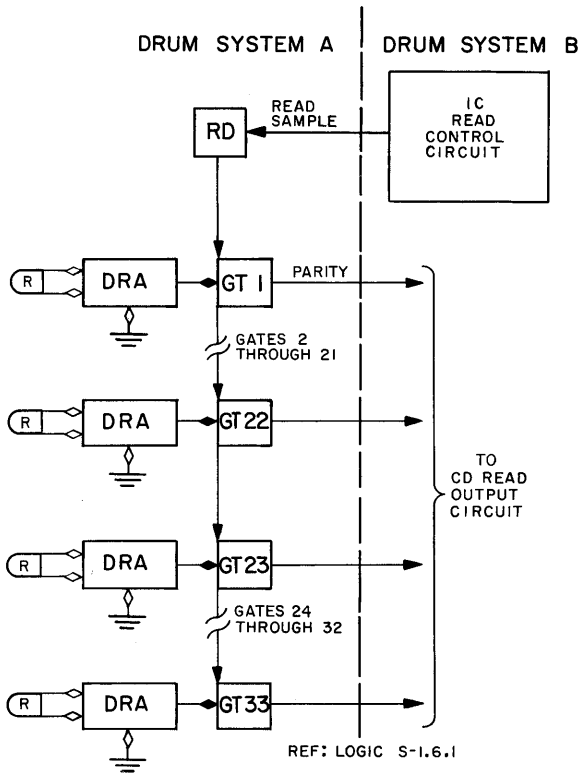


Figure 3–24. Intercommunication – OD-Read Circuit, Simplified Logic Diagram

Figure 3–23 is a chart that summarizes the sequence of events in the OD reading of the IC field.

4.4.2 IC-Angular-Position-Counter-and-Alarm Circuit

The IC-APC-and-alarm circuit is similar to the other APC-and-alarm circuits used in the Drum System. The only difference is that the IC APC is stepped by OD 1 pulses and the APC check flip-flop is set by OD 3 pulses. The operation of a typical APC-and-alarm circuit is discussed in detail in 7.4.2 of Part 2.

4.4.3 IC OD Read Circuit

The IC-read-sample pulses from the B system IC-read-control circuit are amplified by the register driver and applied to GT's 1 through 33 of the IC OD read circuit in Drum System A (fig. 3–24). Each gate is connected to a read head via a drum read amplifier. If a head reads a 1 bit on the drum surface, the drum read amplifier detects it and applies it to the gate to which it is connected as a conditioning level. When the read-sample pulse is received at gates that are so conditioned, a pulse is sent to the CD-read-output circuit in Drum System B. The outputs of the 33 gates then represent the word that has been on the drum. The absence of a pulse output from any of the gates indicates the 0 bits in that word. The CD-read-output circuit of Drum System B transfers the words received in this manner into Central Computer System B.

PART 4
STATUS FIELDS

CHAPTER 1
INTRODUCTION

The Drum System contains eight field-operate circuits, merely designated as status fields since they transfer data by the status method. The individual designation and distribution of these fields is as follows: the MI and XTL fields are contained in the MIXD drum, and the LRI 1, LRI 2, OB 1, OB 2, OB 3, and GFI fields are contained in the LOG drum.

The MI, XTL, LRI, and GFI fields (Ch. 2) transfer data from the Input System to the Central Computer System. The three OB fields (Ch. 3), although employing the status method, carry data from the Central Computer System to the Output System.

The operation of the typical status control circuit described in 7.7 of Part 2 is essentially followed by each of the eight status fields. However, the nature of data carried by LRI, XTL, and OB fields demands special modifications to the typical status control operation. These modifications allow two consecutive data transfers to accommodate the 2-word LRI messages, and three consecutive data transfers to accommodate the 3-word XTL messages. Modifications required by the OB fields are related to two available field selections (SDR OB ODD 30 and SDR OB EVEN 31) which initiate storage on the three OB drum fields.

Other status fields, namely, MI and GFI, require modifications to a lesser degree to accommodate needs which are peculiar to the type of data carried by these fields.

CHAPTER 2
INPUT STATUS FIELDS

2.1 GENERAL

The Input System of the AN/FSQ-7 receives large quantities of input data for transfer to the Central Computer System. This input information is received at different repetition rates and at random intervals. The Drum System stores this data for later transfer to the Central Computer System. The transfer from the Drum System to the Central Computer System is performed on Central Computer System command.

The drum fields on which information is written are named according to the source of their information. Manual input data is written on the MI field, XTL input data is written on the XTL field, etc. The LRI input differs from the other inputs in that it utilizes two drum fields instead of one. These fields are designated LRI 1 and LRI 2. The GFI data utilizes only one drum field.

To regulate the placement of input data on the drum fields, each field is provided with two control channels in addition to the channels assigned to store information words. These two channels are named the OD status channel and the CD status channel. The OD status channel indicates to the OD circuits of the field the availability of the individual registers as storage space for incoming words. The CD status channel indicates to the CD circuits of the field the presence of a word in a register, so that it may be transferred to the Central Computer System when requested.

An OD status control circuit associated with each of the input fields reads the contents of the OD status channel. When storage space is found, the OD status control circuit notifies the Input System that such storage space is available. The Input System examines its own circuits to find a word or words (called a message) that can be written in the space available. If a word is found in the Input System, it is transferred to the OD write circuit of that field. The Input System notifies the OD status control circuit that a word is being sent. The status control circuit causes the OD write circuit to write the transferred word on the drum. The status control circuit also writes in the CD status channel to indicate that a word is being written in that register.

If the register space is available but the Input System has no data for transfer at that time, the status control circuit writes in the CD status channel to indicate that the register remains empty. If the reading of the OD status channel for any given register does not reveal an empty storage space, the status control circuit doing the reading writes in the CD status channel. This indicates to the CD element that a word is still present in that register.

In addition to the OD and CD status channels, a third channel, known as the marker status channel, is provided for the XTL fields. The marker status channel contains markers written by the Central Computer System via the CD circuits. A marker is a 1 bit that is written in the marker channel. If there is to be no marker, a 0 bit is written in the marker channel. Each marker in this channel indicates to the XTL OD input circuit the register in which the wiring of a multiword message should begin. The wiring operation performed under the control of marker status circuits is slightly different from the writing by status-controlled circuits. Writing of a message can begin only in a register which is both empty and marked as the first register of a slot. The remaining word in the input data message may then be written in consecutive registers without the need for examining the status of the registers.

During the writing of GFI words, the GFI OD input circuits write relative time information as part of the GFI word. The relative-time-counter-step circuit receives time indications in the form of pulses from the Central Computer System and synchronizes these pulses with the drum timing pulse operating cycle. The synchronized pulses are used to step the relative time counter. Synchronization is necessary to prevent writing while the contents of the relative time counter are changing.

The operations of the MI and XTL fields, which are on the MIXD drum, are timed by the MIXD drum timing circuit. Timing data from this circuit is also sent to the Input System circuits associated with these fields.

The LRI fields and the GFI field are contained on the LOG drum. Their operations are timed by the LOG drum timing circuit. Timing data from the LOG timing circuit is also sent to the Input System circuits associated with those fields.

Manual input and GFI data are received in the form of 1-word (33-bit) messages. The LRI messages consist of two words; XTL messages, three words. The words of the LRI and XTL messages are written on consecutive registers of the respective fields.

The transfer of input data to the Central Computer from any input field is initiated by instruction pulses from the Central Computer and controlled by status channel CD circuits associated with each input field. These circuits operate similarly to the status channel OD circuits described above. In the case of CD transfer, however, the information read from a drum register must be accepted by the Central Computer before that register is made available for further information.

2.2 MANUAL INPUT FIELD

Manual input data is originated in the Input System and transferred to the Drum System, where it is stored on the MIXD drum MI field. The MI field (logic 1.3.1) is the basic status field and is almost identical in operation with the typical circuit discussed in 7.7.1 of Part 2. The only difference between the typical circuit and the MI field circuits lies in the manner in which compare pulses are generated.

See figure 2—43. Notice the status-field-select level from the selection circuits. This level corresponds to the SEL MI 22 or SEL MI 23 CD field selections (5.3.2 of Part 2) and, in conjunction with the read level from read-write control, is applied to an AND circuit. The AND circuit output conditions GT 10 to pass CD 1 pulses. In the MI-field-CD-status-control circuit, the GT 10 output is sent to the CD-slot-read-control circuit (2.9) rather than directly to the Central Computer. The CD-slot read-control circuit, in turn, produces the compare pulse and sends it to the Central Computer.

2.3 GFI OD TRANSFER, CIRCUIT ANALYSIS

In the performance of certain Central Computer System functions, it is necessary to indicate the relative times at which separate portions of the data are received; for example, one computation that requires data-timing is the determination of target velocity. Because velocity is defined as the distance moved in a given period of time, it is necessary to know the time elapsed between different target-location samplings. Placing time information in each GFI word makes it possible to compute the time difference between the receipt of any two of these words. Timing data is written into bits L10 through L14 of the GFI word at the time the word is transferred onto the drum; therefore, the addition of timing data will be considered in conjunction with the data transfer process.

A block diagram of the OD circuits used to place data-timing information in words written onto the GFI field is shown in figure 4—1.

The clock register in the Central Computer System develops relative-time-counter pulses and sync-relative-time-counter pulses, which go to the relative-time-counter-step circuit. In the relative-time-counter-step circuit, these two series of pulses are synchronized with

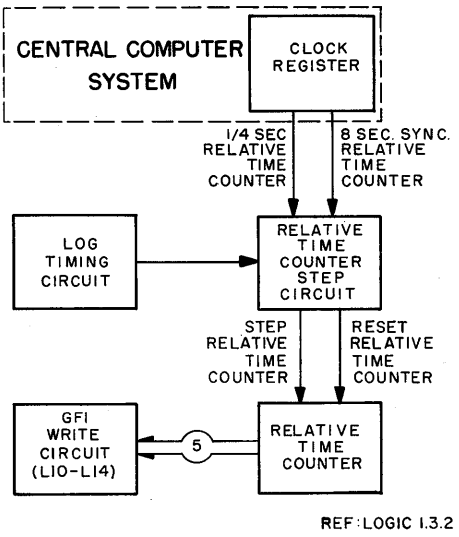


Figure 4—1. Gap-Filler Input Data Timing, Block Diagram

OD 4 pulses from the LOG timing circuit to produce step-relative-time-counter pulses and reset-relative-time-counter pulses, also at OD 4 time.

The two outputs of the relative-time-counter-step circuit go to the relative counter. Each relative-time-counter-step pulse steps the counter. The output of the counter, therefore, represents the number of relative-time-counter-step pulses that have been counted. This output is sent to the OD write circuit of the GFI field, filling bits L10 through L14.

Since the maximum output of the counter, 31, can be expressed in five bits, the largest number of step pulses that can be counted is the binary number which is represented by all the five flip-flops being in the 1 state. Once every 8 seconds, at the time which would correspond to the 32nd step pulse, the reset-relative-time-counter pulse is developed. This pulse clears the counter flip-flops. If all the counter flip-flops are not set at the time the reset-relative-time-counter pulse is received, an error indication is developed.

In the production of timing data for the GFI field, the clock register of the Central Computer System develops two sets of timing pulses. One set consists of relative-time-counter pulses with a 1/4-second recurrence rate. The other set, known as the sync-relative-time-counter pulses, occurs once every 8 seconds. Both types go to the GFI relative-time-counter-step circuit (fig. 4—2).

The relative-time-counter pulses set FF 1. The output level of FF 1 conditions GT 1 to pass OD 1 pulses from the LOG timing circuit. The gate output sets FF 2. The resulting d-c level at the output of FF 2 provides

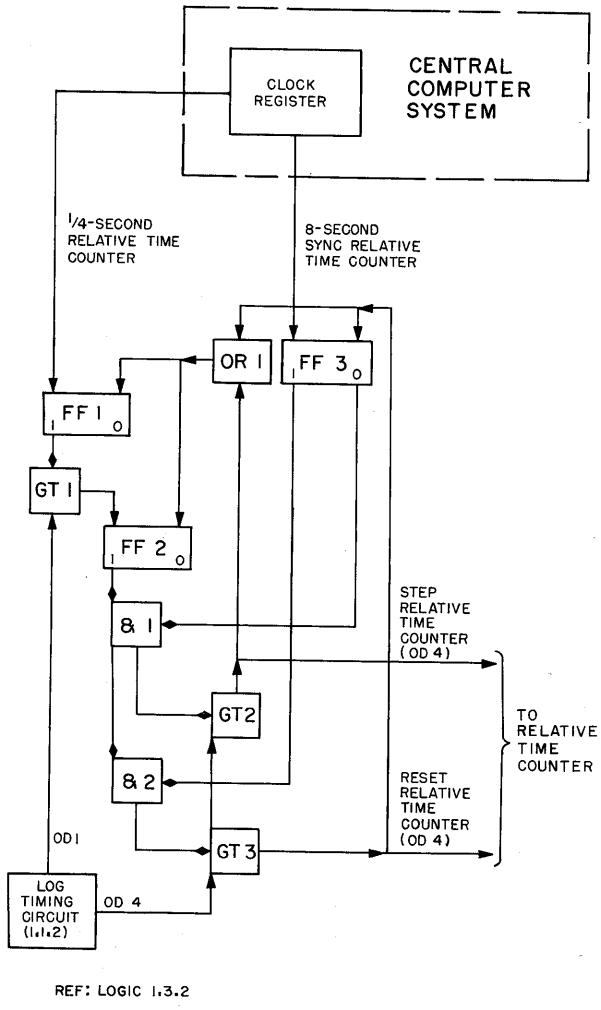


Figure 4–2. Relative Time Counter Step Circuit, Simplified Logic Diagram

one of two levels necessary to produce conduction in AND's 1 and 2.

Assuming that FF 3 is in the 0 state, AND 1 conducts, conditioning GT 2 to pass OD 4 pulses. The gated OD 4 pulses form step-relative-time-counter pulses which go to the relative time counter and OR 1. Conduction in OR 1 clears FF's 1 and 2.

At the end of 8 seconds, the sync-relative-time-counter pulse is sent to the relative-time-counter-step circuit at the same time as the relative-time-counter pulse. As before, the relative-time-counter pulse establishes a d-c level in AND's 1 and 2. However, the sync-relative-time-counter pulse sets FF 3. AND 2 conducts while AND 1 cannot conduct. Gate 3 is conditioned to pass an OD 4 pulse, forming a reset-relative-time pulse. Since AND 1 does not conduct, GT 2 is not conditioned and the 32nd consecutive step-relative-time-counter pulse is not generated. The reset-relative-time-counter pulse goes to the relative time counter and to OR 1 and clears FF 3. Conduction in OR 1 again clears FF's 1 and 2.

The relative-time-counter-step circuit, therefore, produces 31 step-relative-time-counter pulses, then one reset-relative-time-counter pulse, then another 31 step pulses, etc.

The relative time counter (fig. 4–3) counts the step-relative-time-counter pulses. It is cleared by the reset-relative-time-counter pulse. The FF 1 output (1 or 0 d-c level) represents the lowest order digit of a binary number, etc. The complete number of step pulses counted is 31. Refer to 7.4.2 of Part 2 for a discussion of counter circuit operation.

The reset-relative-time-counter pulse serves as a check on the counter. If an error in counting occurred, one or more of the counter flip-flops will provide a 0 output at the time of the reset-relative-time-counter pulse. The 0 output of the flip-flop(s) causes conduction in OR 1, which conditions GT 5 to pass the reset-relative-time-counter pulse as a relative-time-error pulse. The relative-time-error pulse causes an error indication at the maintenance panel.

The flip-flops of the relative time counter form a part of the GFI write register. The d-c levels at the output of the counter go to the GFI OD drum writers. Each time the gap-filler status control circuit develops a write-sample pulse (7.7.1.1 of Part 2), the output of the relative time counter is written on the drum as part of the GFI word.

With the exception of the addition of data-timing information, the GFI field is written in the same way as the typical status field discussed in 7.7.1 of Part 2.

2.4 GFI CD TRANSFER

Transfer of GFI data from the drums to the Central Computer is performed in the same manner for the GFI field as for the MI field (2.2).

2.5 LRI OD TRANSFER, CIRCUIT ANALYSIS

An LRI message consists of two words. By a modification of the basic method of status data, OD transfer, an LRI message is written onto two consecutive registers, with the first word of each message written in an even-numbered register. The two registers which contain one complete message are read consecutively on the CD side of the drum. The group of two registers which contain the message is termed a slot.

Figure 4–4 illustrates a part of the circuits which control the writing of LRI messages. The word-demand pulse is an OD 3 pulse which is passed by GT 2 when FF 1 has been cleared by an OD 4 pulse and not set by the OD 1 pulse. This condition will exist when a 0 is read in the OD status channel.

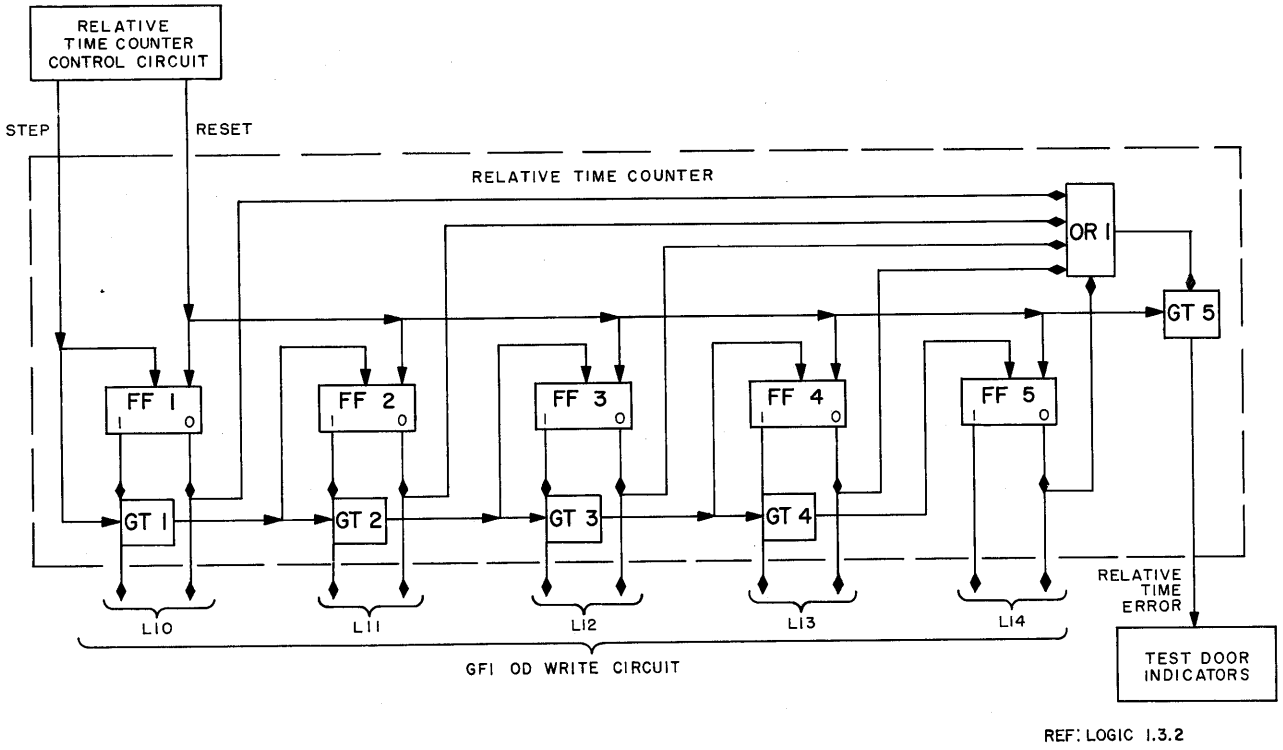


Figure 4–3. Relative Time Counter, Simplified Logic Diagram

Gate 3, which must be conditioned to pass the OD 3 or word-demand pulse, is controlled by the LRI slot counter, FF 2. AND 1 conducts when the Drum System is in the operate mode and when FF 2 is in the 1 state. The LRI slot counter flip-flop (FF 2) is complemented by each OD 1 pulse. Therefore, GT 3 will alternate between the conditions of conduction and nonconduction and will remain in each condition for a period of 10 usec. Gate 3 will consequently block OD 3 pulses during alternate registers. Hence the LRI status control circuit generates a word-demand pulse for each two consecutive vacant registers rather than for each vacant register, as is done in basic-status control.

Once each drum revolution, the LRI slot counter is triggered by the LOG-OD-IX pulse to ensure that it is in the correct position to place the first word of each subsequent message in an even-numbered register.

If the Input System contains an LRI message, its response to the LRI word-demand pulse is two data-available pulses, the second separated from the first by 10 usec. The two data-available pulses cause the message to be written on two adjacent registers and cause the complete message to be written in response to one word-demand pulse.

The two deviations from basic-status control necessary to write the LRI fields involve the generation of a word-demand pulse at every other OD 3 time (when the OD status channel indicates a slot available) and the Input System response of two data-available pulses.

LRI data is written in two fields, LRI 1 and LRI 2. The LRI slot counter is common to both fields, but GT 3 and the power amplifier are duplicated in the status control circuits of the two fields. Hence, the two word-demand pulses occur simultaneously if both fields indicate an available slot. In this event, the Input System transfers the message of LRI field 1.

2.6 LRI CD TRANSFER, CIRCUIT ANALYSIS

LRI messages consist of two words written into consecutive registers, called slots. The first word of each message is written in an even-numbered register; consequently, the LRI CD status control circuits are modified slightly from the basic CD status control circuits (7.7.1.2 of Part 2). Two single-stage counters, the LRI CD slot counter and the LRI status slot counter, constitute the modifications. The LRI CD slot counter serves to ensure that the reading of each LRI slot (two consecutive registers) is begun on even-numbered registers. The LRI status slot counter establishes the register (the first even register after arrival of the read-by-status level) at which stepping of the CD-read-status-disconnect counter begins. This stepping is necessary to prevent development of the status-read-disconnect pulse until the entire

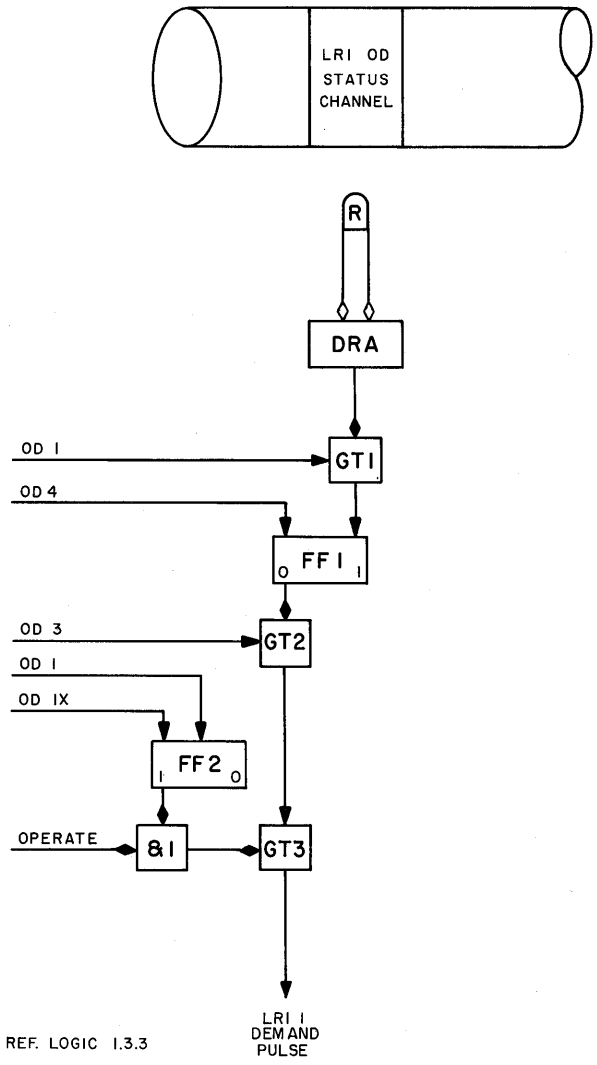


Figure 4–4. LRI OD Slot Counter, Simplified Logic Diagram

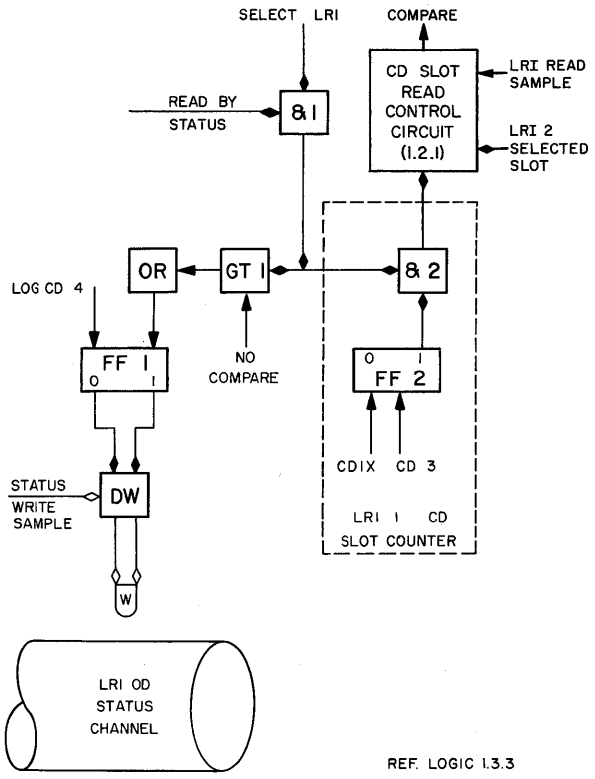


Figure 4–5. LRI CD Slot Counter and Associated Circuits, Simplified Logic Diagram

field (2,048 registers) has been read. Counting begins with register zero.

Because of the action of the LRI CD slot counter (fig. 4–5), LRI CD data transfers are initiated on even-numbered registers. This counter prevents generation of compare pulses during the reading of odd-numbered registers. The LRI CD slot counter flip-flop (FF 2) controls conduction in AND 2, provided AND 1 conducts. AND 1 conducts when the read-by-status and select-LRI levels are present. Flip-flop 2 is cleared by the CD-IX pulse (register zero CD 1 time). Five usec later, the register-zero CD 3 pulse complements FF 2, thereby providing a +10V level at AND 2. Consequently, the AND 2 output is a +10V level which is sent to the CD-read-slot-control circuit (2.9). This circuit produces an LRI-field-compare pulse only when a negative level is present at its input. Therefore, the next read-sample pulse (these pulses are gated to produce compare pulses) at register 1 CD 1 time is blocked and a compare pulse is not generated. The register 1 CD 3 pulse, however, complements FF 2, thus replacing the +10V level at AND 2 with a −30V level. The AND 2 output becomes negative and is applied to the CD-read-slot-control circuit. This action allows the register 2 CD 1 pulse to be passed by the CD-read-slot-control circuit and sent to the Central Computer as a compare pulse. The cycle is repeated for the entire field, with compare pulses being generated every even register. The CD-IX pulse ensures that the register count will begin at register zero and that compare pulses will coincide with the reading of even-numbered registers.

The compare pulse is sent to the Central Computer to request comparison of the identification bits (5.2.1 of Part 2) in the first word of the message with identification bits in the Central Computer. If the comparison is successful, the message is accepted by the Central Computer, and both words are transferred from the drum. Further, the no-compare pulse is inhibited, and zero bits are written in the LRI OD status channel. If, however, the comparison is unsuccessful, the message is re-

jected by the Central Computer. A no-compare pulse is returned for each of the two words, and 1 bits are written in the OD status channel.

To ensure that each LRI slot will be read before the development of the status-disconnect pulse, stepping of the CD-read-status-disconnect counter begins at register zero. This stepping is effected by the LRI-status slot counter (fig. 4–6), which controls the presence of CD 4 stepping pulses at the CD-read-status-disconnect counter. The LRI-status-slot-counter flip-flop (FF 1) is set at register zero CD IX time. The 1 level output from FF 1 is necessary to cause conduction in AND 1, provided the select-LRI level is present. This produces a positive output from AND 1, which is applied to AND 2. When the read-by-status level is present, AND 2 produces an output that conditions GT 1. Since the select LRI and read-by-status levels are always present during LRI field CD reading, the 1 output from FF 1 effectively controls conduction in GT 1. Therefore, the register zero CD 3 pulse will pass through GT 1 and set FF 2, thereby conditioning GT 2. With GT 2 conditioned, the register zero CD 4 pulse is sent to the CD-read-status-disconnect counter, initiating the stepping. Although FF 1 is complemented each CD 3 time, thereby conditioning and deconditioning GT 1 accordingly, the state of FF 2 remains unchanged until the generation of the read-write-reset pulse.

2.7 XTL OD TRANSFER, BLOCK DIAGRAM ANALYSIS

Information from the XTL input element, like that from the GFI and LRI elements, is of a random nature and has a repetition rate different from that of the Drum System timing cycle. However, since XTL messages consist of three words each, it is necessary to modify normal status control of the OD writing operation. The modification employed to write XTL data is known as marker-status control.

Crosstell information is written on the XTL field of the MIXD drum. A spare field on the MIXD drum can also be utilized as an XTL field if certain wiring changes are made. The spare XTL field is designated SP XTL.

Figure 4–7 shows that the only difference at the block diagram level between the XTL fields and other fields lies in the addition of a marker-status channel on the former. The marker channel is written at the start of drum operations under the control of the Central Computer, which designates where in the channel the 1 bits, called markers, are to be placed. The markers in the channel indicate to the Input System the drum registers in which the first word of the 3-word XTL messages is to be written. The remaining two words are placed in the two registers immediately following the register associated with the marker.

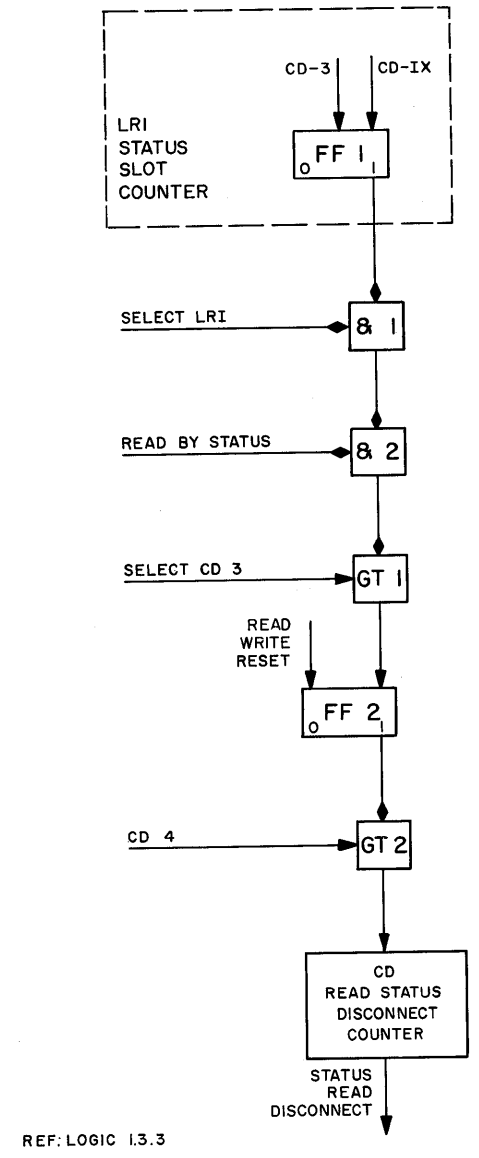


Figure 4–6. LRI Status Slot Counter and Associated Circuits, Simplified Logic Diagram

As the drum rotates, the read heads on the XTL marker and OD status channels read continuously. If a 0 is read in the OD status channel in the same register that a marker (1 bit) is read in the marker-status channel, the marker-status-control circuit produces a drum-demand pulse. The drum-demand pulse goes to the Input System and searches for an XTL message. If a message is found, three consecutive data-available pulses are returned to the XTL marker-status-control circuit at 10-usec intervals. The transfer of each of the data-available pulses is coincident with the transfer of a word to the XTL OD write circuit.

Data-available pulses cause the word in the write circuit to be written on the drum during the period of

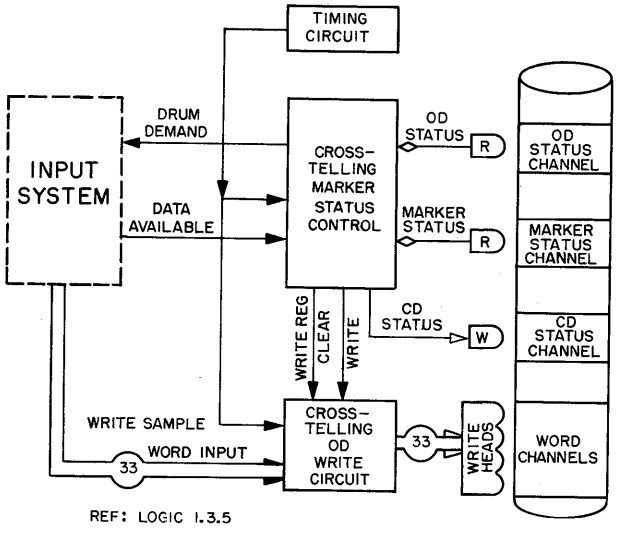


Figure 4–7. Marker-Status Modification of Status Control, Block Diagram

the write-sample pulse from the timing circuit. The data-available pulses also cause the writing of 1's in the OD status channel. After each word is written in the information channel, the XTL marker-status-control circuit produces a write-register-clear pulse. This pulse clears the register flip-flops in the write circuit, preparing them for the next word.

As in normal status-controlled circuits, the XTL and SP XTL marker status operations are synchronized by timing pulses from the drum timing circuit.

2.7.1 Marker-Status Control, Circuit Analysis

The XTL (or SP XTL) marker-status-controlled writing operation is almost identical with normal status control. The major difference between the two operations lies in the techniques employed to produce the drum-demand pulse and in the subsequent response from the Input System.

The OD marker-status-control circuits are shown in figure 4–8. The writing procedure begins with the detection of a 0 in the OD status channel. This prevents GT 1 from passing the OD 1 pulse, and the 0 state of FF 1 is maintained. The output of FF 1 conditions AND 01. To complete the requirements for conduction in AND 01, a 1 output level from FF 01 must also be present. This 1 level is produced by passing an OD 1 pulse from the MIXD timing circuit in GT 01. Gate 01 is conditioned to pass the OD 1 pulse only for those registers that have 1 bits in the corresponding areas in the XTL marker-status channel.

With inputs resulting from both a 1 in the marker-status channel and a 0 in the OD status channel, AND 01 conducts, establishing a d-c level at GT 2. Gate 2

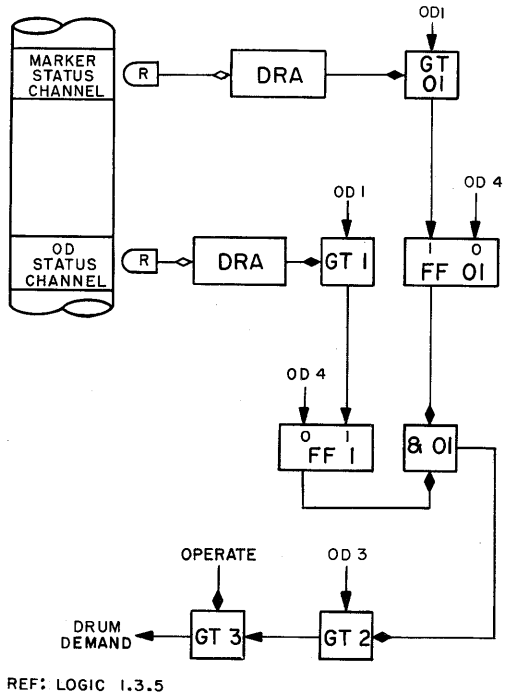


Figure 4–8. Marker-Status Modification of Status-Control Circuit, Simplified Logic Diagram

passes the next OD 3 pulse to GT 3. The GT 3 output is a drum-demand pulse. Immediately after the production of the drum-demand pulse, an OD 4 timing pulse from the MIXD timing circuit clears FF 01 in the marker-status-control circuit. No more drum-demand pulses are formed until the beginning of the next slot, which finds a coincidence of a 1 in the marker channel and a 0 in the OD status channel.

The results of the receipt of an XTL drum-demand pulse in the Input System differ from the results obtained from a drum-demand pulse from fields controlled by normal status. The XTL drum-demand pulse does not search for a single-word, but for a 3-word, message. When the message is found, three data-available pulses are returned to the XTL OD marker-status-control circuit. These pulses are 10 usec apart and coincide with the transmission of three words into the write register of the OD write circuit.

As in normal status control, the receipt of each data-available pulse causes the word placed in the write register to be written at the next OD 3 time. The three

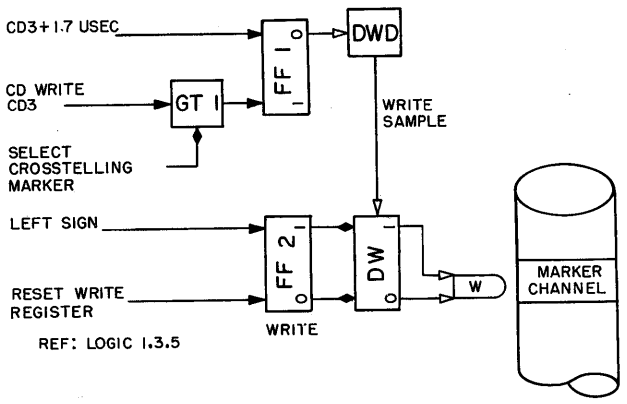


Figure 4–9. Crosstelling-Marker-Channel-Write Circuit, Simplified Logic Diagram

words are written in three consecutive drum registers on the XTL field.

The XTL status modification of normal status control duplicates the effect of having a normal-status-control circuit detect three consecutive 0's in the OD status channel and that of having three words available at the time the resulting word-demand pulses are sent to the Input System.

2.7.2 Writing Marker-Status Channel, Circuit Analysis

To indicate the first word of each XTL field slot, a 1 bit is written in the marker channel.

When the select-XTL-marker level is sent to the marker-channel write circuit (fig. 4–9) from the CD selection encoder circuits, GT 1 is conditioned to pass a CD write pulse (at CD 3 time) from the CD-read-write-control circuit. This CD write pulse sets FF 1. As a result, the flip-flop 0-state level is removed from the drum write driver. The drum write driver output becomes positive since the driver acts as an inverter. At CD 3 time +1.7 usec, a CD 3 +1.7-usec pulse from the MIXD drum timing circuit clears FF 1 and restores the flip-flop 0-state level at the drum write driver, thus driving its output negative again. As a result, a positive write-sample pulse of 1.7-usec duration is applied to the drum writer, which causes the drum writer to write the contents of FF 2 on the marker-status channel. A left-sign pulse from the Central Computer System sets FF 2, causing the drum writer to write a 1 in the marker channel when the write-sample pulse occurs at CD 3 +1.7-usec time. At CD 4 time, the write-register-reset pulse from the CD write circuit clears FF 2. Between the receipt of left-sign pulses, 0 bits written on the marker-status channel are controlled by Central Computer System programming. This is done by address control, as described in Part 2. Writing in the marker-status channel is stopped by the disconnect counter (7.7.2 of Part 2) after one revolution of the MIXD drum.

2.8 XTL CD TRANSFER, CIRCUIT ANALYSIS

A simplified logic diagram of the marker-status-read-control circuit is shown in figure 4–10. Note that this circuit is identical with that for the typical status control circuit (fig. 2–43) except for the addition of the marker-status channel and GT 5. The operation of this circuit is identical with that of the MI CD status control circuit except that a compare pulse is generated only when the first word of a message is read.

When a 1 bit is read on the marker-status channel (during the reading of the first word of a message), read circuit 2 conditions GT 5. The read-sample pulse is passed through GT 5 as a compare pulse. Only one compare pulse is generated for each message. The compare pulse is sent to the Central Computer System to request comparison of the identification bits of the first word of the XTL message with identification bits in the Central Computer System.

If comparison is unsuccessful, a no-compare pulse is sent from the Central Computer System to the Drum System for each word of the message and the words are cleared from the IO buffer register. When a successful comparison is made in the Central Computer System, the message is accepted and the no-compare pulses are not sent to the Drum System.

The disconnect counter (7.7.2 of Part 2) stops operation after one revolution of the drum containing the XTL fields. The operation of the XTL field, when it is connected as such, is identical with that of the XTL field.

2.9 CD SLOT READ CONTROL

It has been pointed out that the status control modifications in the two LRI fields (2.4) provide for two consecutive empty registers to accommodate the 2-word incoming LRI messages. Other provisions have been made to modify the status control so that there are three consecutive empty registers to accommodate the 3-word XTL messages (2.5). These modifications substantially apply to the OD side of the LRI and XTL fields.

The CD-slot-read-control circuit assures that comparison of LRI and XTL messages by the Central Computer takes place at the first word of each message so that full messages are transferred when LRI or XTL fields are selected. This action is accomplished by allowing a compare pulse to be generated once per LRI or XTL slot, at the time the first word in the slot is transferred. If this first word transfer compares favorably with program requirements, the second LRI word or second and third XTL words, as the case may be, are automatically transferred to and accepted by the Central Computer.

Figure 4–11 shows the logic configuration of the CD-slot-read-control circuit. It is significant to note that

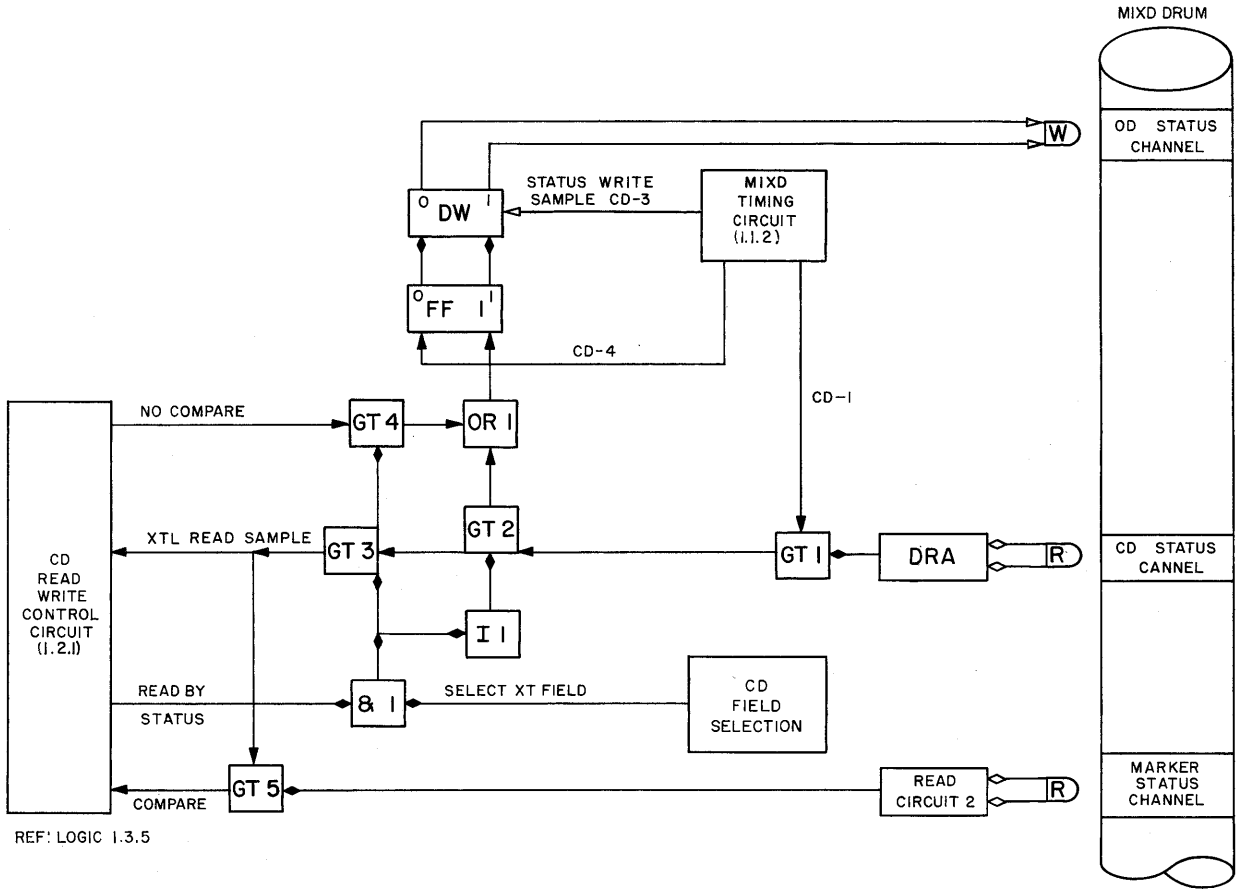


Figure 4–10. Marker-Status-Controlled XTL Field, Simplified Diagram

this circuit undertakes the ultimate generation of compare pulses for all fields in the main drums. In fact, OR 13 receives the compare-addressable, IC-compare, test-or read-sample, MI-read-sample, and GFI-read-sample pulses, as well as the output pulse from GT 5. The output of GT 5, however, is present only at the first word of each LRI or XTL slot. When the system is not in manual test, GT 8 receives the output of OR 13 and converts it into the compare pulse sent to the Central Computer.

The ultimate read-sample pulse, which is sent to the read circuits and to the Central Computer as an IO-buffer-loading pulse, is produced by OR 12. Detailed examination will reveal that OR 12 receives normal read pulses which are, in effect, LRI-read-sample and XGTL-compare-processed pulses. GFI and MI read-sample pulses are directly applied to OR 12, and LRI and XTL read-sample pulses are also applied to OR 12 through the combined operation of OR 9, OR 10, and GT 7.

Summarizing, compare pulses from all fields, with the exception of LRI and XTL, are readily produced by this circuit. Read-sample pulses from all incoming data status fields, including LRI and XTL, are readily produced by this circuit. The discussions that follow will explain the performance of the 2-stage binary counter, which determines the generation of LRI and XTL compare pulses.

The counter generally consists of FF 1 and FF 2, GT 3, and AND 3. The counter is reset by no-compare pulses from the Central Computer or by read-write-reset pulses from the read-write-control circuit. Upon resetting, AND 3 produces an output which conditions GT 5.

2.9.1 LRI Slot Control

Assuming that an LRI message transfer is in progress, LRI 1 and LRI 2 selected slot levels (2.6) apply a −30V level to OR 7. Consequently, the output of OR 7 applied to the inverter (I) circuit is also −30V. The inverter, in turn, applies a +10V level to AND 4. Therefore, when the system is not in manual test, AND 4 has two positive levels, which cause it to condition GT 4.

When GT 4 is conditioned, as previously stated, and GT 5 is conditioned after counter reset, the LRI read samples and the XTL compares applied to OR 8

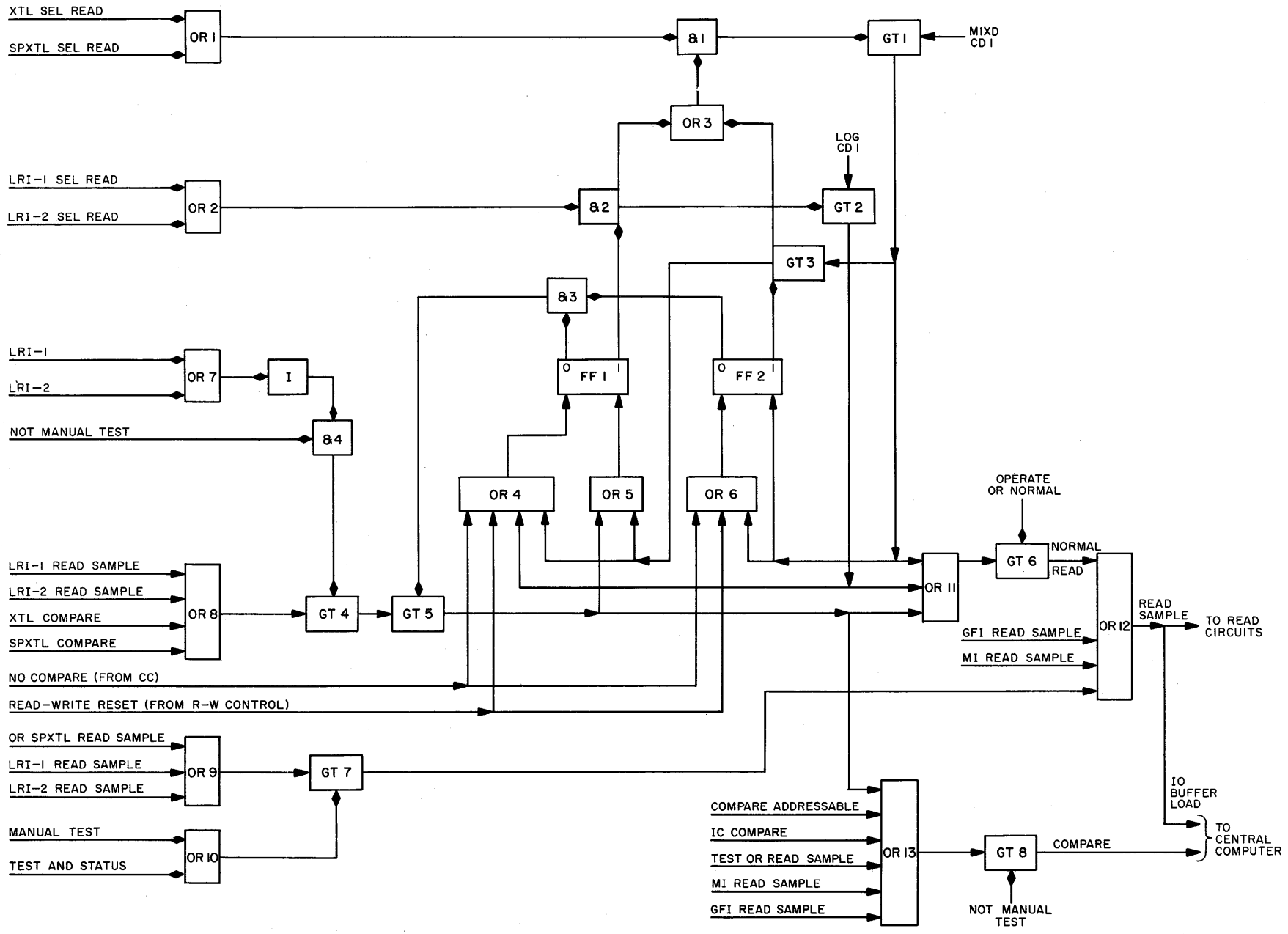


Figure 4–11. CD-Slot-Read-Control Circuit, Simplified Logic Diagram

will find their way clear to OR's 13, 11, and 5. These three OR circuits receive the pulse output from GT 5 and perform different actions as described below.

When OR 13 receives the pulse from GT 5, its output senses GT 8 to produce a compare pulse. OR 11 receives the pulse and senses GT 6 to produce a normal read pulse. OR 5 also receives the GT 5 pulse and sets FF 1. As a result of this action, one of the +10V levels to AND 3 is removed, which, in turn, removes the conditioning level to GT 5 (LRI compare pulses cannot be generated now). Additionally, when FF 1 is set, AND 2 receives a +10V level; the other level to AND 2 is assumed to be present from the read-write-control circuit. Therefore, AND 2 produces an output level which conditions GT 2 to pass the next CD 1 pulse from the LOG Drum.

The CD 1 pulse passing through GT 2 goes to OR's 11 and 4. From OR 11, the gated CD 1 pulse becomes a normal read pulse when GT 6 is conditioned by an operate or normal level from the duplex maintenance console. The gated CD 1 at OR 4 serves to clear FF 1, which re-establishes conductivity through AND 3 and causes GT 5 to be conditioned. The next LRI sample pulse from GT 4 will be passed by GT 5 to generate another LRI compare pulse.

The operation of LRI slot control can be summarized by saying that, when GT 2 is conditioned to pass CD 1 pulses, GT 5 blocks the passage of LRI read-sample pulses, and vice-versa. Considering that LRI read-sample pulses occur at CD 1 time, it follows that this circuit sends LRI compare pulses to the Central Computer strictly every other register of the LRI fields.

2.9.2 XTL Slot Control

Assuming that the transfer of an XTL message to the Central Computer is in progress, the read-write-reset pulse has just reset the counter, which results in AND 3 to condition GT 5. Thus, the next XTL compare pulse applied to OR 8 is passed by GT's 4 and 5 and appears simultaneously at OR's 13, 11, and 5. OR 13 passes the pulses on to GT 8, which, in turn, produces a compare pulse for the Central Computer. OR 11 passes the pulse to GT 6 to produce a normal read pulse. OR 5 receives the same pulse and sets FF 1. Conditioning to GT 5 is thereby removed, thus preventing the generation of the next XTL compare pulse. The positive level from FF 1 set is applied through OR 3 to AND 1. Another level required by AND 1 is supplied through OR 1 by the read-write-control circuit.

When AND 1 receives its two positive levels, GT 1 is conditioned to pass the next CD 1 pulse from the MIXD drums. The first CD 1 pulse from GT 1 senses GT 3, OR 11, and OR 6 (a normal read pulse is produced) and sets FF 2. With FF 2 set, GT 3 is conditioned and GT 1 is also conditioned through OR 3 and AND 1. The second CD 1 pulse passed by GT 1 produces several actions. It is passed by OR 11 to produce a normal read pulse, it clears (complement) FF 2 through OR 6, and it is passed by GT 3 to clear (complement) FF 1. With both flip-flops cleared, AND 3 produces an output to condition GT 5. With the conditioning of GT 5, another XTL compare pulse can be sent to the Central Computer.

To summarize the operation of XTL slot control, notice that XTL compare pulses appearing at OR 8 take place at CD 1 time. Therefore, the circuit operation is such that, during reading of an XTL field, GT 5 is conditioned every third CD 1 pulse to produce one compare pulse sent to the Central Computer.

CHAPTER 3
OUTPUT BUFFER FIELDS

The Central Computer System develops large quantities of tactical data for transfer to the Output System. This information is written on the three OB fields of the LOG drum. Since the Output System cannot process information at the rate it is developed by the Central Computer System, the rate of writing on the OB fields is reduced. Information from the Central Computer system is written on the odd or even registers of the OB fields by status control. Writing on every alternate register (odd or even) effectively reduces the rate of writing since only one-half of the available registers are written on during one complete drum revolution.

Data is transferred from the Drum System to the Output System by the OB OD circuits, which read the information on the OB fields by status-identification control. Since consecutive words are written in alternate registers, the speed of reading is effectively slowed to one-half the normal rate. This is true even though all drum registers of the three OB fields are inspected during the OD reading operation. Status-identification-control reading further enables the Output System to make selective acceptance of transferred information, so that only that data which is pertinent to Output System operation at a given time is taken from the drums.

Unlike other Central Computer field selections, OB selections apply directly to odd- and even-numbered registers of three real drum fields. The Central Computer System thus sees the three OB fields as one large continuous field. These fields are switched consecutively by means of the OB-CD field selector counter. After switching, there is a 120-usec delay before the start of writing on the next field. This delay permits decay of switching transients. When all the odd or even registers (whichever have been selected) of the three OB fields have been inspected, an OB-disconnect pulse is generated which stops the writing operation.

The OB register is read without distinguishing between even and odd registers. The word-identification circuits in the Output System determine whether the contents of a particular register are accepted. The OD reading of the three OB fields is done sequentially. Fields are switched for reading by means of the OB OD field switch circuits. After switching, there is a 120-usec delay before the start of reading on the new field to permit decay of switching transients.

3.1 OB FIELDS AND CD WRITING, BLOCK DIAGRAM ANALYSIS

The flow of data and control signals for CD status-controlled writing on the OB fields is shown in figure 4–12. CD writing on the OB fields is done by status control but only on alternate registers (odd or even). The status-control circuit finds an empty register, but writing will not take place unless the register is odd or even, depending on the mode selected by the Central Computer.

The writing operation begins with the selection of the OB odd or even registers by the Central Computer System, followed by a start-write and an IO-buffer-to-write-register pulse. The CD-read-write-control circuit then produces the write-by-status level as described in Chapter 4. Selection of OB odd or even registers by the Central Computer System causes the CD selection-register-and-selection encoder to set up either an OB-odd or an OB-even d-c level. The selected level and the write-by-status level go to the OB-CD-register-switch-control circuit, where they are combined with the OB-operate level from the OB CD gap counter and the output of the OB CD field switch to produce a write-selected-OB-field level. This level is applied to one of the OB-CD-status-control circuits which controls writing on the selected field. The OB-CD-field-switch circuit generates a select-OB-field level, which is applied to the drum field drivers to energize the heads of the selected OB field.

When the three OB fields have been inspected once, an OB-disconnect pulse is generated by the OB disconnect counter in the OB-CD-field-switch-control circuit and is applied to the CD-read-write-control circuit. The CD-read-write-control circuit converts the OB-disconnect pulse into a read-write-reset pulse, which clears the flip-flops in both the CD-read-write-control circuit and the CD write circuit, thus ending the writing operation. The OB-disconnect pulse also serves as a drum-disconnect pulse which informs the Central Computer System to stop the transfer of words to the OB fields.

3.2 OB FIELDS CD SWITCHING

Writing of the three OB fields is accomplished by a modified form of status control which causes writing in the odd or even registers of these fields. The Central Computer System does not select the individual OB fields where writing is to take place. Switching is per-

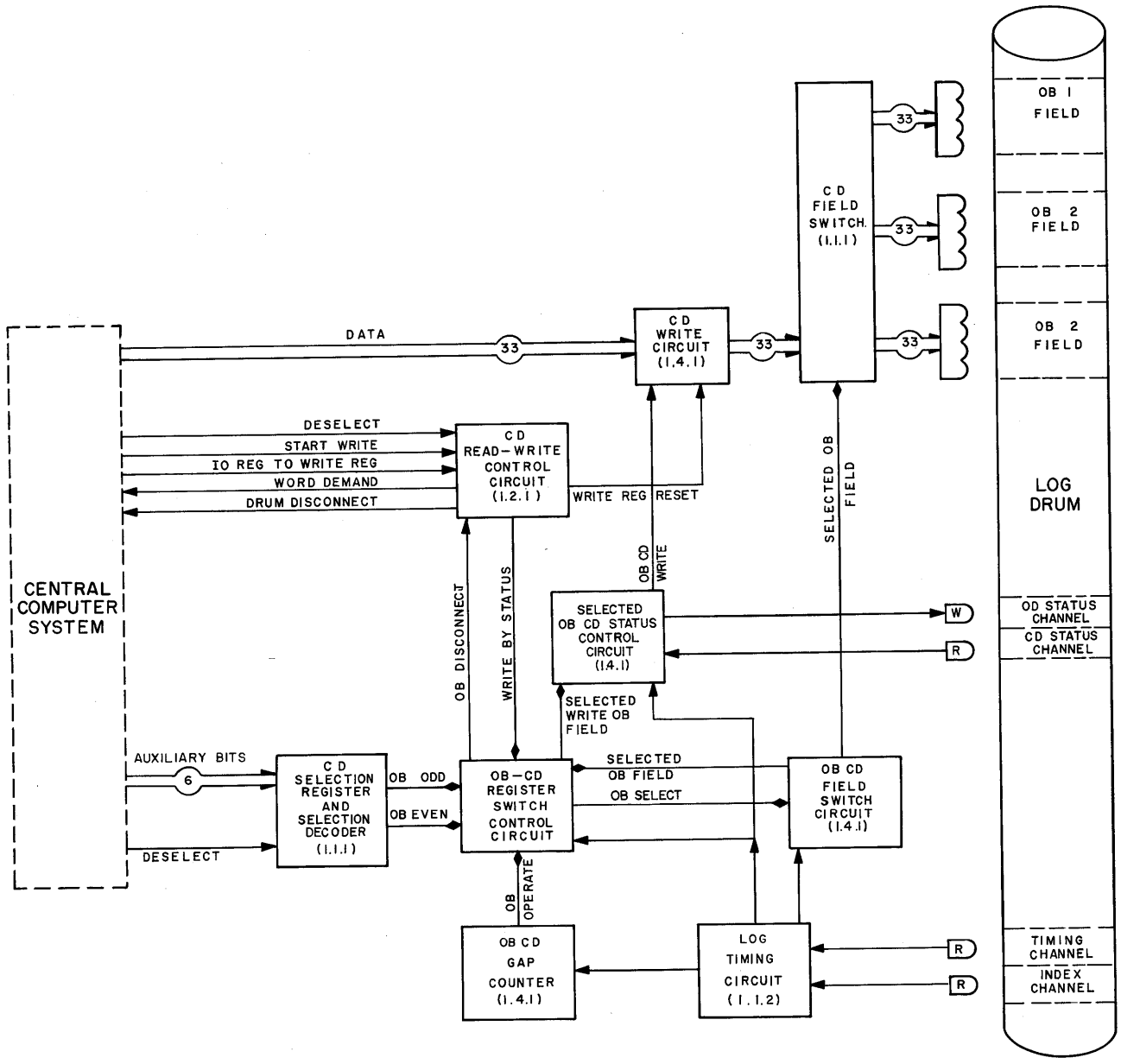


Figure 4–12. OB Fields CD Writing, Block Diagram

formed by the OB-CD-field-switch circuits. A delay is provided between OB field-switching and the start of writing in the new field by the OB CD gap counter. This time interval permits the decay of switching transients in the write heads. All three fields are switched in consecutive order, and the three fields appear as one large field to the Central Computer System. When all three fields have been inspected once, an OB-disconnect pulse is generated, causing the writing operation to stop. The following analysis describes the functions of the circuits involved in switching.

3.2.1 OB-CD-Field-Switch-Control Circuits

The OB CD field switching is accomplished by the OB-CD-field-switch-control circuit (fig. 4–13) as follows.

When power is applied to the Drum System, a power-on-reset pulse sets FF 1 and clears FF 2. The 0-state output of FF 2 and the select-OB level causes AND 1 to conduct. The output of AND 1 is the OB-select-field-1 level.

The 0-state output of FF 2 conditions GT 2 via OR 1; the 1-state output of FF 1 conditions GT 1. Gates 1

and 2 are now conditioned to pass a CD-index pulse from the LOG drum index channel. This causes FF's 1 and 2 to be complemented. Flip-flop 2 is changed to the 1 state, and FF 1 to the 0 state. AND 1 is cut off. The 0-state output of FF 1 conditions AND 2 to produce the OB-field-2 level. Gate 2 remains conditioned by the 0-state output of FF 1 via OR 1.

The next CD-index pulse is passed by GT 2 to complement FF 1. Flip-flop 1 is now in the 1 state, causing AND 2 to be cut off. Flip-flops 1 and 2 are both in the 1 state, causing AND 3 to conduct and producing the OB-field-3 level. The 1 state of FF 1 conditions GT 1.

The next CD-index pulse is passed by GT 1 to complement FF 2. Flip-flop 2 is now in the 0 state, causing AND 3 to be cut off. The 0-state output of FF 2 causes AND 1 to conduct, producing the OB-select-field-1 level, the original condition.

In this manner, OB fields are automatically switched in sequence (1, 2, 3, 1, 2, 3, etc.). The flip-flop states occurring in this circuit are listed in table 4–1.

It should be noted that at no time during normal operation can both flip-flops be cleared and that one of the AND's will conduct whenever the OB fields are selected for writing. The output of AND 1, 2, or 3 (whichever is conducting) goes to the CD field switch and prepares the selected field drum heads to write.

TABLE 4–1. CONDITIONING LEVEL FOR OB FIELD SWITCHING

FLIP-FLOP 1	FLIP-FLOP 2	OUTPUT LEVEL
1	0	OB 1
0	1	OB 2
1	1	OB 3
1	0	OB 1

The CD-index pulses are also counted by the OB-disconnect counter (fig. 4–13), which is a standard, 2-stage, scale-of-3-counter circuit. At the fourth CD-index pulse passed by GT 5, the status of all registers of the three OB fields will have been inspected once. The fourth CD-index pulse causes the OB disconnect counter to produce an OB-disconnect pulse. The OB-

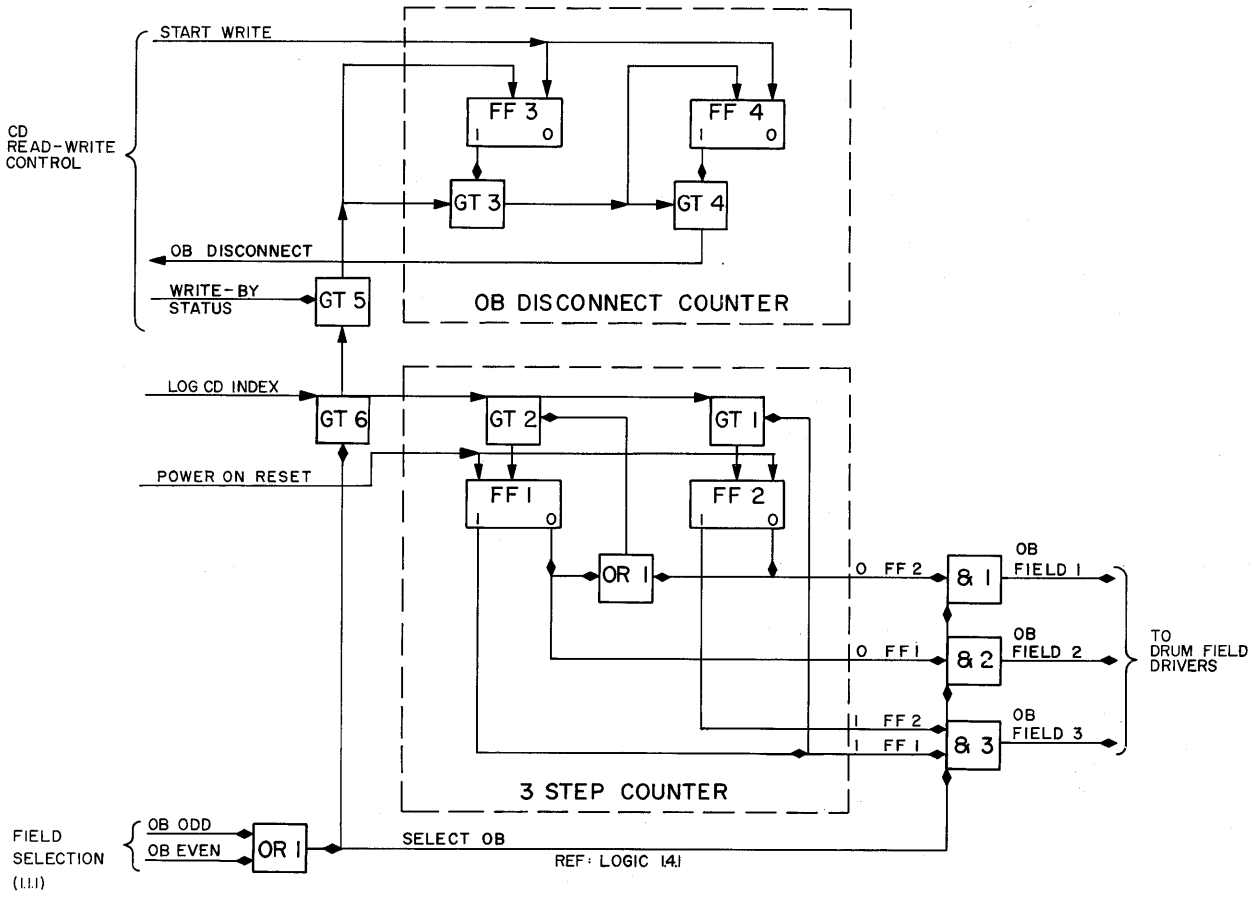


Figure 4–13. OB-CD-Field-Switch-Control Circuit, Simplified Logic Diagram

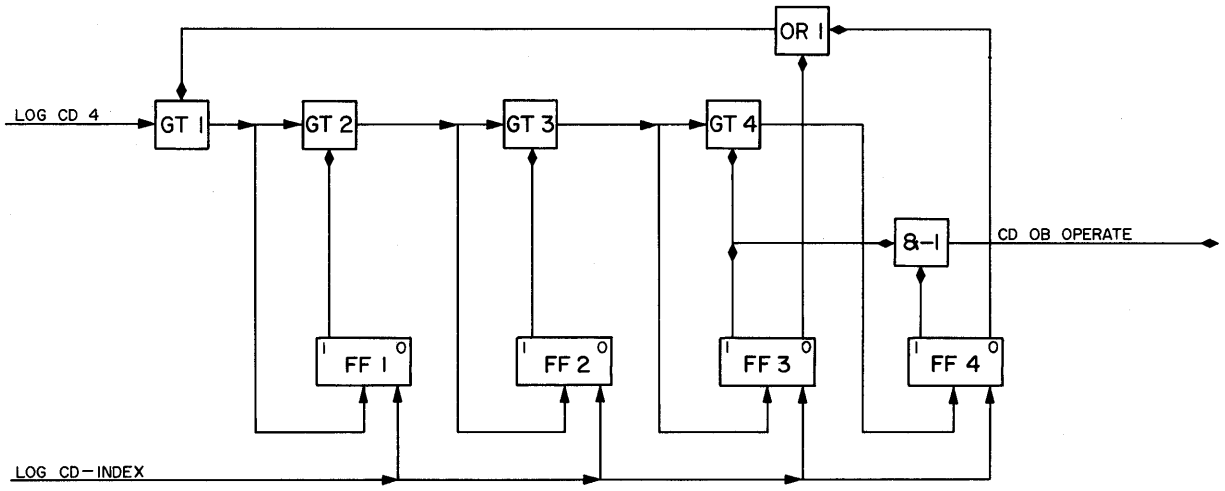


Figure 4–14. OB CD Gap Counter, Simplified Logic Diagram

disconnect pulse goes to the CD read-write-control circuit to end the writing operation.

The OB CD gap counter provides the 120-usec delay necessary between OB field switching and the start of writing in the new OB field.

The gap counter is a 4-stage, scale-of-12-counter circuit (fig. 4–14). A CD-index pulse from the LOG drum clears FF's 1 to 4. The 0-state level of FF 3 or 4 via OR 1 conditions GT 1 to pass CD 4 pulses from the LOG drum. At the 12th CD 4 pulse, FF's 3 and 4 will be in the 1 state. The 1-state levels of FF's 3 and 4 cause AND 1 to conduct, producing the CD-OB-operate level. The CD-OB-operate level goes to the OB-CD-field-switch-control circuit as a necessary condition for the writing operation. Also, since FF's 3 and 4 are both in the 1 state, the conditioning level is removed from GT 1. Gate 1 will not conduct until the next CD-index pulse clears FF's 1 to 4, initiating a new delay cycle.

3.2.2 OB-CD-Register-Switch-Control Circuits, Function and Description

The OD-CD-register-switch-control circuit (fig. 4–15) provides the d-c levels required by the selected status control circuit to cause writing on either the odd or even registers of the OB fields as selected.

The CD 4 timing pulses complement FF 1 continuously from the 0 state to the 1 state and back. Coincidence of the 0-state level of FF 1 and the OB-even level from the CD-selection-register-and-selection encoder produces an output level at AND 2. Similarly, the 1-state

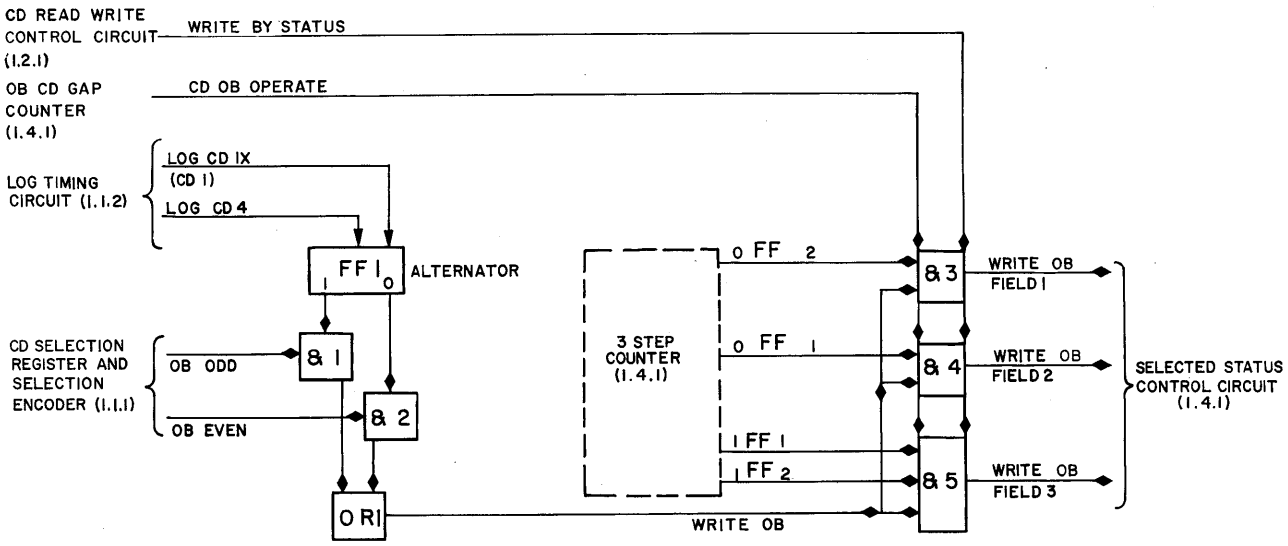


Figure 4–15. OB-CD-Register-Switch-Control Circuit, Simplified Logic Diagram

level of FF 1 and the OB-odd level produce an output at AND 2. The function of the CD-index pulse (at CD 1 time) is to make certain that the previous CD 4 pulse has brought FF 1 to the 0 state. The index pulse, therefore, acts as a check on the even or odd operations and assures that the first CD 4 pulse at the beginning of every drum revolution places FF 1 in the 1 state.

As a result of the action described above, AND conducts for even registers, and AND 1 conducts for odd registers when the respective selection levels are present. Thus, an output is obtained from one of these AND's every other register. There is an interval of 20 usec between the consecutive outputs from the selected AND.

The outputs of AND's 1 and 2 go to OR 1. The resulting condition of OR 1 produces an output level which is sent to AND's 3, 4, and 5. Thus, one condition for energizing AND's 3, 4, and 5 is the output described above, which is present every other register. Determination of which AND (3, 4, or 5) is to conduct is accomplished by output levels from the 3-step counter described in 3.2.1.

The CD read-write-control circuit sends a write-by-status level to be used as one of the necessary input levels to AND's 3, 4, and 5.

The CD-OB-operate level, which feeds AND's 3, 4, and 5, comes from the OB CD field gap counter. This level is the last necessary condition for conduction in these AND's. The output of the selected AND's (3, 4, or 5) is the write-OB-field level, which enables the selected status control circuit to start writing operations on the selected field.

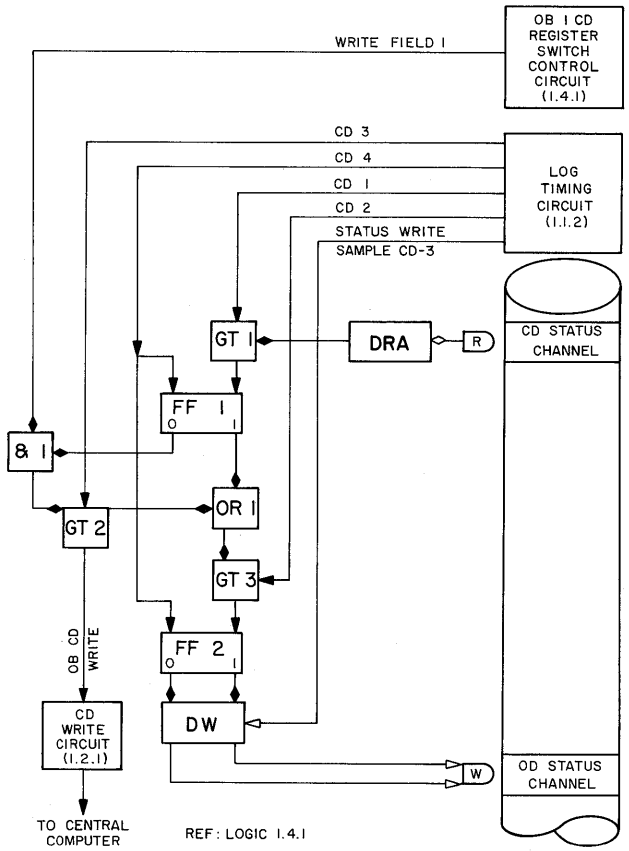


Figure 4–16. OB Field 1 CD-Status-Control Circuit, Write-by-Status Operation, Simplified Logic Diagram

3.3 OB-CD-STATUS-CONTROL CIRCUIT, FUNCTIONAL DESCRIPTION

The write-OB-field level from the OB-CD-register-switch-control circuit goes to the OB-CD-status-control circuit. The write OB field is present at every odd or even register (3.2.2). Thus, this level is present for 10 usec (one drum register) and is absent for 10 usec. The write-OB-field level switches from one state to the other state every CD 4 time. The write-field level (fig. 4–16) goes to AND 1. The circuit shown is for OB field 1. The OB-CD-status control circuits controlling OB fields 2 and 3 are similar.

Sensing a 0 bit in the CD status channel at CD 1 time permits FF 1 to remain in the 0 state. The 0-state output of FF 1 goes to AND 1. If the write-field level is present (the drum register is of the selected mode, odd or even), AND 1 sends an output level to GT 2. Gate 2 passes the next CD 3 timing pulse as an OB-CD-write pulse. This pulse is sent to the CD-read-write-control circuit. There, the OB-CD-write pulse branches. One branch goes to the CD write circuit as a CD-write pulse, causing the data in this circuit to be written on the drum register inspected. The second branch of the OB-CD-write pulse is delayed 2.5 usec (CD 4 time), splits and is sent to the Central Computer System as a word-demand pulse and to the CD write circuit as a write-register-reset pulse. The word-demand pulse requests an additional word; the write-register-reset pulse clears the CD write circuit to prepare it to receive the next word.

The output from AND 1 also goes to GT 3 via OR 1. Gate 3 is conditioned to pass the CD 2 timing pulse after the empty drum register is sensed (CD 1 time). This gated pulse sets FF 2. The 1-state output of FF 2 is applied to the drum writer. When the status-write-sample pulse arrives (CD 3 time), the drum writer enters a 1 bit on the OD status channel, indicating that the associated drum register is full. The OD status channel is written at the same time that the associated drum register is written. Flip-flops 1 and 2 are cleared by the CD 4 timing pulse.

If the empty register had been of the wrong order (odd for the selection of even-writing, or vice versa),

FF 2 would have remained in the 0-state and a 0 would be written in the OD status channel. Thus, the associated drum register is available for writing only when the corresponding type of operation is selected.

When a 1 bit indicating a full register is read in the CD status channel (CD 1 time), GT 1 is conditioned to pass the CD 1 timing pulse occurring during the timing cycle of the register being checked. This gated CD 1 pulse sets FF 1. The 1-state output of FF 1 conditions GT 3 via OR 1 to pass the next CD 2 timing pulse to set FF 2. The 1-state output of FF 2 causes the drum writer to enter a 1 in the OD status channel when the status-write-sample pulse is received (CD 3 time). This indicates that the register is still full. Writing of a new word is prevented by lack of the 0-state output from FF 1 at AND 1.

If the field shown is not selected, AND 1 is cut off. If a 1 is read on the CD status channel, GT 1 is conditioned to pass a CD 1 pulse. The gated CD 1 pulse sets FF 1, causing conduction in OR 1. The resulting output of OR 1 conditions GT 3 to pass a CD 2 timing pulse. The gated CD 2 timing pulse sets FF 2, causing the drum writer to enter a 1 on the OD status channel at CD 3 time. The 1 bit indicates that the associated drum register is full. Flip-flops 1 and 2 are cleared by the next CD 4 pulse. If a 0 is read on the CD status channel, FF's 1 and 2 remain in the 0 state. At CD 3 time, a 0 is written on the OD status channel, indicating that the associated drum register is empty.

Writing, therefore, is possible only on the selected registers (odd or even) of the selected field.

When the OB field switch counter is stepped by the next CD-index pulse, the write-OB-field level is removed until 12 CD 4 timing pulses have been counted by the OB CD gap counter. At this time, the OB-CD-status-control circuit for the next OB field is conditioned for operation.

3.4 OB FIELDS OD READING, BLOCK DIAGRAM ANALYSIS

The status-identification-controlled reading of the three OB fields is similar to the status-identification-controlled reading of the GFI, LRI, and MI fields performed by the CD circuits. The reading of the three OB fields by status-identification control is a continuous operation. Each OB field has an associated OB-CD-status-control circuit which controls the reading of that field. The three OB-OD-status-control circuits are identical.

Each OB field is provided with two channels in addition to the 33 channels which store the drum word and the parity bit (fig. 4–17). These channels are the OD status channel and the CD status channel. On any one field, the bits in each channel refer to specific registers on the same field. A 1 bit in the OD status channel indicates that the register to which it refers contains a word to be read. A 0 bit in the OD status channel indicates that the register is empty.

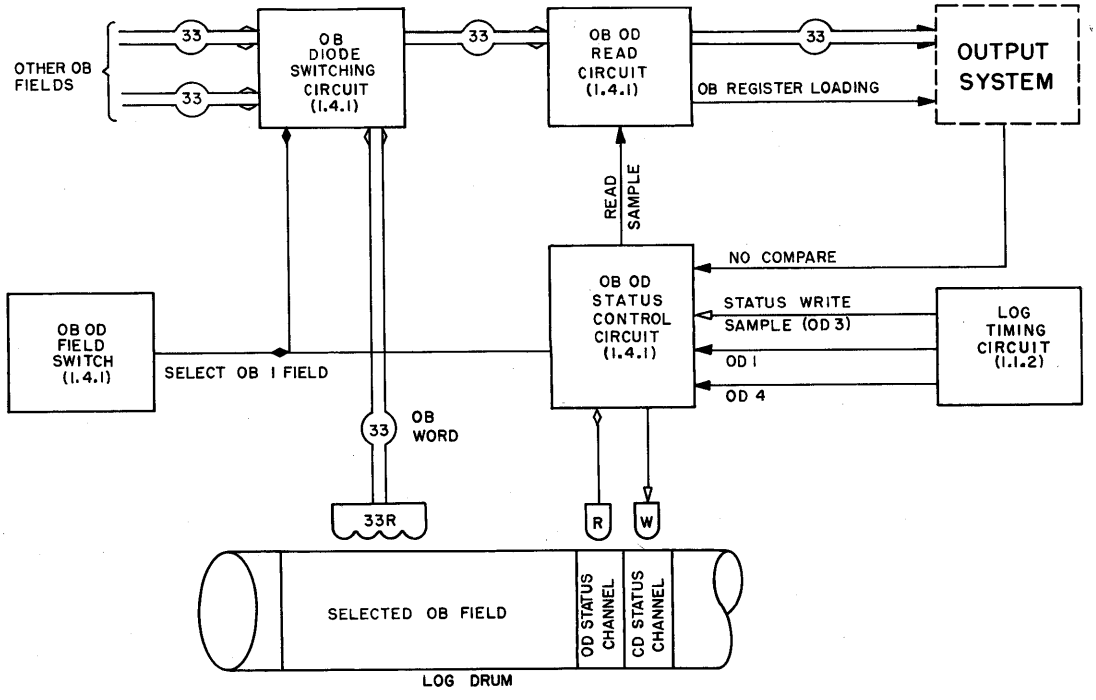


Figure 4–17. OB OD Status-Identification-Controlled Reading Block Diagram

A 1 bit in the CD status channel indicates to the CD circuits that a word is present in the drum register with which the bit is associated and that no word can be written in that register. A 0 bit in the CD status channel signifies that the register referred to is available and a word may be written in it.

The OD status channel is read by the OB OD circuits and written by the CD circuits. The CD status channel is read by the CD circuits and written by the OB OD circuits. During any revolution of the LOG drum, the status channels of the three OB fields are read and written continuously. However, their contents effect the OD operations of only one field at a time. This field is the one chosen by the OB field selection circuits (3.5).

Figure 4–17 is a block diagram of the OD reading operation for the selected OB field. The reading operation for the other two OB fields is identical. When an OD 1 pulse is received by the OD-status-control circuit from the LOG drum timing circuit, the read head for the OD status channel detects the bit for the drum register associated with the timing cycle occurring at that instant. The OD-status-control circuit is selected by a select level from the OB-OD-field-switch circuit. If the OD status channel contains a 0, indicating that there is no word to be read into the Output System, the OD-status-control circuit produces no effect other than the writing of a 0 in the CD status channel when the status-write-sample pulse is received from the LOG drum timing circuit at OD 3 time. If, on the other hand, the OD status channel contains a 1, the OD-status-control circuit produces a read-sample pulse. This pulse is then sent to the OB OD read circuit. In the OB OD read circuit, the read-sample pulse produces an OB-register-loading pulse which goes to the Output System. The OB-register-loading pulse informs the Output System that a word is transmitted from the OB OD read circuit. The word is sent to the Output System at the same time as the OB-register-loading pulse. The word comes from the OB field through the OB-OD-diode-switching circuit.

The OB-OD-diode-switching circuit receives its word input from the OB field selected by the select-field level. The select-OB-field level comes from the field selection circuits. This level goes to the center taps of the read heads of the selected field. Only the contents of the selected field can pass through the OB-OD-diode-switching circuit.

The Output System compares identity bits in the OB word with identity bits in its own circuits. When the Drum System sends a word from one of the OB fields, the CD-status-channel write circuit is conditioned at OD 4 time to write a 0. If the Output System rejects the word, a no-compare pulse sets up the CD-status-channel write circuit to write a 1. This no-compare pulse must come to the status-control circuit before the next OD 3 time when the status bit is to be written.

This operation is continuous, repeating for every register, on each OB field. At the next OD-index pulse, another OB field is selected in rotation. The reading operation remains the same but is now controlled by the OD-status-control circuit of the new OB field.

3.5 OB-OD-FIELD-SWITCH CIRCUIT, FUNCTIONAL DESCRIPTION

The OB-OD-field-switch circuit (fig. 4–18) switches reading operations from one OB field to the next OB field in rotational sequence. The operation of this circuit is similar to that of the OB-CD-field-switch-control circuit (3.2.1).

The OB OD field switch produces selected OB-field levels which go to the center taps of the read heads in the OB-OD-diode-switching circuit, enabling them to send information to the OB-OD-read circuit. The OB-OD-field-switch circuit also produces the selected-OB-OD levels at the outputs of AND's 2, 3, and 4. These levels, produced one at a time, activate the OB-OD-status-control circuits, which control the reading of the OB fields.

In order for AND's 2, 3, and 4 to conduct, the Drum System must be in an operational mode rather than in a test mode (an operate level from the computer-test-control circuit must be present) and must have the OB-operate level from the OB OD gap counter. (Refer to 3.2.1 for a functional description of the OB CD gap counter. The OB OD gap counter operates in a similar manner.) The OB-operate level is present at all times except for the 120-usec period immediately following the OD-index pulse.

3.6 OB-OD-STATUS-CONTROL CIRCUIT

Figure 4–19 shows an OB-OD-status-control circuit which represents any one of the three OB-OD-status-control circuits used in OD OB reading.

An OD 4 pulse from the LOG timing circuit clears FF 1. An OD 1 pulse from the LOG timing circuit appears at GT 1, 2.5 usec later. If a 1 is present in the OD status channel, the read head for the channel and the drum read amplifier connected to this head places a wide pulse at GT 1. The presence of the 1 in the OD status channel indicates the presence of an information word in the drum register associated with that space in the status channel. The wide pulse at GT 1 conditions the gate to pass the OD 1 pulse to GT's 2 and 3. Gate 2 is conditioned by a select-OB-OD level from the OB-OD-field-switch circuit. Gate 2 conducts, producing an OB-read-sample pulse (at OD 1 time), which is sent to the OB OD read circuit. In the OB OD read circuit, the read-sample pulse transfers the word in the drum regis-

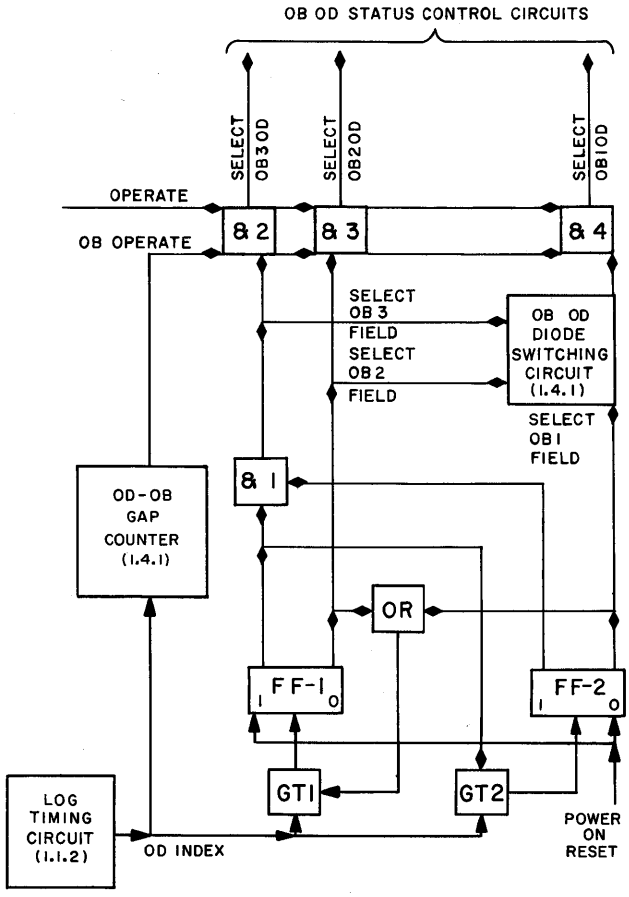


Figure 4—18. OB OD Field Switch Circuit, Simplified Logic Diagram

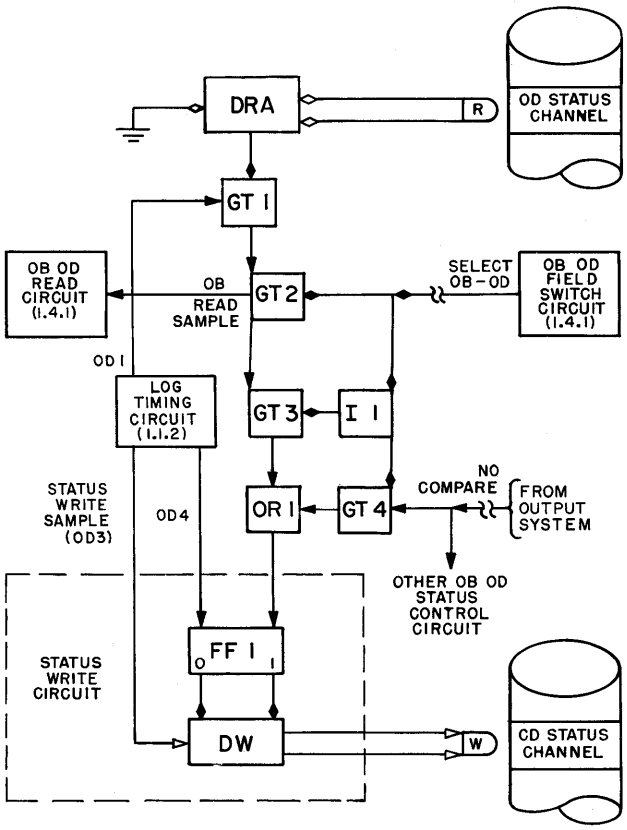


Figure 4—19. Typical OB OD Status-Control Circuit, Simplified Logic Diagram

ter to the Output System and is sent to the Output System as the OB-register-loading pulse.

On receipt of the OB word and the OB-register-loading pulse (at OD 1 time), the Output System compares identity bits in the word with its own identity bits and performs a parity check on the word. The Output System accepts the word if the drum word identity bits compare with the Output System identity bits. However, if the comparison produces negative results, the Output System returns a no-compare pulse to the OD-status-control circuits (fig. 4—19). The no-compare pulse is received at GT 4. In the OB-OD-status-control circuit, the select-OB-OD level is present at GT 4 and conditions the passing of the no-compare pulse to OR 1. OR 1 also conducts if a 1 is read in the OD status channel and if the field is not selected. This is so because the inverter tube places a conditioning level at GT 3 during the absence of the select-OB-OD level. The conditioning level then passes the output of GT 1 (present when a 1 is read in the status channel) to OR 1.

Conduction in OR 1 sets FF 1, placing the 1-state-output-d-c level at the drum writer. During the period of the status-write-sample pulse from the LOG timing circuit (OD 3 to OD 3 plus 1.7 usec), the drum writer places a 1 bit at the CD status channel write head. This bit causes a 1 to be placed in the point in the CD status channel that is associated with the register read into the Output System, providing an indication to the CD circuits that the word in the register has not been used during the drum revolution being considered. The Central Computer System does not write on registers whose CD status channel bits are 1's.

If a 0 bit is read at OD 1 time or if the Output System accepts the word, FF 1 sends a 0-state-output level to the drum writer because the flip-flop remains in the cleared state after the receipt of the OD 4 pulse. At these times, a 0 is written in the CD status channel, indicating to the Central Computer System that the register in question may be written into.

The next OD 4 pulse from the LOG timing circuit clears FF 1 to initiate the writing sequence for the next drum register appearing under the read heads as the drum rotates.

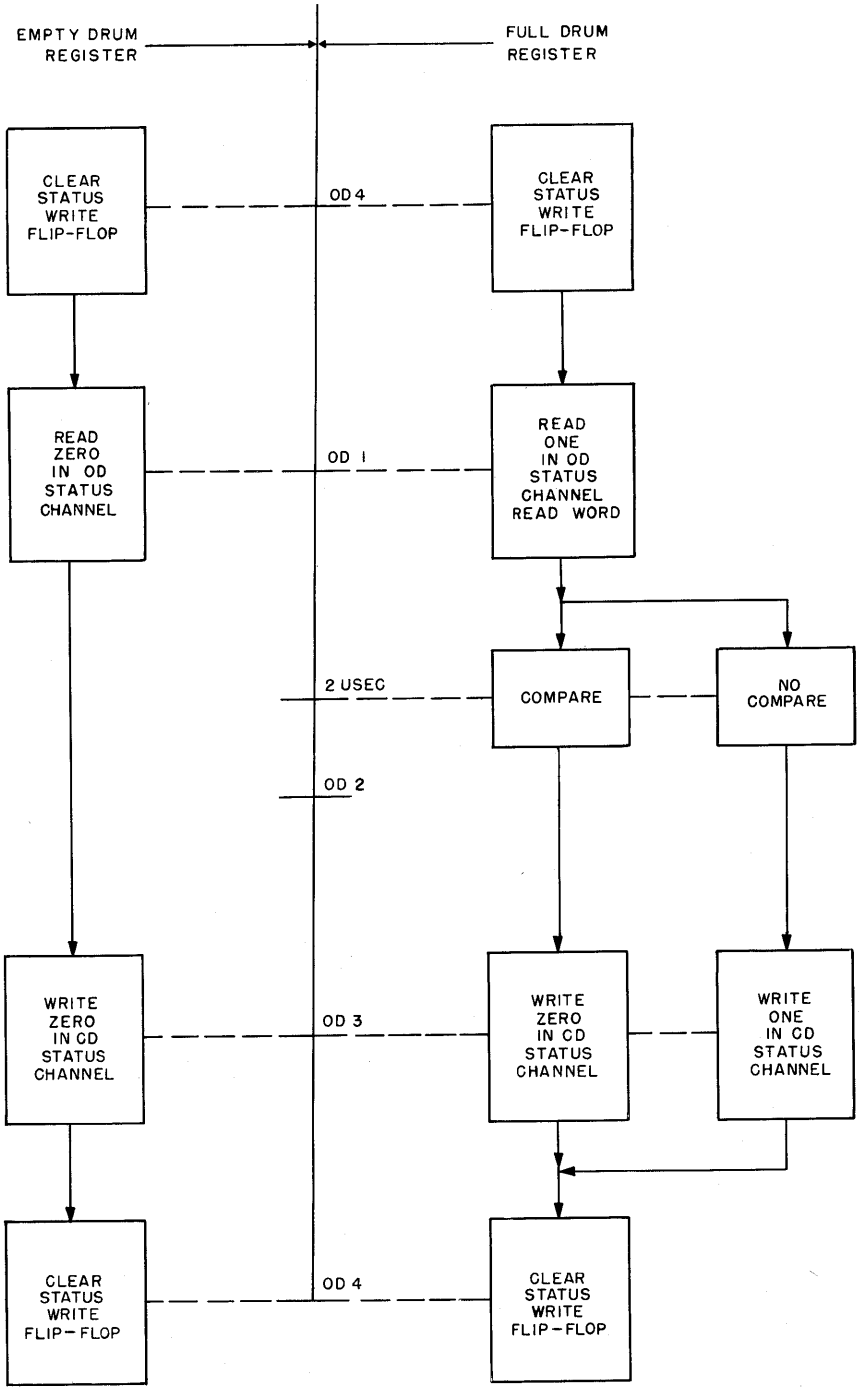


Figure 4–20. Time Sequence of Significant OD Reading Operations

The status reading operation is reviewed in figure 4–20. At OD 4 time, the status write flip-flop (FF 1) is cleared. At the OD 1 pulse which follows immediately thereafter, the bit in the OD status channel is detected. If the drum register is empty and the bit is a 0, the OB-OD-status-control circuit writes a 0 in the CD status channel at OD 3 time. If there is a word in the drum register, a 1 bit is read and the word is transferred to the Output System. If the word compares, no signal is returned, and the OB-OD-status-control circuit writes a 0 in the CD status channel at OD 3 time. If, however, the word does not compare, a no-compare pulse is returned to the Drum System at OD 1 plus 2 usec. Under these circumstances, the OB-OD-status-con-

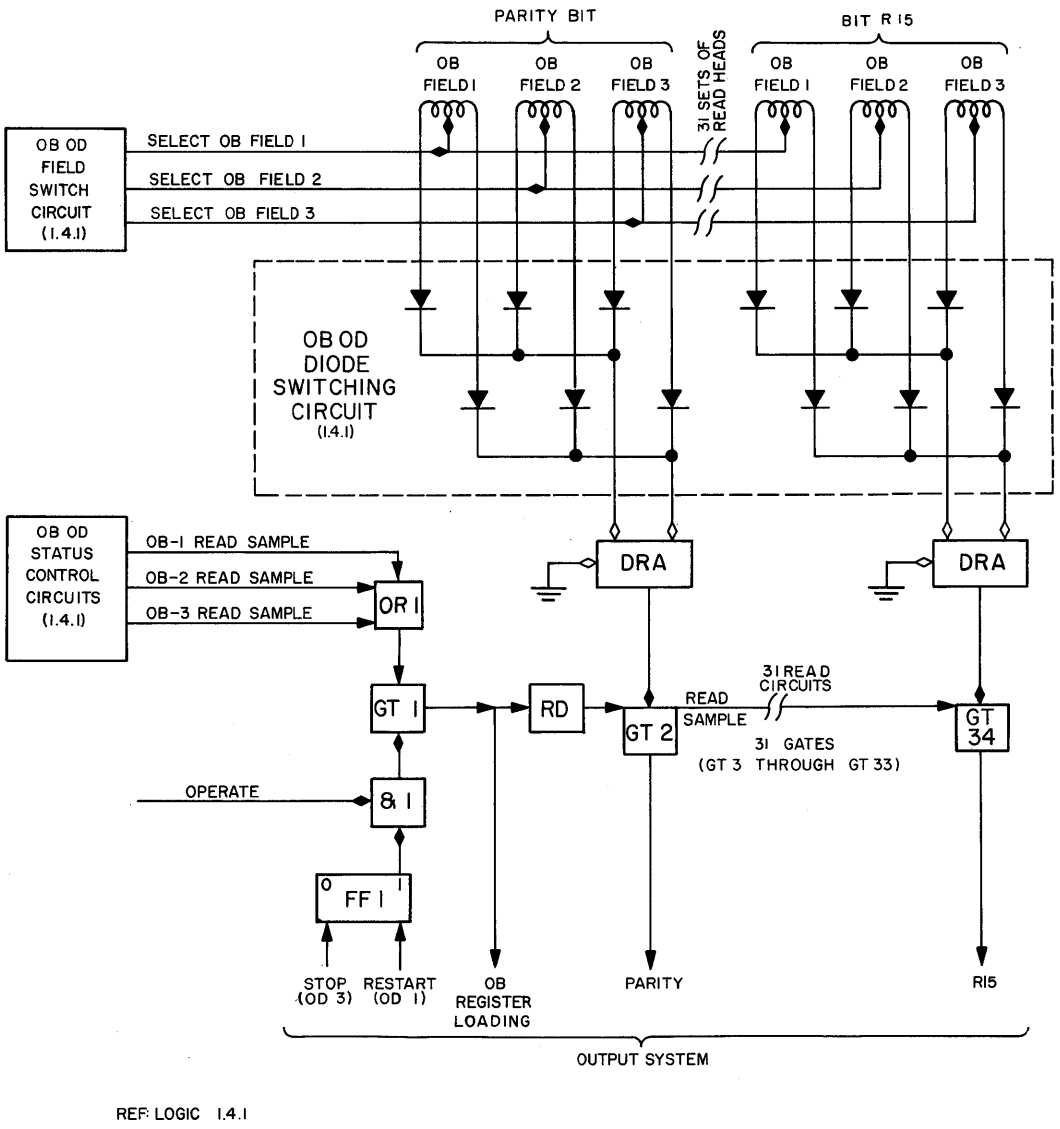


Figure 4–21. OB OD Read Circuit, Simplified Logic Diagram

trol circuit writes a 1 in the CD status channel at OD 3 time. At the OD 4 pulse which follows immediately, the status write flip-flop is again cleared.

3.7 OB OD READ CIRCUITS AND DIODE SWITCH

In the OB OD read circuit (fig. 4–21), the OB-read-sample pulse from the OB-OD-status-control circuit produces conduction in OR 1. The output of OR 1 goes to GT 1. Gate 1 is conditioned if AND 1 conducts and places a d-c level at the gate. Assuming conduction in AND 1, the GT 1 output goes to the Output System as an OB-register-loading pulse. This pulse indicates to the Output System that the Drum System has placed a word in the drum word entry register. This pulse is amplified in the register driver and is applied to GT's 2 through 34 as a read-sample pulse. Each of these gates passes a read-sample pulse to the Output System whenever the gate is conditioned by a wide pulse from the drum-read amplifier to which it is connected.

The drum-read amplifier receives the read head outputs via the OB-OD-diode-switching circuit. The OB-OD-diode-switching circuit makes it possible for a single read circuit to transfer information from the three OB fields to the Output System by activating the read heads on only one field at a time. (For a detailed description of diode-switching, refer to 3.2.)

AND 1 (fig. 4–21) requires two d-c levels to produce an output: the operate level from the computer-test-control circuit and the 1-state output of FF 1 in the

OB OD read circuit. The operate level is present whenever the Drum System is performing normal operations but is absent during test procedures. Flip-flop 1 in the OB OD read circuit. The operate level is present when-Output System and is cleared by a stop pulse. The stop pulse is transmitted to the Drum System OB OD circuits to stop OB reading when it is desired to perform tests on the Output System. At the conclusion of these tests, the restart pulse is sent and normal operations resume. Thus the normal operate mode of the Drum System OB OD element is the continuous reading of the three OB fields, which is interrupted only when the Drum System or the Output System is in the test mode of operation.

PART 5
DRUM SYSTEM TEST CIRCUITS

CHAPTER 1
INTRODUCTION

This part describes the theory of operation of the Drum System test circuits. These circuits fall within two categories: computer-test circuits and manual-test circuits. Also discussed are the manually initiated timing-rewrite-and-erase controls.

Because the Drum System is divided into two areas, the auxiliary drums and the main drums, the associated test circuits are also distinguished in this way. The computer-test circuits affect only the main drums. Although the auxiliary drums are computer-tested, these tests involve the use only of circuits peculiar to normal auxiliary drum operation. The computer-test circuits provide Central Computer System program control of Drum System OD circuits which are not controlled by tactical programs. During main drum computer tests, information written on the CD side of the CD-OD drums by the Central Computer System is read from the OD side of the drum and returned to the Central Computer System. Similarly, the Central Computer System is able to write information on the OD side of the drum; this information is transferred to the Central Computer System on the CD side. With access to both sides of a CD-OD drum, the data stored on and read from these drums may be compared to make certain that no change has taken place.

Other circuits enable manual checks and tests to be performed on the Drum System. These are the auxiliary drums manual-test circuits and the main drums manual-test circuits. The manual-test circuits provide a means by which normal operating conditions may be simulated; thus, normal operating circuits may be checked for correct performance. During Drum System manual tests, the system operates independently from all other data-handling systems.

The Drum System erase circuits are manually activated. Upon completion of an erase operation, timing and index channel rewriting automatically follows. All six main drums or all six auxiliary drums may be simultaneously erased. However, since there is only one timing-and-index-channel-write circuit for each drum group (main drums and auxiliary drums), the corresponding operation is performed sequentially under relay control. This applies only to those systems that use optical timing generation (sites 1 through 16). Sites which employ etched timing generation do not require the timing-and-index-channel-rewrite circuit. (Refer to 4.2 of Part 2.)

1.1 COMPUTER-TEST CIRCUITS

The computer-test mode of operation serves to provide a thorough check, not only of the Drum System itself, but also of its interaction with the Central Computer System. Two basic types of computer tests are performed: one for the fields written on the CD side of the drums and read from the OD side (SD, DD, IC, and OB fields); one for the fields written on the OD side of the drums and read on the CD side (MI, GFI, LRI, and XTL fields). Computer test operation control is determined by the field being tested. If the field is addressable, normal address control (Ch 7, Part 2) is exercised; if the field is status in nature, normal status control (Part 4) is exercised.

The conditions necessary for either type of computer test are the result of manual intervention and programmed selection. The entire CD-OD computer-test operation centers around the state of 3-legged AND circuits in logic 1.8.1 (figs. 2–31 and 2–32). Two of the inputs to these AND circuits are +10V levels made available when the TEST-OPERATE switch on the duplex maintenance console is placed in the TEST position and switch S2 on the module 21L test door (fig. 5–1) is placed in the DRUM-IN-COMPUTER-TEST position. The third condition is realized upon the presence of a test-select level, resulting from a test field selection. With the three conditions satisfied, an OD-test-read or OD-test-write level is produced (as determined by the nature of the field selected) to complete the signal flow connections between the Central Computer System and the Drum System. Upon the selection of a specific test field, the drum heads on the CD side of that drum are energized. The OD-test-read and OD-test-write levels serve to condition the respective test-read and test-write gates.

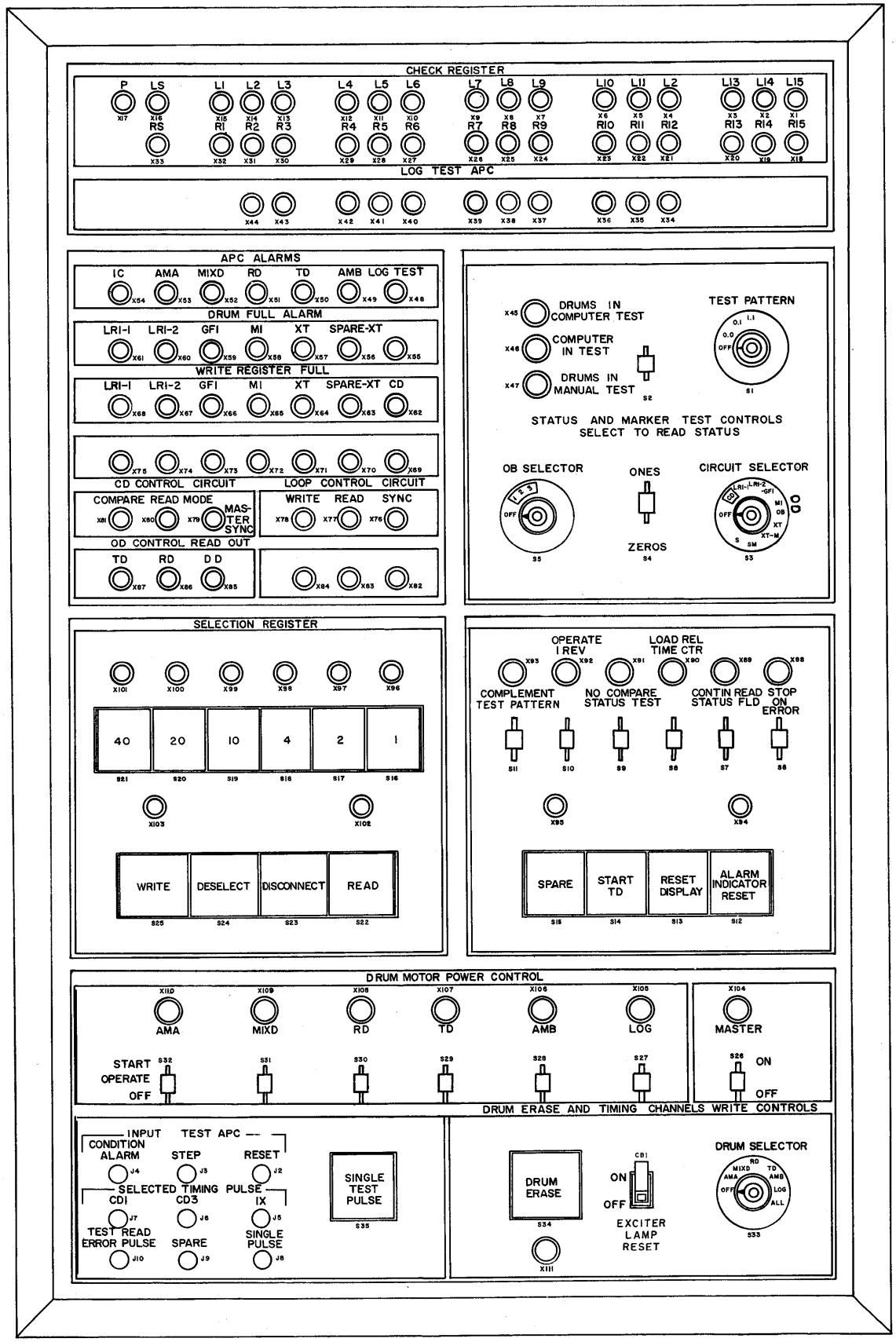


Figure 5–1. Module 21L, Test Door

The normal receipt of control pulses takes place at the read-write-control circuit, which, in turn, sends them to the computer-test-control circuit. These control pulses are also utilized in the CD circuits in the normal manner (Ch 7 of Part 2).

If a start-write operation is programmed with the selection of an OD reading field, a computer-test-control circuit provides the control signals required by the test-selected-OD-read circuit to read that field. The computer-test-control circuit transfers the data through the computer-test-read switch to the CD read bus. This enables the Central Computer System to compare data read on the OD side of the drums with data previously written on the CD side.

If a start-read operation is programmed, an OD writing field is selected, and the computer-test control circuit conditions the computer-test-write-switch circuits to transfer information from the Central Computer System to the selected OD write circuit. The computer-test-control circuit then conditions the selected OD-write-control circuit to write information on the drum. This information is read by the CD read circuits and transferred to the Central Computer System for comparison.

1.2 MANUAL-TEST CIRCUITS

Drum System manual-test circuits enable the simulation of normal operating conditions in the auxiliary and main drums. Each drum type employs individual manual-test circuits; therefore, corresponding tests are separately conducted. The tests are initiated by activation of controls mounted on the associated test doors. These controls serve as a means of generating the various Drum System functions: selection, writing, reading, etc.

During manual tests, only Drum System circuits are exercised. The test pattern is originated at the test door by means of test pattern selection. This information is circulated throughout the system in the normal manner (as determined by the field selected) and returned to the test door for comparison.

Various neon lamps mounted on each test door serve to indicate the results of each phase of a manual-test operation. Therefore, the successful or unsuccessful generation of a Drum System function may be determined at the place of origin. In addition, test door neons provide a visual indication of the compared word. The indications of the above neons reflect only Drum System circuit conditions.

CHAPTER 2
ADDRESSABLE FIELDS

2.1 AUXILIARY DRUM FIELDS, COMPUTER TEST

No test circuits are necessary for computer tests of the fields in the auxiliary drums, AM-A through AM-H, because test operations utilize the same transfer controls as normal operations. A test pattern is originated at the Central Computer System and stored on every register of the auxiliary drum fields. The pattern is returned to the Central Computer System and compared to determine whether any alteration has taken place.

2.2 DISPLAY FIELD COMPUTER TEST

Display field computer-test circuits permit the Central Computer System to read the OD side of the display fields (TD, RD, and DD). Test words previously written on the CD side of these fields by the Central Computer are compared in the Central Computer System with the test words read from the OD side to make certain that they have not changed during the transfer.

The circuits of the display fields of the Drum System normally read the display fields from the OD side of the drums during normal operation and transfer the display data to the Display System. During computer tests on the display fields, a test signal path is provided which allows the Central Computer System to read the OD side of the display fields. For performance of computer tests on the display fields, the computer-test-control circuit is conditioned by a test d-c level from the manual-test circuits (fig. 5–2). To start a reading operation on the OD side of the drums, the Central Computer System sends a deselect pulse to the CD-read-write-control circuit. In the CD-read-write-control circuit, the deselect pulse is converted into a read-write-reset pulse, which clears the flip-flops of the computer-test-control circuit. Clearing the computer-test-control circuit prepares the computer-test signal path to accept programmed operating instructions from the Central Computer System.

A Central Computer System selection, in the form of six auxiliary-bit pulses, enters the CD selection circuits and, depending on the coding of these pulses, produces d-c levels which are used to select the test. Two selections are available in display field testing: one for the DD field, called the DD-test-select level; another for the SD (RD and TD) fields, called the SD-test-select level. The selection level enters the computer-test-control circuit, where it is used in conjunction with a start-read pulse from the computer via the CD-read-write-control circuit to form a test-read d-c level. These same conditions produce the SD-test level and computer-test-start-TD pulse, for SD testing, and the DD-test level and start-DD-test pulse, for DD testing. The test-read level conditions the computer-test-read switch to pass data from the OD read circuit to the Central Computer System via the OR circuit and the CD-read-bus-output circuit. In normal operation, the data goes from the CD read circuit to the Central Computer System via the OR circuit and CD-read-output circuit. When SD testing has been selected, the resulting computer-test-start-TD pulse and the SD-test d-c level start the SD (TD and RD) OD-read-control circuits. The read-control circuits provide read-sample pulses in the normal OD reading patterns of these fields. Similarly, selection of the DD test provides the start-DD-test pulse and the DD-test d-c level, which start the DD-OD-read-control circuit, thus providing read-sample pulses in the normal OD reading pattern of the DD field. The read-sample pulses are used in the OD read circuits to transfer data to the computer-test-OD-read switch. The read-sample pulse also goes to the computer-test-read-switch circuit, where it is converted into the computer-test-compare signal. This computer-test-compare signal goes to the CD-read-write-control circuit, where it is converted into both an IO-buffer-loading pulse and a compare pulse. The IO-buffer-loading pulse notifies the Central Computer System that a word is being transferred to it. A compare pulse requests the Central Computer System to compare the word read on the OD side of the drum with the word previously written on the CD side.

When all information programmed into the DD field or the SD (TD and RD) fields has been read, the Central Computer System sends a computer-disconnect pulse to the CD-read-write-control circuit. The computer-disconnect signal is converted into a read-write-reset pulse, which clears the computer-test-control circuit, ending the test.

During these tests, the data from the OD side is read to the Display System as well as to the Central Computer System. No data is read on the CD side of the fields.

The information read from the OD side of the display drum fields is compared with the information previously written on the CD side of the drums to make

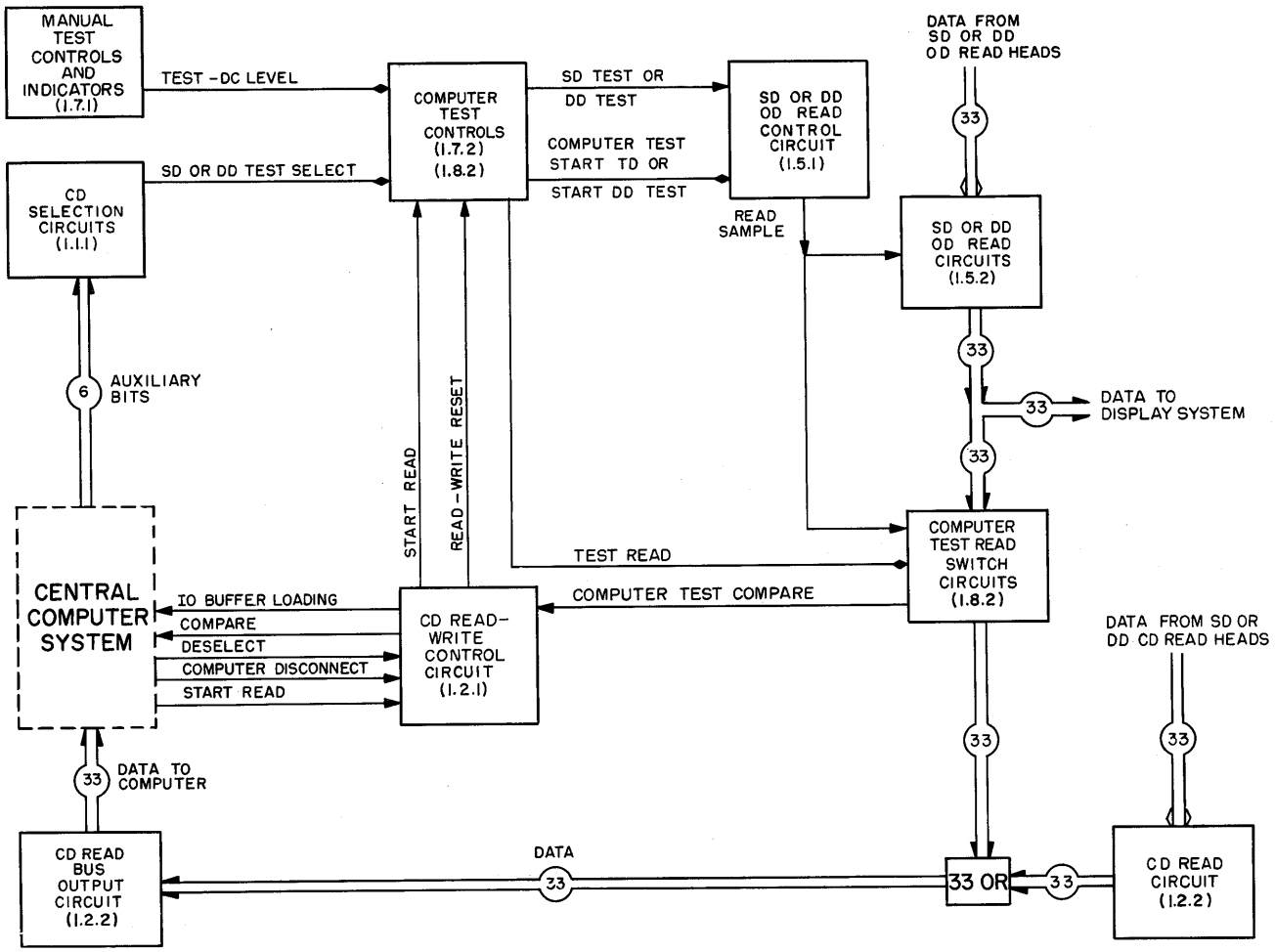


Figure 5–2. Display Fields Computer Test, OD Read, Block Diagram

certain that no changes have occurred in the transfer. Comparison is made by means of identification bits inserted into the programmed words.

2.2.1 Situation Display Computer Test

As in other computer tests performed by the computer-test circuits, a +10V test level is supplied to the computer-test-control circuit. A deselect pulse from the Central Computer System is sent to the CD-read-write-control circuit, where it is converted into a read-write-reset pulse (fig. 5–3). The read-write-reset pulse is used in the computer-test-control circuit to clear FF's 1 (test read), 2 (sync), and 3 and 4 (SD start circuit). This conditions the control circuits to accept operational instructions from the Central Computer System.

Selection of SD testing by commands from the Central Computer System causes an SD-test-select level to be generated in the CD selection circuits and sent to the computer-test-control circuit. A start-read pulse is then received from the Central Computer System via the CD-read-write-control circuit. The start-read pulse creates a 1 output at FF 1 which combines with the SD-test-select level, the 0 level of FF 2, and the test d-c level in AND 2 to produce an SD-pretest level. The SD-pretest level activates GT 1 in the SD start circuit, passing an OD 1 timing pulse to set FF 3 to the 1 side. The 1 output of FF 3 conditions GT 2 to pass the second OD 1 pulse for use as the computer-test-start-TD pulse. This same OD 1 timing pulse is also used to clear FF 3 and to set FF 4 to the 1 side, thus activating GT 3. Gate 3 passes the OD 2 timing pulse following the second OD 1 pulse. This gated OD 2 pulse is used to clear FF 4 and, as a reset-TD pulse, to clear the RD-read-control circuit to prepare it for operation.

The computer-test-start-TD pulse (OD 1) starts the TD-OD-read-control circuit in its precessed reading operation. At the same time, this pulse sets FF 2 to the 1 side. The output of FF 2, combined with the SD-test-select level and the test d-c level in AND 1, produces the SD-test level. This SD-test level activates the SD

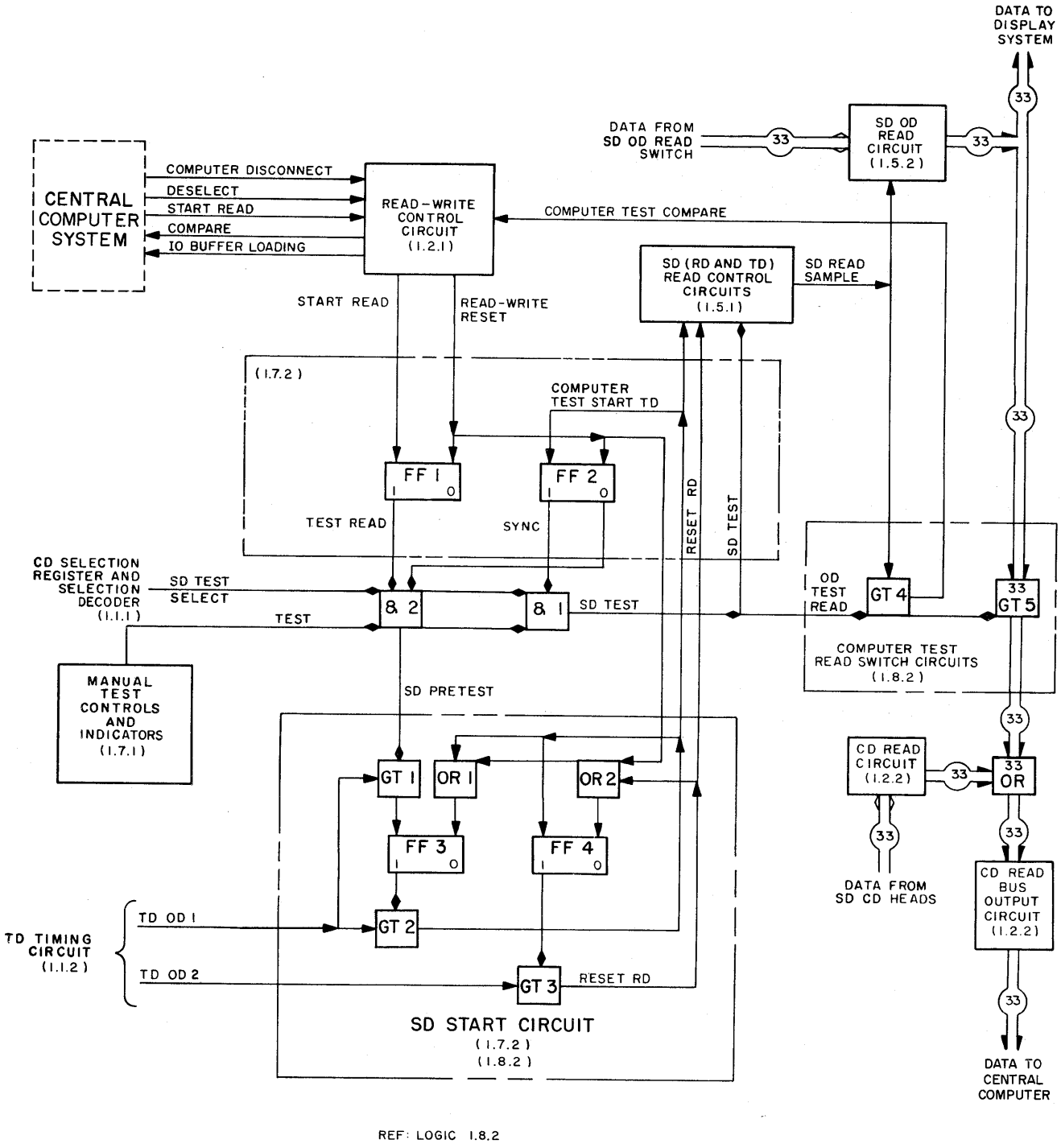


Figure 5–3. Display Fields Computer Test, SD Read, Simplified Logic Diagram

(RD and TD) read-control circuit to produce SD-read-sample pulses, which go to the SD OD read circuit. There, the read-sample pulses are used to transfer data to the computer-test-read-switch circuits. The SD-read-sample pulses also branch off and go to the computer-test-read-switch circuit. Read-sample pulses are produced according to the precession pattern for TD OD reading. Thus, 12 slots of 8 consecutive registers each are skipped, and the 13th is read. This process continues for 13 revolutions per field in order to read all the field registers. After all six TD fields are read, eight of the nine RD fields are read by the precession scheme

for these fields. In this pattern, one register is read and five consecutive registers are skipped. This action goes on until all registers in a field are read, which occurs in six revolutions. The other seven fields are then read in order.

The SD-test d-c level also goes to the computer-test-read-switch circuits as the OD-test-read level. The OD-test-read level conditions GT 5 (one of 33 similar gates) in the computer-test-read-switch circuits to pass data from the SD OD read circuit to the Central Computer System via OR 3 and the CD-read-bus-output circuit. In addition, the OD-test-read level activates GT 4 in the computer-test-read-switch circuits to pass SD-read-sample pulses from the SD (TD and RD) read-control circuits. These gated read-sample pulses are sent to the CD-read-write-control circuit as computer-test-compare pulses. A computer-test-compare pulse is converted in the CD-read-write-control circuit into an IO buffer-loading pulse and a compare pulse.

During SD computer tests, the information read is also sent to the Display System. Because of the absence of a selection level, no reading is done on the CD side of the selected fields at this time.

When all the programmed information on the SD (TD and RD) fields has been read, the Central Computer System sends a computer-disconnect pulse to the CD-read-write-control circuit. This signal forms a read-write-reset pulse, which clears the computer-test-control circuit flip-flops, thus stopping the test.

The words read from the OD side of the display drum fields are compared in the Central Computer System with the words previously written on the CD side of the drums to make certain that no changes have occurred in the transfer. Word comparison is made by means of identification bits inserted into the words originally written on the drums by the Central Computer System.

2.2.2 Digital Display Computer Test

In computer tests of the DD fields, the +10V test level is first supplied and a deselect pulse from the Central Computer System is sent to the CD-read-write-control circuit, where it is converted into a read-wire-reset pulse (fig. 5–4). The read-write-reset pulse is used in the computer-test-control circuit to clear FF's 1 and 2. The computer-test-control circuit is now conditioned to

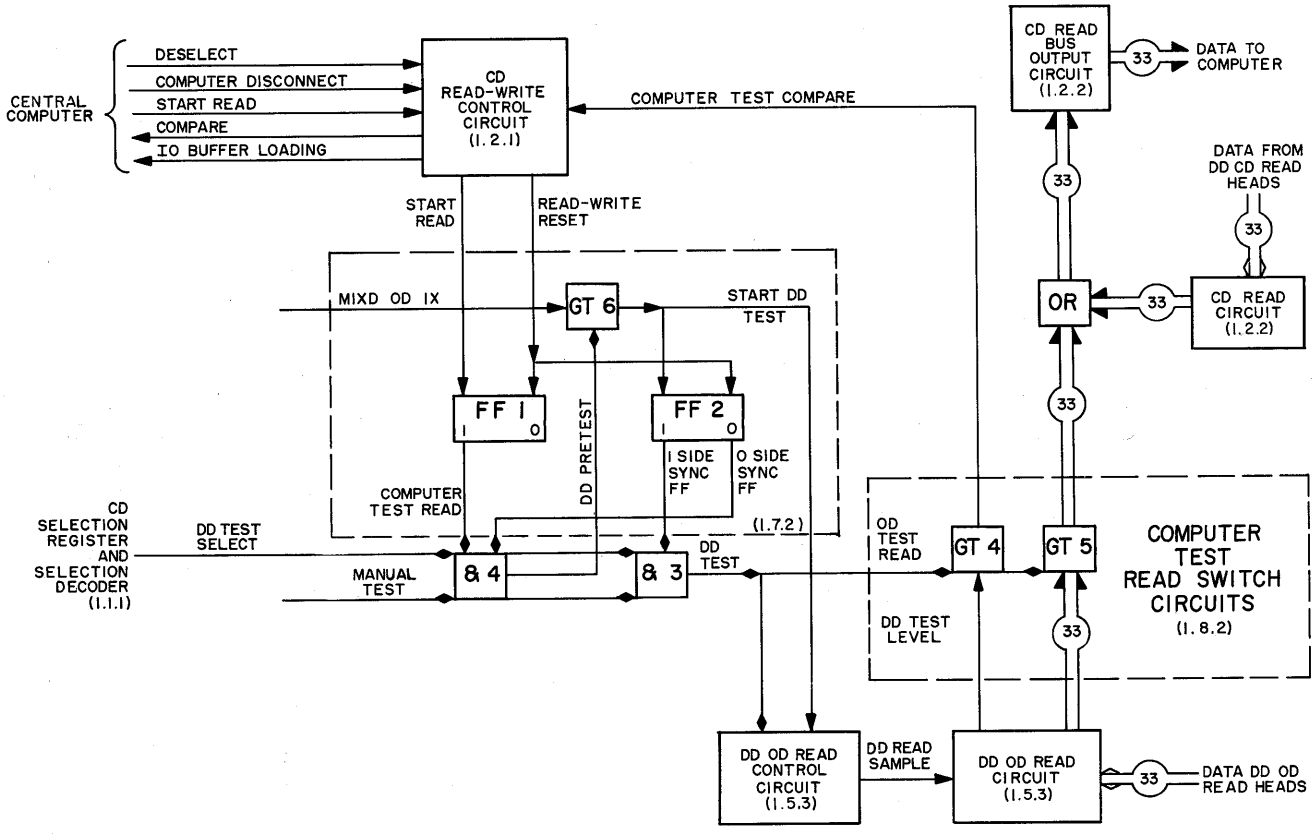


Figure 5–4. Digital Display Field Computer Test, Simplified Logic Diagram

accept operational instructions from the Central Computer System.

Selection of DD testing by commands from the Central Computer System causes a DD-test-select level to be generated in the CD selection circuits and sent to the computer-test-control circuit. In the same manner as that described in 2.2.1 for the SD-pretest level, the DD-pretest level is produced at AND 4. The DD-pretest level conditions GT 6 to pass MIXD-drum-OD-index pulses to form start-DD-test pulses. The start-DD-test pulse goes to the DD-OD-read-control circuit to start its precession reading operation. In addition, the start-DD-test pulse is sent to FF 2 to set it to the 1 side. The 1 output of FF 2 combines with the test d-c level and the DD-test-select level in AND 3 to form the DD-test level. This DD-test level then activates the DD-OD-read-control circuit to produce DD-read-sample pulses, which go to the DD OD read circuit. There the DD-read-sample pulses are used to transfer data to the computer-test-read-switch circuits. The DD-read-sample pulse also braches off and goes to the computer-test-read-switch circuits as the DD-test level.

Digital-display-read-sample pulses are produced according to the precession pattern for DD OD reading. Thus 63 registers are skipped, and the 64th is read. This pattern is continued for a total of 64 drum revolutions in order to read all registers on the DD field.

The DD-test level branches off and is sent to the DD OD read circuit. The remainder of the DD computer test is the same as the SD computer test described in 2.2.1.

2.3 IC FIELD COMPUTER TEST

2.3.1 Overall Description

Intercommunication-field-computer-test circuits enable the Central Computer System to read the OD side of the IC field. Test words previously written on the CD side of these fields by the Central Computer are compared in the Central Computer System with the test words read from the OD side to make certain that they have not changed during transfer.

The IC OD operate circuits normally read data from the OD side of the drum and transfer the data to the standby Drum System. During IC field computer tests, a signal path is provided which permits the Central Computer to read the OD side of the IC field. The computer test is initiated when the computer-test-control circuit (fig. 5–5) is conditioned by a test d-c level from the manual-test circuits. To start a reading operation on the OD side, the Central Computer System sends a deselect pulse to the CD-read-write-control circuit. In the CD-read-write-control circuit, the deselect pulse is converted into a read-write-reset pulse, which clears the flip-flops of the computer-test-control circuit. Clearing the computer-test-control circuit prepares the computer-test signal path to accept programmed operating instructions from the Central Computer System.

A Central Computer System selection, in the form of six auxiliary-bit pulses, enters the CD selection circuit and, depending on the coding of these pulses, produces d-c levels which are used to select the test. The selection level enters the computer-test-control circuit, where it is used in conjunction with a start-read pulse from the computer via the CD-read-write-control circuit to form a test-read d-c level. The test-read level conditions the computer-test-read switch to pass data from the IC OD read circuit to the Central Computer System via the CD-read-bus-output circuit. When IC testing has been selected, the resulting IC-own-test level serves to start the IC OD read circuits. The read circuits generate start-read-IC-own pulses, which, in conjunction with the IC-test level, enable MIXD OD 1 timing pulses to effect data transfers to the computer-test-read switch. Gated MIXD OD 3 pulses go to the read-write-control circuit, where they are converted into compare pulses. The MIXD OD 1 pulses are also converted in the CD-read-write-control circuit into IO-buffer-loading pulses, which serve to notify the Central Computer System that a word is being transferred to it. A compare pulse requests the Central Computer System to compare the word read on the OD side of the drum with the word previously written on the CD side.

When all IC field programmed information has been read, the Central Computer System sends a computer-disconnect pulse to the CD-read-write-control circuit. The computer-disconnect signal is converted into a read-write-reset pulse, which clears the computer-test-control circuit, ending the test.

2.3.2 IC Field Computer Test, Circuit Analysis

The IC field computer tests are initiated with the presence of a +10V test d-c level at the IC-test-control circuit (fig. 5–6). A deselect pulse from the Central Computer System is sent to the CD-read-write-control circuit, where it is converted into an IC-read-reset pulse. The IC-read-reset pulse serves to clear the master sync, computer-test-read, IC-other-sync, IC-other-read, and IC-other-compare flip-flops. This action conditions the control circuits to receive test control signals from the Central Computer System.

The IC-own-test (SEL 76) level, originated by Central Computer selection, is sent to the IC-test-control circuit. A start-read pulse is then received from the Central Computer System via the CD-read-write-control circuit. The start-read pulse connected to OR 3 passes through GT 5, which was previously conditioned by the IC-test level. The GT 5 output becomes a start-read-IC-own pulse. This pulse sets FF 3, thereby conditioning GT 6 to pass the following MIXD OD 1 pulse.

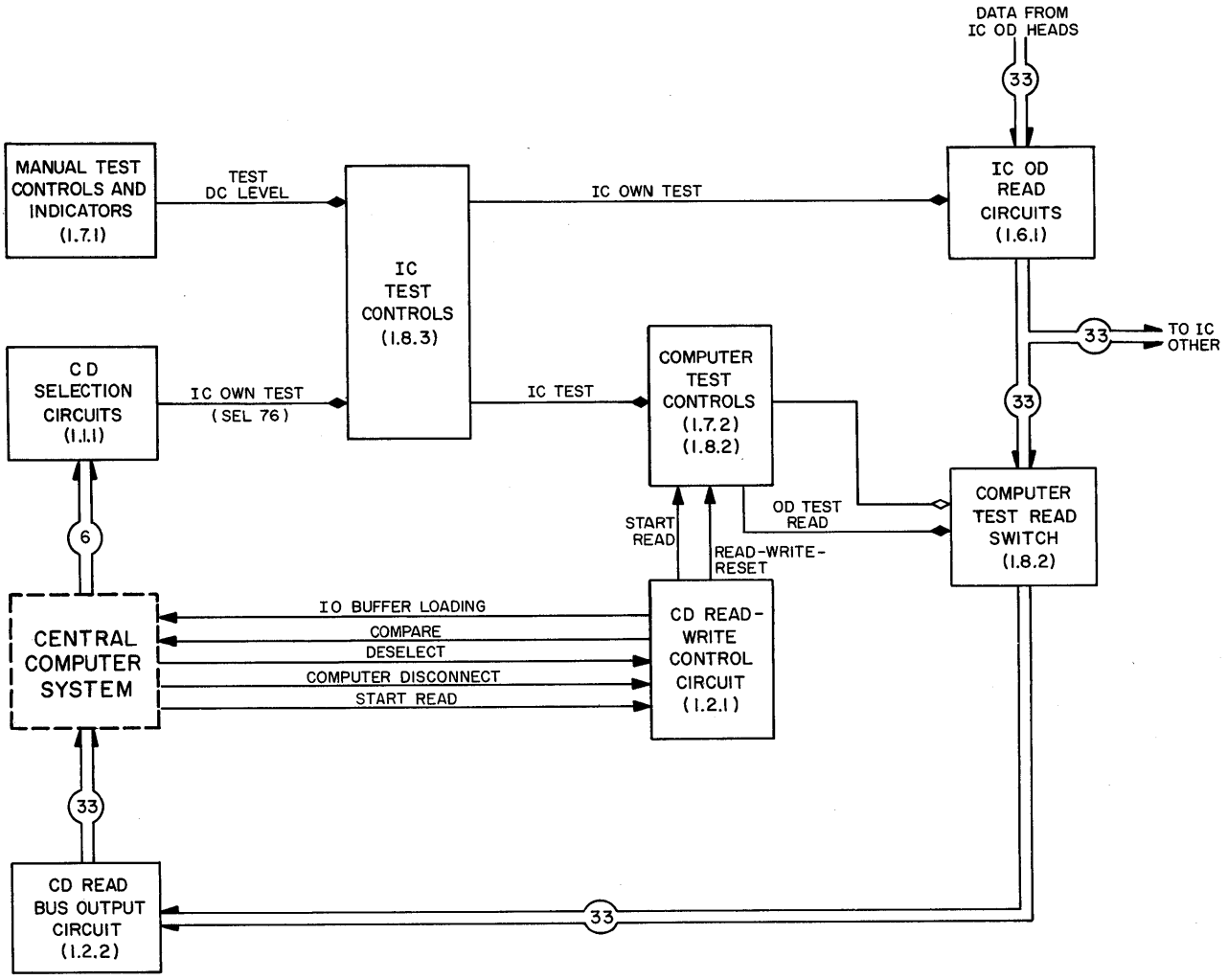


Figure 5–5. IC Field Computer Test, Block Diagram

This gated MIXD OD 1 pulse then sets FF 4, which, in turn, conditions GT 7 to pass the next MIXD OD 3 pulse. The gated OD 3 pulse is utilized as follows: FF 5 is set; GT 9 is sensed; FF 3 is reset through OR 4. The 1 output of FF 5 conditions GT 8 to pass the succeeding MIXD OD 1 pulse. At the same time, GT 9, which is conditioned by the not-manual-test and not-LRI-operate level, passes the MIXD OD 3 pulse, converting it into a compare pulse. The compare pulse is sent to the Central Computer System.

Five usec after gating the OD 3 pulse, the OD 1 pulse passes through GT 8. (Notice that FF 3 is cleared; GT 6 is not conditioned, thus blocking the passage of the OD 1 pulse at this point.) The gated OD 1 pulse from GT 8 senses GT's 10 and 11 and also passes through OR 5 to clear FF 4. Gate 10 is conditioned by the not-manual-test level; the gated OD 1 pulse becomes an IO-buffer-loading pulse. This pulse informs the Central Computer System that a word is being transferred.

The gated OD 1 pulse from GT 8 must pass through a set of relay contacts and a 0.7-usec delay prior to sensing the 33 gates symbolized by GT 11. The IC field relay contacts are closed when the Central Computer System is placed in the test mode at the duplex maintenance console. These relays also determine the information return to the Central Computer System rather than the transfer to the standby Drum System IC field (IC Other). The 0.7-usec delay serves to ensure that the IO-buffer-loading pulse reaches the Central Computer System before the transfer is effected. Thus, 0.7 usec after the generation of the IO-buffer-loading pulse, GT 11 is strobed. Consequently, the information transfer to the Central Computer System via the CD-read-bus-output circuit takes place. Not shown in the illustration are 33 additional gates which feed the CD-

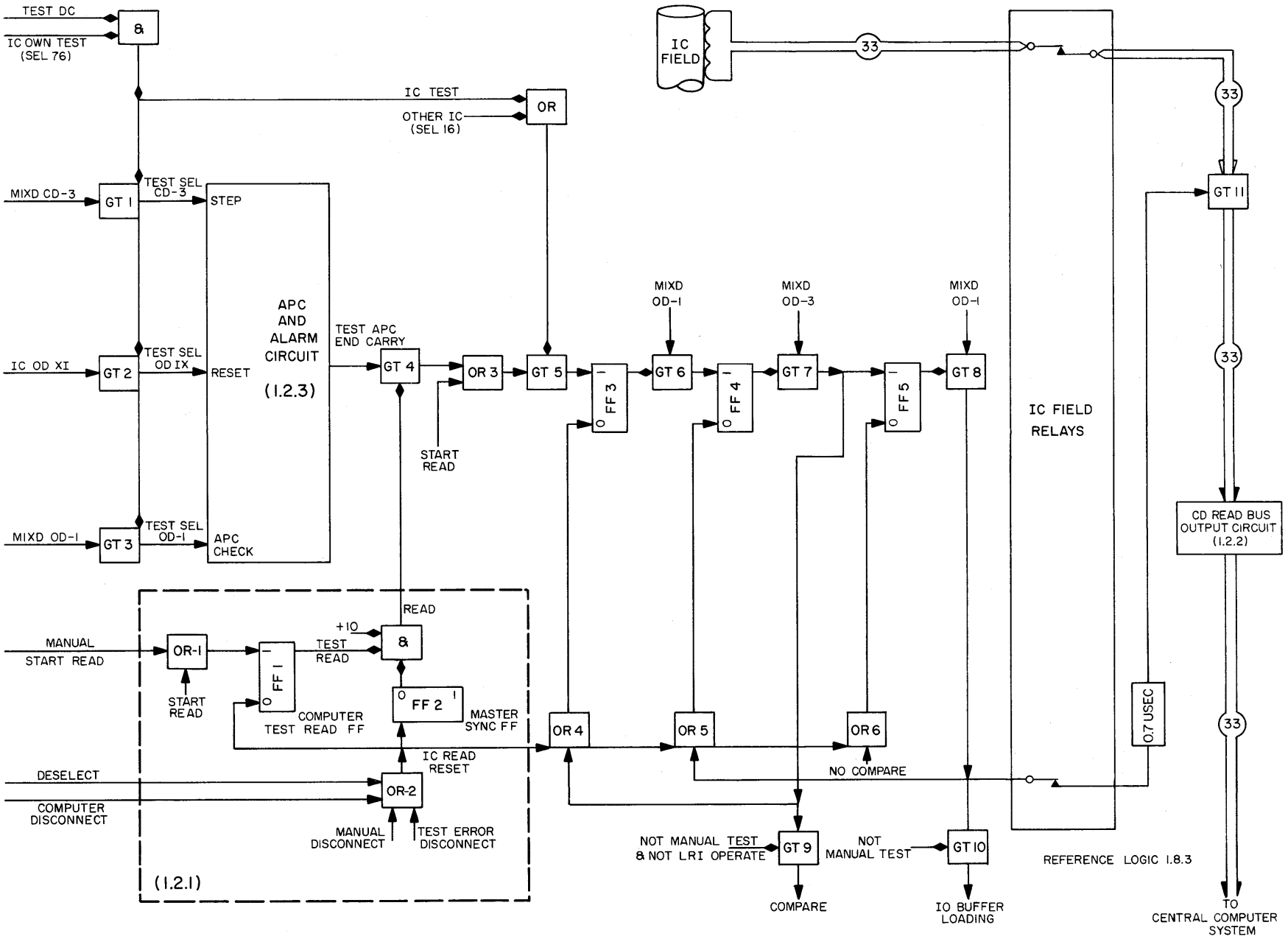


Figure 5–6. IC Field Computer Test, OD Read, Simplified Logic Diagram

read-bus-output circuit. These gates are conditioned by an OD-test-read level.

It should be noted that FF's 3 and 4 are cleared at this time, while FF 5 remains set. Therefore, IC test data transfers can continue to be effected a teach OD 1 time. This condition will remain until a no-compare pulse or a computer-disconnect pulse appears; either pulse will reset FF 5, thereby deconditioning GT 8. With GT 8 deconditioned, MIXD OD 1 pulses cannot be passed to effect a data transfer.

When a no-compare pulse appears, the corresponding register reading is inhibited. However, subsequent reading operations are effected by the MIXD CD 3, IC OD IX, and MIXD OD 1 timing pulses. These pulses are gated to form test-SEL CD 3, test-SEL OD IX, and test-SEL OD 1 pulses, which cause a test-APC-end-carry pulse output from the APC-and-alarm circuit. The test-APC-end-carry pulse senses GT 4, which is conditioned by a read level from the CD-read-write-control circuit. The read level is the result of the IC-read-reset and start-read pulses.

The gated test-APC-end-carry pulse then passes through OR 3 and senses GT 5. Gate 5 passes the pulse as a start-read-IC-own pulse, and the previously described reading operation is repeated. This cycle will continue until all the IC-test data has been read and a computer-disconnect pulse is received.

CHAPTER 3
STATUS FIELDS

3.1 INPUT FIELDS COMPUTER TEST

3.1.1 Overall Description

Input field computer-test circuits permit the Central Computer System to write programmed test words on the OD side of the drums. The test words are read afterward on the CD side of the drums and compared in the Central Computer System with the written test words to see whether any change has occurred in the transfer.

The circuits of the input fields of the Drum System normally write Input System information on the OD side of the drum fields. During computer tests on these fields, a test signal path is provided which allows the Central Computer System to write on the OD side of the drum fields. In the performance of computer tests, the computer-test-control circuit is first conditioned by a test level from the manual-drum-tester circuit (fig. 5–7). To initiate a writing operation on the OD side of the drums, the Central Computer System first sends a deselect pulse to the CD-read-write-control circuit. This pulse clears flip-flops in the CD-read-write-control circuit and, at the same time, is converted into a read-write-reset pulse. The read-write-reset pulse clears flip-flops in the computer-test-control circuit and in the selected OD-status-control circuit. The read-write-reset pulse is converted in the OD-status-control circuit into a write-register-reset pulse, which clears the selected OD write register. The computer-test signal path is now ready for programmed operating instructions from the Central Computer System.

A Central Computer System instruction, in the form of six auxiliary-bit pulses, enters the CD selection circuit, causing the generation of a d-c test-select level. When applied to the computer-test-control circuit, this level determines which field is selected for test. A start-write pulse from the Central Computer System goes to the computer-test-control circuit via the CD-read-write-control circuit. In combination with the test-select level, the start-write pulse results in the formation of the OD-drum-test-write level. This level goes to the computer-test-write-switch circuit and conditions it to pass data from the Central Computer System to the OD write registers. An IO-register-to-write-register pulse from the Central Computer System informs the CD-read-write-control circuit that a word has been transferred from the Central Computer to the computer-test-write-switch circuits and, therefore, to the selected OD write register. The pulse produces a write-register-full level, which is sent to the computer-test-control circuit. On receiving the write-register-full d-c level, the computer-test-control circuit generates the test-write-selected-field level, which conditions operations in the status-control circuit of the selected field.

Sensing an empty register by the selected status-control circuit produces a d-c level, which, when combined with the test-write-selected-field level, causes the production of a write pulse. The write pulse goes to the selected OD write register. The word in the selected OD write register is written on the drum, and the register is cleared in preparation for the next word. At the same time that the write register is cleared, a test-word-demand pulse is sent to the CD-read-write-control circuit via the computer-test-write switch to be converted into a word-demand pulse. The word-demand pulse goes to the Central Computer System to request another word. When all words programmed by the Central Computer System have been written, a computer-disconnect pulse from the Central Computer System clears the control circuits and write registers, stopping the test.

3.1.2 Input Fields Computer Test, Circuit Analysis

Circuits of the Drum System input fields are normally used by the Input System to write on the OD side of the drums. When computer tests are performed on the input fields, a test-signal path is provided which allows the Central Computer System to write on the OD side of the drums.

Before a computer test can be performed on the input element, a +10V test level is supplied to the computer-test-control circuit. This level is produced by setting the TEST-OPERATE switch on the maintenance console to the TEST position and switch S2 on the unit 21 test door to the DRUMS IN COMPUTER TEST position (figs. 5–1 and 5–8).

During test procedures, inverter 1 is cut off by the presence of the test level. This removes the operate level, which goes to the status-control circuit during normal operation.

The test is performed as follows: a deselect pulse is sent from the Central Computer System to OR 1 in the CD-read-write-control circuit. The OR 1 output is

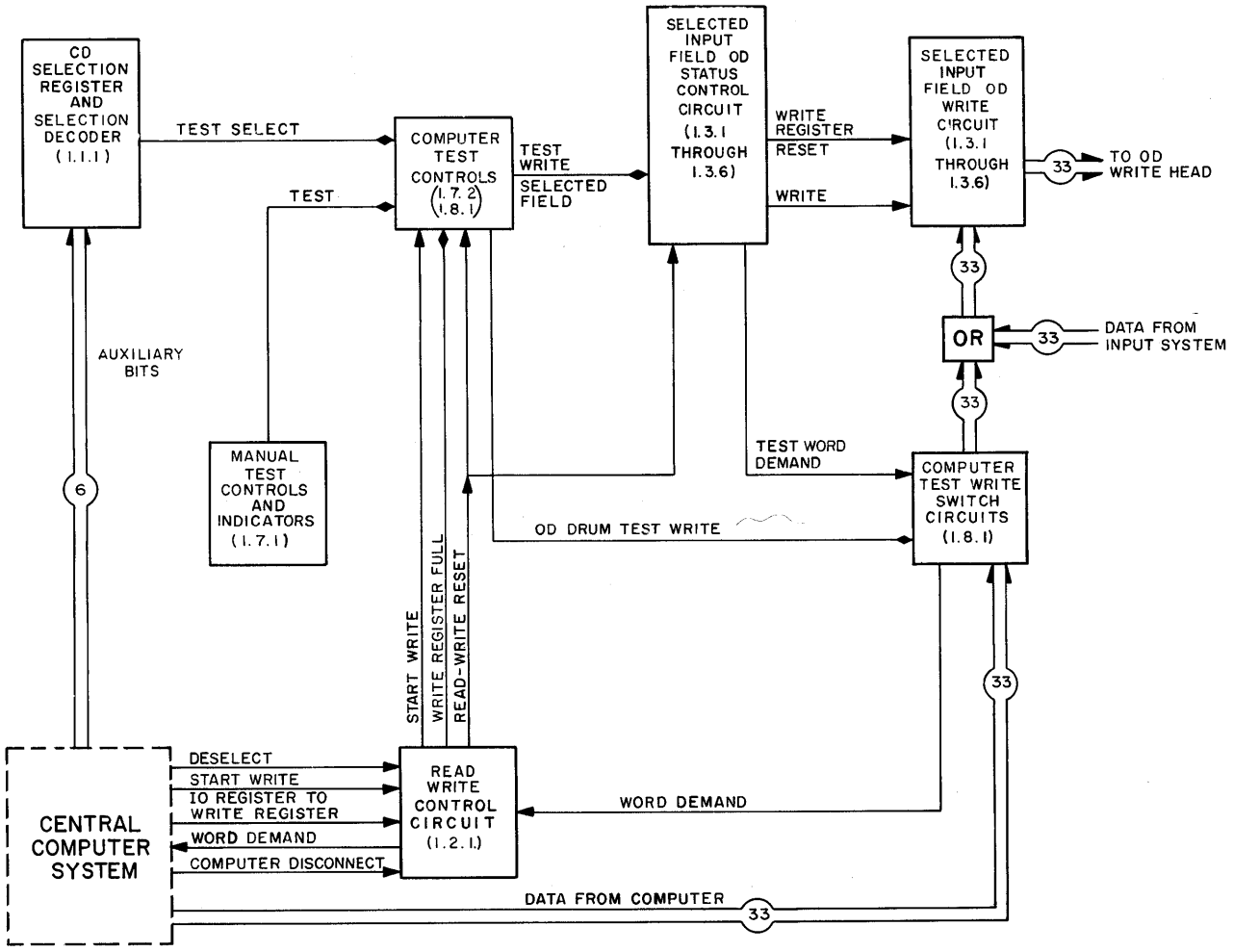


Figure 5–7. Computer Test of Input Fields Block Diagram

the read-write-reset pulse, which clears FF's 1 and 3 in the computer-test-control circuit. It also goes through OR 2 to clear FF 2 in the CD-read-write-control circuit. The test level, fed through the two test switches, conditions GT 1 to pass the read-write-reset pulse to the selected OD-status-control circuit as the computer-test-reset pulse. (This pulse is described later.)

Instructions from the Central Computer System, in the form of auxiliary-bit pulses, produce normal field selection in the CD selection circuits. The CD selection circuits produce the test-select-OD-input-field level, which is sent to AND's 1 and 3 in the computer-test-control circuit. A start-write pulse from the Central Computer System is also sent to the computer-test-control circuit and FF 1. The addition of the 1 output of FF 1 to the test level and the test-select-OD-input-field level causes AND 1 to form the test-write-select-drum-OD level. The test-write-select-drum-OD level goes to the computer-test-write-switch circuit and also provides one of the conditions for conduction in AND 2.

Flip-flop 2 in the CD-read-write-control circuit receives the IO-register-to-write-register pulse from the Central Computer System. The IO register-to-write-register pulse informs the CD-read-write-control circuit that a word has been transferred to the Drum System. A CD-write-register-full level is developed by FF 2 and sent to AND 2 in the computer-test-control circuit. The Central Computer System word is stored in the CD write register and, as will be seen, in all five OD write registers. In AND 2, the CD-write-register-full level is combined with the test level and the test-write-select-drum-OD levels to form the test-write-select-drum level. Since GT's 2 and 3 are now both conditioned, the next OD-index pulse from the selected timing circuit is passed to set FF 3 to the 1 side. The output of FF 3 is added in AND 3 to the test level and to the test-select-OD-input-field level, forming the test-write-selected-field level, which is sent to the selected OD-status-control circuit.

In this selected OD-status-control circuit (fig.

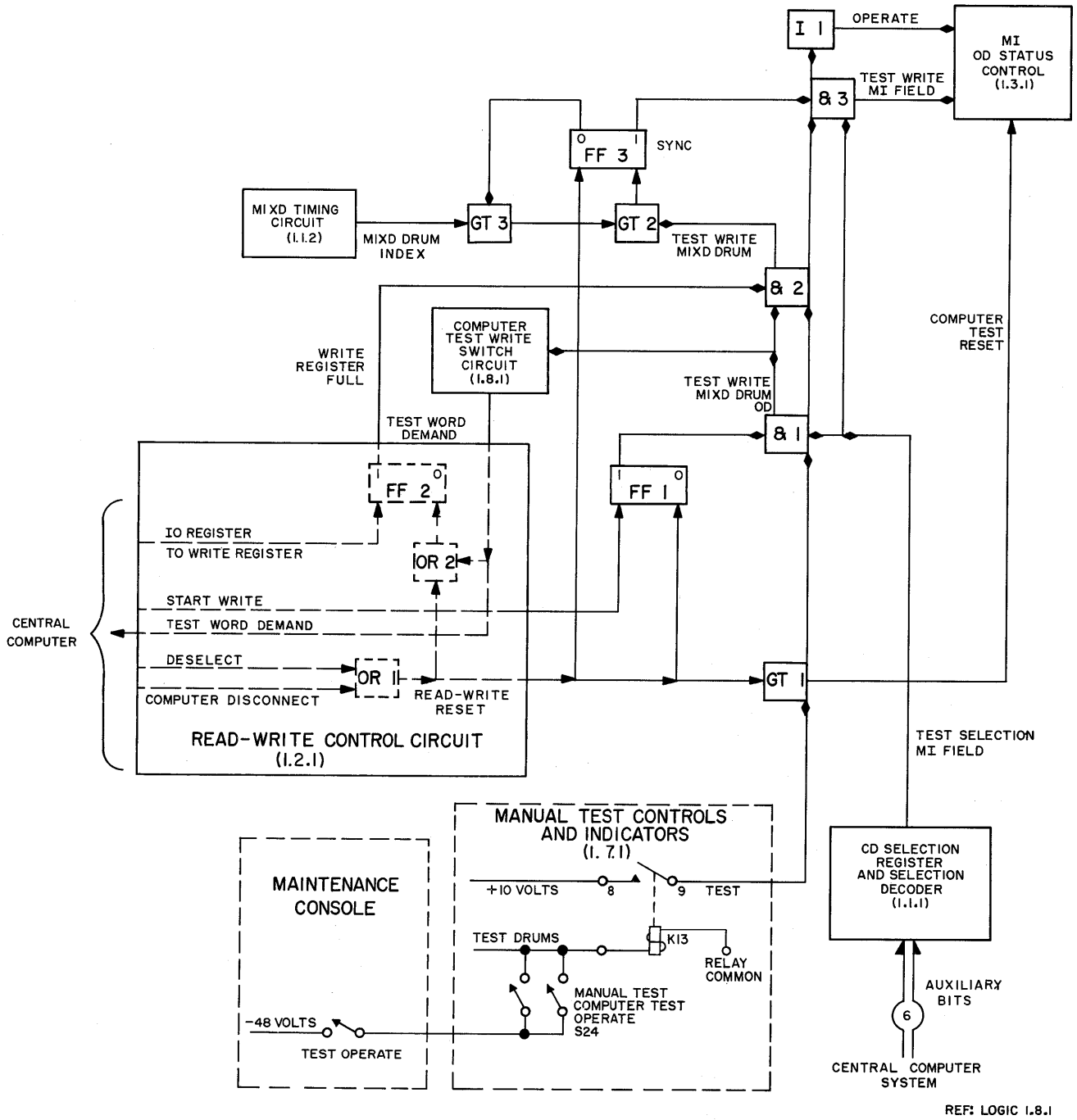


Figure 5–8. Computer Test Write Control for Input Fields, Simplified Logic Diagram

5–7), a computer-reset-write-register pulse clears the write register flip-flops of the selected OD write circuit. Thereafter, the Central Computer System places a word in the write register.

As the drum rotates, the first empty register is indicated by the detection of a 0 bit in the OD status channel of the selected OD-status-control circuit. When a 0 bit rather than a 1 bit is detected, the read circuit cannot condition GT 1 in time for this stage to pass the OD 1 pulse to FF 1. Flip-flop 1, which has been cleared by the preceding OD 4 pulse, remains cleared. The 0-state output of FF 1 conditions GT 2 to pass the next OD 3 pulse. This pulse is fed to both GT 3 and FF 2. In normal operation, the operate d-c level conditions GT 3 to pass the OD 3 (drum-demand) pulse, which is fed to the associated input circuits of the Input System.

The Input System then feeds a normal data-available pulse to FF 3. In the absence of the drum-demand pulse, the normal data-available pulse cannot be created. However, a test-data-available pulse is created as described below.

The 1 output of FF 2 combines with the output of the test-control circuit in AND 1. (During normal operation, the test-write-selected-field level is not present, so that the GT 4 output cannot operate FF's 3 and 4.) AND 1 conducts, placing a conditioning level at GT 4 that passes the next OD 2 pulse from the timing circuit. The gated timing pulse forms the test-data-available pulse, which substitutes for the data-available pulse normally received from the Input System. The test-data-available pulse, like the normal data-available pulse, sets FF 3, causing a 1 to be written in the CD status channel when the timing circuits develop a status-write-sample pulse.

The test-data-available pulse also sets FF 4 to condition GT's 5 and 6. At the next OD 3 input to the OD-status-control circuit, GT 5 produces a write pulse which causes the selected OD write circuit to write the write register contents onto the drum. At the next OD 4 pulse, GT 6 produces a test-word-demand pulse. The test-word-demand pulse is applied to GT 7 in the computer-test-write switch. If the test-write-select-drum-OD level from the computer-test-control circuit is still present, the test-word-demand pulse is gated to the CD-read-write-control circuit. From the CD-read-write-control circuit, it goes to the Central Computer System to request another word.

The test-word-demand pulse at the output of GT 6 is also used to produce a reset-write-register pulse. The reset-write-register pulse clears the OD write circuit, readying it to receive the word from the Central Computer System. The path of this new word can be traced in figure 5–9. When the test-word-demand pulse is received by the Central Computer System, it places the word in the CD write circuit and in the 33 data gates in the computer-test-write-switch circuits. For as long as the test-write-select-drum-OD level from the computer-test-control circuit remains present, the data gates are conditioned to pass the Central Computer System word to the data OR circuits. The data OR circuits receive inputs from the Input System during normal operation but, during test operation, receive the test word from the computer-write-switch circuits. The OR circuits place the test word in the MI-OD-write circuit so that it may be written the next time a 0 bit is detected in the OD status channel.

From here on, the input-fields-computer-test circuit operates as a normal status-controlled circuit. (Refer to 7.7.1 of Part 2.) Writing is continued until the Central Computer System has written the programmed number of words. A computer-disconnect pulse from the Central Computer System then clears FF's 1 and 3 in the computer-test-control circuit (fig. 5–8) and the write registers, ending the OD writing.

If a 1 is read in the OD status channel of the selected status-control circuit (fig 5–9), indicating a full register, the read circuit output will pass the OD 1 pulse through GT 1 to set FF 1. As a result, GT 2 will not be conditioned in time to pass the OD 3 pulse that starts the writing operation described above, and no writing will take place. Flip-flop 3, which has been cleared by an OD 4 pulse, remains cleared and causes a 0 to be written on the CD status channel, indicating that no word has been written.

The information written on the drum in this manner is read from the CD side of the drum by the normal-status-identification-controlled reading operation. In the Central Computer System, the word written on the OD side of the drum is compared with the word read on the CD side of the drum to ascertain whether the information has been correctly transferred.

Writing on the CD side of the drum during computer-test OD writing is stopped by lack of write pulses to the CD write register. Although the CD write register is full, the word cannot be transferred to the CD write heads.

3.2 OUTPUT BUFFER FIELDS COMPUTER TEST

3.2.1 Overall Description

Output buffer (OB) field computer-test circuits permit reading of the OD side of the OB fields by the Central Computer System. Words previously written on the CD side of these fields by the Central Computer are compared in the Central Computer System with those read from the OD side to determine whether the word content has changed in the transfer.

The circuits of the OB fields of the Drum System normally read the OB fields to the Output System from the OD side of the drum. For computer tests on the output fields, a test-signal path is provided which allows the Central Computer System to read the OD side of the drum fields. In the performance of computer tests on the OB fields, the computer-test-control circuit is conditioned by a d-c test level from the manual-test circuits (fig. 5–10). To start a reading operation on the OD side of the drums, the Central Computer System sends a deselect pulse to the CD-read-write-control circuit. The deselect pulse forms a read-write-reset pulse, which clears flip-flops in the computer-test-control circuit. The computer-test signal path for OD reading is ready for programmed operating instructions from the Central Computer System.

A Central Computer System instruction, in the form of six auxiliary-bit pulses, goes to the CD selection

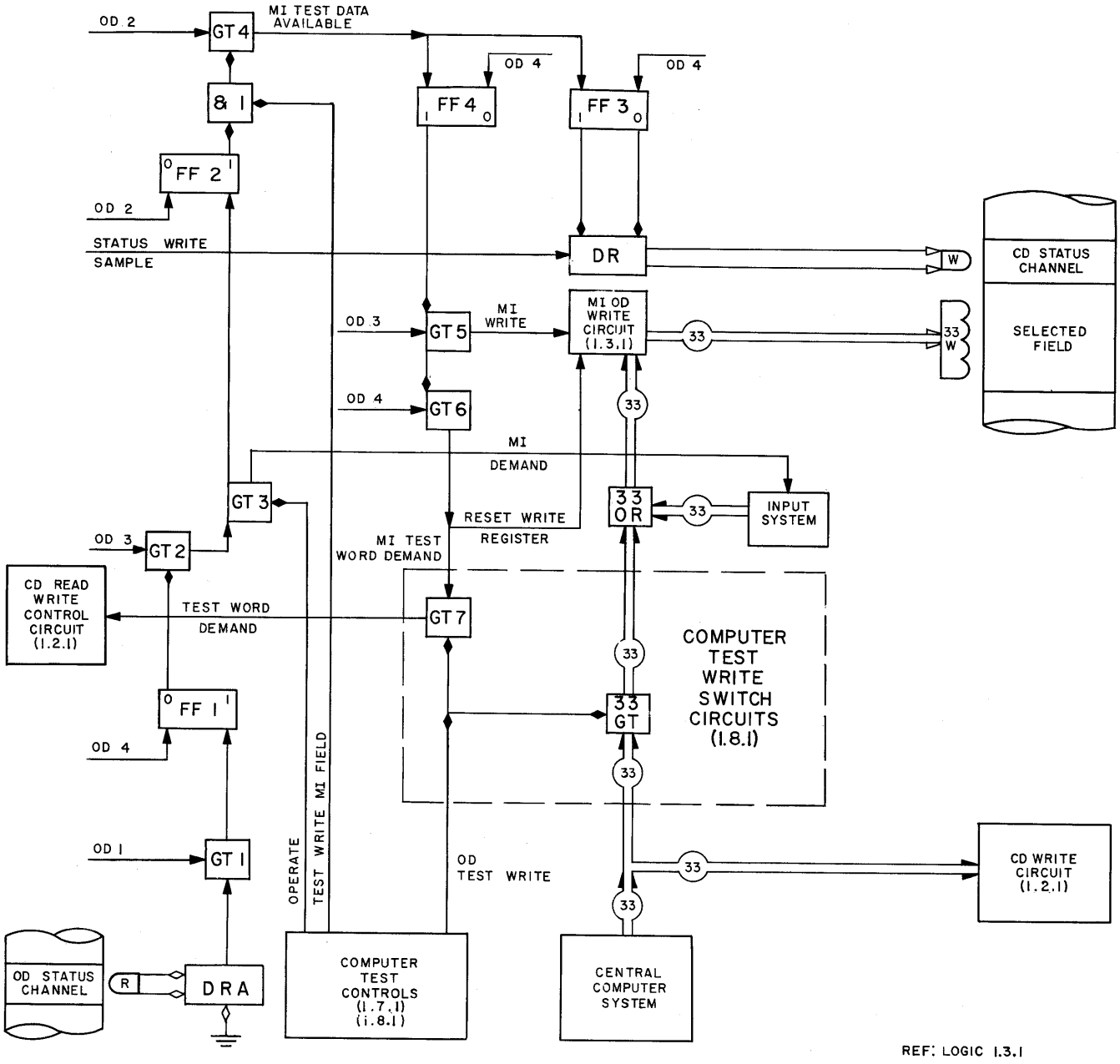


Figure 5–9. Input Fields Status Control Circuit in Computer Test Simplified Logic Diagram

circuits, producing a select-OB-odd-or-select-OB-even level. This level enters the OB field selection circuits, where it develops a select-OB level. The select-OB level is sent to the computer-test-control circuit, which it conditions to perform the OB computer test.

Before the actual test of the fields begins, the computer-test-control circuit enters a pretest phase. The pretest phase is initiated when a test-OD level is received from the OB field selection circuits. This level is produced when the OB field selection circuits have connected the read heads for field 3 to the OB OD read circuits. The heads are switched by applying an OB-OD-field-select level to selected heads via the OB-OD-field-select level to selected heads via the OB-OD-diode-switching circuit.

When counters in the OB field selection circuits determine that the next field (field 1) should be switched into the read circuit, an OB-switch-field pulse is developed. This pulse, in addition to enabling the selection of field 1, also goes to the computer-test-con-

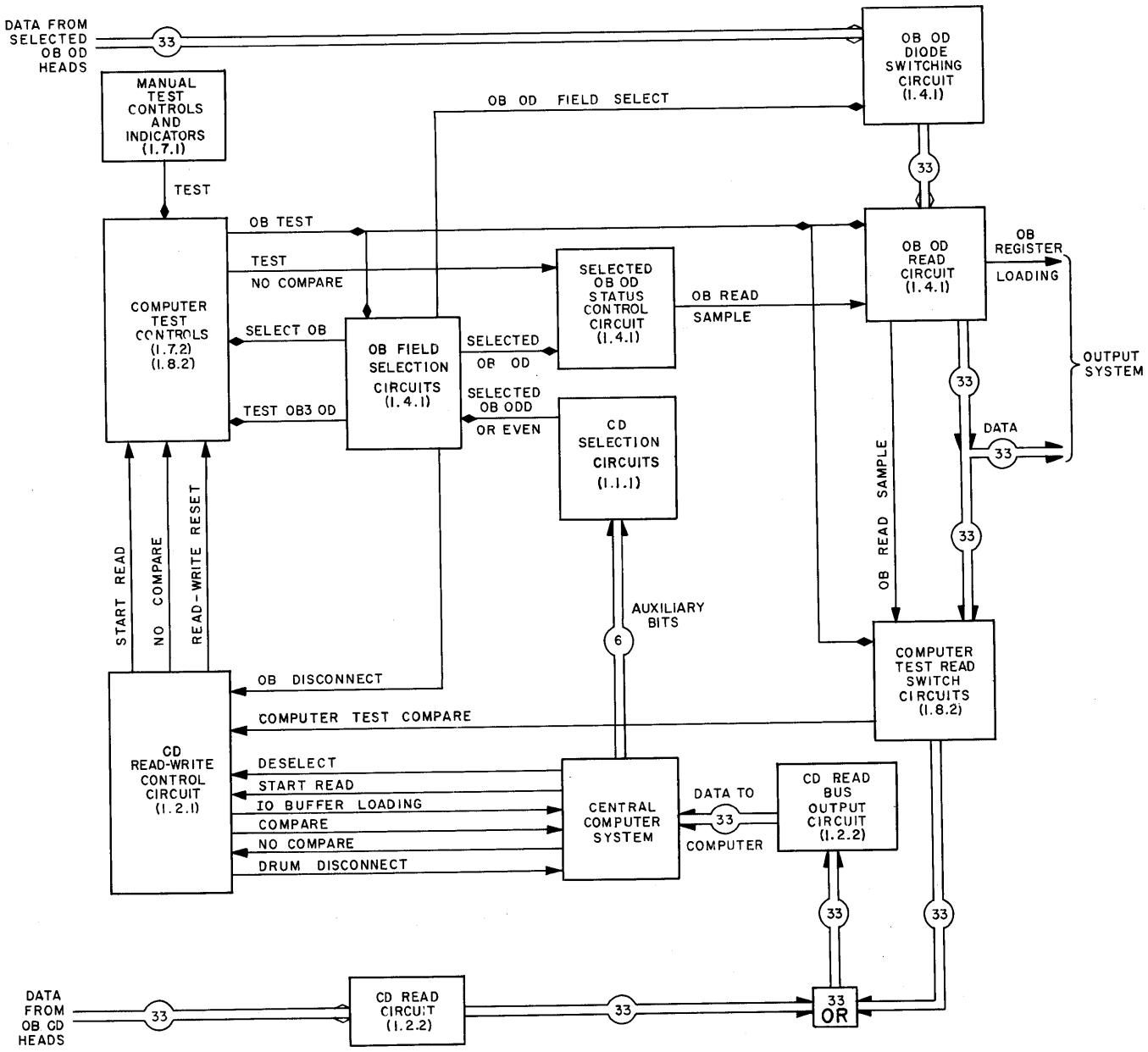


Figure 5–10. Output Buffer Fields Computer Test, OD Read, Block Diagram

trol circuit. In the computer-test-control circuit, it ends the pretest phase and begins the test phase of operation.

The test phase of operation is marked by the production of an OB-test level from the computer-test-control circuit. The OB-test level goes to the OB field selection circuits, conditioning the transmission of a select-OB-OD-selected level to the selected OB-OD-status-control circuit. The OB-test level also goes to the computer-test-read-switch circuits to open gates and to the OB-OD-diode-switching circuits to enable operation during test procedures.

In the selected OB-OD-status-control circuit that receives the select-OB-OD level, the presence of a word in a register of the selected OB field causes an OB-read-sample pulse to be generated. The OB-read-sample pulse is sent to the OB OD read circuit, where it is used to transfer data from the OB-OD-diode-switching circuit to the Central Computer System, via the OB OD read circuit, the computer-test-read switch, 33 data OR circuits, and the CD-read-bus-out-put circuits. Simultaneous reading of the CD side of the OB fields is prevented by lack of read-sample pulses to the CD read circuit.

The same read-sample pulse that produces OD reading branches in the OB OD read circuit and goes to the computer-test-read switch, where, in conjunction with the OB-test level from the computer-test-control circuit, it forms a computer-test-compare pulse. The computer-test-compare pulse goes to the CD-read-write-control circuit. There it is converted into IO-buffer-loading and compare pulses, which inform the Central Computer System that a word has been read that should be compared with the word previously written. Data also goes to the Output System but is not accepted there because the OB-register-loading pulse is absent during computer tests. No-compare pulses from the Central Computer System are fed to the computer-test-control circuit, causing the production of the test-no-compare signal. The test-no-compare pulses enter the selected OB-OD-status-control circuit and prevent the writing of other data in the registers read. This preserves the data written on the drum.

When the 2,048 registers of OB field 1 (the first field selected) have been sampled, OB-switch-field pulses transfer operations to OB fields 2 and 3 in turn. The reading operations for the latter two fields are the same as for field 1. After all programmed information has been read, a disconnect pulse is received from the Central Computer System. This pulse goes to the CD-read-write circuit and is converted into a read-write-reset pulse. The read-write-reset pulse accomplished the disconnecting operation by clearing the counter-test-control circuit. Clearing the computer-test-control circuit removes the OB-test level, preventing the production of field selection levels for use in the OD-status-control circuits.

3.2.2 Output Buffer Fields Computer Test, Circuit Analysis

During normal operation, the circuits of the OB fields of the Drum System read data from the OD side of OB fields to the Output System. During computer testing, a signal path is provided to read this data into the Central Computer System.

Before computer tests can be made on the output fields, the test level is supplied to the computer-test-control circuit. The test circuits are now ready to act on programmed instructions from the Central Computer System.

A deselect pulse from the Central Computer System is sent to the CD-read-write-control circuit, where it is converted into a read-write-reset pulse (fig. 5–11). The read-write-reset pulse clears FF's 1 and 2 in the computer-test-control circuits.

A select-OB-odd or select-OB-even d-c level is produced in the CD selection circuit as the result of decoding the selection indicated by the six auxiliary-bit-pulse signals from the Central Computer System. The selection level produced in this manner goes to the OB-CD-field-and register-switch-control circuit, developing a select-OB level which goes to AND's 1 and 2 in the computer-test-control circuit.

A start-read pulse from the Central Computer System, via the CD-read-write-control circuit, sets FF 1, producing a test-read level, which goes to AND 1. Four of five conditions necessary to conduction in AND 2 are present in the test, select-OB, 0-side-sync-flip-flop (from FF 2), and test-read levels. The fifth level, the test-OB-3-OD level, is produced in the manner described below.

The OB field switch counter (OB and CD) counts 12 CD 1 timing pulses after each CD-index pulse from the LOG timing circuit. At the 12th pulse counted, a CD-OB-operate level is developed which goes to the OB-OD-field-switch circuit. In the OB-OD-field-switch circuit, the CD-OB-operate level causes the production of an OB-field-selection level which goes to the center taps of the read heads of the selected OB field via the OB-OD-diode-switching circuit. At each occurrence of the CD-OB-operate level, the field selection changes to the next highest numbered OB field. When the OB-OD-field-3-select level is produced, the test-OB-3-OD level is produced and sent to AND 1. (The operation of the OB-OD-field-switch circuit is described in detail in Ch 3 of Part 4.)

Conduction in AND 1 of the computer-test-control circuit produces an OB-pretest conditioning level at GT 1. At the next index pulse received by the OB-field-switch counter (OD and CD), an OB-switch-field pulse is developed which changes the selection level produced by the OB-OD-field-switch circuit to select-OB-field 1. The OB-switch-field pulse also goes to GT 1 in the computer-test-control circuit. It is passed by the OB-pretest level to set FF 2. With FF 2 in the 1 state, a 1-side-sync-flip-flop level is added to the select-OB-level (from the OB-field-and-register-switch-control circuit) and to the test level at AND 2. This produces an OB-test level at the output of AND 2. The OB-test level goes to GT 2, to the OB OD read circuit, to the gates in the computer-test-read-switch circuit, and to the OB-OD-field-switch circuit.

In the OB-OD-field-switch circuit, the OB-test level substitutes for the operate level produced by inverter 1 when the Drum System is in normal operation. The OB-test level, therefore, enables the OB-OD-field-switch circuit to produce a select-OB-OD level, which is sent to the selected-OB-OD-status-control circuit (in this case, for OB field 1) when an OB-operate level from the OB-field-switch counter is present. The OB-operate level is present during the reading of each field. Its

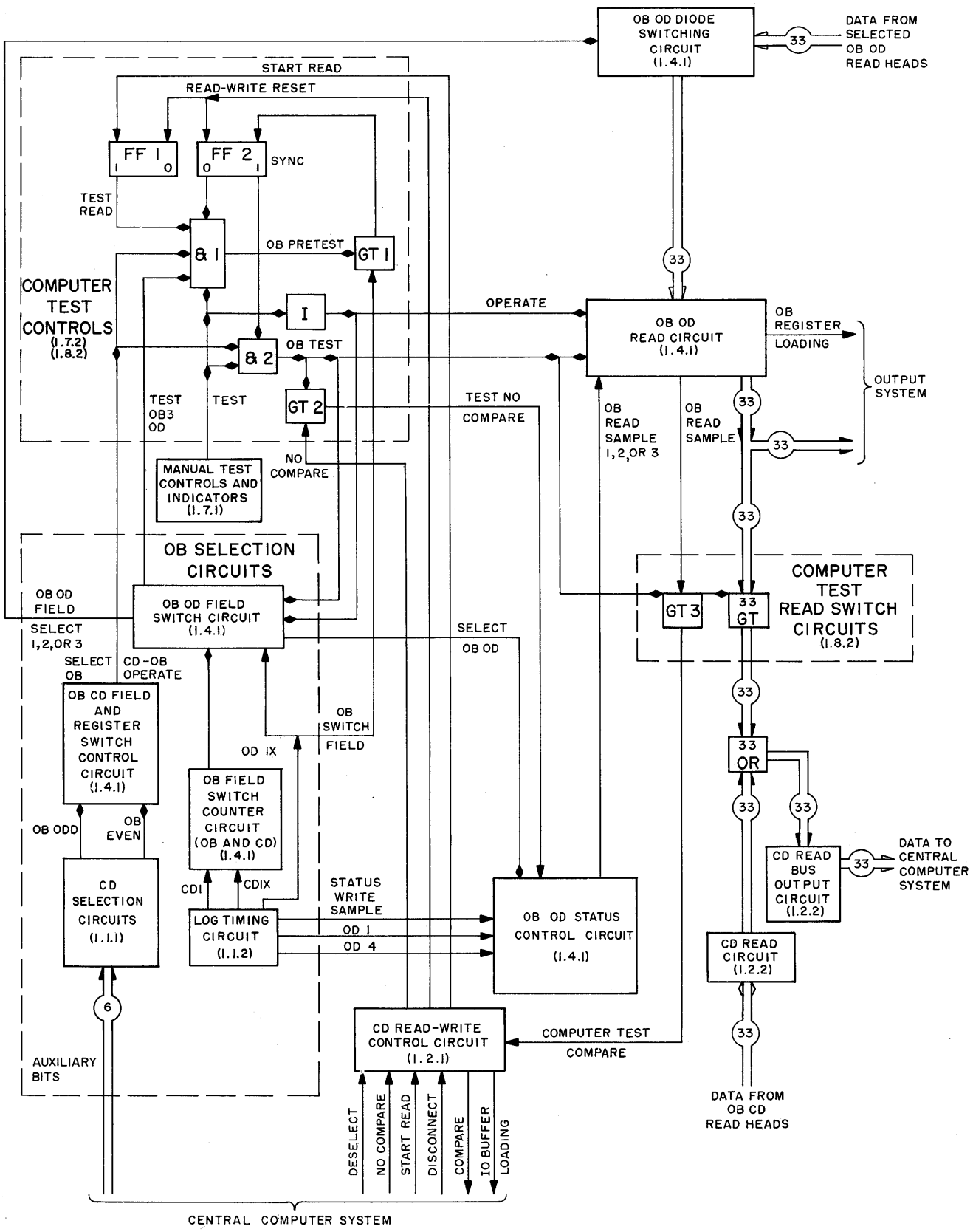


Figure 5–11. Computer Test for OB Fields, Simplified Logic Diagram

absence for 120 μsec after field switching is necessary to provide sufficient delay for transients to die out.

The select-OB-OD level, sent to the selected OB-OD-status-control circuit, enables that circuit to function as though operation is normal. When a full register is sensed, a read-sample pulse is sent to the OB OD read circuit. In the OB OD read circuit, the read-sample pulse is used in the gating of data from the OB-OD-diode-switching circuit to the computer-test-read-switch circuits and is itself sent to GT 3 in the computer-test-read-switch circuits.

In the computer-test-read-switch circuits, the OB-test level conditions GT 3 to pass the read-sample pulse as a computer-test-compare pulse. The computer-test-compare pulse goes to the CD-read-write-control circuit. In the CD-read-write-control circuit, the computer-test-compare pulse branches and is sent to the Central Computer System as an IO-buffer-loading pulse, which informs the Central Computer System of the word transfer, and as a compare pulse, which requests the Central Computer System to compare the identification bits of the words read with those of the words previously written.

Data pulses entering the computer-test-read-switch circuits pass through 33 data gates, which are conditioned by the OB-test level. After being passed through the computer-test-read-switch circuits, the data goes to the CD-read-bus-output circuit via 33 data OR circuits and is sent to the Central Computer System. Data is also read to the Output System but cannot be accepted there because the OB-register-loading pulse, formed from the read-sample pulse in normal operation, is not developed. This OB-register-loading pulse is formed when the operate level from inverter 1 in the computer-test-control circuit is present.

To prevent the writing of new words on the registers being read, the Central Computer System sends a no-compare signal to the CD-read-write-control circuit. From this circuit, the pulse goes to the computer-test-control circuit, where it is passed through GT 2 by the OB-test level as the test-no-compare pulse. The test-no-compare pulse is applied to the selected OB-OD-status-control circuit, where it is passed through GT 2 by the CD status channel. This prevents the writing of a new word in the register involved. As a result, the information written on the OB fields during computer tests is preserved and can be used again.

In this way, reading proceeds through each of the three OB fields in the sequence of field 1, field 2, and field 3. When all the programmed information in the three fields has been read, the Central Computer System produces a disconnect pulse which goes to the CD-read-write-control circuit, forming a read-write-reset pulse. This read-write-reset pulse clears FF's 1 and 2 in the computer-test-control circuit to end the test.

Information read to the computer from the OD side of the OB drum fields is compared with information previously written on the CD side of these fields to ascertain whether the information has been correctly transferred. Comparison is made by means of identification bits inserted into the programmed words.

Transfer of words read on the CD side of the drum to the Central Computer System is prevented by lack of read-sample pulses from the CD-read-write-control circuit.

CHAPTER 4
MANUAL TEST CIRCUITS

4.1 GENERAL

Manual-test circuits serve to check the operation of the Drum System and to isolate the system from all other data-handling systems of the equipment. Individual logic circuits are provided for each of the two drum groups: main drums manual control logic 1.7.1 and 1.7.2; auxiliary drums manual control logic 1-2.3.1. Main drums manual tests are conducted at the test door in module 21L; auxiliary drums manual tests are conducted at the test door in module 20D.

Although the manual-test circuits in each group are distinguished by individual logic, the nature of the fields to be tested determines the circuit differences. Therefore, all addressable fields manual-test circuits in the main or auxiliary drums are identical; these circuits are discussed in 4.2 through 4.2.9. The erase, timing, and index-channel-rewrite circuits are also identical for each group and are described in 4.3 through 4.3.3.

The manual-test circuits which are not identical for all drums are specifically provided in the main drums for status fields. These circuits are discussed in 4.4 through 4.4.6.

4.2 OVERALL MANUAL TESTS

4.2.1 Begin-Manual-Test Circuit

All manual tests on the Drum System must start with the operation of controls related to the begin-manual-test circuit (fig. 5–12). A—48V level is transmitted from the maintenance console to the begin-manual-test circuit when the TEST-OPERATE switch in module E of the maintenance console is in the TEST position. When TEST MODE SELECTION switch S2 on the test door of module 21L is set to the DRUMS IN MANUAL TEST position, the —48V level energizes the coil of relay K6. When K6 is energized, its 1 and 2 contacts close and energize K4, thus completing the circuit to the computer-test-control circuit, where the +10V serves as a test level. The +10V level also passes through the closed 3 and 4 contacts of K6 to several manual-test circuits, where it is used as a manual-test level.

Simultaneously with the formation of the test and manual-test levels, a d-c ground level is brought through closed K4 contacts 5 and 6 to the normally open SINGLE PULSE pushbutton, S35. This button is located on the test door of module 21L (fig. 5–1). When S35 is depressed, the d-c ground is applied to the pulse generator, causing the production of a single 0.1-μsec pulse. This pulse appears at the SINGLE PULSE jack, J8, for use in test procedures requiring a single standard pulse.

4.2.2 Manual-Test-Field-Selection Circuit

Whenever a manual test begins with the operation of switch S2 in the begin-manual-test circuit described above, it is necessary to select the field to be tested. This is done by the operation of controls in the manual-test-field-selection circuit (fig. 5–13).

Initially, DESELECT pushbutton S24 is depressed, applying a test ground level to the input of the pulse generator through the normally open contact of S24 unit 1. Switch S24 is on the module 21L test door.

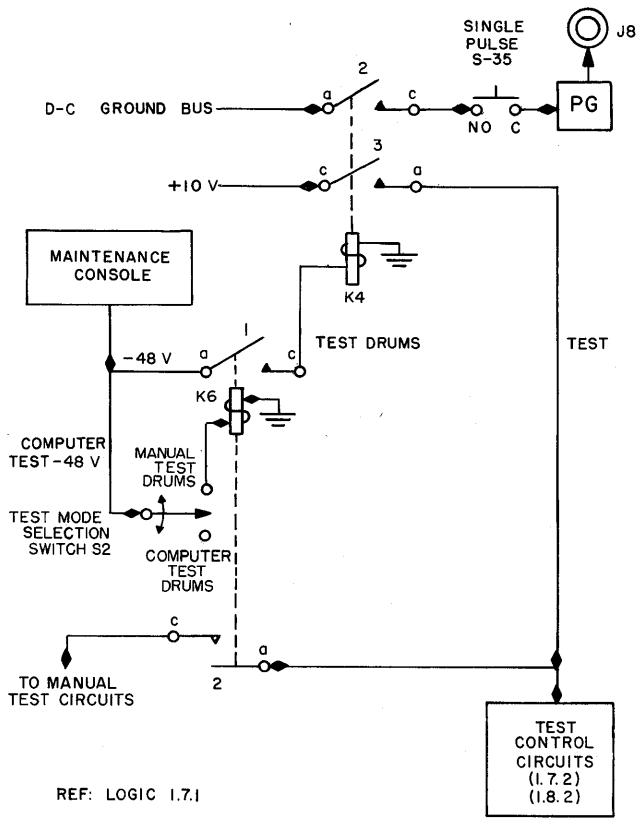


Figure 5–12. Manual-Test Circuit, Simplified Logic Diagram

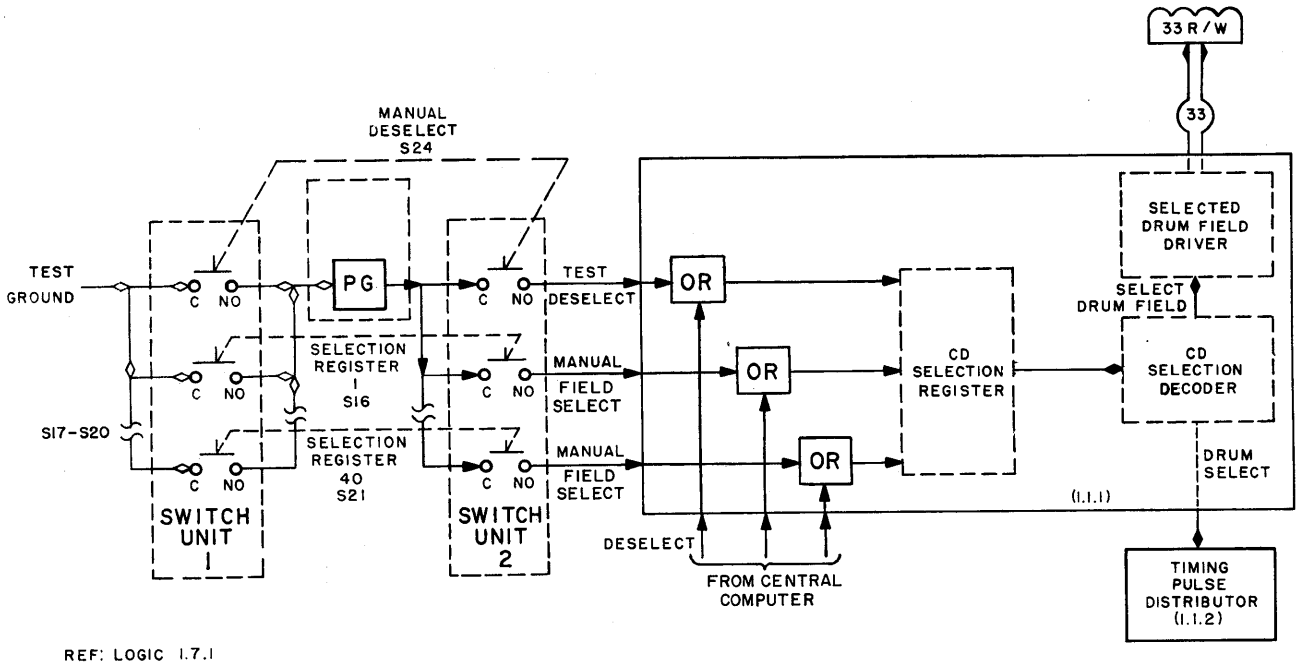


Figure 5–13. Manual-Test Field Selection, Simplified Logic Diagram

When the pulse generator input is grounded, the generator produces one 0.1-μsec pulse. This pulse is conducted through the closed, normally open, contacts of switch unit 2 to the CD selection register as a manual-deselect pulse. The manual-deselect pulse substitutes for the deselect pulse normally produced by the Central Computer System by providing an alternate input to OR 1. The deselect pulse clears the selection register and is sent to the CD-read-write-control circuit to prepare the latter to receive a drum operation instruction.

With the deselect operation completed, it is necessary to substitute manually a drum field selection for the drum field selection that normally comes from the Central Computer System in the form of auxiliary-bit pulses. Pushbuttons S16 through S21, labeled 1, 2, 4, 10, 20, and 40 (on the test door), provide substitutes for the six auxiliary-bit pulses from the Central Computer System. Depressing the pushbuttons produces 1's for the associated auxiliary bits. The resulting configuration of 1's and 0's in auxiliary-bit pulses 1, 2, and 4 determines the value of the units column in the drum field selection code; the resulting configuration of 1's and 0's in auxiliary bits 10, 20, and 40 determines the value of the tens column in the drum field selection code.

Table 5–1 shows the code of the field or test selection and the pushbuttons that must be depressed to produce it. Each pushbutton that is depressed in accordance with this table applies ground to the pulse generator. The pulse generator output (0.1-usec pulse) is conducted through the closed switch unit 2 pushbutton contacts of the OR circuit associated with the auxiliary-bit pulse represented by the individual pushbuttons. The OR circuits normally get auxiliary-bit pulse inputs from the Central Computer System. The pulses pass through the OR circuits and set the associated flip-flops in the CD selection register. On the basis of the setting of the CD selection register, the CD selection decoder determines the drum that has been selected and sends a drum-select level to the timing-pulse-distributor circuit. The CD selection encoder also determines the selected field and sends a select-drum-field level to the selected drum field driver. The selected drum field driver applies this level to the center taps of the drum heads associated with the selected fields, thereby enabling them to read or write.

4.2.3 Select-Manual-Read-or-Write-Drum-Operation Circuit

If the manual test that is to be performed requires a reading or writing operation by the field (or test) that has been selected, it is necessary to develop a manual substitute for the *Read* or *Write* instructions that normally come from the Central Computer System. The necessary substitution is made by the operation of controls in the select-manual-read-or-write-drum-operation circuit (fig. 5–14).

When a manual test involving a reading operation is to be performed on a selected field, the READ push-

TABLE 5–1. MANUAL TEST PANEL SELECTION REGISTER PUSHBUTTON CODE

FIELD OR TEST	CODE	PUSH-BUTTONS
DATA FIELDS		
MI basic status (test)	22	20, 2
MI status identification	23	20, 2, 1
XTL basic status (test)	24	20, 4
XTL status identification	25	20, 4, 1
XTL marker	40	40
LRI basic status (test) 1	34	20, 10, 4
LRI basic status (test) 2	36	20, 10, 4, 2
LRI 1 status identification	35	20, 10, 4, 1
LRI 2 status identification	37	20, 10, 4, 2, 1
GFI 1 basic status (test)	32	20, 10, 2
GFI 1 status identification	33	20, 10, 2, 1
AUXILIARY DRUM FIELDS		
AM A-1	02	2
AM A-2	03	2, 1
AM A-3	04	4
AM A-4	05	4, 1
AM A-5	06	4, 2
AM A-6	07	4, 2, 1
AM B-7	10	10
AM B-8	11	10, 1
AM B-9	12	10, 2
AM B-10	13	10, 2, 1
AM B-11	14	10, 4
AM B-12	15	10, 4, 1
Spare 1	20	20
Spare 2	21	20, 1

FIELD OR TEST	CODE	PUSH-BUTTONS
OUTPUT DATA FIELDS		
OB odd	30	20, 10
OB even	31	20, 10, 1
IC FIELDS		
IC Other	16	10, 4, 2
IC Own	26	20, 4, 2
DISPLAY DATA FIELDS		
DD test	17	10, 4, 2, 1
DD	27	20, 4, 2, 1
TD 1	41	40, 1
TD 2	42	40, 2
TD 3	43	40, 2, 1
TD 4	44	40, 4
TD 5	45	40, 4, 1
TD 6	46	40, 4, 2
SD test	47	40, 4, 2, 1
RD 1	60	40, 20
RD 2	61	40, 20, 1
RD 3	62	40, 20, 2
RD 4	63	40, 20, 2, 1
RD 5	64	40, 20, 4
RD 6	65	40, 20, 4, 1
RD 7	66	40, 20, 4, 2
RD 8	67	40, 20, 4, 2, 1
RD 9	70	40, 20, 10

button is depressed. This applies a test ground to the pulse generator, producing a 0.1-μsec pulse. The pulse serves as a manual-start-read pulse for use in the manual-test-pattern-control circuits, discussed in 4.2.4. It also serves as a substitute for the normal Central Computer System instruction to the CD-read-write-control circuit and computer-test-control circuits.

If the TD or RD fields are to be read, it is necessary to depress the RESET DISPLAY and START TD pushbuttons. Operation of these two pushbuttons also applies ground to the pulse generator, sending manual-reset-display and manual-start-TD pulses which go to the TD-OD-read-control circuit. These pulses substitute for the power-on-reset pulse developed when the equipment is initially energized, or for the end-RD-start-TD pulse produced during normal operation. When a manual test involving a writing operation is to be performed, the WRITE pushbutton is depressed.

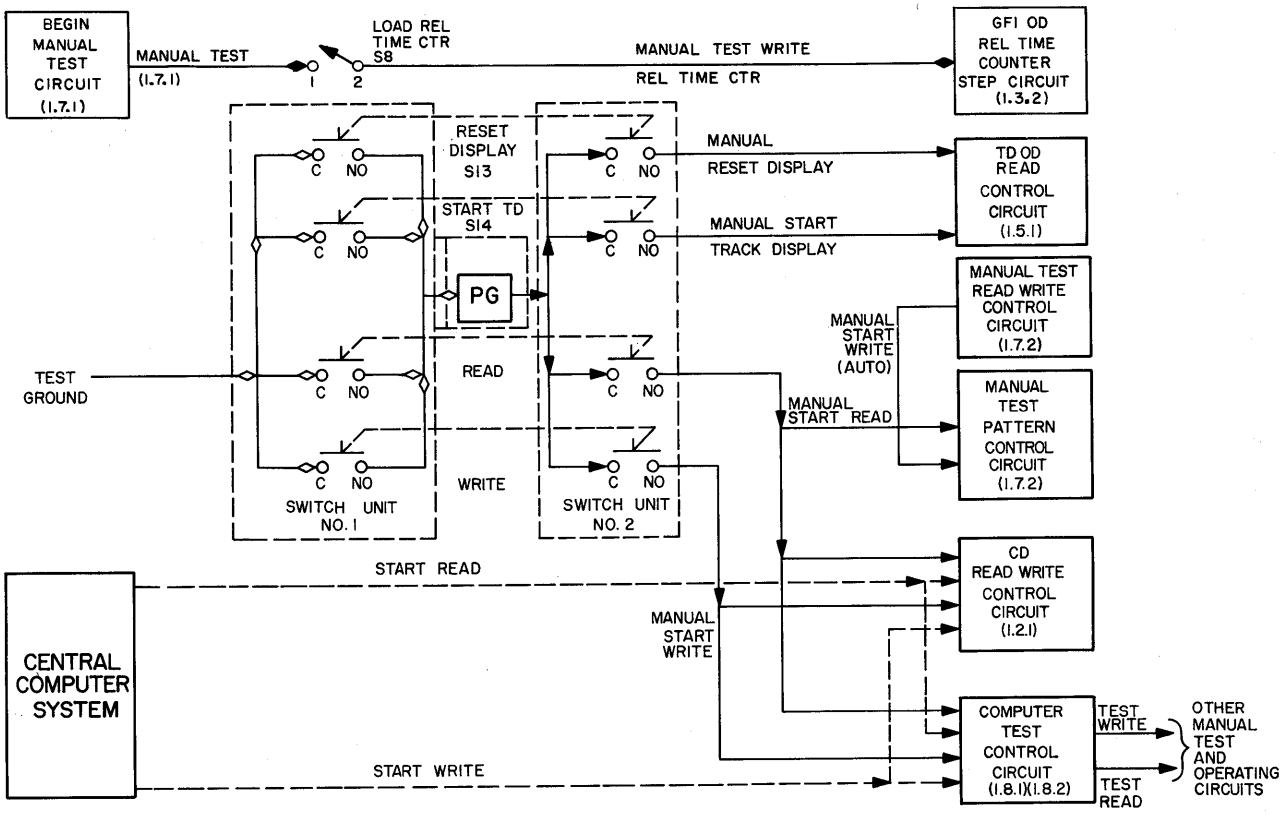


Figure 5–14. Select Manual Read or Write Drum, Simplified Logic Diagram

The action of this pushbutton is similar to that of the READ pushbutton. Manual-start-write pulses go to the CD-read-write-control circuit and to the computer-test-control circuit in place of the normal Central Computer System pulse inputs. An automatic manual-start-write pulse is provided for the manual-test-pattern-control circuit by gating the test-APC-carry pulse through the manual-read-write-control circuit.

If the operation of the relative time counter for the GFI fields is to be tested, it is necessary to operate the LOAD REL. TIME CTR. switch. This allows the begin-manual-test circuit to be sent to the GFI-relative-time-counter-step circuit. In the relative-time-counter-step circuit, this level conditions a gate which provides a test source for the relative-time-counter-reset pulse, which clears the flip-flops in the counter.

4.2.4 Manual-Test-Pattern-Control Circuit

During manual tests that require a known pattern to be written and read on the drum fields, the pattern to be used is selected by operating a control in the manual-test-pattern-control circuit. The complement of this pattern can also be developed by operating a control in the complement-test-pattern circuit. OR 1, in the manual-test-pattern-control circuit (fig. 5–15), conducts upon receipt of either a manual-start-read or a manual-start-write pulse, thereby setting the pattern flip-flop. Although the beginning of every test causes the flip-flop to be set, a complement-test-pattern pulse can be manually produced, which at first application clears the pattern flip-flop and at second application sets it again.

The outputs of the pattern flip-flop go to the contacts of TEST PATTERN switch S1. When the flip-flop side connected to any given contact is up, +10V is seen at the contact. When the flip-flop side is down, −30V is applied to the contact. Table 5–2 outlines the voltage present at the two wiper arms of the TEST PATTERN switch when the flip-flop is set and cleared for each position of the switch.

The output of the RC wiper arm is the odd-pattern-gate level; the output of the LC wiper arm is the even-pattern-gate level. The odd- or even-pattern-gate levels are logically present only when they are positive. The odd-pattern gate, when present, conditions GT 1. The even-pattern gate, when present, conditions GT 2. Gates 1 and 2 receive a pattern-sense pulse from the complement-test-pattern circuits (4.2.5). The pattern-sense pulses will go through the gates (either or both) whenever they are conditioned. The GT 1 output goes to the CD write as a test-write-CD-odd pulse, to

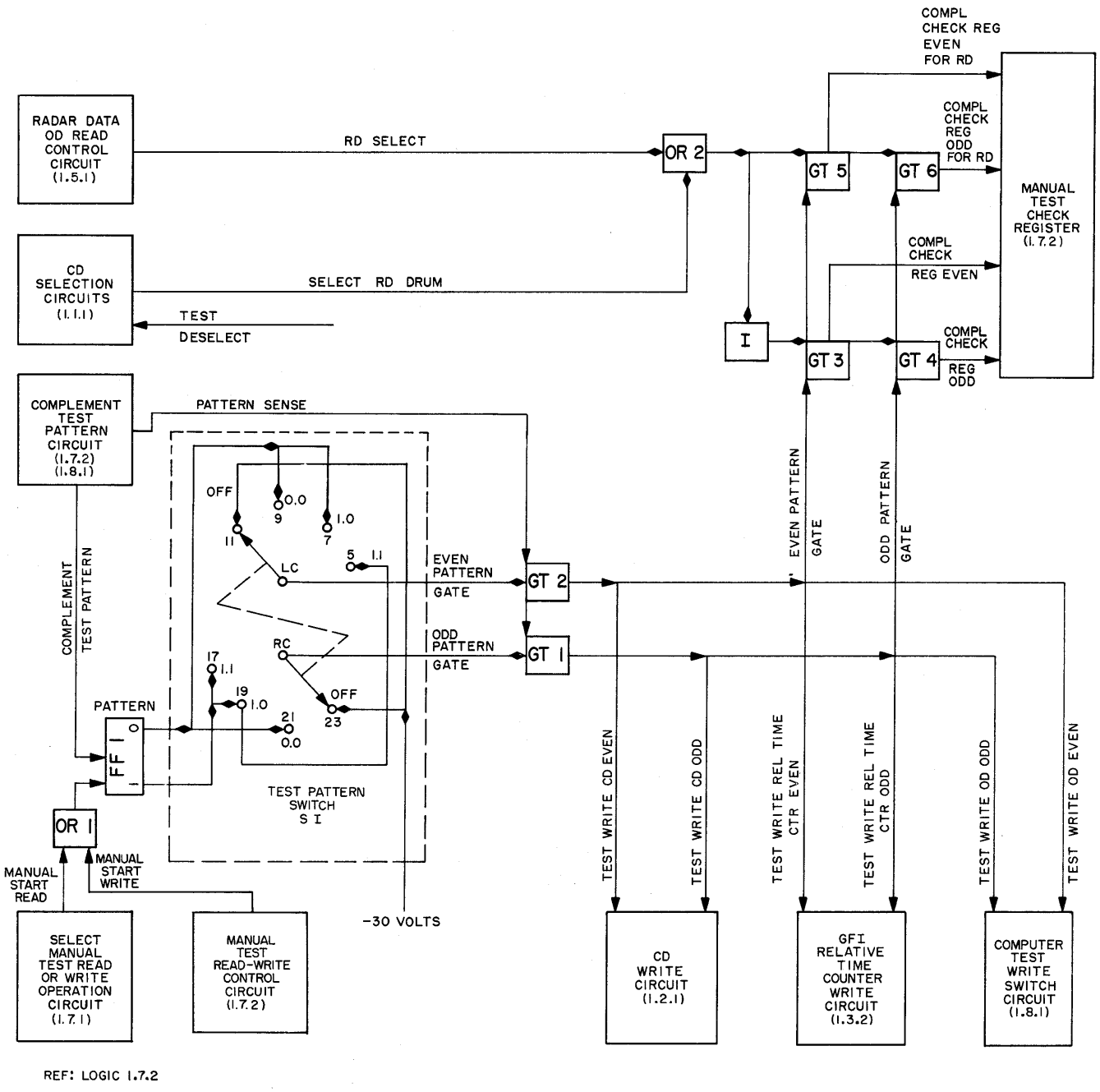


Figure 5–15. Manual Test Pattern Selection and Control Circuits, Simplified Logic Diagram

the computer-test-write switch as a test-write-OD-odd pulse, and to GT's 4 and 6 as an odd-pattern-gate pulse.

Gate 6 is conditioned to pass the odd-pattern-gate pulse if an RD-select level from the RD-OD-read-control circuit or a select-RD-drum level from the CD selection circuits is present at OR 2. Gate 4 passes the odd-pattern-gate pulse if both levels are absent from OR 2 since, at this time, the inverter-tube circuit produces a positive output which conditions the gate. The output of GT 6 is a complement-check-register-odd-for-RD pulse. The output of GT 4 is a complement-check-register-odd pulse. The complement-check-register-odd and complement-check-register-odd-for-RD pulses go to the manual-test-check register.

The output of GT 2 duplicates the functions of the output of GT 1, but as even pulses. Thus, the GT 2 output produces a test-write-CD-even pulse, an even-pattern-gate pulse, and so on. Whenever an output of

TABLE 5–2. TEST PATTERN SWITCH OUTPUT VOLTAGES

SWITCH POSITION	SWITCH CONTACT	WIPER ARM	VOLTAGE WITH FLIP-FLOP SET (Volts)	VOLTAGE WITH FLIP-FLOP CLEARED (Volts)
OFF	4	LC	−30	−30
	10	RC	−30	−30
0.0	3	LC	−30	+10
	9	RC	−30	+10
1.0	2	LC	−30	+10
	8	RC	+10	−30
1.1	1	LC	+10	−30
	7	RC	+10	−30

GT 1 or 2 is present, it causes the placing of 1's in the associated write circuit to which the odd or even output goes. Thus, if the GT 1 output is present, 1's are passed to the odd-numbered channels (L1, L3,..... R1, R3..... and so on) of the write circuits to which it is applied. In the same way, the GT 2 output causes 1's to be passed in the even-numbered channels (L2, L4,.....R2, R4..... and so on) of the write circuits to which it is applied.

A distinction is made between the odd- and even-complement-check-register pulses that are sent during an RD field selection because the RD fields contain

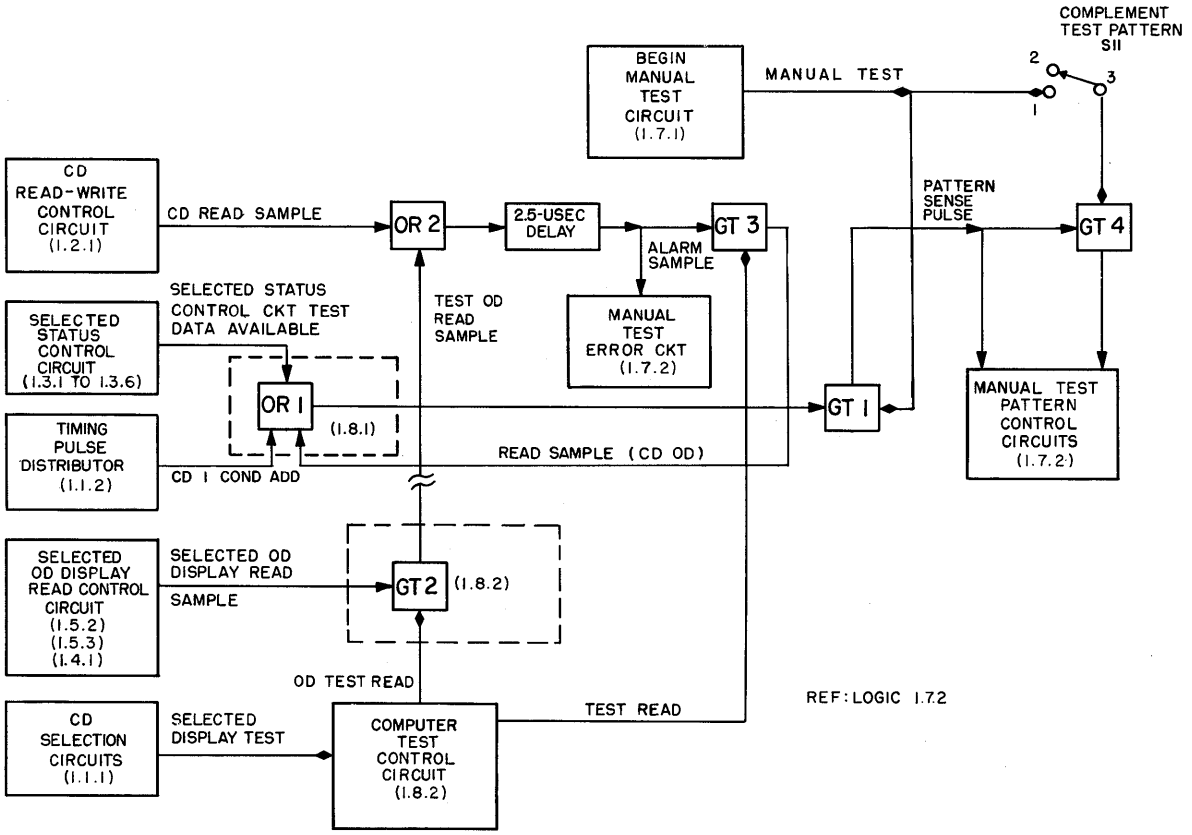


Figure 5–16. Complement Test Pattern Circuit, Simplified Logic Diagram

only 24 bits each. Complement-check-register-for-RD pulses, whether odd or even, are applied to only 24 bits of the manual check register.

4.2.5 Complement-Test-Pattern Circuit

The complement-test-pattern circuit (fig. 5–16) is employed in the production of the pattern-sense pulse, which senses the condition of the pattern flip-flop and TEST PATTERN switch for the varied write circuits involved in manual tests. The pattern-sense pulse is produced during manual-test procedures. A manual-test level conditions GT 1, which will then pass the output of OR 1. Condition in OR 1 is caused either by a selected-status-control-circuit-test-data-available pulse from the selected-status-control circuit, by a CD-1-conditioned-add pulse from the timing pulse distributor, or by a CD-OD-read-sample pulse from the CD-read-write control or the computer-test-control circuits.

During manual-test read operation, the computer-test-control circuit sends a test-read level to GT 3, conditioning the gate. The pulse input to GT 3 is obtained from OR 2, which, in turn, receives pulses either from the CD-read-write-control circuit or from the selected OB-OD-display-read-control circuit via GT 2. When the pulse is obtained from the CD-read-write-control circuit, the CD-read sample is applied directly to OR 2. When the pulse is obtained from the selected-OB-OD-display-read-control circuit, a selected-display-test level (either SD or DD) is transmitted to the computer-test-control circuit. The control circuit then transmits an OD-test-read level to GT 2 if a manual read test is being performed as described in 4.2.3. With GT 2 conditioned, selected SD-OD-read-sample pulses from the selected-SD-OD-display-read-control circuit pass through GT 1 to OR 2.

The output of OR 2 is delayed 2.5 usec and applied to GT 3, which has previously been conditioned by the test-read level from the computer-test-control circuit (as described above), and the output of GT 3 is applied to OR 1. The delayed OR 2 output also goes to the manual-test-error circuit as an alarm sample.

The pattern-sense pulse at the output of GT 1 is also used to produce the complement-test-pattern pulse, which is sent to the manual-test-pattern-control circuits. This pulse is developed by operating COMPLEMENT TEST PATTERN switch S11. This applies a level to GT 4, gating the pattern-sense pulse to form the complement-test-pattern pulses.

4.2.6 Manual-Test-Check-Register-and-Control Circuit

The manual-test-check-register-and-control circuit (fig. 5–17) provides a means of checking the contents of words written by the manual-test-pattern-control circuits. As was indicated in 4.2.4 and 4.2.5, during manual-test write operations, a pattern-sense pulse is developed which causes the manual-test-pattern-control circuit to send complement-check-register pulses to the manual-test-check register. The complement-check-register pulses may appear as odd- and/or even-complement pulses for RD field or as odd- and/or even-complement pulses for all other drum fields. Complement-check-system-odd-for-RD pulses go to the even-numbered flip-flops from 2 to 10 and from 16 to 26. Complement-check-register-odd pulses for all other fields go to all the even-numbered flip-flops.

Complement-check-register-even-for-RD pulses go to all odd-numbered flip-flops from 1 to 11 and from 15 to 27. Complement-check-register-even pulses for all other fields go to all the odd-numbered flip-flops.

In this manner, selection of an RD field for manual-test purposes allows only those flip-flops in the manual-check-register circuit that correspond to the RD drum word bits to be affected.

Each flip-flop in the manual-check-system-control circuit has both its 1 and 0 sides connected to neon indicator lamps on the manual test panel. Since complement pulses sent to the manual-check-register circuit correspond to the pattern pulses sent to the various write circuits during the manual-test write procedures, the flip-flops of the manual-check register which are set by the reading of 1 bits are cleared by the complement pulses.

When manual test writing is completed, a manual test read operation checks the pattern that has been written. The manual-test-check-register-and-control circuit is initially cleared by a reset-check-register pulse from the manual-control circuit if an error was indicated. As explained in 4.2.9, the reset-check-register pulse is produced by manually operating a control on the test panel of the drum unit. After the initial clearing of the manual-test-check register, the contents of the drum register being read at CD 1 time are sent to the flip-flops in the manual-test-check register from the CD-read-bus-output circuit. At any bit in the drum register where a 1 is read, that 1 sets the associated flip-flop in the check register. At CD 2 time, 2.5 usec later, the complement-check-register pulse is sent to the manual-test-check register. All flip-flops that should have 1 bits receive a complement pulse. If the pattern that should have been written is read, all flip-flops in the manual-test-check register are cleared. If, however, a flip-flop that should have a 1 bit has a 0 bit instead, the complement pulse sets that flip-flop. This causes an error indication.

To sum up the operation of the manual-test-check-register-and-control circuit, the presence of a 1 bit in any flip-flop after CD 2 time indicates an error. This 1 bit is sent to the manual-test-error circuit and pro-

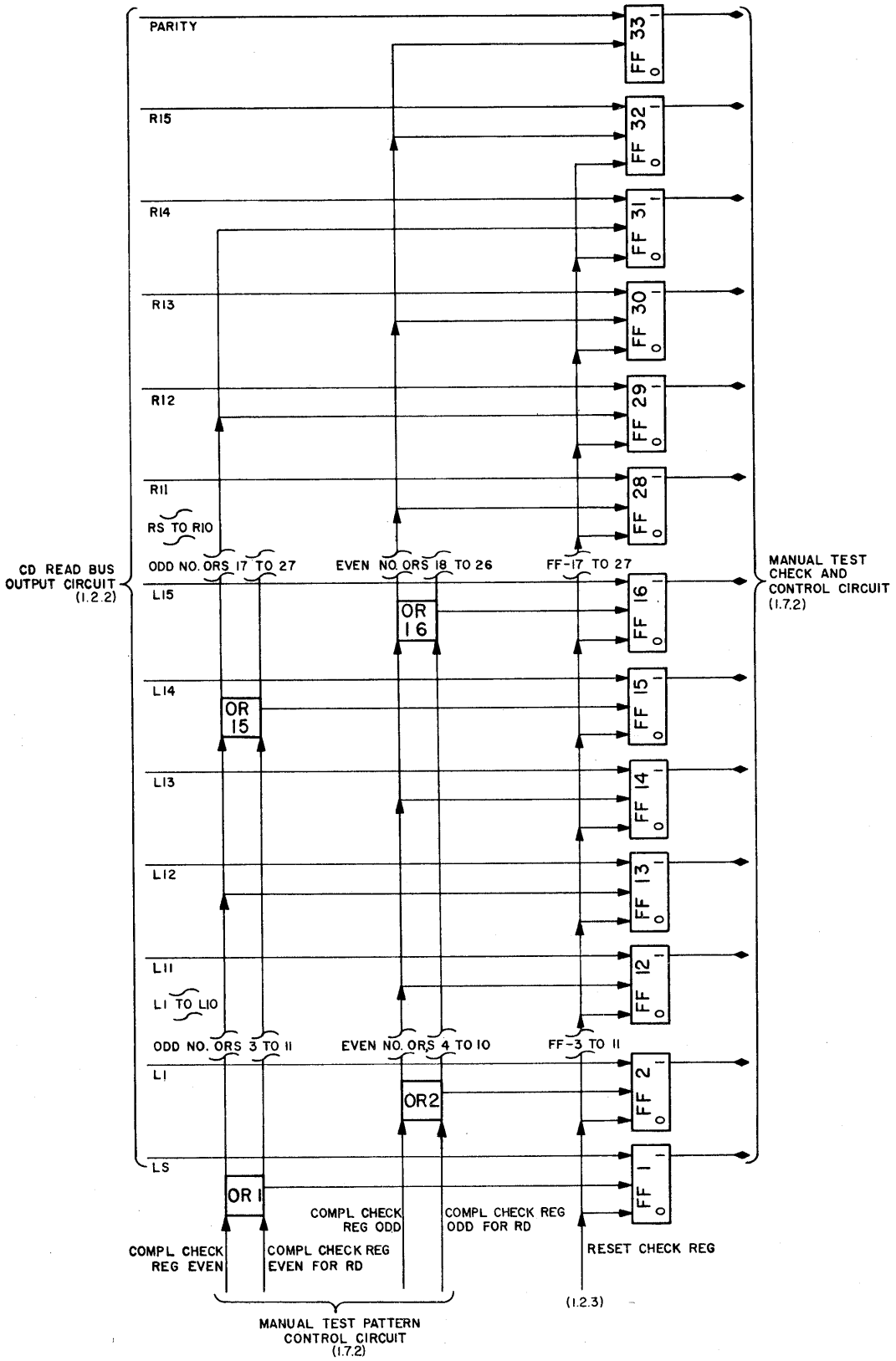


Figure 5–17. Manual Test Check Register and Control Circuit, Simplified Logic Diagram

duces an error indication which stops drum operations. The neon lamps connected to the flip-flops then indicate which drum bit is being incorrectly transferred.

4.2.7 Manual-Test-Read-Write-1-Revolution-Control Circuit

During most of the tests performed on the fields that read and write by status control or a modification of status control, it is desirable to test drum operations for only one drum revolution or its equivalent. The test read or write operation can be stopped at the end of the one revolution of a drum field or at the end of the number of revolutions it takes to complete the read or write operation. The controls that stop the operation at the end of one revolution are shown in figure 5–18.

When OPERATE 1 REV switch S10 is closed, the manual-test level from the begin-manual-test circuit is applied to AND's 1, 2, 3, and 4. Of the four, AND 1 is associated with the display fields, AND 2 with the fields on the LOG drum (with the exception of the OB fields), AND 3 with fields on the MIXD drum (with the exception of the DD field), and AND 4 with the OB fields. The production of the CD-read-compare or CD-write-compare level (depending upon which operation is to be performed) by the CD-read-write-control circuit causes conduction in AND 1. This occurs after the first test-angular-position-counter-carry pulse. The output of AND 1 conditions GT 1 to pass the second test-angular-position-counter-carry pulse from the manual-test-angular-position-counter-alarm circuit. The second test-angular-position-counter-end-carry pulse is produced after all the registers of the field selected for test have had either a read or write operation performed on them. (The manual-test-angular-position-counter-and-alarm circuit is discussed in 4.2.8.) The output of GT 1 goes to OR 3, producing a LOG-disconnect-1-revolution pulse. The LOG-disconnect-1-revolution pulse goes to the CD-read-write-control circuit and stops the read or write operation in progress.

When the GFI- or LRI-test-write level is sent to OR 2 by the computer-test-control circuit, AND 2 conducts. The output of AND 2 conditions the passing of a

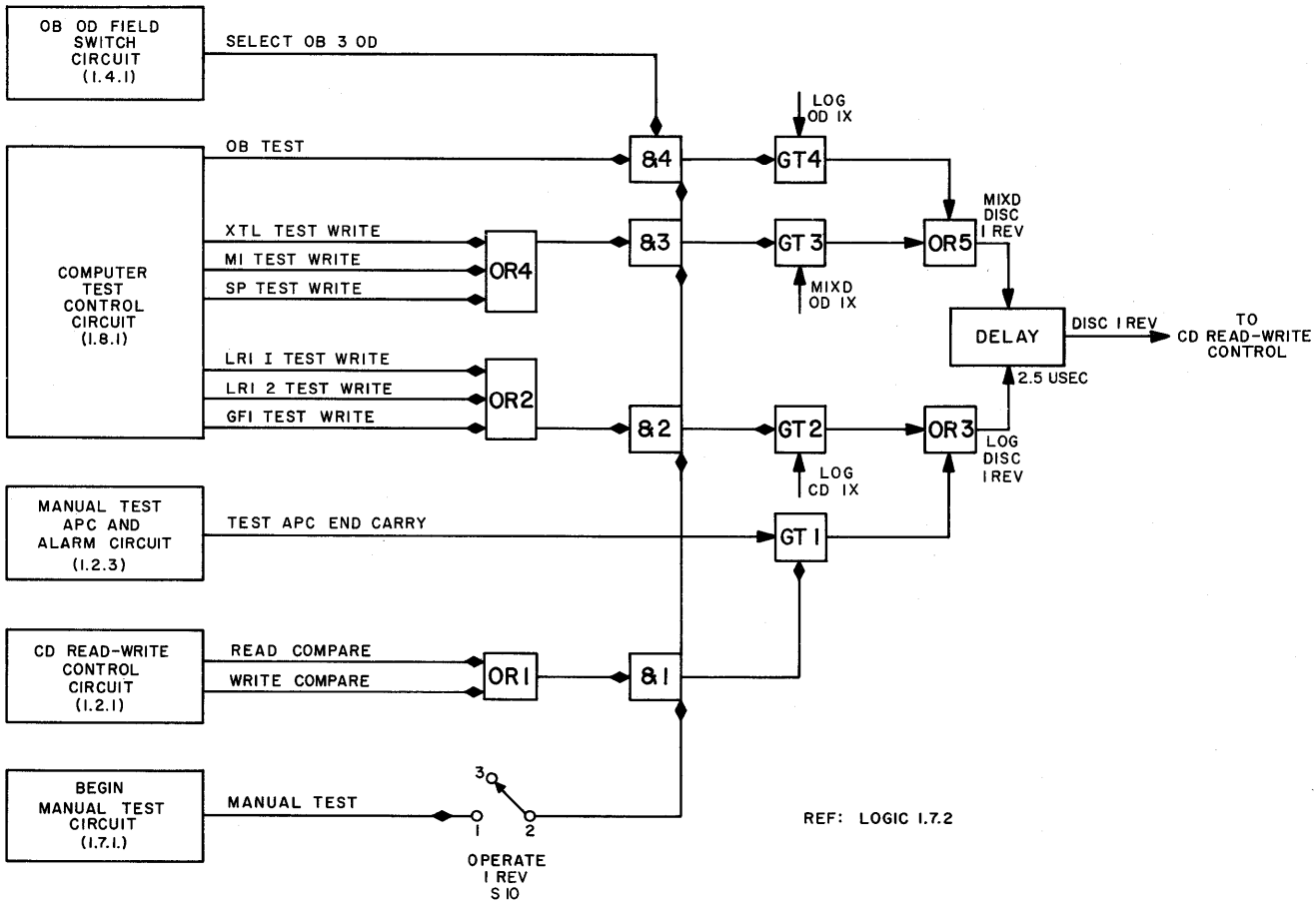


Figure 5–18. Manual-Test-Read-Write-1-Revolution-Control Circuit, Simplified Logic Diagram

LOG-index pulse from the LOG timing circuit in GT 2. The GT 2 provides a second source of the LOG-disconnect-1-revolution pulse at OR 3. Since the test-write levels at the input to OR 2 are formed when the index pulse from the LOG timing circuit is received in the computer-test-control circuit, the test write operation lasts from the index pulse that forms the test-write level to the index pulse that causes the disconnect (one drum revolution).

Similarly, AND 3 conducts when an XTL, MI, or spare-test-write level is produced, causing conduction in OR 4, which then feeds AND 3. The AND 3 output conditions GT 3 to pass the following MIXD-index pulse to OR 5. The resulting OR 5 output is the MIXD-disconnect-1-revolution pulse, which stops the writing operation.

Conduction is produced in AND 4 when it receives both the OB-test level (formed when the reading of the first OB field begins) and the select-OB-3-OD level (formed when reading of the third OB field begins). The output of AND 4 conditions GT 4 to pass the next OB-field-switch pulse from the CD-OB-field-switching circuit. The only time GT 4 is conditioned to pass an OB-field-switch pulse is when all three OB fields have been read. At this time, the OB-field-switch pulse that is gated is the same pulse that causes a switch to OB field 1 from field 3. The output of GT 4 goes to OR 5, producing an all MIXD-disconnect-1-revolution pulse, which stops the test-read operation.

4.2.8 Manual-Test-Angular-Position-Counter-and-Alarm-Control Circuit

The manual-test-angular-position-counter-and-alarm-control circuit (fig. 5–19) is used to provide a means of indicating the drum register being read or written when an error is detected during manual tests. This circuit is also used to check the precessed reading patterns used in the OD display circuits and to check the operation of the drum timing circuits.

The circuit controlling the operation of the manual-test-angular-position-counter-and-alarm circuit is shown in figure 5–19. The test-select-CD-index pulse is sent to OR 1 and causes it to conduct. The output of OR 1 goes to GT 1 and is passed to the 11-stage-angular-position counter as a clear-angular-position-counter pulse. The clear-angular-position-counter pulse clears the flip-flops in the 11-stage-angular-position counter, which is a standard serial-counting circuit. In tests on the manual-test angular position counter itself, the selected CD-index pulse is substituted by a reset-test-angular-position-counter pulse. The reset-test-angular-position-counter pulse is produced by applying a single pulse input to RESET jack J2 on the test door (fig. 5–1). In order for either pulse to be passed to the angular position counter by GT 2, a not-error level from the manual-test-error circuit must be present at the gate. This level is always present except for the time at which an error is detected.

During all tests, except those on fields employing a precessed reading pattern, test-select-CD 3 pulses from the timing pulse distributor are fed to OR 2, which conducts, sending a pulse to GT 2. As with GT 1, GT 2 passes the output of its associated OR circuit only when a not-error level from the manual-test-error circuit is present. The output of GT 2 is the test-angular-position-counter-step pulse, which goes to the 11-stage angular position counter. At the 2,048th select-CD 3 pulse, the angular position counter forms a test-angular-position-counter-carry pulse, which clears FF 1. (Flip-flop is initially set by applying a single pulse to CONDITION ALARM jack J4.) At CD 1 time of the next register, a test-select-CD-index pulse from the timing pulse distributor is fed to OR 1, causing the production of a clear-angular-position-counter pulse. The clear-angular-position-counter pulse clears the flip-flops of the 11-stage angular position counter and goes to GT 3. If a malfunction is present in the 11-stage angular position counter, in the selected drum timing circuit, or in the timing pulse distributor, the test-angular-position-counter-carry pulse is not developed in time to clear FF 1 before receipt of the clear-angular-position-counter pulse. The resulting 1-state level from FF 1 conditions the passing of the clear pulse by GT 3 to produce a test-angular-position-counter-error pulse. This pulse goes to the manual-test-error circuit and indicates an error in the counting operation. It also sets FF 3, causing neon lamp I48 to light and thereby providing visual indication of the presence of an error. In the manual-test-error circuit, the test-angular-position-counter-error pulse causes the not-error-conditioning level to be removed from GT's 1 and 2. Counting in the 11-stage counter is therefore stopped and cannot be resumed until the not-error level is returned.

If an error is detected at any time during a test on other circuits, the presence of that error in the manual-test-error circuit causes also the removal of the not-error level. Should this error occur during the middle of a drum revolution, the removal of the not-error level from GT's 1 and 2 will stop the counter. Neon indicating lamps are connected to the flip-flops in the 11-stage counter and indicate the setting of the counter at the time counting is stopped.

During tests on fields employing precessed reading patterns, it is necessary that all registers be read even though register reading is not sequential. To check this operation, the manual-test-angular-position-counter-and-alarm circuit counts the number of read-sample pulses produced during the reading of a field without respect to the number of drum revolutions required. Thus, when

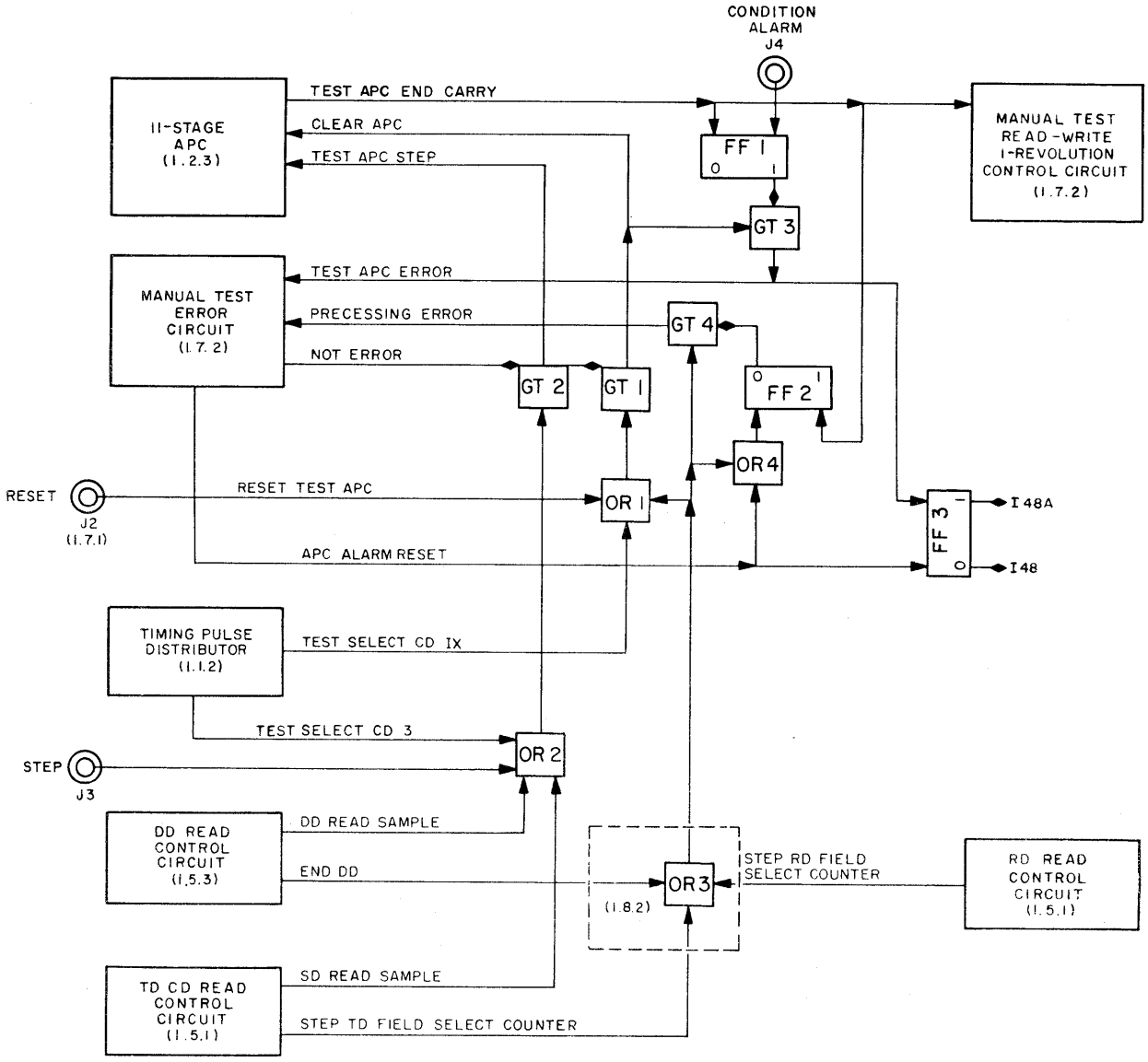


Figure 5—19. Manual-Angular-Position-Counter-and-Alarm-Control Circuit, Simplified Logic Diagram

the DD field is being tested, DD-read-sample pulses from the DD-read-control circuit are received at OR 2. They are passed in GT 2 to form test-angular-position-counter-step pulses. The 2,048th DD-read-sample pulse counted forms a test-angular-position-counter-carry-pulse, which sets FF 2. Setting FF 2 removes the 0-state level from GT 4. At the OD 3 time which follows 5 used after the 2,048th DD-read-sample pulse, an end-DD pulse from the DD-read-control circuit arrives at OR 3 and is conducted to GT 4. In addition, it causes conduction in OR's 1 and 4, clearing FF 2 and causing the production of a clear-angular-position-counter pulse at GT 1. If the number of DD-read-sample pulses produced was insufficient to produce a test-angular-position-counter-carry pulse, FF 2 is cleared before the end-DD pulse arrives, and GT 4 is conditioned in time to pass the end-DD pulse from OR 3 to the manual-test-error circuit. The GT 4 output is the precessing-error pulse. During tests on the RD and TD fields, operation is the same as in the case of the DD field. Situation-display-read-sample pulses from the TD-OD-read-control circuit replace the DD-read-sample pulses at OR 2. Step-TD-field-selector-counter pulses from the TD-OD-read-control circuit (or step-RD-field-selector-counter pulses from the RD-read-control circuit) replace end-DD pulses.

Test-angular-position-counter-carry pulses are sent to the manual-test-read-write-1-revolution-control circuit whenever they are produced, to be employed by the latter circuit as a means of stopping manual tests at the end of one drum revolution or its equivalent. This operation is described in 4.2.7.

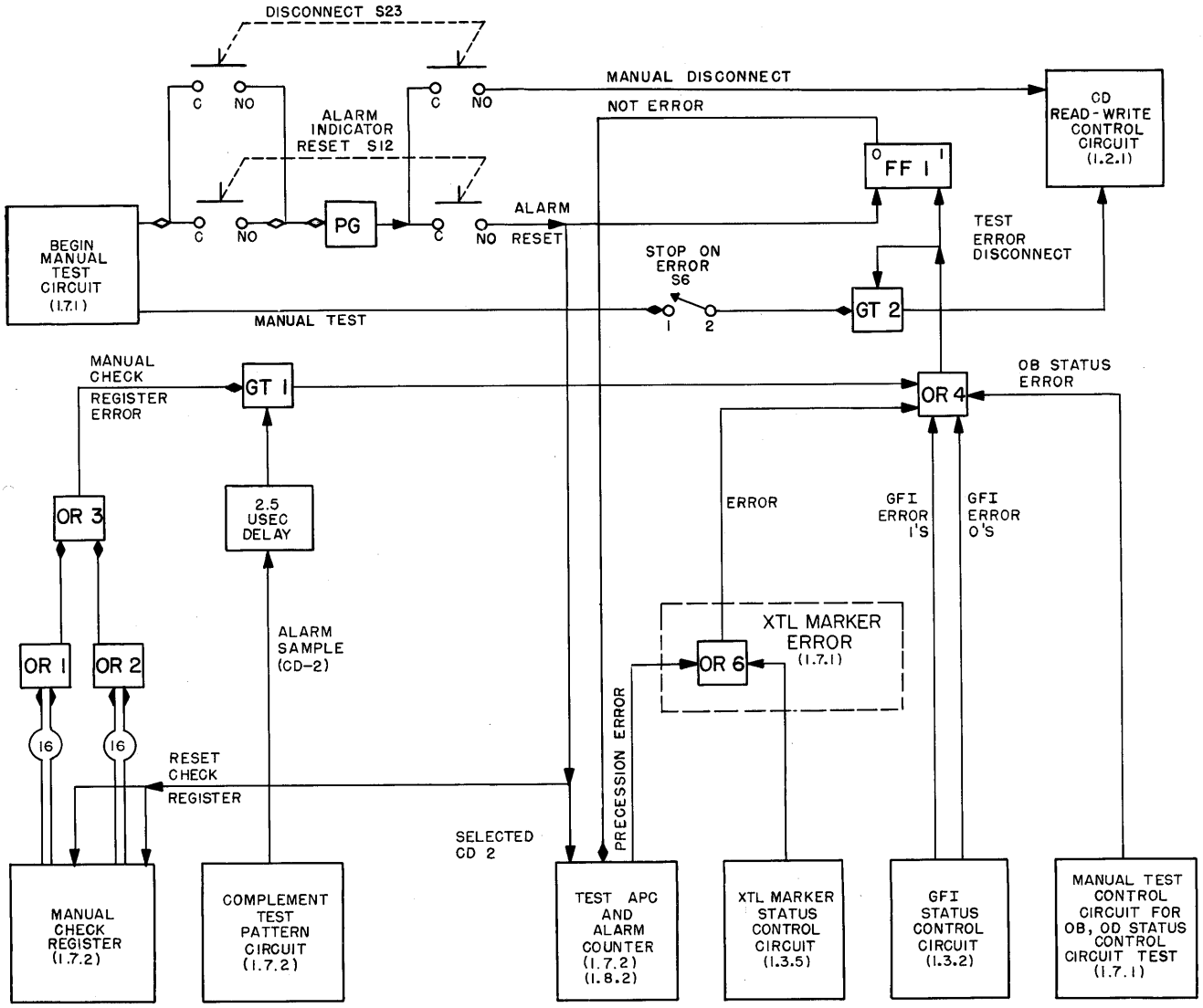


Figure 5—20. Manual-Test-Error Circuit, Simplified Logic Diagram

4.2.9 Manual-Test-Error Circuit

The manual-test-error circuit (fig. 5—20) provides a means of stopping drum operations when errors are detected during manual test and some normal operating procedures.

The presence of a 1 bit in the left-half word of the manual-check-register circuit following a complement of the register flip-flops indicates an error in a pattern test. The 1 bit causes conduction in OR 1. In the same way, an error in the right half of the check register word is indicated by a 1 bit that causes conduction in OR 2. If OR 1 or 2, or both, have an input, the resulting output produces conduction in OR 3. The output level produced by OR 3 (manual-check-register-error level) conditions GT 1 to pass an alarm-sample pulse from the complement-test-pattern circuit (4.2.5) to OR 4, which produces an output pulse, setting FF 1, the not-error flip-flop. Inputs other than the GT 1 output cause conduction in OR 4. These inputs are error-1's or error-0's pulses from a status-control circuit that has been selected for a status control channel check, an OB-status-error pulse from the manual-CD-status-and-OB-OD-status-tests-control circuit, or an output from OR 6. An OR 6 output is developed when a precessing error is received from the test-angular-position-counter-and-alarm circuits, or an XTL-marker-error pulse from the XTL-marker-status-control circuit. When FF 1 is set, the 0-state-output level is removed from the test-angular-position counter and stops the counting operation. Neon indicators associated with the test-angular-position counter are lighted to indicate the drum register on which the error occurred. If STOP

ON ERROR switch S6 has been operated, GT 2 is conditioned to pass the output of OR 4 to the CD-read-write-control circuit as a test-error-disconnect pulse. The test-error-disconnect pulse stops the test at the point at which the error is detected.

A manual-disconnect pulse, which has the same effect as the test-error-disconnect pulse, the Central-Computer-System-disconnect pulse, the status-disconnect pulse, or the OB-disconnect pulse, is generated by depressing the DISCONNECT pushbutton.

To resume operations on the field being tested or on a new field, it is necessary to depress the ALARM INDICATOR RESET pushbutton. The ALARM INDICATOR RESET pushbutton, like the DISCONNECT pushbutton, applied a level to the pulse generator, causing a single pulse to be produced across the second pair of pushbutton contacts. This pulse goes to FF 1 as an alarm-reset pulse, which clears the flip-flop and brings the not-error level up again. The pulse goes to the test-angular-position-counter-and-alarm circuit as an angular-position-counter-error-reset pulse. In the test-angular-position-counter-and-alarm circuit, the angular-position-counter-error-reset pulse returns the counting circuits to the 0 state. The alarm-reset pulse also produces a reset-check-register pulse, which clears both halves of the manual check register.

4.3 DRUM ERASE AND TIMING INDEX WRITE CONTROLS

The magnetic flux patterns on the drums which represent binary data are normally changed only by being written over or by accidental introduction of spurious fields. In certain cases, such as periods following maintenance or during installation, it is desirable to clear all information from the drum surface. This is accomplished by an erasing operation.

When a drum is erased, its surface is cleared of all magnetic flux patterns, including any random fields that might have been established by noise in the drum writing head. The timing and index channels are automatically rewritten after each erasure. The erase-rewrite circuits and components are described in the paragraphs that follow and are shown in detail on logic 1.7.3.

The drums are demagnetized by passing an alternating current of gradually decreasing magnitude through the coils on the drum erase bar. A view of a drum erase coil is shown in figure 5–21. The erase bar consists of a metal channel with a centerpiece which serves as an electromagnetic core for four-coil windings. The coils are electrically connected in series-parallel, as shown in the figure

One assembled drum erase bar is mounted on each of the drums. The erase bars are placed between read-write bar 1 and the drum casting (fig. 2–9). It should

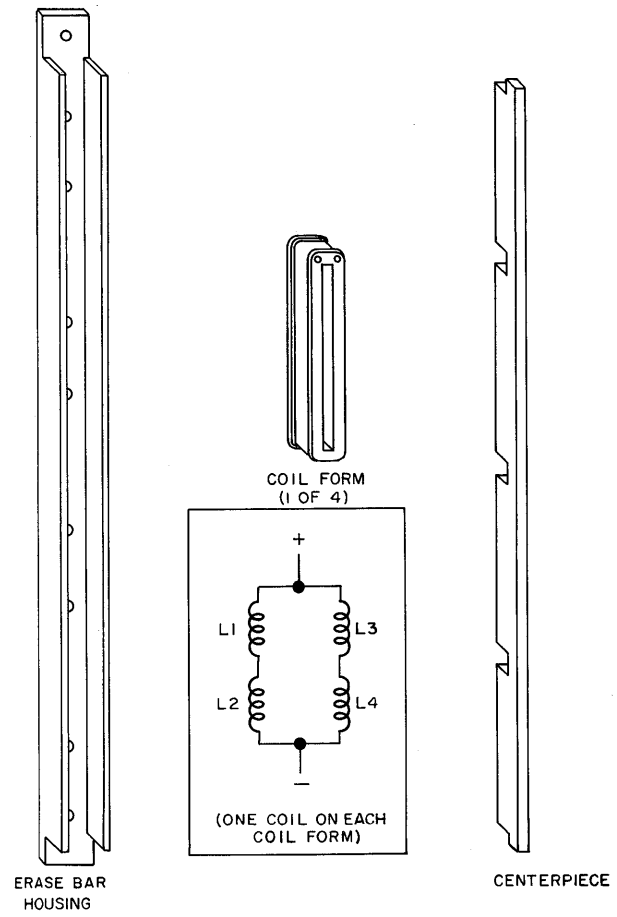


Figure 5–21. Erase Bar Components

be remembered that, although the erase bars are physically fixed on the drums, erasing (and automatic rewriting of the timing channels) is not a continuous operation. Manual controls on the unit 21 test door or on the maintenance console must be operated to erase any of the main drums and to write the timing and index channels for that drum.

4.3.1 Drum Erase

The circuit employed to apply an alternating current of gradually decreasing magnitude is shown in figure 5–22. Relay K4 is energized by moving switch S2 on the module 21L test door (fig. 5–1) to the DRUMS IN MANUAL TEST position. The drum to be erased is selected by rotating DRUM SELECTOR switch S33 to the appropriate position.

Contacts 16 and 17 of the relay apply 115V, 60-cycle power to the erase circuit. To apply power to the erase motor, either one of two switch circuits is used. With DRUM ERASE pushbutton S34 depressed and held down, and with DRUM SELECTOR switch S1 on the maintenance console turned to the OFF position,

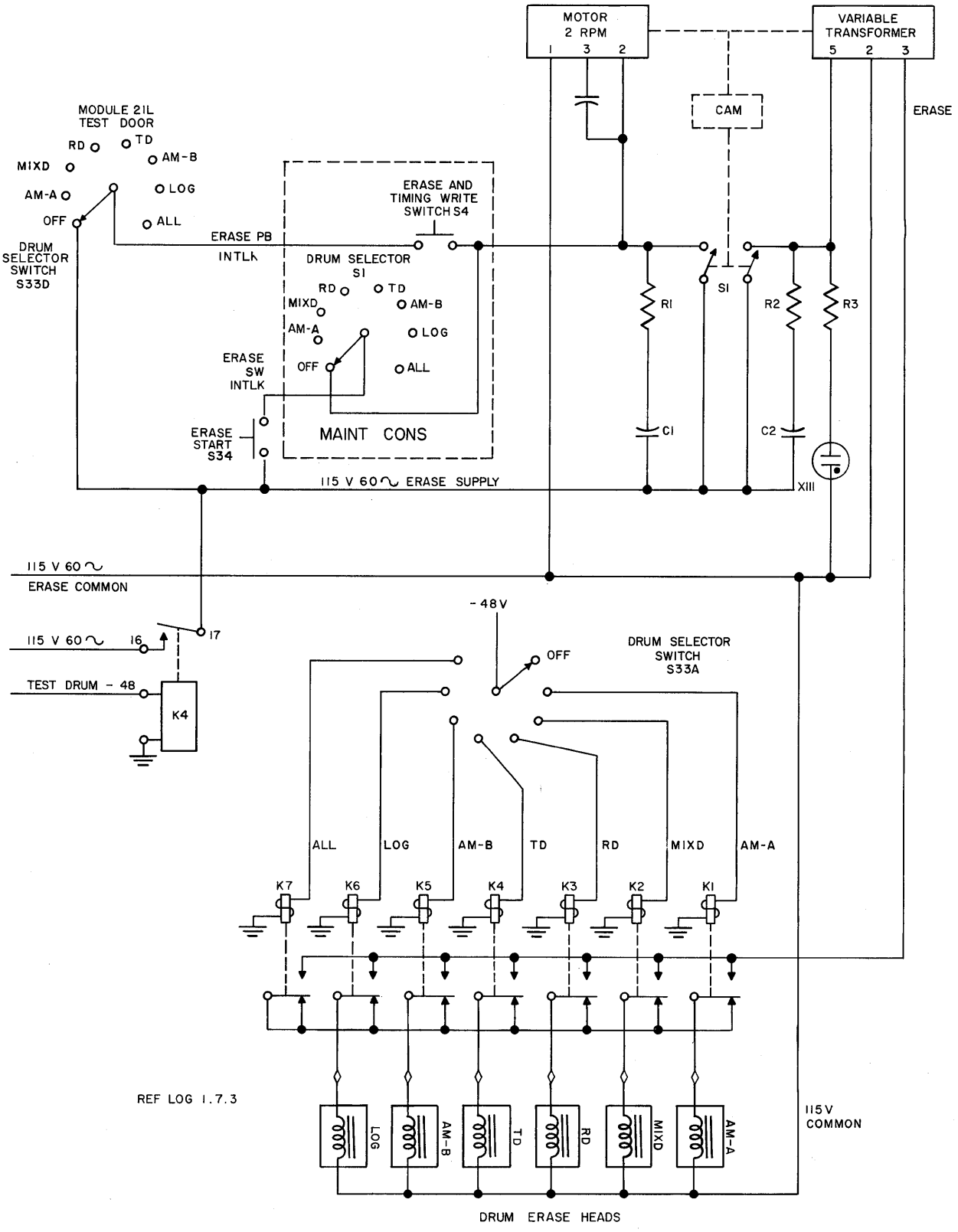


Figure 5–22. Erase-Rewrite-Start Circuit, Simplified Schematic Diagram

the 60-cycle erase supply voltage is applied through the OFF position of DRUM SELECTOR switch S33 on the module 21L test door when ERASE AND TIMING WRITE switch S4 on the maintenance console is depressed and held down. In this event, drum selection is made by means of DRUM SELECTOR switch S1 on the maintenance console. Either DRUM SELECTOR switch S1 or DRUM SELECTOR switch S33 may be used to activate the drum selector relays.

The erase motor is a 2-revolution-per-minute motor which drives the voltage output amplitude control on the variable transformer. As the drum erase motor turns, it drives a cam which closes the contacts of switch S1. When S1 closes, it bypasses the circuits containing the erase pushbuttons and applies power to the motor and the variable transformer. Resistance-capacitance networks R1 and C1, and R2 and C2, are in parallel with S1 to protect the switch contact from arcing. When S1 closes, neon bulb X111 on the test door of module 21L (fig. 5–1) lights, indicating that the erase pushbutton can be released. Switch S1 remains closed for 30 seconds, during which time the variable transformer is slowly turned until its output voltage is reduced to zero. At the end of 30 seconds, the motor-driven cam reopens the switch contacts, and the a-c source is removed.

The output of the variable transformer is applied through the contacts of the drum selection relays to any or all of the erase heads. During erasure, the selected drum rotates at normal speed.

4.3.2 Single Drum Timing and Index Channel Write

Whenever a drum is erased, the timing and index channels of that drum are automatically rewritten. Both channels are rewritten at the same time by means of the component circuits shown in block form in figure 5–23. These circuits are arranged in logical order to show the transfer of signals from one circuit to another during a timing-index-write operation. The drum selection relays and the timing-and-index-channel-write circuits are described in the paragraphs that follow. The optical transducer, the optical frequency generator, and the timing pulse generator are described in Part 4.

Only one of the six optical transducers and frequency generator assemblies can be operated at a given time. The assembly to be used is chosen by means of DRUM SELECTOR switch S33 on the unit 21 test door or switch S1 on the maintenance console. The timing-and-index-write operation follows automatically the erase operation described in 4.3.1. In the event that all six drums are selected for erasure, each of the six drums will be erased at the same time; however, the automatic writing of the timing and index channels for these drums will be performed sequentially, beginning as soon as the erasure is completed. (The automatic sequential selection of the drums for the timing-and-index-channel-write operation is described in 4.3.3.)

Operating one of the drum selector switches, say DRUM SELECTOR switch S33, determines which optical frequency generator has operating voltages applied to its circuits. Operating S33 to the LOG position applies −48V to LOG drum selection relay K6. Contacts 1-2 and 3-4 of K6 close, applying a +250V level and a −300V level to the LOG optical frequency generator (fig. 5–24). Energizing the drum selection relays of a drum applies the 100-kc sine wave from the output of the optical frequency generator to the timing pulse generator through one pair of the relay contacts. Energizing the drum selection relays also applies the output of the drum writers to the writing heads on the timing and index channels of the selected drum. The writing heads are fed through contacts of the appropriate drum selection relay (fig. 5–25). It should be noted that the test-drums level from the maintenance console reaches the drum selection relays only if TEST

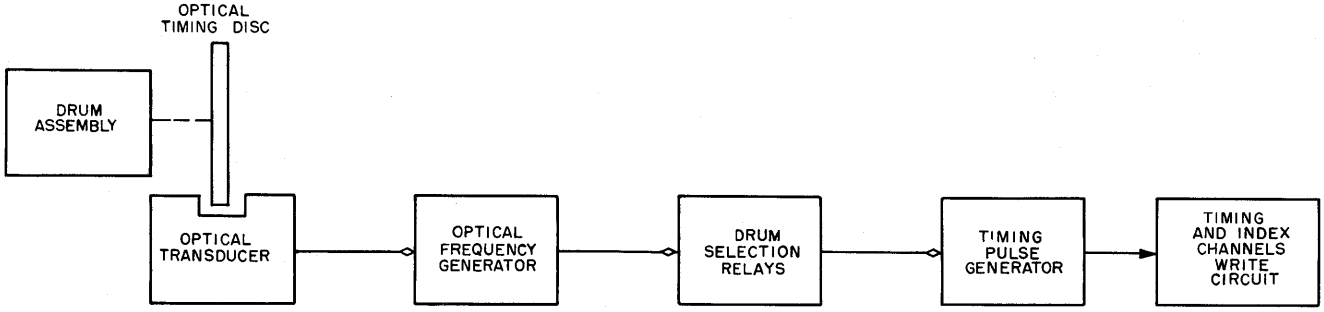


Figure 5–23. Writing of Timing and Index Channels, Block Diagram

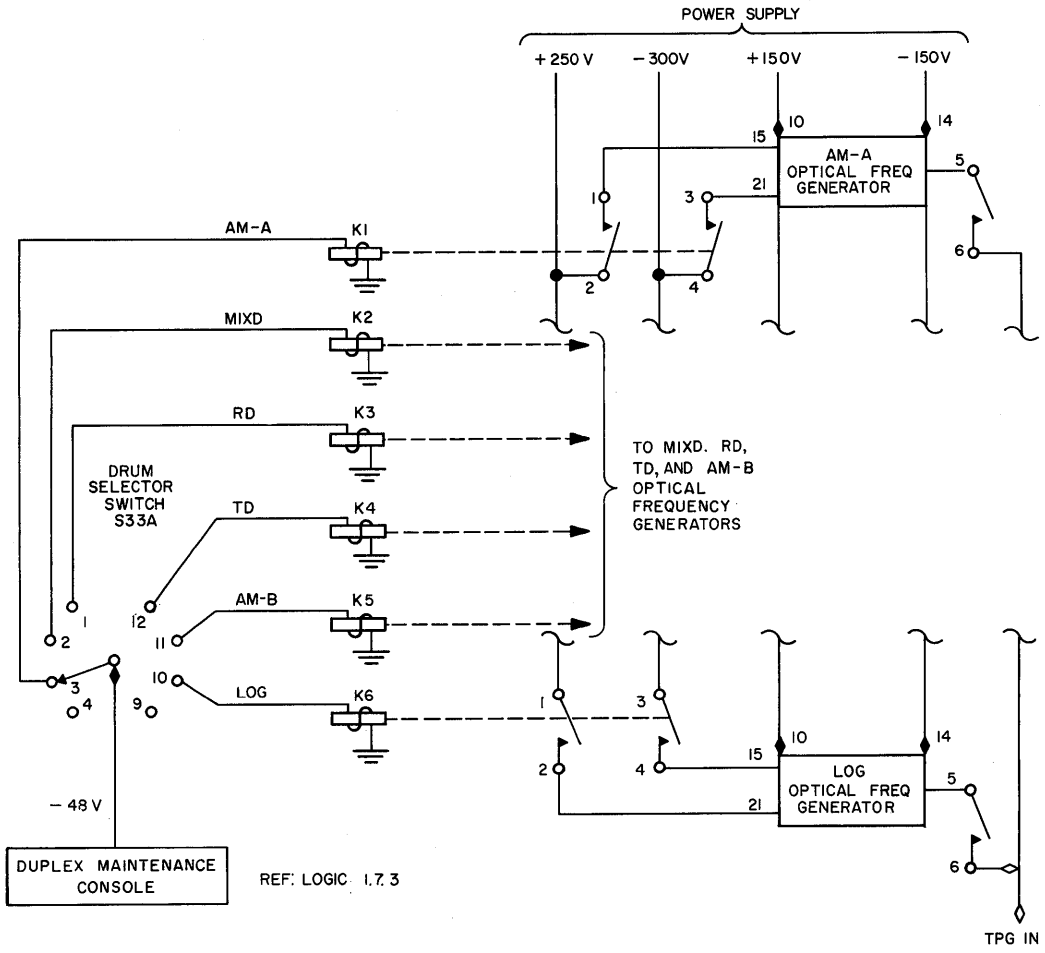


Figure 5–24. Drum Timing and Index Channel Writing, Selection Switches, Simplified Schematic Diagram

MODE SELECTION switch S2 on the test door of module 21L is in the MANUAL TEST position.

When the erasure operation is completed, a drums-erased level (fig. 5–25) is applied to control relay K3. The contacts of K3 close, causing +10V to be applied to pulse generator (PG) 1, which thereupon generates a single 0.1-usec pulse.

The output of PG 1 triggers single-shot multivibrator $_{C}$SS. The single-shot multivibrator triggers PG 2, which cannot be triggered again until the 60-ms delay of $_{C}$SS has expired. The output of PG 2 triggers single-shot multivibrator $_{B}$SS, whose waveform persists for 30 ms. The output of $_{B}$SS goes to GT 2 to operate as a conditioning level and to inverter 1 to prevent conduction in GT 4.

During the 30 ms that GT 2 is conditioned, TP 1 pulses from the timing pulse generator are passed to set FF 2 and clear FF 3. The 0-state output of FF 3 goes to drum writer 2. The 1-state output of FF 2 conditions GT 3 to pass the TP 3 pulses from the timing pulse generator. Each TP 3 pulse passed in this manner goes to the pulse stretcher. In the pulse stretcher, the TP 3 pulse clears FF 4 and sets it 2.0 usec later via the action of the delay line. During the 2.0 usec when FF 4 is in the 0 state, the drum write driver conducts, transferring the contents of the drum writers to the drum heads. The contents of the drum writer for the timing channel will always be 1 bits. During the 30 ms that GT 2 is conditioned, the contents of the index drum writer will be 0's. In this manner, 1 bits are placed in the timing channel once every TP 3 time for 1½ drum revolutions. Since the sine-wave etching on the optical timing disc is continuous, having no distinguishable beginning or end, and since the sine waves on this disc cause the generation of TP 3 pulses, 1 bits written during the first half of the second drum revolution are written directly over those written during the first drum revolution.

During the time that the timing channel head is writing 1 bits, drum writer 1 feeds 0 bits to the write head on the index channel.

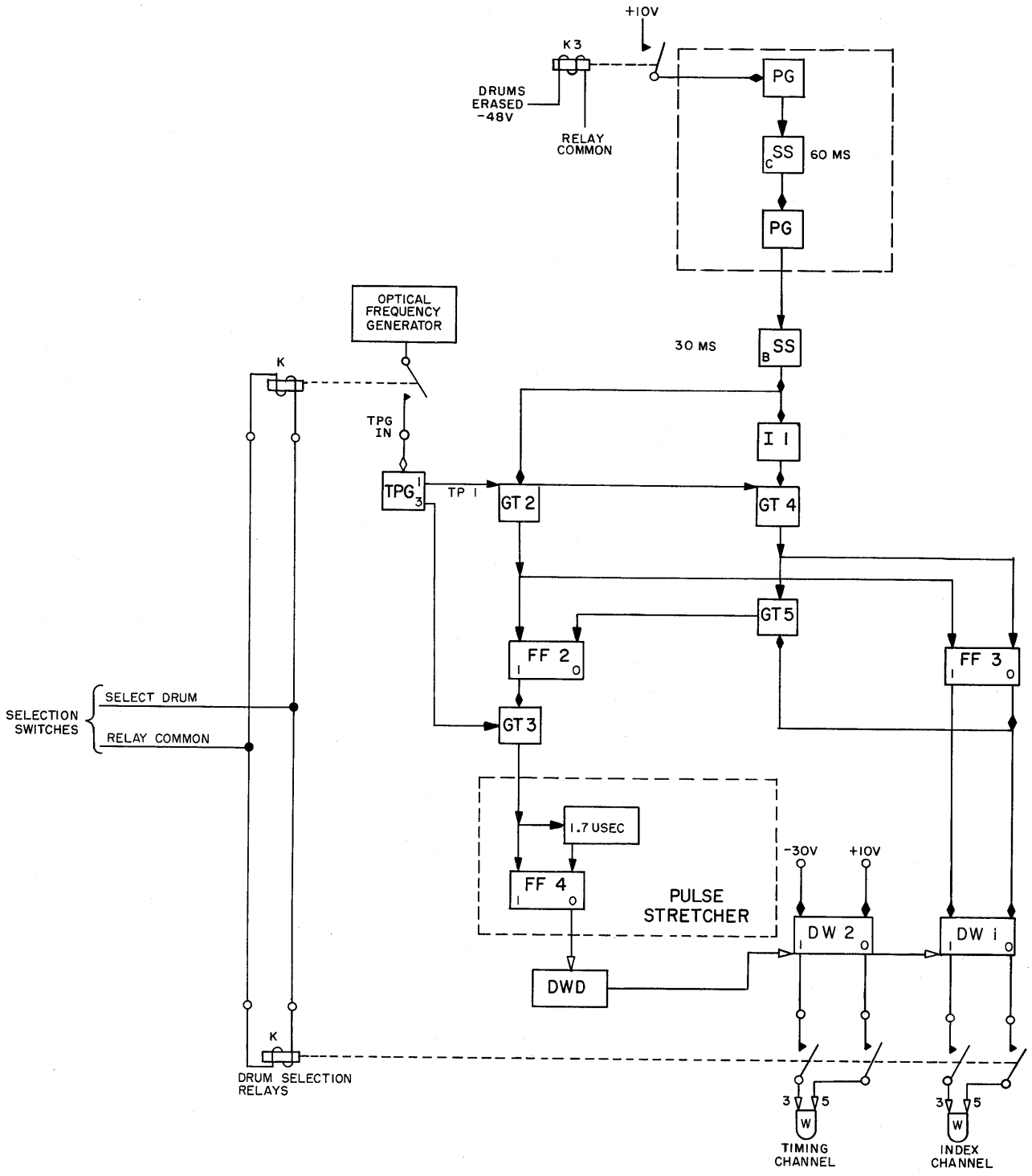


Figure 5–25. Timing-and-Index-Channel-Write Circuit, Simplified Logic Diagram

When the 30 ms are over, the output of the single-shot multivibrator goes negative. Gate 2 is no longer conditioned, and inverter 1 conducts, conditioning GT 4. Gate 4 passes TP 1 pulses to set FF 3. Flip-flop 3 now places a 1-state level in drum writer 1; this 1 output also conditions GT 5. The next TP 3 pulse is passed by GT 3 and sent to the pulse stretcher. The pulse stretcher output, in turn, causes a single 1 bit to be written in the index channel. The next gated TP 1 pulse is passed by GT 5, thereby clearing FF 2 and

preventing further production of pulses by the drum write driver. Thus, operation of the timing-write circuit causes the writing of 2,048 (or 2,060 in the case of the RD and TD drums) 1 bits in the timing channel and a single 1 bit in the index channel of the selected drum.

4.3.3 All Drums Timing and Index Channel Sequential Write

In the event that all drums are selected for erasure, they are all erased simultaneously. The writing of the timing and index channels of the drums starts automatically after the erasing operation. This operation is performed on one drum at a time, the drums being automatically selected in sequence.

Figure 5–26 illustrates the drum sequential selection circuitry. At the start of the drum erasing operation (described in 4.3.1), relay K1 is energized by 115V from the erase motor cam switch. Stepping relay K9 is energized via the contacts of K1. When K9 is energized, its stepping mechanism is cocked. At the conclusion of the drum erasing operation, K1 and K9 are de-energized. When K9 is de-energized, its stepping mechanism is tripped, causing the contact arm of deck A to move from the OFF position to the first position (AM-A). In the AM-A position, the AM-A drum selection relay (K1, fig. 5–24) is energized, selecting the AM-A drum for the timing-and-index-channel write operation.

At this time, +10V from deck B of K9 is applied to PG 1, which thereupon generates a single 0.1-usec pulse. This pulse triggers single-shot circuit 1, producing a positive level of 60-ms duration, which conditions PG 2. The output of PG 2 triggers single-shot circuit 2, producing a positive level of 30-ms duration. The output of single-shot circuit 2 is applied to the timing-and-index-channel write circuit to initiate the writing of the timing and index channels. (Refer to 4.2.1.5 of part 2 for a description of the timing-and-index-channel write operation.)

The output of single-shot circuit 2 is also applied to PG 3, whose output triggers single-shot circuit 2. The output of single-shot circuit 2 persists for 60 ms, during which time the vacuum-tube relay driver contacts are closed, generating the timing-and-index-channel-written level. This level energizes relay K8. Actuation of K8 causes the erase-select-all level from selector switch S1 to re-energize K9, thereby cocking the stepping mechanism. The timing-and-index-channel-written level persists for 60 ms; at the end of this time, K8 and K9 are de-energized. When K9 is de-energized, its stepping mechanism is tripped, causing the contact arm to move from the first position (AM-A) to the second position (MIXD). In the MIXD position, the MIXD drum selector relay is energized, selecting the MIXD drum for the timing-and-index-channel write operation.

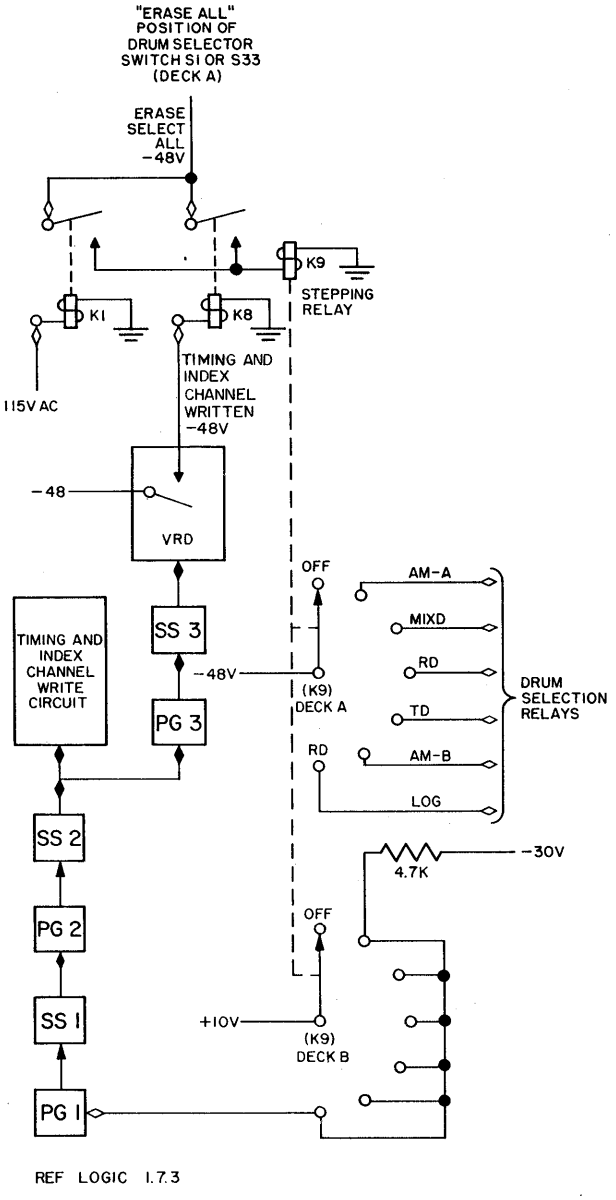


Figure 5–26. Timing-and-Index-Channel-Write Sequencing, Simplified Schematic Diagram

The foregoing operation is repeated until the timing and index channels of the six drums are written. At the completion of writing on the last drum, the stepping relay contact arm will have progressed to the OFF position in preparation for a new erase-rewrite operation.

4.4 STATUS-CONTROL-CHANNEL-MANUAL-TEST CIRCUITS

The paragraphs that follow describe the manual-test operations which are used to check the status-control function. To check the status-control channels of the fields that read and write by status control, 1 or 0 bits are written in the OD and the CD status channels and are read back to make certain that no errors have occurred. The manner in which the status channels are manually written and later checked to detect possible errors is described in 4.4.1 through 4.4.6.

4.4.1 Writing the Status Channels for Manual Test

The circuits employed to write 1's or 0's manually in the status channels of the status-controlled fields are shown in figures 5–27 and 5–28. If it is desired to fill the status channels for a given field with 1 or 0 bits, a manual-test level is produced in the begin-manual-test circuit (4.2.1). The manual-test level is sent to the select-manual-test-read-or-write-operation circuit and to the manual-test-field-selection circuit. The field whose status channels are to be written is manually selected in the manual-test-field selection circuit by producing a deselect pulse and the necessary combination of manual-selection pulses. The deselect pulse and the selected combination of manual-selection pulses go to the CD selection circuits, where they produce a test-select-input-field-level. In figure 5–27, the GFI field is shown as an example. The same operations will be true for the other three input data and three OB-data-status-control circuits. The select GFI input level, in this case, goes to the computer-test-control circuit.

If it is desired to write 1 bits in the status channel of the selected field, a manual-start-write pulse is developed in the select-manual-test-read-or-write-operation circuit. If it is desired to write 0 bits in the status channel, a manual-start-read pulse is produced.

During the writing of 1 bits, the manual-start-write pulse goes to the computer-test-control circuit and the CD-read-write-control circuit. The combination of the select-GFI level from the CD selection circuits and the manual-start-write pulse in the computer-test-control circuit produces a test-write-GFI level, which goes to AND 1 in the GFI-OD-status-control circuit and to the manual-test-read-write-1-revolution-control circuit. The manual-test-read-write-1-write-revolution-control circuit is manually adjusted to produce a drum-disconnect pulse at the end of one revolution of the selected field. (Refer to 4.2.7 for a discussion of the manual-test-read-write-1-revolution-control circuit.) The drum-disconnect pulse goes to the CD-read-write-control circuit and produces a read-write-reset pulse. The read-write-reset pulse goes to the computer-test-control circuit and removes the test-write-GFI level.

AND 1, which is fed by the test-write-GFI level during the writing of 1 bits, conducts when it also receives a +10V level from the 1 side of FF 2. Flip-flop 2 is set to the 1 side by the presence of a 0 bit in the OD status channel. A 0 bit in the status channel produces a read circuit output too late to condition GT 1 to pass an OD 1 pulse from the LOG drum timing circuit. Flip-flop 1 therefore remains in the cleared state that resulted from the arrival of the previous OD 4 pulse. The 0 side level from FF 1 conditions GT 2 to pass the next OD3 pulse. The gated OD 3 pulse sets FF 2. The FF 2 output joins the test-write-GFI level at AND 1. The resulting output of AND 1 conditions GT 3 to pass an OD 2 pulse, which forms a test-data-available pulse input to OR 1. Normally, OR 1 gets data-available pulses from the Input System element with which the GFI-OD-status-control circuit is associated. Thus, OR 1 conducts upon receipt of the test-data-available pulse and, in turn, causes conduction in OR 2. OR 2 will also conduct as a result of detection of a 1 bit in the OD status channel. In this circumstance, FF 1 is set, but FF 2 remains in the cleared state in which it was placed by the previous OD 2 pulse. The 0-state-output level of FF 2 conditions GT 4 to pass an OD 1 pulse to OR 2. When OR 2 conducts, its output sets FF 3, causing a 1 bit to be written in the CD status channel when the status-write-sample pulse is received.

It can be seen that, when a 1 bit is already present in the OD status channel, a 1 bit is automatically placed in the CD status channel. If a 0 bit is detected, a test-data-available pulse is produced because of the presence of the test-write-GFI level from the computer-test-control circuit. The test-data-available pulse substitutes for the data-available pulse produced during normal operation and causes the writing of a 1 bit in the CD status channel. Therefore, 1 bits are written in the CD status channel regardless of whether a 0 or a 1 is read in the OD status channel.

At the same time that 1 bits are being written in the CD status channel, 1 bits are also being written in the OD status channel. This operation is accomplished as follows: after the 1 bits have been written in the CD status channel, the individual bits pass under the CD status channel read head as the drum rotates (fig. 5–28). The read head is located in the CD-status-control circuit. The 1 bits are detected by the read circuit so that GT 1 is conditioned to pass one CD 1 pulse from the LOG drum timing circuit for each 1 bit on the channel. The GT 1 output goes to GT 2. Gate 2, in turn, is conditioned to pass the CD 1 pulses in the following manner: since a manual-test-write pulse is produced during the writing of 1 bits, the read-by-status level from the CD read-write-control circuit is absent at AND

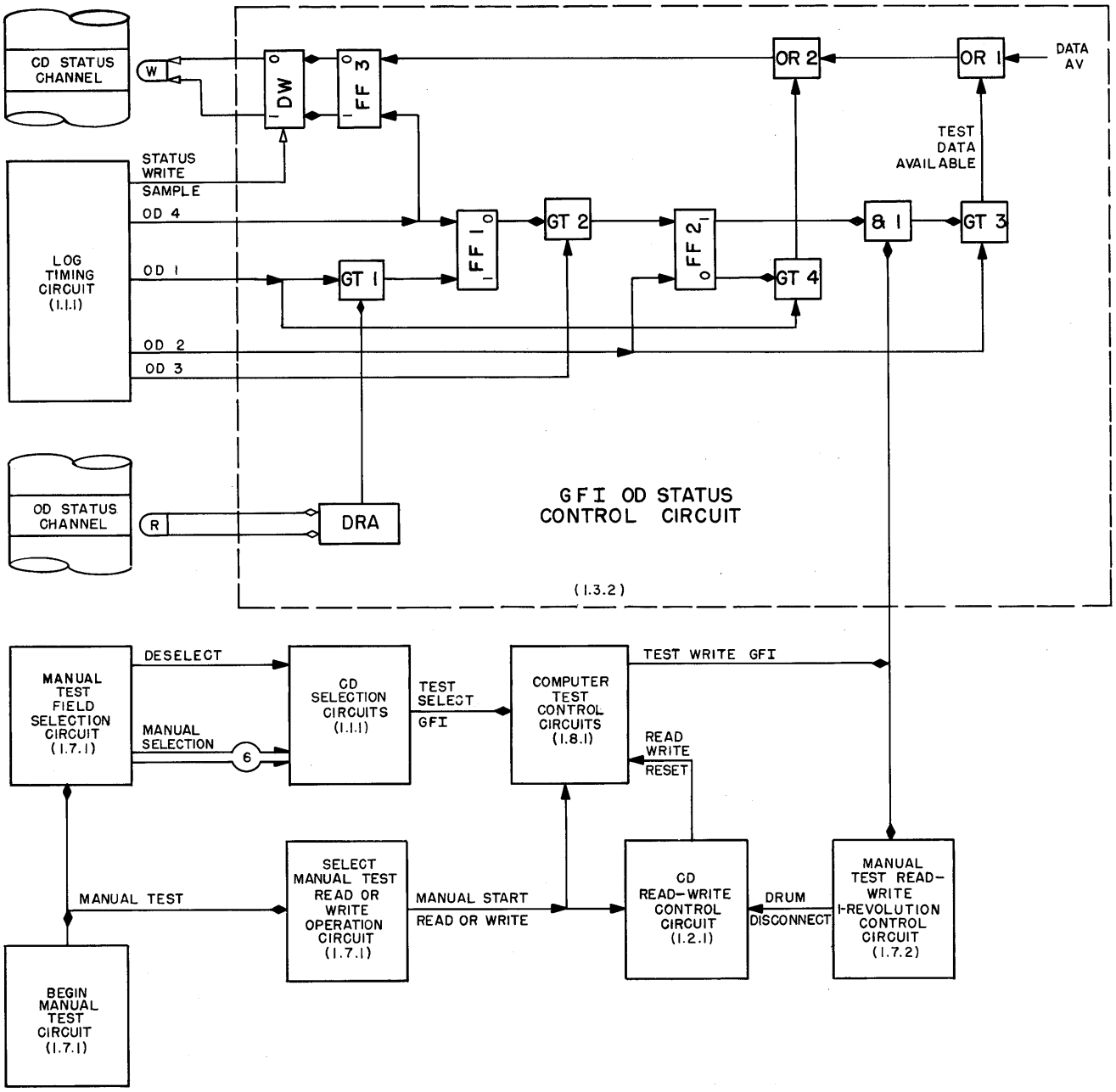


Figure 5–27. Writing CD Status Channel for Manual Test, Simplified Logic Diagram

1. With this level absent, AND 1 cannot conduct, thereby causing inverter 1 to produce an output level which conditions GT 2 to pass the CD 1 pulses from GT 1. The GT 2 output sets FF 1 via OR 1. The 1-state level of FF 1 causes the drum writer to write 1 bits in the OD status channel on receipt of status-write-sample pulses. This operation stops at the end of one revolution of the selected field. While the operation is in progress, however, 1 bits are written in every space on both the OD and CD status channels.

When it is desired to write 0 bits in the status channels, a manual-start-read pulse is produced by the select-manual-test-read-or-write-operation circuits. The manual-start-read pulse goes to the CD-read-write-control circuit, enabling the CD-read-write-control circuit to produce a read-by-status level. The read-by-status level goes to AND 1 in the CD-status-control circuit (fig. 5–28). At this time, AND 1 conducts, cutting off inverter 1 and conditioning GT 3. If a 1 bit is detected in the CD status channel, GT 1 passes a CD 1 pulse, not

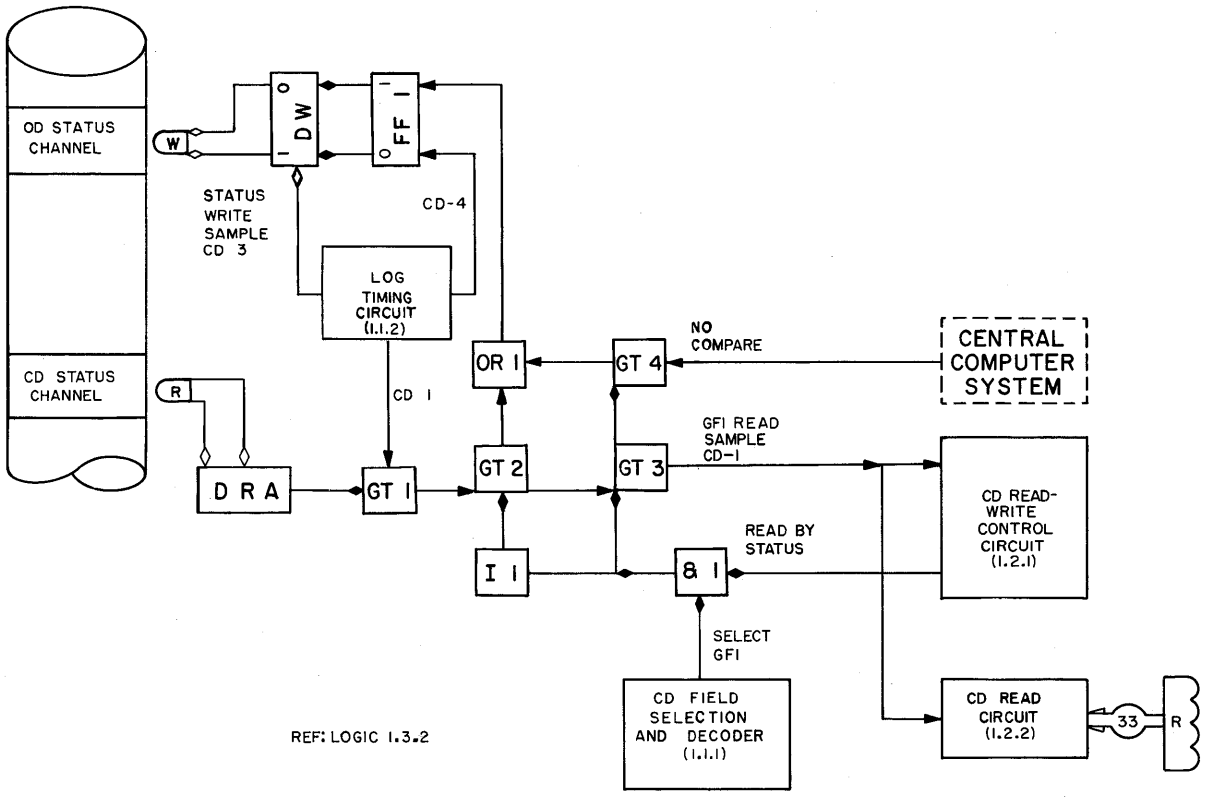


Figure 5–28. Writing OD Status Channel for Manual Test, Simplified Logic Diagram

only to GT 2, but also to GT 3. The latter produces a read-sample pulse which goes to the CD-read-write-control circuit. Since the Drum and Central Computer Systems are both in test operation, the no-compare pulse (normally returned when a word is to remain on a drum register) is not produced. Gate 4 receives no pulse input, and, therefore, no pulse appears at its output to produce conduction in OR 1. With no input to OR 1 and with GT 2 deconditioned, FF 1 remains in the 0 state in which it is placed by each CD 4 pulse from the LOG drum timing circuit. When a status-write-sample pulse is received, the drum writer places a 0 in the OD status channel.

After the bits are written in the OD status channel by the write head in the CD-status-control circuit, the drum rotates until the bits come under the read head in the OD-status-control circuit (fig. 5–27). The absence of a manual-start-write pulse prevents the production of the test-write-GFI level. With no test-write-GFI level present in the GFI-OD-status-control circuit, the test-data-available pulse is not produced. Therefore, OR 1 does not conduct. Since only 0 bits have been written on the OD status channel by the OD-status-control circuit, all bits detected by the read head on the CD side are 0 bits. Flip-flop 1 is cleared throughout the drum revolution. Gate 2 thus passes every OD 3 pulse around the drum to set FF 2. Since FF 2 is always set at OD 3 time, an OD 1 pulse cannot be passed in GT 4 to produce conduction in OR 2. With the two input sources of OR 2 removed, FF 3 remains in the cleared state in which it is placed by each OD 4 pulse. Each status-write-sample pulse entering the drum writer from the LOG drum timing circuit thus causes the writing of a 0 bit. In this manner, the two status channels on each field can be filled with all 0 bits or all 1 bits.

4.4.2 Circuit Selection for Status-Control Manual Test

Selection of status-control testing is accomplished by means of OB SELECTOR switch S5, ONES-ZEROS switch S4, and CIRCUIT SELECTOR switch S3. Figure 5–29 shows in diagram form the interrelation of these controls. A manual-test level from the begin-manual-test circuit is applied to ONES-ZEROS switch S4 and OB SELECTOR switch S5. The position of switch S4 determines whether ONES or ZEROS are on the status-control channel to be checked. In the ONES position, the manual-test level is applied to the pole of the A wafer of CIRCUIT SELECTOR switch S3. In the ZEROS position, the manual-test level is applied to the pole of the B wafer of CIRCUIT SELECTOR switch S3.

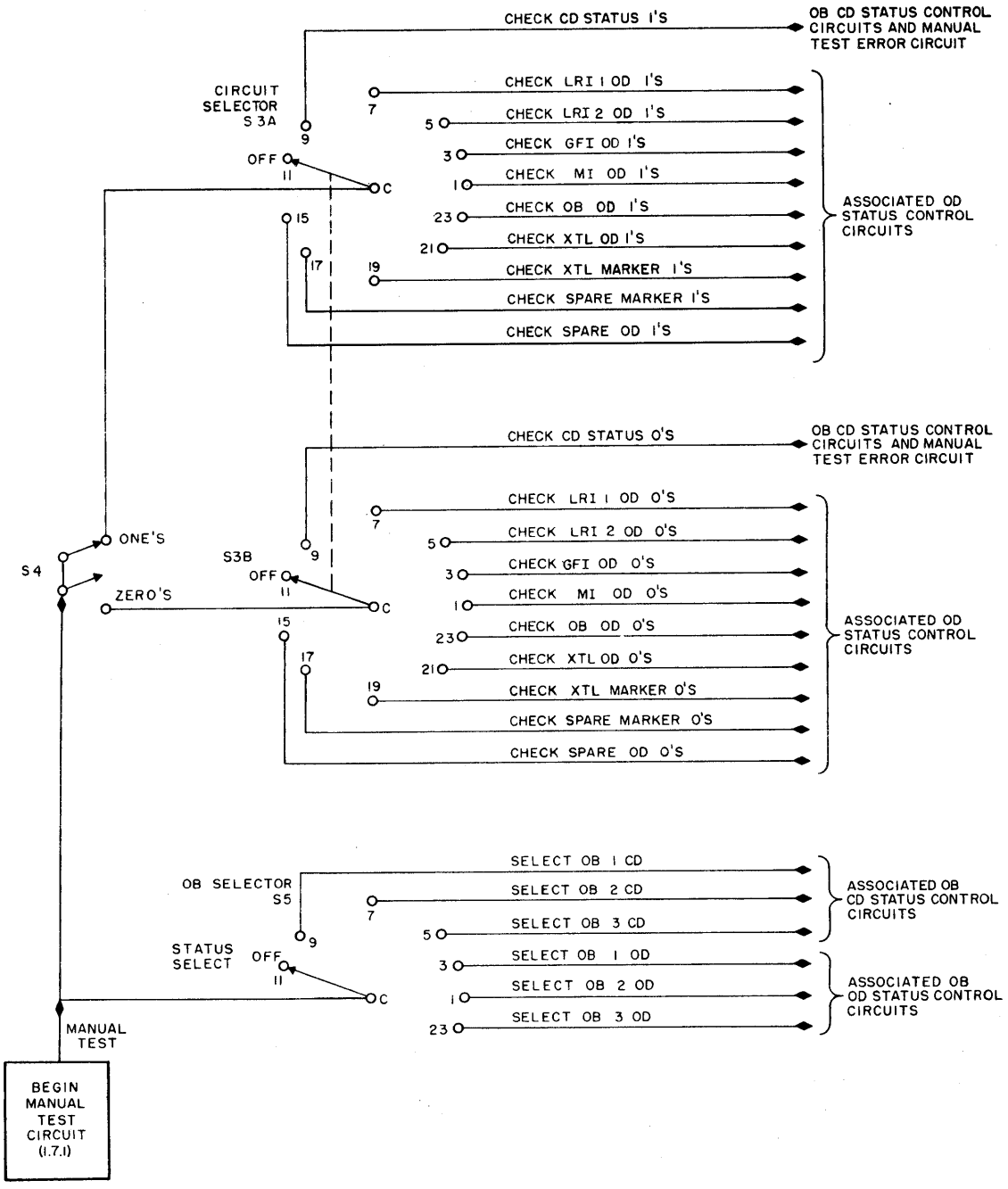


Figure 5–29. Field Selection Circuits for Status Control Channel Tests

The position of this switch determines which of the two status-control channels of a field is to be checked.

It can be seen that, with S4 in the ONES position and S3 in the OD-MI position, the manual-test level is applied to contact 3 of S3A, producing a check-MI-OD-1's-output level. This level goes to the MI-OD-status-control circuit to check the OD-status-control channel. In the same way, a check 1's or check 0's level can be sent to the status-control circuit for any field employing status control. When the CD-status-control channel of any of the fields is to be checked, switch S3 is operated to the CD position.

An additional condition is imposed upon the status-control channel test for the OB fields. In addition to the setting of switch S4 to select a check of 1's or 0's and the setting of switch S3 to select OB OD or CD status-control channels, OB SELECTOR switch S5 must be operated to select the specific OB field to be checked. To test for 1's in the OD status-control channel for OB field 2, for instance, switch S4 has to be operated to the

ONES position, switch S3 has to be operated to the OD-OB position, and switch S5 has to be operated to the OB 2 OD position.

4.4.3 Manual Test for Input Fields OD Status Channels

The portions of the OD-status-control circuits that are used to check 1's or 0's after they have been written are shown in figure 5–30. During either check, the check-selected-status-circuit-OD-1's level is produced by setting the switches in the manual-test-for-status-control-selection circuits to the desired positions. When 1's are being checked, the check-selected-status-circuit-OD-1's level is sent to GT 1. (In fig. 5–30, the GFI field is chosen as an example.) If one of the bits in the OD status channel is a 0 instead of a 1, FF 1 remains in the 0 state in which it has been placed by the last OD 4 pulse. The 0 state output of FF 1 conditions GT 3 to pass an OD 3 pulse to GT 1. Since GT 1 is conditioned by the GFI-check-status-circuit-OD-1's level, the OD 3 pulse is passed to the manual-test-error circuit as an error-1's pulse. In the manual-test-error circuit (4.2.9), the error-1's pulse stops drum operation.

When 0's are being checked, the GFI-check-status-circuit-OD-0's level is sent to GT 4. If one of the bits in the OD status channel is a 1 instead of a 0, FF 1 is set. Gate 3 is therefore not conditioned in time to pass an OD 3 pulse. As a result, FF 2 remains in the 0 state in which it has been placed by the previous OD 2 pulse. The 0-state output of FF 2 conditions GT 5 to pass an OD 1 pulse. The gated OD 1 pulse is sent to GT 4. Since GT 4 is conditioned by the GFI-check-status-circuit-OD-0's level, the GT 5 output is passed to the manual-test-error circuit as an error-0's pulse. The error-0's pulse also stops drum operations.

During manual test write procedure for the selected field, the presence of a 0 in the OD status channel also produces an error-0's pulse. At such time, FF 1 again remains cleared long enough to pass an OD 3 pulse in GT 3. The GT 3 output sets FF 2. The 1-state output of FF 2 is added in AND 1 with the GFI-test-write level produced in the computer-test-control circuit when a manual test is selected. The resulting conduction in AND 1 conditions GT 6 to pass an OD 2 pulse, which forms a test-data-available pulse. The test-data-available pulse goes to the complement-test-pattern circuit to produce the pattern-sense pulse (4.2.5).

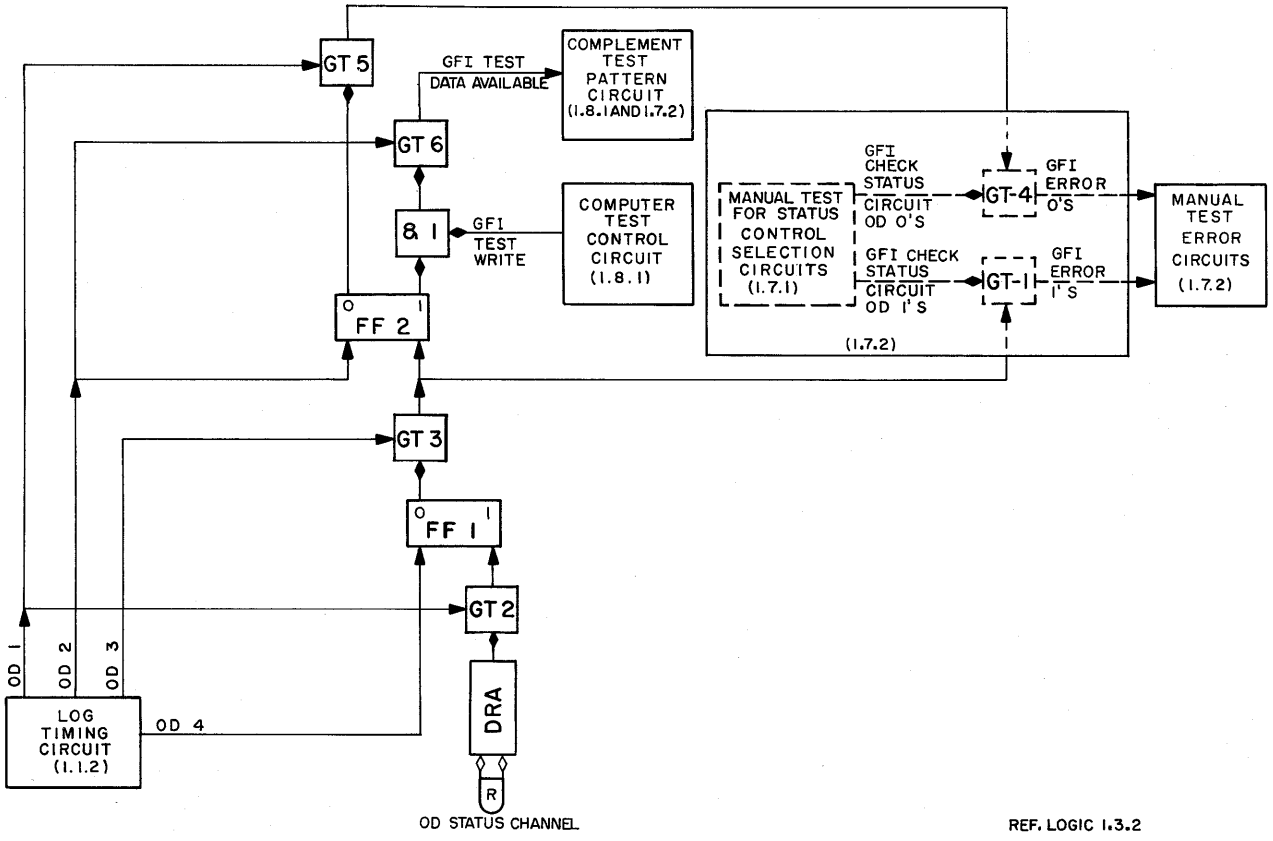


Figure 5–30. Manual Test Components of GFI-OD Status Control Circuit, Simplified Logic Diagram

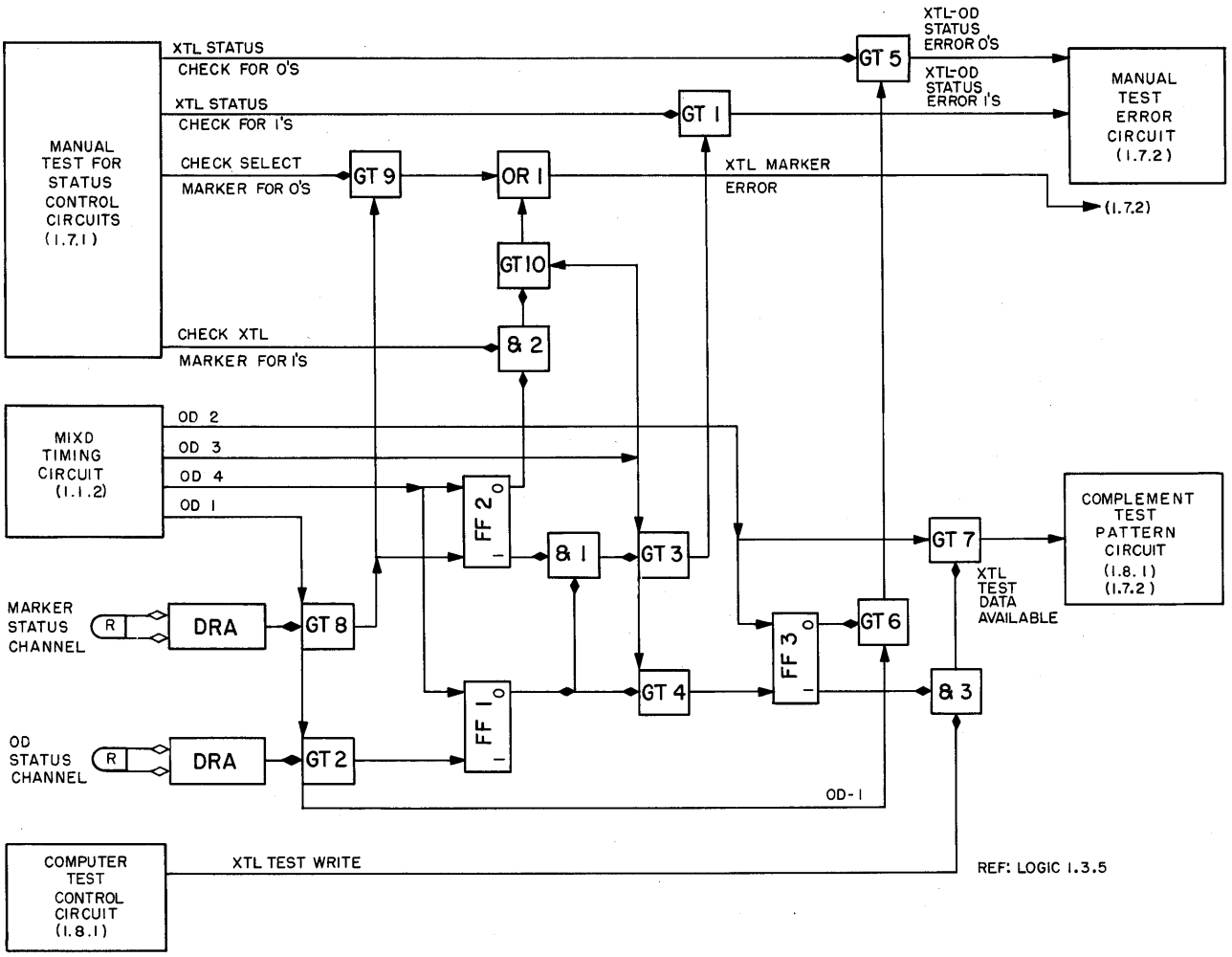


Figure 5—31. Manual Test Components of XTL-OD-Status-Control Circuit, Simplified Logic Diagram

4.4.4 Manual Test for Marker-Status Channels

The check status channel OD 1's and 0's procedures are modified when the marker-status-control circuits are being examined. Figure 5—31 is a diagram of the XTL-OD-marker-status-control circuit. If a check is made for 1's in the OD status channel, the presence of a 0 in the OD channel permits FF 1 to remain cleared. The FF 1 output is added in AND 1 to the output of FF 2 (present when a 1 is read in the marker-status channels). The output of AND 1 goes to GT 3 to condition the gating of an OD 3 pulse. The GT 3 output is passed by the XTL-status-check-for-1's level at GT 1. The GT 1 output is the error-1's pulse, which goes to the manual-test-error circuit. Thus, the only modification of the 1's check for the OD status channel in the marker-status-control circuits is the added condition of the presence of a 1 in the marker-status channel when the OD status channel is read.

The check for 0's in the marker-status-control circuit is identical with the check for 0's in the normal-status-control circuit. If a 1 is present in the OD status channel, FF 3 remains cleared. Gate 6 is conditioned to pass an OD 1 pulse to GT 5. This pulse is gated by the XTL-status-check-for-0's level to form an error-0's pulse, which goes to the manual-test-error circuit.

Additional facilities are provided to check the contents of the marker-status channel. If the marker-status channel has been written to contain all 0's, the check-select-marker-for-0's level is produced in the manual-test-for-status-control circuits. This level conditions GT 9 to pass an output from GT 8. Gate 8 has an output only when a 1 is read in the marker-status channel. The output of GT 9 produces conduction in OR 1. The pulse output of OR 1 is the XTL-marker-error pulse, which goes to the manual-test-error circuit and stops drum operations.

When all the bits in the marker-status channel have been written as 1's, the check-XTL-marker-for-1's level is produced in the manual-test-for-status-control selection circuits. This provides an input to AND 2, which

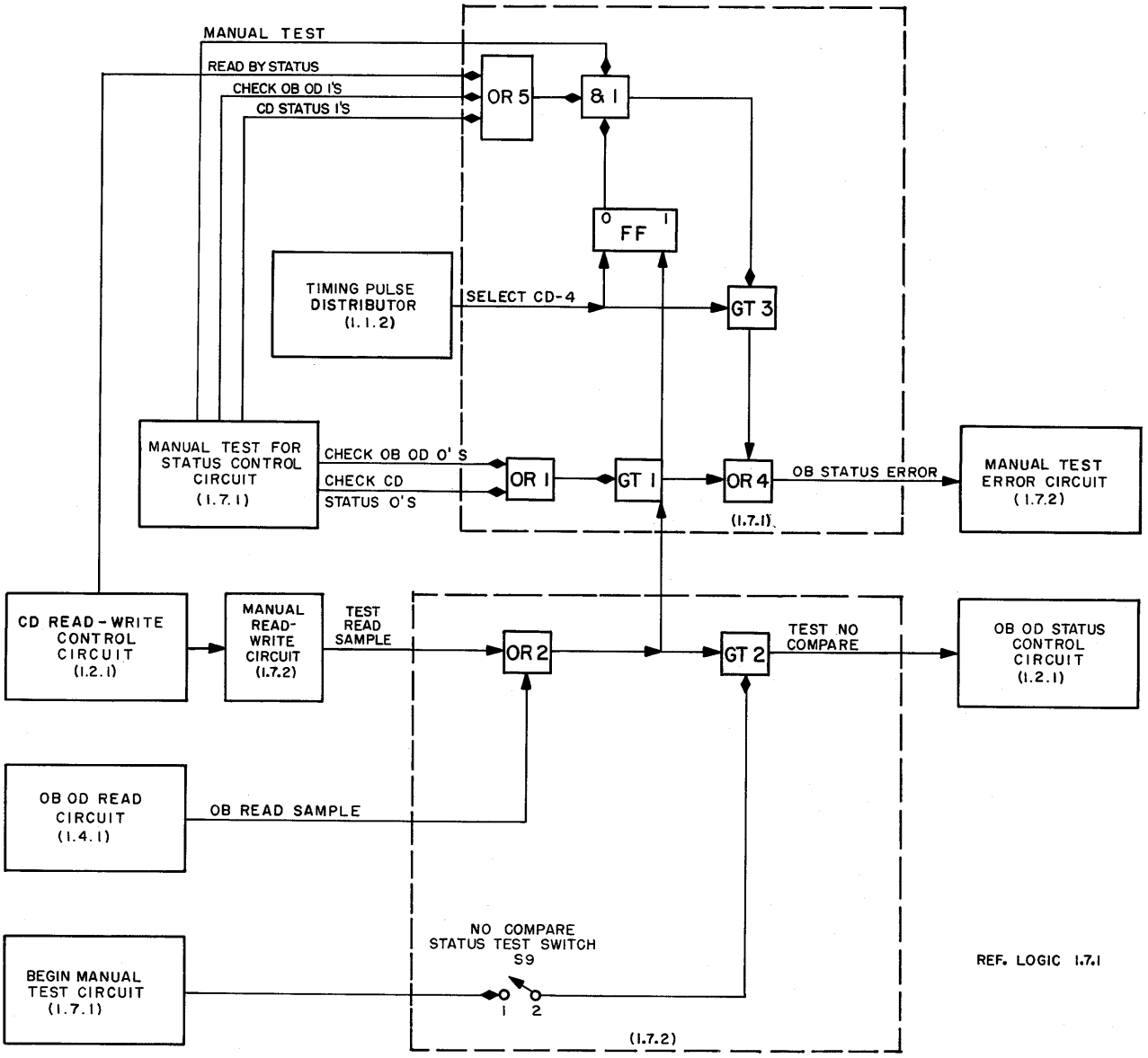


Figure 5–32. Manual-CD-Status-and-OB-CD-Status-Test-Control Circuit, Simplified Logic Diagram

conducts only if FF 2 remains cleared at the OD 1 pulse following the OD 4 pulse which clears it. Flip-flop 2 remains cleared only when the channel contains a 0 bit, and GT 8 does not pass a setting pulse to FF 2. When AND 2 does conduct, GT 10 is conditioned to pass an OD 3 pulse to OR 1, and the XTL-marker-error pulse is produced. (The test-data-available-pulse circuit is described in 4.4.3.)

4.4.5 Manual Test for Input Fields, CD Status Channels, and OB OD Status Channels

One portion of the manual-test circuits is used specifically to perform 1's and 0's checks on the CD status channels of the input fields and the OD status channel of the three OB fields (fig. 5–32).

During a check for 0's in any of the above-mentioned fields, a check-OB-OD-0's or a check-CD-status-0's level, as the case may be, is fed to OR 1. Thus, OR 1 conducts, sending a conditioning level to GT 1. Gate 1 receives a pulse input if the selection of any status-control circuit for the check results in the production of a read-sample pulse (an OB-read-sample pulse from the OB OD read circuit, or a test-read-sample pulse from the CD-read-write-control circuit). A read-sample pulse can be developed by one of these circuits only when a 1 bit is detected in the respective CD status channel or OD status channel of the OB field that is being tested. The read-sample pulse from any of the possible sources provides the necessary input to GT 1. The resulting

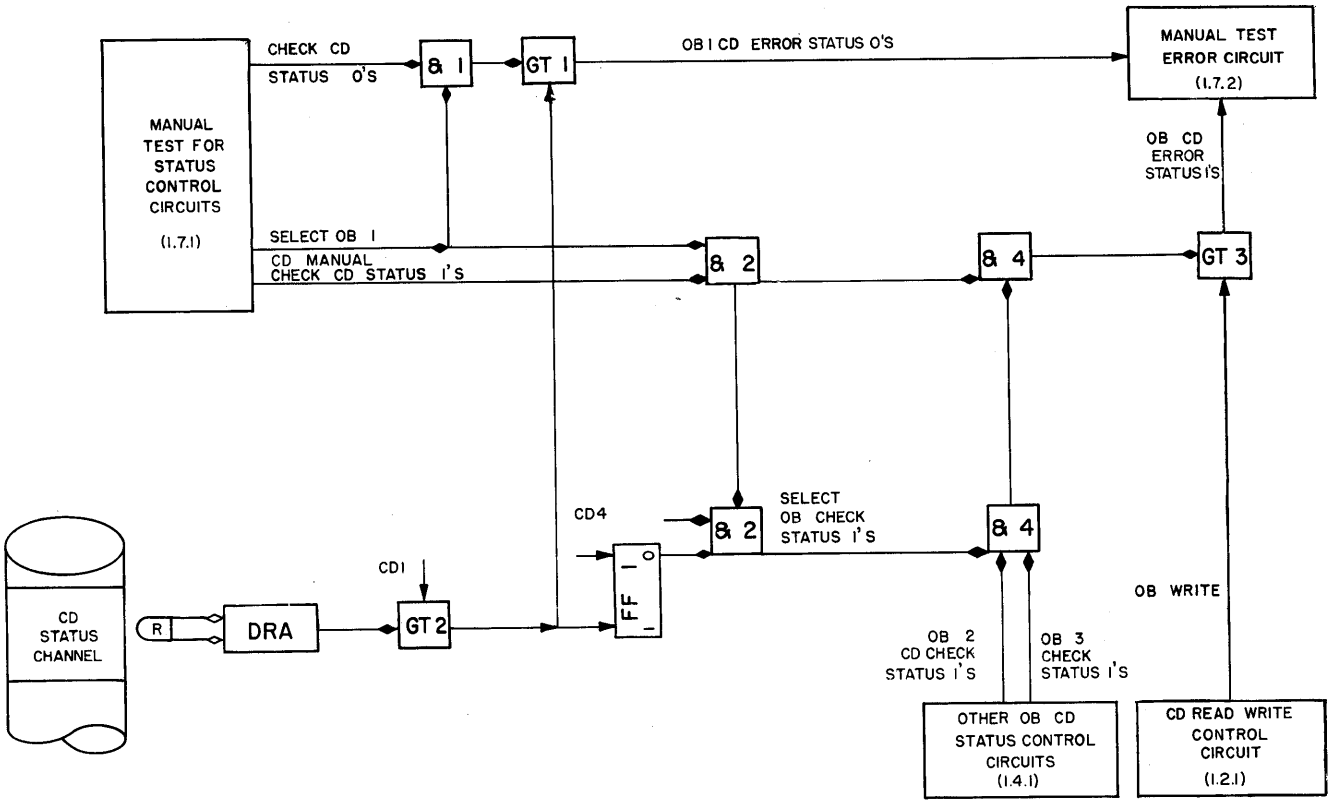


Figure 5–33. Test Components of OB1 OD-Status-Control Circuit, Simplified Logic Diagram

GT 1 output goes to OR 4, forming an OB-status-error pulse, which goes to the manual-test-error circuit and stops drum operations.

The principle that read-sample pulses are produced only when a 1 bit is read in the selected-status-control circuit is employed in the check for 1's in the status channels.

The check-CD-status-1's level, the check-OB-OD-1's level, and the read-by-status level are brought into OR 5. The output of OR 5 is added to the manual-test level from the manual-test-for-status-control circuit and the 0-state level of the flip-flop in AND 1. If either read-sample pulse is present at OR 2, the flip-flop is set. If, however, there is a zero in the status channels, the read-sample pulses are not produced, and the flip-flop remains in the cleared state produced by a select-CD 4 pulse from the timing pulse distributor. AND 1, when conductive, produces the operating level for GT 3, which then passes the next select-CD 4 pulse. If the flip-flop had remained set, the rise time of the 0 side of the flip-flop would have exceeded the select-CD 4 pulse time. With GT 3 conditioned in time to pass the select-CD 4 pulse, however, an input is sent to OR 4. The OR 4 output is the OB-status-error pulse.

Should it be desired to perform a test requiring the use of a test-no-compare pulse, switch S9, the NO COMPARE STATUS TEST switch, is closed. This applies a manual-test level from the begin-manual-test circuit to GT 2. Should a read-sample pulse be produced, it is passed at GT 2 to form a test-no-compare pulse, which goes to the OB-OD-status-control circuit.

4.4.6 Manual Test for OB CD Status Channels

The portion of the CD-OB-status-control circuit used during a manual test check for the contents of the OB CD status channel is shown in figure 5–33. To check 0's or 1's, the select-OB-1-CD-manual level must be produced in addition to the check levels. When checking for the presence of 0's in the channel (1's are errors), the select-OB-1-CD-manual level is added with the check-CD-status-0's level in AND 1. The output of AND 1 conditions GT 1. Gate 1 receives an input only if an error is present; that is, a 1 in the status channel. The resulting output of GT 1 is the select-OB-CD-error-0's pulse.

When checking for 1's in the channel (0's are errors), the select-OB-1-CD-manual level is added with the check-CD-status-1's level in AND 2. The output of

AND 2 goes to AND 3, which conducts only if it gets another input from the 0 side of FF 1. Flip-flop 1 is cleared by each CD 4 pulse. If a 1 is read in the channel, FF 1 is set, and AND 3 can have no input. Flip-flop 1 remains cleared when a 0 (error) is detected in the CD status channel. The output of AND 3 produces conduction in OR 1, which also conducts if it receives a similar output from either of the other two OB-CD-status-control circuits. The OR 1 output goes to AND 4, which is also fed by the check-CD-status-1's level from the manual-test-for-status-control circuits. With both inputs present, AND 4 conditions GT 3 to pass the OB write pulse from the CD-read-write-control circuit. The write pulse which is passed forms the OB-CD-error-status-1's pulse, which goes to the manual-test-error circuit and stops drum operations.

PART 6
DRUM SYSTEM IN A COMBAT CONTROL CENTRAL

6.1 GENERAL

The AN/FSQ-8 Combat Control Central has been equipped to exercise all the functions performed by the AN/FSQ-7 Combat Direction Central, except the processing of radar data. Therefore, the Drum System in the AN/FSQ-8 equipment, although designed identically as the Drum System in the AN/FSQ-7 equipment, has no facilities for RD transfer. A comprehensive block diagram of this system is shown in figure 6—1. The long-range radar input (LRI) and gap-filler radar input (GFI) fields are not included. Consequently, the RD drum fields have been removed.

Since the corresponding areas in the AN/FSQ-7 and AN/FSQ-8 Drum Systems operate identically, the contents of this manual apply to the AN/FSQ-8 Drum System with the exceptions listed in table 6—1.

The physical differences are primarily established by the removal of pluggable units which, in the AN/FSQ-7 System, contain the LRI, GFI, and RD field circuits, and also by the consequent disabling of the RD drum itself. To utilize the data storage space available in this drum, a circuit modification has been introduced in the AN/FSQ-8 Drum System. Through this modification, the TD drum has been redesignated as a TD-A

TABLE 6—1. AREAS OF TEXT NOT APPLICABLE TO COMBAT CONTROL CENTRALS

PART	CHAPTER	PARAGRAPH	REMARKS
1	3	3.3.6	References to LRI and GFI fields do not apply.
		3.3.8	References to RD display information do not apply.
2	1		References to LRI, GFI, and RD fields do not apply.
	4	4.2.3	Descriptions of RD timing circuits do not apply.
		4.3.5	TD timing distribution is based on TD-A TD-B drum operation (Part 6). References to RD drum performance do not apply.
	5		All references made in this chapter to selection of RD fields are not applicable. When cyclic operation of the two display data drums is called for, Part 6 should be consulted.
		6.7	References made to LRI, GFI, and RD fields do not apply.
3	3	3.5	TD-RD drum handling of SD data does not apply. Description of TD-A TD-B drum operation described in Part 6 should be consulted.
4	1		References to LRI and GFI fields do not apply.
	2	2.3 2.4	GFI field descriptions are not applicable .
		2.5 2.5	LRI field descriptions are not applicable.
5	2	2.2.1	Situation display tests in the AN/FSQ-8 Drum System cover the TD-A TD-B operation.
	3	3.1	References made to testing of LRI and GFI fields do not apply.
	4		References made throughout this chapter to manual testing of LRI, GFI, and RD fields do not apply.

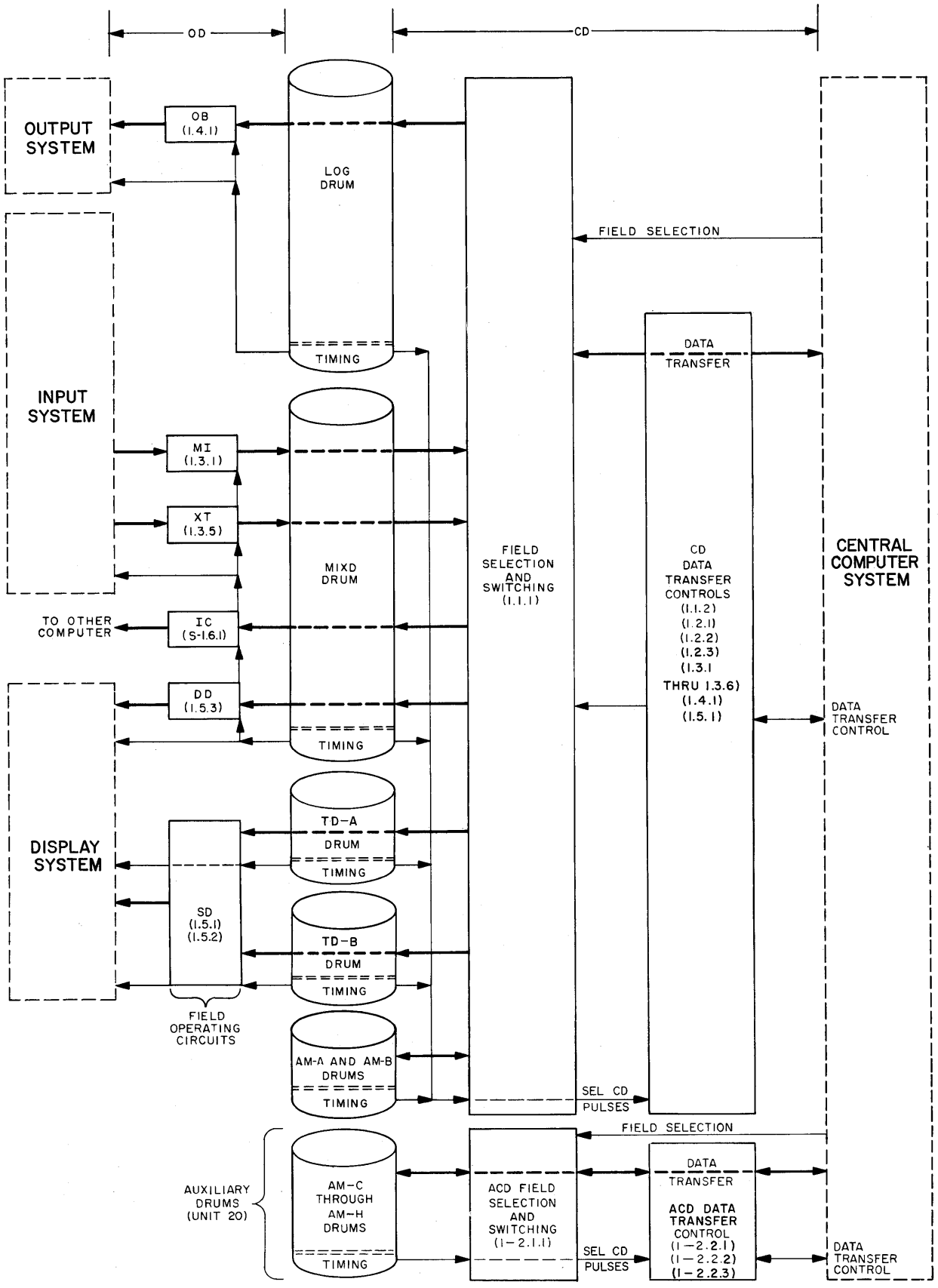


Figure 6–1. Drum System, Operational Block Diagram (AN/FSQ-8 Equipment)

drum and the other display drum as a TD-B drum. Depending upon the amount of data traffic at each AN/FSQ-8 site, the field capacity of the TD-A drum may suffice, or the two drums, TD-A and TD-B, may be operated in alternate sequence. In that case, the TD-B drum may supply 1, 2, 3, or up to 6 additional fields for storage and transfer of track data to the Display System. Display data transfer circuits in the AN/FSQ-8 Drum System are described in 6.2.

6.2 TRANSFER OF SITUATION DISPLAY IN AN/FSQ-8 EQUIPMENT DRUM SYSTEM

6.2.1 Overall Description

In the Drum System installed with the AN/FSQ-8 equipment, two display drums, TD-A and TD-B, contain identical OD-field-operate circuits to transfer track data to the Display System. In accordance with the amount of data traffic in each AN/FSQ-8 site, a minimum of six TD fields or a maximum of 12 TD fields may be supplied by the Drum System. When the minimum of six fields suffices, the TD-A drum is self-cycled; i.e., the six TD fields are read in sequence and, at the end of the sixth field, reading of the first field starts again. When more than six TD fields are required, the cycling takes place from the TD-A to TD-B drum and back to TD-A, in that alternate order. However, the six fields in the TD-A drum are always utilized, whereas the number of TD-B fields (from one to six) is determined by pushbutton setting at module E (auxiliary drum panel) of the duplex maintenance console. To illustrate, assume an AN/FSQ-8 site utilizing nine TD fields. In that particular Drum System, the six fields in the TD-A drum are read, then the three fields in the TD-B drum, back to the TD-A drum, and so on.

6.2.2 Track Data Transfer, Functional Description

Situation display reading begins in the OD display circuits (logic 1.5.1) when the Drum System is energized. A power-on-reset signal from the manual control panel is sent to the TD-A OD-read-control circuit (fig. 6–2). In the read-control circuit, the power-on-reset pulse produces a field-select level. This level goes to the TD-diode-switching circuit to cause the contents of field 1 to be switched into the SD drum switch. The drum switch enables the OD display circuits to use one set of read circuits for both TD-A and TD-B words by transferring the contents of the selected field from the drum that is being read to the SD OD read circuits. At the end of every 13th TD drum revolution, the field-select level is changed, switching the contents of fields 1 through 6, in that order, into the read circuits. The TD-A OD gap counter develops a 120-usec delay at the beginning of each revolution, which provides for decay of switching transients when fields are being switched. (Refer to Ch 6 of Part 2.)

The field contents are passed through the read circuits to the SDGE when an SD-read-sample pulse is received by the read circuits from the TD-OD-read-control circuit. Read-sample pulses are produced in a regular pattern. While the first 12 8-word slots of a TD field pass under the read heads, no read-sample pulses are produced; however, eight read-sample pulses are produced (one for each word) for the 13th slot. Twelve more slots are skipped, and one is read into the SDGE. During the last drum register of each revolution, an index pulse from the TD timing circuit advances the slot count. By the end of 13 drum revolutions, all slots of the selected TD field are read.

Two and one-half usec before each read-sample pulse is produced, a TD-A-word-on-way (WOW) pulse is generated to inform the SDGE that a word is about to be read. The WOW pulses go to the SDGE via the SD timing pulse switch, which transfers them along with timing and index pulses from the TD-A timing circuit.

At the start of the Third TD-A field, a start TD-6 pulse is sent to the Display System. This pulse occurs 0.54 second after the start TD-A pulse and serves to substitute for the function of the start RD pulse in the Display Pulse.

After the drum has rotated 78 times (13 times for each of the six fields), all registers of the TD-A drum have been read, and an end-TD pulse is produced in the TD-A OD-read-control circuit. This pulse stops TD-A reading and goes to the TD-A, TD-B drum cycling control. If the setting has been made at the duplex maintenance console for six fields, the end-TD pulse becomes a start-TD pulse. If the setting is for 7, 8, 9, 10, 11, or 12 fields, the end-TD pulse becomes an end-TD-A-start-TD-B pulse which goes to the TD-B drum.

The preset number of the TD-B fields is read in exactly the same sequence specified for the TD-A fields, and an end-TD-B-start-TD-A pulse is produced, whereupon the cycling control acts to start reading of the TD-A drum.

6.2.3 TD-A TD-B Drums OD Reading

Since the field sequencing circuits in each of the two track data drums are identical, general reference is made to descriptions in 3.3, 3.4, and associated subparagraphs of Part 3. In examining this information, it should be noted that RD field operation does not apply.

6.2.4 TD-A TD-B Drum Cycling Control

Figure 6–3 illustrates the logic circuits which control cycling of TD-A and TD-B drum operation. Control in this circuit is initiated by switch S16, mounted on the auxiliary drums panel of the duplex maintenance

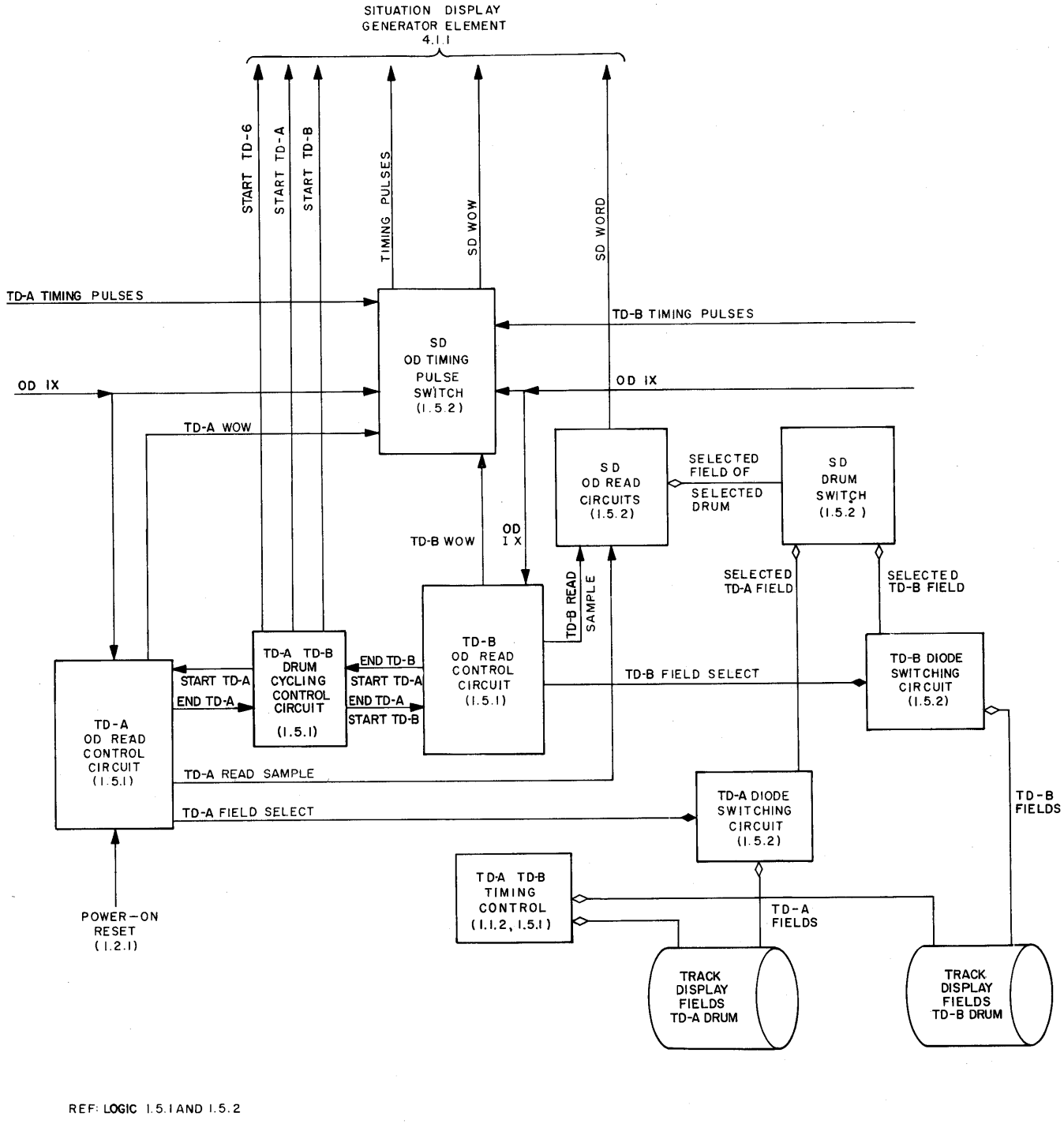


Figure 6–2. SD Reading, Block Diagram

console. Switch S16 is a key-operated, 7-pushbutton switch. To operate the push-buttons, the key has to be inserted in the lock and held twisted while the desired pushbutton is firmly depressed; only one pushbutton remains depressed at any given time.

The switch contains three sections in tandem. In section S16-1, one of the seven sets of a and c contacts closes when the corresponding pushbutton is depressed, and applies a —30V level to the pulse generator circuit. The pulse generator, in turn, produces a start-TD-A pulse through OR 1. This action causes TD cycling to start every time switch S16 is operated. The seven sets of a and b normally closed contacts in section S16-2 of the switch are wired in series to bring —48V power to

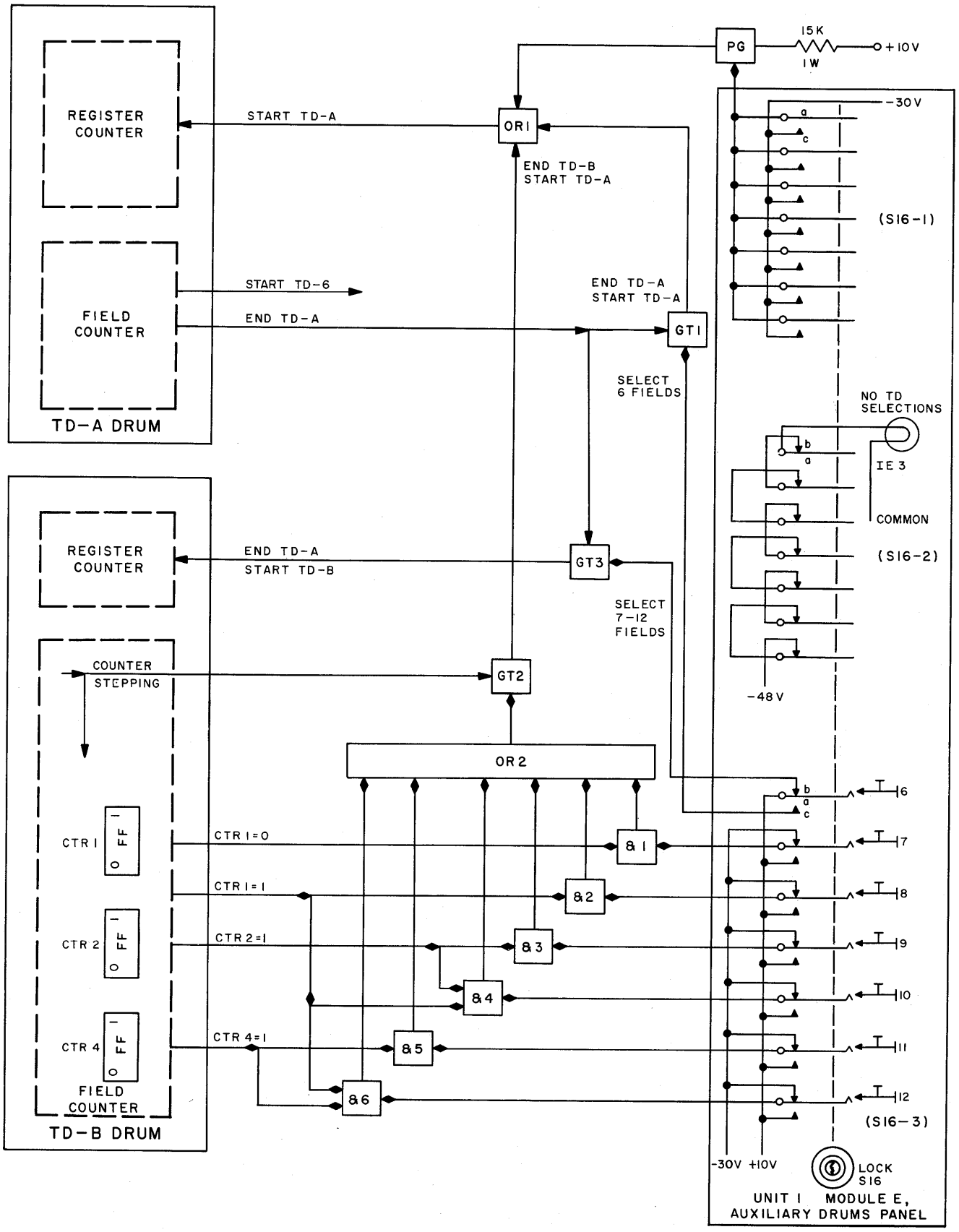


Figure 6–3. TD-A TD-B Cycling Control

the NO TD SELECTIONS lamp (IE3). Whenever the desired pushbutton is not firmly depressed, the seven sets of contacts remain closed, causing the lamp to light and the OD transfer of display data to stop.

The seven sets of a, b, and c contacts in section S16-3 of the switch serve to control the actual cycling of the TD-A drum, or the TD-A and TD-B drums, as the case may be. Depressing pushbutton 6 (meaning six TD-fields required) causes contacts a and c to close, thereby utilizing the +10V present in contact a to condition GT 1. Therefore, when the end-TD-A pulse appears, GT 1 passes the pulse through OR 1, as a start-TD-A pulse, back to the input of the TD-A drum circuits.

When any of the other pushbuttons (7 through 12) in the switch is depressed, contacts a and b of pushbutton 6 remain closed, thus applying a conditioning voltage to GT 3. Therefore, when the end-TD-A pulse appears, it is passed by GT 3, resulting in an end-TD-A-start-TD-B pulse applied to the input of the TD-B drum circuits.

The a contact in each of pushbuttons 7 through 12 is connected to AND circuits 1 through 6, respectively. In addition to the level provided by the depressed pushbutton, each AND circuit receives another level or levels from the field counter circuit in the TD-B drum. A counter-1-equals-zero condition is obtained only at the end of the first field read. Each of the conditions which are unique in the counter at the end of each field read is reflected by the levels applied to each AND circuit. However, the output of each AND circuit depends upon the levels from the field counter as well as the level from the depressed pushbutton.

Assuming that pushbutton 10 is depressed (meaning the six fields in the TD-A drum plus four fields in the TD-B drum), at the end of the fourth TD-B field reading, counter 1 equals 1 and counter 2 also equals 1. These two levels are received by AND 4 together with the level from pushbutton 10, causing an output applied to OR 2. The OR 2 circuit transfers the level to condition GT 2. When the next stepping pulse is applied to the TD-B field counter, it also appears at GT 2 and is passed by this gate as an end-TD-B-start-TD-A pulse. This pulse passes through OR 1 as a start-TD-A pulse, and the entire cycle begins with the sequential reading of the six fields in the TD-A drum.

The action previously explained for the selection of 10 fields applies in a similar manner when the selection is made for any number of the six fields available at the TD-B drum.

6.2.5 Situation Display Timing Pulse Switch

In the Drum System installed with the AN/FSQ-8 equipment, the two display drums, TD-A and TD-B,

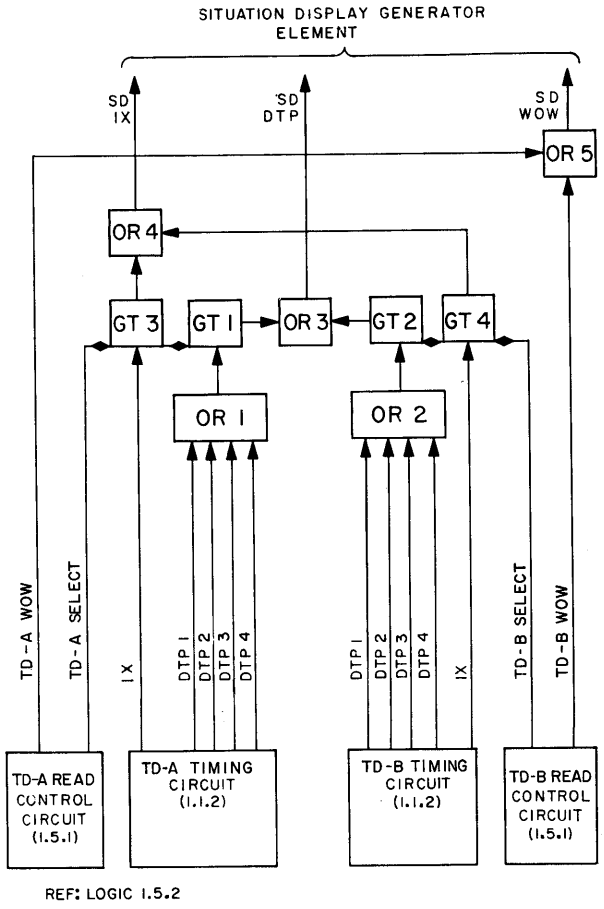


Figure 6–4. SD Timing Pulse Switch

share the SD timing pulse switch of the OD display circuits. These circuits serve to produce timing, index, and WOW pulses for the SDGE.

The AN/FSQ-8 SD timing pulse switch is shown in figure 6–4. The drum timing pulses from the TD-A timing circuit go to OR 1. The drum timing pulses from the TD-B timing circuit go to OR 2. OR's 1 and 2 conduct each time they receive one of the four drum timing pulses. The outputs of OR's 1 and 2 go to GT's 1 and 2, respectively. The TD-A or TD-B drum being read at a given time has a select level generated in its read-control circuit. This select level goes to the gate pulsed by the drum timing pulses of the selected drum. For example, if the TD-A drum is being read, the TD-A select level goes from the TD-A-read-control circuit to GT 1.

The gate conditioned by a select level passes the drum timing pulse inputs to OR 3. The OR 3 outputs are thereafter referred to as SD drum timing pulses and are sent to the SDGE.

Each select-drum level (when present) conditions a gate which is pulsed by the index pulses to the asso-

ciated timing circuit. Thus the TD-A select level is established at GT 3 during TD-A reading, and the TD-B select level at GT 4 during TD-B reading. The index pulses go to OR 4. The OR 4 outputs are referred to as SD-index pulses and go to the SDGE.

The drum being read at any given time produces a WOW pulse before sending a word into the SDGE. The TD-A or TD-B WOW pulse, whichever is present, produces conduction in OR 5. The OR 5 output is referred to as an SD-WOW pulse and goes to the SDGE.

The SD-timing-and-index pulses are used to time the operation of the generator element, and the WOW pulses prepare it to receive the words read from both drums.

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