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THEORY OF OPERATION

OF

OUTPUT SYSTEM

FOR

AN/FSQ-7
COMBAT DIRECTION CENTRAL

AND

AN/FSQ-8
COMBAT CONTROL CENTRAL

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CONTENTS

CONTENTS (cont'd)

CONTENTS (cont'd)

CONTENTS (cont'd)

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CONTENTS (cont'd)

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CONTENTS (cont'd)

CONTENTS (cont'd)

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LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (cont'd)

LIST OF ILLUSTRATIONS (cont'd)

LIST OF ILLUSTRATIONS (cont'd)

LIST OF ILLUSTRATIONS (cont'd)

LIST OF ILLUSTRATIONS (cont'd)

LIST OF ILLUSTRATIONS (cont'd)

LIST OF ILLUSTRATIONS (cont'd)

LIST OF TABLES

PART 1
INTRODUCTION

CHAPTER 1
GENERAL

1.1 FUNCTION OF OUTPUT SYSTEM IN AN/FSQ-7 COMBAT DIRECTION CENTRAL

The Output System in the AN/FSQ-7 Combat Direction Central transfers output messages from the Central to adjacent Centrals and remote sites through telephone facilities. (See fig. 1–1.) After forming an output message, the Central Computer System stores it on the output buffer (OB) fields of the LOG drum in the Drum System for eventual transfer to the Output System. The Output System accepts the output message from the OB fields and transfers the message to telephone facilities for transmission to its intended destination(s). The path followed by the output message from the Central Computer System to the telephone facilities is shown in figure 1–2. The general manner in which the Output System accepts output messages from the OB fields and transfers them to telephone facilities is discussed below. Because the Output System is logically divided into two elements, the output control element and the output storage element, as shown in figure 1–3, the following general description of the operations performed by the Output System is treated by referring to these two elements.

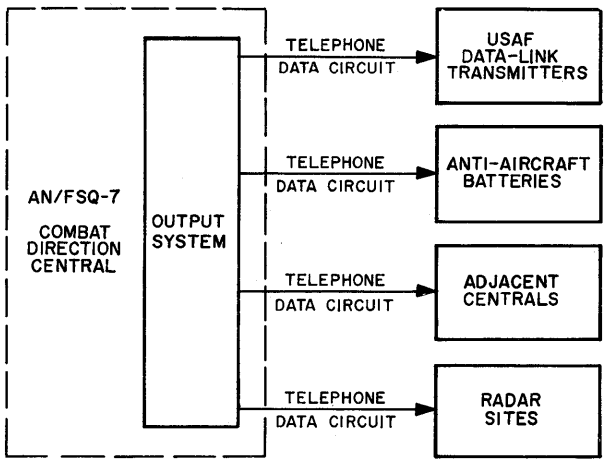

Figure 1–1. Remote Sites, Block Diagram

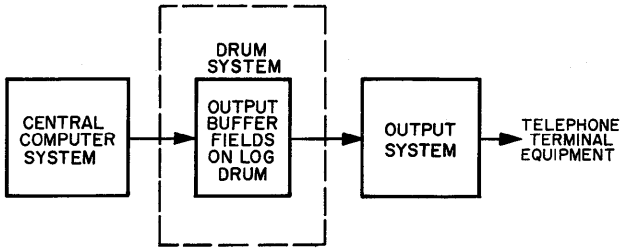

Figure 1–2. Output Message Flow, Block Diagram

1.2 FUNCTION OF OUTPUT SYSTEM IN AN/FSQ-8 COMBAT CONTROL CENTRAL

The operational function (tactical) of a Combat Control Central is exclusively concerned with monitoring and directing the operational activities of Combat Direction Centrals. A Combat Control Central has no provision for conducting ground-to-air communications with manned or unmanned interceptors; hence, certain facilities in the equipment complex (Output) of a Combat Control Central are not utilized.

The Output System facilities that are part of the equipment complex in a Combat Direction Central but are not required for use in the tactical activity of a Combat Control Central are the ground-to-air-FD, BOMARC 1, BOMARC 2, and the ground-to-air-TD storage sections. The Output System facilities utilized in a Combat Control Central are the ground-to-ground and the teletype storage sections.

Nevertheless, the function of the Output System in an AN/FSQ-8 Combat Control Central is similar to the function outlined for that of an AN/FSQ-7 Combat Direction Central, and is discussed in Part 5.

1.3 OUTPUT CONTROL ELEMENT

The output control element primarily controls the flow of output message words from the OB fields of the LOG drum to the output storage element. Another function of the output control element is to make available to the Central Computer System specific data which is used by the Air Defense program as an aid in con-

trolling the transmission time of output messages. The output control element also provides visual indications of alarm conditions that might occur in the Output System and, in addition, contains Output System test equipment which can be used both as an aid in detecting the sources of trouble within the Output System and as an aid in checking certain elements of the Input System.

1.4 OUTPUT STORAGE ELEMENT

The output storage element temporarily stores the words of an output message and then, at the completion of read-in (when the complete message is present in the output storage element), transfers the message serially to telephone terminal equipment. This element contains six storage sections; each accommodates a different class of output messages. Output messages are grouped into six classes: ground-to-air frequency division (G/A-FD), BOMARC 1 (BO1), BOMARC 2 (BO2), ground-to-air time division (G/A-TD), ground-to-ground (G/G), and teletype (TTY). The storage sections are labeled accordingly: the G/A-FD storage section, the BO1 storage section, the BO2 storage section, the G/G storage section, the G/A-TD storage section, and the TTY storage section. These storage sections receive and store output messages and then transfer them serially to the telephone terminal equipment. However, the transfer rate employed by the storage sections differs and depends upon the class of output message handled. Output messages in the G/A-FD, BO1, BO2, G/G, and G/A-TD classes are sent over telephone data channels to sites equipped with automatic input equipment. Sites not equipped with automatic input devices are supplied with teletypewriter receivers. Output messages destined for such sites are in the TTY message class and are transferred by the TTY storage section to telephone equipment at the standard TTY rate of 60 words per minute (wpm).

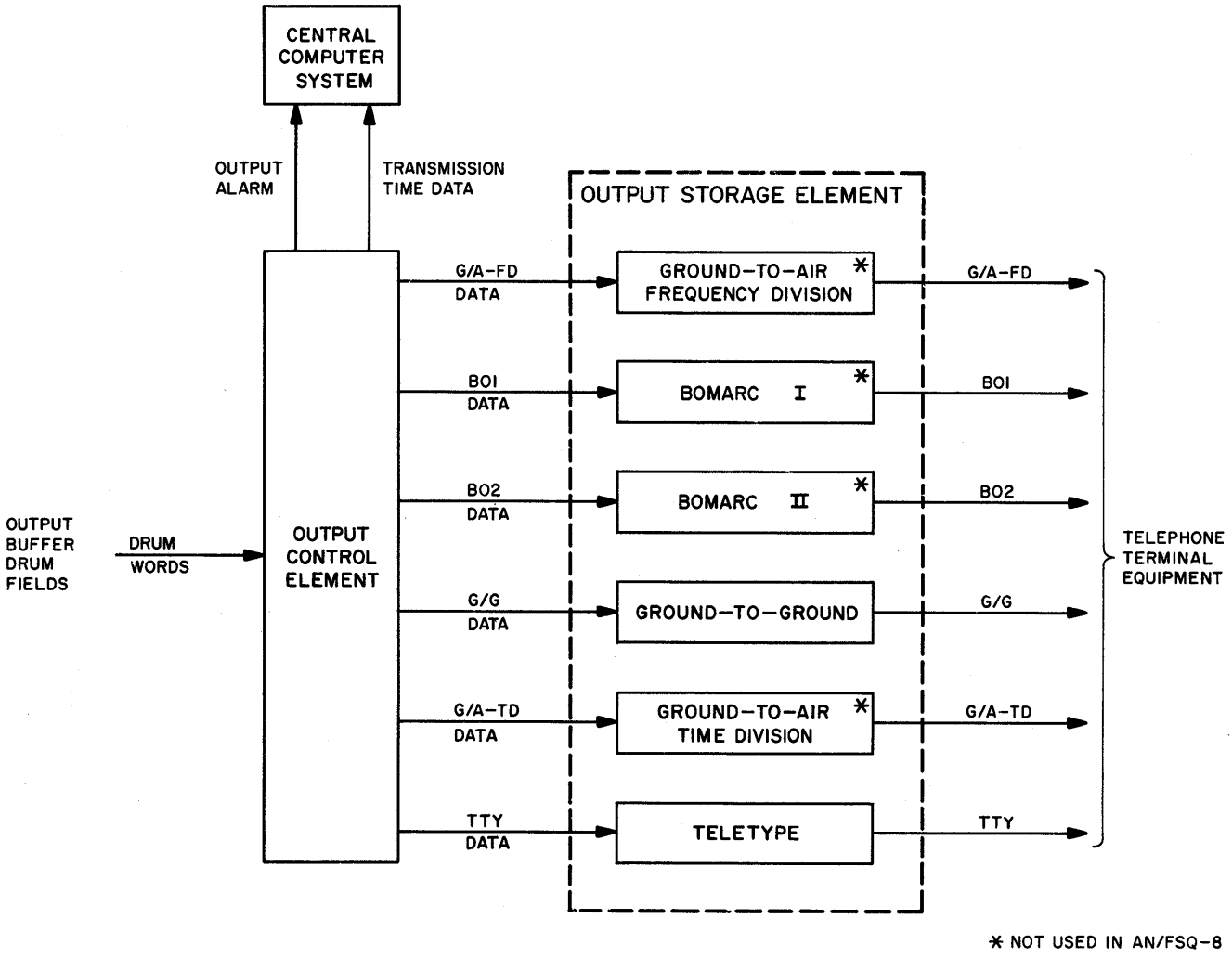

Figure 1–3. Output System, Block Diagram

CHAPTER 2
OUTPUT MESSAGES

2.1 GENERAL

An output message is a communication sent from an AN/FSQ-7 Combat Direction Central to adjacent Centrals or remote units. The Central Computer System performs various operations, controlled by the air defense program, upon air defense situation data supplied to the Central Computer System by radar sites, adjacent Centrals, and by personnel (manually) through the Input System. If the results of these operations are to be transmitted to remote units, such results are formed into output messages. As previously indicated, an output message falls into one of six classes: G/A-FD, BO1, BO2, G/G, G/A-TD, and TTY. The data used to form each message class and the purpose or purposes of each class are described below.

Ground-to-air-FD and -TD messages are composed of data which will help manned fighter aircraft intercept assigned enemy targets. The G/A-FD and -TD messages are transmitted from the Central to the remote G/A-FD and -TD data-link transmitters which provide the radio link with the aircraft. BOMARC 1 and BOMARC 2 messages are used specifically to control unmanned interceptors (missiles).

A G/G message is composed of either crosstelling (XTL) data, forwardtelling data, or a height-finder request. Ground-to-ground XTL messages are transmitted to adjacent AN/FSQ-7 Combat Direction Centrals, and G/G forwardtelling messages are sent to an AN/FSQ-8 Combat Control Central. Crosstelling information is data that aids the receiving Central in performing its assigned function. Forwardtelling data is a report on the overall situation in the area of the sending Central. The remaining type of G/G message is composed of a height-finder request which is sent to height-finding equipment at a radar site. A height-finder request message is employed whenever the altitude of a specific target is required.

Teletype messages are formed of either information intended for higher headquarters, information for nonautomatic adjacent sectors (sectors not equipped with AN/FSQ-7 Combat Direction Centrals), or early warning information intended for antiaircraft batteries. Forwardtelling information sent to higher headquarters is a summary tabulation of the up-to-the-minute air defense situation. The TTY messages sent to nonautomatic adjacent sectors contain information similar to the data in G/G messages. Teletype messages sent to the antiaircraft batteries are composed of early warning radar data.

2.2 TIMING OF OUTPUT MESSAGE TRANSMISSIONS

The time for the transmission of each output message is selected in the Central Computer System, and certain Output System circuits ensure that the message is transmitted at the selected time. The reasons for this control and the means by which it is accomplished are described in the following text.

Output messages must be transmitted in correct sequence within each of the six classes: G/A-FD, BO1, BO2, G/G, G/A-TD, and TTY. In addition, certain types of messages in each class must be transmitted at the proper times.

2.3 MESSAGE FORMATION

2.3.1 General

An output message as formed by the Central Computer System is composed of several words; the exact number of words used to form each message varies with the class of the message. G/A-FD, BO1, and BO2 messages contain a maximum of 13 words; a G/G message contains five words; a G/A-TD message, four words; and a TTY message, an indefinite number of words. Each drum word is composed of 32 bits and is divided into halves, the left half-word and the right half-word (fig. 1–4). The right half-word contains output data to be transmitted, and the left half-word is made up of address data and a burst number. After formation and

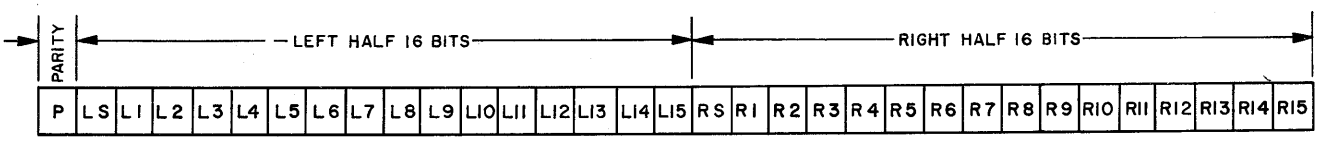

Figure 1–4. 33-Bit Word

prior to storing the word on the OB fields for eventual transfer to the Output System, a parity bit is added, increasing the total number of bits to 33.

2.3.2 Left Half-Word

The left half-word of each word contains a 3-bit section address, a 5-bit register address, and a burst number which may contain as many as eight bits (fig. 1–5). This data is used to inform the Output System of the output storage section that is to transmit the right half-word, the storage register in the selected output storage section where the right half-word is to be stored, and the burst period during which the right half-word is to be accepted from the OB fields and transmitted by the selected storage section. The combination of the section address and register address determines the group of remote sites to which the right half-word is transmitted. In order to understand how the section and register addresses are used to accomplish this, a short discussion pertaining to the logical composition of the storage device employed in the output storage sections and to the telephone facility connections is required.

The output storage sections employ ferrite core arrays as storage devices. An array is composed of 26 core registers, each of which has the capacity to store a right half-word. An array within an output storage section is logically divided into slots, each formed by the number of registers required to accommodate the right half-words of one output message. Therefore, a slot can store one output message. Since the number of words forming an output message varies according to the output message class, the number of registers forming a slot differs in each output storage section. A G/A-FD, a BO1, or a BO2 slot is composed of 13 registers; a G/G slot, of five registers; a G/A-TD slot, of four registers; and a TTY slot, of only one register. The TTY slot requires only one register because only one word of a teletype message is transmitted during a teletype burst period.

During the formation of an output message, the remote site intended to receive this message is known as a result of the Central Computer System operations performed on air defense situation data. A binary code for a storage section is selected and assigned as a section address. This section address is assigned to each left half-word of the output message. The section address is a general address because it merely specifies the output storage section that is to transmit the message. In order to complete the addressing of the output message, the words of the message must be addressed to those registers composing the slot in the selected output storage section array that supplies the telephone circuit connected to the intended destination of the message. Therefore, successive words in the output message are sequentially assigned the register addresses of the registers in the slot concerned.

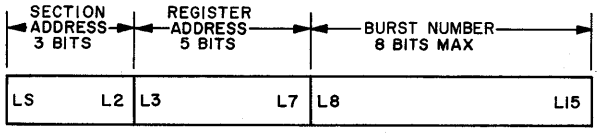

Figure 1–5. Left Half-Word

The remaining portion of a left half-word is the burst number. The burst number that is assigned to a message indicates the burst period during which the words of the message are to be accepted by the Output System from the OB fields and then transmitted. The same burst number is assigned to each left half-word of the message (or messages, if there is more than one in a burst).

2.3.3 Right Half-Word

The right half-word of each output message word is formed by the Central Computer System, using only a part of the data composing a complete output message. The remaining output message data is used to form the right halves of the other words in the message. The G/A-FD messages contain a maximum of 13 right half-words which are used by the Central to carry required data to manned airborne interceptors. A right half-word in a G/A-FD message contains interceptor address bits RS through R3, message label bits R4 through R7, and actual data bits R8 through R15. The message label of each right half-word of a G/A-FD message identifies the data contained therein.

The G/A-FD messages are transferred from the Central through telephone data circuits to G/A-FD data-link transmitter sites. A G/A-FD data-link receiver at the site receives the messages from one telephone data circuit and provides radio communication to many airborne interceptors. Each of the right half-words in a G/A-FD message is used by the G/A-FD data link transmitter to modulate one of 13 subcarrier frequencies. In this manner, separate subcarriers are modulated by a different right half-word of the G/A-FD message; that is, right half-word 1 modulates the first subcarrier, right half-word 2 modulates the next subcarrier, etc.

BOMARC messages contain a maximum of 13 right half-words which are used by the Central to carry required data to unmanned interceptors (missiles). A right half-word in a BOMARC message contains missile address bits RS through R2, message label bits R3 through R6, and command data bits R7 through R14. The BOMARC messages are handled in the manner described for G/A-FD messages.

A G/G message contains five right-half drum words (a total of 80 bits) employed by the Central to carry

either XTL information to an adjacent Central, forwardtelling data to an AN/FSQ-8 Combat Control Central, or a height-finder request to a radar site. The data used to form a G/G XTL or forwardtelling message can be varied by the air defense program in the Central Computer System. Therefore, the amount of XTL or forwardtelling data used to form each right half-word of a G/G message is not fixed.

Each right half-word of a typical XTL or forwardtelling message is formed by the Central Computer System. The last (third) type of G/G message is employed to carry height-finder requests to radar sites.

A G/A-TD message is composed of four right half-words that are separated into groups of two right half-words and transmitted over separate telephone channels to manned interceptors via data-link transmitters. Two data phone lines are used to transmit the G/A-TD message to the manned interceptor. One data phone line handles information relating to site address, aircraft address, and the message label, whereas the command data associated with the G/A-TD message is transmitted over the other data phone line. One G/A-TD message contains four commands. The G/A-TD messages are sent from the Central via data-link transmitters that are located within a given area, with each transmitter operating on the same assigned frequency. Selection of a particular data-link transmitter is established by the site address portion of the G/A-TD message. If a G/A-TD message is addressed to a particular aircraft in a group of aircraft, only that aircraft will take action on the transmitted message.

A TTY message is employed by the Central to carry information to remote sites not equipped with automatic input devices through telephone TTY circuits. Each right half-word of a TTY message contains the binary equivalent of three TTY code symbols. A TTY code symbol represents either a letter, a figure, or a TTY operation. Table 1–1 shows the TTY letter, figure, or operation associated with a 5-bit binary code symbol. As shown in table 1–1, a binary code may represent either a letter or a figure. Because of this, a code symbol representing either of the TTY operations, entitled letters or figures, must be transmitted prior to the group of letter or figure codes. The three 5-bit code symbols employed to form a right half-word of a TTY message depend upon the data to be transmitted. The 15 bits of the three 5-bit code symbols occupy bit positions R1 through R15 of a TTY right drum word. Bit RS is always a 1 (fig. 1–6). The TTY transmission procedure is described in greater detail in Part 3, Chapter 5.

TABLE 1–1. TELETYPE CODE

CHARACTERS		
LETTERS	**FIGURES**	**CODE SIGNALS**
A	–	00111
B	?	01100
C	:	10001
D	$	01101
E	3	01111
F	!	01001
G	&	10100
H	#	11010
I	8	10011
J	'	00101
K	(	00001
L	)	10110
M	.	11000
N	,	11001
O	9	11100
P	0	10010
Q	1	00010
R	4	10101
S	Bell	01011
T	5	11110
U	7	00011
V	;	10000
W	2	00110
X	/	01000
Y	6	01010
Z	"	01110
Space		11011
Carriage return		11101
Line feed		10111
Figures		00100
Letters		00000
Blank		11111

2.3.4 Parity Bit

A parity bit is added to the drum word to cause the sum of the 1's in a word to be odd if odd parity is desired and to be even if even parity is desired.

A parity check for the correctness of the drum word is accomplished by counting the number of 1 bits of the drum word which are stored in the OB register and affecting odd parity.

In the Central Computer System, after the left and right halves of a word are formed, a count is made of the 1 bits in the word. When an odd total is discovered, a 0 parity bit is assigned; however, should an even total result, a 1 parity bit is added. In both cases, the total number of 1 bits in the word plus the parity bit is odd. Therefore, the number of 1 bits in a word, together with its parity bit, when placed on the OB fields, should always be odd. The 32-bit word plus the parity bit is referred to as a 33-bit drum word. When the Output System reads a drum word from the OB fields, it performs a parity count during which the 1 bits in the drum word are added. If the result is an odd total, the drum word is assumed to contain no errors, but if an even total results, the drum word contains an error and is effectively destroyed by the Output System.

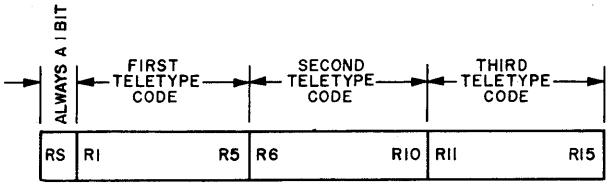

Figure 1–6. Teletype Right Half-Word

CHAPTER 3
DRUM STORAGE

3.1 GENERAL

There are three OB fields on the LOG drum in the Drum System upon which drum words are stored by the Central Computer System for eventual transfer to the Output System. These OB fields are used consecutively and therefore may be thought of as one triple-size drum field. One restriction upon this concept is the fact that a continued reading from, and writing onto, these fields is interrupted because a delay of 120 μsec is introduced when switching from one field to the next. These OB fields are divided into 6,144 drum-word registers (2,048 per field); however, only 2,036 registers per field are used to store drum words because 120 μsec are required at the beginning of each field to allow for switching fields. Thus, 12 drum registers per field have no usable information in them (dead registers); consequently, only 2,036 drum-word registers are used. The drum rotation is such that successive registers are spaced 10 μsec apart.

The drum words of an output message are written onto the OB fields at the maximum rate of 50,000 drum words per second. They remain on the OB fields until the arrival of the burst period, during which the output message is intended for transmittal by the Output System. At the start of this burst period, the drum words of the output message are accepted by the Output System from the OB fields at the maximum rate of 100,000 drum words per second, but not for the same section.

In addition to transferring drum words stored on the OB fields to the Output System, the Drum System supplies the Output System with OD LOG drum timing pulses. The Output System utilizes these timing pulses to synchronize its operations with those of the Drum System.

3.2 OB FIELDS WRITING

The drum words of an output message are written on either all odd or all even drum-word registers of the OB fields, as specified by the Central Computer System. Since there is a 10-μsec interval between successive registers, the minimum interval between the writing of successive drum words of an output message onto the OB fields is 20 μsec; i.e., writing cannot occur at a rate greater than 50,000 drum words per second. The drum words of the same output message are intended for a specific storage section of the Output System, which receives them at the same rate at which they are written onto the OB fields. The maximum rate at which information can be placed in a ferrite core array employed by an output storage section is 50,000 pulses per second (pps). Thus, limiting the writing of successive drum words onto only odd or even drum registers ensures that the rate at which the drum words of a message are transferred to a particular core array never exceeds 50,000 drum words per second.

Successive drum words of one message are not necessarily written onto these drum fields in successive odd or even registers. Instead, each drum word is written onto the first odd or even drum-word register that is made available to the drum word.

A drum-word register is considered to be available if its contents have been accepted by the Output System; it is considered unavailable when it stores a drum word that has not yet been accepted by the Output System. Thus, when a drum word is accepted by the Output System, the status of its associated drum-word register is changed to indicate an available register. In like manner, the status of a register is changed to unavailable when a drum word is written onto the register. No separate erasing procedure is performed when a drum word is accepted by the Output System because the action of writing a new drum word onto an available register effectively erases the old drum word as part of the write-in process.

Frequently, each successive drum word must wait for a register to become available; consequently, successive drum words are often placed on the OB fields several drum-word registers apart. Therefore, the interval between the writing of successive drum words of the same message may be greater than 20 μsec (but the interval is always a multiple of 20 μsec).

3.3 OB FIELDS READING

The contents of the drum-word registers on the OB fields are read consecutively and transferred to the Output System. Since there is a 10-μsec interval between drum-word registers, the drum words cannot be read at a rate greater than 100,000 drum words per second. Each drum word received by the Output System is examined and either accepted, rejected for being in error, or rejected for arriving too soon. The statuses of the registers associated with the drum words that are either accepted or rejected for being in error are changed to

"available." The drum words that are rejected for arriving too soon remain on the OB fields. These rejected drum words contain good information and will be accepted at a later time. Consequently, the statuses of the registers containing the rejected drum words remain unchanged to prevent the writing of new drum words over still useful information.

3.4 LOG DRUM OD TIMING PULSES

The LOG drum OD timing pulses are used to synchronize the transfer operations of the Drum System with the processing operations of the Output System. There are four OD timing pulses, designated OD 1, OD 2, OD 3, and OD 4. These pulses occur in sequence from OD 1 through OD 4 with a spacing of 2.5 μsec between successive pulses. Therefore, an OD cycle, which is the interval between an OD 1 pulse and a following OD 1 pulse, is 10 μsec. The OD pulses are generated continuously, with every OD 4 pulse followed 2.5 μsec later by an OD 1 pulse (fig. 1–7).

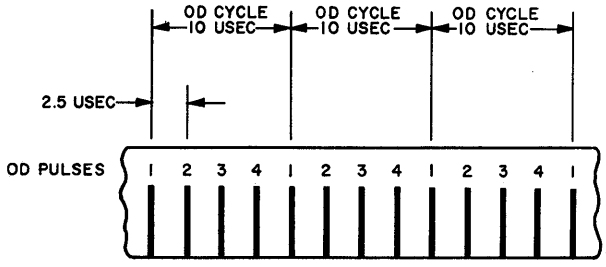

Figure 1–7. OD Cycle, Timing Chart

CHAPTER 4

OUTPUT SYSTEM, BLOCK DIAGRAM ANALYSIS

4.1 GENERAL

The Output System transmits each output message from the Central to the intended destination of the message. This transmission is done in serial form during the proper burst period and at the correct rate of transmission over either a telephone data channel or a telephone teletype channel. The Output System is composed of two elements, the output control (unit 42) and the output storage (unit 33). These elements perform the Output System functions. A separate discussion of each element follows, related to the Output System block diagram (fig. 1–8).

4.2 OUTPUT CONTROL ELEMENT, BLOCK ANALYSIS

Although the output control element has several functions, it primarily controls the flow of right half-words from the OB fields to the output storage element. Secondly, the output control element makes available to the Central Computer System the contents of the G/A-FD, G/G, G/A-TD, and TTY burst counters and the G/A-FD elapsed-time counter. Specifically, there are four burst time counters. One burst time counter is common to the G/A-FD, BO1, and BO2 sections, whereas the remaining three sections each have their own burst time counter. This information aids the Central Computer System in assigning the proper burst number to future bursts. The output control element also provides visual indications of any alarm conditions that might occur in the Output System. Furthermore, this element contains test equipment which can detect the sources of trouble within the Output System and can also be used to aid in checking certain elements of the Input System.

The output control element receives 33-bit drum words successively from the OB fields at the maximum rate of 100,000 drum words per second. As each drum word appears, the section and register addresses are decoded and a parity count is made of the bits of the drum word. The parity count is initiated by an OB-loading pulse that is received from the Drum System simul-

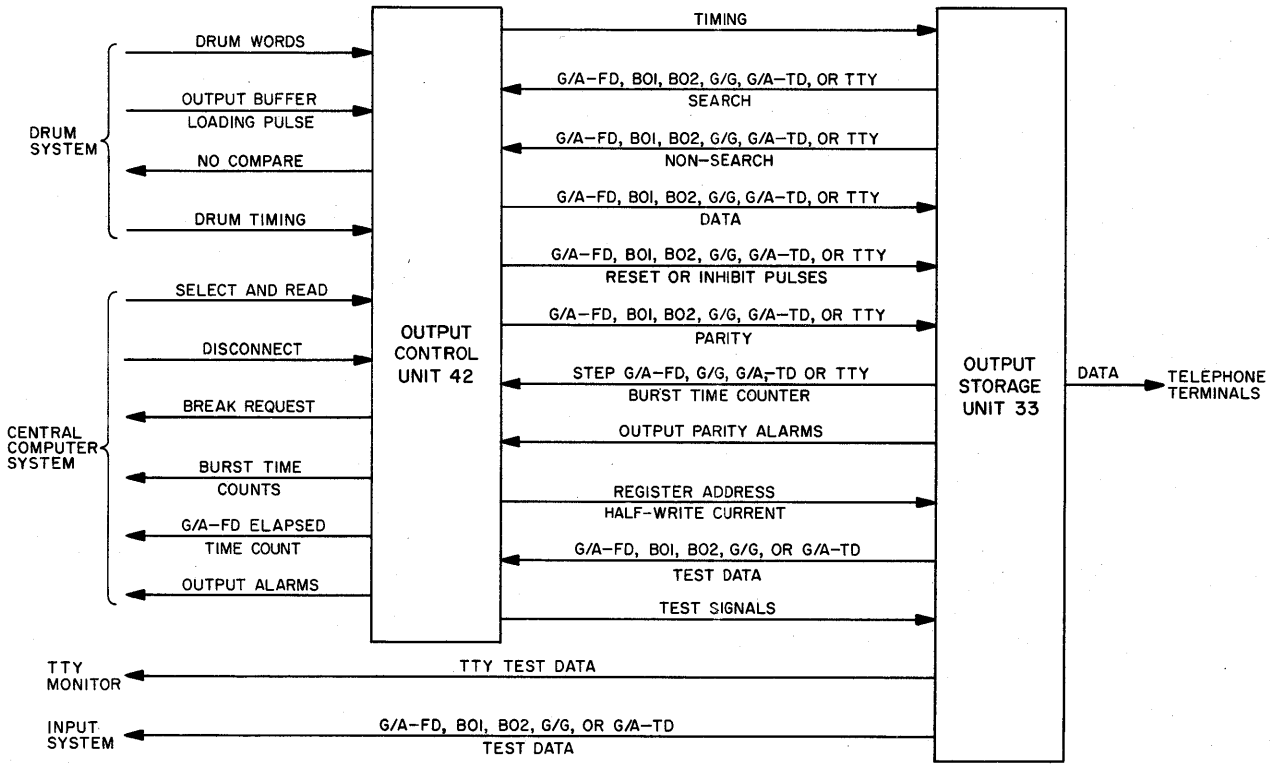

Figure 1–8. Output System (3.0), Simplified System Diagram

taneously with each drum word. Coincidental with the decoding of the section and register addresses and the parity check, the burst number is compared to the contents of the G/A-FD (BO1, BO2), G/G, G/A-TD, and TTY burst counters. Each burst counter is associated with an Output System storage section. If the burst number of the drum word is equal to the contents of any one burst counter, the output control element generates either a G/A-FD-compare, BO1-compare, BO2-compare, G/G-compare, G/A-TD-compare, or TTY-compare level. The specific level generated depends upon the burst counter whose contents match the burst number.

A compare level generated in the output control element will start the transfer of the right-half drum word from the output control element to the output storage element if the following conditions are met:

a. The correct storage section must have been selected; this is indicated by the section address (e.g., the G/A-FD storage section).
b. The compare level must be received from the burst counter associated with the selected storage section. (If the G/A-FD storage section is selected, it is required that the G/A-FD-compare level be received.)
c. The parity count result must be odd.
d. Receipt of the drum word from the OB fields must occur during search time for the selected storage section. (If the G/A-FD storage section is selected, receipt of the drum word must occur during the G/A-FD search time.)

The last condition is controlled by the output storage element which applies three levels to the output control element; each level indicates search time for a different storage section. These levels are labeled search-G/A-FD, search-BO1, search-BO2, search-G/G, search-G/A-TD, and search-TTY, respectively. If the search level is up for a particular storage section, and the other listed conditions are also met, a correct compare level causes the transfer of the 16 bits of the right-half drum word to the selected storage section as half-write message pulses. A half-word-address pulse, which results from decoding the register address, is transferred in parallel with the 16 bits of the output word when the compare level is up.

When the burst number of a drum word does not compare to the contents of any of the burst counters, it is an indication that this drum word is not to be accepted at this time. Consequently, the drum word is rejected and a no-compare pulse is generated by the output control element. The no-compare pulse is sent to the Drum System, where it causes the status of the drum-word register upon which the rejected drum word is stored to remain unchanged. If the Drum System does not receive a no-compare pulse from the output control element during the 10-μsec interval between drum words, it is an indication that the drum word is accepted, and the status of the drum-word register storing the accepted drum word is changed to indicate that the register is now available.

During the parity count of the drum word by the output control element, a parity bit is added to ensure that the right-half drum word contains an even number of 1 bits. This parity bit causes the total number of 1's in the 16-bit right-half drum word plus this parity bit to be even. This parity bit is transferred to the output storage element in parallel with the right-half drum word as a G/A-FD, BO1, BO2, G/G, or TTY parity bit, depending upon the section address in the drum word. However, in the case of the G/A-TD section, a parity bit is added to ensure that the right-half drum word contains an odd number of 1 bits. This is a prime requisite for the G/A-TD section. The G/A-TD word transfer operation is the same as that mentioned for the other sections.

The G/A-FD, BO1, BO2, G/G, and G/A-TD data, after being processed, is transferred from the output storage element to telephone terminal equipment via relays in the output storage element. These relays do not interfere with the flow of G/A-FD, BO1, BO2, G/G, and G/A-TD data to the telephone terminal equipment in a normal operation. During test operations, however, the flow of data is rerouted by these relays. If the Output System is under test (unit test), only one section at a time is rerouted. Therefore, test data, after being processed by the output storage element, is matched to original test data that was manually loaded into the output control element. In this manner, the accuracy of the data, after passing through the Output System, is checked. If a computer test is being made to check the flow of information, the route of the output data received from the output storage element is changed by the output test equipment. In this case, the output data is sent from the output storage element of the Input System. At the termination of the computer test, the test data is examined by the Central Computer System for errors.

The four burst counters (G/A-FD, G/G, G/A-TD, and TTY) and the elapsed time counter are contained in the output control element; their contents are always present there. Upon receipt of a select-and-read pulse from the Central Computer System, a burst-time-count and elapsed-time-count transfer operation (burst-count read cycle) is initiated, during which the contents of the burst counters are sequentially transferred to the Central Computer System with a 10-μsec interval between burst time counts. The elapsed time count which is associated only with the G/A-FD, BO1, and BO2 storage sections is transferred in parallel with the G/A-FD

burst time count. Simultaneous with the transfer of each burst time count, a break-request pulse is sent to the Central Computer System, initiating the input-output (IO) break during which the burst time count enters the Central Computer System. When the Central Computer System has read any or all of the burst time counters as desired, it generates a disconnect pulse that is sent to the output control element. This pulse terminates the burst-time-count and the elapsed-time-count transfer operation.

If an alarm condition is detected during the processing of output data by the output storage element, an alarm pulse is generated by the pertinent storage section and sent to the output control element as either a G/A-FD, BO1, BO2, G/G, G/A-TD, or TTY alarm pulse. In the output control element, if an error is discovered in the drum word that is being examined, or if one of the six alarm pulses from the output storage element is received, an Output System alarm level is produced. This alarm level is sent to the maintenance console of the Central Computer System, causing the illumination of a visual alarm.

The output control element contains the complete test equipment for the Output System. This test equipment allows the Output System to be tested separately from the Central Computer during a unit loop test function. Various test operations are visually indicated on neons and lamps of the alarm portion of the Output System.

The output control element receives LOG-OD timing pulses from the Drum System; these are employed to synchronize the operations of the Drum and Output Systems. These OD timing pulses are distributed by the output control element to the various sections of the Output System. The output control element also generates and sends to the output storage element the timing pulses that are used in transferring the output data from the output storage element to the transmission equipment.

4.3 OUTPUT STORAGE ELEMENT, BLOCK ANALYSIS

The purpose of each of the storage sections in the output storage element is to receive, temporarily store, and transfer messages in the proper form and at a rate compatible with the transmission facilities.

The burst number of each drum word read from the OB fields is received in the output control element and is compared to the contents of the four burst counters. If the burst number matches the contents of a burst counter, that burst counter produces a G/A-FD-compare, BO1-compare, BO2-compare, G/G-compare, or TTY-compare level which is sent to the output control element.

The contents of the burst counters and the elapsed time counter in the output control element are labeled G/A-FD burst time count, G/G burst time count, G/A-TD burst time count, TTY burst time count, and elapsed time count, respectively. In this manner, the contents of these counters are always present in the output control element and made available to the Central Computer System through a programmed IO select-and-read pulse.

Each storage section in the output storage element has its own timing circuits which enable it to record the start and end-of-search time for each burst period. Each storage section sends a search level to the output control element. When this level is up, it indicates search time for the pertinent storage section. These levels are labeled search-G/A-FD, search-BO1, search-BO2, search-G/G, search-G/A-TD, and search TTY.

During search time of each burst period, a storage section can receive the right-half drum words of the burst that is to be transmitted during the remaining portion of the burst period (referred to as the readout interval). The drum words of a particular burst are stored by the Central Computer System on the OB fields at a maximum rate of 50,000 words per second. Because of this, an output storage section receives drum words during search time at the maximum rate of 50,000 words per second. This rate corresponds to the switching rate of the ferrite cores that are employed in the core array storage devices.

The 16 bits of each right-half drum word accepted by the Output System are sent from the output control element to the correct storage section in the output storage element as specified by the section address in the left-half drum word, as half-write-message pulses. In addition, a half-write-address pulse that is indicative of the register address is also received by the pertinent storage section in parallel with the half-write-message pulses. This half-write-address pulse causes the half-write-message pulses to be written into the correct register of the core array in the selected storage section.

A parity bit is also received in parallel with the half-write-address pulses and the half-write-message pulses and is written into the selected register together with the half-write-message pulses of the right-half drum word. The contents of a register are labeled as an output word. When this word is transferred from the output storage element, the parity bit provides a means of checking it for accuracy. At the completion of search time for a storage section, the burst stored in the core array of the storage section is transferred from the storage section to transmission facilities.

Because of the type of transmission equipment employed, the form of each message in a burst must be modified before it can be transmitted. The G/A-FD, BO1, BO2, G/G, and G/A-TD messages are modified by

their respective conversion circuits and then transmitted to their destinations over telephone data channels in serial form. The TTY messages are also transmitted in serial form. However, the TTY storage section simulates several TTY transmitters and sends a TTY message at the rate of 60 words per minute to a telephone TTY channel. For these reasons, the forms of the output messages are modified to a serial form and transferred to the proper transmission facilities at the proper rate. The TTY messages, likewise, are transferred over telephone data channels to their destinations.

A parity check is performed when a message is transferred from a storage section. If a parity error is detected, an alarm pulse is generated by the storage section. This alarm pulse is sent as a G/A-FD-alarm, BO1-alarm, BO2-alarm, G/G-alarm, G/A-TD alarm, or TTY alarm pulse to the output control element. This element produces an output-alarm level that is sent to the maintenance console, causing the illumination of a neon alarm indicator.

When the output control element is used to test equipment, there is an interchange of numerous pulses and levels between the test equipment and the output storage element during either a computer or unit test. Drum timing pulses which are used to synchronize the operations of the output storage element with the operations of the Drum System are received by the output storage element from the output control element. In addition, the timing pulses required to transfer the output messages from the output storage element at the proper rates are also received by the output storage element from the output control element.

CHAPTER 5
HEART OF STORAGE SYSTEM

5.1 FERRITE CORE ARRAY

The ferrite core array is a coincident-current storage device, similar in some respects to the core memory of the Central Computer System. This array consists of 572 ferrite cores arranged to form 22 columns and 26 rows. As shown in figure 1–9, the two axes are termed the message axis and the address axis, and each row is known as an address register.

The ferrite core is a device with square loop hysteresis characteristics, capable of two saturated states. These two states represent binary digits 0 and 1. Read-in of information switches one or more cores in the array from the 0 state to the 1 state and allows other cores to remain in the 0 state. Readout of information sequentially senses the state of all cores in the array and switches the cores previously set to the 1 state back to the 0 state.

During read-in of information, a particular core in the array is set to the 1 state upon receipt of two half-write currents: one from the address axis and one from

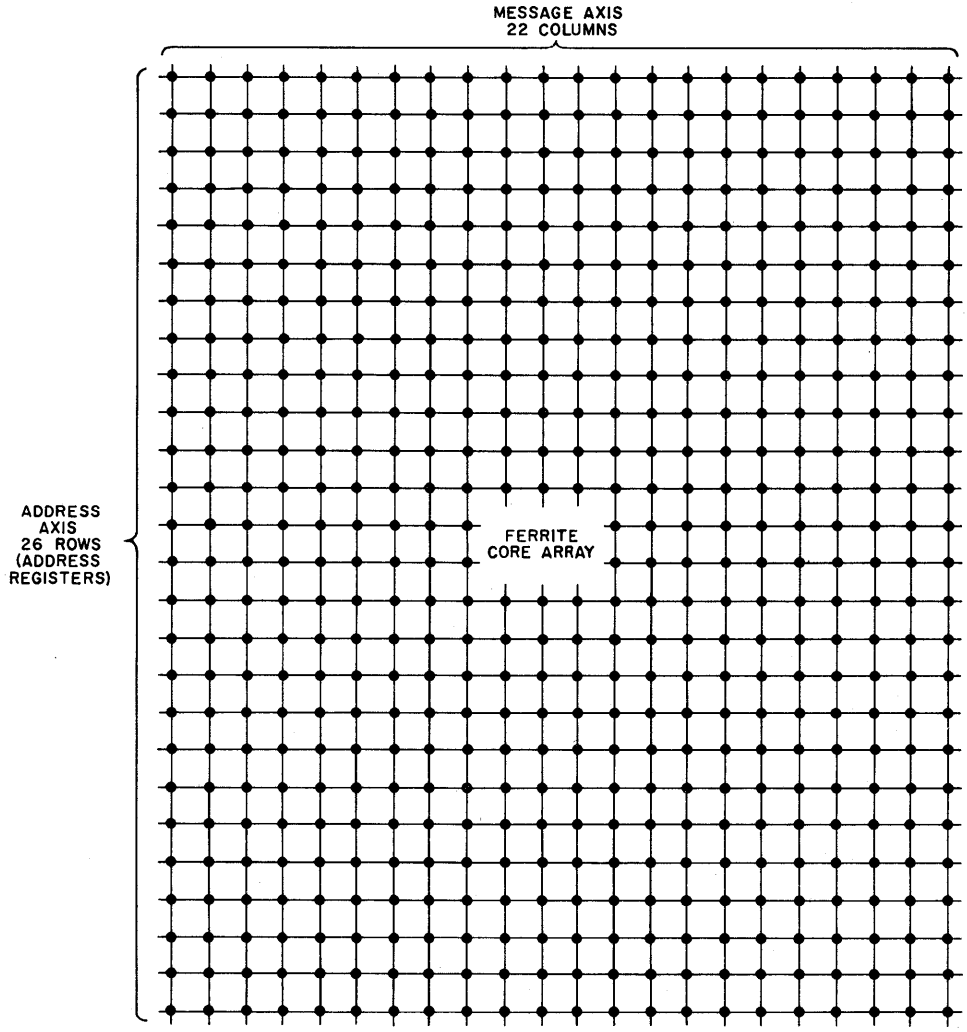

Figure 1–9. Ferrite Core Array

the message axis. Each column and each row is provided with a 2-turn read-in winding which carries the half-write current. Figure 1–10 shows a simplified version of an array and the method by which a particular core is selected for read-in of information. The coincidence of two half-write currents applied to a particular core results in the full-write current necessary to switch the core from the saturated 0 state to the saturated 1 state.

Readout of information from an array necessitates two windings for each column and each row in addition to the read-in windings previously mentioned. (See fig. 1–11.) These windings are termed the readout winding and the sense winding. Readout differs from read-in in that it is not produced by two coincident currents; instead, a single readout current flows through the 2-turn readout winding of all ferrite cores of a column. Sequentially, one column after another is read out in this manner. This process is illustrated in figure 1–12. When the readout current pulse is applied to a given column, all cores in that column that were previously switched to a 1 state are switched back to the 0 state. The sense winding is a single-turn winding which connects all the cores in a given row. The effect of pulsing the readout winding is to induce a voltage in the sense winding. The induced voltage is of either of two configurations, depending upon whether the core was already in a 0 state or whether the core switched from the 1 state to the 0 state.

In accomplishing the read-in and readout processes in accordance with requirements imposed on the Output Storage System, various special circuits are employed. These circuits are explained in detail in Chapter 2 of Part 2. The paragraphs which follow explain the overall relationships of these circuits with each other and with the ferrite core array.

5.2 ARRAY READ-IN

The ferrite cores of each column and each row of an array receive half-write current from a tape core device known as a core current driver (CCD). (See fig. 1–13.) The CCD is switched from either of two satu-

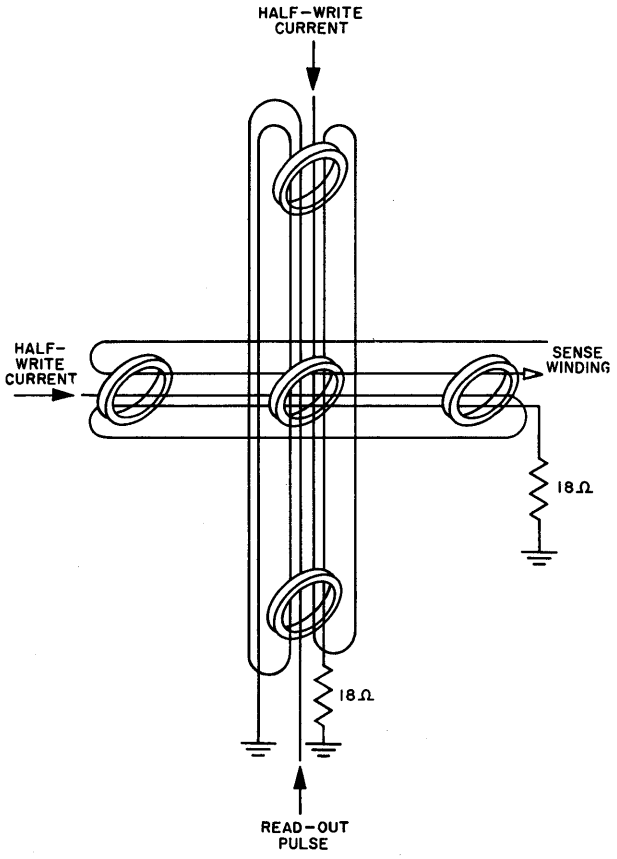

Figure 1–11. Core Windings, Simplified Diagram

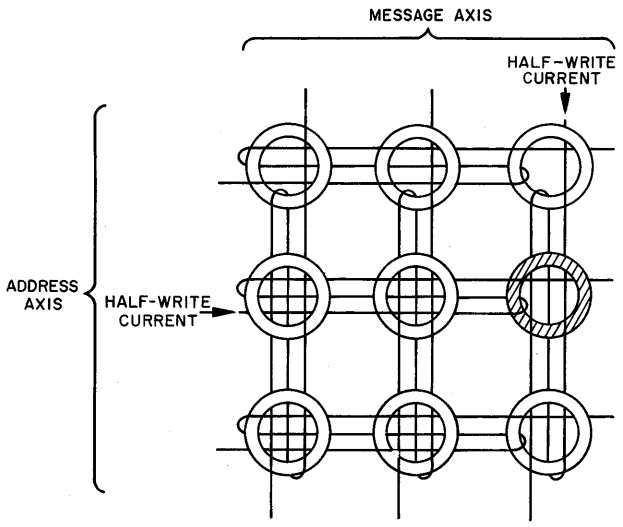

Figure 1–10. Core Current Coincidence for Read-in, Simplified Diagram

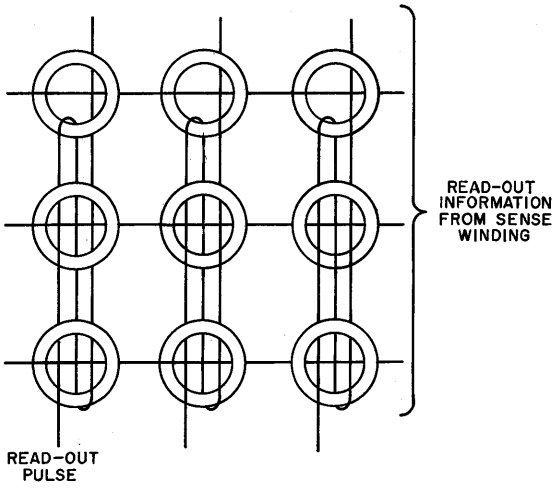

Figure 1–12. Readout by Columns, Simplified Diagram

rated states, 0 and 1. A core is said to be set when it is switched to the 1 state and reset when it is switched to the 0 state. A separate CCD is coupled to each row and each column of the array. When a CCD is switched from the 0 to the 1 state, the associated ferrite cores remain unaffected. However, when the CCD is switched from the 1 state back to the 0 state, a half-write current is transferred to all the ferrite cores in the associated row or column.

The CCD is set to the 1 state by a circuit known as the set driver (STD). Particular STD's are selected along the address and message axes. Pulsing the selected STD's sets the associated CCD's to the 1 state. The CCD's must now be reset in order to transfer half-write currents into the array.

Associated with each ferrite core array are three identical circuits called reset-inhibit drivers (RID). Each RID is used to reset 16 CCD's, the three RID's simultaneously switching all 48 CCD's. When the RID's are pulsed, all previously set CCD's are reset to the 0 state, causing the read-in of half-write currents into the ferrite cores.

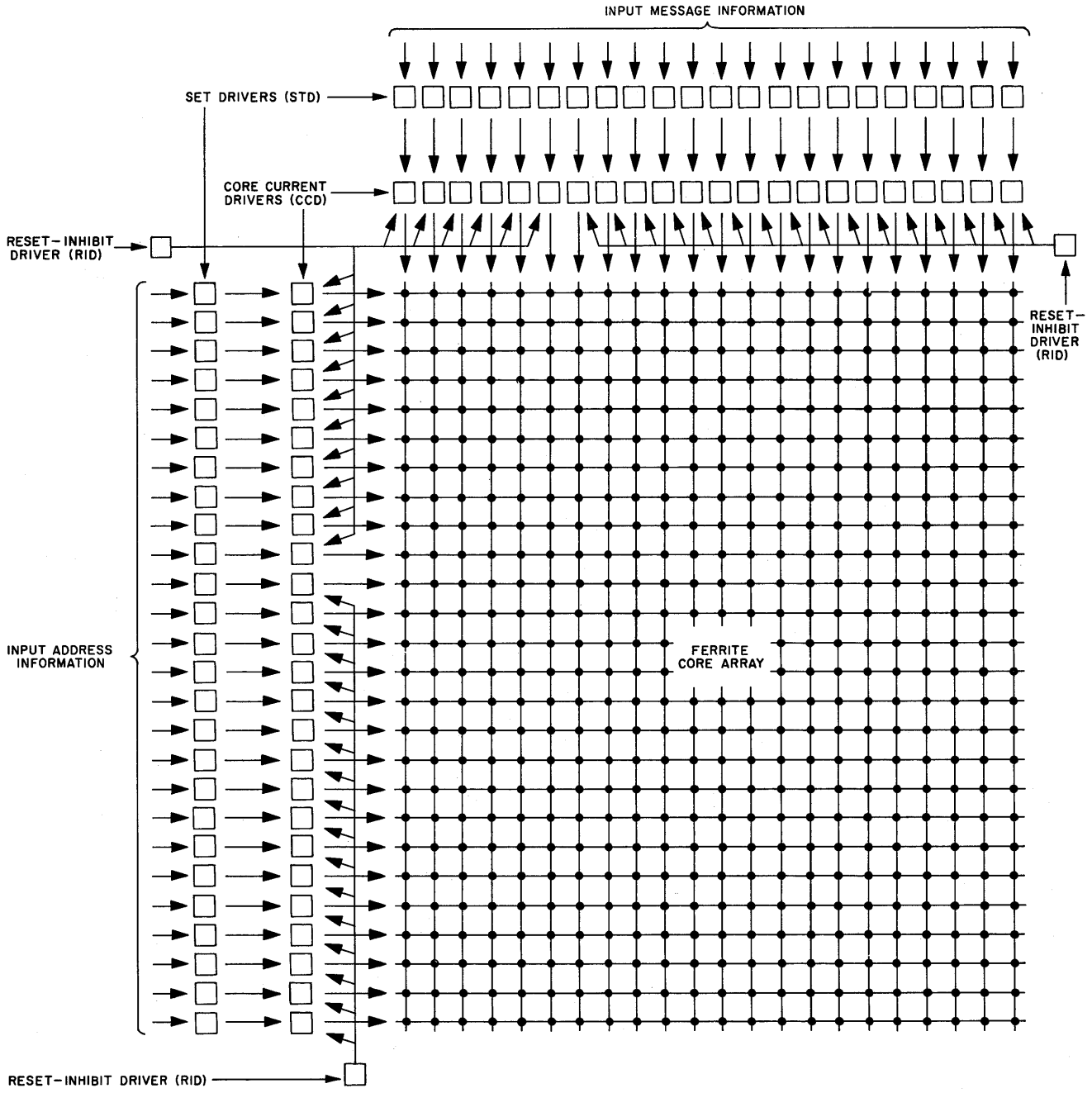

Figure 1–13. Ferrite Core Array with Associated Special Circuit used for Read-In, Block Diagram

The RID's also perform another function. Information is simultaneously transmitted to all arrays used in the Output System. However, information at a given time is intended for storage in only one array. To prevent entry of information into certain arrays, the RID's associated with these arrays are pulsed in such a way as to reset all associated CCD's. This inhibiting pulse, delivered at the same time the STD's are pulsed, cancels the effect of the set pulse delivered to the CCD's. For that array intended for storing information, the RID does not inhibit the effect of the STD on the CCD.

To summarize the read-in operation: the RID's are used to select the array intended for storing information by inhibiting the setting of CCD's in all other arrays. The selected STD's are pulsed, setting their associated CCD's along the address and message axes of the

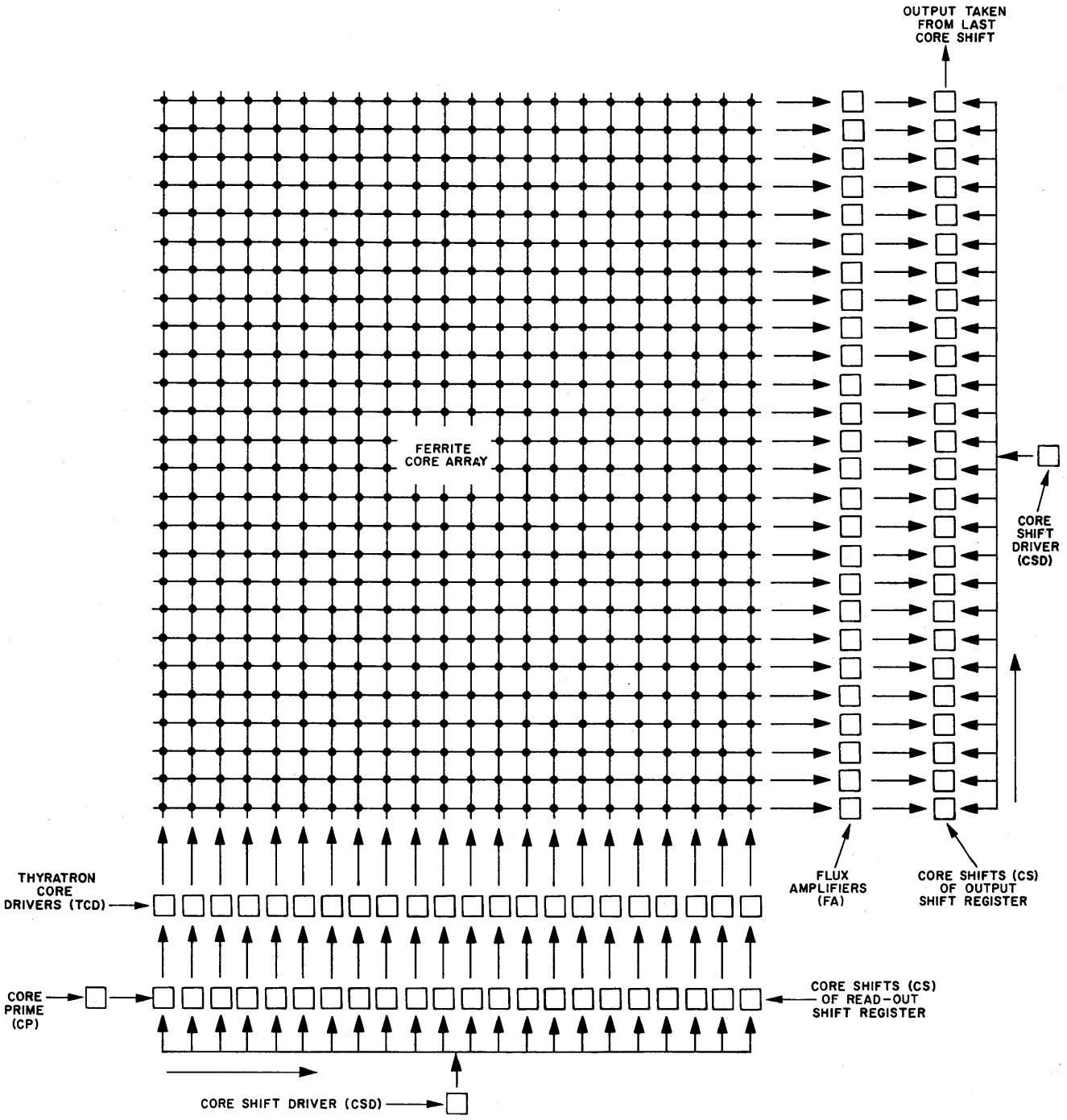

Figure 1–14. Ferrite Core Array with Associated Special Circuits used for Readout, Block Diagram

selected array. Then the RID delivers a reset pulse to the CCD, resetting previously set 1's to 0's. Resetting of the CCD's results in half-write currents being transferred to the associated ferrite cores in the row or column. Upon receipt of two coincident half-write currents, a ferrite core is switched from the 0 state to the 1 state. At the completion of the read-in operation, each selected address register of the array contains word information.

5.3 ARRAY READOUT

The current necessary to read out the ferrite cores in the array is produced by a thyratron core driver (TCD), a circuit which delivers a current output only when triggered. (See fig. 1–14.) One such driving circuit is associated with each column of the array. Upon receipt of a pulse from a given TCD, all ferrite cores in the corresponding column which were previously switched to the 1 state are switched back to the 0 state.

Triggering of the TCD's is controlled by core shift (CS) units, each unit controlling a separate driver. Each CS contains a tape core which may be saturated in either of two states. This group of CS's is known as the readout shift register.

In order to trigger the TCD's sequentially, one at a time, the CS's of the register must be sequentially switched, one at a time. This process is as follows: The core prime (CP), a driver circuit, pulses the first CS of the register, switching this core from the 0 to the 1 state. Then, all CS's are pulsed simultaneously by the core shift driver (CSD). This latter pulse switches the first core back to 0. The switching causes two things: It switches the second CS from 0 to 1, and it triggers the corresponding TCD which reads out the associated column (switches the ferrite cores to 0). The CSD is then pulsed again, which switches the second CS back to 0 and the third CS to 1. Switching of the second CS to 0 fires the second TCD, which reads out the second column. This action continues until all columns have been read out. Thus, it might be said that readout information is serially entered into the readout shift register and that message information is taken from the column by parallel readout.

As each column of the array is pulsed, a voltage is induced into the sense winding of each row. Each sense winding drives a flux amplifier (FA). The FA either rejects the sense winding signal if the corresponding ferrite core contained a 0 or accepts it if the core contained a 1. Each FA drives a separate CS of the output shift register (OSR). Ferrite cores that contained 1's cause associated CS's to be switched to the 1 state; ferrite cores that contained 0's allow associated CS's to remain in the 0 state. Since the information contained in all the ferrite cores of a column is entered simultaneously into the OSR, the register is said to receive this information by parallel entry.

Once the information contained in a column is transferred to the OSR, the CSD associated with the register is then pulsed repeatedly. With each pulse, information contained in each CS is transferred to its succeeding CS. Output from the register is taken from the last CS. The CSD is pulsed until all information is serially read out of the register.

To summarize the readout operation: the first CS in the readout register is switched to the 1 state by a core prime. This is necessary to initiate the serial switching which takes place in the register. As the CSD pulses the readout shift register, the first CS is reset to 0, the second CS is set to 1, and the first TCD is triggered to reset all ferrite cores in the first column to 0. Information contained in the first column is transferred through the flux amplifiers to the OSR. The associated CSD is pulsed repeatedly until all information is serially read out of the register, output information being taken from the last CS in the register.

After the first column has been read out, the CSD associated with the readout shift register is pulsed again. This initiates readout of the second column. This action continues until all columns in the array have been read out. Thus, the word information contained in each row of the array is serially read out column by column. The array is now ready for read-in again.

PART 2
OUTPUT CONTROL ELEMENT

CHAPTER 1
INTRODUCTION

1.1 GENERAL

The primary purpose of the output control element is to control the flow of intelligence from the output buffer (OB) fields of the drum to the output storage element and then to the transmission facilities. In addition, the output control element, upon request, sends burst count information (essential for the computer program) to the Central Computer System and performs specific tests on the Output System. The tests include both system and programmed computer tests. The output control element also provides visual indications of any Output System alarm conditions.

Several terms, used frequently in the output control element, are explained as follows:

a. Drum Word. This is a 33-bit word entered into the output control element from the OB drum fields of the Drum System. It contains the intelligence destined for transmission, the data which identifies the storage location, and the transmission sequence of the word.

b. Output Word. This is the intelligence portion of the drum word (right half) and is the portion sent to the output storage element from the output control element.

c. Burst. A burst is the group of words consisting of the messages which are simultaneously transferred from a storage section to the associated telephone lines during the complete emptying of the storage section.

d. Burst Period. The burst period is the interval between the entrance of successive bursts into the Output System. The burst period consists of search time and readout time. Search time (read-in time) is the time required to read the burst from the OB drum field into one of the output storage sections. Readout (nonsearch) time is the time required to empty the burst out of the output storage section and into the telephone lines, plus any pauses or delays. The bursts are counted in each output storage section so that information is always available as to which burst period is in progress.

e. Burst Number. The burst number is part of the 33-bit drum word and designates the particular burst period during which the word is to be entered into the output storage section.

f. Elapsed Time. The elapsed time is the time that has elapsed since the start of a burst period.

1.2 ELEMENT DIAGRAM ANALYSIS

The output control element is divided into four major sections as shown in figure 2–1. They are the output buffer, output computer, output alarm, and output test equipment sections.

The OB drum section receives a drum word from the LOG drum OB fields in parallel form, tests the parity of the word, examines its addresses and burst number, and checks the validity of the word. On the basis of the word addresses, this section determines to which storage section and core array register within this storage section the right-half drum word (intelligence portion of the word) should be sent. It also generates an output parity bit for the right-half drum word. If the right-half drum word is valid, it is sent to the selected section and register in the output storage element.

The output computer section transfers the burst counts of the G/A-FD, G/G, G/A-TD, and TTY burst counters to the Central Computer System at the latter's request. The elapsed time count is sent with each G/A-FD burst count. Upon receipt of a select-and-read pulse, the output computer section releases this information to the Central Computer System. The Central Computer System utilizes the information to assign the proper burst numbers to future output messages. In addition to this function, the output computer section generates some, and distributes all, timing pulses used for controlling operations in the Output System.

The output alarm section stores information regarding the status of several alarms and displays the status of these alarms by neon indicators. It also dis-

IBM FIELD ENGINEERING BULLETIN

Project: SAGE Number: 0308

Class: Maintenance

Equip: Outputs

Type: Information

Date: August 12, 1964 Page 1 of 4

LOCATIONS AFFECTED:

25th AD ___	26th AD ___	26th AD PROVISIONAL ___	28th AD ___	29th AD RCC ___	30th AD ___	PCI ___
BAADS X	BOADS X	CHADS X	DEADS X	DUADS X	GRADS X	LAADS X	MOADS X
NYADS X	PHADS X	POADS X	READS X	SCADS X	SEADS X	WAADS X	OTTAWA X

SUBJECT: E. C. R-74325 G/A T/D Modification

INFO: IBM TRA'S: Dept. s 276, 274, 272, 266, 281, 282, 280, 284

The installation of E. C. R-74325 accomplishes a major change in the operation of the Outputs G/A T/D section. The result is an extensive change in the logic layout particularly logic 3. 2. 5. Until the maintenance personnel have had the opportunity to review and troubleshoot with the new logic layout, the retrofit changes may be somewhat difficult to understand. The intent of this letter is to provide sufficient detailed information regarding the changes to facilitate an easier understanding of the new logic flow in the G/A T/D section.

The following discussion is divided into two parts for ease of explanation. The first part outlines the signal changes made to achieve the specified signals required on the output phone lines. Part II outlines the specific function of the new circuitry added to achieve the output signal requirements.

Part I

Signal Specifications and Requirements for E. C. R-74325

A second mode of operation is being added to the outputs G/A T/D section. This will be known as the single channel mode. The purpose of this is to route all T/D output signals to the channel No. 1 output phone lines. This means that the time for operation of the T/D section, per each burst time count, must be increased by 100 per cent to allow serial transfer of all the array words out on channel No. 1 lines. The slowed down operation is being accomplished by changing the 15 counter to an 18 counter and by disabling the fast shift on logic 3. 2. 5.

Originator: N. H. Prothe

Dept: Field Technical Support - 255

INTERNATIONAL BUSINESS MACHINES CORPORATION
FEDERAL SYSTEMS DIVISION KINGSTON, NEW YORK

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plays the drum word bits and certain test operations on neon indicators and indicator lamps. These indicators are located on the maintenance consoles and output unit test panels.

The output test section, which is an integral part of the output control element, is used to perform programmed computer and unit tests within the Combat Direction Central.

Two types of loop tests are provided for the Output System: the unit loop test and the computer loop test. Each test involves the feedback of test information to its origin for the purpose of checking whether this information was correctly transmitted. The Output System test equipment effects the modification of information paths to form the test information path required for the test undertaken; i.e., unit test or computer test.

A description of the logical operations performed by the four sections comprising the output control element is included in the following text. The block schematic diagrams used have been simplified by the exclusion of nonlogical circuits such as cathode followers and amplifiers. For the complete circuitry of a logical circuit, refer to the Engineering Data Book. The logical reference number of each of these drawings has been included in the caption of each of the corresponding simplified diagrams in this manual.

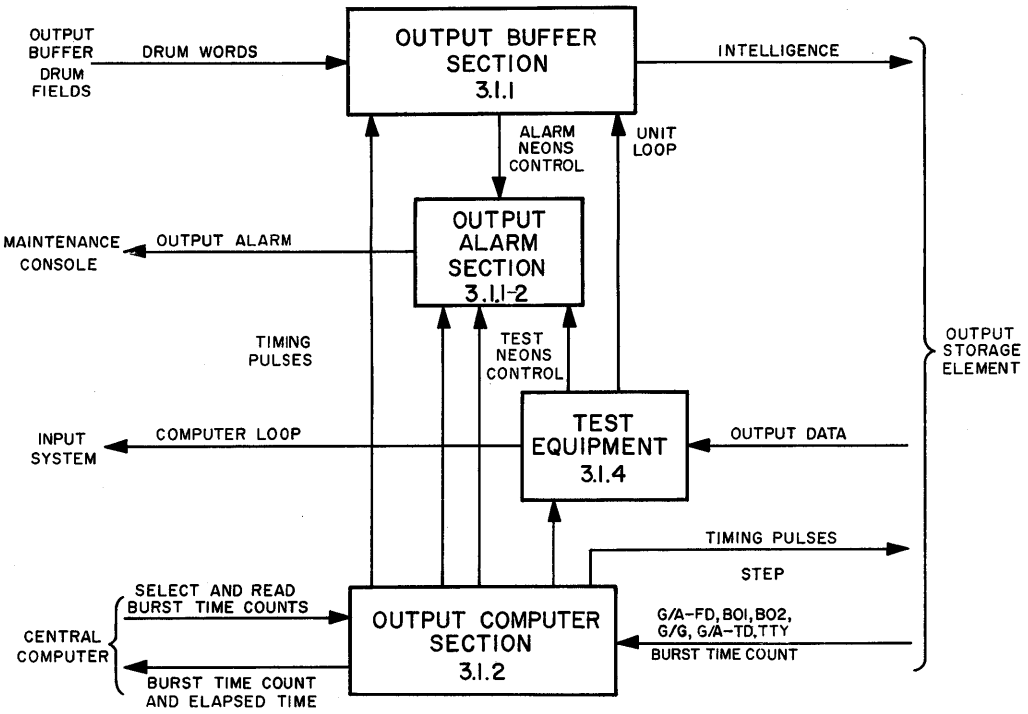


Figure 2–1. Output Control Element, Block Diagram

CHAPTER 2
OUTPUT BUFFER SECTION

2.1 FUNCTIONS AND ANALYSIS OF OUTPUT DRUM SECTION

2.1.1 Operations Performed

The output drum section of the output control element performs the following basic related operations:

a. Enters the complete drum word from the OB fields of the LOG drum into the OB register flip-flops.
b. Checks the parity of the drum word in the OB register flip-flops.
c. Decodes the output section and register address in the output word.
d. Checks the legality (correctness) of the output section and register addresses.
e. Generates a parity bit for the output word if needed.
f. Controls the read-in of the output word into the proper section and register address in the output storage element.

These basic operations are discussed in relation to the overall action performed by the output drum section in processing and accepting or rejecting the word.

2.1.2 Entrance of Drum Word

A drum word is received from the OB field of the LOG drum via a relay in the output test equipment section. Registers containing drum words are normally read at a 10-μsec rate. However, since words are written on alternate registers, odd or even, by the computer, they are accepted at the rate of multiples of 20 μsec. The purpose of the relay is to permit insertion of the test word in place of the drum word during test periods.

Drum timing pulses, called OD pulses, are employed in the Output System to regulate the processing of information from the LOG drum.

2.1.3 OD Timing Pulses

The OD timing pulses are four standard 0.1-μsec pulses generated in the Drum System; these pulses are designated OD 1 to OD 4. There is a 2.5-μsec interval between OD pulses; therefore, the complete OD cycle takes 10 μsec. Since the complete OD cycle is recycled without interruption, there is a 10-μsec interval between successive OD 1 pulses, successive OD 2 pulses, etc. Each word is read out of the LOG drum at time OD 1. If the drum speed varies, the interval between the OD timing pulses varies proportionately.

2.1.4 Flip-Flop Registers

The drum word entry into the Output System takes place at the five flip-flop registers in the OB section (fig. 2–2). The five registers correspond to the information represented by the groups of binary digits which make up the drum word. These registers have a total of 33 flip-flops corresponding to 33 binary digits (bits). The 16 bits which make up the right portion of the drum word contain the intelligence of the drum word as shown in figure 2–3. The 16 bits which make up the left portion of the drum word contain the section, register addresses, and burst number of the right drum word. A parity bit is added to the word in the Central Computer in order to complete the word. The bit is chosen so that the complete word always has an odd parity.

The section address and the register address portions of the left drum word are in the form of binary coded words which designate, respectively, the section of the output storage element (G/A-FD, BO1, BO2, G/G, G/A-TD, or TTY section) and the register address (0 to 31) of the section within which the output word is to be stored.

The burst number portion of the left-half drum word is a group of digits which make up a number that identifies the burst period (2.1.6.2) during which the associated right-half drum word is to be inserted in the output storage section. In other words, the burst number identifies the time and sequence for the insertion of the right-half drum word into the output storage section. The burst number is assigned by the program in order to obtain the desired sequence of output information. All the words which make up the message to be sent out during a particular burst have the same burst number. All the words which make up one burst are entered during the search-time portion of the burst period and cannot be entered during the readout time. If a word shows up with a burst number which indicates that it is assigned to a burst period that has ended search time and is in the readout process, the word has arrived too late to be entered into the Output System. It is a missed word. This indicates an error in programming, and the word will be rejected by the Output Sys-

tem and effectively erased from the LOG drum. An alarm is also produced to indicate this condition.

2.1.5 Checking Drum Word for Acceptance

2.1.5.1 Acceptance Requirements

In order for the right-half drum word to be read out of the output control element into the output storage element, the complete drum word must meet all of the following requirements:

a. Correct parity

b. Correct section and register addresses

c. Correct timing

d. Favorable comparison between the burst number and the contents of the burst counter.

If a drum word has either incorrect parity, an illegal section address or register address, or incorrect timing, it is not accepted by the Output System and is erased from the OB field. If all conditions for acceptance are correct except the burst number, the word is rejected temporarily by the Output System. This word is preserved for use at a later time because its correct parity and correct address have caused the generation of a no-compare pulse. If the burst number does not compare with the contents of the burst counter, and the particular burst period in progress is in the readout operation (nonsearch time), a no-compare pulse is still generated, even though the timing is apparently wrong. This is so because, although readout is taking place, the lack of comparison indicates that the word is not as-

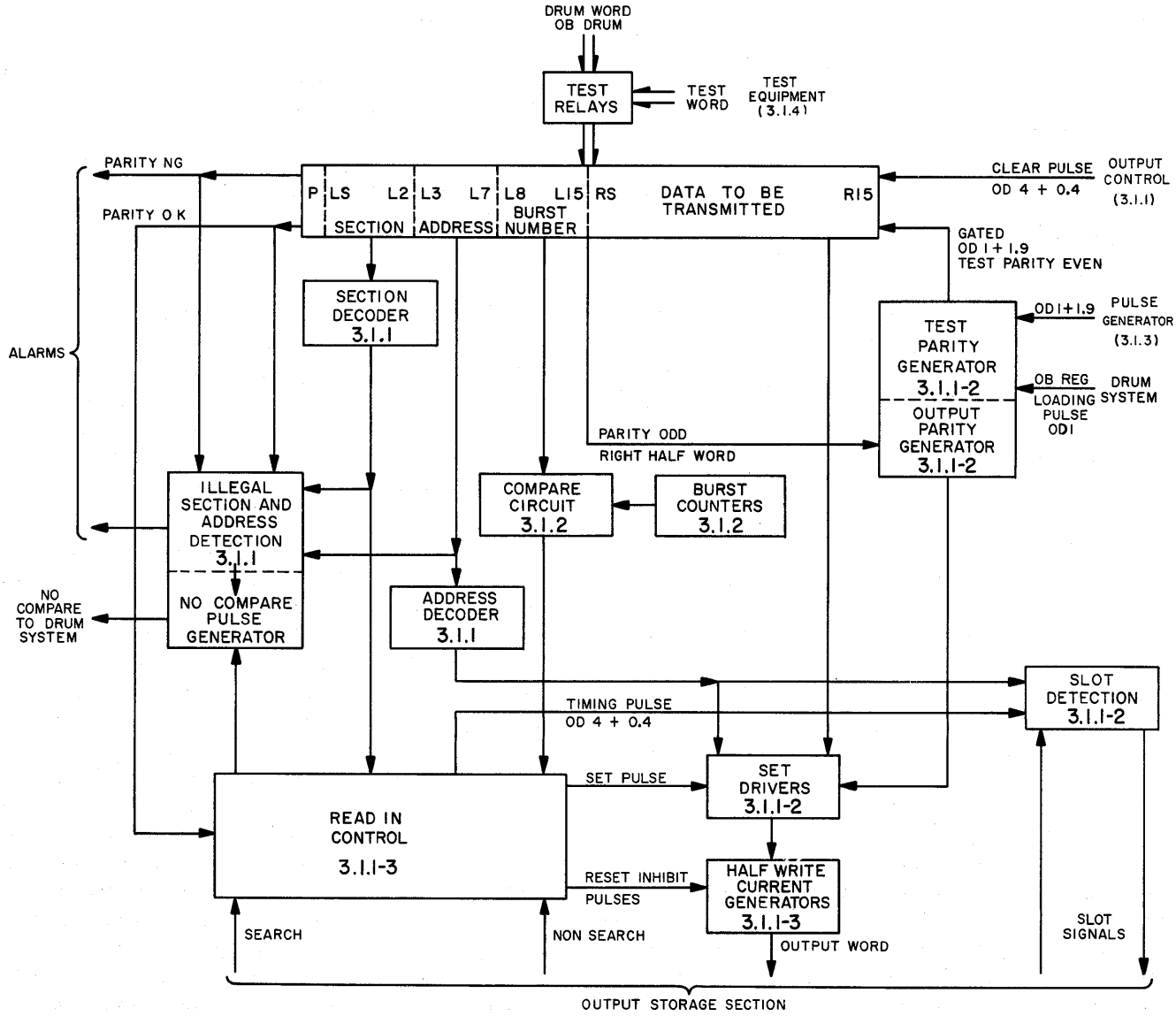


Figure 2–2. Output Buffer Section (3.1.1), Block Diagram

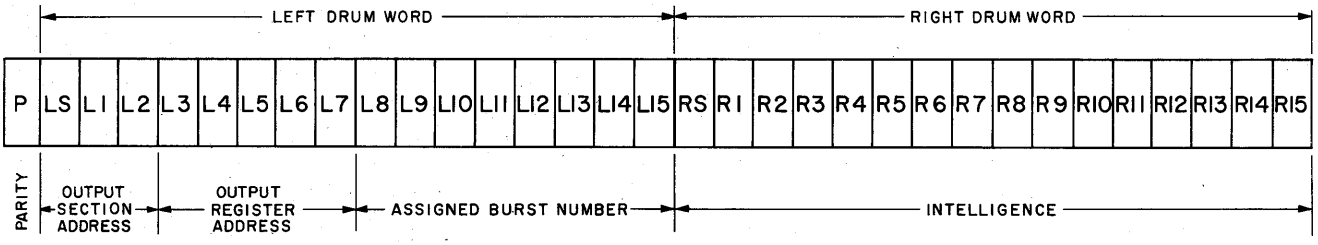


Figure 2–3. Drum Word Structure

signed to this particular burst period. Therefore, the word has not been missed and is still good. It should therefore be stored until a later time, so a no-compare pulse is generated. On the other hand, if the burst number compares with the contents of the burst counter, and readout is taking place (incorrect timing), there has been a programming error, as previously described. The word cannot be entered into the Output System and must be erased from the OB field of the drum. A no-compare pulse is not generated.

When all four of the conditions listed above are satisfactorily met, the output word (right-half word) is transferred to the storage section and register indicated by the respective addresses.

2.1.5.2 Acceptance Checks Made in Output Drum Section

A summary of the conditions for acceptance or rejection of a drum word by the Output System is found in table 2–1.

The output drum section performs the checks to determine whether the parity is correct and whether the section and register addresses are legal. The burst number comparison is made in the output control element. The timing check is made in the output storage element. The results of all four checks are passed to the read-in control (fig. 2–2) of the output drum section. This circuit then examines the results of the checks and proceeds to accomplish one of the following functions:

a. Operates the set drivers (STD's) to read the right-half drum word into the output storage section if all checks are correct.
b. Generates a no-compare pulse and rejects the drum word if only the burst number fails to check.
c. Rejects the drum word and does not generate a no-compare pulse if the parity or either of the addresses is not correct.

2.1.6 Sequence of Operations in Output Drum Section

2.1.6.1 Parity Bit

The drum word includes a parity bit, which is entered into the 33rd flip-flop register (parity register)

TABLE 2–1. CONDITIONS FOR ACCEPTANCE OR REJECTION OF A DRUM WORD

PARITY	SECTION ADDRESS	REGISTER ADDRESS	BTC	IN SEARCH	WORD DISPOSITION	BITS PUT IN STATUS CHANNEL
OK	OK	OK	OK	Yes	Accepted	0
OK	OK	OK	OK	No	Lost	0
Bad	OK	OK	OK	Yes	Lost	0
Bad	OK	OK	OK	No	Lost	0
OK	Illegal	OK	OK	Yes	Lost	0
OK	Illegal	OK	OK	No	Lost	0
OK	OK	Illegal	OK	Yes	Lost	0
OK	OK	Illegal	OK	No	Lost	0
OK	OK	OK	Bad	Yes	Saved	1
OK	OK	OK	Bad	No	Saved	1

(fig. 2–2). The parity bit is entered into the drum word in the Central Computer as either a 0 or a 1 so that each drum word always has an odd number of 1's. When the drum word enters the flip-flop register, a parity check is made to see if there is still an odd number of 1's. If such is the case, a parity-OK pulse is produced at the parity gates associated with the parity register. A parity-OK pulse is passed to the read-in control section. Without this pulse, the right drum word is not read into the output storage section. If there is an even number of 1's in the drum word, a parity-NG pulse is produced. A parity-NG pulse is passed to the output alarm section to produce an alarm.

2.1.6.2 Burst Number

As the parity of the complete word is being checked, the digits in the burst number flip-flop register (fig. 2–2) are compared with the number in the burst counter. If the burst number compares with the contents of the burst counter, a compare signal is generated in the output control element and sent to the read-in control circuit of this element. The output storage section sends a search signal to the read-in control if the search-time portion of the burst period is in progress. The read-in control reads the right drum word into the output storage element only if both the search and compare levels are present.

2.1.6.3 Section and Register Address Decoding

The section address portion and the register address portion of the left-half drum word are both in coded form. Therefore, to determine the designated addresses, decoding operations are performed. The section decoder (fig. 2–2) examines the coded section address and obtains a select-section signal on the one of eight transmission lines which is designated to correspond to the specified section address. The address decoder examines the coded register address and obtains a select-register signal on the one of 32 transmission lines which is designated to correspond to the particular register address within the specified section. The register address lines go to the STD's, and the select section lines go to the read-in control section. If the addresses and other conditions are correct, the right-half drum word is then read into the specified addresses in the output storage element.

2.1.6.4 Illegal Address Detection

The section and register address information is also passed to the illegal section and register address detection circuits (fig. 2–2). Only 6 of the 8 section addresses and only 26 of the 32 register addresses for the G/A-FD, BO1, and BO2, 25 of the 32 register addresses for the G/G and TTY, and 12 of the 32 register addresses for the G/A-TD storage sections have been assigned; therefore, address words which call for an unassigned address are illegal (in error). The illegal address detection circuits determine whether the section or register address of a drum word is illegal. If either or both are illegal, a pulse is sent to the output alarm section. If both addresses are legal, a -30V level is sent to the no-compare pulse generator by the read-in control. In order that a no-compare pulse may be generated, parity must be OK and the burst number should not compare. If either of the addresses is illegal, the signal levels in the correct select section and select register lines will be missing. The read-in control will detect this and reject the associated right drum word. Since a no-compare pulse is not generated in this case, the incorrect word is not passed to the output storage element and is erased from the OB drum registers.

2.1.6.5 Slot Detection

As each right-half drum word is placed in a register of a storage section of the output storage element, the slot detection circuit counts the entrance of this word. Since, within a storage section, a slot is a group of registers which make up one message and therefore feed one telephone channel, it is necessary to know how many registers in a particular slot are filled with words. The slot detection circuit produces a $+10$V level as each G/G or G/A-TD word is read into a particular storage array. Conversely, a slot pulse is produced as each G/A-FD, BO1, and BO2 is read into a particular storage array.

G/G or G/A-TD message slots require that a certain number of words be present in a G/G or G/A-TD slot before the message contained in a particular slot can be transmitted on the phone line. In the case of G/G, five words constitute a complete message slot; for G/A-TD, four words constitute a complete message slot. If the prescribed number of words for a particular message slot is not met, that message slot is considered incomplete and is not transmitted to the telephone lines. The slot detection circuit generates a slot level that is counted each time a G/G or G/A-TD word is read into a particular message slot. In this way, the status of each G/G or G/A-TD message slot can be determined and therefore used to control the transmission of G/G or G/A-TD messages.

G/A-FD, BO1, and BO2 message slots do not require a specific number of words to constitute a complete message. However, the number of words contained in a particular slot must be known if the parity checking circuit is to function properly. Hence, the slot detection circuit generates slot pulses each time a G/A-FD, BO1, or BO2 word is read into a message slot of a particular section.

The TTY storage section does not require slot detection because the data which is contained in one regis-

ter is considered to be a complete message. Also, the output parity checking circuit is not dependent upon the number of words contained in the array. Thus, the TTY storage array may be considered as consisting of 25 slots.

2.1.6.6 Output Parity Bit

The output drum word does not remain intact after being processed by the output control element because only the right-half drum word (intelligence) is transmitted further. Therefore, a new parity bit must be generated in order to make a parity check at the receiving terminals of the telephone lines. The output parity bit is generated in the parity generator and delay circuits (fig. 2–2) and is either a 0 or 1 in order to obtain an even number of 1's in the output word. Parity checking of the G/A-FD, BO1, BO2, G/G, and TTY right-half drum word requires that an even number of 1 bits be present for a valid word, whereas the G/A-TD right-half drum word requires that an odd number of 1 bits be present. The parity bit is added to the right drum word at the STD's.

2.1.7 Read-In Operation

The portions of the output drum section which read in the right-half drum word and the output parity bit to the output storage section consist of the STD's and the half-write current generators which are conditioned by the read-in control (fig. 2–2). The read-in control may be considered to be a gate which permits the passage of only an acceptable right-half drum word to the output storage element.

At the beginning of the read-in operations, the read-in control circuit is supplied with the following data, as previously described, which is necessary to determine whether the drum word is to be accepted and transferred to the storage array:

a. Result of parity check
b. Selected storage section
c. Result of the comparison between the drum word burst number and the contents of the burst counters.
d. Presence of search or nonsearch time in each output storage section.

The selected register address and the right-half drum word are passed directly to the STD's which are controlled by the read-in control circuit.

If the selected storage section corresponds to one of the six assigned sections, and the contents of the burst counter for this section match the burst number of the word, the right half of the drum word is intended to be entered into the designated storage section during the search time of the current burst period. It follows, of course, that the word can be entered into a register of this storage section only if the register address of the word corresponds to an assigned register. This is taken care of directly at the STD's.

A storage section can receive data only during the first part of the burst period (search time). It transmits data during the remaining portion of the burst period (readout time). It cannot receive data during readout. The read-in control circuit is informed of the portion of the burst period in progress in each storage section. A nonsearch signal indicates that readout is taking place, whereas a search signal indicates that search is in progress. Correct timing of a drum word, then, means that the drum word is entered during a search period.

If, at the beginning of a read-in operation, search time is in progress in the selected storage section, if the burst number is equal to the contents of the selected storage section burst counter, and if no parity or address errors are detected, the drum word is acceptable. The read-in control circuit then causes the STD's to transfer the right-half drum word to the selected register in the selected storage section. However, if all the preceding conditions are met, except that readout is in progress rather than search (incorrect timing), then the drum word is missing from the burst being transmitted. Since the word has arrived too late, its entry into the storage section would interfere with the readout process. Hence, it is not entered into the output storage section. This is referred to as a nonsearch alarm condition. If this condition exists, an alarm is sent to the output alarm section. Also, since the word has been missed (too late), it has no further use and is erased from the OB fields.

If all the preceding conditions are met except comparison of the burst number, the drum word is assumed to have shown up too early and is not acceptable. However, since the information in the word is still needed and is assumed to be correct, the word must not be erased from the OB fields, but merely stored until it is ready to be used. If this is the case, the read-in control circuit causes the no-compare pulse generator located in the illegal address detection circuit to generate a no-compare pulse (fig. 2–2). Thus, although the read-in control rejects the drum word, it is not erased from the OB drum fields.

2.1.8 Summary

If an error is detected in a drum word (illegal address, illegal section, or even parity), or a nonsearch condition exists although the burst number compares, the read-in control circuit rejects the word, and a no-compare pulse is not generated. Hence, the word is not sent to a storage section and is erased from the OB fields.

If the drum word and timing are correct, the read-in control circuit produces the signals required to trans-

fer the right-half drum word from the STD's to the half-write current generator. In coincidence with this, the circuits associated with the particular register address that is selected produce the additional half current needed to put the data bits in the core array. Thus, the message is stored in a storage array, as determined by the section decoder, and in a register address, as determined by the address decoder.

2.2 DRUM WORD ENTRY

2.2.1 Flip-Flop Register

Each drum word is temporarily stored in a flip-flop register which is divided into the right-half drum word, burst number, register address, section address, and parity registers. The drum word consists of 33 binary digits grouped as shown in figure 2–3. The right drum word, consisting of bits RS to R15, inclusive, represents the intelligence intended for transmission as the output word. The left drum word (bits LS to L15, inclusive) consists of the output section address, the output register address, and the burst number. The addresses denote the output storage section and register to which a right-half drum word is assigned; the burst number determines the time and sequence of transmission of the associated right-half drum word. The remaining drum word bit is a parity bit.

2.2.1.1 Right-Half Drum Word Register

The right-half drum word register consists of 16 flip-flops, as shown in figure 2–4. A right-half drum word is applied to the register flip-flops in the form of parallel standard pulses from the OB fields. A 1 bit is represented by the presence of a pulse and a 0 bit by the absence of a pulse. The right-half drum word register is cleared prior to the receipt of each drum word; thus, when a right half-word is applied, it is reproduced at the flip-flop outputs as d-c levels. The flip-flops are cleared approximately 7.9 μsec after receipt of a right-half drum word in preparation for the next word. The time interval between the registering and the clearing of the drum word is chosen to be approximately 7.9 μsec because approximately 10 μsec are required for each drum register of the OB field to pass the drum read head. Hence, since a new drum word may be passed from the OB field to the Output System flip-flop register every 10 μsec (time OD 1), the flip-flop register must be cleared after a time interval of slightly less than 10 μsec.

During the time that the right-half drum word is in its register, its bits are applied to the STD's of the read-in circuit, the parity gates, and the output test equipment section (fig. 2–2). The STD's initiate preparations for the transfer of a word into one of the storage sections, should it be accepted. For a discussion of the STD's, refer to 2.6.4. The parity gates, which are in the same location as the right-half word register, permit a sampling of the right-half drum word when checking the parity of the complete drum word. The gates utilize both the 0 and 1 flip-flop outputs. The STD's require only the 1 outputs to perform their functions.

2.2.1.2 Burst Number Register

The burst number register temporarily stores bits L8 to L15 of the drum word. The assigned burst number can have a maximum of eight binary digits and, therefore, 256 possible variations. The number of possible variations (different possible burst numbers) must be large enough to ensure that all bursts within a program frame can be assigned a different burst number.

The burst number register, shown in figure 2–5, contains eight flip-flops designated L8 to L15. Bits L8 to L15 are inserted in the register at the same time that the other bits of the drum word are placed in their respective registers. As in the case of the right-half drum word register, the burst number flip-flops are cleared approximately 7.9 μsec later. During this interval, both the 1 and 0 outputs are made available to the parity gates, which are in the same location as the burst number register, and to the burst counter compare circuits. This permits the parity check and burst number comparison operations to be conducted. The burst number comparison operation consists of comparing the burst number of the drum word with the contents of the

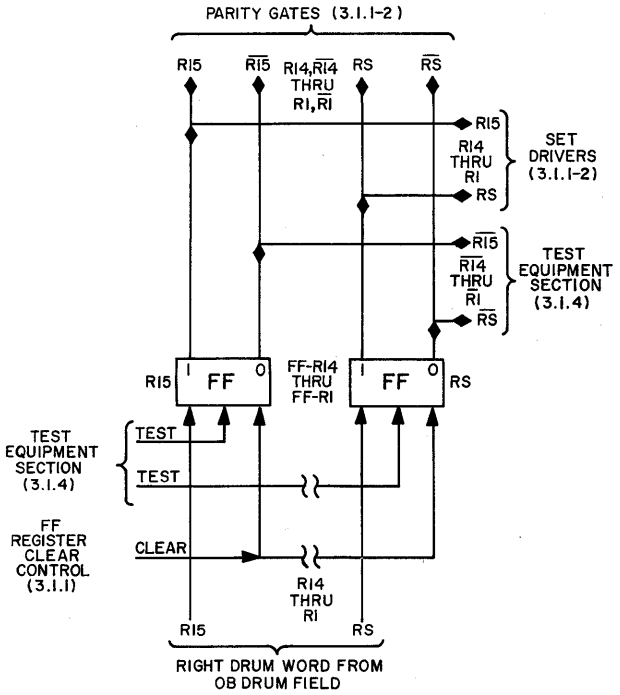


Figure 2–4. Right Drum Word Register (3.1.1-2), Simplified Logic Diagram

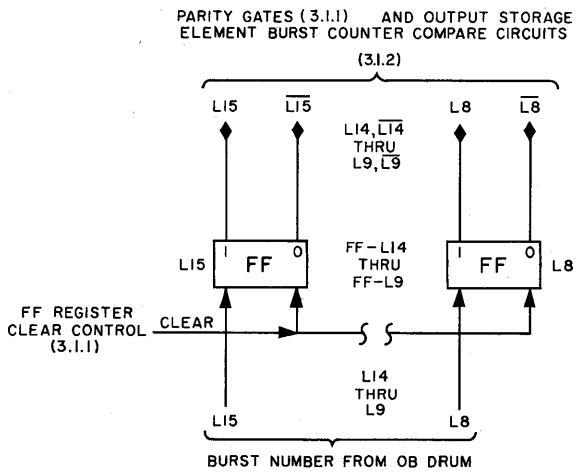


Figure 2–5. Burst Number Register (3.1.1), Simplified Logic Diagram

burst time counter in the output control element. Therefore, the contents of the counter indicate the burst number of the drum word which should be stored next. If the drum word which has been entered does not have the right burst number, but if all other information in the word is found to be correct, the word is rejected from the Output System but is not erased from the OB field of the drum. It is therefore available to be reentered at the correct time. A no-compare pulse is generated (2.6.3) to accomplish this operation.

2.2.1.3 Section Address Register

Binary digits LS to L2 of the drum word constitute a binary coded message that designates the section address. This address denotes the specific output storage section in which the associated right-half drum word is to be stored. At present, there are only six output storage sections (G/A-FD, BO1, BO2, G/G, G/A-TD, and TTY). Since three binary digits can make up eight possible combinations, there are eight possible addresses. It follows that since only six addresses are assigned, an error exists if one of the other two addresses is called for by the coded message. The illegal section address detection circuit (2.5.2) determines whether the section address is in error.

A simplified logic diagram of the section address register is shown in figure 2–6. The outputs of these three flip-flops are routed to the parity gates, which are in the same location as the register, and also to the section address decoder. The latter decodes the information contained in bits LS through L2 to produce a signal level on one of the six section address lines. This action produces control which directs the right-half drum word to the assigned storage section. The illegal section detection circuit produces an illegal-section-address pulse if the decoded section address indicates one of the two unassigned section addresses. This pulse is used in the alarm circuit. Also, an illegal-section level is generated which is used in the no-compare pulse generator circuit (2.6.3) to cause a drum word which has an illegal section address, and is therefore rejected from the Output System, to be erased from the drum.

As in the case of the other flip-flop registers, the clear pulse is applied to the section address register approximately 7.9 μsec after entrance of the bits. This clears the register.

2.2.1.4 Register Address Register

Binary digits (bits) L3 to L7 of the drum word constitute a binary coded message which designates the register address. This address denotes the specific register within a storage section in which the associated right-half drum word is to be stored. At present the G/A-FD, BO1, and BO2 storage sections use 26 registers; the G/G and TTY storage sections, 25 storage registers; and the G/A-TD storage section, 12 registers. A 5-bit code is used which furnishes 32 distinct addresses. Therefore, there are seven unassigned register addresses each for G/G and TTY, six unassigned register addresses for G/A-FD, and 10 unassigned for G/A-TD. It follows that if the 5-bit register address designates an unassigned storage address for the storage section designated by bits LS to L2, the register address is in error (illegal). This error is detected by the illegal register address detection circuit mentioned in 2.5.3. This circuit produces an illegal-register-address pulse if the register address is illegal. This pulse is used in the output alarm circuit and is also used in the same manner as the illegal-section-address pulse mentioned in 2.2.1.3. The illegal register address detection circuit uses only the signal levels from the 1 side of the flip-flops (2.5.3).

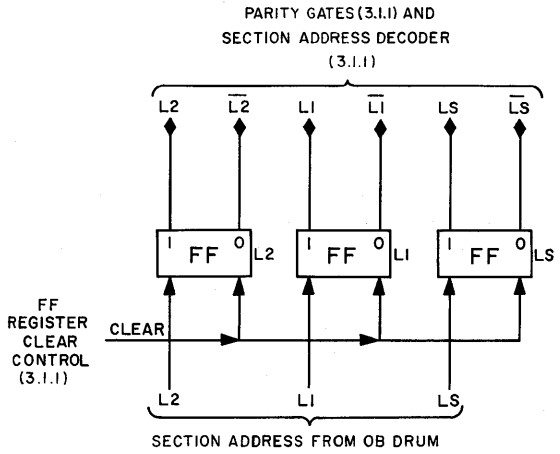


Figure 2–6. Section Address Register (3.1.1), Simplified Logic Diagram

A simplified logic diagram of the address register is shown in figure 2–7. The outputs of these five flip-flops are routed to the address decoder, to the illegal address detector, and to the parity gates. The parity gates are in the same location as the address registers. The register address decoder decodes the message contained in bits L3 to L7 to produce a signal level on one of the register address lines; there is one line for each register address. This signal level is passed to the STD's (fig. 2–2) and produces control which directs the right-half drum word to the assigned register in the assigned storage section.

As in the case of the other registers, the clear pulse clears the flip-flops approximately 7.9 μsec after the bits are entered.

2.2.1.5 Parity Register

The 33rd binary digit, designated P, is inserted in the drum word at the Central Computer System for parity checking purposes. The parity bit is therefore transmitted from the parity register to the parity gates to be counted with the other drum word bits. The parity register is merely a one flip-flop circuit (fig. 2–8). The parity register and gates are in the same location. For a detailed discussion of the parity checking operation, refer to 2.3.

2.2.2 Flip-Flop Register Clearing

The temporary storage period of the OB register is controlled by the flip-flop clear (reset) pulse. This pulse is generated by the drivers section of the parity register and drivers circuit. The controlling factors for the application of the clear pulse are shown in figure 2–9. The clear pulse is a gated OD 4 + 0.4-μsec timing pulse that is sent out on separate lines to clear various

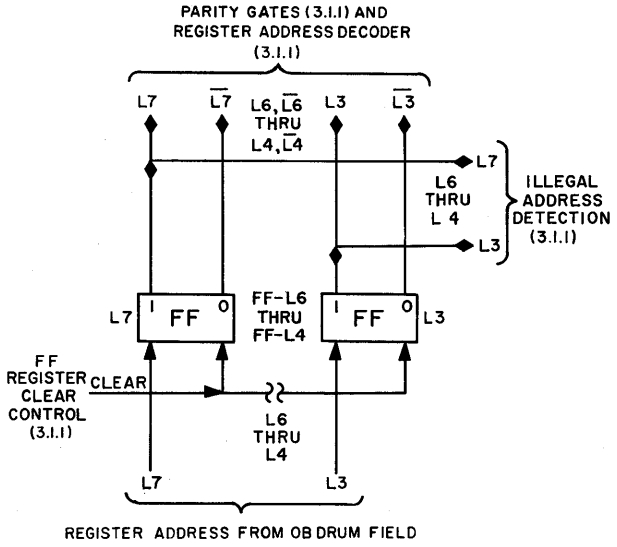


Figure 2–7. Register Address Register (3.1.1), Simplified Logic Diagram

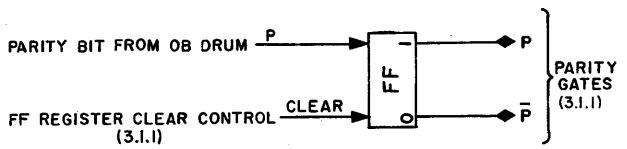


Figure 2–8. Parity Register (3.1.1), Simplified Logic Diagram

flip-flops and flip-flop registers as indicated in the figure.

Since the OB register receives the drum word at OD 1 time, the normal storage time of the OB register can be established at 7.9 μsec (OD 1 to OD 4 + 0.4). Referring to figure 2–9, it can be seen that the application of the clear pulse is dependent upon GT 1 and GT 2 being conditioned. The conditioning level that is applied to GT 1 is a not-error level (+10V) which is always present at this gate in normal operation. However, this level is brought down when an error in a word transfer operation occurs during a computer loop test operation. Gate tube 2 is normally conditioned by a +10V level which is applied through the normally closed contact points of de-energized relay K2. This relay is energized only during a unit loop test. Therefore, during normal operation, all of the OB register flip-flops will be cleared 7.9 μsec after receipt of a drum word.

When the Output System is placed in the unit loop test, K2 will be energized, preventing the right OB register flip-flops from being cleared except by manual operation. During a unit loop test, the right half-word is processed through a particular storage section, through the test circuitry, and then returned to complement the right OB register flip-flops. Each flip-flop containing a 1 will be complemented to its 0 side. Thus, by preventing the normal clearing of the right OB register flip-flops and by using neons, a visual indication of how correctly the test word was processed can be obtained.

Whenever K2 is energized, the conditioning level that is applied to GT 2 is dependent upon the output levels generated in the address decoder. In a unit loop test operation, the address portion of the OB register (L3-L7) is stepped once for each test word that is read into the storage array until all of the legal register addresses are made to contain the test word. When this occurs, and depending upon the section that is under test, an add-12 (G/A-TD), add-25 (G/G and TTY), or add-26 (G/A-FD, BO1, and BO2) level will be applied to condition GT 2. Conditioned GT 2 will then pass an OD 4 + 0.4 pulse to end the test word read-in operation.

To summarize, the registers are always cleared 7.9 μsec after a word is entered into the registers during normal operations. Only during test operations is it

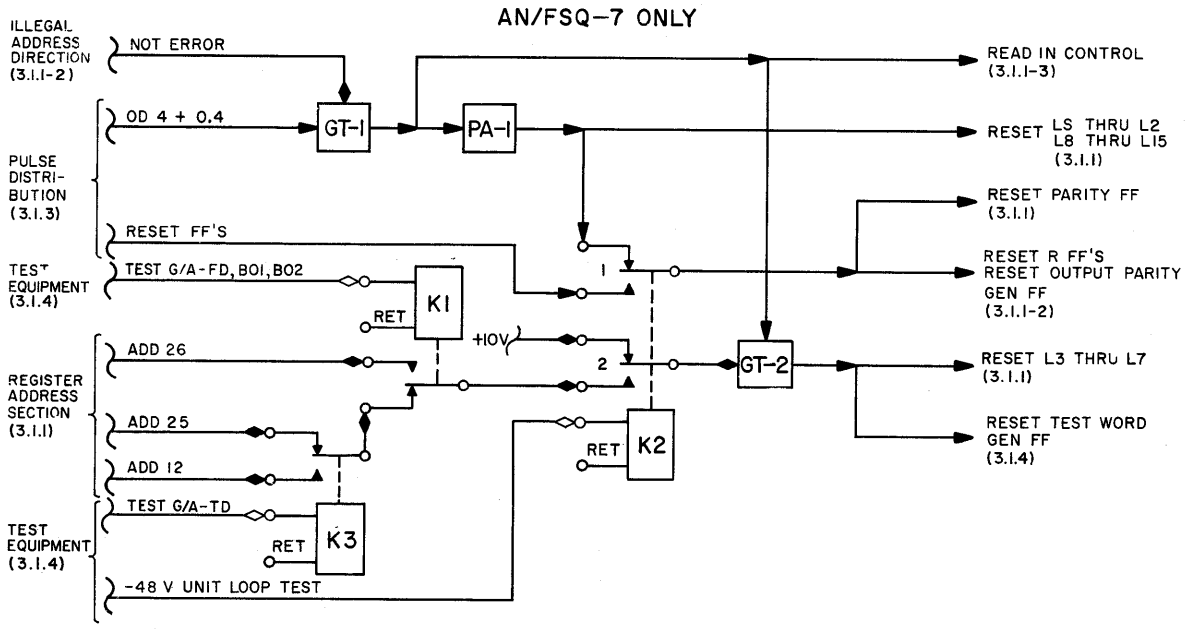


Figure 2–9. Flip-Flop Register Clear Control (3.1.1), Simplified Logic Diagram

possible for the drum word to remain in the registers longer than this period. Thus, during testing, a drum word may be retained longer than a normal time interval when test operations require this condition.

The OD 4 + 0.4 reset pulse shown in figure 2–9 is gated in the read-in control circuit when a word is missed. It then becomes a nonsearch signal to the output alarm section and the Central Computer. The OD 4 + 0.4 pulse is used since it occurs at a time sufficiently later than the time of entrance of the word (OD 1) to permit complete examination of the word.

2.3 PARITY CHECKING

2.3.1 Type of Parity Check

One of the conditions imposed on a drum word before acceptance by the Output System is correct parity. An odd parity check is employed, and each drum word received should have an odd number of 1's. The parity check functions in the following manner. The drum word (less the parity bit) is examined at the Central Computer System to determine whether the total number of 1's is odd or even. If the number of 1's is odd, a 0 parity bit is registered; the total number of 1's in the 33-bit drum word thus remains odd. Should the total number of 1's be even (before insertion of the parity bit), a 1 parity bit is registered, and the 33-bit drum word now contains an odd number of 1's. Therefore, any drum word received by the Output System should contain an odd number of 1's.

The presence of an even number of 1's in the drum word indicates that a 1 was either lost or gained during the time of transit between the Central Computer System memory buffer register and the Output System. Should such a situation arise, steps are taken to prevent the further transmission of the incorrect word. Also, an alarm signal is generated. (Note that the parity check would fail if the word were to gain or lose two 1's; the total number of 1's would then be odd and the word would appear to be correct. However, the probability of such an occurrence is slight, and the described parity check method is considered to be sufficiently accurate.)

A parity check is also performed on the transmitted output word at the equipment receiving the message. This requires the addition of a parity bit to the output word. The output word parity is not to be confused with drum word parity described above. More detailed information concerning output word parity is given in 2.3.4.

A discussion of the generation of the drum-word-test-parity pulse, the method of determining the parity status of a drum word, and the generation of the output word parity is given below.

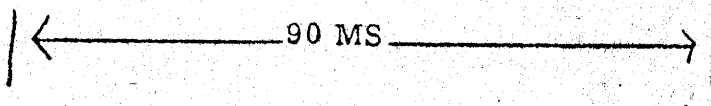
2.3.2 Drum Word Test Parity Generator

The parity check operation is initiated by applying a test-parity-even pulse to the right-half drum word register parity gates. This pulse is produced and controlled by the drum word test parity generator (figs. 2–2 and 2–10). The parity gates operated by all the flip-flop registers are connected serially, and the application of the test-parity pulse at the beginning of the

A switch is added to the unit 1 outputs panel for control of the T/D section operation. Two modes of operation are provided. The dual channel mode of the switch allows the operation to remain exactly as it was prior to E.C. R-74325 installation. The single channel mode position of the switch picks relays to transfer the T/D section to a single phone line output operation. The layout of the array address readout to the phone line is as shown below. While the dual mode is unchanged, it is also shown to facilitate comparison to the single line mode.

Dual Line Mode for One Burst Period

	adr.	adr.		adr.	adr.		adr.	adr.		
OSR1	9	8	S	5	4	S	1	0	S	to phone line 1
OSR2	11	10	S	7	6	S	3	2	S	to phone line 2



period of 1 complete array readout and 1 BTC step.

Single Line Mode for One Burst Period

	adr.	adr.		adr.	adr.		adr.	adr.		adr.	adr.		adr.	adr.		
OSR2	11	9	*	10	8	S	7	5	*	6	4	S	3	1	*	2	0	S

to phone line 1

OSR1 not used phone line 2 not used.

period of 1 complete array readout and BTC step.

Definition of Symbols

* -- 00000 (5 spaces for dummy sync format.)
S -- 00S00 (sync format.)
adr. -- one address of 17 bits with address numbering the same as shown on the array logic 3. 2. 5.

series connection produces a check of whether the complete drum word, including the parity bit, has odd parity.

The test parity flip-flop is set by the flip-flop register-loading pulse at OD 1 time. This pulse is received by the output control element from the OB drum signal simultaneously with each drum word. The flip-flop output level, after passing through an AND circuit, conditions GT 2 which passes an OD 1 + 1.9-μsec pulse as the test-parity-even pulse. A sampling of the parity gates then follows to determine drum word parity. (Refer to 2.1.3 for an explanation of OD timing.) At the completion of the parity check, a parity-OK or parity-NG pulse will be generated at approximately OD 2 + 0.8 μsec to clear the flip-flop, deconditioning GT's 1 and 2. The timing is such that GT 1 will not be conditioned at OD 3 time if a parity check of the drum word has been completed. Should the test-parity pulse not be generated, or if it does not get through all of the parity gates, GT 1 will be conditioned to pass the OD 3 pulse which will cause the generation of a lost parity alarm.

In order for the conditioning level of the two gates to be up, coincidence is required between the flip-flop output and the single-shot multivibrator output. The single-shot multivibrator used here has a normally positive output. Thus, when it is pulsed by the restart signal from the test equipment, the single-shot multivibrator produces a negative output level of 100-ms duration before reverting to its normal positive level. This inhibits the passage of test-parity pulses.

During an Output System test operation, the flow of drum words from the OB fields to the output control element is temporarily halted by the inhibiting action of a stop pulse manually generated in the output test equipment section and sent to the read circuits of the OB fields. Therefore, during a test operation, output data which should be transmitted at the time the test operation is in progress accumulates on the OB fields. At the completion of a test operation, a restart pulse is manually generated in the output test section and sent to the OB field read circuits where it restarts the flow of drum words to the output control element. The restart pulse is also sent to the drum word test parity generator, shown in figure 2–10, where it triggers the single-shot multivibrator. The drum words received by the output control element following a test operation are those that should have been transmitted during the test operation. Thus, these drum words contain old data and will be destroyed.

Destruction of these drum words is accomplished in the output control element by accepting all drum words from the OB fields and not transferring them to the output storage element during the 100 ms following the generation of the restart pulse. This is the purpose of the single-shot multivibrator in the drum word test parity generator. Since its output is produced by the restart pulse, the test-parity signals are not generated during the 100-ms interval following receipt of the restart pulse. Because no parity check is performed on the drum words received during this time, the drum words are accepted by the output control element from the OB fields but are not transferred to the output storage element. Consequently, during the 100-ms interval, successive drum words are loaded into the flip-flop register, and approximately 7.9 μsec after each drum

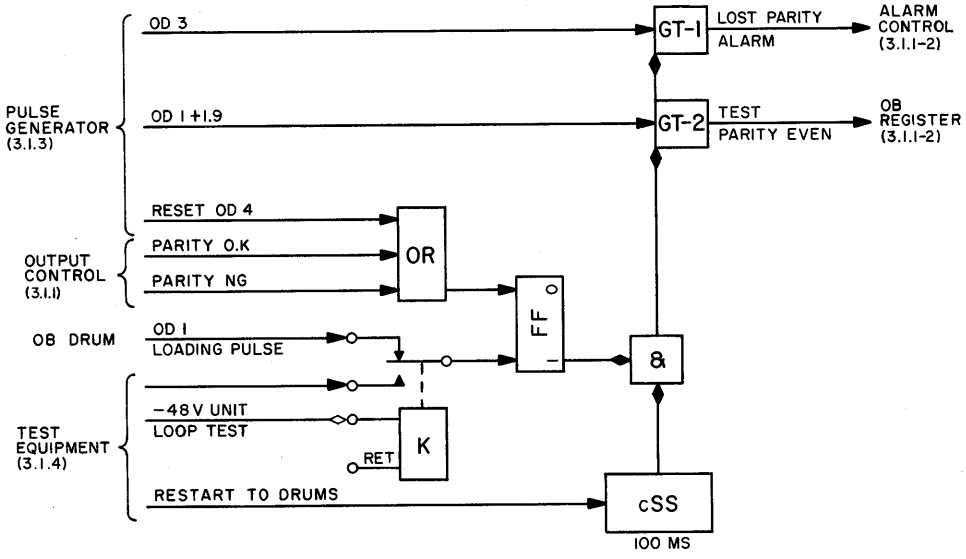


Figure 2–10. Drum Word Test Parity Generator (3.1.1-2), Simplified Logic Diagram

word is placed in the flip-flop register, the flip-flop register is cleared. Since these words are accepted from the OB fields, the status of the drum registers in which they were stored on the OB fields is changed to indicate that the registers contain old information. Thus, successive clearance of the flip-flop register destroys the drum words. Approximately 65 ms are required to read the three OB fields; therefore, at the completion of the 100 ms following a test operation, all old output data has been destroyed.

As shown in figure 2–10, the flip-flop may also be set by a selected read-in-test-word pulse from the test equipment. This is also a test equipment function and is used to generate a test-parity signal while the equipment is under test, since information flow from the OB fields, including the OB-register-loading pulse, is cut off during test.

2.3.3 Drum Word Parity Gates

The drum word received from the OB drum is subjected to a parity test to determine whether it contains an odd or even number of 1's. It has been shown that a correct incoming word must be of odd parity. An even parity indicates the presence of an error. Both the 1 and 0 outputs of the register flip-flops serve as conditioning signals for the parity gates (fig. 2–11). A test-parity pulse then successively samples the parity gates associated with the 33 drum word bits. The result is either a parity-OK signal, indicating odd parity, or a parity-NG signal, indicating even parity.

The test-parity pulse is simultaneously applied to GT's 1 and 2 (which are in the right-half drum word register at OD 1 + 1.9 μsec). Assume that flip-flop R15 of the right drum word register is set in the 1 state. Gate 1 is conditioned to pass the test-parity pulse and passes a pulse which is then designated odd. Gate 2 does not pass the test-parity pulse because the conditioning of GT 1 resulted from register R15 being in the 1 state. The portion of the drum word thus far scanned contains an odd number of 1's. Therefore, the output of GT 1 is designated as odd. Carrying this procedure to the following stage, the odd pulse then simultaneously samples GT's 4 and 5. Assume that level R14 is down (bit R14 of the drum is a 0); GT 5, as expected, passes an odd signal to the next stage.

Consider the case where bits R14 and R15 are 1's. The scanning of the two respective stages should then indicate an even parity. The odd pulse from GT 1 samples GT's 4 and 5, but only GT 4 is conditioned to pass the signal which is appropriately labeled "even."

The scanning continues in similar fashion through the remaining gates associated with all the drum word bits. The result, at the output of the parity gates, is either the parity-OK or the parity-NG pulse, indicating odd or even parity, respectively. The parity-OK pulse, if generated, goes to the read-in control of the read-in section (figs. 2–2 and 2–11). The action of the pulse is described in 2.6. Briefly, a parity-OK pulse is necessary for the right-half drum word to be transferred to the output storage section. The parity-NG pulse, if generated, goes to the output alarm section to set an alarm indicating an error in the parity of the input drum word.

Either the parity-OK or parity-NG pulse, depending upon which is generated, goes to the illegal address detection section. The action of these pulses is described in 2.5. Briefly, the pulse that is present is used as a pulse

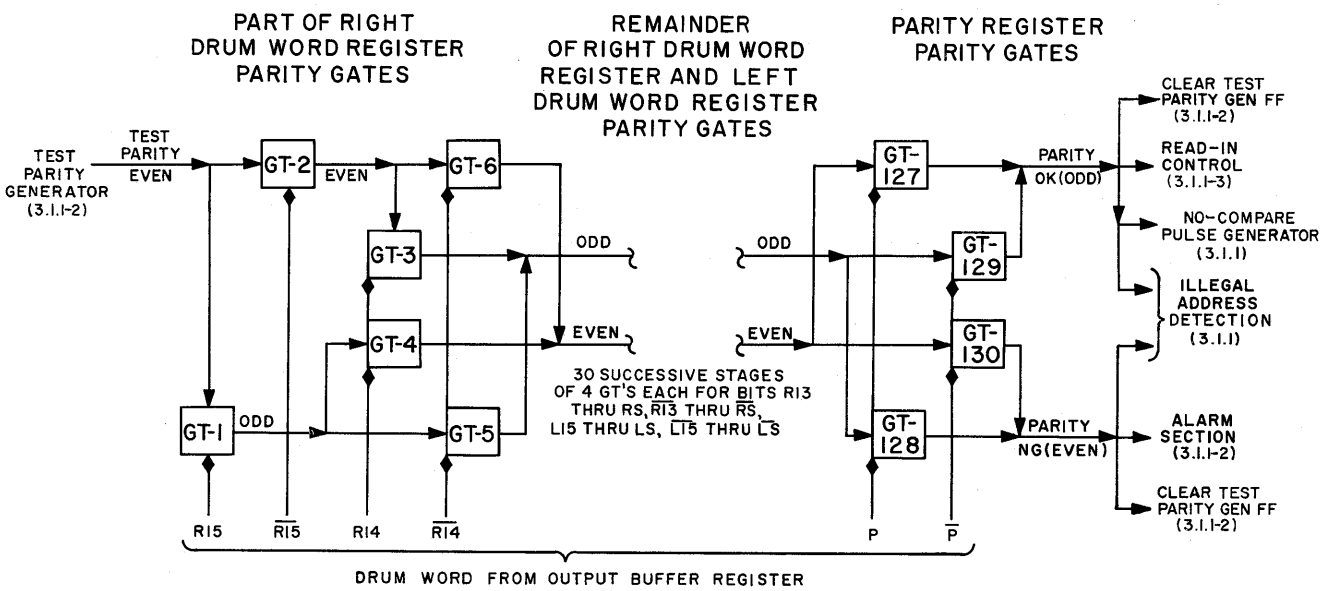


Figure 2–11. Drum Word Parity Gates (3.1.1, 3.1.1-2), Simplified Logic Diagram

source for the generation of the illegal-register-address pulse and the illegal-section-address pulse, if either of the addresses is illegal. Also, the parity-OK pulse is used in the generation of the no-compare pulse. The no-compare pulse is generated when the burst number is wrong but the address, parity, and search timing are correct. (Refer to 2.6.) The reason that parity-OK or -NG pulses are used in the illegal address detection circuits is to cause these checks to be made after the parity check but to be independent of the results. In addition, the parity-OK or parity-NG pulses are used to clear the test parity generator flip-flop for the reasons explained in 2.3.2.

2.3.4 Output Word Parity Generator

Since the drum word does not remain intact beyond the output control element, the drum word parity bit cannot be used as the storage word parity bit. Therefore a new parity bit is generated for each right-half drum word as it is read into the storage array and is transmitted with it on the telephone lines. This permits one parity check to be made as the message leaves the Output System and another at the receiving equipment. Thus, possible errors incurred during the processing of the word through the storage element or through the telephone equipment may be detected.

The following paragraph describes the operation of the output parity generator circuit for all sections except G/A-TD which is discussed in paragraph 4.4.6.4 of Part 3.

In normal operation, relay K1 is de-energized (fig. 2–12); also, the flip-flop is cleared 7.9 μsec after each word is read into the OB register. The parity-checking pulse (OD 1 + 1.9) emanates from the last parity gate of the right-half drum word (RS) as either a parity-odd or parity-even pulse to strobe the gate. This pulse occurs at approximately OD 2 time. If parity of the right-half drum word is even, the flip-flop remains clear; thus, the storage parity bit will be a 0 maintaining an even number of 1 bits in the storage array. On the other hand, if the parity-checking pulse appears on the odd line, the flip-flop will be complemented to its set side. Then the parity bit added to the right half-word will be a 1, making the total number of 1 bits even. It can be seen that for all sections except G/A-TD, storage parity will be even.

The storage parity of a G/A-TD word is odd; therefore, additional circuitry is required to utilize the output parity generator flip-flop in a manner similar to that of the other sections. When a G/A-TD word is read into the OB register, a select-section-5 level will be generated to condition the gate. This gate will then pass the OD 1 + 1.9 parity-checking pulse which strobes it to set the flip-flop. Assuming that the right half-word has odd parity, a parity-odd pulse (OD 2) will be produced to complement the flip-flop to its clear side. Thus, odd parity of the right half-word is maintained. The relay will be energized only when unit loop testing any section other than G/A-TD. During unit loop test, the operation of the parity generator circuit is, by necessity, slightly different; however, even storage word parity for all sections other than G/A-TD (which has odd parity) will be maintained. For a more detailed discussion of this circuit during a unit loop test, refer to 2.5 of Chapter 2, Part 5. Since the AN/FSQ-8 uses only a G/G and a TTY storage section, the operation of the output parity generator circuit differs somewhat

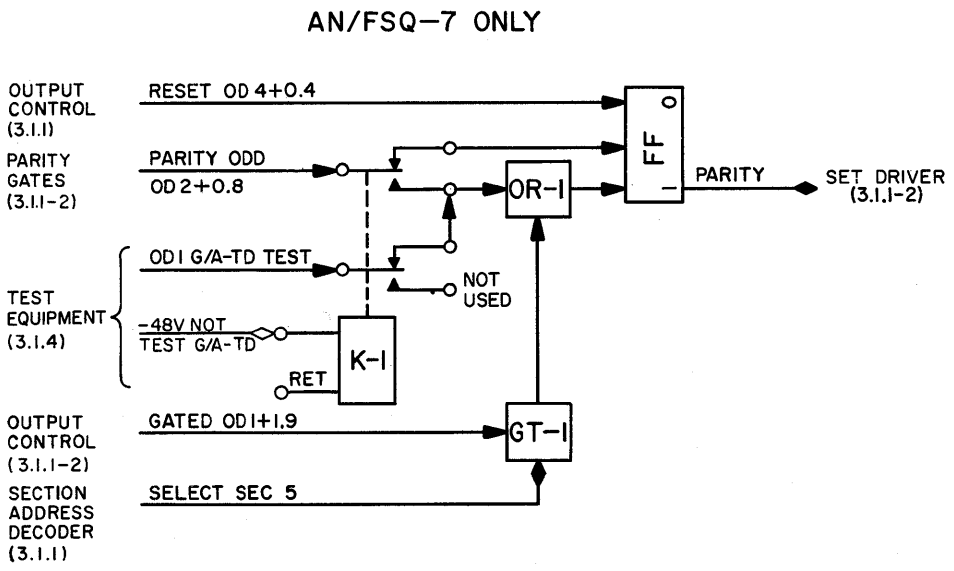


Figure 2–12. Output Parity Generator (3.1.1-2), Simplified Logic Diagram

from the previous description. For a discussion of the operation of the AN/FSQ-8 output parity generator circuit, refer to 2.2.2 of Chapter 2, Part 5.

2.4 DECODING

2.4.1 Need for Decoding

Previously, it was mentioned that each right-half drum word has associated with it a storage section address and a storage register address. The addresses are in binary coded form and must be decoded before a word can be routed to its proper destination. Further, each word falls into a particular slot. A slot is a group of registers within a storage array that feed one telephone channel. Therefore, the contents of a given slot are words of one message having a common destination. The method of slot detection and the coding of the section address and register address are explained below.

2.4.2 Section Address Decoder

The input signals to the section address decoder consist of the three address bits from the section address register flip-flops (fig. 2–13). There are eight possible variations of section decoder inputs in binary code whose equivalents correspond to decimal digits 0 through 7. Each of the eight combinations of three d-c levels is fed to a separate AND circuit. When all three inputs to one of the AND circuits are simultaneously positive, a select-section level is fed to the read-in control circuit. Select sections 1, 2, 3, 5, 6, and 7 represent the G/A-FD, G/G, TTY, G/A-TD, BO1, and BO2 sections, respectively. Numbers 0 and 4 are presently unassigned since present plans call for only six output sections. Therefore, a binary code corresponding to these numbers (illegal sections) constitutes an error in the section address. If a select-section-0 or a select-section-4 level is produced, it is sent to the illegal sec-

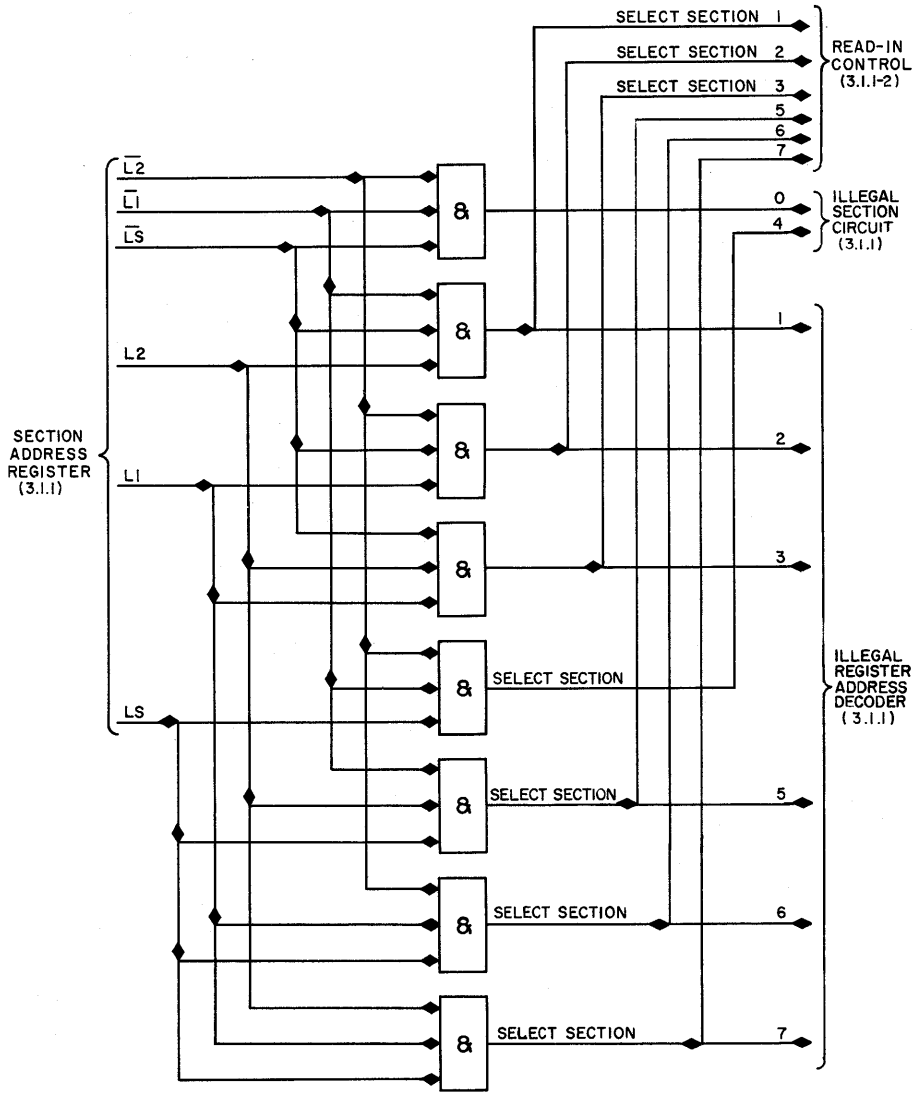


Figure 2–13. Section Address Decoder (3.1.1), Simplified Logic Diagram

tion circuit and thence to the alarm control circuit, whereupon an illegal section alarm is generated. The possible binary codes and their respective section assignments are shown in table 2–2.

The AN/FSQ-8 section address decoder is basically the same as that described above except that only two section addresses, G/G and TTY (010, 011, respectively), are legal. Therefore, the other section address numbers 0 and 4 through 7 will be decoded as illegal sections.

2.4.3 Register Address Decoder

Each right-half word entering the Output System has an associated register address in binary code. The address consists of five bits with 32 possible combinations. A decoding operation is then necessary to produce one signal corresponding to each 5-bit address (fig. 2–14).

Bits L3 to L7 are applied to the decoder from the register address register flip-flops. Two of the five bits (L3 and L4) are fed in four combinations to four AND circuits. The remaining bits (L5, L6, and L7) form eight combinations, each of which is applied to an AND circuit. By further combining the L3 and L4 AND outputs with the L5, L6, and L7 AND outputs, output signals are produced on 32 possible lines, each line representing a different register address.

A +10V level is produced on the line which corresponds to the decoded address. This level is then sent to the STD's in preparation for reading the right-half drum word into a storage section register address. Register addresses 0 through 25 are passed to the STD's, whereas register addresses 26 through 31 are designated unassigned. The G/A-FD, BO1, and BO2 storage sections use register addresses 0 through 25; the G/A-TD storage section uses register addresses 0 through 11; the G/G storage section, addresses 0 through 24; and the TTY storage section, register addresses 0 through 24. Note that register addresses 0 through 25 are sent to the slot detection network (refer to 2.4.4) and that addresses 12, 25, and 26 are sent to the OB register clear control circuit. The register addresses in binary code and their respective decoded assignments are given in table 2–3.

TABLE 2–2. SECTION ADDRESS ASSIGNMENT

BINARY CODE (INPUT)			SELECT SECTION	SECTION ASSIGNMENT (OUTPUT)
LS	L1	L2		
0	0	0	0	Illegal section
0	0	1	1	*Ground-to-air – FD
0	1	0	2	Ground-to-ground
0	1	1	3	Teletype
1	0	0	4	Illegal section
1	0	1	5	*Ground-to-air – TD
1	1	0	6	*BOMARC 1
1	1	1	7	*BOMARC 2

*Illegal sections in AN/FSQ-8

2.4.4 Slot Detection, Circuit Description

As each right-half drum word is ready to be placed in a storage section register, the corresponding slot is noted in the slot detection circuit. The purpose of this circuit is to produce signals which are used in the G/A-FD, BO1, BO2, G/G, and G/A-TD output storage sections to determine how many registers in each slot are filled. The TTY output storage section does not require slot detection information since there is only one register per slot for this storage section.

It is necessary to produce a +10V slot level on the line associated with a particular slot whenever a G/G or G/A-TD word appears which has a register address corresponding to this slot. This is known as slot detection and is accomplished as shown in figure 2–15, fold-out. The G/G slot levels are developed as the outputs of five 6-way OR circuits; each OR circuit produces an output for each register address introduced from the register address decoder. One G/G storage section has 25 registers divided into five slots. Consequently, only register addresses 0 through 24 are required to produce G/G slot signals 1 to 5. Hence, five +10V slot levels are required for each G/G slot (one +10V level for each word read into a slot); in effect, this indicates that all five registers of a message slot are filled and can be transmitted. Therefore, if a G/G array were filled with information, 25 +10V levels would be generated, indicating that 25 registers are filled and ready for transmission.

The G/G slot levels are also produced by a d-c level from the completed message shift register. This signal, labeled clear-G/G-CMSR, is not associated with a specific right-half drum word. Rather, it is a timed level which arrives just before readout begins, to check the completeness of a G/G message, if any, in each message slot. If a G/G message slot is not filled by the time G/G readout is to take place, that message is considered to be incomplete and is not sent out on the telephone lines. The action of the G/G slot levels in the completed message shift register of the output storage section is to prevent a G/G message from being sent to the telephone lines if the clear-G/G-CMSR signal arrives at the slot detection OR circuits before all the registers in a slot have been filled.

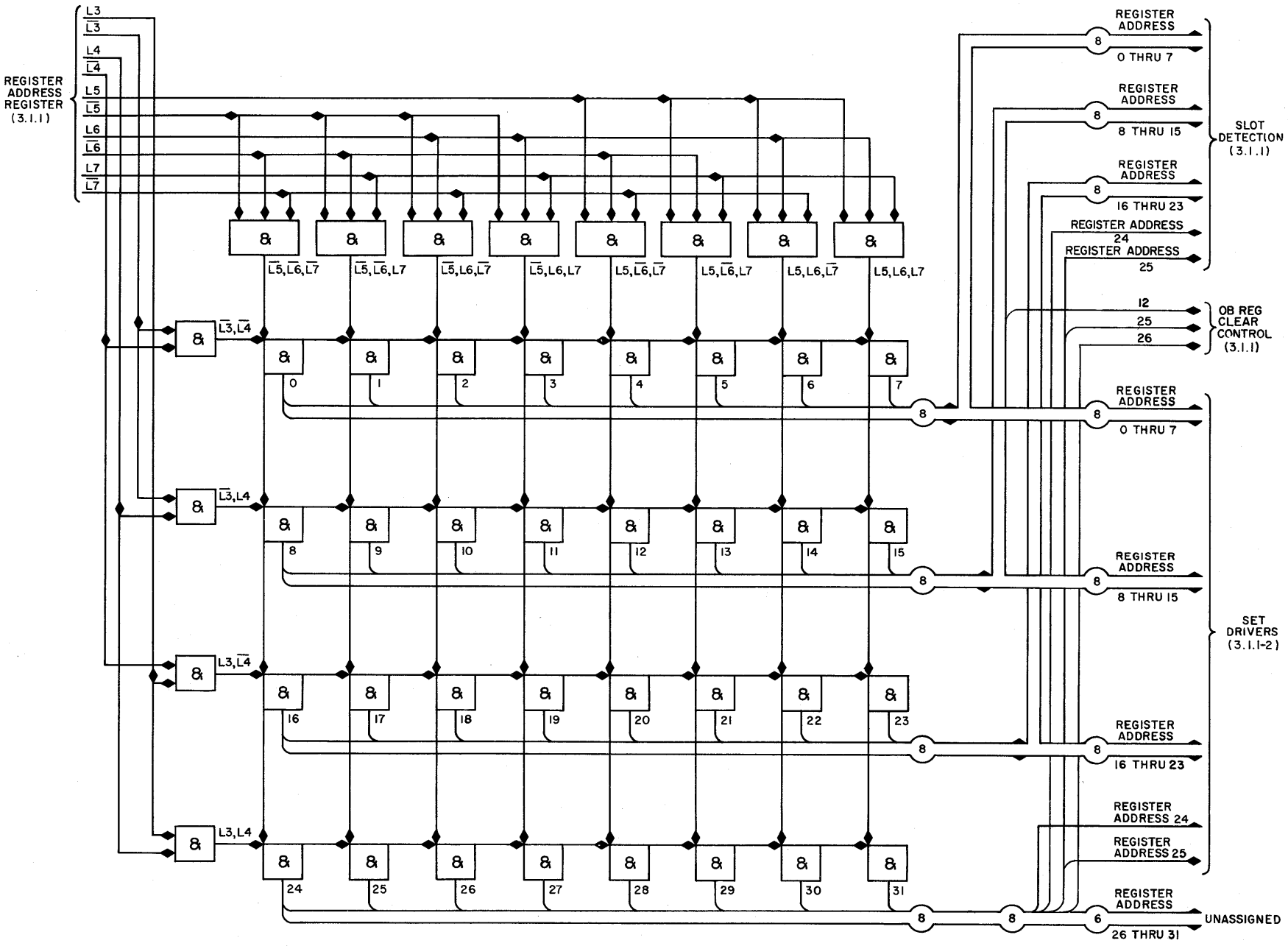


Figure 2–14. Register Address Decoder (3.1.1), Simplified Logic Diagram

Although the register addresses for all six storage sections enter the five OR or G/G circuits, the signals are rejected from the completed message shift register unless the shift pulse from the shift-completed message shift register pulse generator (fig. 2–15) is also sent to the completed message shift register. Since this pulse is sent only if the section address is G/G, if the burst number compares with the G/G burst counter, and if G/G search time is in progress, the completed message shift register responds to the slot signal only if a G/G word is to be entered.

The operation of the slot detection circuit for G/A-TD is the same as that described for the G/G storage section except that G/A-TD has only three slots. Now consider the production of the G/A-FD slot pulses. The G/A-FD storage array consists of 26 registers which are divided into two slots, whereas the G/A-TD storage array consists of 12 registers which are divided into three slots. It is arranged that a G/A-FD word whose register address is one of 0 through 12 produces a G/A-FD slot 1 pulse; a 13 through 25 register address produces a G/A-FD slot 2 pulse. Also, a G/A-TD word whose register address is 0 through 3 produces a G/A-TD slot 1 pulse; register address 4 through 7, a G/A-TD slot 2 pulse; and register address 8 through 11, a G/A-TD slot 3 pulse.

The production of the G/A-FD slot pulses differs from that of the G/A-TD slot pulses in that additional circuitry is required to divide the 26 G/A-FD register addresses into two groups so that two G/A-FD slot pulses may be produced. As shown in figure 2–15, G/A-FD registers 13 through 25 are connected to OR 9. Should any one of these input lines be positive, a positive level conditions GT 1 to produce a G/A-FD-slot-2 pulse at OD 4 +0.4 time. Should a G/A-FD word be addressed to a register in the 0 through 12 group, a −30V level will be applied to OR 9, causing the inverter to condition GT 2, which produces a G/A-FD slot 1 pulse at OD 4 +0.4 time. The G/A-FD slot pulses are then routed to the storage parity check circuit in the output storage element. Here, a check is made to determine whether the number of busy bits equals the number of filled registers. (Refer to Ch 2 of Part 3.) In the G/A-FD storage section, readout is not controlled by the slot pulses, because a G/A-FD message may be complete even if all the registers in a slot are not filled. The pulse which is passed by the G/A-FD slot detection circuit is an enable-G/A-slot pulse from the G/A-FD read-in control (refer to 2.6.2). This enable pulse is present only if the drum word has a G/A-FD section address, if the burst number compares with the contents of the G/A-FD burst counter in the output storage section, and if search time is in progress. In other words, the G/A-FD slot pulse is produced only if the

TABLE 2–3. REGISTER ADDRESS ASSIGNMENT

CODED REGISTER ADDRESS (INPUT)					DECODED REGISTER ADDRESS (OUTPUT)
L3	L4	L5	L6	L7	
0	0	0	0	0	Register address 0
0	0	0	0	1	Register address 1
0	0	0	1	0	Register address 2
0	0	0	1	1	Register address 3
0	0	1	0	0	Register address 4
0	0	1	0	1	Register address 5
0	0	1	1	0	Register address 6
0	0	1	1	1	Register address 7
0	1	0	0	0	Register address 8
0	1	0	0	1	Register address 9
0	1	0	1	0	Register address 10
0	1	0	1	1	Register address 11
0	1	1	0	0	Register address 12
0	1	1	0	1	Register address 13
0	1	1	1	0	Register address 14
0	1	1	1	1	Register address 15
1	0	0	0	0	Register address 16
1	0	0	0	1	Register address 17
1	0	0	1	0	Register address 18
1	0	0	1	1	Register address 19
1	0	1	0	0	Register address 20
1	0	1	0	1	Register address 21
1	0	1	1	0	Register address 22
1	0	1	1	1	Register address 23
1	1	0	0	0	Register address 24
1	1	0	0	1	Register address 25
1	1	0	1	0	Register address 26
1	1	0	1	1	Register address 27
1	1	1	0	0	Register address 28
1	1	1	0	1	Register address 29
1	1	1	1	0	Register address 30
1	1	1	1	1	Register address 31

word is a G/A-FD word and has arrived in the correct sequence during G/A-FD search time. The BO1 and BO2 storage section slot detection circuit operates in the same manner as the G/A-FD slot detection circuit.

2.5 ILLEGAL ADDRESS DETECTION

2.5.1 Introduction

At present, not all of the possible storage section addresses and register addresses are assigned. A code representing one of the unassigned addresses is known as an illegal address and denotes an address error. The detection of illegal register and section addresses is discussed below.

2.5.2 Illegal Section Address Detection

Of the eight possible storage section addresses, only six (sections 1, 2, 3, 5, 6, and 7) are presently used. Consequently, the presence of section address 0 or 4 is indicative of a section address error. An error in a section address is detected by means of the illegal section address circuit (fig. 2–16). The detection is accomplished by passing either one of the illegal select-section levels through an OR circuit to condition a gate. The illegal-section pulse is produced when either the parity-NG or the parity-OK pulse samples the gate. In this manner, the illegal-section pulse is generated after the parity check is made and is independent of the parity check results. The illegal-section pulse is then sent to the alarm section; also, an illegal-section level is made available to the no-compare pulse generator. A no-compare pulse cannot be generated if there is an illegal-section level (+10V) present. (Refer to 2.6.)

2.5.3 Illegal Register Address Detection

Consider first an illegal register address associated with a TTY or G/G word, both of which have the same number of registers. Referring to figure 2–17, note that a select-section level, designating that the

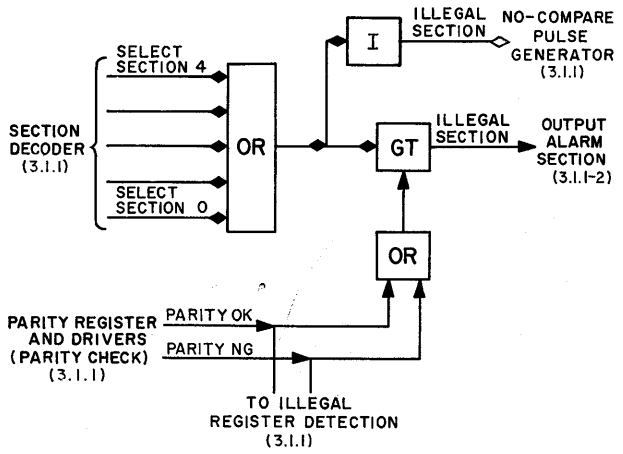


Figure 2–16. Illegal Section Address Detection (3.1.1), Simplified Logic Diagram

G/G or the TTY section, as called for by the left-half drum word, is sent by the section decoder to the illegal register address detection circuit. The OR 1 circuit applies a level to the AND 1 circuit if either of these sections is designated by the left-half drum word. Also applied to this AND circuit are bits L3 and L4 of the left drum word, and bit L5, L6, or L7 of the left drum word, via the OR 2 circuit. These bits make up the coded register address. Therefore, in order for AND 1 to pass a pulse, a select-section-2 or -3 pulse must be present (G/G or TTY); bits L3 and L4 must both be 1's; and one of the bits L5, L6, or L7 must be a 1. Checking the register address assignment table (table 2–3), bits L3 and L4 are both 1's only for register addresses 24 through 31. However, only for register addresses 25 through 31 is there a 1 for L5, L6, or L7. Therefore, only for register addresses 25 through 31 does the AND circuit produce a +10V level. In brief, then, a +10V level is produced from the AND 1 circuit if the decoded section address portion of the drum word is G/G or TTY and the coded register address bits have 1's in such a position as to call for register address 25, 26, 27, 28, 29, 30, or 31. Since these register addresses are unassigned, and therefore are illegal, the level designates an illegal address.

The G/A-FD, BO1, and BO2 storage sections use register addresses 0 through 25. In figure 2–17, it is seen that the AND 2 circuit passes a +10V level only if register address word bits L3, L4 and either L5 or L6 are 1's and if a select-section -1, -6, or -7 level is sent from the section address decoder. Again, referring to the register address assignment table (table 2–3), L3 and L4 are 1's only for registers 24 through 31. However, L5 or L6 is a 1 at the same time only for registers 26 through 31. Therefore, the AND 2 circuit produces a +10V level only when the decoded section address portion of the drum word is G/A-FD, BO1, and BO2 and the coded register address bits have 1's in such a position as to call for register address 26, 27, 28, 29, 30, or 31. Since these register addresses are unassigned, and therefore are illegal, the level designates an illegal address.

The G/A-TD storage section uses register addresses 0 through 11. Referring to figure 2–17, the AND 3 circuit will produce a +10V level only when the select-section-5 level is present and when register address bit L3 is a 1. Referring to table 2–3, L3 will be a 1 for addresses 16 through 31, making these addresses illegal. The AND 4 circuit will pass a +10V level when the select-section-5 level is present and when register address bits L4 and L5 are 1's. These bits will both be 1's for addresses 12, 13, 14, and 15, thereby making them illegal. Therefore, a +10V illegal-address level will be produced by either AND 3 or AND 4 for addresses 12 through 31.

The four AND circuits feed an OR circuit. Therefore, if any of the AND 1, 2, 3, or 4 circuits passes an illegal-register-address level, the OR circuit will pass this level. This conditions a gate which then passes an illegal-address pulse derived from either the parity-OK or parity-NG pulse. In this way, the illegal-register-address pulse is generated after the parity check is made and is independent of the parity check results. The illegal-address pulse goes to the output alarm section and the illegal-address level goes to the no-compare pulse generator. A no-compare pulse cannot be generated if there is an illegal-register-address +10V level.

2.6 STORAGE ELEMENT

2.6.1 Review of Operations

The following briefly summarizes the action of the Output System to this point. The drum word received from the OB drum, after being placed in the flip-flop register, is examined to ascertain its parity, section address, register address, and storage array slot. Moreover, provision is made for detecting an illegal register or section address. In addition, the burst number is compared with the contents of the burst counter in the output control element. Favorable results of the above tests then form the basis for acceptance of a right-half drum word by the Output System.

The flow of a right-half word from the drum word register through the STD's and half-write current generator to a storage matrix is shown in figure 2–18. The read-in control circuit acts as a valve which permits the passage of an acceptable right-half word and prevents entrance of a right-half drum word which does not conform to the established criteria.

The read-in operations associated with each drum word occur during a 5.4-μsec interval from OD 2 to OD 4 + 0.4 (OD 4 pulse delayed 0.4 μsec). A drum word is received by the OB register from the OB fields at OD 1 time. Between this OD 1 time and the follow-

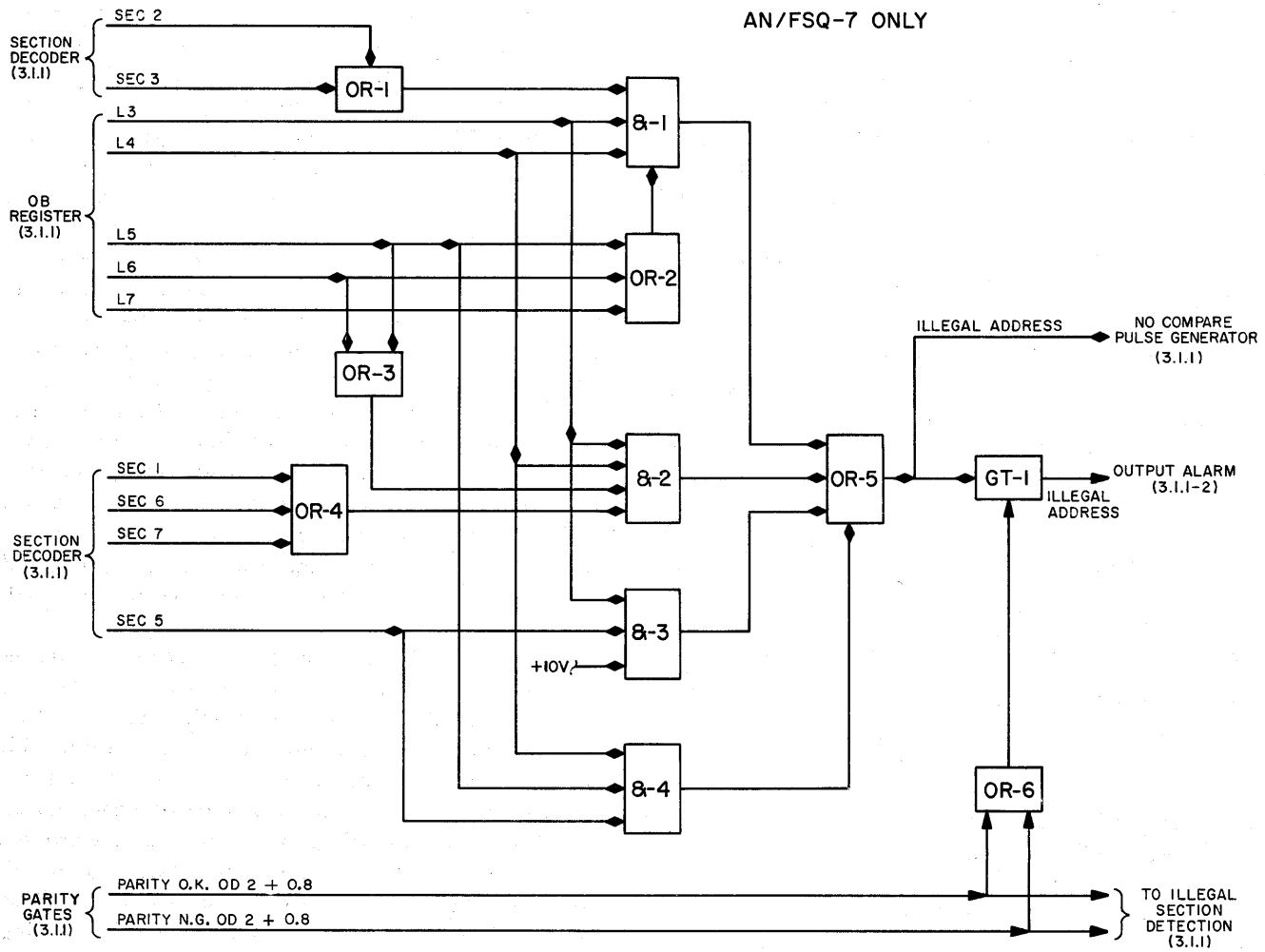


Figure 2–17. Illegal Register Address Detection (3.1.1), Simplified Logic Diagram

ing OD 2 time, the operations mentioned in the preceding text occur. The right-half drum word, output storage parity bit, and register address pulses are present in the STD's by the OD 2 time. If the drum word is acceptable, this data will be transferred to the selected storage section through the half-write current generator. The acceptance of a drum word is determined by the read-in control circuit.

At the initiation of read-in operations, the read-in control circuit is supplied with the data required to determine whether the drum word is to be accepted and then transferred. This information is:

a. The selected storage section.
b. The result from each burst counter of the comparison between the burst number and the contents of the burst counter.
c. The presence of search or nonsearch time in each storage section.
d. The result of the parity count.

If a storage section is selected and the burst number matches the contents of the burst counter associated with the selected storage section, the right half of the drum word is intended to be transmitted by the selected storage section during the current burst period. A storage section receives data during the first part of a burst period called search time. It transmits the data during the later portion of the burst period, called readout time, and cannot receive data during readout. The read-in control circuit is informed of the portion of a burst period in progress in each of the six storage sections.

If, at the initiation of the read-in operation, search time is in progress in the selected section, if the burst number is equal to the contents of the selected storage section burst counter, and if no parity or address errors are detected, the drum word is acceptable. With these favorable conditions present, the read-in control circuit causes the transfer of the data in the STD's to the selected storage section. However, if all conditions are the same except that readout is in progress, the drum word is missing from the burst being transmitted. This is referred to as a nonsearch alarm condition. When such a condition is detected, an alarm pulse is generated by the read-in control circuit and sent to the alarm section of the output control element. Also, the word is rejected and effectively erased from the OB field.

If there are no errors in the drum word, but the burst number does not compare, the drum word is assumed to have arrived too early and is not acceptable at this time. Under this condition, the read-in control circuit causes the no-compare pulse generator to produce a no-compare pulse. This pulse is sent to the OB fields and causes the register associated with the drum word to retain its status. Thus, although the drum word is rejected, it remains on the OB fields for acceptance during a future burst period.

Whenever a parity or address error is detected in a drum word, or a nonsearch condition exists, while at the same time the burst number compares, the generation of a no-compare pulse is suppressed. Thus, whenever an error is found, the status of the drum word register on the OB fields is changed (the word is erased). In addition, the read-in control circuit prevents the transfer of data to the storage element. This arrangement provides a means of eliminating incorrect or missed drum words from the OB fields and preventing their transmission.

The read-in control circuit produces the signals required to transfer the data from the STD's through the half-write current generator. The half-write current generator, in general terms, consists of several channels, any of which could be filled with the data from the STD's. At least one channel connects the half-write current generator with each storage section. Upon acceptance of the drum word, the read-in control circuit ensures that the data from the STD's is routed through the proper channel in the half-write current generator to the selected storage section.

At OD 2 time (start of read-in), six inhibit pulses are generated by the read-in control circuit and sent to

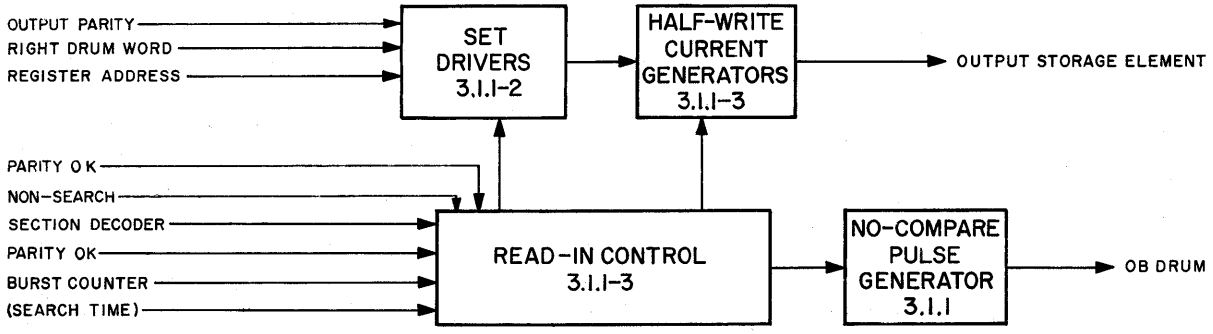
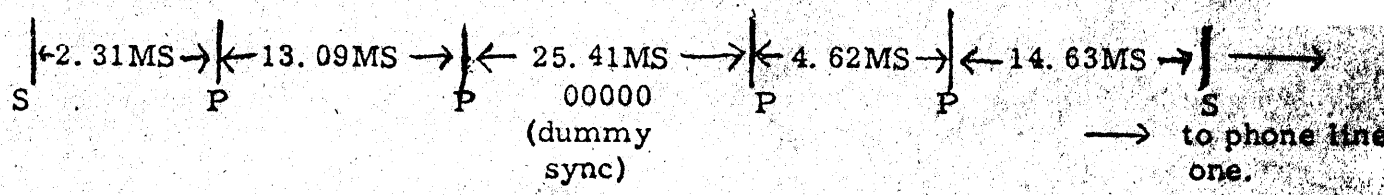


Figure 2–18. Read-In to Storage Element, Simplified Logic Diagram

Another item not yet mentioned is the auto parity bit generation during no data transmission times. With no data loaded into the array for readout, an auto parity bit is generated on phone line 1 for each address. The auto parity format for each group of 4 addresses is as follows:



Part II

Specific Functions of the New Single Channel Circuitry

1. 42GC K4 and K7 (logic 3.1.2). In single channel mode, the burst time counter step time is changed to a time of 180 MS per step. The high order BTC position (42FC BFF6) is not used for a BTC compare. This results in the complete BTC cycle or total step time being the same in both dual and single channel mode.

2. 33EK relays K1, K2, K4, K5, K6, K7 and K8 (logic 3.2.5, coord. 9-13A). This transfers the 15 counter into an 18 counter during single channel operation.

3. 33EK relay K9 (logic 3.2.5, coord. 3B). It disables the fast shift circuit from operation during single channel mode.

4. Relays 33NNK4, 33NJK5 and 33NNK1 (logic 3.2.5 area 4D and E). Their function is to eliminate data from phone line 2 and route all signals to the channel 1 output lines. At BOADS, NLK3, NLK1, and NJK5 are used for this application.

5. 33EJ (logic 3.2.5 coord. 6A). The 270 OR, with 18 = 6, 12, and 18, inputs, is used to generate the sync bits on the phone line in single channel mode. The OR, with 18 = 3, 9, and 15, is used to generate the dummy sync format.

the half-write current generator flip-flops. These inhibit pulses block the channels to the storage sections that are not selected. A set pulse is generated 1.2 μsec after the inhibit pulses, producing a level which is sent to the STD's. The set level gates the data (right-half drum word, storage parity bit, and register-address levels) to the half-write current generator. As a result of the inhibit pulses, the data is placed only in the selected storage section channel (the one uninhibited channel). At the termination of read-in to the CCD's, a reset level is produced in the read-in control circuit at OD 4 + 0.4 time. This reset level is applied to the CCD's of the selected storage section and shifts the data to the selected address of the selected storage section.

2.6.2 Read-In Control

The read-in control circuit gathers the data that is necessary for the acceptance of a drum word. On the basis of the collected information, the circuit responds either to accept or reject the word. If the word is acceptable, the read-in control circuit initiates steps which subsequently cause the word to be transferred into its storage section.

The read-in control circuit is divided into seven parts. Those portions of the read-in control circuit that are associated with the G/A-FD, BO1, BO2, G/G, G/A-TD, and TTY drum words form six of the seven parts. The remaining part is that which is common to all six. The G/A-FD, BO1, BO2, G/G, G/A-TD, TTY, and common parts of the read-in control circuit are discussed separately, followed by a summary of their combined operation, below.

The action of the G/A-FD read-in control can best be understood by referring to the simplified logic diagram (fig. 2–19). The G/A-FD read-in control operations are dependent upon four levels: search-G/A-FD, compare-G/A-FD, select-section-1, and not-search-G/A-FD. The select-section-1 level is received from the section address decoder, and when up, indicates that the drum word in the OB register is addressed to the G/A-FD storage section. The search and not-search levels originate in the G/A-FD storage section. The G/A-FD compare level, when up, informs the G/A-FD read-in control that the burst number of the drum word compares with the G/A-FD burst counter. The two levels, search-G/A-FD and not-search-G/A-FD, are up alternately. A positive G/A-FD-search level denotes that search time for the G/A-FD storage section during the current G/A-FD burst period is in progress and data may be read into its array. However, when the not-search level is up, it indicates that readout time for the current G/A-FD burst period is in progress and data cannot be read into the G/A-FD storage array. The polarity of these four levels establishes the basis for acceptance or rejection of data for the G/A-FD storage section and governs the actions of the G/A-FD read-in control. Three groupings of the four levels are:

a. Select-section-1, compare-G/A-FD, and search-G/A-FD levels are up.
b. Either the select-section-1, the compare-G/A-FD, or the search-G/A-FD level is down.
c. Select-section-1, compare-G/A-FD, and not-search-G/A-FD levels are up.

Should the select-section-1, compare-G/A-FD, and search-G/A-FD levels be up simultaneously, it is an indication that the word is acceptable to the G/A-FD storage section, and a select-search-and-compare-G/A-FD level is produced (fig. 2–19). This level is simultaneously applied to GT 1, GT 3, and an inverter, and is sent to the common read-in control. The common read-in control circuit, after receipt of the select-search-compare-G/A-FD level, sends a set-pulse level (OD 2 + 1.2 to OD 4) to the STD's, providing the parity check is OK. Gates 1 and 3 are conditioned and strobed by an OD 4 + 0.4 pulse. At this time, the OD 4 + 0.4 pulse is passed by GT 3 and sent as an enable-G/A-FD-slot pulse to the slot detection circuit. (Refer to 2.4.4.) Simultaneously, GT 1 also passes the OD 4 + 0.4 pulse and sends it as a reset-G/A-FD pulse to the RID flip-flop which conditions one leg at the G/A-FD CCD's. The reset-G/A-FD level in the half-write current generator shifts the data into the G/A-FD storage section.

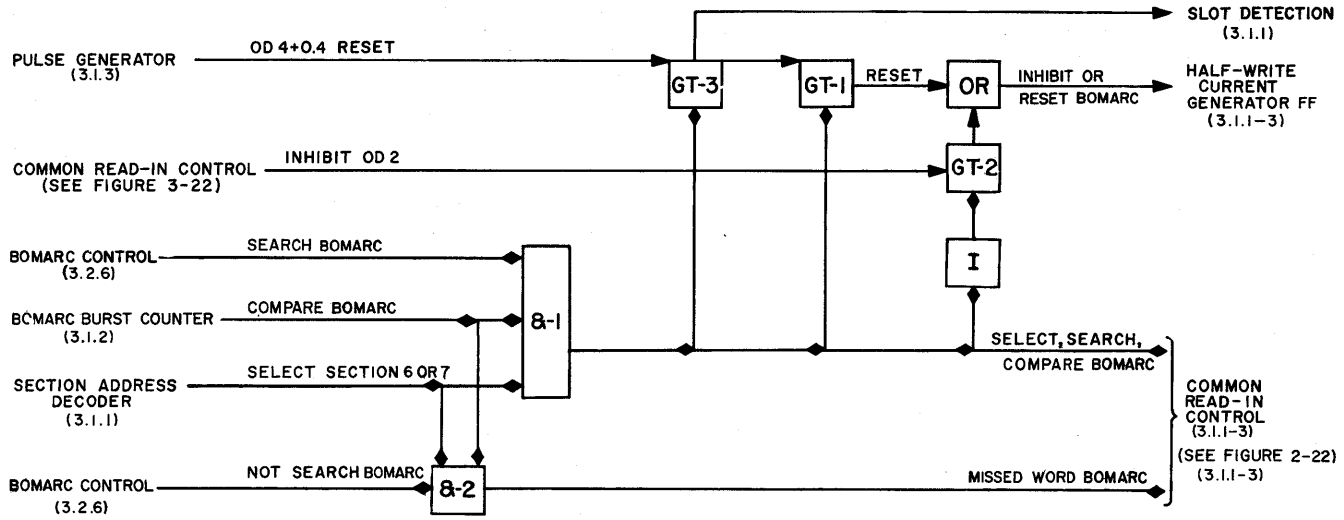
Consider the situation where one of the compare-G/A-FD, search-G/A-FD, or select-section-1 levels applied to AND 1 (fig. 2–19) is down. This indicates that the data in the drum word is not to be sent to the G/A-FD storage section. Such a situation will produce neither a positive select-search-compare-G/A-FD level, nor a reset-G/A-FD pulse, nor an enable-G/A-FD-slot pulse. At this time, the output from AND 1 is down and the output of the inverter is up. Gate 2 is conditioned and passes an inhibit-OD 2 pulse to the RID flip-flop which, in turn, generates an inhibit level. The inhibit-G/A-FD level in the half-write current generator prevents the read-in of the right-half drum word to the G/A-FD storage section.

If the select-section-1, compare-G/A-FD, and not-search-G/A-FD levels are up, a missed word (nonsearch) condition exists. This signifies that the word in the OB register is missing from the G/A-FD burst that is being transmitted during the readout in progress. As shown in figure 2–19, a missed-word level is produced by AND 2 and sent to the common read-in control which produces the nonsearch-alarm pulse and suppresses the generation of a no-compare pulse. The BO1 and BO2 sections read in information in the same manner as the G/A-FD storage section. The G/A-TD and G/G storage sections each employ two storage arrays, designated A and B, respectively. Consequently,

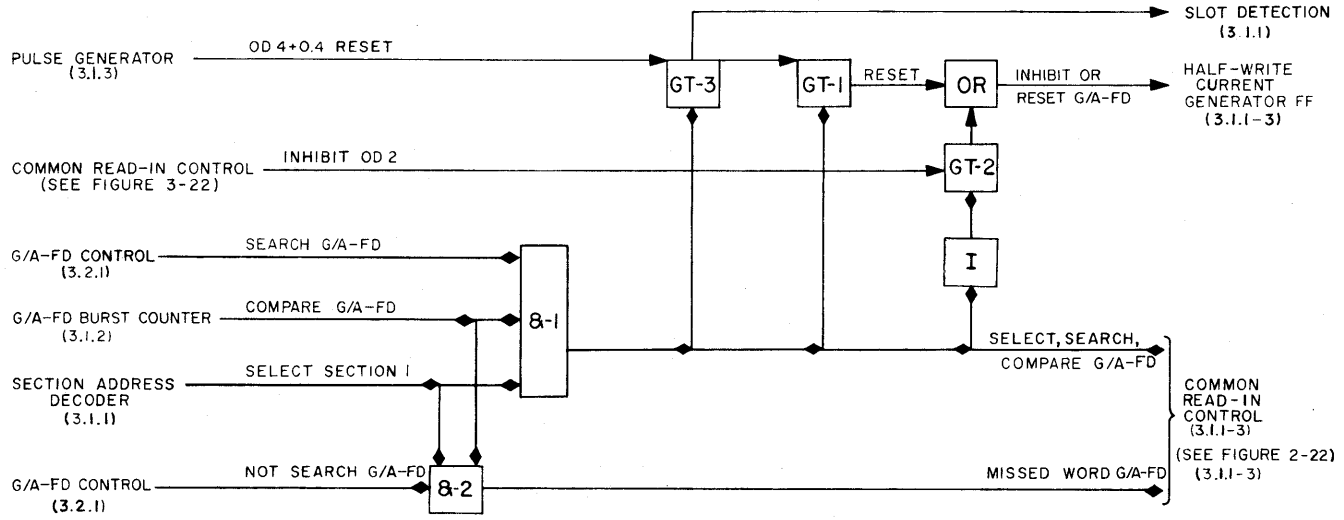
their read-in control circuits differ from the G/A-FD, BO1, and BO2 read-in control circuits in that an additional pair of voltage levels must be considered (fig. 2–20). For the sake of brevity, only the operation of the G/G read-in control circuit is discussed herein.

The levels which originate in the G/G storage section are designated shift-phase A and shift-phase B. The nature of the two levels is such that they do not occur simultaneously; each level, when up, denotes that the contents of its associated array is being read out. Consequently, output words can be written into the other array. Thus, when the select-section-2, search-G/G, and compare-G/G levels are up coincident with the shift-phase B level, a reset-G/G-A pulse is generated in preparation for reading into G/G matrix A.

Another function of the read-in control circuit is the generation of shift pulses which are passed to the completed message shift register in the G/G output storage section. The completed message shift register and the shift pulse are used with the G/G slot level (2.4.4) to count the number of words entered into the G/G storage array. The read-in control circuit is used to generate the required shift pulses. A combination of a parity-OK pulse, and compare, search, and select-



(A)
BOMARC



(B)
GROUND-TO-AIR (FD)

Figure 2–19. G/A-FD and BOMARC Read-In Control Circuits (3.1.1-3), Simplified Logic Diagram

section levels for a G/G word generates a completed-message-shift-register-shift pulse; that is, a shift pulse is produced once for each word entered into a G/G storage array. Hence, coincidence between a shift pulse and a slot level indicates that the slot level is for G/G rather than for the other sections.

The remaining portion of the G/G read-in control is identical with the G/A-FD read-in control. The operation of the TTY read-in control circuit is the same as that of the G/A-FD read-in control circuit and therefore requires no further description (fig. 2–21).

The common read-in control functions when a select-search-compare G/A-FD, BO1, BO2, G/G-A, G/G-B, G/A-TD-A, G/A-TD-B, or TTY level is present (fig. 2–22). One of these levels passes an 8-way OR circuit and is applied to GT 1, GT 2, and the no-compare pulse generator. (Refer to 2.6.3.)

Gates 1 and 2 will conduct when strobed. Gate 2 is strobed by an odd parity pulse at OD 2 + 1.2 time, producing a set pulse which is sent to the STD's. This set pulse causes the STD's to transfer the right half-word, its parity bit, and its register address to the half-write current generator. Similarly, GT 1 is sensed by an OD 2 pulse which is passed and sent to the G/A-FD, BO1, BO2, G/G, G/A-TD, and TTY read-in sections as an inhibit (OD 2) pulse.

Missed-word levels from the six storage section read-in control circuits are sent to a 6-way OR circuit in the common read-in control. Any one of these levels will pass and be supplied as nonsearch levels to both GT 3 and the no-compare pulse generator. A positive nonsearch level indicates a missed word combination which means that the drum word in the OB register would be erased. This is accomplished by suppressing the no-compare pulse and not relaying the data to the storage element. The nonsearch level conditions GT 3 which is strobed by an OD 4 + 0.4 reset pulse from the OB register clear control. The output from GT 3 is a nonsearch pulse that is sent to the alarm control section where it causes a nonsearch alarm to be generated. The overall action of the read-in control circuit can best be described by considering the case of a G/A-FD word. Assume that the select-search- and compare-G/A-FD levels are up; with this condition present, the other

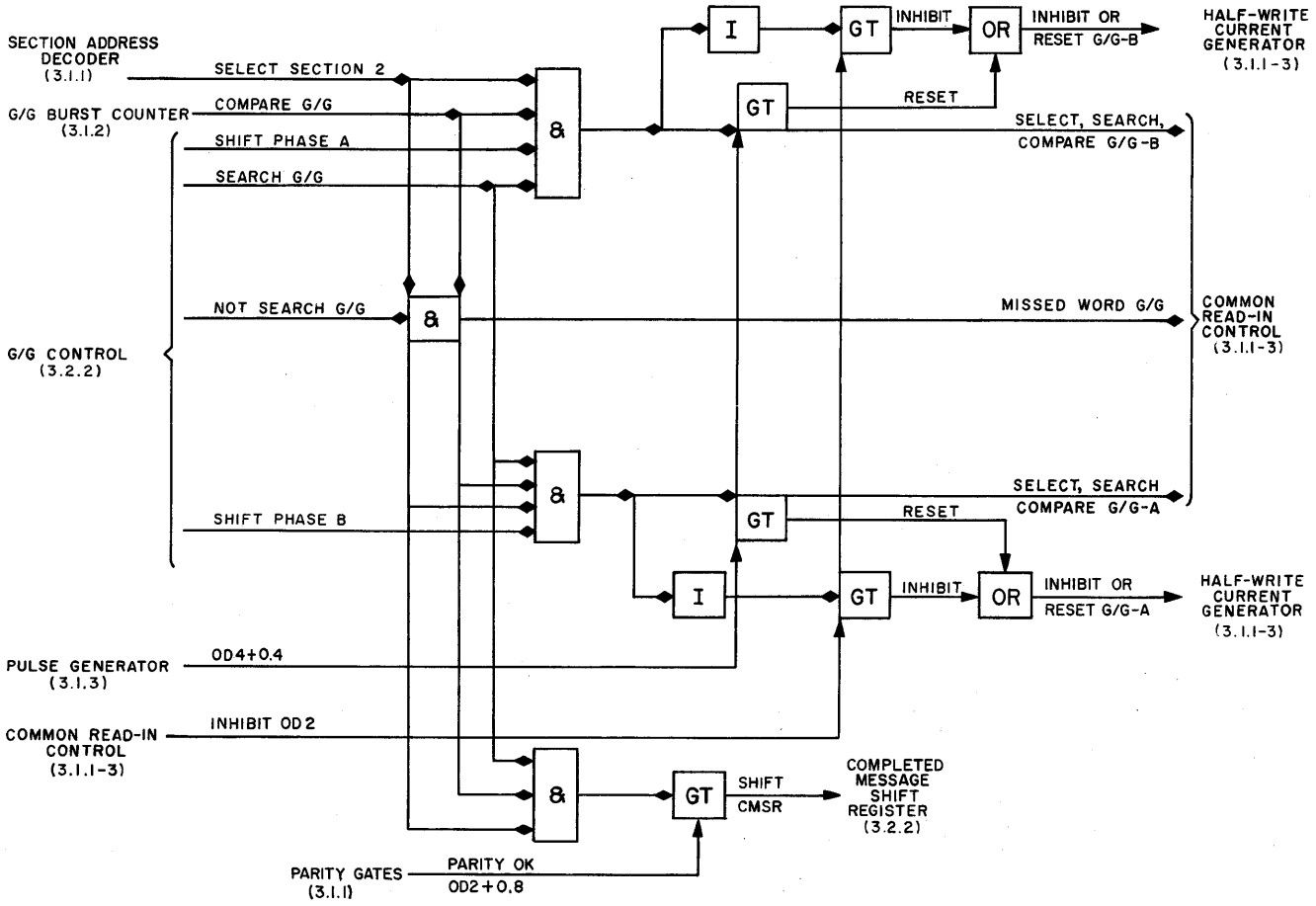


Figure 2–20. G/G Read-In Control (3.1.1-3), Simplified Logic Diagram

sections find the word unacceptable, and, consequently, their select-search-compare levels are down. However, the G/A-FD read-in control finds the word acceptable. As a result of the positive select-search-compare-G/A-FD level, an inhibit (OD 2) pulse is generated by the common read-in control. This pulse, under the existing conditions, prevents the output data from being transferred to the G/G, G/A-TD, BO1, BO2, and TTY storage sections.

The next step of the common read-in control is to pass (1.2 μsec later) a set pulse (OD 2 + 1.2) which will set the set-pulse flip-flop, causing a level of +10V

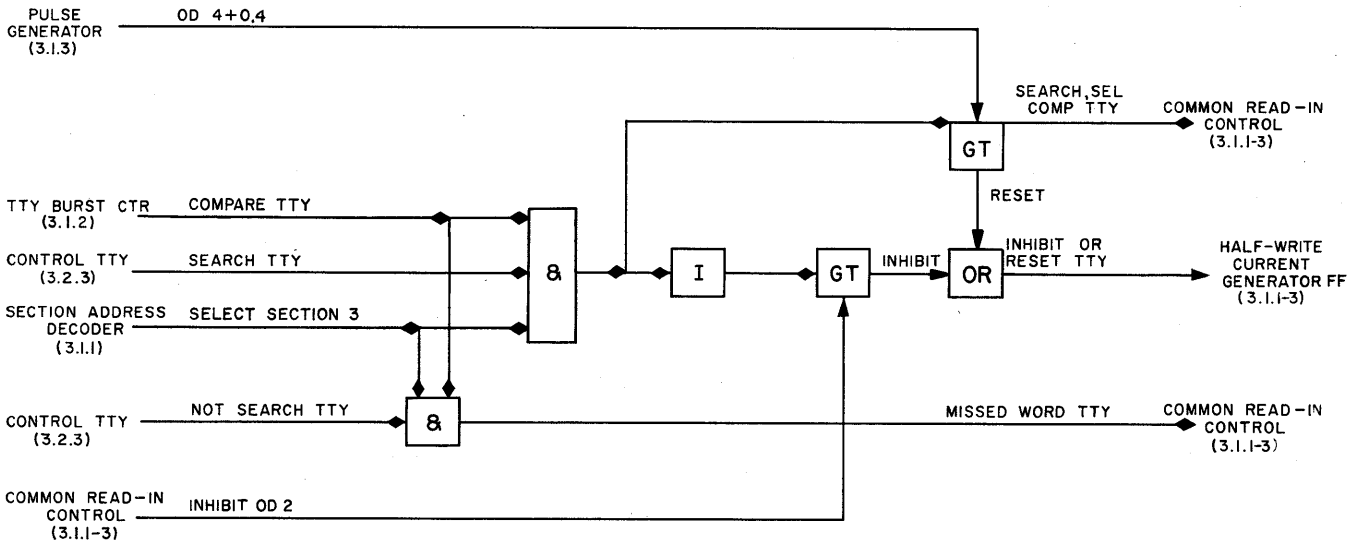


Figure 2–21. TTY Read-In Control (3.1.1-3), Simplified Logic Diagram

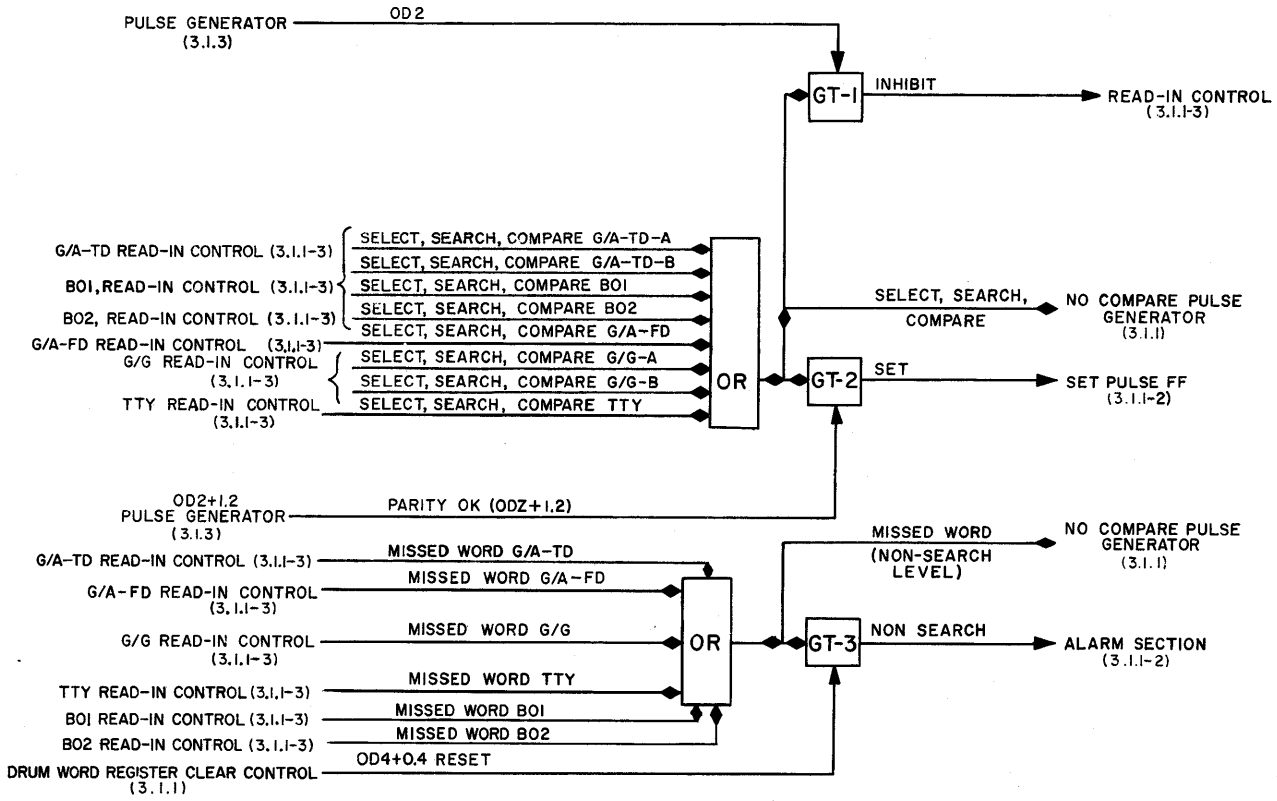


Figure 2–22. Read-In Control Common Equipment (3.1.1-3), Simplified Logic Diagram

to be generated for 3.8 μsec (OD 2 + 1.2 to OD 4). The generated +10V level is applied to the STD's, causing the output data to be transferred from the STD's to the G/A-FD CCD's. The timing is such that the transfer of data from the STD's to the CCD's of the other sections is inhibited by the 3.8-μsec inhibit level. A reset-G/A-FD pulse is generated by the G/A-FD read-in control 4.2 μsec later (OD 4 + 0.4). The reset-G/A-FD pulse causes the transfer of the data from the half-write current generators (CCD's) to the G/A-FD storage array, terminating the read-in.

2.6.3 No-Compare Pulse Generator

When a word is accepted by the Output System, the drum register containing the word is used to store a succeeding word. This has the effect of erasing the first word. However, should the assigned burst number of a word not compare with the burst count at this time, it may be necessary to retain the word on the drum, thereby making it available to the Output System during the next drum cycle. In this manner, a word may be stored until the time it is scheduled to be transmitted; that is, when the assigned burst number does compare with the burst count. When all conditions (with the exception of compare) are favorable for the acceptance of a word, a no-compare pulse is generated and sent back to the drum section. This prevents the word from being erased from the OB drum.

A simplified logic diagram of the no-compare pulse generator is shown in figure 2–23. The signals which affect the generation of the no-compare pulse are as follows:

a. Nonsearch level when burst number compares (missed word)
b. Illegal section
c. Illegal register
d. Search-select-compare
e. Parity-OK

Since the above signals, with the exception of parity-OK, are applied to inverters, the no-compare pulse can be generated only when all these signals are coincidentally absent (assuming correct parity). The presence of any one of these signals automatically inhibits the production of a no-compare pulse.

Gate 2 passes a no-compare pulse only if the following conditions are present:

a. Select-search-compare down (—30V)
b. No missed word
c. Legal address
d. Legal section
e. Parity OK

The select-search-compare level will be down without affecting one of the other listed conditions in only two situations: search and no-compare or nonsearch and no-compare. Either one of these situations will bring the select-search-compare level down, but a no-compare pulse will be generated only if the four remaining listed conditions are met. It should be noted that bringing the select-search-compare level down (—30V) in any other way will result in acquiring either a missed-word or an illegal-section level, either of which prevents the generation of a no-compare pulse. This is summarized in table 2–4.

The previously mentioned signals are functions of four basic variable quantities, assuming that parity is OK; these are compare, select section, select register,

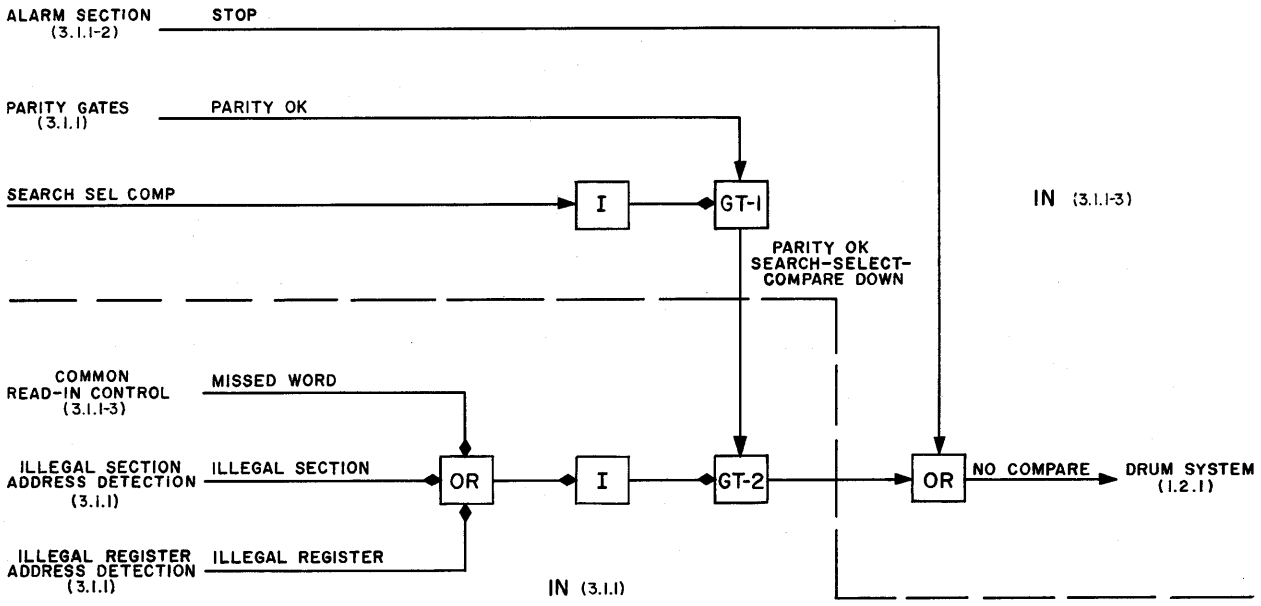


Figure 2–23. No-Compare Pulse Generator (3.1.1-3), Simplified Logic Diagram

and search time. In table 2–4, the 0's indicate the absence and the 1's denote the presence of the quantity shown at the top of each column. The 16 possible combinations of the four basic signals are shown with the resultant effects of those signals used for no-compare pulse generation. It should be noted that the missed-word signal occurs when select section and compare occur during nonsearch time. The results show that no-compare is generated when the assigned burst number does not compare with the burst count, providing that the section and register addresses are legal and parity is OK (table 2–1). The significance of these results may be summarized as follows:

a. First, it is desired to retain a word on the OB drum when it appears before its predetermined time of transmission. This is accomplished by returning a no-compare pulse to the Drum System when the assigned burst number does not compare with the burst count.

b. Second, it is not desired to retain a word associated with incorrect parity, illegal register, or illegal section address. Consequently, a no-compare pulse is generated only when parity is correct and the section and register addresses are valid.

c. Third, the generation of a no-compare signal is not restricted to a word occurring during search time. Thus, a word that does not compare and occurs during nonsearch time (being favorable for acceptance in other respects) can be made available for transmission when it does compare (i.e., at a later time).

Referring again to the no-compare generator, it will be noted that aside from the above considerations the no-compare signal is also generated upon the appearance of a stop pulse from the alarm section. (See fig. 2–23.) The stop pulse is generated when either parity-NG, illegal-section, or illegal-register signals exist. This enables an incorrect word to be retained on the drum for further examination.

2.6.4 Set Drivers

A set driver (STD) is basically a coincidence type circuit which produces a current that is capable of changing the state of a core from 0 to 1. Functionally,

TABLE 2–4. TABULAR SUMMARY, NO-COMPARE PULSE GENERATOR (A 0 INDICATES ABSENCE; A 1 INDICATES PRESENCE)

COMPARE	SELECT SECTION	SELECT REGISTER	SEARCH	MISSED WORD	ILLEGAL SECTION	ILLEGAL REGISTER	SEARCH SELECT COMPARE	NO-COMPARE
0	0	0	0	0	1	1	0	0
0	0	0	1	0	1	1	0	0
0	0	1	0	0	1	0	0	0
0	0	1	1	0	1	0	0	0
0	1	0	0	0	0	1	0	0
0	1	0	1	0	0	1	0	0
0	1	1	0	0	0	0	0	1
0	1	1	1	0	0	0	0	1
1	0	0	0	0	1	1	0	0
1	0	0	1	0	1	1	0	0
1	0	1	0	0	1	0	0	0
1	0	1	1	0	1	0	0	0
1	1	0	0	1	0	1	0	0
1	1	0	1	0	0	1	1	0
1	1	1	0	1	0	0	0	0
1	1	1	1	0	0	0	1	0

the STD circuit, shown in figure 2–24, delivers signals to the half-write current generator for each address, for busy bits, whenever a 1 appears in the right drum word and when an output parity bit is included. These outputs are produced only when these 1's appear at the same time as a set pulse from the read-in control circuit. (See fig. 2–22.) It will be recalled that the set signal is generated by a word accepted by one of the six storage sections. Therefore, the STD circuit serves as common equipment for all words accepted by the Output System. The actual selection of a storage section occurs in the half-write current generator circuit. It should be noted that only those words which prove acceptable for transmission cause the STD's to send the appropriate signals to the half-write current generator.

There is provision in the STD's for generating two 1 bits, referred to as busy bits, whenever data is transferred from the STD's to the half-write current generator. The generation of these busy bits is made possible by the connection of two STD's to a +10V source. Thus, whenever a set pulse is applied to the STD's, the two busy bits are produced and transferred, together with the other data, to the half-write current generator. These busy bits are required by the G/A-FD, BO1, BO2, and TTY storage sections; their functions are described in the discussions of these storage sections (Ch 2 and 4 of Part 3).

Provisions are made for register addresses 0 through 25, representing the maximum number of registers used in any one output storage section. However, for a given word, only one register address level is present. Thus, the information sent to the half-write current generator consists of signals denoting a register address, the right drum word, output parity, and busy bits. The manner in which this information is employed by the half-write current generator is discussed below.

2.6.5 Half-Write Current Generator

The half-write current generator circuit produces currents which are capable of changing the state of ferrite cores from the signals delivered to it by the STD's and the read-in control circuit. These currents are utilized by a ferrite core storage matrix in the output storage section to cause storage of a word in the matrix. The manner in which the half-write currents are combined to effect storage is covered in paragraph 2.3 of Chapter 2, Part 3.

2.6.5.1 Flip-Flops and Reset-Inhibit Drivers

The current generator is discussed from the standpoint of the current generator flip-flops, shown in figure 2–25, and the current generator matrix, shown in figure 2–26. It is the function of the flip-flops to deliver the required inputs to the reset-inhibit drivers (RID) which, in turn, deliver currents required by the current generator matrix. Functionally, an RID is capable of producing a current which will either reset or inhibit a change of state in the cores when applied to tape core windings. The cores are wound in a manner which causes a reset signal to reset the cores to the 0

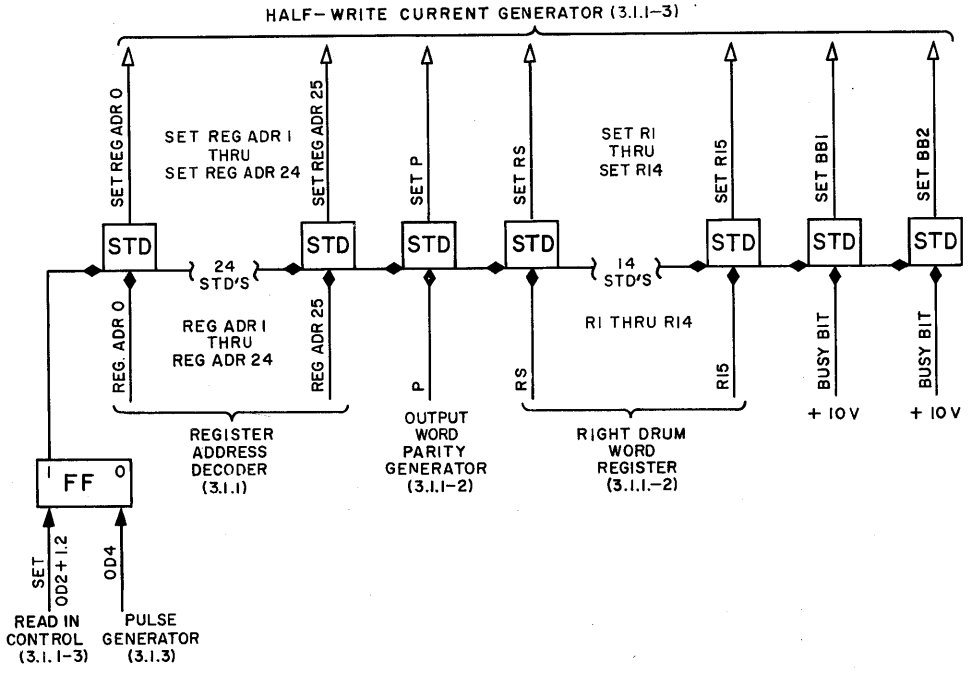


Figure 2–24. Set Drivers (3.1.1-2), Simplified Logic Diagram

state or an inhibit signal to prevent a core from being changed from 0 to 1. It is important to note that an RID produces an output voltage only from a negative voltage input. Referring to figure 2–25, initially, all the flip-flops which control the RID's have been cleared and the 0 sides are up. Under this condition, there is no current out of the RID's, and the half-write current generator cores (fig. 2–26) which are connected to the RID's can then have 1's set into them by the STD's. However, when an inhibit pulse is sent to a flip-flop, the 0 side is brought down to —30V. The corresponding RID then passes either an inhibit signal or a reset signal to the related cores in the half-write current generator. These two signals are identical in magnitude but differ in timing and function. An inhibit pulse is sent at the beginning of a read-in operation and prevents a 1 from being set into a core by the STD. A reset pulse is sent after the information is set into the cores and drives the cores which have been set to 1 back to 0. This causes the 1's to be read out of the cores and into the appropriate ferrite cores in the appropriate output storage array.

2.6.5.2 Core Current Drivers

The half-write current generator matrix consists of 48 vertical columns and 12 horizontal rows of tape core current drivers (CCD's). Each of the 576 CCD's is capable of delivering a current of half the amplitude required to cause a change of state in a corresponding ferrite core in the output storage element. At present, only eight of the 12 rows are in use, one each for G/A-FD, BO1, BO2, G/G-A, G/G-B, G/A-TD-A, G/A-TD-B, and TTY.

The lines which pulse the horizontal rows feed the signals in from the RID's. Similarly, the lines pulsing

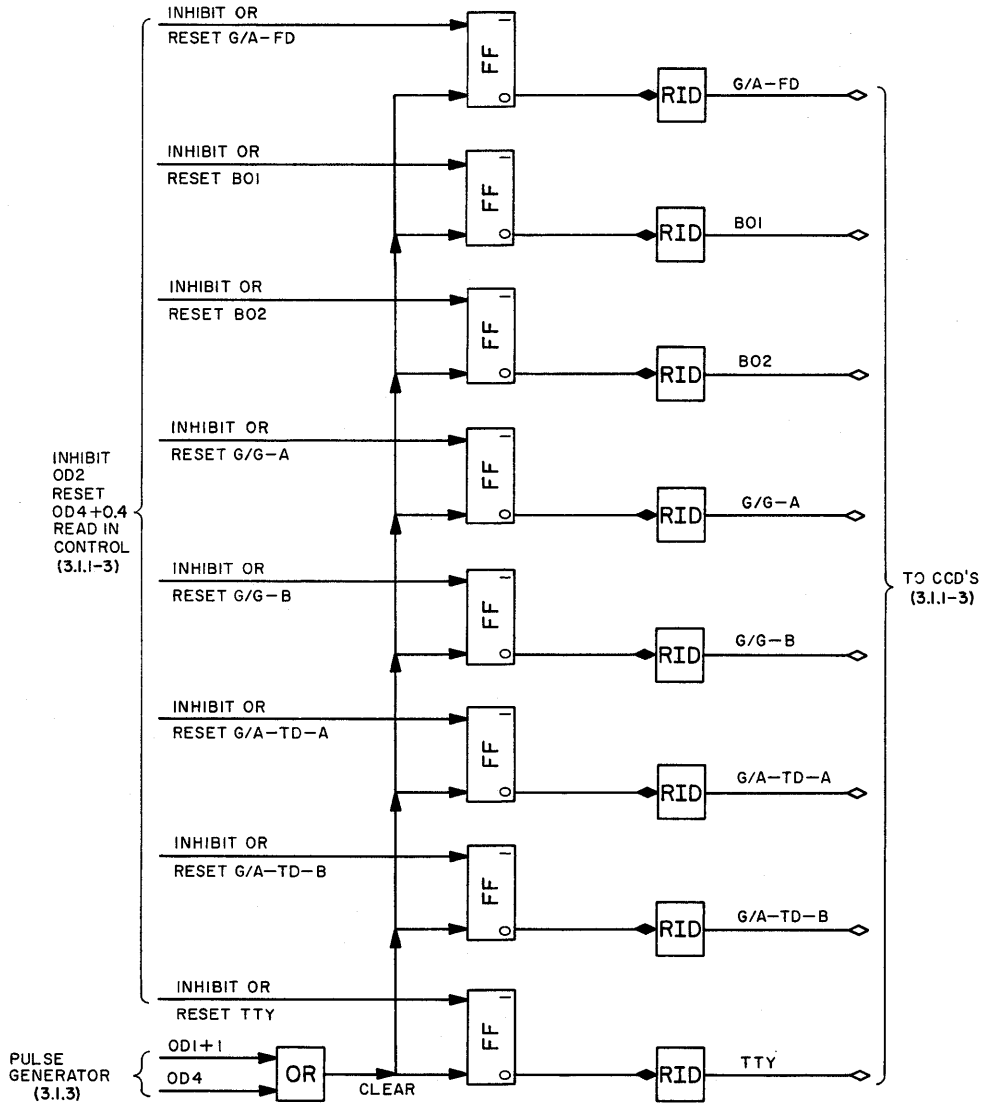


Figure 2–25. Half-Write Current Generator Flip-Flops (3.1.1-3)

the vertical column bring in the bits of the right drum word, the associated register address of that word, the output parity bit, and the busy bits from the STD's.

Initially, all the cores in the CCD's are in the 0 state. During the time that the vertical columns are pulsed, the horizontal row of cores corresponding to the section associated with the word being read into the CCD's is not pulsed. Those cores associated with sections not selected are pulsed by inhibit signals. In this manner, the cores corresponding to the selected section change state in accordance with the information being read in, whereas the other cores are prevented from changing state. That is, only in the selected section cores do 1 bits cause a change of state from 0 to 1; the 0 bits have no effect. Some time later, a reset signal is applied to all of the cores. This causes the cores containing the temporarily stored information to revert to the 0 state and, in the process of changing state, the information is transferred out as half-write currents. For the sake of clarity, the lines leading to the output storage element from each CCD are not shown in figure 2–26.

2.6.5.3 Timing Cycle

To illustrate how the half-write current generator functions, consider the case for a G/A-FD word. The timing sequence for this condition is shown in figure 2–27. The drum word, after being taken off the OB drum, is placed in the drum word register. The contents of the right drum word register are then made available to the STD's during the interval between OD 1 and OD 4 + 0.4. The STD's pass their information along to the CCD's of the half-write current generator between OD 2 + 1.2 and OD 4. (See figs. 2–24 and 2–27.) (This assumes that all conditions are favorable for accepting the word.) Since the section selected is G/A-FD, the read-in control circuit delivers inhibit signals to the half-write current generator flip-flops associated with the other seven arrays. Since an inhibit pulse is not delivered to the G/A-FD flip-flop, the 0 side of this flip-flop is up. Therefore, there is no current from the RID

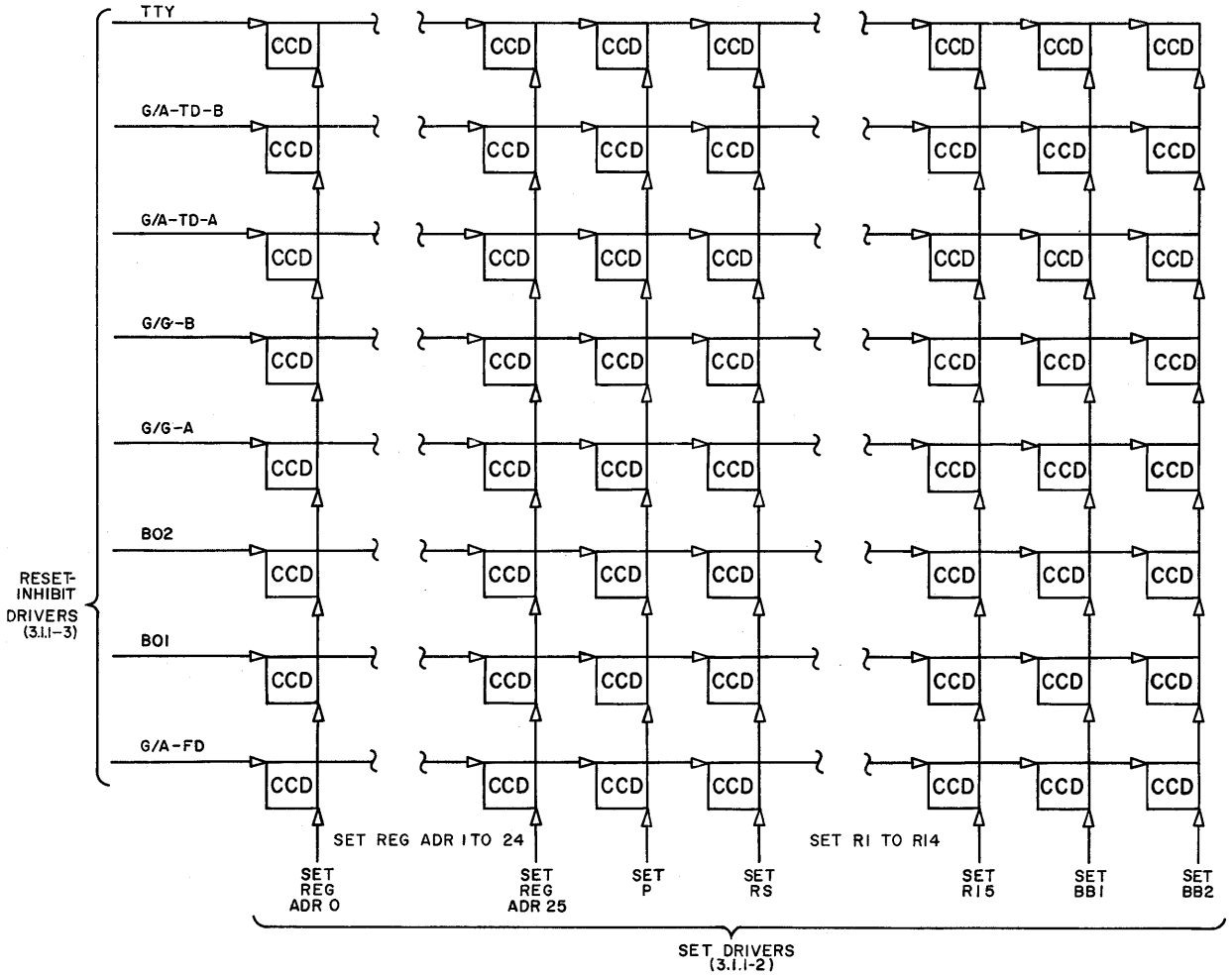


Figure 2–26. Half-Write Current Generator Matrix (3.1.1-3), Simplified Logic Diagram

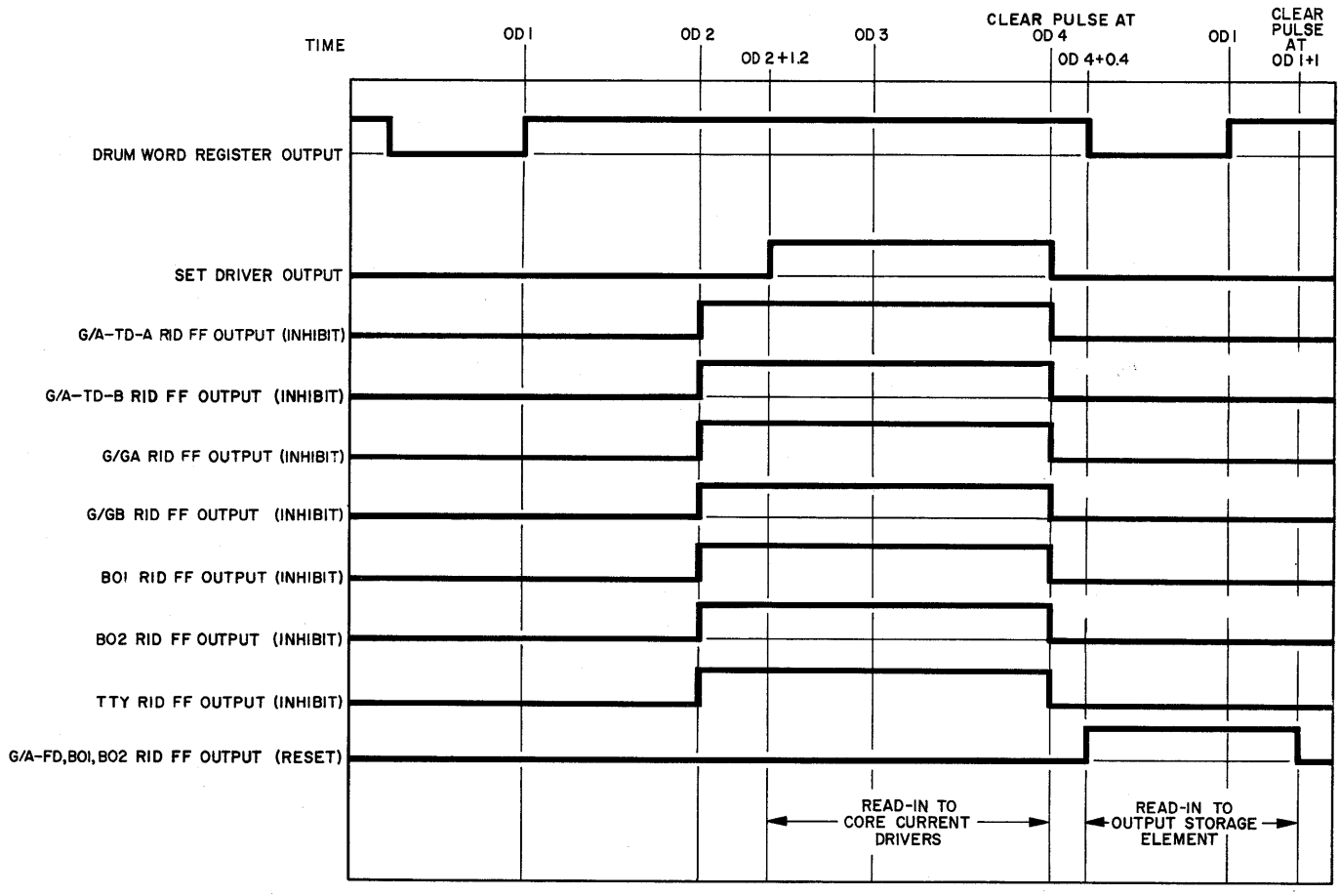


Figure 2–27. Half-Write Current Generator Timing for G/A-FD Word, Functional Representation

associated with this flip-flop. On the other hand, the other RID's deliver inhibit currents to the CCD's associated with BO1, BO2, G/G-A, G/G-B, G/A-TD-A, G/ATD-B, and TTY, from OD 2, to OD 4, at which time the RID flip-flops are cleared. (See fig. 2–25.) Actually, only the RID's which were inhibited change back to the 0 side up, since the uninhibited RID (G/A-FD, in this example) was not originally changed from this condition. The inhibit level is up for an interval that is concurrent with and slightly longer than the STD outputs representing the right drum word, the associated register address, and the busy bits. This assures complete inhibiting. Because of the inhibiting action, no information is placed in the CCD's corresponding to the sections not selected.

During the interval discussed above, the G/A-FD CCD's are free to receive the right drum word, the corresponding register address, the output parity bit, and the busy bits. Referring again to the timing chart, it can be seen that the G/A-FD RID flip-flop output is up from OD 4 + 0.4 to OD 1 + 1 and represents a reset signal. (See figs. 2–18, 2–25, and 2–27.) No other information is being fed into the CCD's during this interval. The G/A-FD reset signal clears the G/A-FD CCD's to the 0 state, causing the temporarily stored data to be read into the GA-FD storage matrix in the output storage element. The CCD's are then all in the 0 state, prepared for the receipt of another word. It should be noted that the OD pulse times mentioned in this discussion are approximate, since considerations such as cable delays and rise and fall times of the circuits were not taken into account.

All the RID flip-flops are cleared at OD 1 + 1, as shown in figure 2–25. This action sets the 0 side of the reset RID flip-flop up, the RID flip-flops which were inhibited having been cleared at OD 4.

6. Single channel sync control FF in 33DF (logic 3. 2. 5, coord. 5A)
In single channel mode, this circuit is used in conjunction with the SYNC GEN in 33EH to control sync and dummy sync generation and to sequence the auto parity bits to the phone lines at their proper times.

SUMMARY

It is requested that this letter be circulated to the personnel responsible for outputs maintenance for their review. The time spent in familiarization with the new logic will result in improved system check-out and troubleshooting procedures after E. C. R-74325 is installed.

CHAPTER 3
OUTPUT COMPUTER SECTION

3.1 GENERAL

The Central Computer System must have access to the burst counts and the elapsed-time count of current burst periods. The burst counts are contained in periodically stepped burst counters in the output control element and represent the burst numbers of current burst periods. Similarly, the elapsed-time count is produced by the elapsed-time counter for the GA-FD, BO1, and BO2 storage sections. As the name implies, it represents the time that has elapsed since the start of search time of an associated G/A-FD burst. It should be noted that elapsed time is a function of G/A-FD, BO1, and BO2 messages only. This is because the required accuracy of these time-to-go messages is much greater than the accuracy required of G/G, G/A-TD, or TTY messages. Hence, since these latter three sections do not require a very accurate measurement of the time that has elapsed in a burst period, they do not require elapsed-time counters.

The transfer of the burst and elapsed-time counts to the Central Computer System is accomplished in the output computer section of the output control element upon request by the Central Computer System. In addition, the output computer section generates various timing pulses used for controlling numerous operations throughout the Output System.

3.2 BURST-COUNT SELECTION AND TRANSFER

3.2.1 General

The selection of burst counts and elapsed-time counts and their transfer to the Central Computer System is the function of the output computer section. The contents of each of the four burst counters and the elapsed-time counter are made available to the Central Computer System through the sections of the burst-count selecting counter, the selecting counter decoder, and the burst-time count switch. (See fig. 2–28.)

3.2.2 Burst-Count Selecting Counter

This circuit controls the read cycle of the burst-time count. During this cycle, the current contents of each burst counter and the G/A-FD elapsed-time counter are transferred to the Central Computer System. A burst-time count read cycle is initiated upon receipt of a select-and-read pulse from the Central Computer System. The burst-count selecting counter is then stepped at the rate of 100,000 pps (every 10 μsec), causing successive 3-bit binary codes to be generated. Each code selects a different burst counter and causes the transfer of the burst counter contents to the Central Computer System. The elapsed-time count is transferred with the G/A-FD burst count. After five codes have been produced, the contents of the four burst counters and elapsed-time counter are in the Central Computer System (code 011 is unassigned). The burst-time selecting counter then receives a disconnect pulse from the Central Computer System, terminating the burst-time count read cycle.

The selecting counter control generates the stepping and clear pulses used by the selecting counter. A burst-time count read cycle is begun with the reception of a select-and-read pulse from the Central Computer System. As shown in figure 2–29, the select-and-read pulse sets FF 1. This starts the following sequence of operations: the 1 side of FF 1 conditions GT 2, passing an OD 3, which sets FF 2; GT 4 is conditioned and passes the next OD 1 pulse; each successive OD 1 pulse is gated through GT 4 as long as FF 2 remains set; these OD 1 pulses are sent to the selecting counter as stepping pulses.

If (fig. 2–29) either a disconnect signal or selecting-counter-equals-eight pulse is applied to the OR circuit, FF 1 is cleared. Gate 1 is conditioned and the next OD 3 pulse is passed, clearing FF 2. The 0 side of FF 2 conditions GT 3 and the succeeding OD 1 pulse is gated through. All OD 1 pulses passed through GT 3 are sent to the selecting counter as clear pulses.

The selecting counter generates the binary codes which select the burst counts to be transferred to the Central Computer System. This circuit is a scale-of-eight counter composed of three flip-flops. (See fig. 2–30.)

As each burst-count read cycle begins, the counter is clear; i.e., the binary output is 000. The first stepping pulse applied to the counter produces an output binary code of 001. A second stepping pulse changes this to

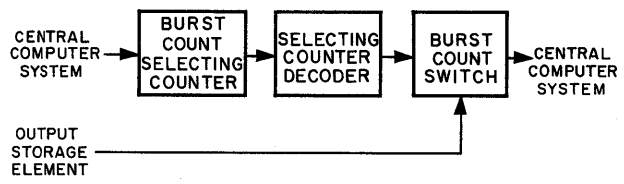


Figure 2–28. Burst Count Selection and Transfer, Block Diagram

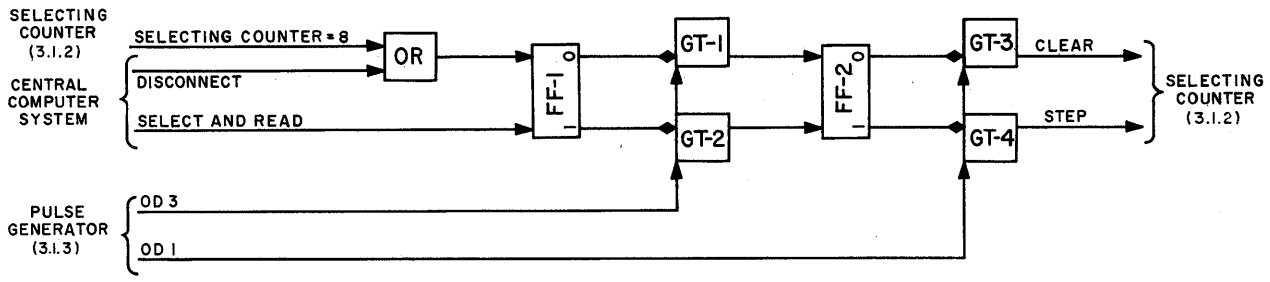


Figure 2–29. Selecting Counter Control (3.1.2), Simplified Logic Diagram

010. The third stepping pulse causes the counter to generate a binary combination of 011. This counting process continues until the binary output is 111 or, in other words, the counter is equal to eight. The counter-equals-eight pulse is sent to the selecting counter control, thus causing the counter to be cleared. However, if a disconnect pulse is received by the selecting counter control prior to the action of the counter-equals-eight pulse, the counter is cleared at that time.

Although the burst-count selecting counter is a scale-of-eight, its scale is controlled by the Central Computer System through the action of the disconnect pulse. The burst-count selecting counter is a scale-of-eight to produce a binary output for each of the eight possible storage sections. Since only six storage sections are employed, which utilize only four burst time counters, it would be a waste of time to allow the selecting counter to count to its maximum limit. The Central Computer System is programmed for the number of burst-time counters that are employed in the Output System. The program determines the number of burst counts that can be received during a burst-time count read cycle. The Central Computer System then generates a disconnect pulse after receiving the number of burst-time counts desired, which may be one or more. For example, there are six storage sections in the output storage element. However, only four burst counters are utilized since one burst-time counter is shared between the G/A-FD, BO1, and BO2 storage sections. After four stepping pulses from the selecting counter control, the burst-count selecting counter is equal to four, and the burst count from each of the four burst counters has been sent to the Central Computer System. The four stepping pulses have been sent to the Central Computer System as break-request pulses (fig. 2–30). These pulses prepare the Central Computer System for the reception of each burst count and they step a counter in the Central Computer System for each burst number transferred. When the counter in the Central Computer System counts the number of burst counts desired, it generates a disconnect pulse upon reception of the third break-request pulse. The disconnect pulse causes the burst-count selecting counter to be cleared, thus ending a burst-time count read cycle.

The select-and-read OD 1 pulses (fig. 2–30), which are coincident in time with the stepping and break-request pulses, are fed to the burst-time count switch to cause the transfer of the burst-time and elapsed-time counts.

3.2.3 Selecting Counter Decoder

The selecting counter decoder receives the 3-bit binary combination from the burst-count selecting counter. For each binary code, a signal to select a particular

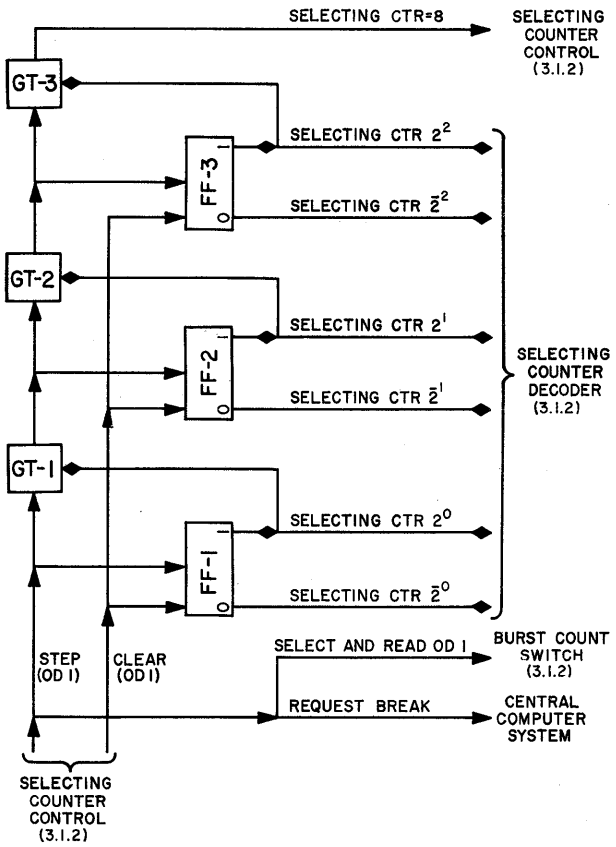


Figure 2–30. Selecting Counter (3.1.2), Simplified Logic Diagram

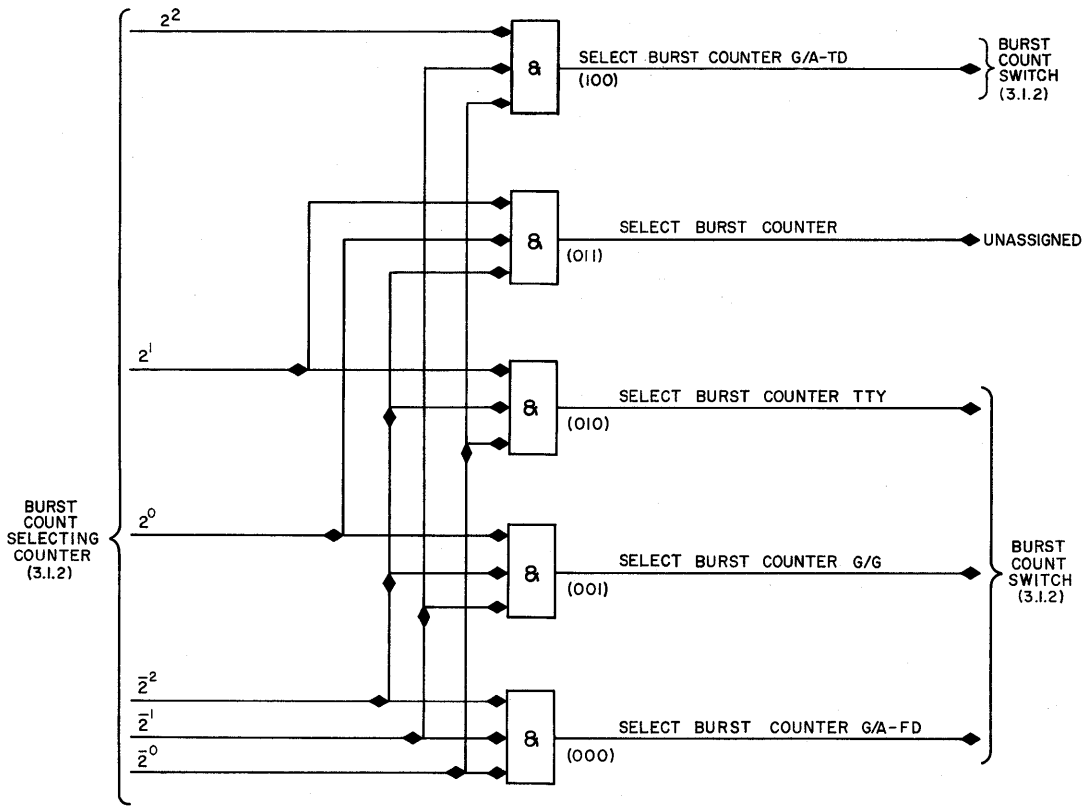


Figure 2–31. Selecting Counter Decoder (3.1.2), Simplified Logic Diagram

burst counter is produced and sent to the burst-time count switch.

As shown in figure 2–31, the selecting counter decoder is composed of five 3-way AND circuits. The three inputs to each AND circuit constitute a different 3-bit binary code. Therefore, for each binary code received, an output level is produced by one of the five AND circuits. However, only four levels are presently used. They are select-G/A-FD, select-G/A-TD, select-G/G, and select-TTY.

The first binary combination received by the decoder is 000 which causes AND circuit 1 to produce a select-G/A-FD burst-counter level. This is followed 10 μsec later (time OD 1) by binary combination 001 that causes a select-G/G-burst-counter level to be produced by AND circuit 2. The third binary code that is received during each burst-count read cycle is 010. At the time of reception of this binary code, AND circuit 3 generates a select-TTY-burst-counter level. The fourth binary code that is received during the burst-count read cycle is 011. This causes AND circuit 4 to generate a level; however, this level has no application and is considered only for reasons of representing a count of the selecting counter. The final binary code that is received during each burst-count read cycle is 100. At the time of reception of this binary code, AND circuit 5 generates a select G/A-TD-burst-counter level.

3.2.4 Burst-Time Count Switch

The burst-time count switch contains the current count of each burst counter and the elapsed-time counter. It furnishes, through the burst-count readout process, the current contents of each burst counter and the elapsed-time counter to the Central Computer System. For purposes of discussion, the burst-count switch is divided into two parts, the burst selector and the computer gates. The burst selector is that part of the burst selector switch which is connected directly to the burst counters and elapsed-time counter. The burst selector is subdivided into four parts: the G/A-FD burst selector, the G/G burst selector, the G/A-TD burst selector, and the TTY burst selector. Each burst selector consists of a row of 2-way AND circuits. (See figs. 2–32 and 2–33.)

The G/A-FD burst selector section contains an additional row of four 2-way AND circuits to accommodate the elapsed-time count (fig. 2–32).

The first burst counter selected during a burst-count read cycle is the G/A-FD burst counter. The contents of the G/A-FD-burst-counter level is applied to the AND circuits. The G/A-FD burst count and the elapsed-time count are then fed to the computer gate.

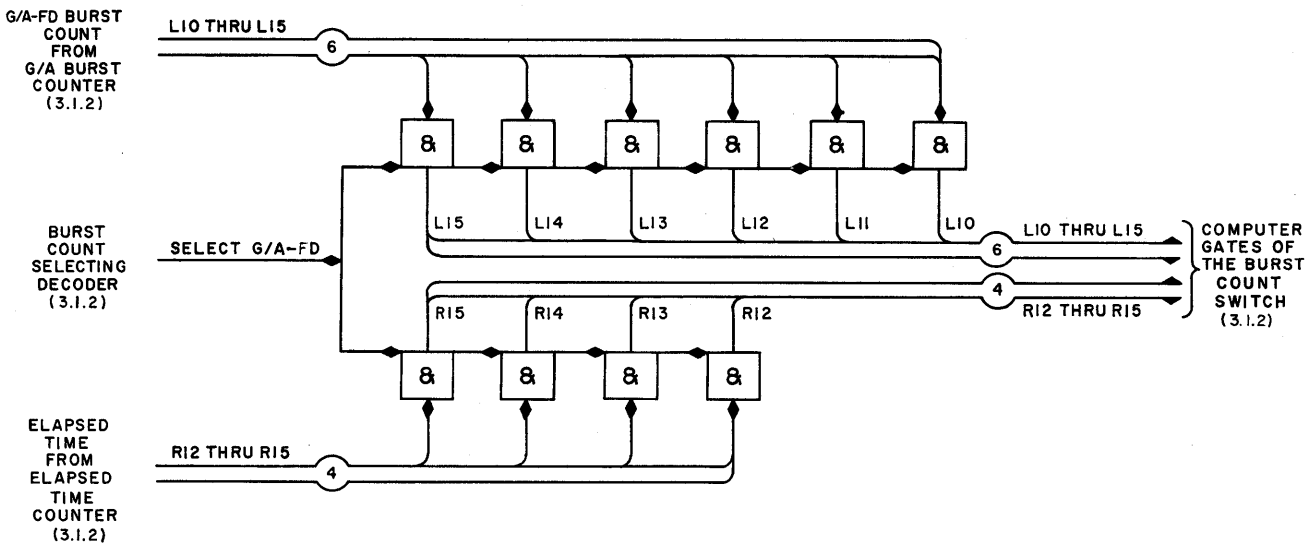


Figure 2–32. G/A-FD Burst Selector of the Burst-Time Count Switch (3.1.2), Simplified Logic Diagram

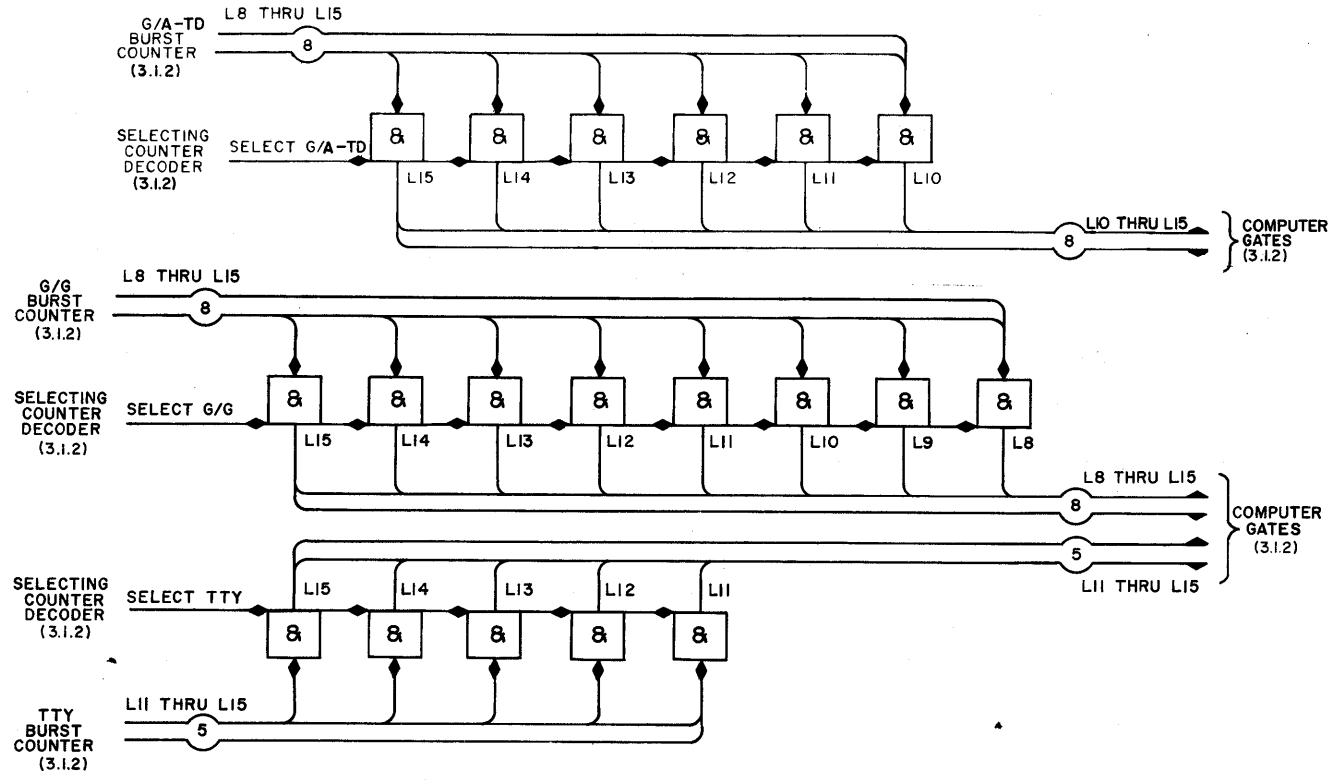


Figure 2–33. G/A-TD, G/G, and TTY Burst Selectors of the Burst-Time Count Switch

The G/G burst counter, the TTY burst counter, and the G/A-TD burst counters are selected after the G/A-FD burst counter. Their burst counts are also sent to the computer gates as they are selected. The computer gates transfer the burst counts and the elapsed-time count to the Central Computer System.

As shown in figure 2–34, the bits fed from the burst selector are applied to a number of OR circuits. Each OR circuit is fed a corresponding bit from each burst counter. Since the burst counters are selected individually, only one of four lines applied to any OR circuit is up at any one time. The bits of the selected

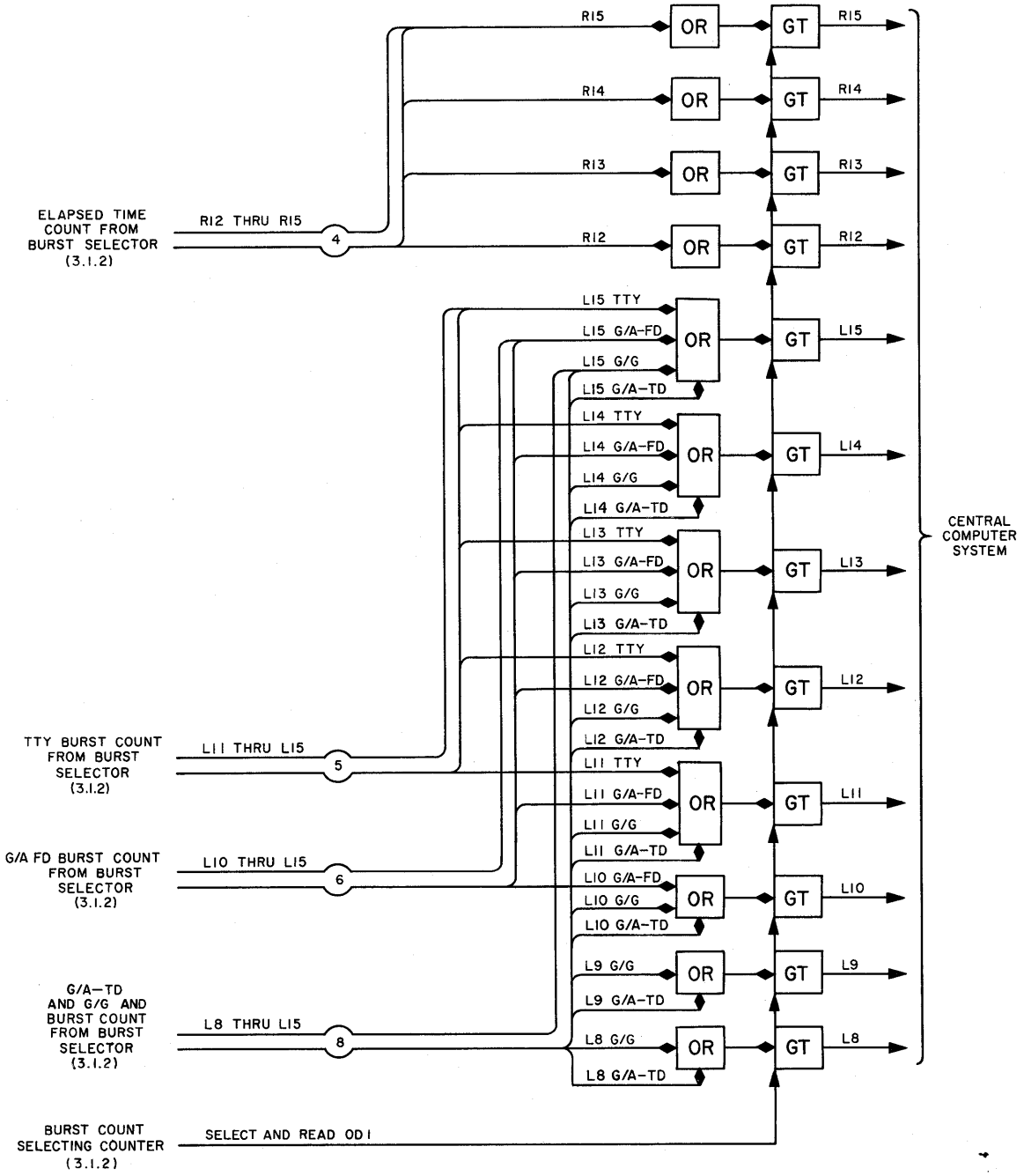


Figure 2–34. Computer Gates of the Burst-Time Count Switch (3.1.1-3), Simplified Logic Diagram

burst counter are passed through the OR circuits to condition their associated gates.

The pulse which gates the burst counts through to the Central Computer System is the select-and-read-OD 1 pulse. It is coincident with both the stepping pulse utilized by the burst-count selecting counter and the break-request pulse sent to the Central Computer System. Each time that this select-and-read-OD 1 pulse is generated, a different burst count is transferred to the Central Computer System.

To summarize the selection and transfer process, a complete burst-count read cycle is discussed below. During the discussion, refer to figures 2–29 and 2–35.

Each burst-count read cycle is begun with the reception of a select-and-read pulse from the Central Computer System. However, prior to the reception of this pulse, the three units employed in the selection and transfer of the burst counts are in the following statuses: (1) The burst-count selecting counter is clear; its binary output is 000. (2) This binary code is ap-

plied to the selecting counter decoder which produces a select-G/A-FD burst-counter signal. As this signal is applied to the G/A-FD burst selector section within the burst-time count switch, the G/A-FD burst count and the elapsed-time count are fed to the computer gates which are also within the burst-time count switch.

When the burst-count selecting counter receives a select-and-read signal from the Central Computer System, it feeds successive OD 1 pulses to the selecting counter as stepping pulses, to the Central Computer System as break-request signals, and to the computer gates as select-and-read-OD 1 signals.

The first OD 1 pulse initiates three operations which occur simultaneously. It steps the burst-count selecting counter, thus changing the binary output of the burst-count selecting counter to 001. Coincident with this, the Central Computer System receives a break-request pulse that prepares it for the reception of a burst count and also records the fact that one burst count is read. Simultaneously with these two operations, the first OD 1 pulse, labeled select-and-read-OD 1, transfers the G/A-FD burst count and the elapsed-time count to the Central Computer System.

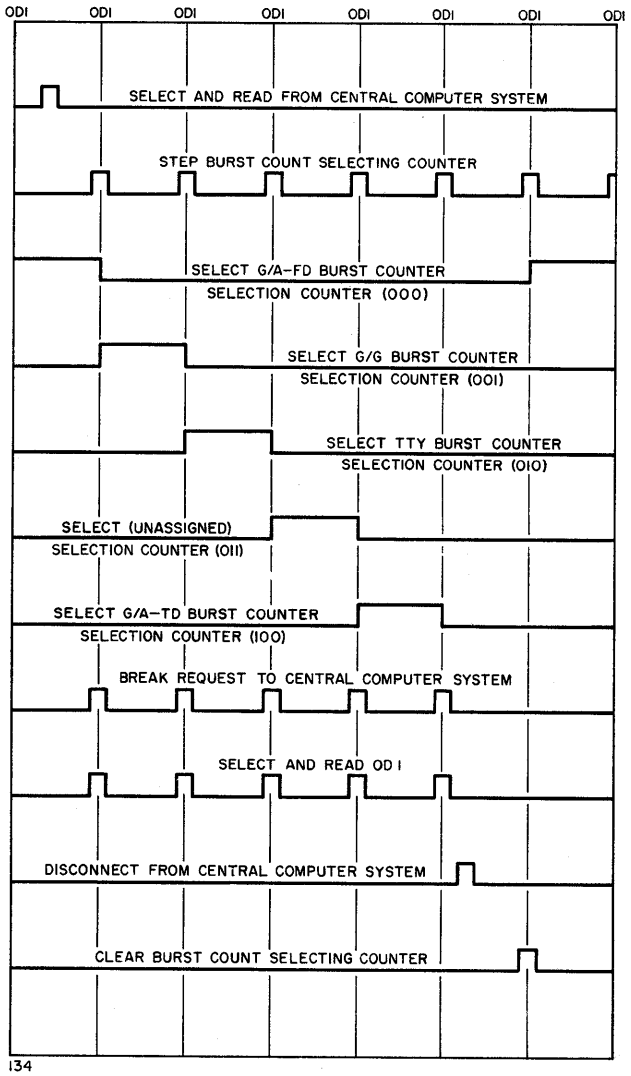


Figure 2–35. Burst Counter Read Cycle, Timing Chart (Functional Representation)

The binary code 001, which was produced as a result of the selecting counter being stepped by the first OD 1 pulse, then causes the select-G/G burst counter line to be up. This signal is applied to the G/G burst counter selector section, and the G/G burst count is fed to the computer gates.

The second OD 1 pulse, which occurs 10 μsec after the first pulse, steps the selecting counter to 010, is sent to the Central Computer System as a break-request pulse, and gates the G/G burst count to the Central Computer System. The stepping of the selecting counter results in the selection of the TTY burst counter. When the third OD 1 pulse appears, it steps the selecting counter to 011, is sent to the Central Computer System as a break-request pulse, and transfers the TTY burst count to the Central Computer System.

The fourth OD 1 pulse, which occurs 10 μsec after the third pulse, steps the selecting counter to 100 and is sent to the Central Computer System as a break-request pulse. However, no transfer of this particular count is made to the Central Computer because, as stated in paragraph 3.2.3, this count has no application.

The fifth OD 1 pulse occurs which steps the selecting counter to 101; it is sent to the Central Computer System as a break-request pulse and transfers the G/A-TD burst count to the Central Computer System.

The fifth break-request pulse also informs the Central Computer System that four burst counts have been read. The Central Computer System then generates a disconnect signal. This disconnect pulse results in the clearing of the burst-count selecting counter, thus terminating the burst-time count read cycle.

3.3 PULSE GENERATOR AND PULSE GENERATOR CONVERSION UNIT

3.3.1 General

The pulse generator and pulse generator conversion unit produce some and distribute all timing pulses used in the Output System (fig. 2–36). The pulse generator consists of several individual circuits which control and distribute all the pulses used in the Output System. It also contains the circuit which generates the 91-pps pulses. The pulse generator conversion unit is a circuit which generates 1,300-pps pulses. These pulses are fed to the pulse generator for distribution and control. Each of the circuits is described below.

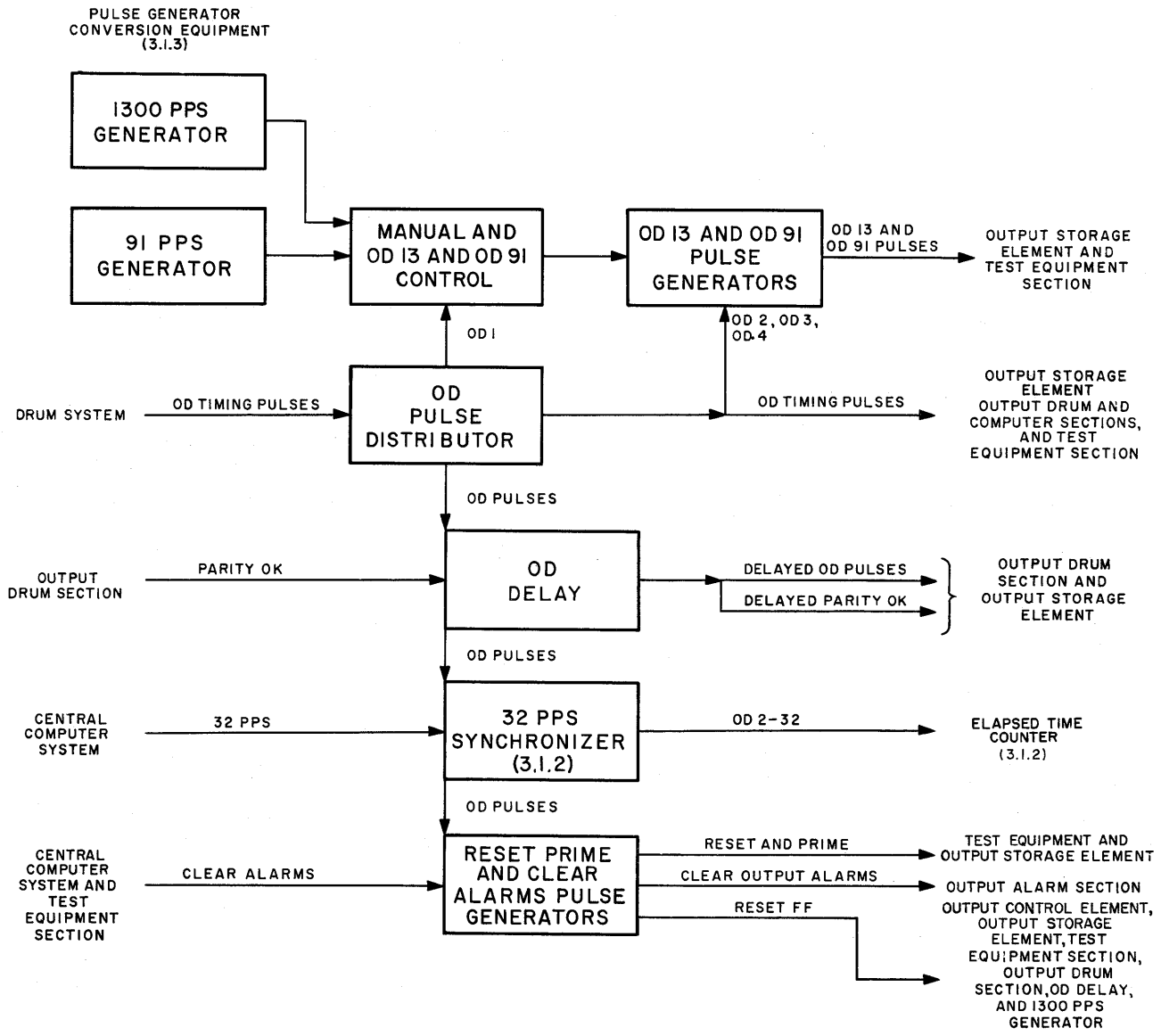


Figure 2–36. Pulse Generators (3.1.3), Block Diagram

3.3.2 OD Pulse Distributor

The OD pulse distribution circuit consists of four gates and four register drivers (fig. 2–37). Each gate is fed a different OD pulse from the Drum System. The OD pulses are a series of timing pulses generated within the Drum System as described in 2.1 of Chapter 2.

The four gates of the OD distribution circuit are simultaneously conditioned by the enable-OD pulses d-c level. This level is produced in the test equipment section and remains up unless an error is detected during a test operation. The OD pulses are passed through the gates and register drivers and then distributed to the output storage element, the output drum section, the output computer section, and the output test equipment section.

3.3.3 91-PPS Generator

The 91-pps generator contains a tuning fork oscillator, a Schmitt trigger, and a pulse generator (fig. 2–38). The 91-pps generator tuning fork oscillator is turned to 364 cps which is a multiple (4th harmonic) of the desired frequency of 91 pps. The output of the oscillator is a sine wave which is fed to the Schmitt trigger. This circuit generates a trigger pulse for each cycle. These trigger pulses are fed to the pulse generator which generates pulses at the rate of 364 pps. Two divider circuits are then used to step down the tuning fork oscillator frequency. Each divider circuit is composed of a flip-flop and a gate. (See fig. 2–38.) Pulses occurring at the rate of 364 pps are applied to frequency divider A as complementing signals. This results in

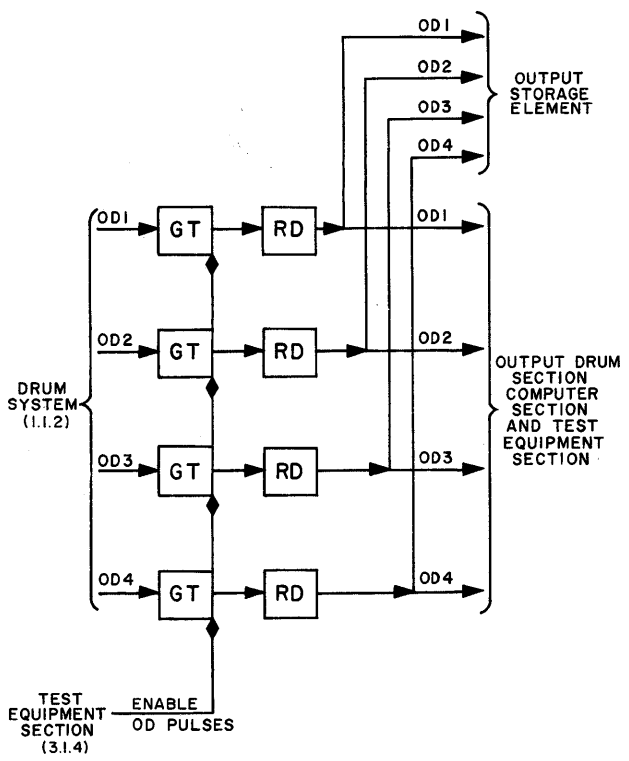


Figure 2–37. OD Pulse Distributor (3.1.3), Simplified Logic Diagram

frequency divider A producing output pulses at the rate of 182 pps which are then applied to frequency divider B. The final result is the desired output of 91 pps which is sent to the OD 91 pulse control circuit. The detailed method by which the frequency is brought down to 91 pps is as follows: Assume that initially FF 1 and FF 2 are both cleared (the 0 side up). When the first 364-pps pulse arrives, it cannot pass GT 1, since this gate is not conditioned. However, this pulse will set FF 1, conditioning GT 1. When the second 364-pps pulse arrives, it passes through the now-conditioned GT 1. The pulse cannot pass through GT 2, since FF 2 is clear at this time, but it does set FF 2, conditioning GT 2. Also, this second pulse clears FF 1. The third 364-pps pulse cannot pass GT 1 since FF 1 was cleared by the second 364-pps pulse. However, the third pulse again sets FF 1. During this time, FF 2 has remained with its 1 side up. Therefore, when the fourth 364-pps pulse is applied, both gates are conditioned because both flip-flops are set, so the pulse passes through both gates. At the same time, this fourth pulse resets both flip-flops to their clear sides which was the original condition assumed. The action repeats continuously, one pulse passing GT 2 for every four pulses applied to GT 1. It follows that the 364-pps pulses are reduced to 91-pps pulses (1/4 of 364) at the output of GT 2. The following chart summarizes the action:

364-PPS PULSE NO.	GT 1	FF 1	GT 2	FF 2
Original State		0		0
1		1		0
2	Pulse	0		1
3		1		1
4	Pulse	0	Pulse	0

3.3.4 OD 91 Pulse Control Circuit

The OD 91 control circuit (fig. 2–38) controls the synchronizing of the 91-pps signals with OD timing pulses. The 91-pps signals, when synchronized with OD pulses, are referred to as OD 91 pulses. Means are provided to control the generation of the pulses in the OD 91 control circuit.

The 91-pps pulses are fed to GT 3 which is conditioned by a d-c level (enable-OD pulses) from the test equipment section. The enable-OD-pulses level remains up during normal operating conditions and may be brought down only during unit loop test. During normal operation, the 91-pps pulses then pass through a series of logical circuits, are synchronized with OD 4 + 0.4 timing pulses, and produce output pulses at GT 4 occurring at the rate of 91 pps (OD 4 + 0.4–91). That is, the output pulses are OD 4 + 0.4 pulses occurring at the rate of 91 pps. The logical circuit consists of FF 3 and GT 4. The 91-pps generator produces pulses at a rate of 91 pps. A pulse is applied to the 1 side of FF 3 which brings its 1 side up. This conditions GT 4 which passes an OD 4 + 0.4 pulse. However, before the next OD 4 + 0.4 pulse is applied to GT 4, the clear pulse at time OD 2–91 clears FF 3, deconditioning GT 4. An OD 4 +0.4 pulse will not be passed through GT 4 until the next 91-pps pulse arrives to condition GT 4. Hence, it follows that GT 4 passes OD 4 + 0.4 pulses at the rate of 91 pps. These pulses are called OD 4 + 0.4–91 pulses.

3.3.5 OD 91 Pulse Generator

The TTY output storage element requires controlling pulses occurring at the rate of 91 pps. It is further required that these pulses be provided in three groups:

a. 91 pps synchronized to occur at OD 2 time (OD 2–91).

b. 91 pps synchronized to occur at OD 3 time (OD 3–91).

c. 91 pps synchronized to occur at OD 4 time (OD 4–91).

The above pulses are synchronized in the OD 91 pulse generator (fig. 2–38).

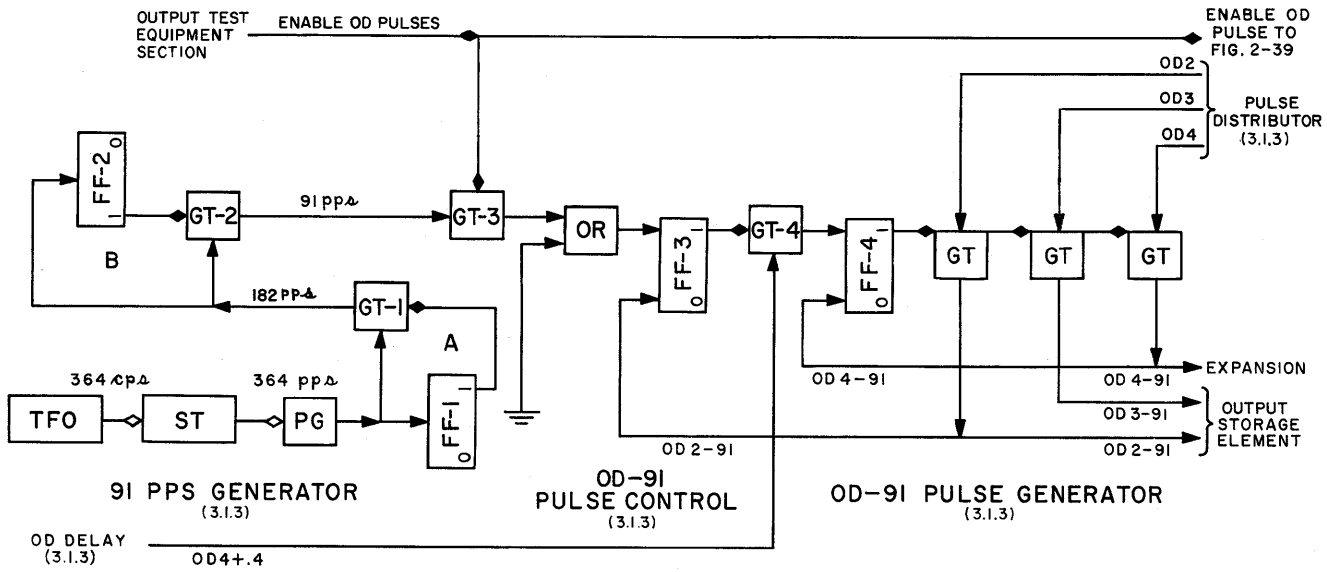


Figure 2–38. 91-PPS Generator, OD 91 Control, and OD 91 Pulse Generators (3.1.3), Simplified Logic Diagram

Each OD 4 + 0.4–91 pulse is applied to the OD 91 pulse-stop flip-flop (FF 4), causing a level to be generated which conditions a series of gates. The result is the generation of the desired OD 2–91, OD 3–91, and OD 4–91 pulses. Every OD 2–91 pulse is sent back to the OD 91 pulse control circuit as a clear pulse, as described before. The OD 4–91 pulse clears the pulse-stop flip-flop so that only one series of OD pulses will pass through the gates for each start-OD 91 pulse applied to FF 3. Synchronized OD 2–91 and OD 3–91 pulses are fed to the output storage element.

3.3.6 1,300-PPS Generator

The 1,300-pps generator makes up the pulse generator conversion unit and consists basically of a tuning fork oscillator, a zero detector, and a flip-flop. (See fig. 2–39.) The tuning fork oscillator also feeds 1,300 cps to the output storage section which uses this signal as a continuous 1,300-cps timing signal. (Refer to Part 4.)

The output of the tuning fork oscillator is a continuous 1,300-cps sine wave. This signal is fed to a data conversion receiver (DCR) which functions in this circuit as a zero detector. Under this condition, the zero detector provides a pulse every time the sine wave passes through zero degrees in a negative-going direction. Hence, it provides continuous pulses at 1,300 pps. These pulses are applied to the 1 side of FF 1. The flip-flop converts the negative pulses from the zero detector to the standard positive level required to condition GT 1. Flip-flop 1 is reset by an OD 2–13 pulse from the OR circuit as described in 3.3.7. The flip-flop can also be cleared by the reset flip-flops or start pulse at the OR circuit. This is done when power is first supplied to the system or when a test is started.

3.3.7 OD 13 Pulse Control Circuit

The OD 13 control circuit (fig. 2–39) functions similarly to the OD 91 control circuit described in 3.3.4. The OD 13 control circuit controls the synchronizing of the 1,300-pps signals with OD timing pulses.

The 1,300-pps pulses cause GT 1 to be conditioned by FF 1 at a rate of 1,300 times per second. A gated OD 4 + 0.4 pulse is applied to this gate. The gated OD 4 + 0.4 pulse is present as long as GT 2 is conditioned by the enable-OD-pulses level, which is the case during all normal operations. The enable OD pulse may be brought down only during a unit loop test.

The OD 4 + 0.4 pulse is passed by GT 1 only when the gate is conditioned. Since the OD 2–13 clear pulse resets FF 1 after an OD 4 + 0.4 pulse is passed by GT 1, this gate does not pass another OD 4 + 0.4 pulse

until FF 1 is again set by the 1,300-pps signal. Since this action takes place at a rate of 1,300 times per second, GT 1 passes OD 4 + 0.4 pulses at a rate of 1,300 pps. These pulses are called OD 4 + 0.4–13 pulses.

3.3.8 OD 13 Pulse Generator

By comparing figures 2–38 and 2–39, it can be seen that the OD 13 pulse generator operates similarly to the OD 91 pulse generator described in 3.3.5.

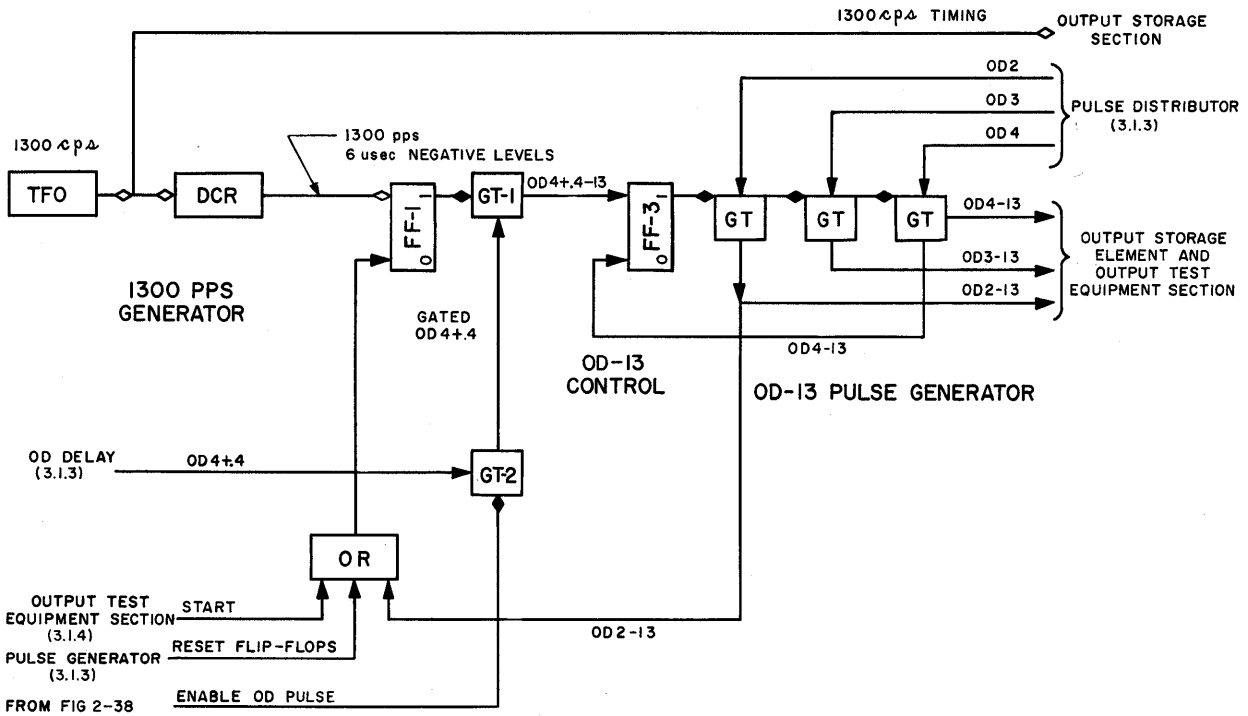


Figure 2–39. 1,300-PPS Generator, OD 13 Control, and OD 13 Pulse Generator (3.1.3), Simplified Logic Diagram

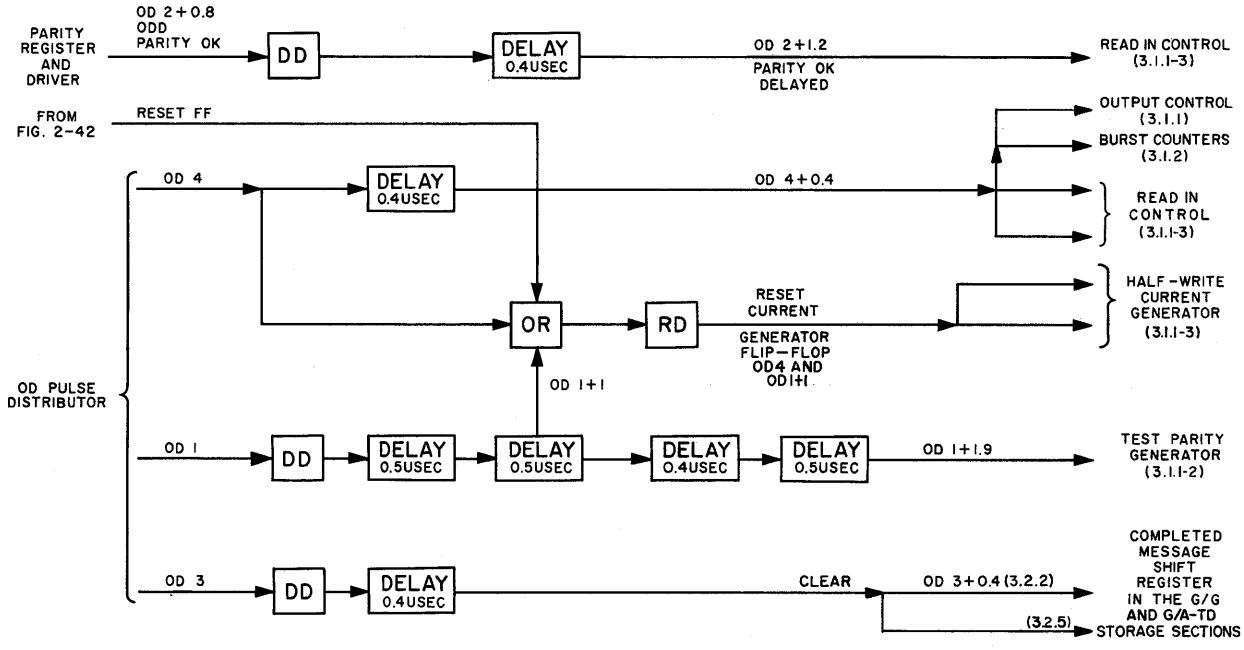


Figure 2–40. OD Delay (3.1.3), Simplified Logic Diagram

3.3.9 OD Delay

In order to perform their functions in proper sequence, sections of the output control and output storage elements require pulses that occur between OD pulses. These delays are essential to the output control element where the delayed pulses initiate, in correct sequence, the parity count and certain read-in operations. A delayed pulse is also required for proper operation of the completed message shift register in the G/G and G/A-TD storage sections. These delayed pulses are produced by passing the OD pulses through delay circuits and their associated delay drivers (fig. 2–40). The delayed pulses are then distributed to the test parity generator, the half-write current generator, the read-in control, and the pulse generators, all of which are located in the output control element, and to the completed message shift register in the output storage element.

3.3.10 32-PPS Synchronizer

The elapsed-time counter in the G/A-FD storage section of the output storage element is employed to record time in steps of 1/32 second and must therefore be stepped at the rate of 32 pps. This stepping pulse is applied to the elapsed-time counter by the 32-pps synchronizer. (See fig. 2–41.) A 32-pps signal from the Central Computer System is synchronized with OD pulses, and the resulting step-elapsed-time-counter pulse (OD 2–32) is fed to the G/A-FD elapsed-time counter.

3.3.11 Reset Flip-Flop, Reset and Prime, and Clear-Alarms Pulse Generators

Prior to and following each test operation, reset flip-flop and reset-and-prime pulses are applied to the output storage element, and to other circuits of the Output System. These pulses are produced as shown in figure 2–42. The generation of these pulses is controlled by either of two pushbuttons, one located in the test equipment section and the other at the maintenance console of the Central Computer System. The reset flip-flop levels thus produced trigger the respective pulse generators which produce a reset flip-flop pulse. This pulse is sent to the output storage element, the output control element, the test equipment section, the right flip-flops, the set pulse flip-flop, the burst-time counter, and the 1,300-pps generator. It is also applied to a series of flip-flops and gates whose output is the reset-and-prime pulse which is sent to the output storage element and test equipment section.

A reset flip-flop pulse is also produced by the vaccuum tube relay driver (VRD) and its associated pulse generator. The VRD operates a relay which causes the pulse generator to produce a pulse when the power to the system is turned on. This ensures that the flip-flops are cleared at the start of operation. Provision is made at the maintenance console for clearing output alarm indications at the alarm display.

3.3.12 Reset Drum Status Bit Generator

The reset drum status bit generator circuit shown in figure 2–43 is used during a test operation to restore drum status bits onto the drum status channels of the three OB drum fields, thereby causing data information stored on the drums to be retained following a drum readout cycle. This function is particularly desirable for testing the Output System in that a program is stored and retained on the drums where it can be read out repeatedly, without the intervention of the Central Computer, to test individual storage sections of the Output System.

This test function is accomplished by activating the NO COMPARE TO DRUMS switch to energize relay K1 shown in figure 2–43. Following a drum readout cycle of the three OB drum fields, and at the completion of the G/A-TD burst counter cycle, a burst time carry (BTC) pulse (OD 4) is generated to set the reset drum status bit flip-flop. This BTC pulse is generated at the completion of the G/A-TD burst time counter cycle or every 23 seconds (256 x 90 ms). Since the G/A-TD BTC cycle is longer than the BTC cycles of the other storage sections, a complete search of the drums occurs in the 23-seconds cycle. All words will have been read; therefore, all the drum status bits will be in the zero state.

The reset drum status bit flip-flop, when set by a BTC pulse, remains in this state for a period of 60 ms. In turn, a gating level is applied to GT 1 which is normally strobed by OD 1 + 1.9 pulses. The latter are passed by the conditioned gate for 60 ms and routed through the closed contact points of energized relay K1 as no-compare pulses to the Drum System. Sufficient time is provided, therefore, to allow the reset drum

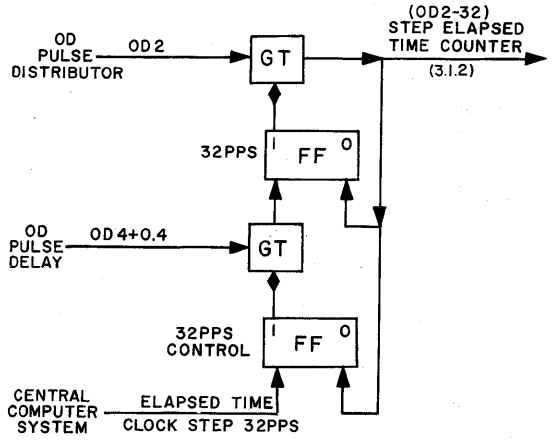


Figure 2–41. 32-PPS Synchronizer (3.1.2), Simplified Logic Diagram

status bit generator to write 1's in the status channels associated with the three drum fields of the OB drum (20 ms per field). This causes the drum test data to be retained on the drums in preparation for a subsequent drum readout cycle and without further intervention from the Central Computer.

In general, programs used for this particular test function are written so that a burst-time count equal to zero is never included in the program. Accordingly, the generation of a non-search alarm is prevented. In addition, prior to the test function and loading of a program on the drums, the OB drums should be erased and placed in a COMPUTER TEST mode. Following the loading of the program on the drums, the drums are placed in the OPERATE mode. This action prevents the drum status channels from being restored to the 1 state while a program is being loaded on the drums. If the program does not fill all available drum addresses, all zero words will be sent to the Output System. This will cause a drum parity alarm and an illegal section alarm which should be disregarded for the purposes of this type of test.

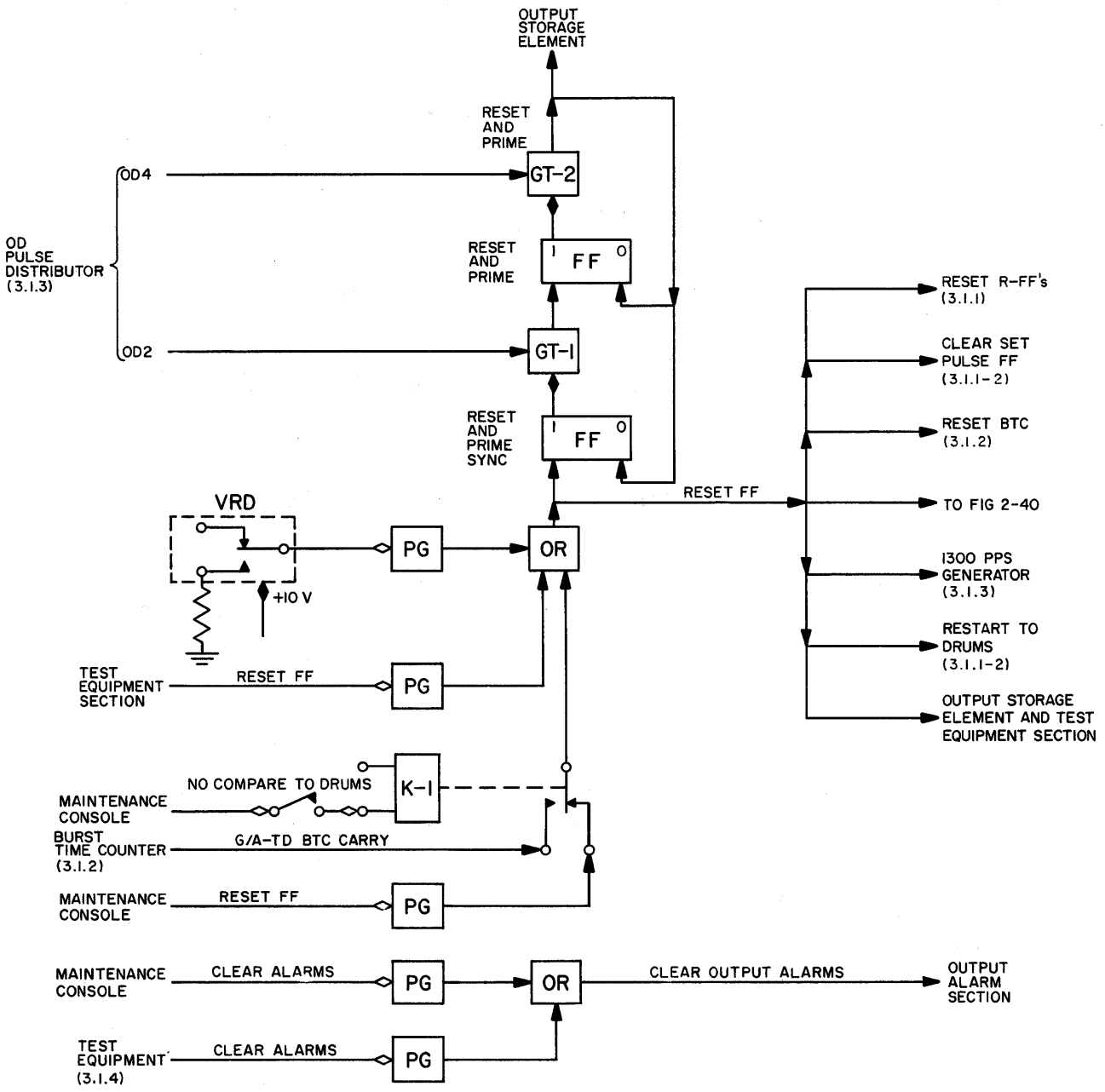


Figure 2–42. Reset Flip-Flop, Reset-and-Prime, and Clear-Alarms Pulse Generators (3.1.3), Simplified Logic Diagram

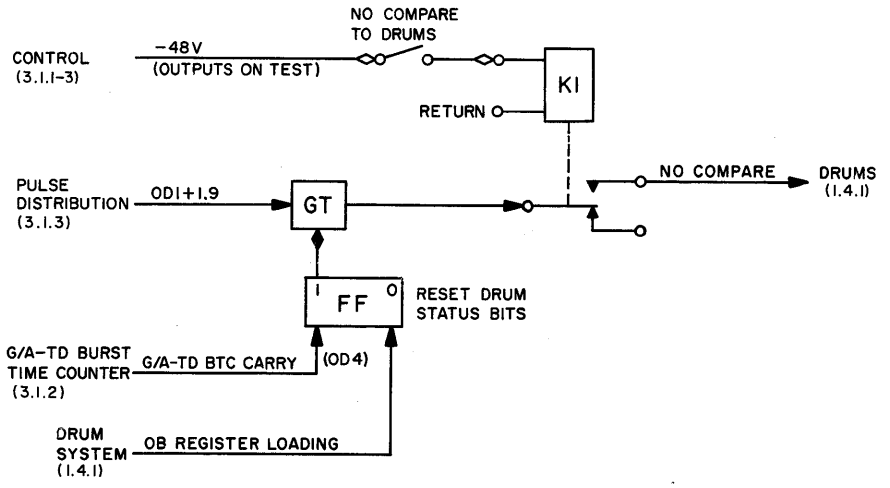


Figure 2–43. Reset-Drum Status Bits Generator, Simplified Logic Diagram

CHAPTER 4
OUTPUT ALARM SECTION

4.1 INTRODUCTION

It is necessary to install certain alarms in the Output System to indicate to maintenance personnel the nature of errors which may develop within the system. It is the function of the output alarm section to store the status of the alarms and to display their status by means of neon indicators. The alarms which are provided are the nonsearch comparison, G/A-FD, G/G, G/A-TD, BO2, BO1, TTY, parity-NG, illegal address, illegal section, and lost parity.

The output alarm system displays other conditions, as shown in figure 2–44. The contents of the output drum section flip-flop register, some of the OD pulses distributed by the output computer section, and the various test pulses are also displayed by neon indicators. Besides this, indicator lamps are included to display certain test operations.

The nonsearch comparison alarm is generated when a word on the OB drum is read into the flip-flop register with the proper burst number for the section to which it is addressed; but the word arrives during the nonsearch period of the current burst. In this case, conditions are such that this word can never be accepted from the drum because the nonsearch period is the last part of any given burst period and the burst number changes before another search period can occur. Thus, the word will be lost (erased).

The G/A-FD, BO1, or BO2 alarm occurs whenever the respective storage section parity is bad or when the number of words read into the array does not agree with the number of busy bits read out of the array. The G/A-TD, G/G, or TTY alarm is generated when its storage parity is bad. The parity NG alarm is generated when the parity of the word received in the OB register is bad. The illegal address or illegal section alarm occurs when the storage register address or the section address contained in the left half-word of the OB register has not been assigned to an actual section or

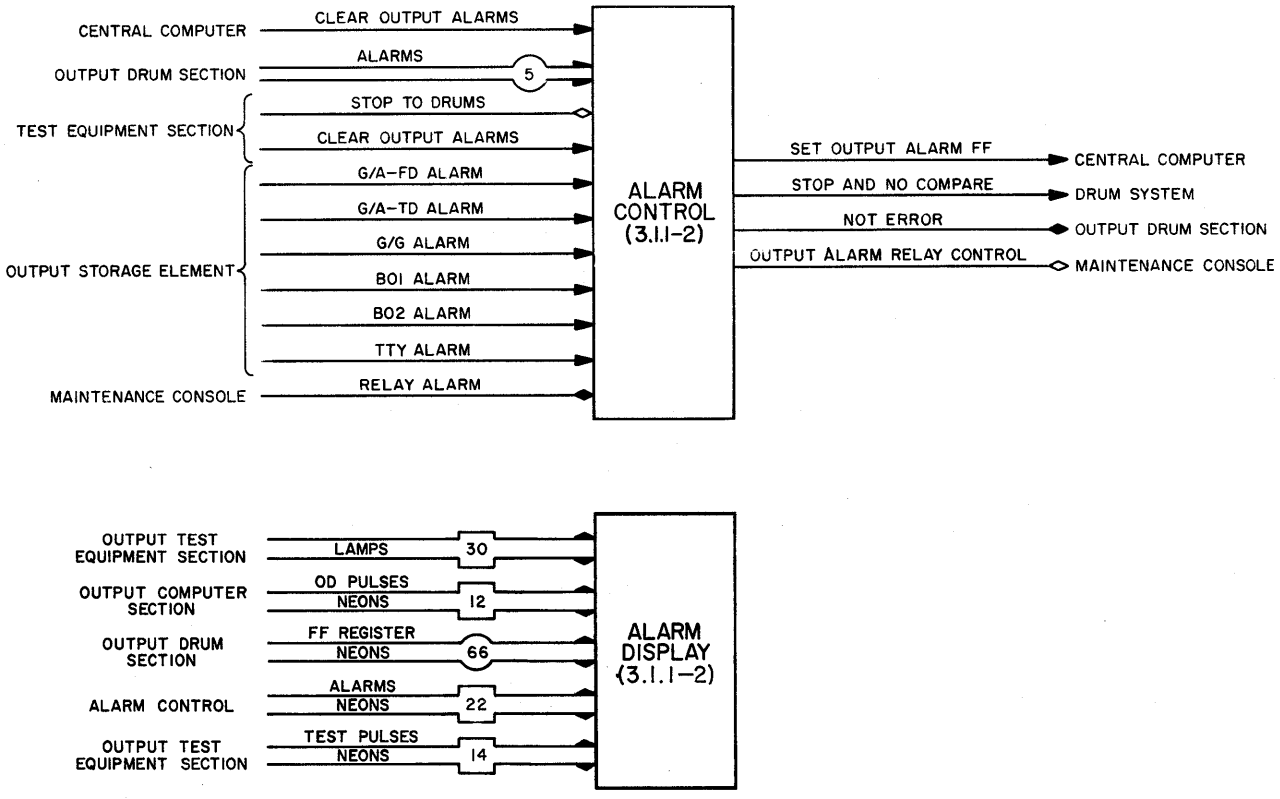


Figure 2–44. Output Alarm Section, Block Diagram

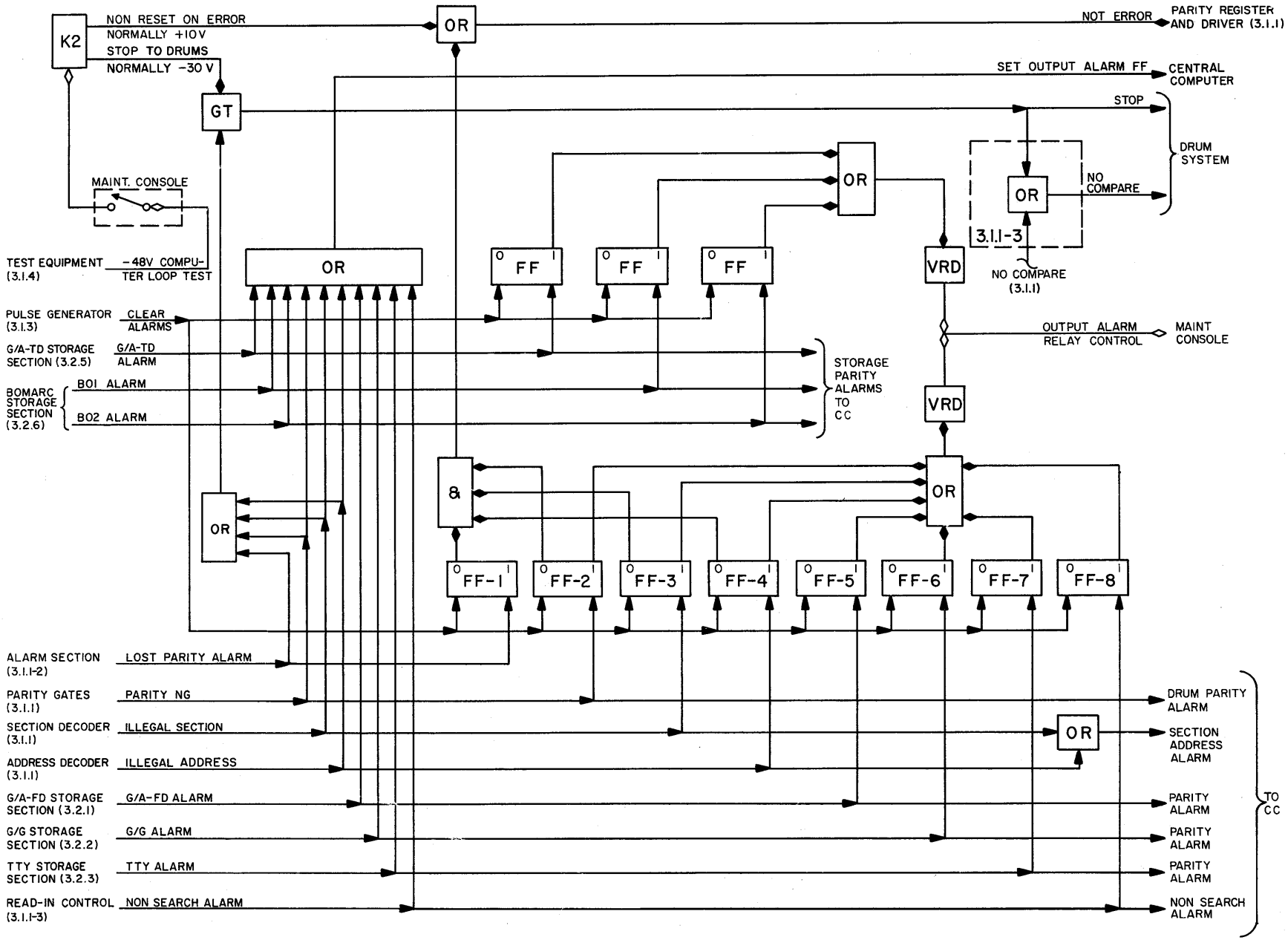


Figure 2–45. Output Alarm Control (3.1.1-2), Simplified Logic Diagram

register within the Output System. The lost parity alarm is generated when a parity check on the word in the OB register is not initiated or completed.

The output alarm section is broken down into two parts: the alarm control and the alarm display. (See fig. 2–44.)

4.2 ALARM CONTROL

The statuses of the various alarms are stored within the alarm control. (See fig. 2–45.) One flip-flop is provided for each alarm. The 1-side indicator neon of each flip-flop is located in the alarm display unit.

The 1 outputs of all the alarm flip-flops are sent through an OR circuit to a VRD, the relay of which continually sends to the maintenance console in the Central Computer System indication of whether there is an output alarm. These two signals activate indicator lights on the maintenance console. The 0 sides of the illegal address, illegal section, parity NG, and lost parity alarm flip-flops are fed to an AND circuit. The output of this AND circuit feeds one leg of a 2-way OR circuit. The other leg of the OR circuit is connected to either +10V or −30V, depending on the status of the STOP TO DRUMS relay. In normal operation, this relay will be de-energized, thus supplying +10V through its N/C contacts to the OR circuit. Therefore, the output of the OR circuit generates a NOT ERROR level; that is, always +10V during normal operation. This level is used to condition a gate tube in the OB register reset control circuitry. When the gate tube is conditioned, the resetting of various flip-flops in the Output System, in addition to the OB register flip-flops, is effected in the normal manner. It is sometimes desired, during computer loop test, to have the operation of the Output System halt, when an error is incurred, and to inhibit the resetting of the various flip-flops, particularly the OB register flip-flops. Thus, the word that caused the error is retained in the register for examination. This is accomplished by the STOP TO DRUMS switch on the duplex maintenance console which controls the STOP TO DRUMS relay mentioned previously. When the switch is activated, −48V is supplied from the test circuitry through the switch to energize the STOP TO DRUMS relay. With the relay energized, −30V is fed to one leg of the OR circuits which supply the NOT ERROR level. Therefore, the NOT ERROR level will now be dependent upon the status of the illegal address, illegal section, parity NG, and lost parity alarm flip-flops. If one of these flip-flops is set as a result of an error, no level (NOT ERROR) will be present at the gate, deconditioning the gate tube which passes the reset pulse. Therefore, the contents of the OB register may be examined to determine the cause of the error.

The parity-NG, illegal-address, illegal-section, and lost-parity pulses are also fed through an OR circuit to a gate. When this gate is conditioned by a stop-to-drums signal from the test equipment section, a stop pulse is transmitted to the Drum System and to the read-in control unit. When an error occurs here, the stop pulse or a no-compare pulse passes through an OR circuit and goes to the Drum System. The purpose of the stop pulse during the test procedure is to inhibit the transfer of data from the OB drum to the Output System, to prevent the erroneous word in the drum register from being erased, and to hold the operation of the Output System so that the error can be examined.

The alarm pulses from the various sections also cause a set-output-alarm-synchronizing flip-flop signal to be sent to the Central Computer System. This flip-flop is used by the Central Computer System to sense an output alarm. The alarm pulses from the various sections also go to a group of OR circuits. An output parity alarm is generated if parity does not check out in any of the six output sections. A nonsearch alarm, drum parity alarm, or a section or register alarm is generated if any of these conditions do not check out. These alarms are used in the Central Computer System.

4.3 ALARM DISPLAY

The purpose of the alarm display is to indicate to maintenance personnel any malfunctioning of the Output System. The alarm displays (fig. 2–46) are on the indicator and test control panel located on the test door on the back of output control unit 42. Neon indicators on the panel indicate the statuses of the Output System alarms. Neon indicators are also provided for various registers within the Output System. Among the quantities represented in the alarm display are the contents of the drum word flip-flop register and certain of the timing pulses. Also represented in the alarm display of neons and lamps are various control functions used in testing the Output System.

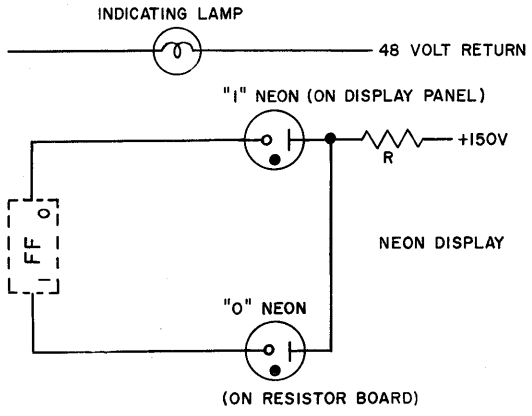


Figure 2–46. Alarm Display (3.1.1-2), Simplified Block Diagram

Note in figure 2–46 that there are two neon tubes associated with each display. Only the 1 neon is on the display panel and is read. If it is on, it indicates a 1 bit; if it is off, it indicates a 0 bit. The other neon is used to cut off the firing of the 1 neon when the 0 side of the flip-flop is up (+10V) since, at this time, the 1 side is down (—30V). In order to cut off the firing of the 1 neon when the 1 side is down (—30V), the 0 neon is included. This neon fires when the 1 side is down and effectively shorts out the voltage across the 1 neon. If the 0 neon were not included, a rather complex circuit would be necessary to cut off the firing of the 1 neon when the 1 side of the flip-flop goes from up to down.

PART 3
OUTPUT STORAGE ELEMENT

CHAPTER 1
INTRODUCTION

1.1 GENERAL

Data processed by an AN/FSQ-7 Combat Direction Central is made available to associated components of the Air Defense Command sector through the Output System and commercial telephone line facilities. Information enters the Output System from the Drum System at a relatively high rate of speed. By temporarily storing this information, the output storage section of the Output System slows down the rate of transmission to a frequency that is compatible with commercial telephone line equipment.

Output data is classified into six general categories: ground-to-air frequency division (G/A-FD), BOMARC 1 (BO1), BOMARC 2 (BO2), ground-to-air time division (G/A-TD), ground-to-ground (G/G), and teletype (TTY). G/A-FD and G/A-TD data is utilized by airborne interceptors; BOMARC data is used in conjunction with unmanned interceptors; G/G data is intended for adjacent centrals, higher headquarters, and height-finder radars. Among the possible uses for TTY data are crosstelling to nonmechanized adjacent sectors, crosstelling to higher headquarters, and the feeding of early-warning data directly to antiaircraft gun batteries.

The output storage element is divided into six sections to accommodate the six general categories of output data now being used. (See fig. 3–1.) Provision is made, however, for possible future expansion of the output storage element to eight sections.

All information enters the output storage section through the output control element after being checked for accuracy and proper sequence. The output control element accepts words from the output buffer drum at 10-μsec intervals. However, the words are distributed on the drum fields so that the smallest interval between successive words entering a storage section is 20 μsec. This provides ample time for a storage section to store a word and prepare for the next incoming word.

Each storage section has its own timing and control circuits (G/A-FD, BO1, and BO2 sections share their circuits) which enable it to accept words and transmit messages independently of the other sections. Synchronism with the Drum System and the output control element is achieved by using the OD drum timing pulses.

1.2 BURSTS

Each storage section can store and then transmit more than one message simultaneously. The simultaneous transmission of all messages stored in a storage section is called a burst. The six storage sections differ in the number of messages that can be stored at one time. Therefore, the burst size of each of these sections differs. The size of each burst for each section is as follows:

OUTPUT MESSAGE	NO. OF MESSAGES	OUTPUT WORDS PER MESSAGE	BITS PER OUTPUT WORD
G/A-FD	2	13	18
BO1	2	13	18
BO2	2	13	18
G/A-TD	3	4	17
G/G	5	5	17
TTY	25	1	18

An output word consists of a right half-word, a storage parity bit, and, in some cases, additional 1 bits called busy bits. Drum words containing the right half-words of messages to be transmitted during a burst are assigned the same burst number by the Central Computer System. This enables the Output System to identify the drum words for a particular burst and to ensure that only those words are accepted from the output buffer (OB) drum and subsequently transmitted during the associated burst period.

1.3 BURST PERIOD

The interval during which an Output System storage section receives all messages of a specific burst and then transfers the burst to transmission equipment is a burst period. The burst periods of each of the six Output System storage sections are of different duration and occur successively. The length of each burst period is as follows:

STORAGE SECTION	BURST PERIOD
G/A-FD	0.25 sec
BO1	0.25 sec
BO2	0.25 sec
GA/-TD	0.090 sec
G/G	0.070 sec
TTY	0.495 sec

Each burst period is composed of search time and readout time. Search time is the only portion of a burst period during which the Output System storage section can receive the output words of a burst from the OB drum. Readout time is the interval during which the burst is transferred to transmission equipment. Since drum words containing the right half-words of a burst are written at random on the three OB fields, some drum words of a specific burst may be stored on each of these fields. To ensure that all drum words of the burst are read during search time, the minimum search interval is made equal to the amount of time required to read all three OB fields. This search interval is determined as follows: 6,108 drum word registers (2,036 per field) times 10 μsec (interval between successive drum registers) plus 360 μsec (120 μsec per field for switching) equals 61.4 ms. Allowing for drum speed variations, search time for each burst period, except for G/A-TD, is set at approximately 65 ms. The search interval is approximately the same for five of the six storage sections. The search interval for G/A-TD is approximately 86.2 ms.

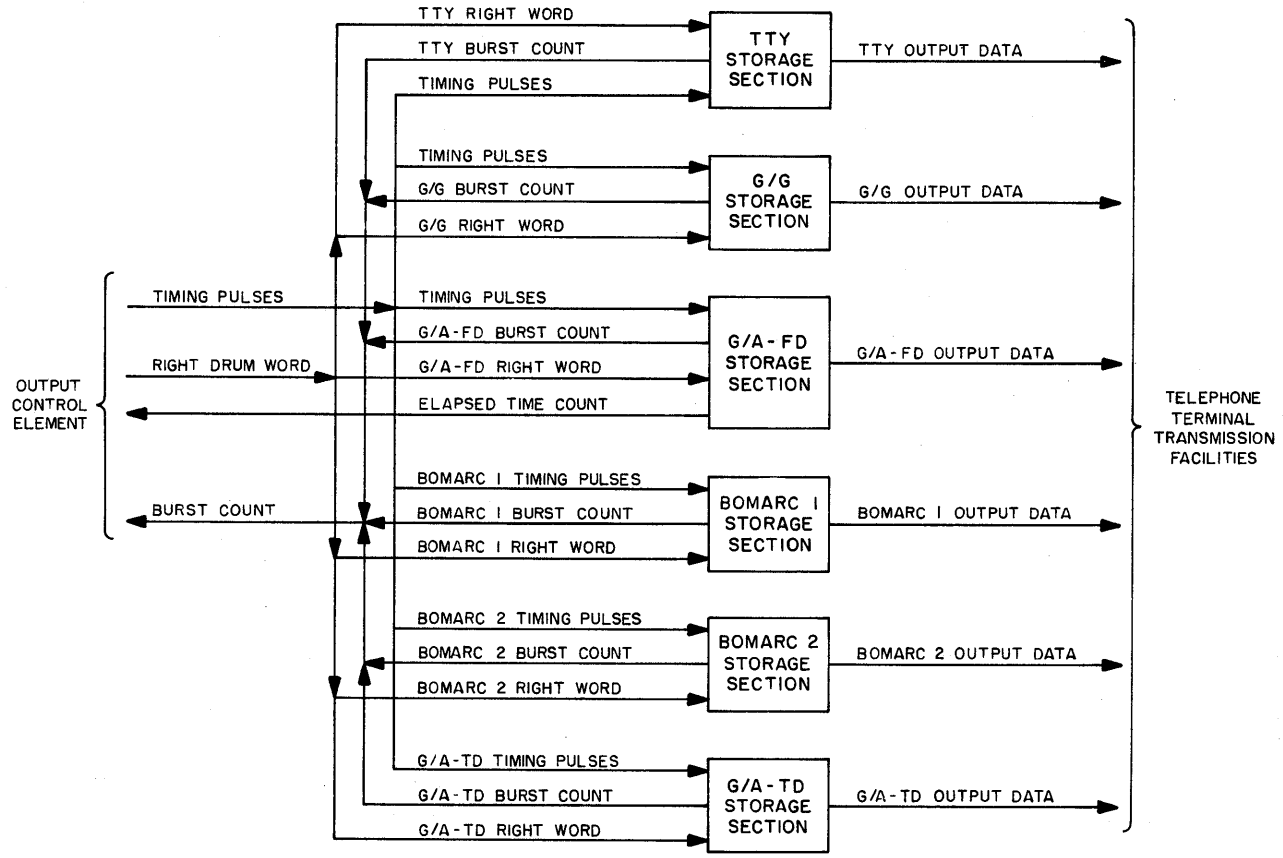


Figure 3–1. Output Storage Element, Block Diagram

CHAPTER 2

GROUND-TO-AIR FREQUENCY DIVISION, BOMARC 1, AND BOMARC 2 STORAGE SECTIONS

2.1 GENERAL

This chapter contains information pertinent to the functional operation of the G/A-FD, BO1, and BO2 storage sections. Since these storage sections are identical physically and functionally, it suffices to present only a discussion on the theory of operation of the G/A-FD storage section. All information presented concerning the G/A-FD storage section is also applicable to the BO1 and BO2 storage sections.

The G/A-FD, BO1, and BO2 storage sections receive output words in parallel form from the output control element and assemble these words into messages in serial, interleaved form for transmission over telephone data channels to data-link transmitters. The data-link transmitters relay the G/A-FD messages to manned airborne interceptors and the BOMARC messages to unmanned interceptors (missiles). Each G/A-FD output word transmitted constitutes one interceptor message; that is, a message on which the aircraft takes action. Each G/A-FD data-link transmitter operates on a particular frequency which is received only by some of the aircraft within a particular area. Only those aircraft prepared to receive information on the particular frequency take action.

2.2 OPERATION (G/A-FD, BOMARC)

A simplified diagram of the G/A-FD storage section which is also representative of the BOMARC storage sections is shown in figure 3–2. As depicted in this diagram, the G/A-FD storage section is logically divided into the following areas:

a. Storage. The storage circuits store the two G/A-FD messages prior to their being sent to the readout circuits.

b. Control. The control circuits initiate and control all operations of the G/A-FD output storage section.

c. Readout. The readout circuits prepare the messages for transmission to the conversion circuits.

d. Burst counting and compare. The burst counting and compare circuits check the drum word in the output control element to ensure the correct sequence of message transmission.

e. Message check. The message check circuits check the transmitted messages for errors.

f. Conversion. The conversion circuits modify the G/A-FD messages to gated 1,300-cycle sine waves for transmission over the telephone data channels.

g. Switching. The switching circuits are used to perform test functions. They are also used to switch output storage data from the telephone lines to the test equipment section.

The operation of the G/A-FD storage section is repetitive; that is, it completes its sequence of operations and then repeats these same operations as long as the system is in operation. One complete cycle of operations of the storage section is called a burst period. The burst period is divided into two functional intervals called search time and readout time. The division of the burst period into these two intervals is accomplished by the action of the control circuits. These circuits, shared by both storage sections, are represented as the 13 counter, 25 counter, and G/A-FD control. In addition, these circuits also control the functions of the storage section during each separate interval.

2.2.1 Counter Operation

In order for the counters to control the operation of the output storage section and perform the timing functions specified in the following paragraphs, the 13 counter and the 25 counter are operated as follows:

a. The 13 counter is shifted at a 1,300-pps rate by timing pulses received from the output control element. For every 13th shift of the 13 counter, a 13-counter-carry pulse is generated. These pulses are used to shift the 25 counter. The 25 counter is therefore shifted every 13/1300 or 1/100 second.

b. The 25 counter repeats its counting cycle after it has been shifted 25 times; that is, every 25/100 second. During this interval, a complete operational cycle of the G/A-FD output storage section occurs and is known as a G/A-FD burst period. Therefore, the G/A-FD burst period is 0.25 second long.

2.2.2 Search Time

Search time is the interval during which output words are accepted for storage by the storage section.

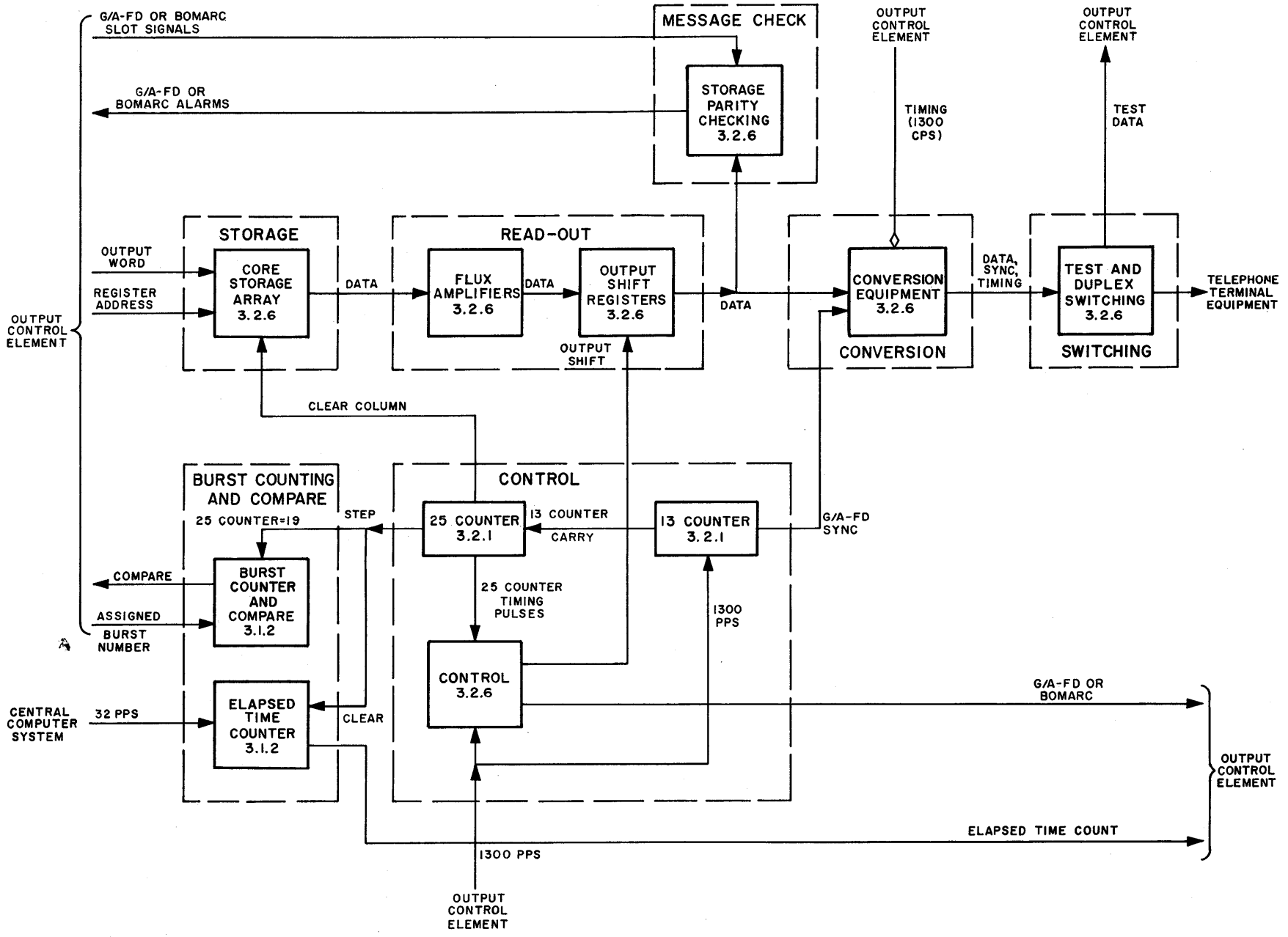


Figure 3–2. G/A-FD or BOMARC Output Storage Section (3.2.1, 3.2.6), Block Diagram

The duration of search time is 65 ms and is so chosen to allow sufficient time to examine each register in the OB fields for words to be transferred to the core storage array.

The 25 counter controls the start and end of search time. Search time starts at the time of the 19th shift of the 25 counter, called 25-counter-19 time. At this time, a 25-counter-19 pulse is generated, which shifts the burst counter, clears the elapsed-time counter, and, together with the G/A-FD control, supplies a search level to the output control element to indicate that it is ready to receive output words for a new burst.

During search time, every word present on the OB drum is examined both in the output control element and in the burst counting and compare circuits of all storage sections. The output control element determines in which storage section the word is to be entered. It also determines if there are any errors in the word. If the word is correct and is assigned to the G/A-FD section, and if the assigned burst number of the word compares with the present contents of the G/A-FD burst counter, the word is accepted and read into the storage array.

The accepted output words, each of which consists of a right half-word and a storage parity bit, are assembled in the G/A-FD core storage array in two slots, each composed of 13 core registers. The information contained in the two slots at the completion of search time makes up the two G/A-FD messages.

Search time continues until the 25th shift of the 25 counter. At this time, called 25-counter-25 time, the 25 counter generates a 25-counter-carry pulse. This pulse causes a sync pulse to be generated by the 13 counter, and also causes the G/A-FD control to raise the not-search level, thereby ending search time. The 25 counter now repeats its operational cycle. The time of the next shift of the 25 counter is called 25-counter-1 time. At this time, the 25 counter generates an output pulse called a clear-column-1 pulse; this pulse starts the interval of the burst period called readout time.

2.2.3 Readout Time

Readout time is the interval between 25-counter-1 time and 25-counter-18 time; in other words, the interval between 25-counter-equals-1 and 25-counter-equals-18. During this interval, output words previously assembled in the core storage array are transmitted out over the telephone data channels. Readout is accomplished as follows. When the 25 counter is shifted by the 13 counter at 25-counter-1 time, a clear-column-1 pulse is generated by the 25-counter. This pulse is sent to the core storage array where it serves to send all information contained in the first column of cores through the flux amplifiers (FA's) and into the output shift registers (OSR's).

In the interval between 25-counter-1 time and 25-counter-2 time, the 13 counter is shifted 13 times. Simultaneously with each shift of the 13 counter, one bit of each of the two G/A-FD messages contained in the OSR's is sent to both the storage parity check circuit and the conversion circuits. At the storage parity check circuit, the data is entered and later examined for errors. If an error is found, a G/A-FD alarm is sent to the alarm generator in the output element. At the conversion circuits, the data is made compatible for transmission by the telephone data channels. From the conversion circuits, the modified data is sent through the switching circuits out onto the telephone data channels. At the end of the 13-counter cycle, the OSR's are empty and the first bit of each word of the two G/A-FD messages has been sent out serially over two telephone data channels, one message to each data channel.

When the 13 counter is shifted for the 13th time following 25-counter-1 time, thus ending a 13-counter cycle, a 13-counter-carry pulse is generated which shifts the 25 counter. At this time, 25-counter-2 time, the 25 counter generates a clear-column-2 pulse. This pulse is sent to the core storage array where it serves to send the information contained in the second column of cores through the FA's and into the OSR's. This information is sent out over the telephone data lines in the same manner as the information from the first column of cores.

Readout continues as explained above until 25-counter-19 time. During this interval, all information contained in the columns of the core storage array is read out by the clear-column pulses. These clear-column pulses are generated each time that the 25 counter is shifted during the interval from 25-counter-1 time to 25-counter-18 time. At 25-counter-equals-19, the core array is completely clear and search time begins.

In the following paragraphs, the detailed operation of the various circuits of the G/A-FD output storage section as shown in figure 3–2 is discussed.

2.3 STORAGE (G/A-FD, BOMARC)

2.3.1 Core Storage Array

A core array is employed as the storage unit within the G/A-FD storage section. This core array is divided into two slots, each slot having the capacity to store one G/A-FD message. The array consists of 26 core registers, each register containing 18 cores. As shown in figure 3–3, a vertical line of cores is referred to as a column. It should be noted that figure 3–3 shows only one slot of the core array and, although only 13 registers are shown in this slot, there are 26 registers in the complete array.

Each core in the array has four separate windings. Three of these feed pulses into the core; the remaining

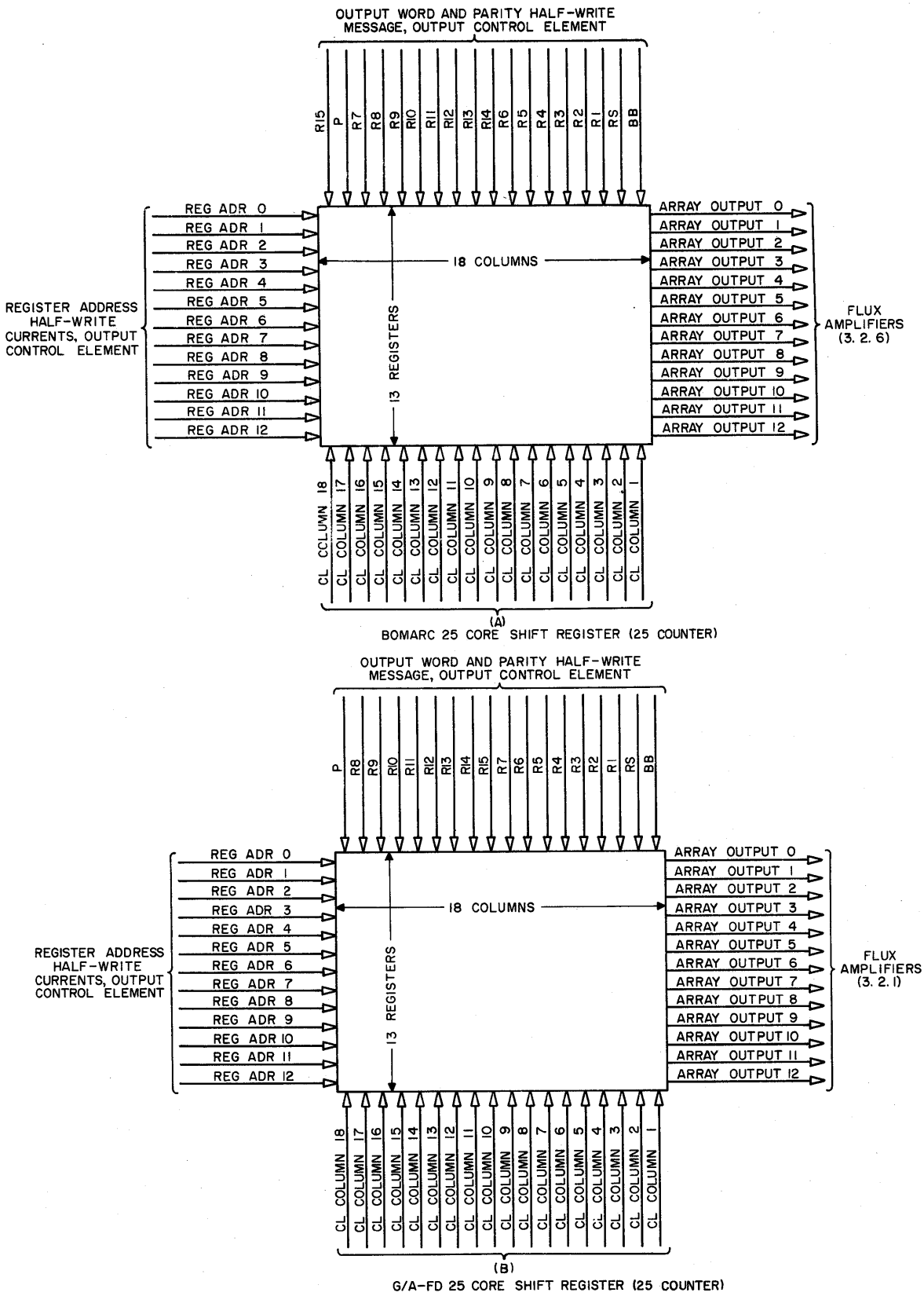


Figure 3–3. G/A-FD and BOMARC Core Storage Arrays (3.2.1, 3.2.6), Slot 1, Simplified Logic Diagram

winding is an array output winding known as the sense winding. (See fig. 3–4.)

The two input lines labeled half-write register address and half-write message, respectively, are used to write information bits into the cores. Each current pulse impressed upon one of these lines is equal in amplitude to a pulse carried on the other. A half-write message pulse or a half-write register address pulse, when applied separately to a core, has no effect upon the gate of that core. However, when both pulses are simultaneously applied to a core, the combined amplitudes set the core to the 1 state.

When a readout current pulse is applied to the third winding, labeled clear column N, the information contained in the cores is transferred to the sense winding which is labeled array output.

2.3.2 Core Array Read-In

Each core register in the array has the capacity to store an output word containing 18 bits. The output word is formed in the following manner. Eighteen bits (a right half-word, its associated parity bit, and a busy bit) are sent to the core array from the output control element. They are received over the 18 half-write message lines. (See fig. 3–3,B.) The busy bit is applied to column 1, the 16-bit right half-word is fed to columns 2 through 17 in the order shown, and the parity bit is applied to column 18. However, for a BOMARC word, the busy bit is applied to column 1, and the right half-word is fed to columns 2 through 18 in the order shown in figure 3–3,A. G/A-FD bits R8 through R15 are reversed as they enter the core array (fig. 3–3,B); similarly, BOMARC bits R7 through R15 are also modified to the order shown in figure 3–3,A. This is necessary in both cases because of data-link transmitter characteristics. The eight G/A-FD bits (R8 through R15) contain numerical data on which the manned aircraft takes action. The wiring in the airborne receiver is such that this information must be shifted in with its least significant bit first. The function of the G/A-FD or BOMARC busy bit is to indicate, at the data-link transmitter, that amplitude modulators for corresponding subcarriers are to be turned on for transmission data.

Half-write current pulses alone are not of sufficient amplitude to cause information bits to be written into the cores. However, simultaneously with the reception of the right half-word, the parity bit, and the busy bit, one of the 26 registers is selected by a half-write register address-current pulse. The right half-word, the parity bit, and the busy bit are then loaded into the selected

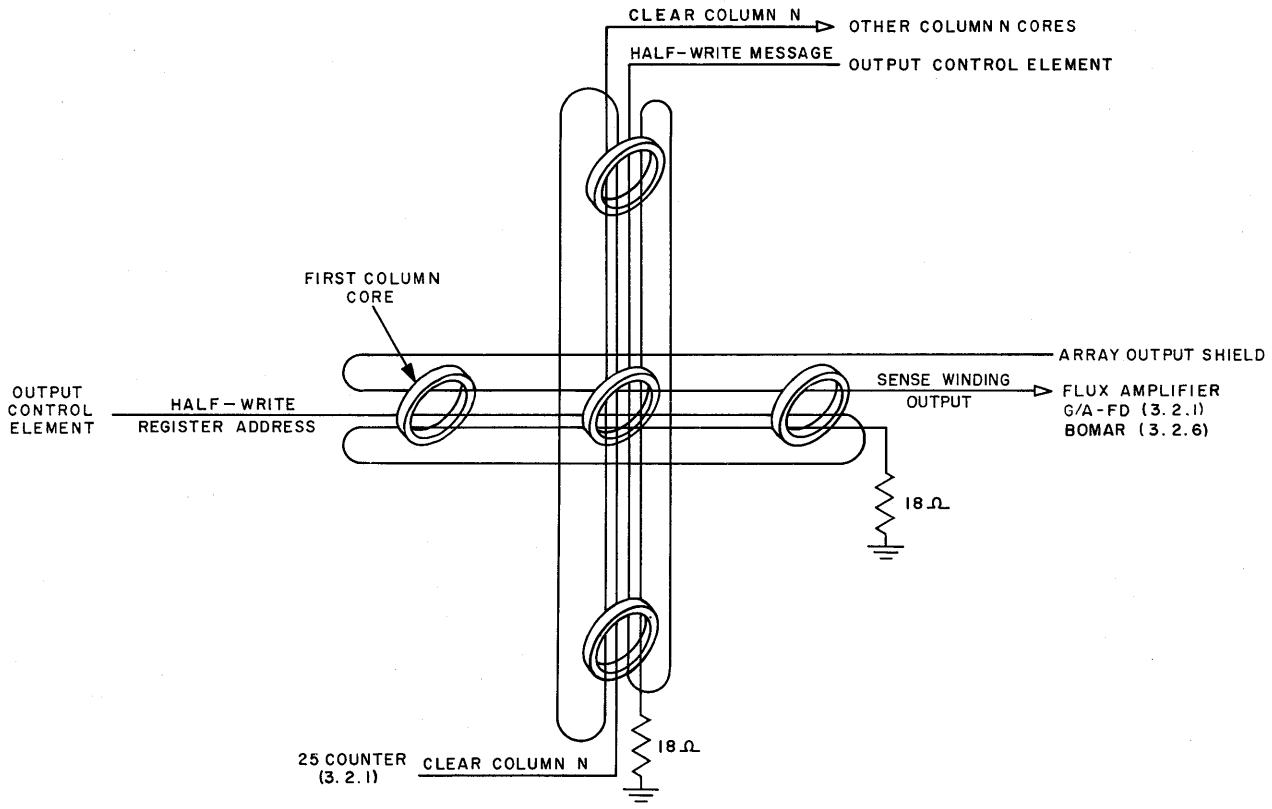


Figure 3–4. Core Windings, Simplified Diagram

register as the half-write message pulses and the half-write register-address pulse combine within the cores of the selected register. This operation is repeated each time an output word is read into the core array. The read-in operation occurs during search time of each G/A-FD burst period.

2.4 CONTROL (G/A-FD, BOMARC)

2.4.1 Timing

The G/A-FD and BOMARC burst periods are 0.25 second in duration; approximately 65 ms of this is search time. This is due to the fact that both storage sections share the same burst counter. Setting the search interval at approximately 65 ms allows sufficient time to read the OB fields and eliminates the possibility of missing a word of a G/A-FD burst. At the end of search time, there is an interval of approximately 5 ms during which a G/A-FD sync pulse is generated. Immediately following the 5-ms interval, readout starts and continues for the remaining 0.18 second of the G/A-FD burst period.

All signals controlling the above operations of the G/A-FD storage section are supplied by the 25 counter, 13 counter, and G/A-FD control circuits. (See fig. 3–5,B.) Similarly, the circuits used to control BOMARC signals are shown in figure 3–5,A. These circuits produce the pulses which initiate and terminate these and other various functional operations at the required times during each G/A-FD burst period. The functional operations controlled by the 13 counter, 25 counter, and G/A-FD control circuit are listed below in the order in which they occur:

a. Start and end search time during each burst period.
b. Generate a sync pulse following search time and prior to readout during each burst period.
c. Produce (at 100 pps) the clear-column pulses that clear the messages from the core array during readout of each burst period.
d. Cause continuous 1,300-pps shift pulses to be applied to the OSR only during readout of each burst period.
e. Generate a string of 13 busy bits once per second.

A detailed discussion of each of the timing circuits, 13 counter, 25 counter, and G/A-FD control circuits is contained in the following paragraphs.

2.4.2 13 Counter

The 13 counter, shown in figure 3–6, is a 13-core core shift register (CSR) used as a ring counter which is cleared, primed, and then continuously stepped at 1,300 pps. This counter is shared by both the G/A-FD and BOMARC storage sections. Individual outputs from this counter step the 25 counter, generate a sync pulse, and end search time. At the start of Output System operation after a shutdown or test operation, the pulse generator in the output control element sends a reset-and-prime pulse (at OD 4 time) to the 13 counter. This reset-and-prime pulse is applied as a set pulse to the 13-counter shift flip-flop which is cleared by successive OD 3 pulses. Since the reset-and-prime pulse occurs at OD 4 time and the 13-counter shift flip-flop is cleared at OD 3 time, a 7.5-μsec (OD 4 to OD 3) pulse is developed. This 7.5-μsec pulse is applied to the core shift driver (CSD) circuits which clear the 13 counter.

The reset-and-prime pulse from the pulse generator in the output control element is also applied to the 25 counter. Thus, each reset-and-prime pulse is simultaneously received at OD 4 time by both the 13 and 25 counters. The 25 counter produces a 25-μsec prime-13-counter pulse at the next OD 3 time after receipt of the reset-and-prime pulse, corresponding to the end of the 7.5-μsec 13-counter-clear pulse. This prime-13-counter pulse is applied to a core prime circuit in the 13 counter which drives the first core of the 13 counter to the 1 state.

Successive OD 2–13 pulses, which occur at the rate of 1,300 pps, each synchronized with an OD 2 pulse, are sent from the pulse generator in the output control element, through the 25 counter, through test equipment relay contacts in the output control element, to the 13 counter. After passing through the 25 counter, the OD 2–13 pulses are relabeled gated-13-CSR-shift pulses. These pulses are unchanged by the 25 counter, except that one pulse is suppressed every 25-counter cycle. (Refer to 2.4.3.) Each gated-13-CSR-shift pulse is applied as a set pulse to the 13-counter shift flip-flop, which is, in turn, cleared by successive OD 3 pulses. Therefore, for each combination of an OD 2–13 gated-13-CSR-shift pulse and an OD 3 pulse, a 2.5-μsec 13-counter-shift pulse is produced. These 2.5-μsec 13-counter-shift pulses are generated at the same rate as the OD 2–13 pulses (1,300 pps). Starting at the first OD 2 time following the fall of the prime-13-counter pulse at OD 1 time, successive 13-counter-shift pulses shift the 1 primed into the first core through the 13 counter.

Transferring the 1 from one core to another produces a 13-counter-output pulse. Each 13-counter-output pulse is labeled according to the numerical position of the core in the 13 counter that originates the output pulse. For example, after the application of the first 13-counter-shift pulse to the 13 counter, the 1 is shifted from core 1 to core 2 and a 13-counter-equals-1 pulse is generated. Thus, as the 1 is shifted through the 13 counter, 13 individual pulses are generated. These pulses are labeled 13-counter-equals-1 through 13-counter-equals-13, respectively.

As each 13-counter-equals pulse is produced, it is sent over a separate line to the test equipment section in

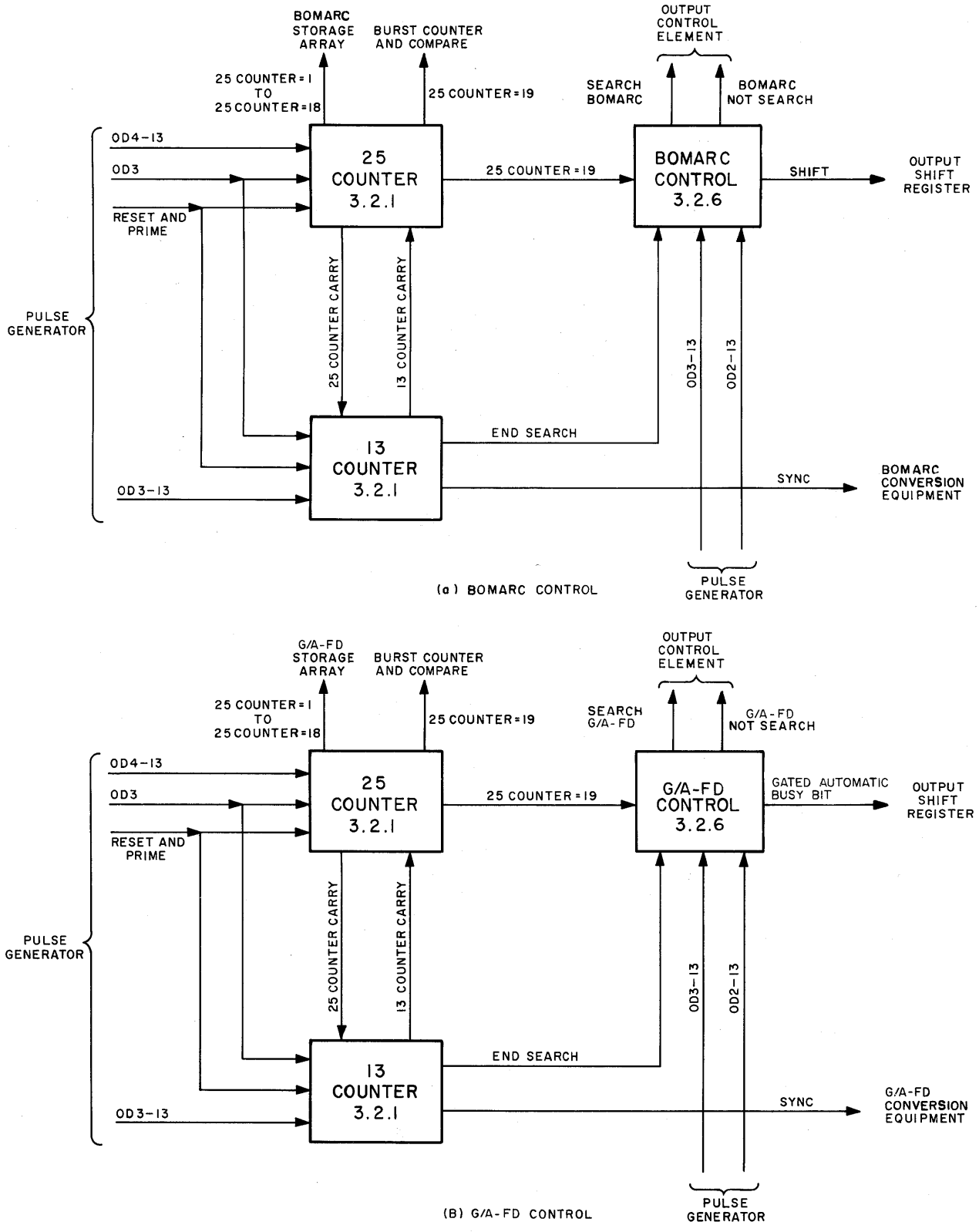


Figure 3–5. G/A-FD and BOMARC Control Circuits (3.2.1), Block Diagram

the output control element. The test equipment section utilizes these pulses as aids in performing test operations involving the G/A-FD storage section. Certain 13-counter-equals pulses are also used to generate controlling pulses as explained below.

The 13-counter-equals-7, -11, and -13 pulses are applied as conditioning levels to GT's 5, 3, and 1, respectively, and serve to control the passage of OD 3–13 pulses through these gates. An OD 3–13 pulse occurring at 13-counter-7 time (that is, the time when a 13-counter-equals-7 pulse is generated) passes through GT 5 and is applied to GT 4. An OD 3–13 pulse occurring at 13-counter-11 time passes through GT 3 and is applied to GT 2. Gates 4 and 2 are conditoned only dur-

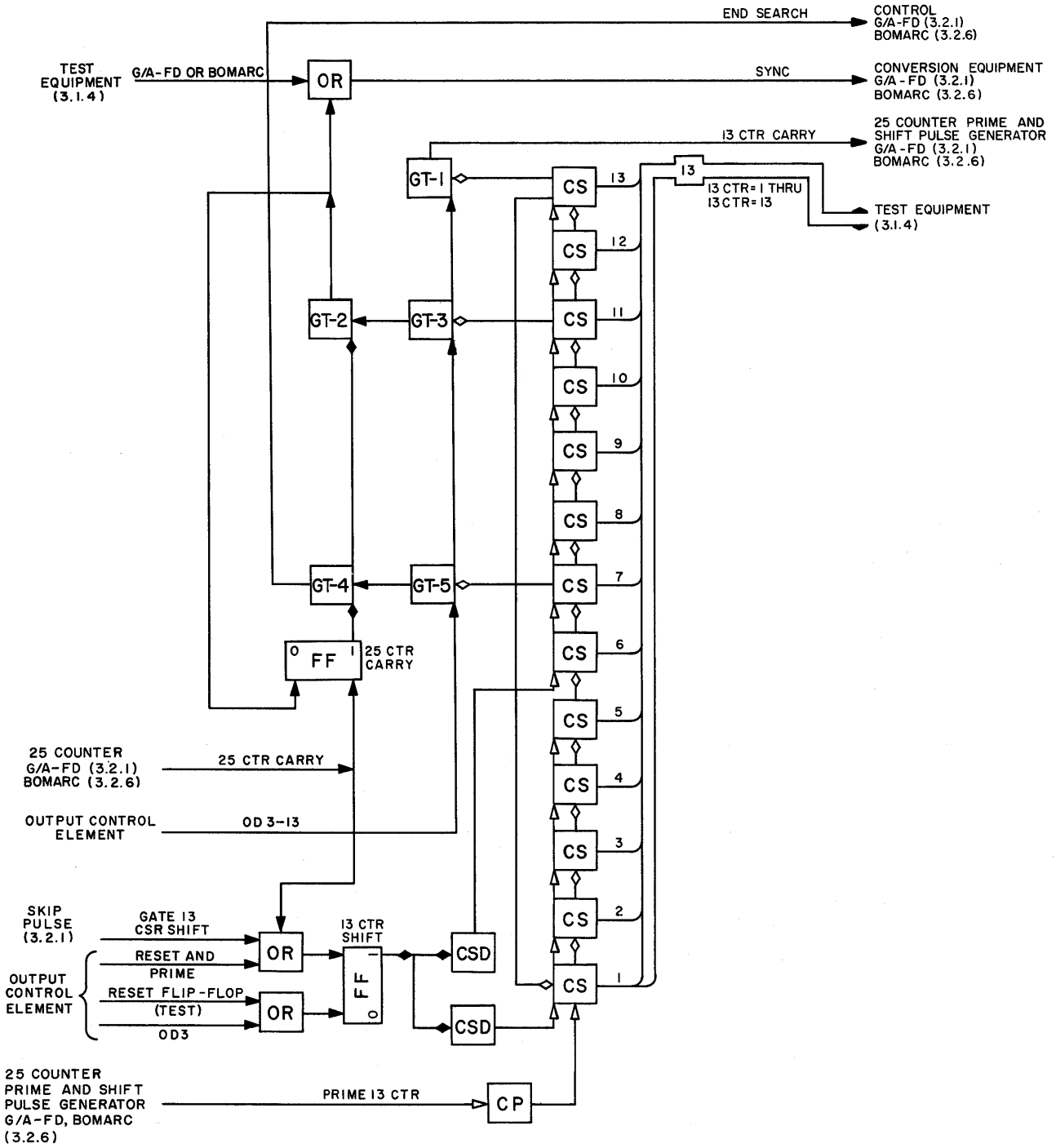


Figure 3–6. G/A-FD and BOMARC 13 Counter (3.2.1), Simplified Logic Diagram

ing 25-counter-25 time. The output of GT 4 is therefore a standard pulse synchronized with an OD 3 timing pulse, occurring when a 13-counter-equals-7 pulse is generated during 25-counter-25 time. This pulse is sent to G/A-FD control (fig. 3–10) as an end-search pulse. (Refer to 2.4.4.) Similarly, the output of GT 2 is a standard pulse synchronized with an OD 3 timing pulse, occurring when a 13-counter-equals-11 pulse is generated during 25-counter-25 time. This pulse is used in the 13 counter and is also sent to the G/A-FD conversion equipment (fig. 3–19) as a G/A-FD sync pulse.

In order to generate the end-search pulse and the G/A-FD sync pulse just discussed, GT's 2 and 4 must be conditioned for the duration of the 25-counter-equals-25 interval. This is effected by the action of the 25-counter-carry flip-flop. This flip-flop is set at 25-counter-25 time by a 25-counter-carry pulse and produces a level on its 1 side which is used to condition GT's 2 and 4. The flip-flop is cleared by the next 13-counter-equals-11 pulse, thereby lowering the level applied to the gates. In this way, GT's 2 and 4 are conditioned during the interval between 13-counter-1 and 13-counter-11 time, when this interval occurs during 25-counter-25 time.

The 13-counter-equals-13 pulse is used to condition GT 1 at 13-counter-13 time. An OD 3–13 pulse occurring at this time passes through GT 1 and is sent to the 25-counter-prime and shift pulse generator (fig. 3–7) as a 13-counter-carry pulse. Since the 13 counter is stepped at 1,300 pps, a 13-counter-carry pulse occurs once per 13 shift pulses or at the rate of 100 pps (13/1,300). Consequently, 13-counter-carry pulses are sent to the 25 counter at 100 pps.

Simultaneously with the generation of each 13-counter-carry pulse, the 1 is transferred from core 13 to core 1. Since the 13-counter-shift pulses are generated continuously, and since after 13 shifts the 1 is returned to core 1, the 13 counter maintains a continuous serial count of each group of 13 shift pulses.

At the end of each burst period, 25-counter-25 time, a 25-counter-carry pulse (OD 4–13) is applied to the 13-counter shift flip-flop. The combination of this pulse and the following OD 3 pulse generates a 7.5-μsec shift pulse which clears the 13 counter. The 13 counter is then primed by the 25 counter (refer to 2.4.3.), after which its shifting is resumed.

2.4.3 25 Counter

The 25 counter is primarily a 25-core shift register stepped at 100 pps which is used to record the passage of time during each G/A-FD burst period in steps of 1/100 second. The 25-counter outputs are used to control various functional operations performed in the G/A-FD storage section during each burst period. At the start of operation of the central, after a shutdown or following a test operation, the 25 counter receives a reset-and-prime pulse from the pulse generator in the output control element. This pulse prepares the 25 counter for shifting operation by causing it to be cleared and then primed prior to the application of shift pulses. The manner in which the 25 counter is cleared and primed is discussed in the following text. During the following discussion, refer to figure 3–7 and the associated timing chart (fig. 3–8).

The reset-and-prime pulse, which occurs at OD 4 time, is applied as a set pulse to the 25-counter shift flip-flop shown in figure 3–7. The level developed by the 1 side of the 25-counter shift flip-flop conditions GT 2 and is also applied to the 25-counter CSD's shown in figure 3–9. Successive OD 3 pulses are applied to GT 2 (fig. 3–7) sensing the 25-counter shift flip-flop output. Since the 25-counter shift flip-flop is set at this moment by the reset-and-prime pulse, the following OD 3 pulse is now passed through GT 2 and clears the 25-counter shift flip-flop. Thus, the 1 side of the 25-counter shift flip-flop is up from OD 4 until the next OD 3, an interval of 7.5. μsec. The CSD's apply this 7.5-μsec level to the 25-counter, thus clearing the register.

The OD 3 pulse that passes GT 2, in addition to

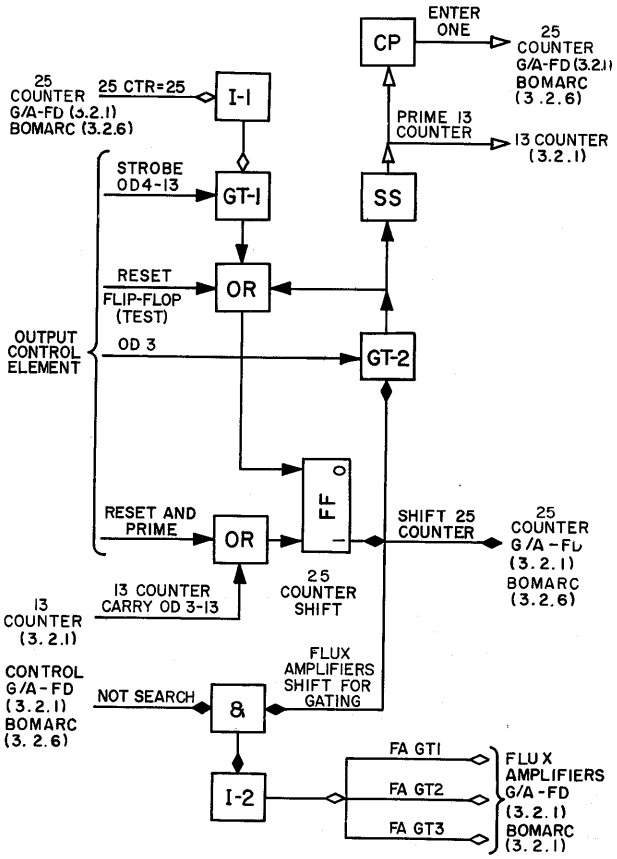


Figure 3–7. G/A-FD and BOMARC 25-Counter Prime and Shift Pulse Generator (3.2.1, 3.2.6), Simplified Logic Diagram

clearing the 25-counter shift flip-flop, also triggers a single-shot multivibrator. This single-shot multivibrator generates a 25-μsec signal which is sent to the 13 counter as a prime-13-counter signal and is also applied to a core prime circuit within the 25 counter. The core prime circuit applies the 25-μsec pulse, labeled enter-1, to core 1 of the 25 counter, setting it to 1. Therefore, at the completion of the above-mentioned steps, the 25-counter has been cleared and primed. These operations are initiated by receipt of a reset-and-prime pulse.

The 25-counter shift operation is continuous and is composed of successive 25-counter cycles, each of which is 0.25 second in duration, the length of a G/A-FD burst period. Although a G/A-FD burst period and a 25-counter cycle are of the same duration, they start at different times. A 25-counter cycle is initiated when the first core of the counter is primed. A burst period starts in the midst of a 25-counter cycle when the 1 primed into the counter is transferred from the 19th to the 20th core. This is referred to as 25-counter-19 time.

The reason for the difference in the starting times of a 25-counter cycle and a G/A-FD burst period is as follows. After a shutdown or test operation, the core array must be free of unwanted data upon initiation of active operation. This is accomplished by having a readout operation occur, during which the core array is cleared prior to the initiation of the first burst period. Readout occurs from 25-counter-equals-1 through 25-counter-equals-18. Initiation of a burst period at 25-counter-equals-19 ensures that the core array is always cleared at the start of active operation. Upon completion of a 25-counter cycle, the 25 counter automatically recycles. During a 25-counter cycle, the 1 primed into the counter is shifted at 100 pps. After 25 shifts, a 25-counter cycle is completed and the counter is automatically cleared and primed in preparation for the following cycle. A step-by-step discussion of a 25-counter cycle follows. (See fig. 3–8.)

Continuous 13-counter-carry pulses are received from the 13 counter at the rate of 100 pps and applied as set pulses to the 25-counter shift flip-flop shown in

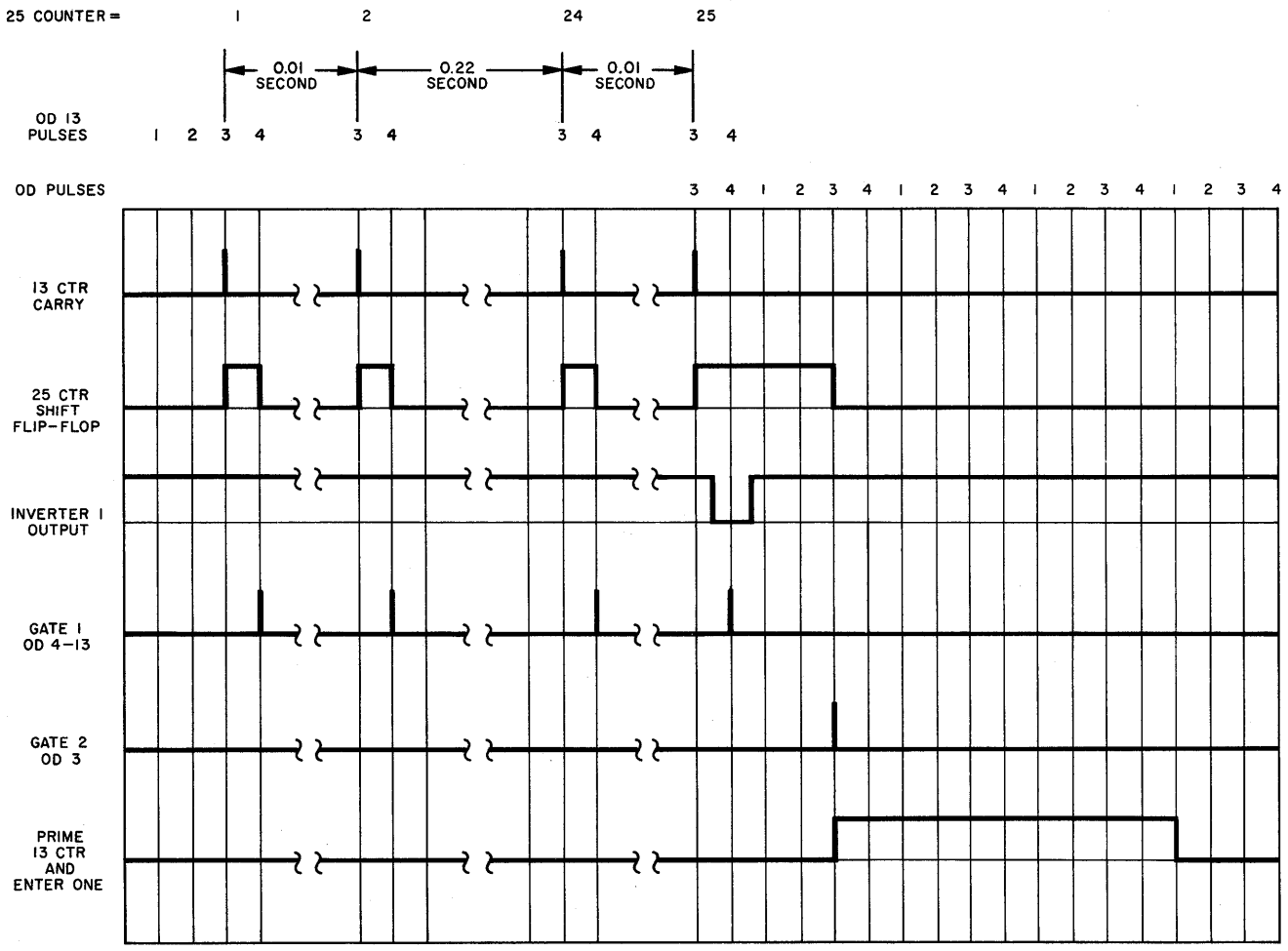


Figure 3–8. Shift, Clear, and Prime 25 Counter, Timing Chart

figure 3–7. Each 13-counter-carry pulse is received at an OD 3–13 time. The 25-counter shift flip-flop may be cleared by an output from either GT 2 or GT 1. Gate 1 is conditioned by inverter 1, which produces a down level whenever it is pulsed. This inverter is pulsed by the output from core 25 of the CSR. Consequently, the output of inverter 1 remains up until the 1 that is shifted through the 25 counter is shifted out of the 25th core. This occurs at 25-counter-25 time, the time the register is shifted for the 25th time. Therefore, at all times except 25-counter-25 time, GT 1 is conditioned and passes successive OD 4–13 pulses, each of which clears the 25-counter shift flip-flop. At 25-counter-25 time, inverter 1 causes GT 1 to inhibit one OD 4–13 pulse, causing the 25 counter to automatically prime itself. This will be covered in detail later in this section.

For each combination of a 13-counter-carry pulse followed by an OD 4–13 pulse, the 1 side of the 25-counter shift flip-flop is up for 2.5 μsec. The 2.5-μsec level thus developed is applied to the CSD shown in figure 3–9 and causes the 1 primed into the 25 counter to be shifted one core. The 13-counter-carry pulses

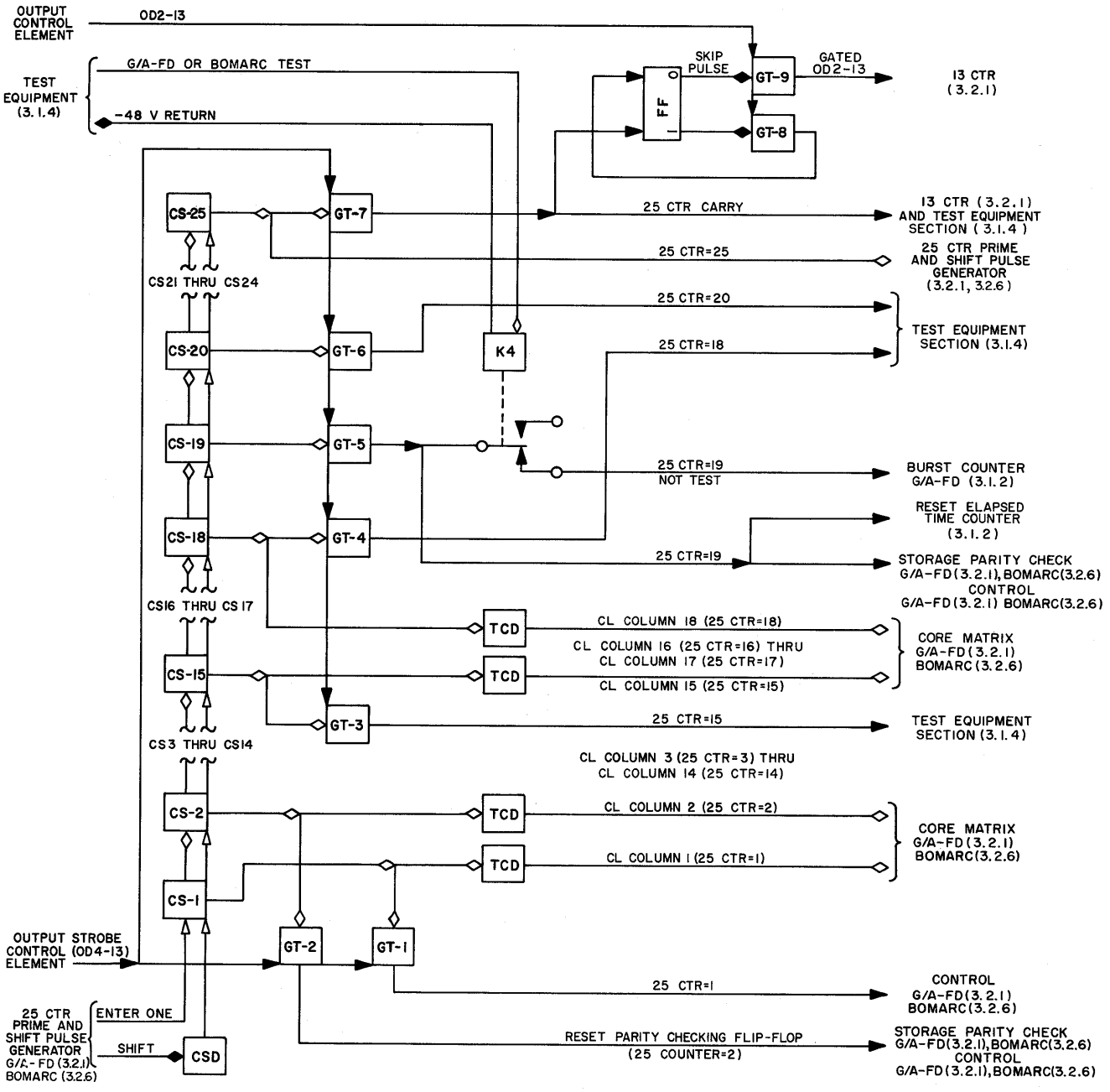


Figure 3–9. G/A-FD and BOMARC 25 Counter (3.2.1), Simplified Logic Diagram

occur at 100 pps and consequently the 2.5-μsec shift pulses are developed at the same rate. Therefore, the 1 is shifted through the register (fig. 3–9) at 100 pps. In addition, the 2.5-μsec shift pulses are transferred through an AND circuit (fig. 3–7) when a G/A-FD not-search level is up, is inverted, and then employed to gate the FA's. The FA's are turned on when this gating level is down; that is, during the time that the 25 counter is shifted. (Refer to 2.5.2.)

As the 1 is transferred from one core to the next, a 25-counter-equals pulse is generated. These 25-counter-equals pulses are generated in sequence from 1 through 25 at 100 pps. The first 18 of the 25-counter-equals pulses are each applied to a thyratron core driver (TCD). (See fig. 3–9.) The TCD produces clear-column pulses used to clear successive columns in the G/A-FD core storage. Since 25-counter-equals pulses are produced at 100 pps, the successive clear-column pulses are produced at the same rate. The 18 clear-column pulses are labeled clear-column-1 through clear-column-18, respectively. The interval from 25-counter-equals-1 through 25-counter-equals-18 is the readout interval.

The 25-counter-equals pulses are also used to control other G/A-FD storage operations. The 25-counter-equals-1, -2, -15, -18, -19, -20, and -25 pulses are used to condition GT's 1 through 7, respectively, in the 25 counter. The OD 4–13 timing pulses are applied to each of these gates. An OD 4–13 pulse occurring at a time when one of these gates is conditioned by a 25 counter-equals pulse will be passed by the particular gate and sent to other circuits as a control or test pulse. The distribution of these pulses is specified in the following paragraphs.

An OD 4–13 pulse occurring at 25-counter-1 time is sent to the G/A-FD control as a 25-counter-equals-2 pulse, where it is used to end the transmission of busy bits. (Refer to 2.4.4.) This pulse is also sent to the storage parity checking circuit (fig. 3–15) where it is used in the busy bit check. (Refer to 2.6.2.)

An OD 4–13 pulse occurring at 25-counter-2 time is sent to the G/A-FD control as a 25-counter-equals-2 pulse, where it is used to end the transmission of busy bits. (Refer to 2.4.4.) This pulse is also sent to the storage parity checking circuit (fig. 3–15) where it is used in the busy bit check. (Refer to 2.6.2.)

The OD 4–13 pulses occurring at 25-counter-15, -18, and -20 are sent to the test equipment section where they are utilized in performing test procedures.

An OD 4–13 pulse occurring at 25-counter-19 time is sent to the following circuits:

a. To the G/A-FD control as a start-search pulse, where it is used to initiate the search G/A-FD level.
b. To the storage parity checking circuit as a 25-counter-equals-19 pulse, where it is used in the storage parity check. (Refer to 2.6.3.)
c. To the elapsed-time counter (fig. 3–18) as a 25-counter-equals-19 pulse, where it is used to reset the counter. (Refer to 2.7.3.)
d. Through the contacts of relay K4 to the G/A-FD burst counter (fig. 3–16) as a 25-counter-equals-19 pulse. During normal operation, relay K4 is de-energized and this pulse is used to step the burst counter. (Refer to 2.7.2.) Relay K4 is energized only during test operation, at which time the burst counter is prevented from being stepped.

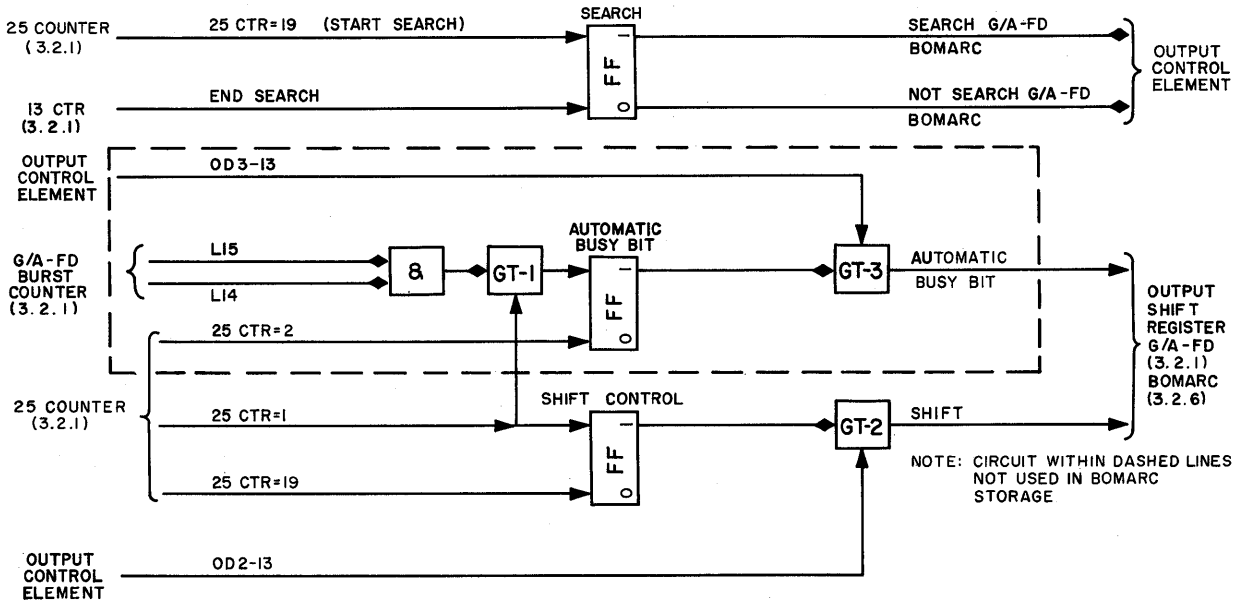


Figure 3–10. G/A-FD and BOMARC Control (3.2.1, 3.2.6), Simplified Logic Diagram

An OD 4–13 pulse occurring at 25-counter-25 time is sent to the following circuits as a 25-counter-carry pulse:

a. To the 13 counter (fig. 3–6), where it is used to develop a clear pulse and to condition GT's 2 and 4 in this counter. (Refer to 2.4.2.)
b. To the skip pulse flip-flop in the 25 counter (fig. 3–9) where it is used to suppress an OD 2–13 pulse. (Explained in detail later in this section.)
c. To the test equipment section where it is used in test operations.

In addition to its previously explained gating function, the 25-counter-equals-25 pulse is applied to inverter 1 within the 25-counter prime and shift pulse generator (fig. 3–7). The output of this inverter is always positive except at 25-counter-25 time when the output level falls because of the 25-counter-equals-25 pulse. This normally positive level is applied to GT 1 as a conditioning level, allowing the OD 4–13 pulses to pass this gate and clear the 25-counter shift flip-flop. At 25-counter-25 time, the conditioning level falls and the succeeding OD 4–13 pulse is prevented from clearing the 25-counter shift flip-flop. Consequently, the level developed by the 25-counter shift flip-flop, which shifted the 25-core shift register and thereby caused the generation of the 25-counter-equals-25 pulse, remains up after the OD 4–13 pulse. The next OD 3 pulse, 10 μsec after the setting of the 25-counter shift flip-flop by a 13-counter-carry pulse, passes GT 2, since its conditioning level is up, clears the 25-counter shift flip-flop, and triggers the single-shot multivibrator. The 10-μsec level thus developed by the 25-counter shift flip-flop clears the 25 counter. The 25-μsec pulse developed by the single-shot multivibrator is sent to the 13 counter as a prime-13-counter pulse and is also applied to the core prime circuit as an enter-1 pulse which primes core 1 of the 25 counter. Therefore, at each 25-counter-25 time, the 25 counter is cleared and primed automatically. Stepping of the 25 counter then continues, thereby initiating a new 25-counter cycle.

A secondary function of the 25 counter is to control the flow of OD 2–13 pulses sent from the pulse generator in the output control element to the 13 counter. These OD 2–13 pulses, after passing through the skip-pulse circuit of the 25 counter (fig. 3–9), are relabeled gated-13-CSR-shift pulses. It is required that the 25-counter suppress the first OD 2–13 pulse received after the 25-counter-carry pulse is generated. The successive OD 2–13 pulses are applied simultaneously to GT 9 and GT 8, which are conditioned by the 0 and 1 side, respectively, of the skip-pulse flip-flop. Normally, the 0 side of the skip-pulse flip-flop is up, conditioning GT 9, which passes the OD 2–13 pulses to the 13 counter as gated-13-CSR shift pulses. However, the 25-counter-carry pulse, when developed, sets the skip-pulse flip-flop, which removes a conditioning level from GT 1 and applies a conditioning level to GT 3. The following OD 2–13 pulse is then passed through GT 3. This OD 2–13 pulse clears the skip-pulse flip-flop and returns the conditioning level to GT 1. In this manner, the first OD 2–13 pulse that occurs after the 25-counter-carry pulse is developed is suppressed in the 25 counter.

2.4.4 Control

The G/A-FD control circuit produces two levels which indicate the start and end of search time and also controls the pulses which cause shifting of data bits to the transmission equipment. In addition, it generates a string of automatic busy bits once per second. The G/A-FD control circuit shown in figure 3–10 contains a search flip-flop which is set by a start-search pulse that occurs at 25-counter-19 time. This pulse raises the 1 side of the search flip-flop, developing a search G/A-FD level. The search G/A-FD level is sent to the output control element, informing it that the G/A-FD storage section can receive data. Approximately 65 ms after the setting of the search flip-flop, an end-search pulse is received from the 13 counter, which clears the search flip-flop. This terminates the search level and develops a G/A-FD nonsearch level which is sent to the output control element. This level informs the output control element that search time is completed and, thus, that the flow of data to the G/A-FD storage section should be halted.

The G/A-FD control circuit also governs the flow of shift pulses sent to the OSR circuit. Successive OD 2–13 pulses are applied to GT 2 within the G/A-FD control circuit. The shift flip-flop in the G/A-FD control circuit is set by a 25-counter-equals-1 pulse denoting the start of readout, and cleared by a 25-counter-equals-19 pulse which signifies the end of readout and the initiation of search time for the following burst period. Gate 2 is conditioned by the 1 side of the shift flip-flop and, therefore, upon receipt of a 25-counter-equals-1 pulse, successive OD 2–13 pulses are passed to the OSR as shift pulses. Therefore, shift pulses are supplied to the OSR between generation of 25-counter-equals-1 and 25-counter-equals-19 pulses, which is the duration of readout time.

The G/A-FD control circuit contains an automatic busy bit flip-flop which is set by the 25-counter-equals-1 pulse once per second. This occurs because two levels developed by the burst counter circuit labeled burst counter L15 and burst counter L14, respectively, are up together only once per second. Both of these levels are applied to a 2-way AND circuit whose output conditions GT 1. Gate 1 is sensed by each 25-counter-equals-1

pulse. Therefore, once per second when L14 and L15 are up together, GT 1 is conditioned and passes a 25-counter-equals-1 pulse. This pulse sets the automatic busy bit flip-flop (G/A-FD only). The 1 side of the automatic busy bit flip-flop conditions GT 3, which is pulsed by OD 3–13 pulses. Gate 3 now passes successive OD 3–13 pulses to the OSR. The automatic busy bit flip-flop is then cleared by the following 25-counter-equals-2 pulse. Since there is 1/100-second interval between successive 25-counter-equals pulses and since OD 3–13 pulses occur at 1,300 pps, a string of 13 OD 3–13 pulses is sent to the OSR as automatic busy bits. A timing sequence of the essential operations performed in the control circuits is summarized in figure 3–11.

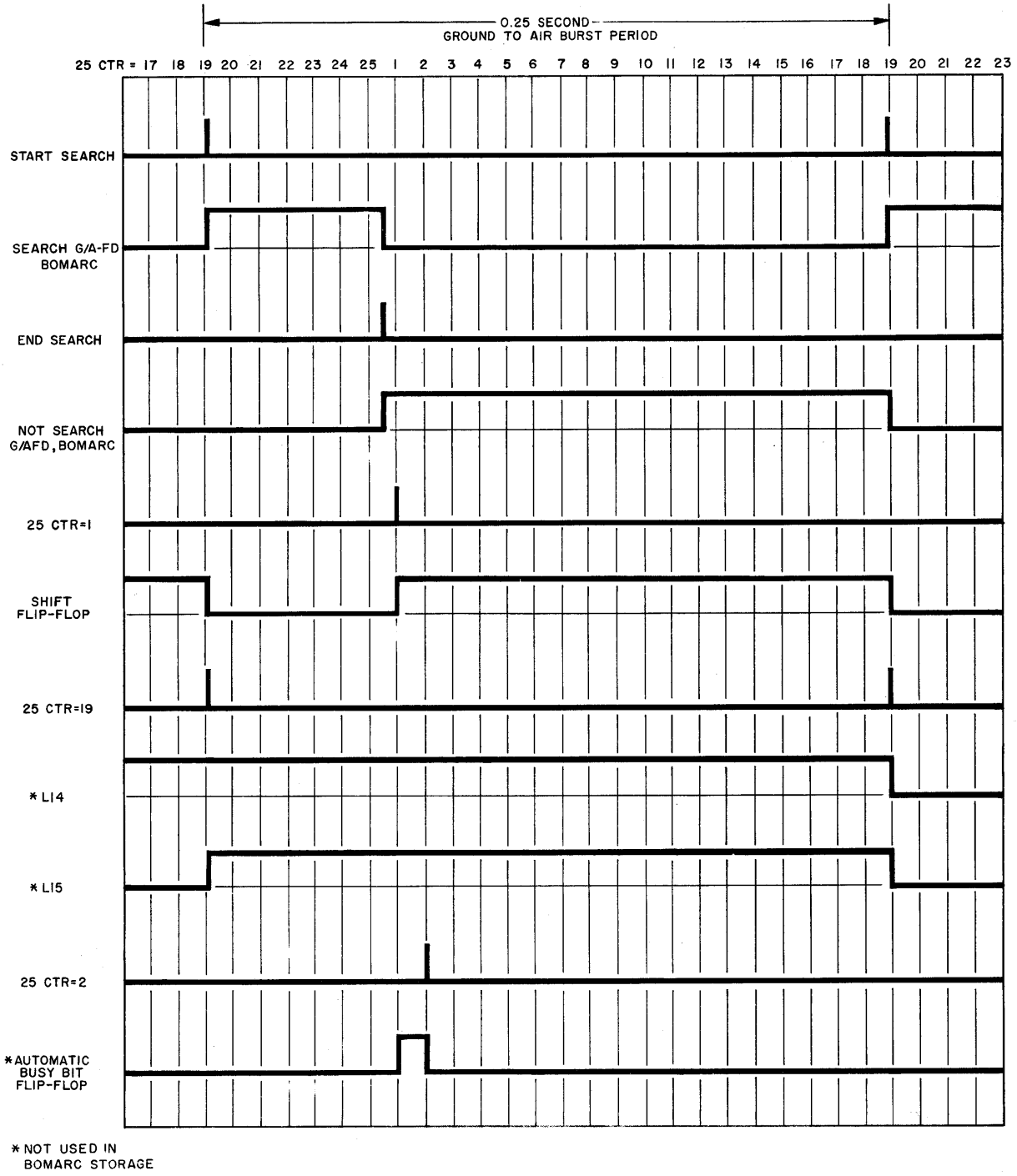


Figure 3–11. G/A-FD and BOMARC Control, Timing Chart

2.5 READOUT (G/A-FD, BOMARC)

2.5.1 General

Readout of the core array commences 5 ms after the termination of search time during each G/A-FD burst period. During readout, the two G/A-FD messages stored in the array are transferred through FA's to the OSR. (See fig. 3–12.) The messages are then serially transferred from the OSR at 1300 pps to the G/A-FD conversion equipment. The messages are transmitted in an interleaved fashion.

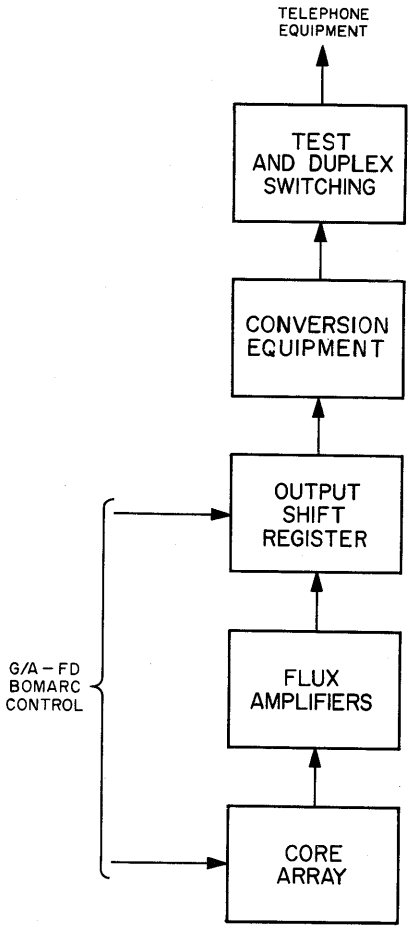


Figure 3–12. G/A-FD or BOMARC Readout, Block Diagram

2.5.2 Core Array Readout

The G/A-FD messages are read out of the core array by columns; 18 columns are employed in the core array. (See fig. 3–3,B.) During readout, these columns are pulsed serially, column 1 through column 18, by clear-column pulses applied by the TCD's located in the 25 counter. These clear-column pulses occur at 100 pps; that is, one column per 10 ms. Each time that a column is pulsed, the 26 bits stored in its cores are shifted from the core array in parallel to the FA's. The 26 bits from each column are composed of one bit from each of the 26 output words, 13 bits from each of the two G/A-FD messages.

The information contained in each of the 26 arrays of the G/A-FD core storage is applied to an FA shown in figure 3–13. A 1 bit is represented by a pulse, and a 0 bit is indicated by the absence of a pulse. Each FA is normally inoperative in order to prevent the amplification of noise and spurious signals. The amplifiers are turned on, however, at the appropriate time by the application of gating levels 1, 2, and 3, shown in figure 3–13. These gating levels are 2.5-μsec negative pulses produced in the 25 counter simultaneously with each shift of this counter that occurs during readout time. (Refer to 2.4.3.) Since each shift of the 25 counter

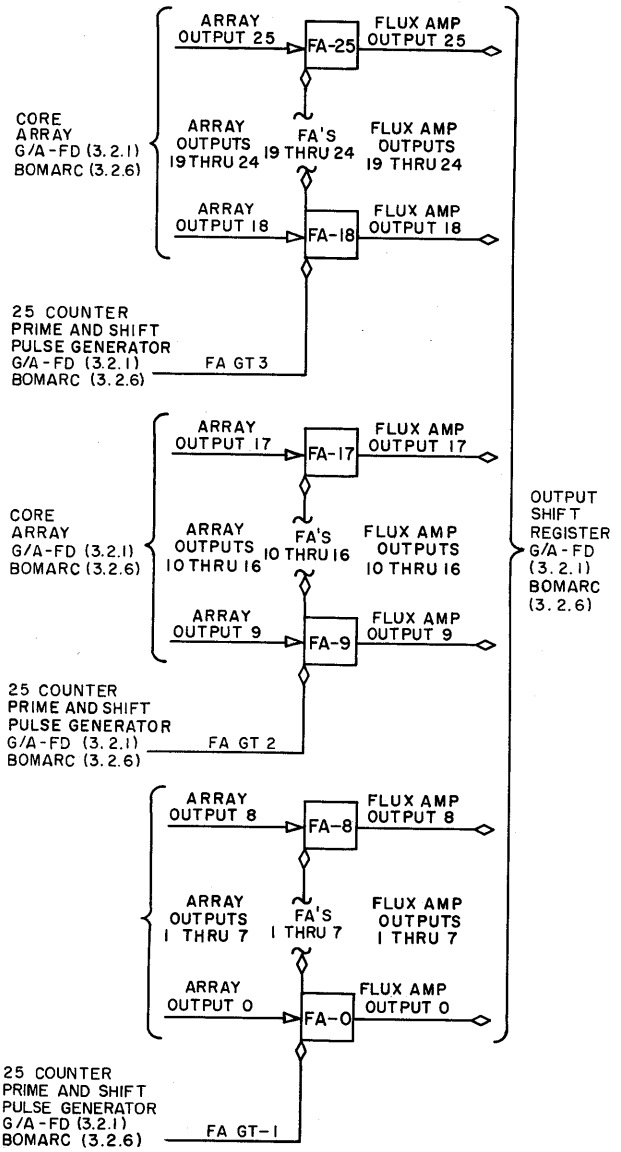


Figure 3–13. G/A-FD and BOMARC Flux Amplifiers (3.2.1, 3,2,6), Simplified Block Diagram

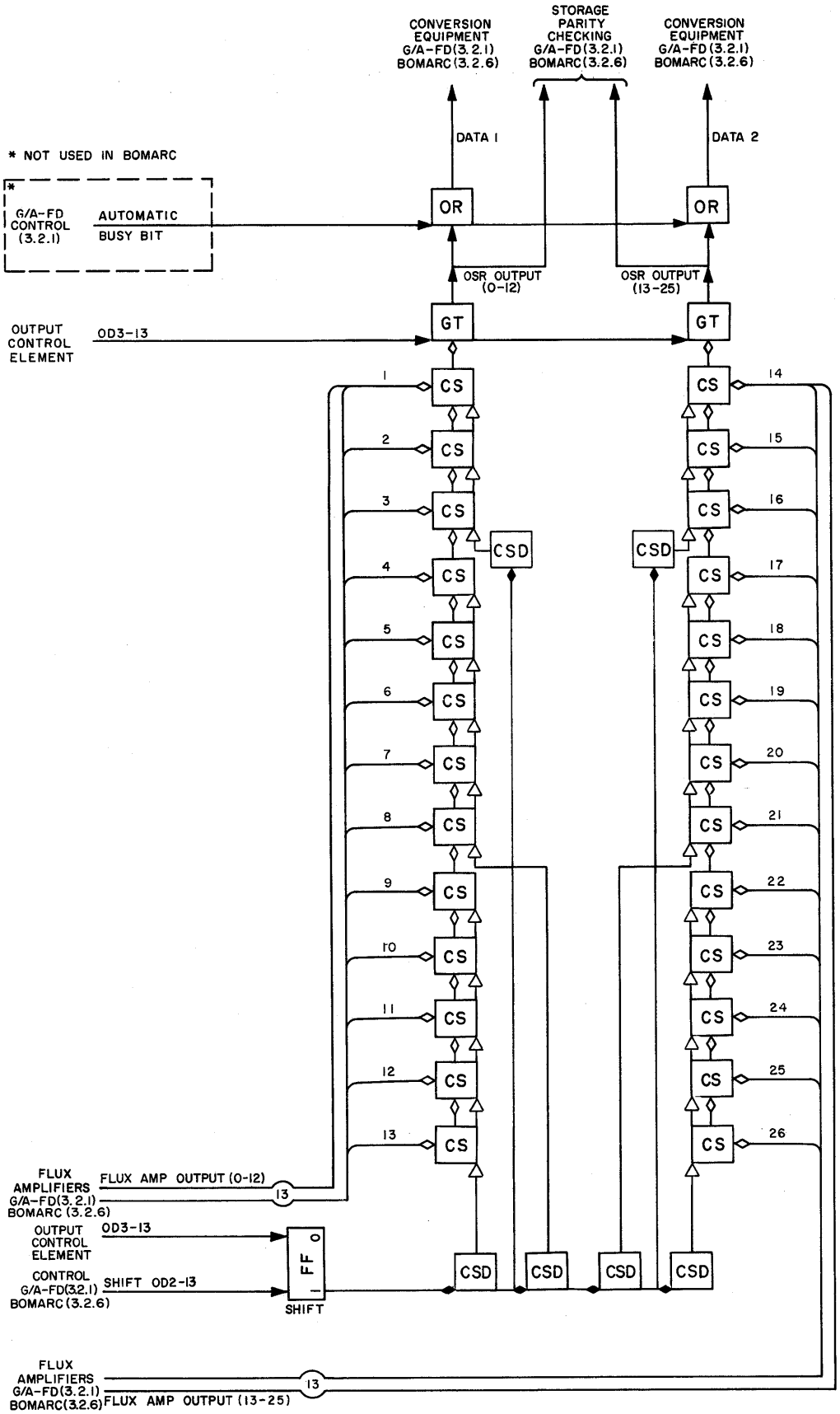


Figure 3–14. G/A-FD and BOMARC Output Shift Register (3.2.1, 3.2.6), Simplified Logic Diagram

produces a clear-column pulse which reads out a column of the core storage array, array outputs are applied to the FA's during the time that the gating level is applied and the FA's are operative.

After amplifying and stretching the array output pulses, the FA's send the pulses to the OSR (fig. 3–14) as FA outputs. The outputs from the FA's are sent over 26 lines labeled FA output 0 through FA output 25.

2.5.3 Output Shift Register (OSR)

During readout time, the OSR (fig. 3–14) receives successive groups of 26 FA outputs at the rate of 100 groups per second. Between receipt of successive groups of FA outputs, the register transfers the 26 bits of one group, in two 13-bit groups, to the G/A-FD conversion equipment. This is done at a rate of 1,300 pps.

The OSR consists primarily of two 13-core shift registers. The FA outputs 0 through 12, which are the output from the slot in the storage array that stores messages intended to be transmitted through data channel 1, are loaded into core 1 through core 13 of one 13-core shift register. Simultaneously, FA outputs 13 through 25, which are the outputs from the slot in the core storage array that stores messages intended to be transmitted through data channel 2, are loaded into cores numbered 14 through 26 of the other 13-core shift register. During readout time, the two 13-core shift registers receive new contents every 1/100 second.

During readout time, the OSR receives successive OD 2–13 shift pulses from the G/A-FD control circuit which are applied as set pulses to the shift flip-flop, which is cleared by successive OD 3–13 pulses from the pulse generator in the output control element. Therefore, for each combination of an OD 2–13 shift pulse followed by an OD 3–13 pulse, the shift flip-flop produces a 2.5-μsec level at the rate of 1,300 pps. These levels are applied to the CSD circuits in the OSR, causing the two 13-core shift registers to be shifted simultaneously at 1,300 pps.

Since the cores of the two 13-core shift registers are reloaded every 1/100 second by the FA outputs, and since these 13-core shift registers are continually shifted at 1,300 pps, there is a continual flow of pulses from cores 1 and 14 of the 13-core shift registers at the rate of 1,300 pps. These pulses condition one of two gates which are simultaneously pulsed by OD 3–13 pulses. The 2.5-μsec shift levels that cause shifting of the CSR are up from OD 2–13 until OD 3–13. Therefore, the outputs from cores 1 and 14, if they are 1 bits, are up at OD 3–13, at which time an OD 3–13 pulse is passed by the gate. The pulses passed by the two gates are applied to two OR circuits and, from these, sent to the G/A-FD conversion equipment (fig. 3–19) as G/A-FD data-1 and G/A-FD data-2 pulses, respectively. In addition, the pulses labeled OSR output (0–12) and OSR output (13–25) are sent to the storage parity checking circuit (fig. 3–15) where the messages are examined for errors. Automatic busy bits from the G/A-FD control circuit are also applied to the OR circuits in the OSR on their way to the G/A-FD conversion equipment.

The readout process interleaves the bits of one output word with the bits of each of the other output words in a G/A-FD message. Thus, successive bits of the same output word in a G/A-FD message are 13 bits apart as a G/A-FD message is transferred to the G/A-FD conversion equipment. The readout process is summarized in the following text.

A G/A-FD burst consists of two G/A-FD messages, each composed of 13 output words. Each G/A-FD message is stored in a separate slot of the G/A-FD core storage array. G/A-FD message 1 is stored in the slot composed of storage array registers 0 through 12, which individually stores output words 1 through 13. G/A-FD message 2 is stored in the slot composed of storage array registers 13 through 25, which individually stores output words 14 through 26. A G/A-FD message is transferred by column from the core array. A column contains one bit from each output word in the core array. The contents of each column are transferred in parallel to the OSR, which sends it serially to the G/A-FD conversion equipment. An output word is composed of 18 bits and there are 13 output words in a G/A-FD message. Therefore, 234 data bits (18 x 13) form a G/A-FD message. The relationship between the data bits in the G/A-FD message and the bits of the output words stored in the core array is shown in table 3–1.

2.6 MESSAGE CHECK (G/A-FD, BOMARC)

2.6.1 Purpose

Each G/A-FD message is examined as it is fed out of the G/A-FD storage section. This inspection consists of two checks: the busy bit check and the output parity check. Both checks are performed by the storage parity circuit and occur at different times during the readout interval of a burst period. The following text describes the busy bit and output parity checks.

2.6.2 Busy Bit Check

The busy bit check is made to assure that the number of busy bits transferred from the OSR is equal to the number of output words loaded into the G/A-FD core storage from the output control element. This is a partial check on the accuracy of the output word, since, during the read-in operation, one busy bit should have been generated and added to each output word by the output control element.

The busy bit check is performed by the storage parity checking circuit shown in figure 3–15. As shown in

this figure, the checking circuit is primarily composed of two flip-flops which are employed as simple counters indicating odd or even counts. The appropriate flip-flop is stepped by a G/A-FD slot pulse from the output control element each time that a word is loaded into a particular slot of the G/A-FD core storage. During readout of the first column of the core array, each flip-flop is fed each data bit of the appropriate G/A-FD message from the OSR output lines as these data bits are transferred from the OSR to the G/A-FD conversion equipment. The circuit then compares the number of pulses received from the output control element to the number received from the OSR and generates an alarm if the number of pulses differ. Detailed circuit operation is as follows.

The busy bit check is begun at 25-counter-19 time; that is, the start of search time for each G/A-FD burst period. If either flip-flop is in the set condition at this time, the gate tube will be conditioned and will pass the 25-counter-equals-19 pulse sent from the 25 counter. This pulse will clear the flip-flops. Each time that a word is now loaded into slot 1 or 2 of the G/A-FD core storage, a signal is sent to FF 1 or 2, respectively, stepping this flip-flop. This counting continues until the end of search time. At this time the core storage has received all the words addressed to it during the present burst period. The flip-flops in the storage parity check circuit indicate odd or even counts of the words loaded into the G/A-FD core storage slots.

The last part of the busy bit check occurs during the first 0.01 second of readout time. This is the time duration between the 25-counter-equals-1 and 25-counter-equals-2 pulses. The 25-counter-equals-1 pulse is applied to the G/A-FD core storage as a clear-column-1 pulse. This pulse clears column 1 and transfers its contents to the OSR. The first column in the G/A-FD core storage stores all of the busy bits in a G/A-FD burst. These busy bits, like the data bits which follow them, are shifted out of the OSR serially by slots. These bits are transferred simultaneously to the storage parity check circuit and G/A-FD conversion equipment. (Refer to 2.5.2.)

In the storage parity check circuit, the busy bits of each G/A-FD message from the OSR are applied to the flip-flops. In this manner, the busy bits are added to the odd or even count of the words which have been loaded into the G/A-FD core storage. The number of busy bits generated in the G/A-FD core storage should be equal

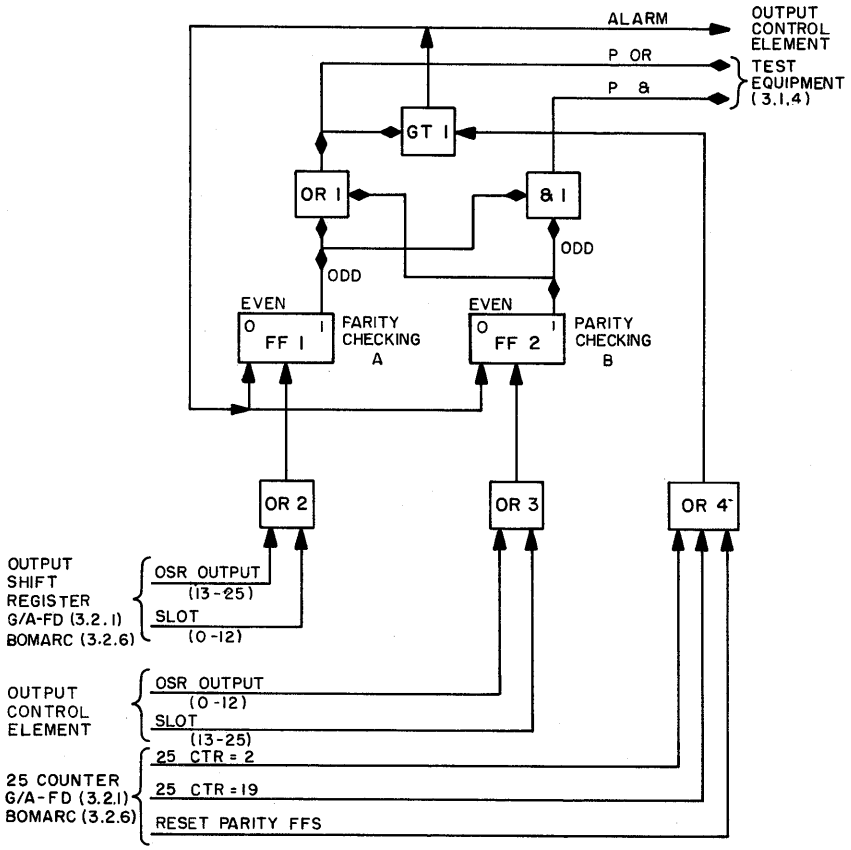


Figure 3–15. G/A-FD and BOMARC Storage Parity Checking (3.2.1, 3.2.6), Simplified Logic Diagram

to the number of words loaded into the G/A-FD core storage from the output control element. Therefore, the sum of the busy bits and word count should be even. If the count is odd, the 1 side of one or both flip-flops is up.

The 1 side of each flip-flop is connected to a 2-way OR circuit whose output is employed as a conditioning signal for a gate. This gate is pulsed by 25-counter-equals-2 and 25-counter-equals-19 pulses. The 25-counter-equals-2 pulse is received after a busy bit check and the 25-counter-equals-19 pulse is applied after an output parity check.

If the 1 side of one or both flip-flops is up at 25-counter-2 time, it is an indication that an incorrect number of busy bits is present in a G/A-FD message. The gate is conditioned as a result of an odd count and the 25-counter-equals-2 pulse is passed and sent to the alarm section as a G/A-FD alarm signal and to the flip-flop as a clear pulse.

2.6.3 Output Message Parity

The output parity check is made to assure that there are an even number of 1 bits present in each G/A-FD message. This is a partial check on the accuracy of the

TABLE 3–1. INTERLEAVING OF G/A-FD AND BOMARC MESSAGES

	MESSAGE	MESSAGE 1 CORE SHIFT REGISTER 1		MESSAGE 2 CORE SHIFT REGISTER 2	
CLEAR COLUMN	DATA BIT	OUTPUT WORD	BIT	OUTPUT WORD	BIT
1					
	1	1	1	14	1
	2	2	1	15	1
	3	3	1	16	1
	•	•	•	•	•
	12	12	1	25	1
	13	13	1	26	1
2					
	14	1	2	14	2
	15	2	2	15	2
	•	•	•	•	•
	26	13	2	26	2
3					
	27	1	3	14	3
	•	•	•	•	•
17					
	209	1	17	14	17
	•	•	•	•	•
	221	13	17	26	17
18					
	222	1	18	14	18
	•	•	•	•	•
	233	12	18	25	18
	234	13	18	26	18

message, since, during search time, each output word was modified by the output control element to contain an even number of 1 bits.

The output parity check is performed in the storage parity checking circuit (fig. 3–15) and follows the busy bit check. From 25-counter-equals-2 to 25-counter-equals-19, the data bits stored in the G/A-FD core storage are shifted out via the OSR and fed simultaneously to the storage parity check circuit and the test equipment section. In the storage parity checking circuits, the data bits are employed as stepping signals for the flip-flops.

The busy bit check normally results in an even count, and when it does not, the flip-flops are automatically cleared when the alarm is given. Therefore, the flip-flops are always clear at the start of the output parity check. A parity count for each output message is therefore carried out as the data bits are applied to the flip-flops from the OSR output lines. At 25-counter-19 time, the output parity count is complete. A correct parity or even number of 1's in each message is indicated by both flip-flops being clear.

Should a parity error be detected, the 1 side of one or both flip-flops will be up. This causes the gate to be conditioned and the 25-counter-equals-19 pulse is passed through the gate and sent to the alarm section as a G/A-FD alarm signal and to the flip-flops as a clear pulse.

2.7 BURST SEQUENCE AND TIMING (G/A-FD, BOMARC)

2.7.1 General

The G/A-FD burst counter and compare circuit and the burst number of the assigned G/A-FD message are the basic means employed to control the order and time of transmission of messages. The assigned burst numbers of each drum word are compared to the current contents of the burst counters. If the assigned burst number is equal to the contents of the G/A-FD burst counter, and if all other conditions are favorable, the word is accepted by the Output System.

To be sure that the message is transmitted in proper sequence and at the proper time, the Central Computer System assigns a burst number to each G/A-FD message to which the reading of the G/A-FD burst counter will be equal at the predicted transmission time. Each word of a burst is assigned the same burst number by the Central Computer System. To make it possible for the Central Computer System to determine this burst number, it is given access to the current readings of the G/A-FD burst counter and elapsed-time counter through the output-computer section of the output control element.

2.7.2 Burst Counter and Compare Circuit

This unit incorporates the G/A-FD and BOMARC burst counter and its associated compare circuit. The compare circuit is employed to compare the contents of the burst counter to the assigned burst number of each word loaded into the OB register of the output control element. The G/A-FD burst counter records the number of burst periods that have occurred during a program frame. The current contents of the counter indicate the burst period in effect at the present time.

Only six of the eight bits of the left-hand drum word assigned to the burst number are used in G/A-FD drum words. For this reason, the G/A-FD burst counter (fig. 3–16) is composed of only six flip-flops. These flip-flops make up a standard flip-flop counter having a scale of 64. This counter is stepped by each 25-counter-equals-19 pulse which corresponds to the start of search time for each burst period. This occurs every 0.25 second.

The 6-bit burst count produced is fed to the computer section of the output control element and the G/A-FD compare circuit. Bits L14 and L15 are also sent to the G/A-FD control where they are employed in the generation of the automatic busy bits (G/A-FD only). These automatic busy bits must be generated once per second. Since L14 and L15 are both up together once per second, they are utilized in controlling the generation of these bits. The burst counter can be cleared by a reset signal from the pulse generator located in the output control element. This signal is utilized only during a test function. In normal operation, the counter, after reaching its maximum limit of 64, is cleared by the next stepping pulse that is applied.

The G/A-FD compare circuit (fig. 3–17) forms the basis upon which bursts are accepted from the OB fields. The burst number of each output word is fed into the G/A-FD compare circuit, where it is then examined to ascertain whether it is equal to the contents of the burst counter. If the G/A-FD compare circuit finds that they are equal, it generates a G/A compare signal.

The G/A-FD compare circuit consists of 12 3-way AND circuits, 4 3-way OR circuits, and 1 inverter. Each AND circuit is fed a bit from the burst number and a bit from the burst count. Although these two bits are numerically equal, they represent opposite states; that is, one represents a 1 and the other represents a 0. Under these conditions, an AND circuit produces a signal only when corresponding bits of the assigned burst number and the current burst count are unequal. When they are equal, none of the 12 AND circuits produces an output.

The AND circuits are connected to three OR circuits which, in turn, are connected to a single OR circuit. Any output from an AND circuit passes through the OR's and is applied to an inverter.

The inverter generates a level which is normally in the up position. If a signal is applied to the inverter,

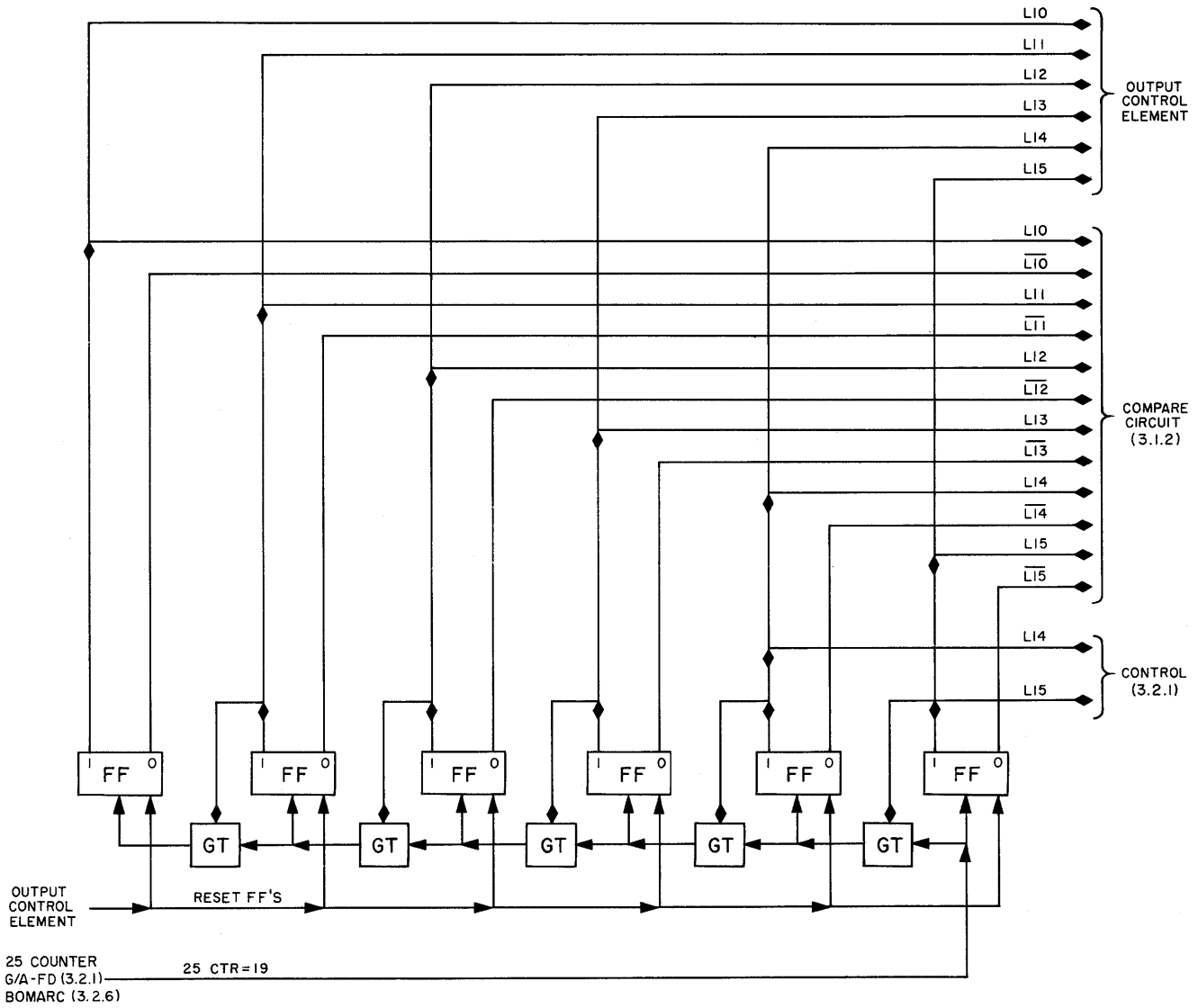


Figure 3–16. G/A-FD and BOMARC Burst Counter (3.1.2), Simplified Logic Diagram

the output will be down. Therefore, if the burst number and burst count are unequal, the AND circuits will pass at least one signal. This signal, which passes through the OR's is applied to the inverter, causing the output from the inverter to go down. Should the burst number be equal to the burst count, the inverter will not have a signal applied to it. It then produces a positive level which is sent to the output element as a G/A-FD compare signal.

2.7.3 Elapsed-Time Counter (G/A-FD Only)

This circuit records the time that elapses from the start of search time of one burst until the start of search time of the next. The elapsed-time counter consists of a 4-flip-flop counter having a scale of 16 and is used only in the G/A-FD storage section. A simplified logic block diagram of the elapsed-time counter is shown in figure 3–18. The counter is cleared by each 25-counter-equals-19 pulse, which indicates the start of search time. The elapsed-time counter is then stepped at the rate of 32 pps. The stepping pulses are fed to the elapsed-time counter from the pulse generator located in the output control element. A 4-bit binary output is produced by the elapsed-time counter and sent to the output control element, where it is made available to the Central Computer System. The Central Computer System program can determine the time that has elapsed during the present burst period by examining the current contents of the elapsed-time counter. The programmer utilizes this information in assigning burst numbers to future G/A-FD messages.

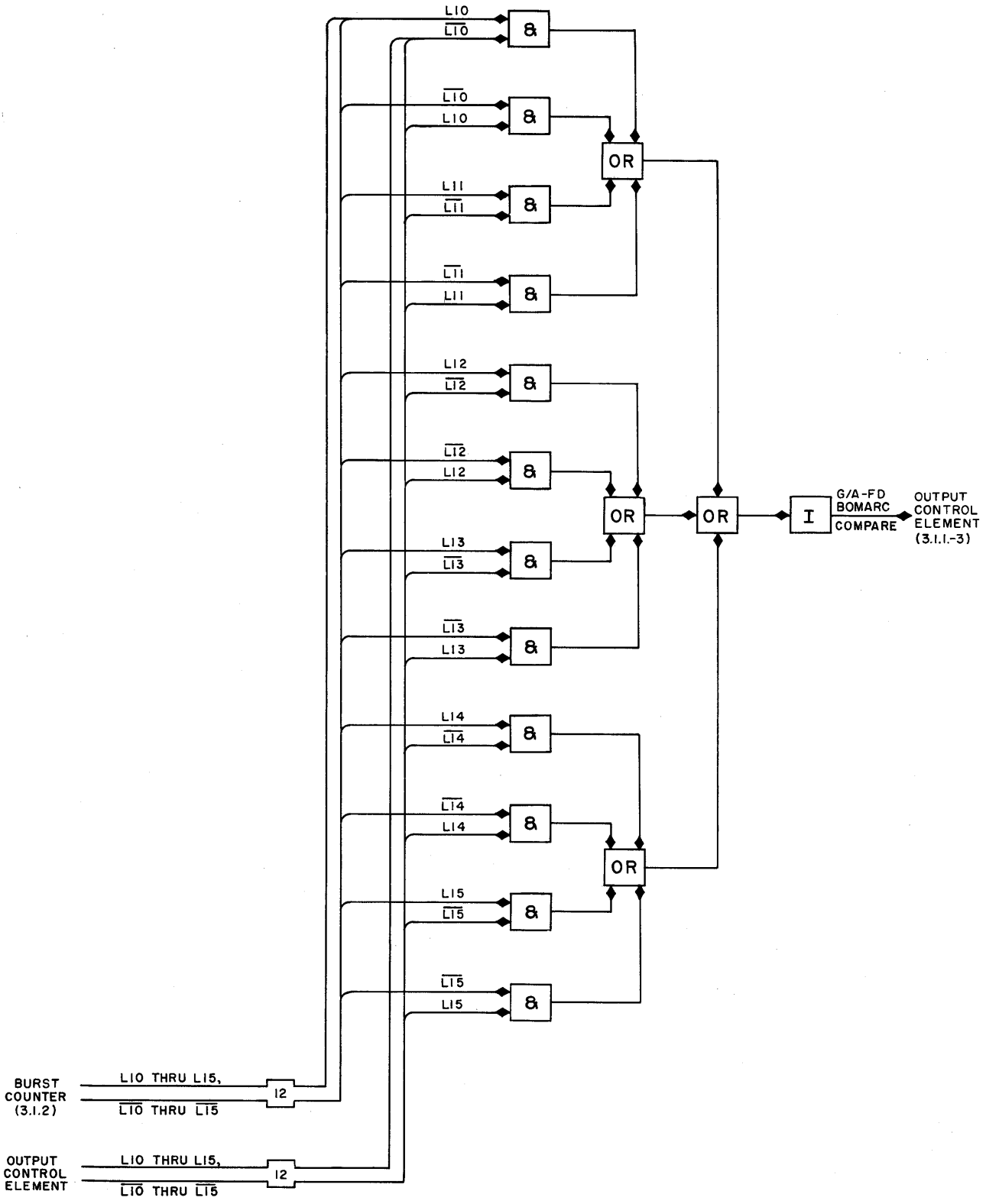


Figure 3–17. G/A-FD and BOMARC Compare (3.1.2), Simplified Logic Diagram

2.8 CONVERSION (G/A-FD, BOMARC)

2.8.1 General

Information leaving the G/A-FD OSR is sent to the conversion circuits before being fed through the switching circuits to the telephone transmission equipment. The conversion circuits convert the G/A-FD data and sync information, which consists of standard 0.1-μsec pulses, to a series of synchronized, gated, 1,300-cps sine waves. The information is modified in this manner to make it compatible with telephone company equipment requirements.

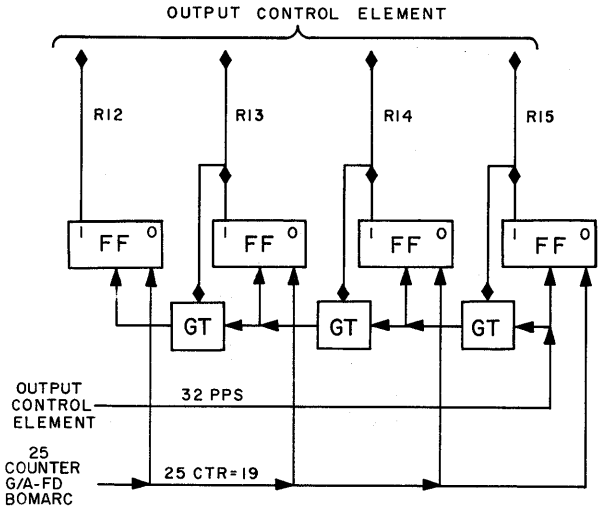


Figure 3–18. G/A-FD and BOMARC Elapsed-Time Counter (3.1.2), Simplified Logic Diagram

2.8.2 Conversion Equipment

2.8.2.1 General

This equipment contains two identical channels, one for each of the two G/A-FD messages. Each message channel contains a data conversion channel, an identical sync conversion channel, and a timing channel. The data and sync conversion channels perform the required conversion on their respective information inputs. The timing channel serves to match the timing signal, a 1,300-cps sine wave, to the telephone equipment, but does not modify its waveshape.

The two message channels are identical in operation. For this reason, the detailed operation of only one channel, the conversion channel for message 1 (fig. 3–19), is covered in the following paragraphs.

2.8.2.2 Data Conversion Channel

The G/A-FD and BOMARC data are made up of standard pulses at OD 3–13 time. The presence of a pulse represents a 1; the absence of a pulse, a 0. This data is applied to the G/A-FD output data channel 1 flip-flop. This flip-flop will be set by a G/A-FD data pulse and cleared by the following OD 2–13 timing pulse.

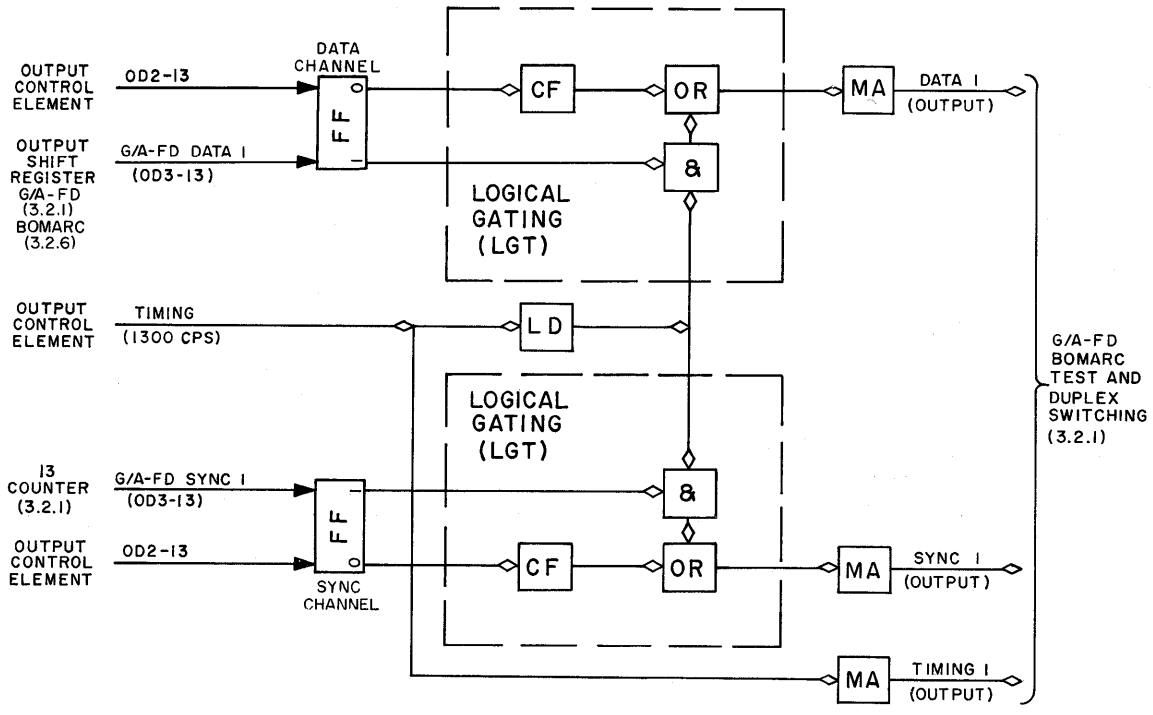


Figure 3–19. G/A-FD and BOMARC, Conversion Message 1 (3.2.1, 3.2.6), Simplified Logic Diagram

The G/A-FD output data channel 1 flip-flop supplies an input level to the 2-way AND circuit component of a logical gating (LGT) circuit. The LGT is comprised of this AND circuit plus a cathode follower and an OR circuit. The other input to the 2-way AND circuit is the 1,300-cps timing signal supplied via a logic driver (LD) circuit. The output of the AND circuit is either the timing signal or a —30-volt level, depending on whether the flip-flop is set or clear, respectively.

The flip-flop also supplies an input level to the OR driver cathode follower component of the LGT circuit. This cathode follower generates a clamped ground or a —30-volt output level, depending on whether the flip-flop is clear or set, respectively.

The AND circuit and cathode follower outputs both constitute the inputs of the OR circuit component of the LGT circuit. The output of this OR circuit is either the 1,300-cps timing signal or a ground level, depending on whether the flip-flop is set or clear, respectively. This output is sent to the telephone equipment.

When the flip-flop is set by receipt of a 1 bit (that is, a standard pulse occurring at OD 3–13 time), the data conversion channel will send a 1,300-cps sine wave to the telephone equipment. This sine wave will continue until the flip-flop is cleared by the following OD 2–13 pulse. Since the OD 3–13 pulses recur at a 1,300-cps rate and the OD 2–13 pulse precedes the next OD 3–13 pulse by 2.5 μsec, the interval between an OD 3–13 data pulse and the following OD 2–13 clear pulse will be 2.5 μsec less than the period of the 1,300-cps timing signal. Therefore, for each 1 bit received by the flip-flop, slightly less than one cycle of the 1,300-cps timing signal will be sent to the telephone equipment.

When the flip-flop is clear at OD 3–13 time due to the receipt of a 0 bit (that is, the absence of a standard pulse), a ground level will be sent to the telephone equipment.

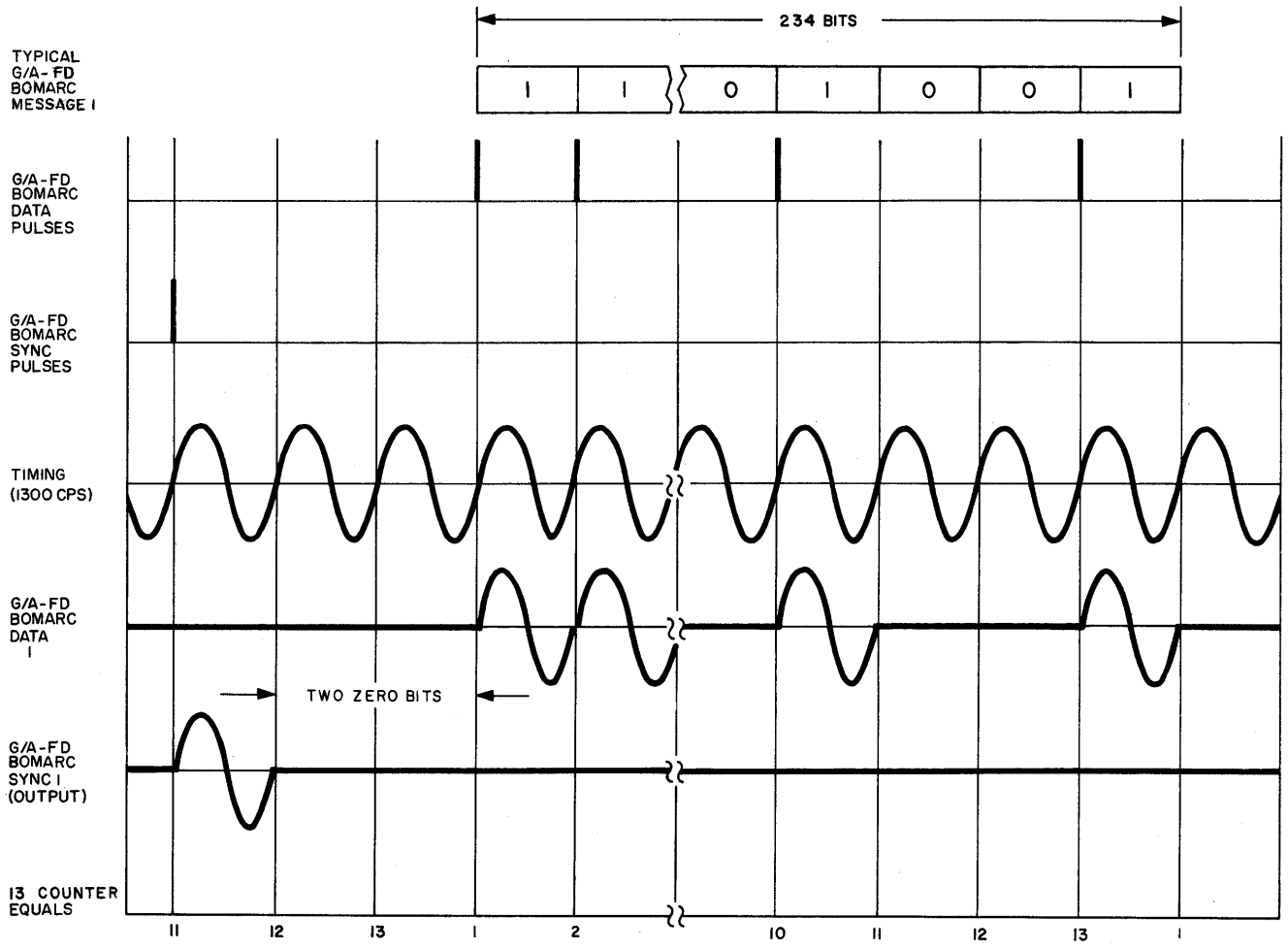


Figure 3–20. G/A-FD and BOMARC Input and Output Signals

2.8.2.3 Sync Conversion Channel

The sync conversion channel shown in figure 3–19 operates in a manner identical to the data conversion channel just described. For each sync pulse received, the sync conversion channel transmits slightly less than one cycle of the 1,300-cps timing signal to the telephone equipment. The sync pulse is applied to the conversion equipment at such a time that exactly two 0 bits occur on the data lines between the end of the output sync signal and the time that the first data bit is transmitted over the data lines. (See fig. 3–20.) This timing, which is necessary for decoding in the airborne receiver, is obtained by having an OD 3–13 sync pulse occur at 13-counter-11 time just prior to the readout portion of each burst period. (Refer to 2.4.2.) The sync pulse therefore precedes the data pulses, which are read out starting with the next 13-counter-equals-1 pulse, by two 13-counter shifts. In this manner, two 0 bits (the absence of two data pulses on the data lines at OD 3–13 time) occur between the receipt of the sync pulse and the start of the data pulses (. . . 00SS00).

The data, sync, and timing inputs and outputs of one message channel of the G/A-FD conversion equipment for a typical G/A-FD message are shown in figure 3–20. The outputs of this message channel, together with the outputs of the second identical message chan-

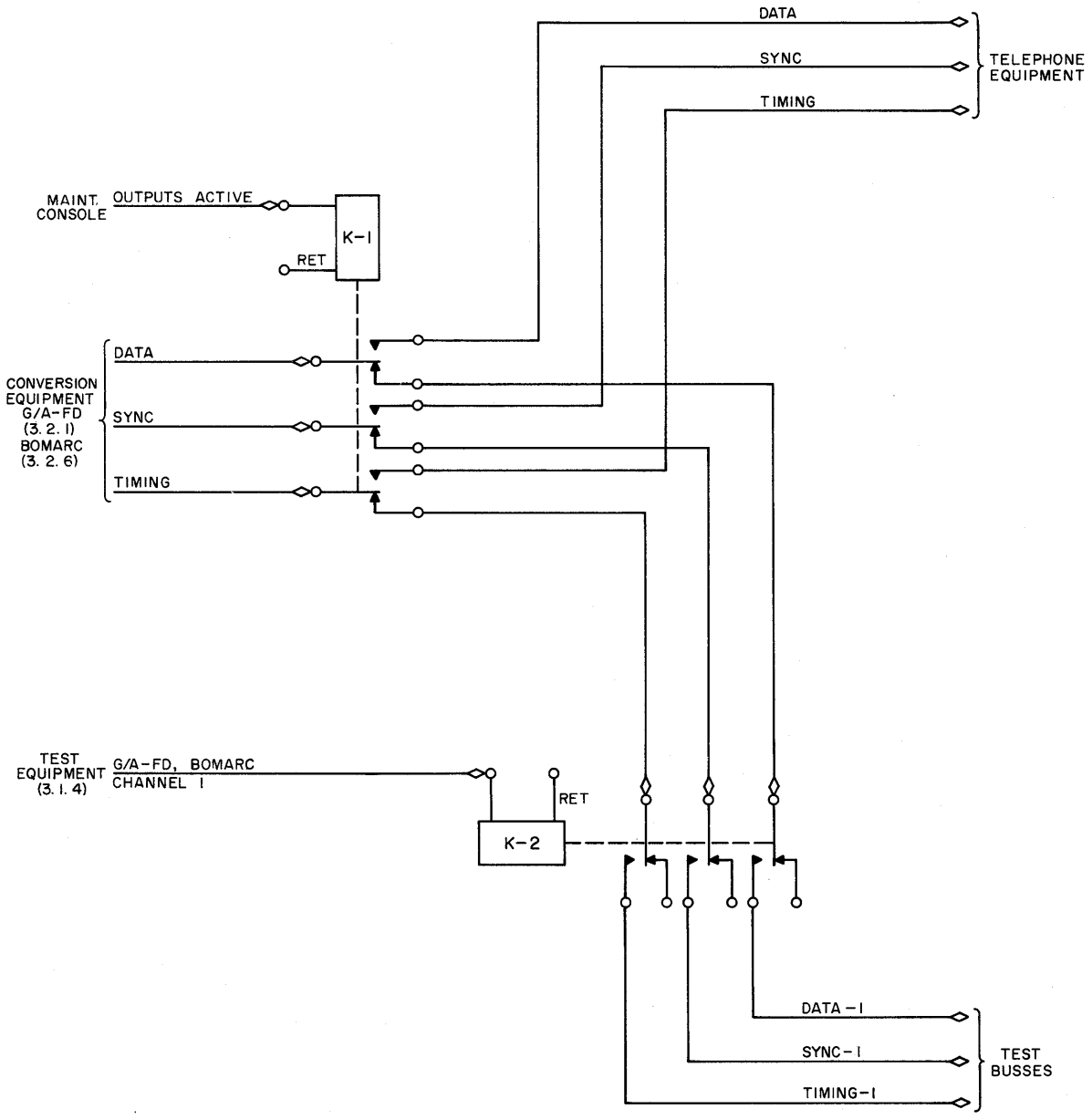


Figure 3–21. G/A-FD and BOMARC Test and Duplex Switching, Message 1 (3.2.1, 3.2.6), Simplified Diagram

nel, are fed to the switching circuits and from there sent out to the telephone equipment.

2.9 SWITCHING (G/A-FD, BOMARC)

The G/A-FD test and duplex switching circuits control the output of the Output System of each computer. The switching circuits contain relays which provide for the switching of each G/A-FD message. However, the relay circuits for each message are identical. For this reason, figure 3–21 shows a simplified diagram of the G/A-FD test and duplex switching circuits for only one G/A-FD message.

The relays provided by the G/A-FD test and duplex switching circuits are controlled so that only the Output System of the active computer is presented to the telephone line terminal equipment. Relays are also provided to enable the Output System on standby status to be switched to the LRI test busses through pattern generators. These relays are operated during test operations only.

CHAPTER 3
GROUND-TO-GROUND STORAGE SECTION

3.1 GENERAL

The G/G output storage section assembles output words received in parallel form from the output control element into messages, and then transmits these messages serially over telephone data channels to specific destinations. These messages are transmitted at 1,300 pps. A simplified diagram of the G/G storage section is shown in figure 3–22.

Five G/G messages may be transmitted simultaneously during each G/G burst period. Each message is composed of five output words and is transmitted over a separate telephone data channel to a specific destination. These messages are of the following types:

a. Forwardtelling messages to an AN/FSQ-8 Combat Control Central

b. Crosstelling messages to an adjacent AN/FSQ-7 Combat Direction Central

c. Height-finder request messages to height-finder radars at radar sites.

A parity check is performed on each output word by the site receiving the G/G message to determine whether the original contents of the output word have been altered by noise affecting the transmission channel. To ensure greater accuracy in the parity check, the output words in the G/G messages are transmitted in a serial interleaved form. The 17 bits of an output word are therefore spaced five bits apart on the telephone data channel. (See fig. 3–23.) With this manner of transmission, errors in up to five adjacent bits can be detected by the parity check. The fact that no two adjacent information bits are checked by the same parity check circuit insures that double errors will be detected if they are in adjacent bits of the message.

The time required to read out all messages in a G/G core storage array is 70 ms. This is about equal to G/G search time which is 65 ms. To eliminate the waste of telephone line time which would result if the line were not used during search time, two core storage arrays are included in the G/G storage section. One array receives information while the contents of the second array are read out to telephone line channels. Twice as many G/G messages can therefore be sent. Since two storage arrays are employed and search time for one storage array occurs simultaneously with the readout of the other, a G/G burst period is set at 70 ms.

3.2 SYSTEM OPERATION

The G/G storage section is logically divided into storage, readout, control, message check, burst counting and compare, conversion, and switching circuits, as shown in figure 3–22. These circuits perform functions similar to the corresponding circuits of the G/A-FD and BOMARC storage sections. (Refer to 2.2) However, since the G/G message structure differs from a G/A-FD or BOMARC message, the operation of the G/G circuits varies somewhat from corresponding G/A-FD or BOMARC circuits. These differences occur mainly in the timing of circuit functions. A description of the operation of the G/G storage section follows.

3.2.1 Counter Operation

The control circuits consist of the G/G control, the 5 counter, and the 19 counter. The two counters control the timing operations and operate as explained below.

The 5 counter is shifted at a 1,300-pps rate by pulses from the output control section. On every fifth shift, a 5-counter-equals-5 pulse is generated which is used to shift the 19 counter. The 19 counter repeats its counting cycle after it has been shifted 19 times. A complete G/G burst period takes place during this cycle, during which time one G/G core storage array is read into while the other is simultaneously read out.

A G/G operational cycle consisting of read-in and readout for one of the two core arrays is described in the following paragraphs. The G/G read-in interval and the readout interval for a single core array each takes place during successive burst periods. Two G/G burst periods are therefore required for the G/G storage section to complete a cycle of operations. In actual operation, the read-in and readout functions occur simultaneously; while one core array is being written into, the other array is simultaneously being read out.

3.2.2 Read-In

Each G/G burst period starts at the 19th shift of the 19 counter. At this time, the 5 counter and the 19 counter are cleared and primed. The 19-counter cycle starts with its next shift. At 19-counter-1 time, the G/G control sends a search level to the output control element. This level signals the output control element that read-in can now take place. The core array which had been read out during the previous burst period is now written into. Each correct G/G output word (right half

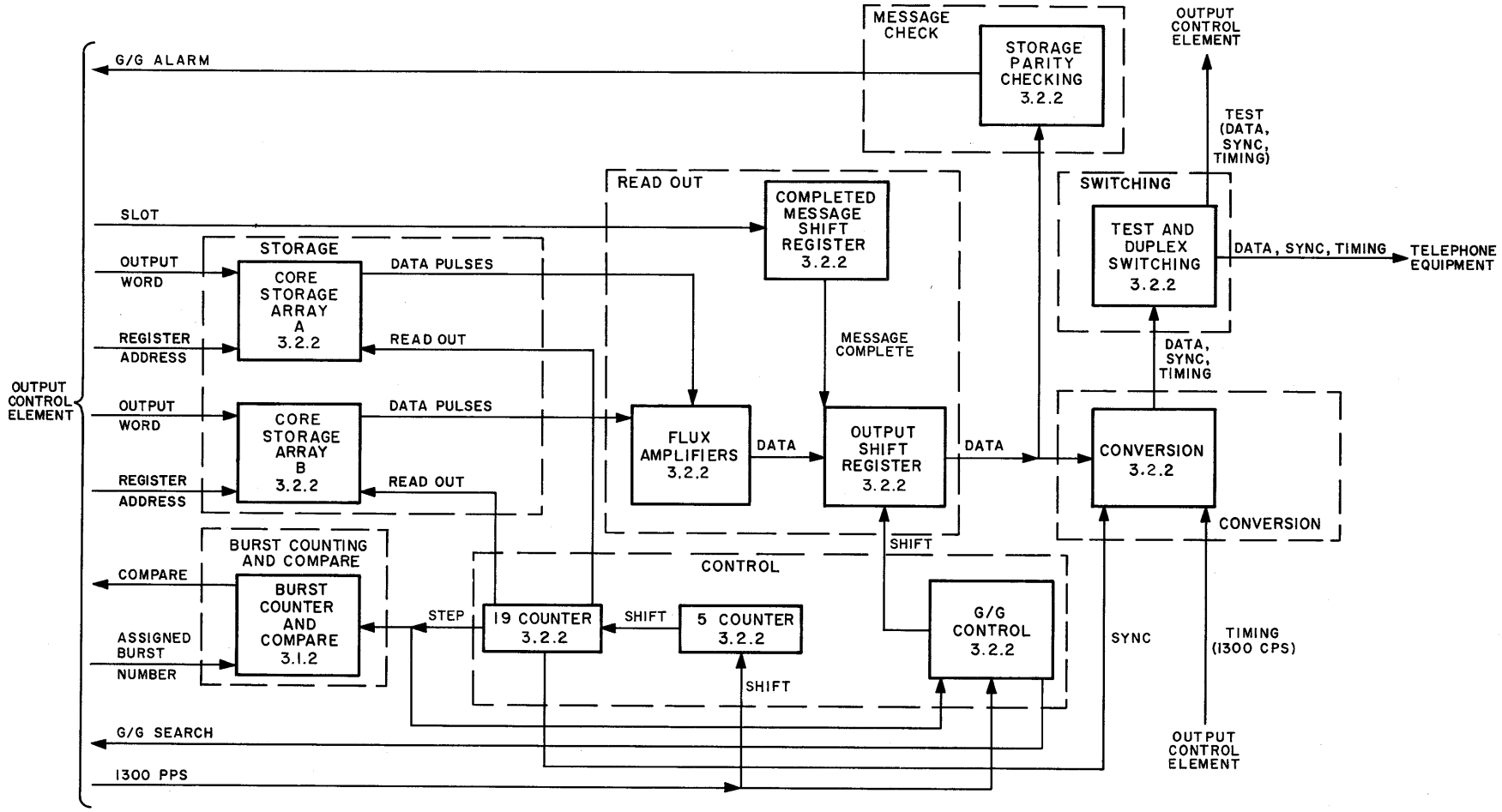


Figure 3–22. G/G Output Storage Section (3.2.2), Simplified Block Diagram

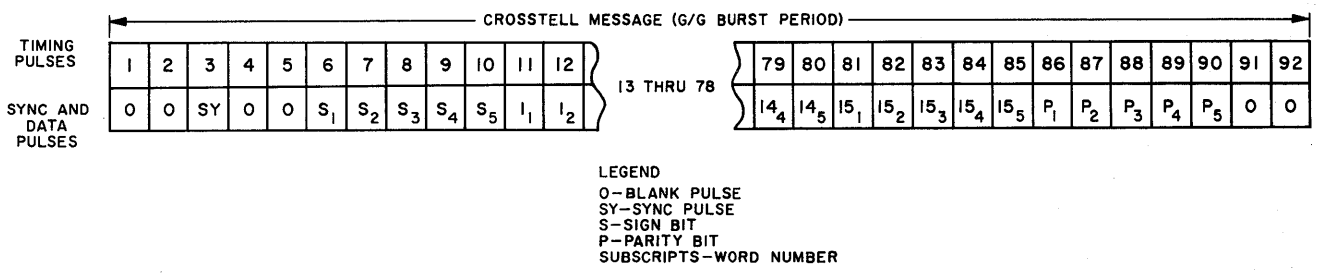


Figure 3–23. G/G Message, Serially Interleaved Form

drum word bits RS through R15 plus an even parity bit) whose assigned burst number matches the contents of the G/G burst counter is written into; a pulse is sent to the completed message shift register by the control element. The completed message shift register counts the number of words loaded in each message slot in a core array.

Read-in is completed before 19-counter-18 time. At this time, the G/G control generates a sync pulse, a not-search level, and a shift-phase level. The sync pulse is sent to the conversion equipment; the not-search level prevents the output control element from writing into any more core registers. The shift-phase level switches core arrays so that the array just read into will be read out during the next burst period.

3.2.3 Readout

Readout of the core array which has been written into starts at 19-counter-1 time. At this time, the 19 counter generates a clear-column-1 pulse. This pulse is sent to the core storage array where it serves to send all the information contained in the first column of cores through the FA's and into the OSR's. This information is now passed out of the OSR (as explained in the following paragraphs) only if the completed message shift register has counted five words written into that slot of the core array. This prevents transmission of incomplete messages.

In the interval between 19-counter-1 time and 19-counter-2 time, the OSR's and the 5 counter are shifted five times. With each shift of the OSR, one bit of each of the five G/G messages is sent to the conversion circuits, to the storage parity checking circuit, and to the output control element. The output control element utilizes this information when test procedures are performed. At the storage parity checking circuit, the data is entered and later examined for errors. A G/G alarm is generated if an error is found. At the conversion circuits, the data is made compatible for transmission by telephone data channels.

Simultaneously with the fifth shift of the 5 counter, the OSR is emptied. At this time, the 5 counter generates a 5-counter-equals-5 pulse. This pulse shifts the 19 counter, causing it to read out another column of the core storage array into the OSR. The information is then shifted out of the register in the same manner as the data from the first column. The process repeats itself until the entire message has been read out of the core array.

3.3 STORAGE

3.3.1 Core Storage Arrays

The output words comprising G/G messages are stored in rectangular ferrite core storage arrays. Each G/G output word, which is 17 bits in length, is stored in one register or row of the array. The array has 17 columns and 25 rows, and can therefore store 25 output words. (See fig. 3–24.)

Two identical arrays are included to provide the most efficient use of telephone channels. Each array is written into row by row and read out column by column. Writing is done by coincident currents. (See fig. 3–25.) As each word is transferred to the core storage array, a half-write current is applied to the register address winding of the row in which that word should be written. Simultaneously, right drum word half-write current pulses are applied to those column windings in which a 1 should be recorded. During readout, a read current pulse is applied to a clear column winding. Each core in the column receives a full-read current, with each core output appearing on the array output winding for its row. Corresponding row array output windings in the two arrays are wired in series. (See fig. 3–26.) No interference between matrices results since only one array is read out at a time through use of gated TCD's.

3.3.2 Core Array Read-In

During each burst period, G/G message words are written into the core storage array which is not being read out. The right drum word with its even parity bit is applied by the output control element to the core storage array as half-write pulses on those drum word lines whose bits are 1's. The row in the array on which the word is written is specified by the register address contained in the left drum word. Thus, message assembly is accomplished by the assigned burst number and

the register address. Since the search period for the OB fields is approximately 65 ms, read-in to one array can be completed during the 70-ms readout time for the other array.

The selection of an array for read-in is accomplished by the output control element. The G/G control supplies that element with information on which array is being read out. The output control element, in turn, routes words for read-in into the other array.

3.4 CONTROL

3.4.1 General

While many of the control functions of the G/G output storage section are managed by the output control element, certain functions unique to the section are managed by control circuits within the section. These control units include the 5 counter, the 19 counter, and the G/G control.

3.4.2 5 Counter

The 5 counter, shown in figure 3–27, is a 5-core ring counter which is cleared, primed, and then continuously stepped at 1,300 pps. The outputs from this counter are used in performing test operations and controlling functions of the storage section. The operation of the 5 counter follows.

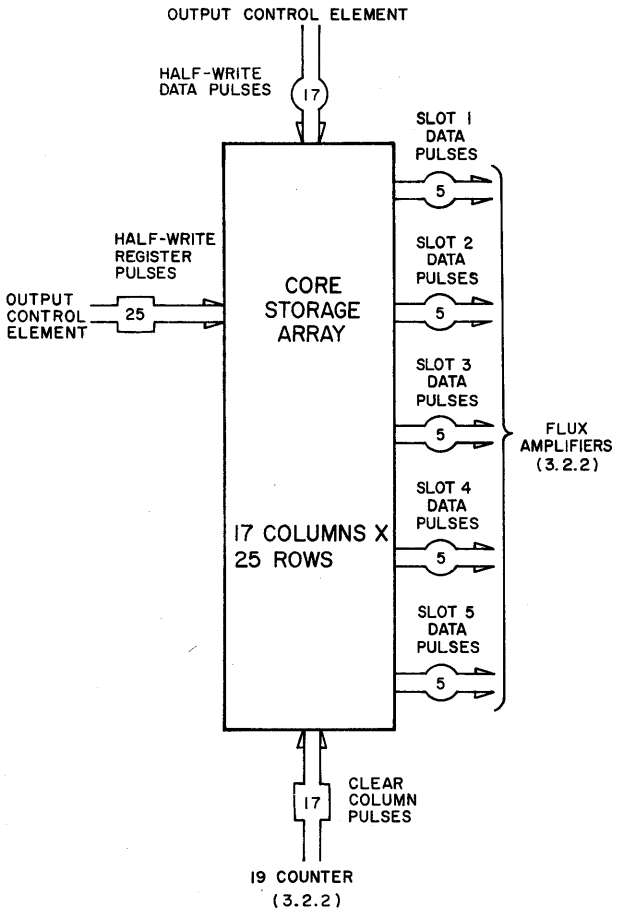


Figure 3–24. G/G Core Storage Array (3.2.2), Simplified Block Diagram

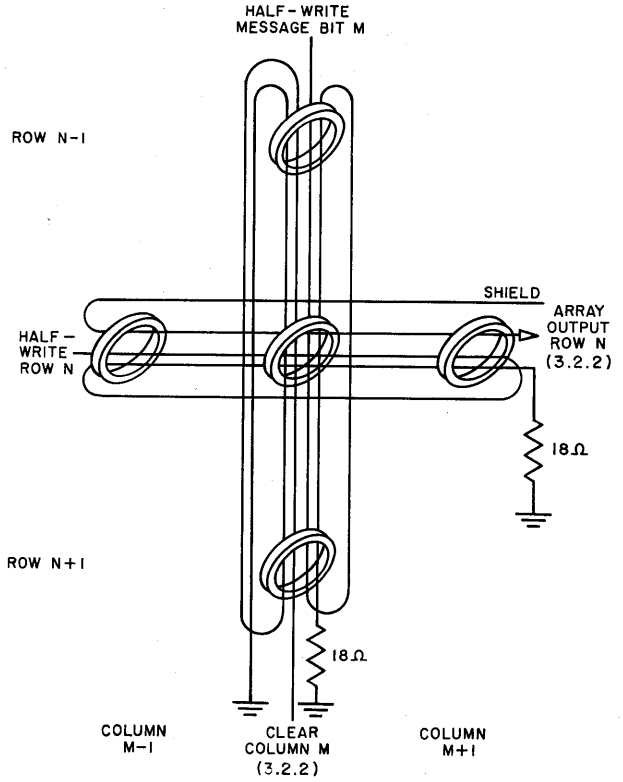


Figure 3–25. Portion of G/G Core Storage Array (3.2.2), Simplified Diagram

At the start of system operation or after a shutdown or test operation, the output control element sends an OD 4 reset and prime pulse to the 5 counter and the G/G control. This pulse and the following OD 3 pulse cause a 7.5-μsec shift pulse to clear the 5 counter. The G/G control then primes the 5 counter by entering a 1 in its fourth core. (Refer to 3.4.4.) Generated by the flip-flop for each combination of an OD 2–13 and OD 3 pulse applied to it, 5-counter shift pulses shift this 1 through the counter. As the 1 is shifted out of the fifth core, it is transferred to the first core. From this point until the end of the burst period, the 5 counter maintains a continuous serial count of each group of five shift pulses.

As the 1 is transferred from one core to another, a 5-counter-equals pulse is generated. The 5-counter-equals-1 through 5-counter-equals-5 pulses are sent to the test equipment section. The 5-counter-equals-5 pulse is also used to condition a gate which is pulsed by OD 3–13 timing pulses. At 5-counter-5 time, an OD 3–13 pulse is passed by the gate and sent to the G/G control (fig. 3–29) as a 5-counter-equals-5 pulse. This pulse is used to generate a 19-counter-shift pulse and a G/G

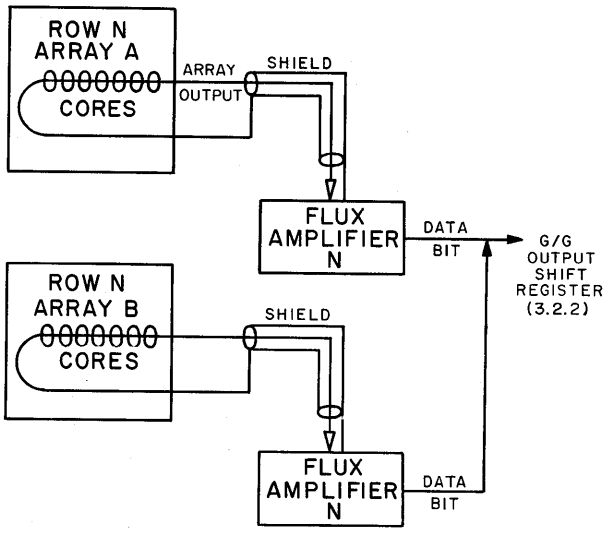


Figure 3–26. Output Wiring of G/G Core Arrays A and B, Simplified Diagram

sync pulse. The sync pulse is generated only at 19-counter-18 time.

The 5 counter is continually shifted until the 19th shift of the 19 counter. At this time, which is the end of the burst period, the 5 counter is cleared by a 7.5-μsec shift pulse developed by the combination of a 19-counter-equals-19, an OD 4–13 pulse, and the following OD 3 pulse. The 19 counter is simultaneously cleared by the G/G control, which then primes both counters. (Refer to 3.4.4.) The 5 counter then resumes shifting to start the next burst period.

The 5 counter is always primed by entering a 1 in its fourth core. This is done to satisfy the requirement that 92 timing pulses (5-counter shift pulses) occur during a G/G burst period. By priming the 5 counter in this way, two 5-counter shifts are made to occur between 19-counter-19, which is the time of priming, and 19-counter-1, which is the start of readout and read-in. Since 90 5-counter-shift pulses occur between 19-counter-1 and 19-counter-19, the 92 required 5-counter shift pulses are obtained.

3.4.3 19 Counter

The 19 counter (a 19-core shift register) sequences the readout of each column of the core storage array. Each time this counter is stepped, from 19-counter-1 through 19-counter-17, one column in the core storage array is read out. Figure 3–28 shows a simplified diagram of the 19 counter.

At the start of operation, the 19 counter is cleared and primed by the G/G control. (Refer to 3.4.4.) The 19 counter is then shifted by the G/G control once for each 5-counter-equals-5 pulse. Each time the 19 counter is shifted, a 19-counter-equals pulse is generated. These pulses are generated in sequence from 1 through 19. The first 17 of these pulses are applied to two gated TCD registers to produce clear-column pulses. These pulses are used to read out each column of the core array. Since only one register is conditioned at any one time, clear-column pulses are applied to only one core storage array at a time. The conditioning levels for the TCD registers, shift-phase-B, are supplied by the G/G control.

The 19-counter-equals -1, -17, -18, and -19 pulses are applied as conditioning levels to four gates in the 19 counter. An OD 4–13 pulse occurring at either 19-counter-1, -17, -18, or -19 time will be passed by the gate whose conditioning level is up as a result of the 19-counter-equals pulse.

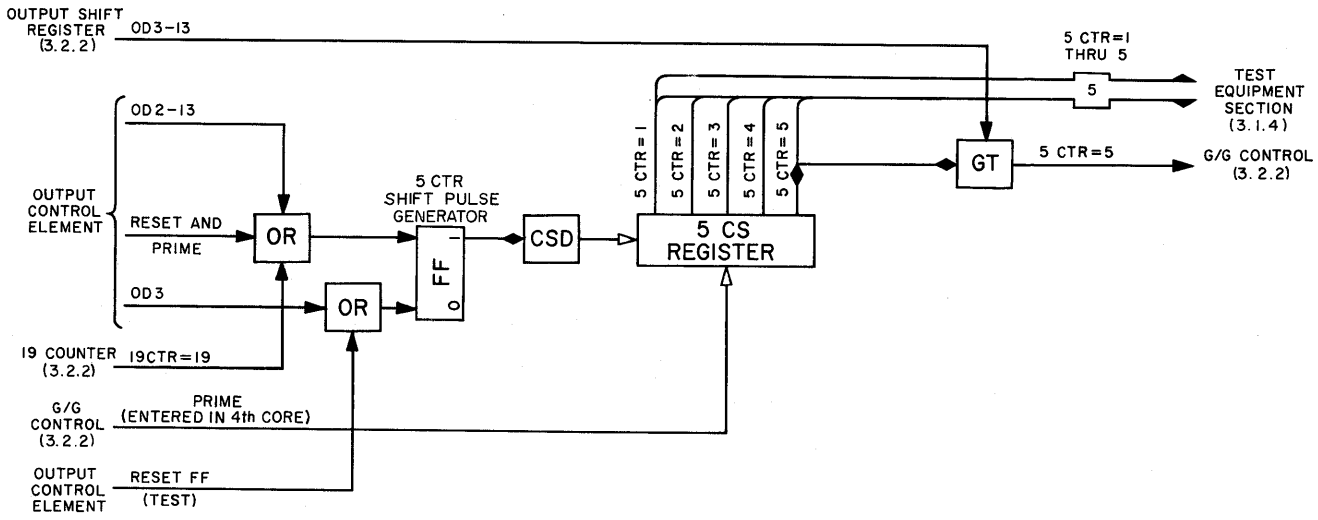


Figure 3–27. 5 Counter (3.2.2), Simplified Logic Diagram

An OD 4–13 pulse occurring at 19-counter-1 time is sent to the G/G control (fig. 3–29) as a 19-counter-equals-1 pulse, where it starts the shifting of the OSR and also initiates the search G/G level. (Refer to 3.4.4.) In addition, the 19-counter-equals-1 pulse is sent from the G/G control, through relay contacts in the 19 counter, to the burst counter (fig. 3–35). During normal operation, the relay in the 19 counter is de-energized and the 19-counter-equals-1 pulse is used to step the burst counter. During test operation, the relay is ener-

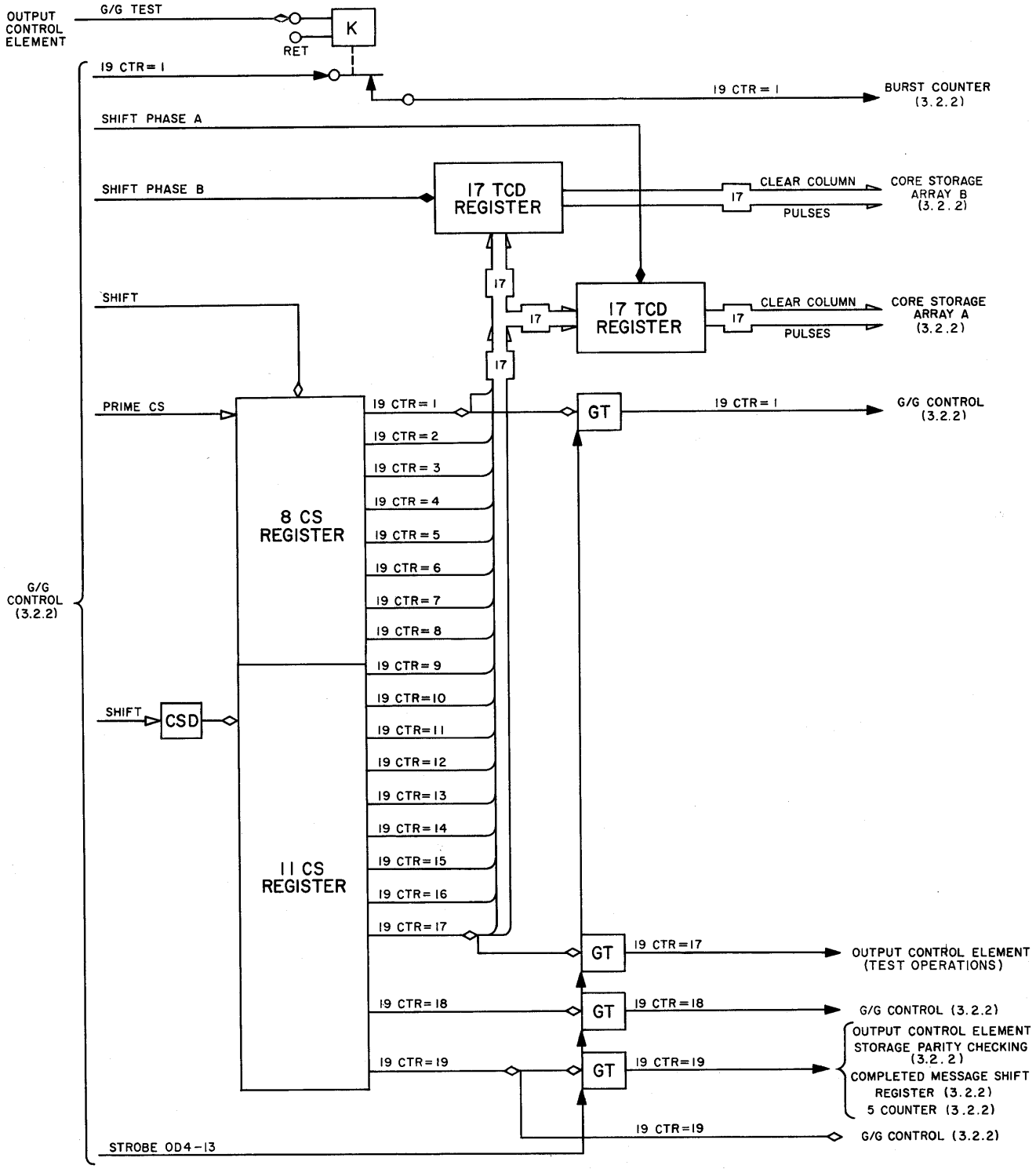


Figure 3–28. 19 Counter (3.2.2), Simplified Logic Diagram

gized and the burst counter is prevented from being stepped.

An OD 4–13 pulse occurring at 19-counter-17 time is sent to the test equipment section when it is used in test operations.

An OD 4–13 pulse occurring at 19-counter-18 time is sent to the G/G control as a 19-counter-equals-18 pulse, where it performs the following functions (refer to 3.4.4):

a. Ends shifting of the OSR
b. Initiates the not-search level
c. Functions in the generation of the G/G sync pulse
d. Selects G/G-A or G/G-B arrays for readout

An OD 4–13 pulse occurring at 19-counter-18 time is also sent to the completed message shift register (fig. 3–33) as a 19-counter-equals-18 pulse, where it is used to reset the output flip-flops. (Refer to 3.5.4.)

An OD 4–13 pulse occurring at 19-counter-19 time is sent to the following circuits as a 19-counter-equals-19 pulse:

a. To the 5 counter (fig. 3–27) where it serves to clear the registers. (Refer to 3.4.2)
b. To the storage parity checking circuit (fig. 3–34) where it is used in the storage parity check. (Refer to 3.6.)
c. To the completed message shift register (fig. 3–33) where it is used in the completed message check. (Refer to 3.5.4.)
d. To the test equipment section where it is used in test operations.

In addition to gating an OD 4–13 pulse as previously explained, the 19-counter-equals-19 pulse is applied to an inverter within the G/G control. This pulse serves to prime the 5 counter and the 19 counter as explained in detail later in this section.

3.4.4 G/G Control

The G/G control (fig. 3–29) handles the bulk of control functions in the G/G output storage section. This control supplies two sets of levels to the output control element: search G/G or not-search G/G levels, and shift-phase-A or shift-phase-B levels.

The G/G search and G/G not-search levels are developed by the 1 and 0 sides, respectively, of the G/G search flip-flop. This flip-flop is set by each 19-counter-equals-1 pulse. This raises the search G/G level which is sent to the output control element, informing it that the G/G storage section can receive data. The search G/G level remains up until the flip-flop is cleared by a 19-counter-equals-18 pulse. At this time the search G/G level is terminated and the not-search G/G level is raised. This level is sent to the output control element, halting the flow of data to the G/G storage section.

The shift-phase-A and shift-phase-B levels are developed by the 0 and 1 sides, respectively, of the G/G shift-phase flip-flop. This flip-flop is complemented by each 19-counter-equals-18 pulse. The two shift-phase levels therefore alternate between burst periods, each level being raised at the end of every other burst period. These levels are sent to the output control element where they cause data to be written into the core array not being read out at the time. These levels are also applied to the 19 counter, where they are used to condition the TCD registers. (Refer to 3.4.3.)

Shift pulses for the OSR are supplied by the output control element as OD 2–13 pulses. These pulses are gated through the G/G control between 19-counter-equals-1 and 19-counter-equals-18 by the action of the G/G shift control flip-flop. The strobe pulse used to sense the counter-conditioned gates in the 19 counter also originates in the output control element as OD 4–13. Since it is used in the G/G control, the strobe pulse is routed through there before being applied to the 19 counter.

The sync pulse indicating the beginning of a burst period transmission is developed in the G/G control by the action of the G/G sync generator flip-flop. This flip-flop is set by a 19-counter-equals-18 pulse. The level developed by the 1 side of this flip-flop conditions a gate which is sensed by 5-counter-equals-5 OD 3–13 pulses and is applied to the conversion equipment as a G/G sync pulse. This 5-counter-equals-5 pulse also sets the 19-counter carry flip-flop.

The remaining portion of the G/G control (the portion labeled core shift registers control in fig. 3–29) supplies all clear, prime, and shift pulses for the 19 counter and the completed message shift register, the prime pulse for the 5 counter, and the gating levels which are applied to the FA's.

The major component of the CSR's control is the 19-counter shift flip-flop. At the start of operations, this flip-flop is set by a reset-and-prime pulse applied by the output control element at OD 4 time. The level thus developed by the 1 side of the flip-flop is applied to the 19-counter CSD's and to a gate sensed by OD 3 pulses. The following OD 3 pulse is passed by this gate and clears the 19-counter shift flip-flop. Thus, the 19-counter shift flip-flop develops a 7.5-μsec level which is applied by the CSD's to the 19 counter, thus clearing its register.

The OD 3 pulse that clears the 19-counter shift flip-flop also triggers a single-shot multivibrator. This multivibrator generates a 2.5-μsec signal which primes the 5 counter, the 19 counter, and the completed message shift register.

The 19-counter shift flip-flop is now set by the following 5-counter-equals-5 pulse received at OD 3–13 time. This flip-flop is cleared by the next OD 4–13 pulse when the gate through which the pulse is applied is conditioned by the 19-counter-not-19 level from the inverter. Thus, for all conditions of the 19 counter except 19-counter-equals-19, the 19-counter shift flip-flop is set between 5-counter-equals-5 (OD 3–13) and 5-counter equals-5 (OD 4–13) for 2.5 μsec. The flip-flop output levels are sent as shift pulses to the 19 counter.

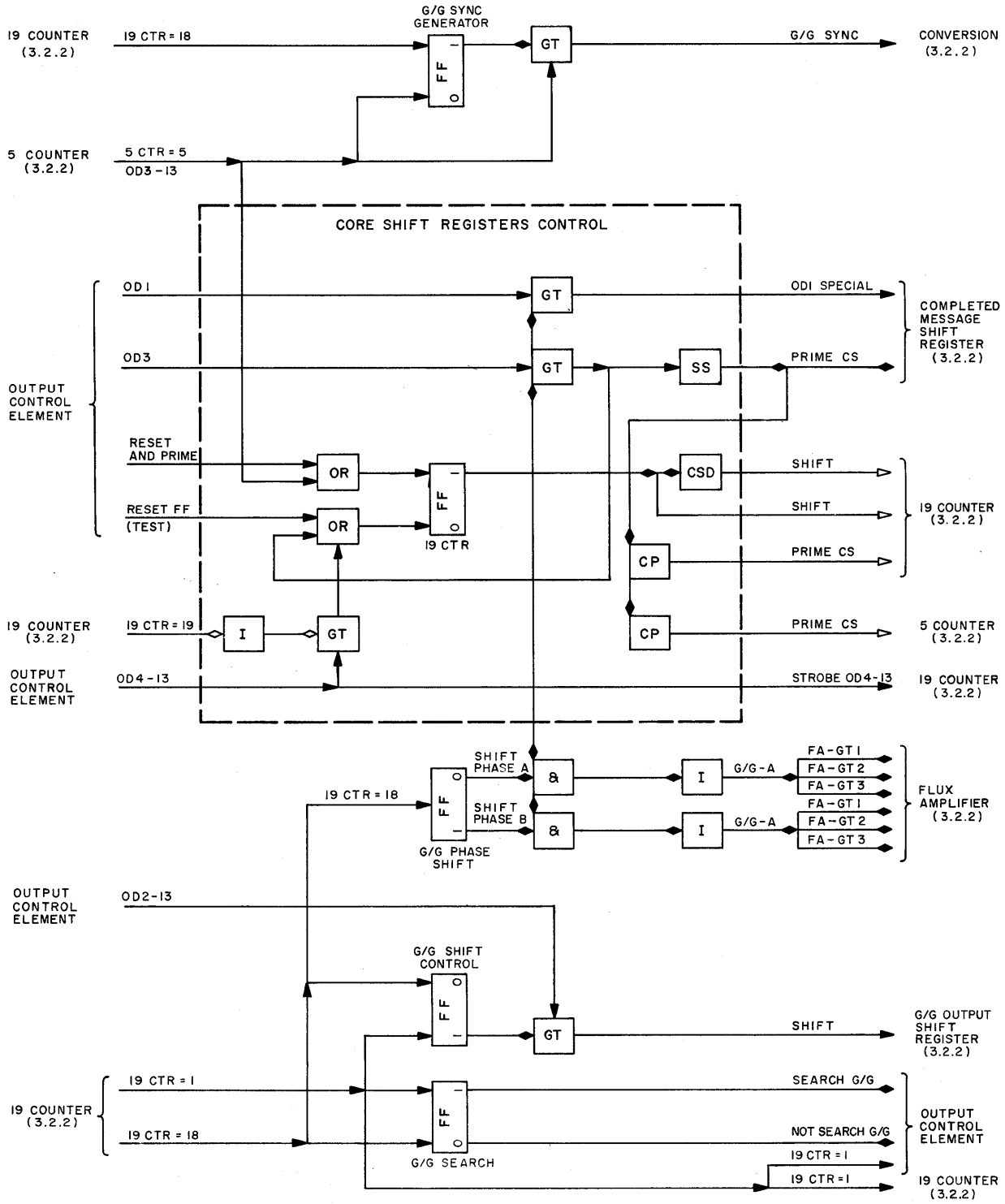


Figure 3–29. G/G Control (3.2.2), Simplified Logic Diagram

In addition, these output levels are sent to strobe two 2-way AND circuits. The latter are associated with the respective output lines of the G/G shift-phase flip-flop. Hence, when an output level is generated by the 19-counter shift flip-flop and is present at either AND circuit in coincidence with a G/G shift-phase level (A or B), the conditioned AND circuit will pass a level to its respective inverter circuit. The level is thus inverted and sent as gating levels 1, 2, and 3 to the FA's. The flip-flop output also conditions two gates. However, the timing of the pulses which sense these two gates is such that the gates produce no output. The conditioning level will not be up fast enough for the gate sensed by OD 3 to pass that pulse, and the level will be down before the OD 1 pulse senses the other gate. Therefore, the only outputs of the CSR's control during 19-counter-not-19 time are the shift pulses for the 19 counter and the FA gating levels.

When the 19 counter reaches 19, the 19-counter flip-flop is set, as before, by a 5-counter-equals-5 pulse, which occurs every fifth OD 3–13 pulse. However, at this point the OD 4–13 clear pulse is not passed by the gate, since the inverter deconditions the gate at 19-counter-equals-19. The flip-flop therefore remains set until the gate sensed by OD 3 passes that pulse to clear the flip-flop, an interval of 10 μsec. This 10-μsec pulse from the flip-flop acts as a clear pulse for the 19 counter and is applied on the shift line. The OD 3 pulse which clears the flip-flop also triggers a single-shot multivibrator to produce a prime pulse for the 5 counter, the 19 counter, and the completed message shift register. The other gate, sensed by OD 1, passes this pulse as OD 1-special to the completed message shift register to sense the gates therein and set the completed message flip-flops. Thus, at 19-counter-equals-19, clear pulses are generated for the 19 counter, and prime pulses are generated for the 5 counter, 19 counter, and the completed message shift register. Figure 3–30 shows the timing of the various functions of the G/G control.

3.5 G/G READOUT

3.5.1 General

Readout of a G/G message is accomplished in three steps. Each message is read out of the core storage ar-

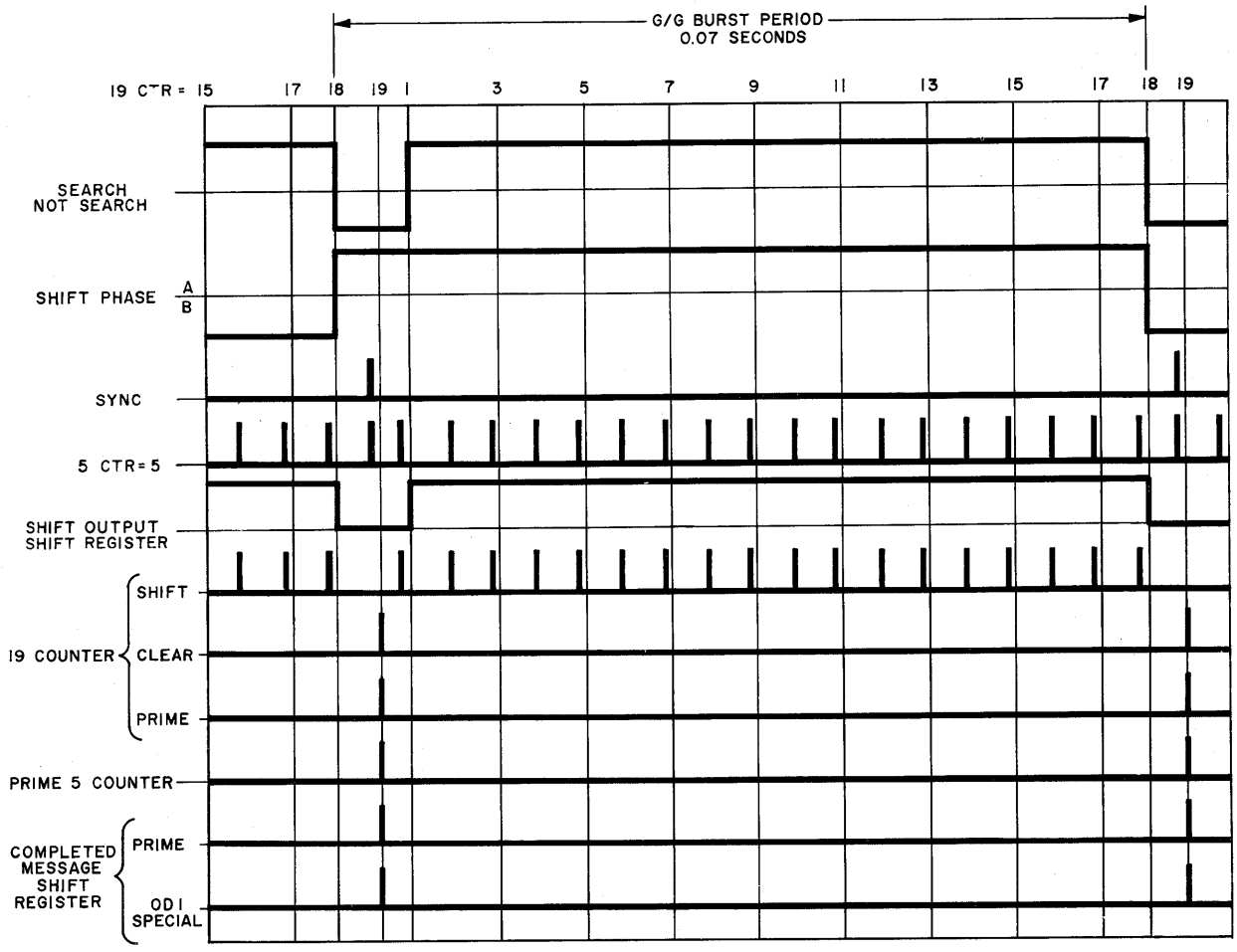


Figure 3–30. G/G Control Timing Chart

ray, five bits at a time, through the FA's into the OSR. (See fig. 3–22.) These five bits are shifted serially out of the OSR. Finally, if permitted by the completed message shift register, the data bits are presented to the conversion equipment. Although this and the following discussion treats only one message slot, the G/G output storage section contains five message slots, allowing transmission of five messages simultaneously. The accompanying illustrations show all five slots; the discussion of one channel applies equally to the other four.

3.5.2 Core Array Readout

Each message slot is read out of the core array by columns at the start of a burst period. The core array is comprised of 17 columns, pulsed serially by clear-column pulses that are applied by the TCD's located in the 19 counter. Each time that a column is pulsed, the five bits stored in its cores, one bit from each of the five output words in the message slot, are shifted from the core array in parallel form to the FA's. The G/G core array readout is similar to the G/A-FD core array readout. (Refer to 2.5.2.)

Each of the five array output pulses from the G/G core storage array is applied to an FA. A 1 bit is represented by a pulse and a 0 bit by the absence of a pulse. Separate groups of the five FA's shown in figure 3–31 are gated by gating levels 1, 2, and 3. These levels are 2.5-μsec OD 3–13 and OD 4–13 negative pulses employed to prevent noise and spurious signals from passing through the FA's. They are produced in the G/G control simultaneously with each shift of the 19 counter that occurs during readout time. (Refer to 3.4.4.) Since these 19-counter shifts generate clear-column pulses which read out columns of the core array, the core storage array outputs are applied to the FA's during the 2.5 μsec that the FA's are gated and operative. The FA's, after amplifying and stretching the array output pulses, send the pulses to the OSR as FA outputs. The outputs from the FA's are sent over 25 lines labeled FA output 0 through FA output 24, respectively.

3.5.3 Output Shift Register (OSR)

The OSR (fig. 3–32) receives five bits at a time from each of the five messages, and loads them into five 5-core shift registers. Shift pulses from the G/G control shift each register 1,300 times per second. Since the gate at the output of each 5-core shift register is sensed only when the data bits are placed in the shift register, no spurious output pulses are generated when the register is loaded. The shift signals from the flip-flop are 2.5 μsec in duration.

The output of the first gate is applied to the storage parity check circuit and to a second gate. This gate is conditioned by a completed-message level from the completed message shift register. If the level is applied,

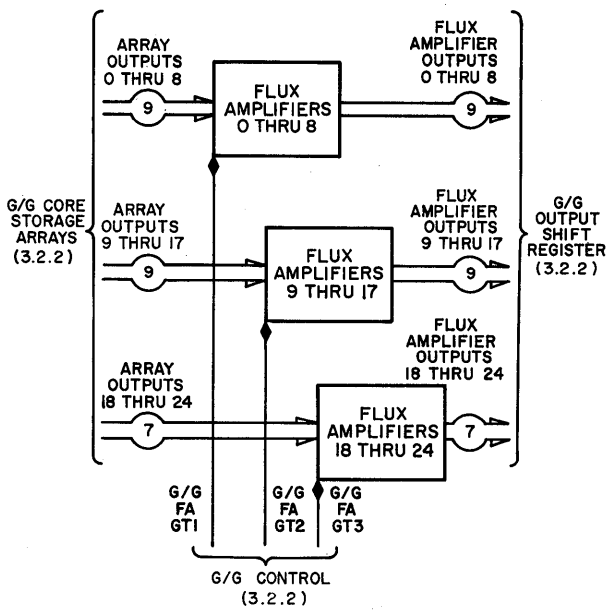


Figure 3–31. Flux Amplifiers (3.2.2), Simplified Block Diagram

the contents of the OSR are sent to the conversion equipment.

The next five 5-bit groups from the FA's must be loaded into the OSR within 4 ms after the first groups have been shifted out. This is done to maintain an even 1,300-pps output rate from the OSR.

3.5.4 Completed Message Shift Register

The completed message shift register (fig. 3–33) counts the number of output words written into each slot in the core storage array. If the full five words are written into a slot during a burst period, the message in that slot will be passed through the OSR to the conversion equipment. If not, the second gate in the OSR is not conditioned and no data from that message is presented for transmission.

At the beginning of a burst period, each OSR in the completed message shift register unit is primed by the G/G control which writes a 1 in the first core. (Refer to 3.4.4.) As each word is written into the appropriate core storage array, a slot level is raised corresponding to the message slot in which the word is written and a shift-completed-message-shift-register pulse is supplied by the output control element. This pulse shifts ahead the 1 in the shift register corresponding to that slot. After five words have been written into a slot, the last core in that shift register will hold the 1.

As the read-in ends, the flip-flops which now hold the results of the complete message check on the message that was being simultaneously read out from the

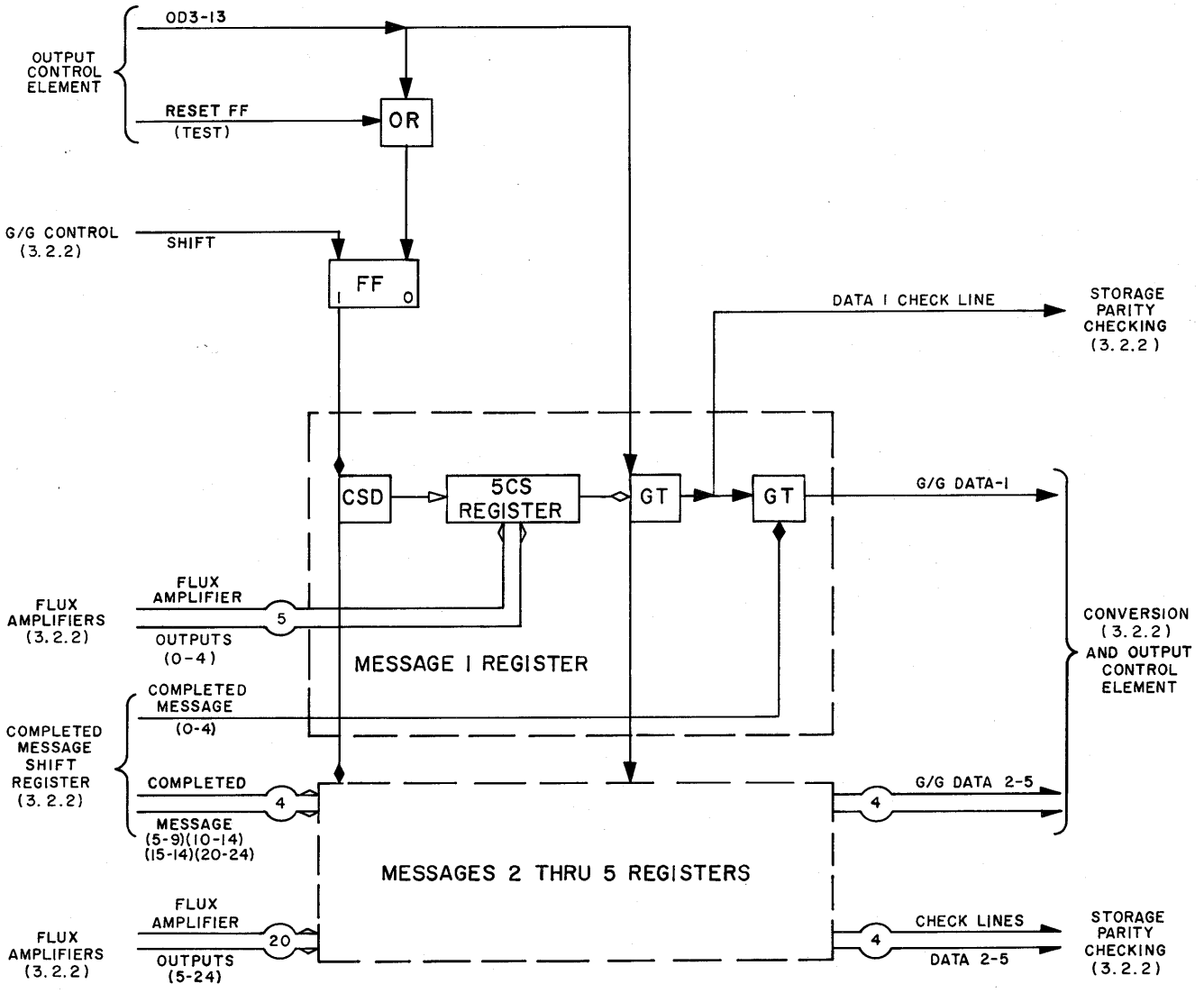


Figure 3–32. G/G Output Shift Register (3.2.2), Simplified Logic Diagram

other array are cleared by a 19-counter-equals-18 pulse. A 19-counter-equals-19 pulse from the 19 counter is now applied both to a single-shot multivibrator and to the shift-pulse generator flip-flop. The output of the single-shot multivibrator is sent to the output control element, which returns it to the completed message shift register as a conditioning level on all five AND circuits. Thus, the 19-counter-equals-19 pulse shifts all 5-core shift registers simultaneously. If the last core of a register holds a 1 when this last shift occurs, the gate at the output of the CSR is conditioned and then sensed by the special OD 1 pulse which occurs at this time. This sets the corresponding flip-flop, supplying the completed-message level for that slot. If fewer or more than five words are written in a slot during a search period, the 1's placed in the first core of each CSR will not be in the last core of the register to set the flip-flops, and the completed-message level will remain down.

3.6 MESSAGE CHECK

As G/G messages are transferred out of the output storage section for transmission, a parity check is taken on each message. The data check lines from the OSR, shown in figure 3–32, are applied to the storage parity checking circuit (fig. 3–34). In that circuit, the number of 1's in each message is counted. The number should be even, counting the parity bit added to each right-half drum word by the output control element. If the parity count in any message is odd, the 1 side of that message channel flip-flop will be up, conditioning the gate through the OR. When the gate is sensed at 19-counter-

equals-19, a G/G alarm is generated. This alarm is also used to clear the flip-flops.

3.7 BURST SEQUENCE AND TIMING

3.7.1 Purpose

G/G messages are transmitted in 70-ms burst periods. Successive messages on a single channel may follow each other immediately if sufficient message words are delivered through the OB fields to the output storage section. Messages are addressed to specific receiving points and also sequenced for transmission. This sequencing is accomplished by assigning each message word a burst number and keeping a count of the number of the burst to be next transmitted. By comparing the assigned burst number of a message word to the burst count for the next burst period, and by writing into the core storage array during read-in only those message words which are scheduled for transmission within that burst period, the time sequence is established.

3.7.2 Burst Counter

The G/G burst counter (fig. 3–35) is a standard 8-bit flip-flop counter (scale of 256) which is stepped by 19-counter-equals-1 pulses at all times except during test operations. Two sets of outputs are taken from the counter, one set from the 1 sides of the flip-flops, designated the burst counter contents, the other set from the 0 sides of the flip-flops, designated the burst counter complement. The burst counter contents are supplied to the output control element and are also used in the comparison circuits. A reset-flip-flops signal from the output control element is supplied after shutdown or test operations.

3.7.3 Burst Number Comparison

The burst counter is stepped at the start of a burst period by a 19-counter-equals-1 pulse. The number in the burst counter during each burst period corresponds to the number of the next burst period. G/G message words are read from the OB fields by status identifica-

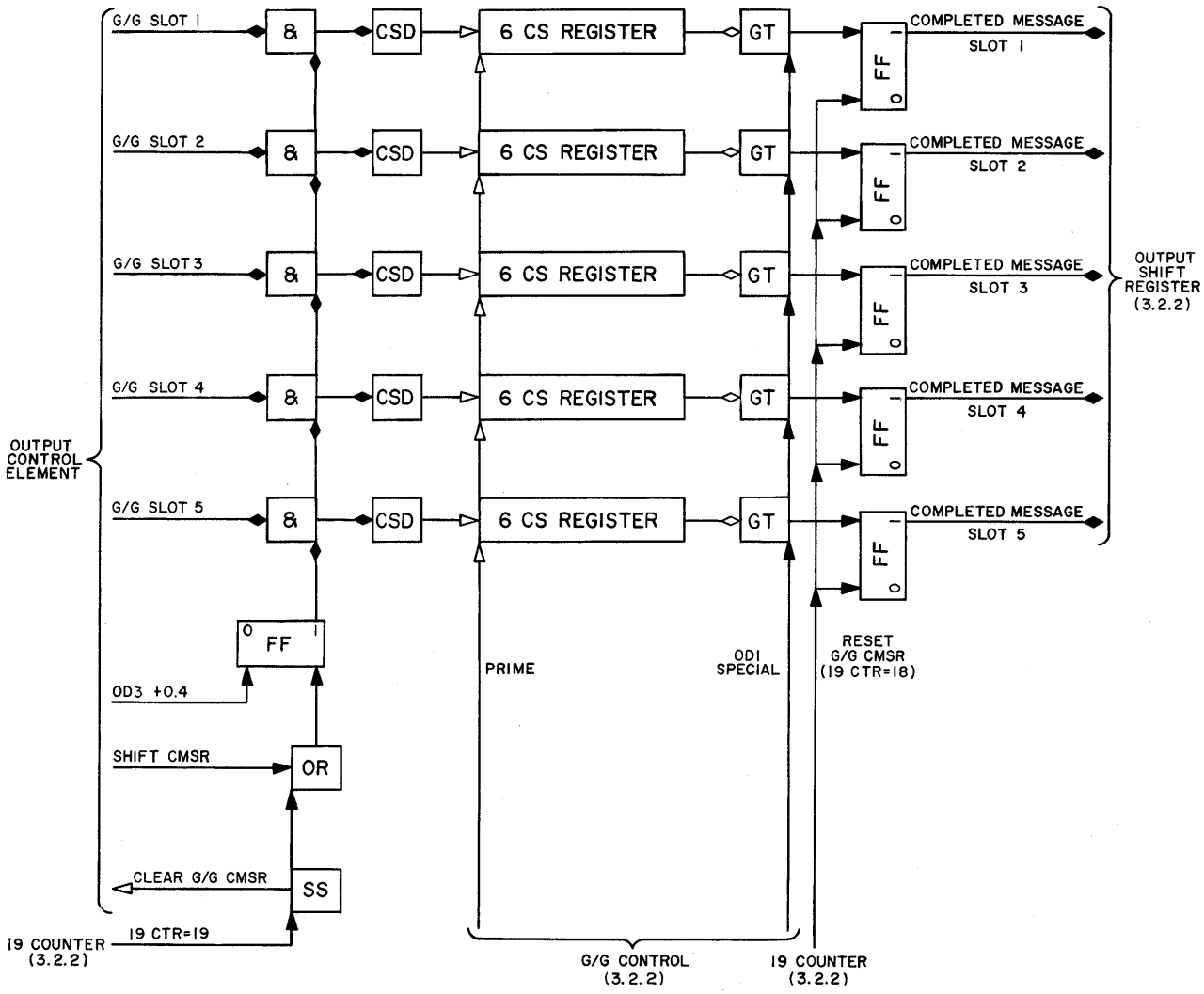


Figure 3–33. Completed Message Shift Register (3.2.2), Simplified Logic Diagram

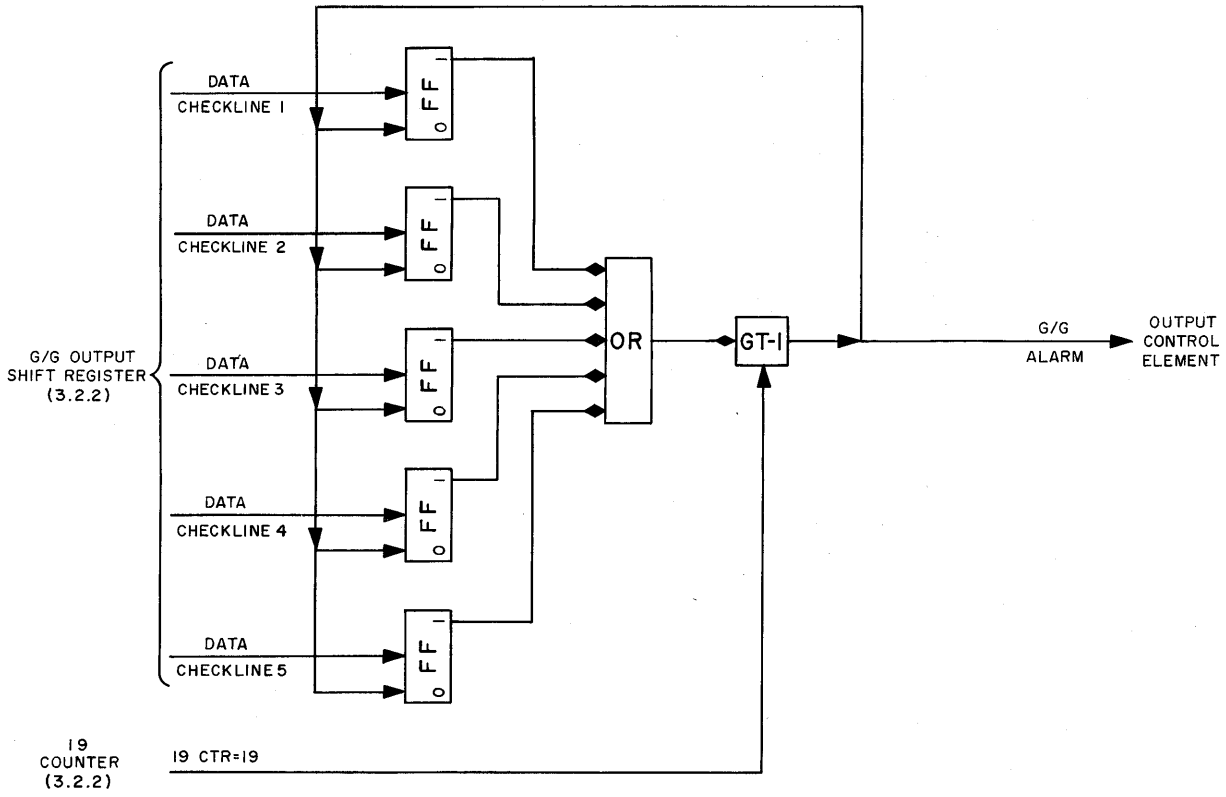


Figure 3–34. G/G Storage Parity Checking (3.2.2), Simplified Logic Diagram

tion, using the burst number as the identity code. As a word on the OB fields moves into reading position, bits L8 through L15 (which contain the assigned burst number) are read into a flip-flop register in the output control element. This register supplies to the G/G burst counter both the assigned burst number of the word and the complement of the assigned burst number. The assigned burst number of the word and the complement of the G/G burst counter contents are applied to an AND circuit, while the complement of the assigned burst number and G/G burst counter contents are applied to another AND circuit. If the assigned burst number matches the burst counter contents, the outputs of the AND's will be down. Since all the inputs to the OR circuit shown in figure 3–35 are down, the output of the inverter (compare-G/G) will be up. The word will therefore be accepted, and the output word will be written into the core storage array in the slot and register to which it was addressed by the left drum word.

If the assigned burst number of the words does not match the G/G burst counter contents, one or more AND outputs will be up, suppressing the compare-G/G level from the inverter. In this case, the drum word is not accepted and the search continues to the next word.

3.8 CONVERSION

Information leaving the G/G output shift register is modified by the conversion circuits before being fed

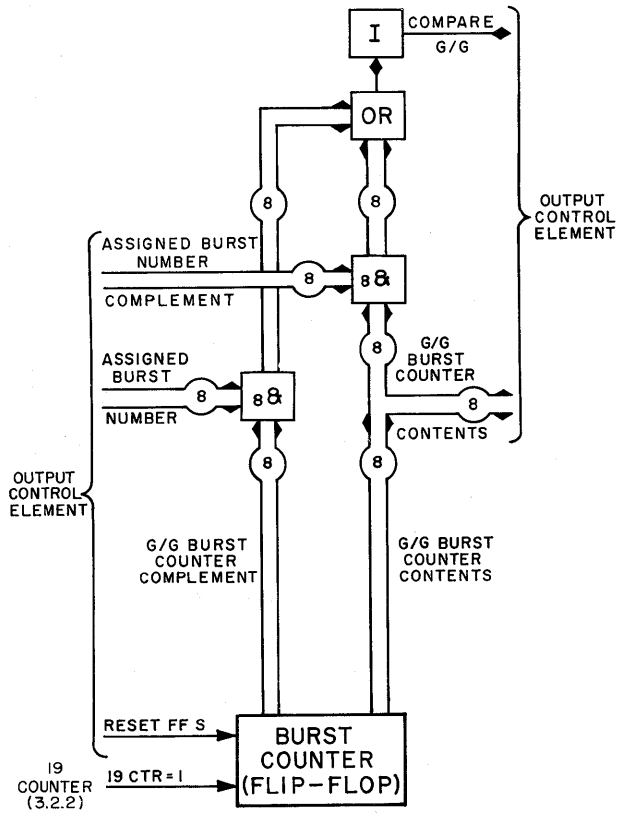


Figure 3–35. G/G Burst Counter (3.1.2), Simplified Logic Diagram

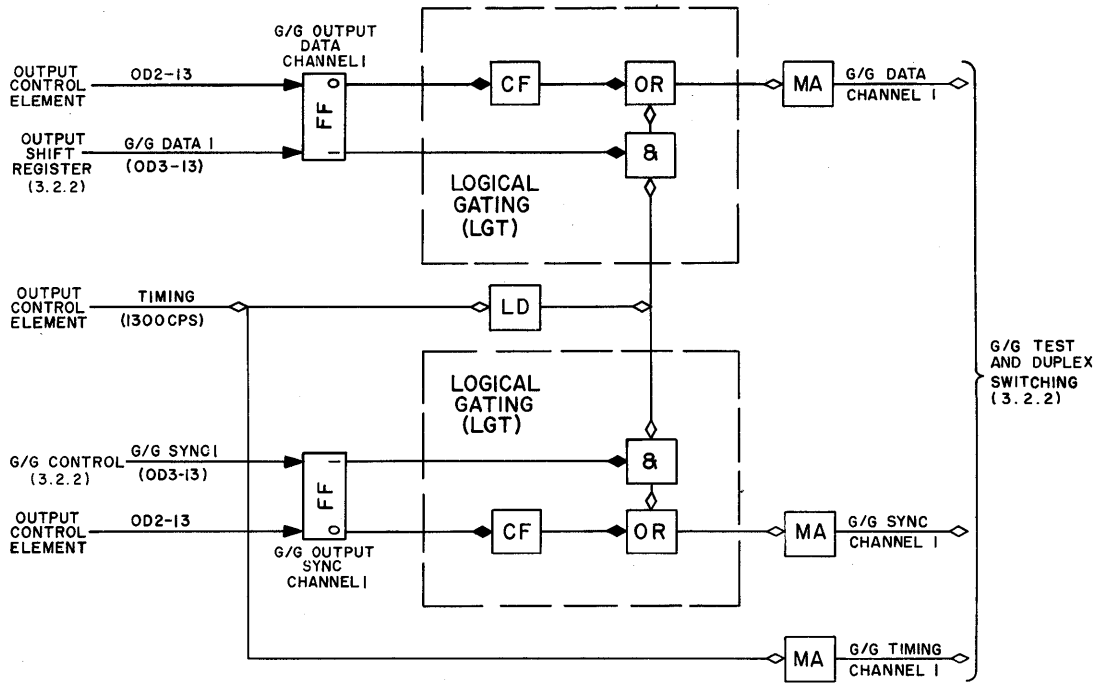


Figure 3–36. G/G Conversion, Message 1 (3.2.2), Simplified Logic Diagram

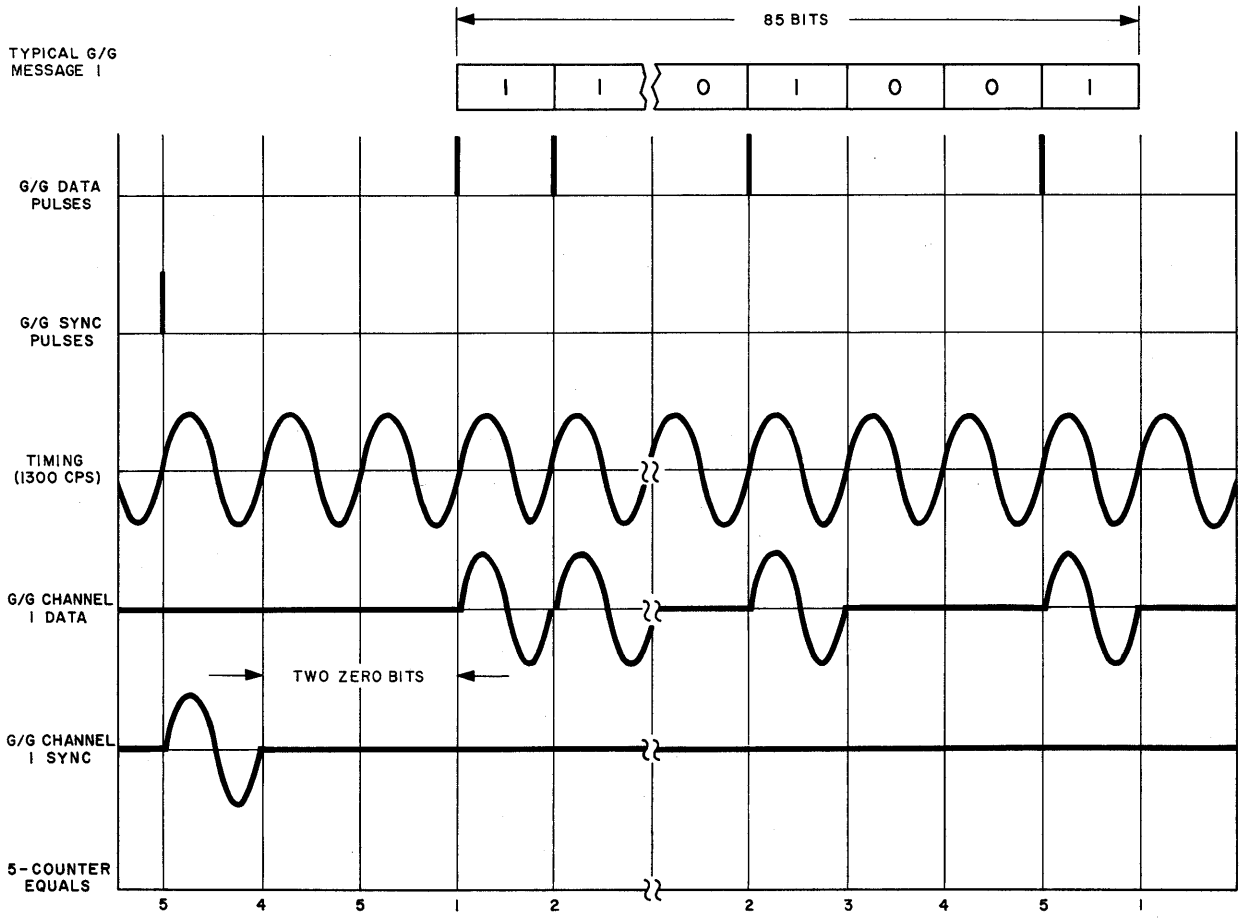


Figure 3–37. G/G Conversion, Input and Output Signals

through the switching circuits to the telephone transmission equipment. The conversion circuits convert the G/G data and sync standard pulses to a series of synchronized, gated, 1,300-cps sine waves. The information is modified in this manner to make it compatible with telephone company equipment requirements.

The conversion circuits contain five identical channels, one for each of the G/G messages. These channels are identical in circuitry and operation to the G/A-FD conversion channels described in 2.8.2. Figure 3–36 shows one of the five identical G/G message conversion channels, the channel for G/G message 1. For each data or sync pulse received, the conversion channel will transmit slightly less than one cycle of the 1,300-cps timing signal to the telephone equipment over the data or sync lines.

It is required that exactly two 0 bits occur on the data lines between the end of the output sync signal and the beginning of the first data bit. (See fig. 3–37.) This is accomplished by applying an OD 3–13 G/G sync pulse to the sync conversion channel simultaneously with the 19th shift of the 19 counter. Since two 5-counter shifts occur between 19-counter-19 and the start of readout which occurs at 19-counter-1 time (refer to 3.4.2), the required sync pattern (. . . 00S00) is obtained.

The data, sync, and timing inputs and outputs of one G/G message conversion channel for a typical G/G message are shown in figure 3–37. The outputs of this message channel, together with the outputs of the other four identical message channels, are fed to the switching circuits and from there sent out to the telephone equipment.

3.9 SWITCHING

The G/G test and duplex switching circuits control the G/G output of the Output System of each computer. The switching circuits contain relays which provide for the switching of each of the five G/G messages. However, the relay circuits for each message are identical. For this reason, figure 3–38 shows a simplified diagram of the G/G test and duplex switching circuits for only one G/G message.

The relays provided by the G/G test and duplex switching circuits are controlled so that only the Output System of the active computer is presented to the telephone line terminal equipment. Relays are also provided to enable the Output System on standby status to be switched to the appropriate test busses through the pattern generator. These relays are operated during test operations only.

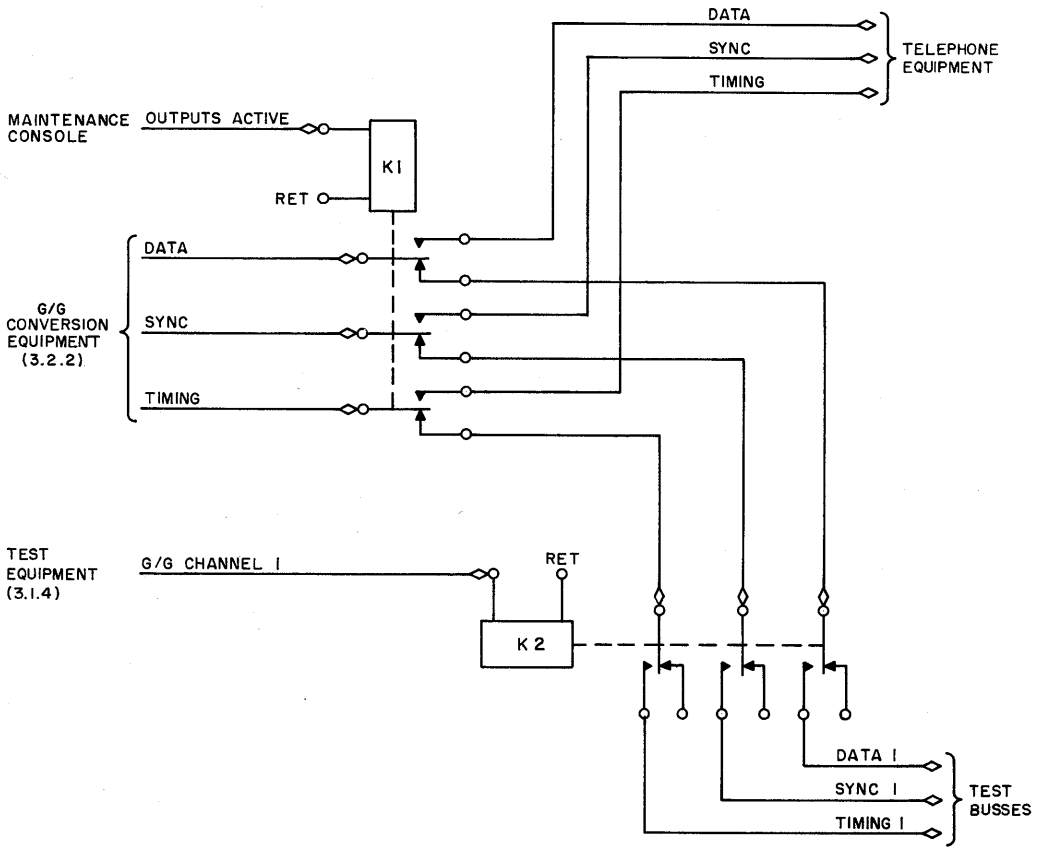


Figure 3–38. G/G Test and Duplex Switching, Message 1 (3.2.2), Simplified Diagram

CHAPTER 4

GROUND-TO-AIR TIME DIVISION STORAGE SECTION

4.1 GENERAL

The G/A-TD output storage section assembles output words received in parallel form from the output control element into messages, and then transmits these messages serially over telephone data channels to control manned interceptors. These messages are transmitted at a 1,300-pps rate. A simplified diagram of the G/A-TD storage section is shown in figure 3–39.

Three G/A-TD messages may be transmitted during a G/A-TD burst period. Each message is composed of four output words which are separated in groups of two words and transmitted over separate telephone channels to manned interceptors, via data-link transmitters. Each G/A-TD data-link transmitter that is located within a given area operates on the same assigned frequency. Selection of a particular data-link transmitter is established by the site address portion of a G/A-TD message. If a G/A-TD message is addressed to a particular aircraft in a group of interceptors, only that aircraft will take action on the transmitted message.

A parity check is performed on each output word to determine whether the original contents of the output word have been altered. There are an odd number of 1 bits present in each G/A-TD word, as opposed to the even number of 1 bits required in all G/A-FD, BOMARC, G/G, and TTY words.

The time required to read out all three G/A-TD messages in a G/A-TD core storage array is 90 ms. This is about equal to G/A-TD search time which is 86.2 ms. To eliminate the waste of telephone line time which would result if the line were not used during search time, two core storage arrays are included in the G/A-TD storage section. One array receives information while the contents of the other array are read out to the telephone line channels. Since two storage arrays are employed and search time for one storage array occurs simultaneously with the readout of the other, a G/A-TD burst period is set at 90 ms.

4.2 SYSTEM OPERATION

The G/A-TD storage section is logically divided into storage readout, control, message check, burst counting and compare, conversion, and switching circuits, as shown in figure 3–39. These circuits perform functions similar to the corresponding circuits of the G/A-FD, BOMARC, G/G, and TTY storage sections. However, since the G/A-TD storage section timing and word makeup differs somewhat from the other storage sections, a discussion of the G/A-TD circuits follows.

4.2.1 Counter Operation

The control circuits consist of the G/A-TD control, the 15 counter and the 17 counter. The two counters control the timing for the G/A-TD storage section. A brief discussion of these counters follows. The 17 counter is shifted at two rates, a 25-kc (40-μsec) fast-shift rate and the normal 1,300 cps (770-μsec) slow-shift rate, which are discussed in detail in 4.4.2 and 4.4.4. The 17 counter controls the shifting of the 15 counter. During one burst period, the 15 counter is shifted through a complete cycle of operation. A G/A-TD operational cycle consisting of read-in and readout of the two core storage arrays is described in subsequent paragraphs. The G/A-TD read-in interval and the readout interval for a single core array take place during successive burst periods. Thus, two G/A-TD burst periods are required for one G/A-TD core storage array to complete a cycle of operations. In actual operation, the read-in and readout functions occur simultaneously; as one core array is being written into, the other array is simultaneously being read out.

4.2.2 Read-In

The read-in operation of the G/A-TD storage section is similar to the read-in operation described for the G/G storage section except for the differences stated below.

In general, all counters are reset and primed in order to control the read-in of the G/A-TD word in the output section. The G/A-TD burst period begins at the first shift of the 15 counter. Search time for the G/A-TD storage section also begins at this time. The search level signals the G/A-TD output control element that read-in of the G/A-TD words can now take place. The G/A-TD output word to be read in is made up of bits RS through R15 plus an odd parity bit. It is to be noted that only in the G/A-TD section is an odd parity used. Like the G/G section, a pulse is sent to the CMSR to count the number of words loaded into each of the three message slots in a core storage array. One G/A-TD message slot contains four words.

The read-in of the G/A-TD words is completed before 15-counter-15 time. At 15-counter-15 time the

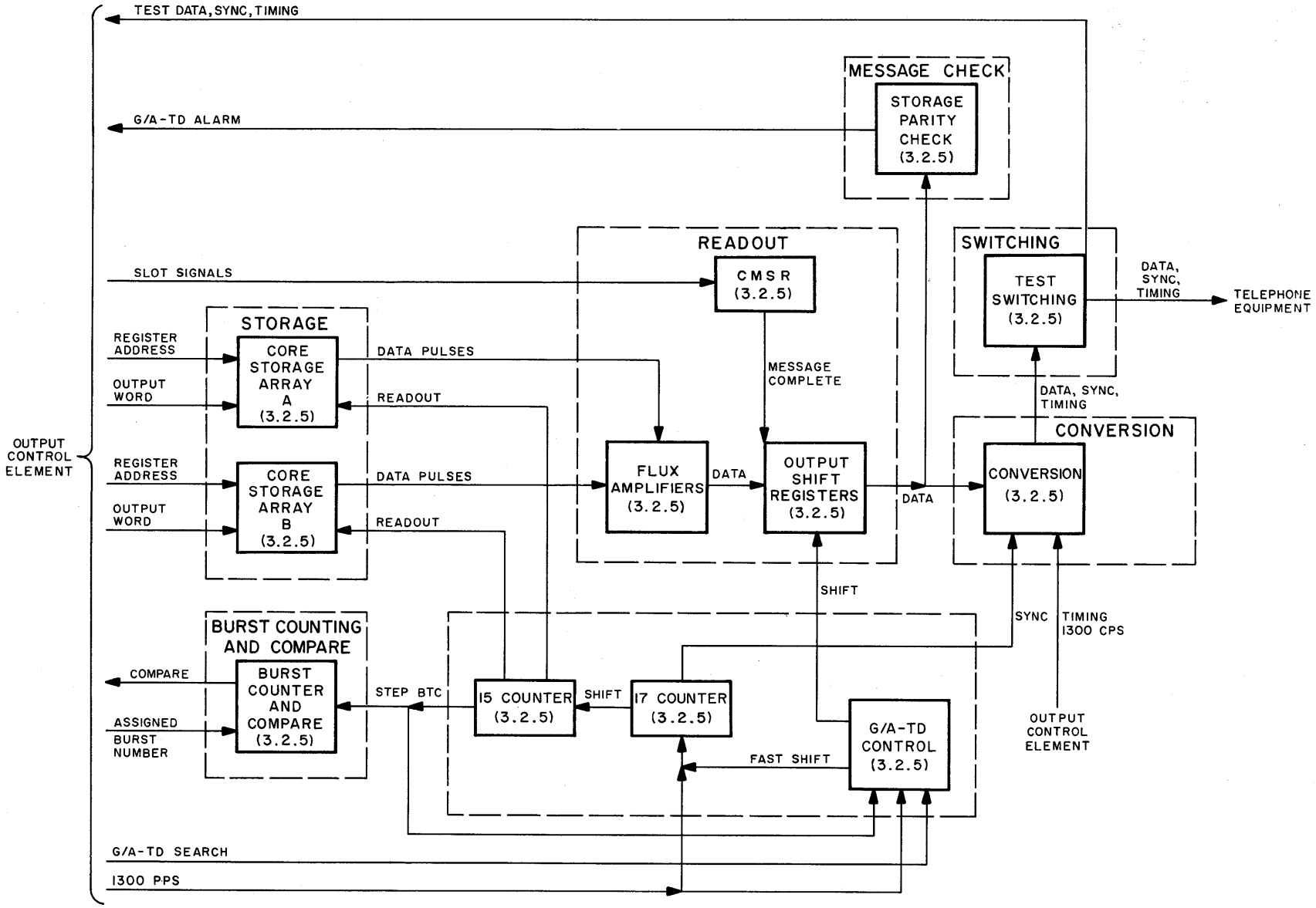


Figure 3–39. G/A-TD Output Storage Section, Simplified Block Diagram

G/A-TD control generates a not-search level and a shift-phase level. The not-search level prevents the output control element from writing into any more core registers. The shift-phase level switches core arrays so that the array just read into will be read out during the next burst period.

4.2.3 Readout

Readout of the core storage array that was written into in the previous cycle starts at 15-counter-1 time. In the G/A-TD storage section, two OSR's are used. At 15-counter-1 time, a clear-column pulse is generated to read out the first column in one of the selected storage arrays. The column of bits in this array are read out and sensed by the FA's where they are amplified to prime the cores of the first OSR. In the interval between 15-counter-1 and 15-counter-2 time, the word is fast-shifted from OSR 1 to OSR 2.

At 15-counter-2 time, the second clear-column pulse is generated to read out the second column of bits from the array into OSR 1. There are now two G/A-TD words contained in the OSR's; that is, register address 0 is in OSR 2 and register address 1 is in OSR 1. The latter is then shifted out in serial fashion only if there is a complete G/A-TD message made up of four words in a slot. This prevents the transmission of an incomplete G/A-TD message.

In the interval between 15-counter-2 and 15-counter-3 time, the words contained in OSR 1 and OSR 2 are shifted out serially under the control of the 17 counter to the conversion equipment, to the storage parity checking circuits, and to the test equipment section. In the storage parity checking circuits, the words are examined for proper parity (odd). If parity is even, a G/A-TD output alarm will be generated. Nevertheless, the G/A-TD word is allowed to go out over the phone lines regardless of output word parity.

In the conversion equipment, the information is made compatible with the phone line equipment. The test equipment circuits make use of the information received only if a unit-loop-test or computer-loop-test condition exists. These test modes are discussed in detail in Part 4.

At 17-counter-17 time, the last bits of the G/A-TD words are read out of both OSR's; at the same time, a pulse is gated to the 15-counter shift flip-flop. The output of this flip-flop will generate the next clear-column pulse at 15-counter-3 time. This, in effect, transfers the third G/A-TD word (register address 2) to OSR 1, whereupon it will be fast-shifted under the control of the 17 counter to OSR 2. When the next clear-column pulse is generated at 15-counter-4 time, the fourth G/A-TD word (register address 3) is read out of the core storage array into OSR 1. The third and fourth G/A-TD words are read out of the OSR's under the control of the 17 counter; this, then, completes the readout operation cycle for one complete G/A-TD message slot.

4.3 STORAGE

4.3.1 Core Storage Arrays

The output words comprising the G/A-TD messages are stored in ferrite core arrays. Each G/A-TD output word is 17 data bits in length, and is stored in one register column of the array. The array has 12 columns and 17 rows and can therefore store 12 output words. (See fig. 3–40.)

Two identical arrays are included to provide more efficient use of telephone channels. Each array is written into column by column and read out column by column; in this fashion, the G/A-TD storage array is read out word by word rather than bit by bit as in the G/A-FD, BOMARC, TTY, and G/G storage sections. As each word is transferred to the core storage array, a half-write current is applied to the register address winding of the column in which that word should be written. Simultaneously, right drum word half-write current pulses are applied to those row windings in which a 1 should be recorded. During readout, a read current pulse is applied to a clear-column winding. Each core in the column receives a full read current, with each core output appearing on the array output winding for its row. Corresponding row array output windings in the two arrays are wired in series. (See fig. 3–25.) No interference between matrices results, since only one array is read out at a time through use of gated TCD's.

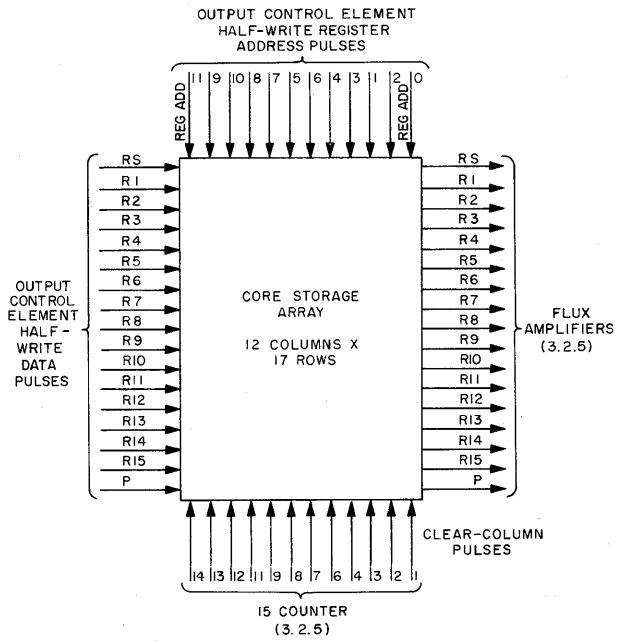


Figure 3–40. G/A-TD Core Storage Array, Simplified Logic Diagram

4.3.2 Core Array Read-In

During each burst period, G/A-TD message words are written into the core storage array which is not being read out. The right drum word with odd parity is applied by the output control element to the core storage array as half-write pulses on those drum word lines whose bits are 1's. The row in the array on which the word is written is specified by the register address contained in the left drum word. Thus, message assembly is accomplished by the assigned burst number and the register address. Since the search period for the OB fields is approximately 86.2 ms, read-in to one array can be completed during the 90-ms readout time for the other array.

The selection of an array for read-in is accomplished by the output control element. The G/A-TD control supplies that element with information on which array is being read out. The output control element, in turn, routes words for read-in into the other array.

4.4 CONTROL

4.4.1 General

While many of the control functions of the G/A-TD output storage section are managed by the output control element, certain functions unique to the section are managed by control circuits within the section. The control circuits for G/A-TD are the 17 counter, the frequency divider, the fast-shift circuits, the 15 counter, and associated control circuits.

4.4.2 17 Counter

The 17 counter, as shown in figure 3–41, is a 17-core ring counter which is cleared, primed, and then continuously stepped at a 1300-pps and also at a 25-kc rate (fast shift). The outputs of this counter are used

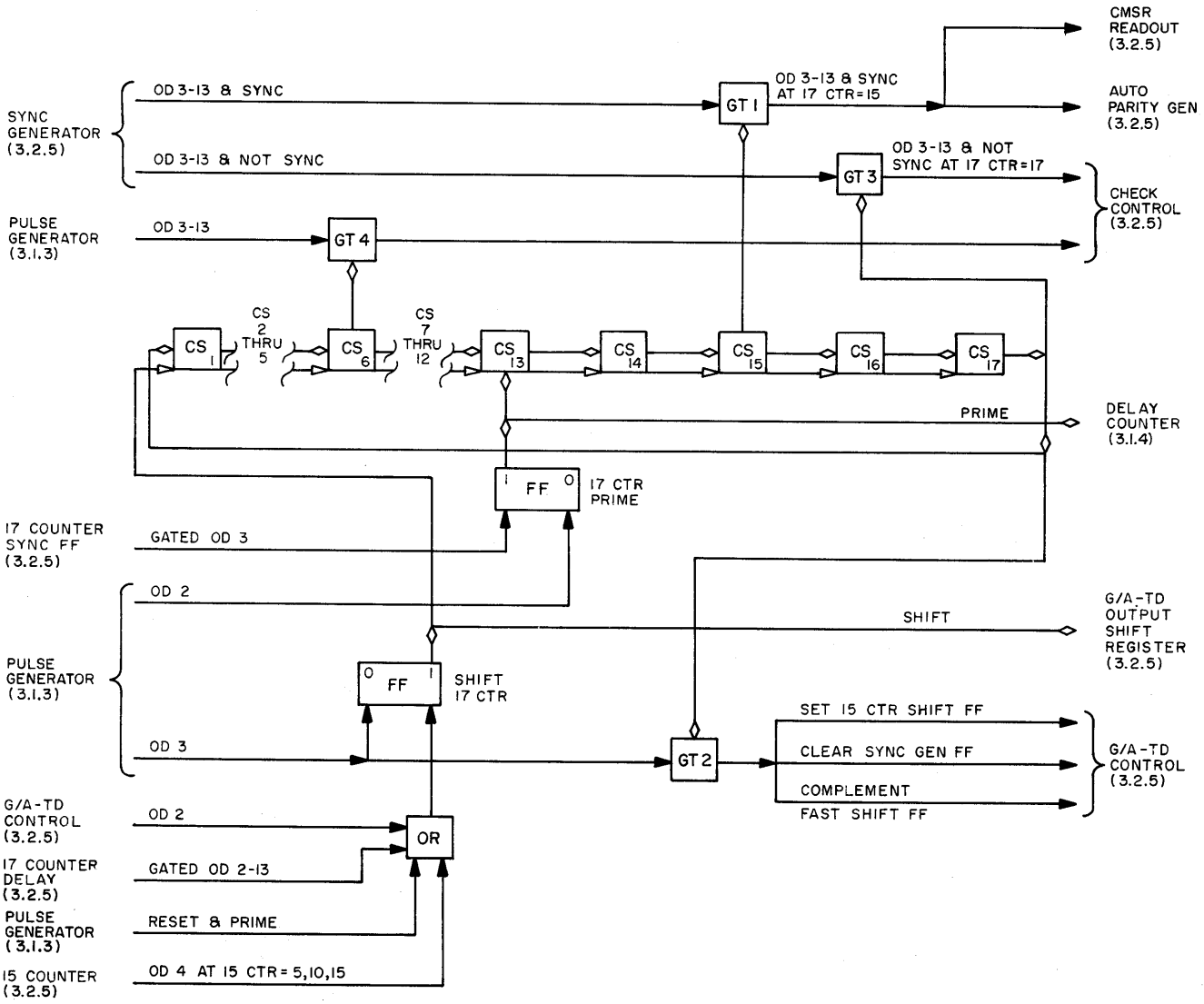


Figure 3–41. G/A-TD 17 Counter (3.2.5), Simplified Logic Diagram

to control certain functions in the G/A-TD storage section. The controlled functions are:

a. Generation of the G/A-TD sync pattern.
b. Stepping of the 15 counter.
c. Fast and slow shifting of G/A-TD words into and out of the OSR's.
d. Generation of parity bits to the phone line in the absence of a G/A-TD message or an incomplete message from the OB drum fields.

At the start of system operation or after a shutdown or test operation, the output control element sends an OD 4 reset-and-prime pulse via OR 1 to the 17-counter shift flip-flop and the G/A-TD control. This OD 4 pulse, in conjunction with the following OD 3 pulse, allows the 17-counter shift flip-flop to produce a 7.5-μsec reset level which clears (resets) the 17 counter and both OSR's. This reset level (7.5 μsec) is again generated whenever the 15 counter is stepped to 15-counter-5, -10, and -15. The latter reflects those times when a G/A-TD message (four words) has been read out of the OSR's to the phone lines. This same OD 3 pulse is gated to set the 17-counter prime flip-flop, which is normally cleared by a following OD 2 pulse. Setting of the 17-counter prime flip-flop generates a level to prime a 1 into the 13th core of the 17 counter (fig. 3–41). This priming allows for the generation of the G/A-TD sync pattern (00S00) that is required at the beginning of each G/A-TD message. The 1 bit is then shifted from the 13th core to the 14th core of the 17 counter; at the same time, both OSR's will also be shifted by 2.5-μsec shift pulses which are generated from the 17 counter shift flip-flop. During a normal shift cycle, this flip-flop is set by gated OD 2–13 pulses and cleared by the following OD 3 pulses. However, since no information is present in either OSR, the first 0 bit of the G/A-TD sync pattern is now generated. When the 17 counter is shifted to 17-counter-14 time, another 0 is sent to the phone lines. At 17-counter-15 time, GT 1 is conditioned to pass an OD 3–13 and sync pulse to set both G/A-TD output sync flip-flops in the DCT's, thus providing the synchronizing pulse of the sync pattern. In addition, the gated OD 3–13 and sync pulse clears the automatic parity bit generation flip-flop, thus preventing the generation of spurious 1 bits on the phone line. The generation of parity bits is discussed in detail in 4.4.6.4. Successive stepping of the 17 counter to 17-counter-16 and -17 time generates the remaining 0 bits of the sync pattern.

After the 17 counter steps to 17-counter-17, it returns to prime a 1 bit in the first core of the 17 counter. Also at this time, GT 2 is conditioned to pass an OD 3 pulse to complement the fast shift flip-flop to the set side. Since the sync pattern has been generated, this same gated OD 3 pulse will clear the sync generation flip-flop and cause the 15-counter shift flip-flop to be set. This, in effect, causes the 1 bit located in a core of the 15 counter to be shifted to its succeeding core.

When the 17 counter is shifted to 17-counter-6 time, a level will be generated to condition GT 4. (Refer to 4.4.6.4.) Conditioned GT 4 will pass an OD 3–13 pulse which is sent to the phone lines as an odd parity bit in lieu of G/A-TD words when the latter are absent from the phone lines.

4.4.3 Frequency Divider

The G/A-TD frequency divider circuit shown in figure 3–42 is a 2-stage flip-flop counter which is used to fast-shift the 17 counter and both G/A-TD OSR's at a 25-kc rate.

As shown in figure 3–41, OD 2 pulses are used to step the 17 counter. The operation of the counter is such that every fourth OD 2 pulse is gated to the fast-shift circuit. Hence, it can be seen from the figure that the frequency divider circuit supplies OD 2 pulses at a 40-μsec rate (25 kc) to the fast-shift circuit.

4.4.4 Fast-Shift Control

As previously mentioned in 4.2.3, readout of the G/A-TD word is accomplished by transferring a complete G/A-TD word out of the core storage array and into OSR 1. This G/A-TD word must then be shifted serially into OSR 2 before the following OD 3–13 time to prevent spurious data from appearing on the phone lines and to ensure that OSR 1 will be clear to receive the next incoming G/A-TD word from the core storage array. The fast-shift circuit (fig. 3–42) described below enables the above word transfer to be accomplished during the required time.

As shown in figure 3–42, at 17-counter-17 time the sync pattern has been generated and the OD 3 pulse, which is now an OD 3-at-17-counter-17 pulse, is passed to complement the fast-shift flip-flop to the set side. The output of the set side of this flip-flop conditions GT 3, which is strobed by OD 2 pulses occurring at a 40-μsec rate (25 kc) from the frequency divider.

These gated OD 2 pulses set the 17-counter shift flip-flop via OR 3. This flip-flop is cleared at the following OD 3 time; therefore, the 17 counter and both OSR's are fast-shifted through the complete 17 counter cycle. When the 17 counter is at 17-counter-17 time, an OD 3 pulse is passed to complement the fast shift flip-flop to the clear side, thus ending the fast-shift operation. A timing chart is presented in figure 3–43, foldout, to better illustrate the timing of the fast-shift control circuit.

4.4.5 15 Counter

The 15 counter, as shown in figure 3–44, foldout is a 15-core shift register which is cleared, primed, and then shifted by an OD 3 pulse at 17-counter-17. The outputs

of this counter are used for controlling certain functions in the G/A-TD storage section. These functions are:

a. Initiating the start of the G/A-TD search period
b. Stepping the G/A-TD burst time counter
c. Controlling the readout of each column in two arrays
d. Initiating the generation of the sync pattern for each succeeding G/A-TD message by resetting and priming the 17 counter.

At the start of the operation, the 15 counter shift flip-flop is set by an OD 3 pulse at 17-counter-17 time. The 15-counter shift flip-flop is cleared by a following OD 4 pulse. Thus, the flip-flop generates a 2.5-μsec shift pulse to shift the 1 bit from core 1 to core 2 of the 15 counter. When the bit is shifted from the first core to the second core in the counter, an output level is generated to condition GT 1 to pass an OD 4–13 pulse. This OD 4–13 pulse is used to set the search flip-flop and to step the G/A-TD burst time counter.

The output level generated by the first core of the 15 counter also causes the G/A-TD word contained in the first column of the selected array to be read out into OSR 1. In the interval between 15-counter-1 and 15-counter-2 times, the G/A-TD word now contained in OSR 1 is fast-shifted into OSR 2. At 15-counter-2 time, the second G/A-TD word is read out of the second column of the selected array into OSR 1. In the interval between 15-counter-2 and 15 counter-3 time, both G/A-TD words are shifted serially out of both OSR's at the same time to their respective phone lines. When the counter is shifted to 15-counter-3 and 15-counter-4, the remaining two G/A-TD words of slot 1 are read out of the selected array in the manner described for 15-counter-1 and 15-counter-2 times.

Readout of G/A-TD message slot 2 is performed in the same manner as that described for G/A-TD message slot 1. However, its readout time occurs from 15-counter-4 time through 15-counter-9 time.

Similarly, G/A-TD message slot 3 is also read out in the manner described for G/A-TD message slots 1

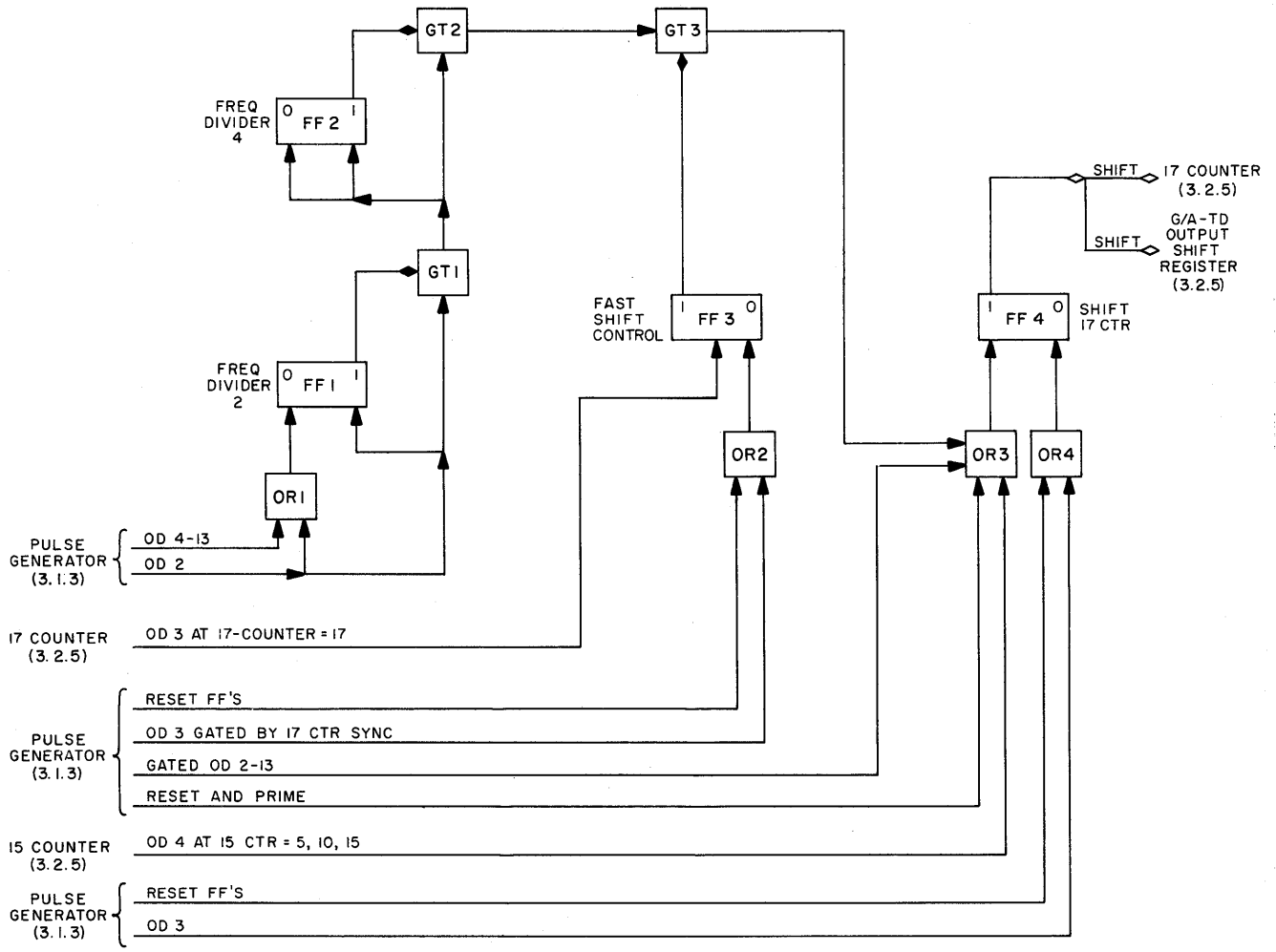


Figure 3–42. G/A-TD Frequency Divider, Fast-Shift Control, 17-Counter Shift Circuits, Simplified Logic Diagram

and 2; however, its readout time is from 15-counter-11 time through 15-counter-14 time.

At 15-counter-2 time, an OD 4 pulse is passed through GT 2 to the G/A-TD CMSR circuitry. This OD 4 pulse at 15-counter-2 time strobes the gate that is associated with the CMSR slot-1 flip-flop. If a complete message has been read into G/A-TD message slot 1, the gate will be conditioned to pass the OD 4 pulse at 15-counter-2 time to set the CMSR readout flip-flop. Setting this flip-flop permits the G/A-TD words of message slot 1 to be shifted out of OSR 1 and OSR 2 to the phone lines.

The operation described above is again repeated when the 15 counter is shifted to 15-counter-7 and 15-counter-12 time for the subsequent readout of G/A-TD message slots 2 and 3, respectively. The CMSR slot flip-flops (FF's 1, 2, and 3) are subsequently cleared whenever the 15 counter is stepped to 15-counter-12 time.

Whenever the 15 counter is shifted to 15-counter-5, -10, and -15, GT 5 passes an OD 4 pulse to set the sync generation flip-flop, the 17-counter shift flip-flop, and also the 17-counter sync flip-flop. Setting these flip-flops permits the generation of the G/A-TD sync pattern which must precede each G/A-TD message. G/A-TD sync pattern generation is discussed in detail in 4.4.2.

When the 15 counter has completed its operational cycle at 15-counter-15 time, GT 6 is conditioned to pass an OD 4—13 pulse. This pulse complements the phase flip-flops and clears the search flip-flop, thus ending the G/A-TD search period. In addition, this 15 counter-15 end-carry level is returned to the 15-counter shift circuitry, whereupon the 15 counter is reset in preparation for a new 15 counter cycle.

A timing chart is presented in figure 3—45, fold-out, to illustrate the overall timing process of the G/A-TD storage section.

4.4.6 Associated Control Circuits

In addition to the G/A-TD counters that are used for timing and control purposes in the G/A-TD storage section, other control circuitry is required to control the various operations listed below:

a. G/A-TD search and not-search
b. Array selection
c. 15-counter shift control
d. Automatic parity bit generation
e. 17-counter associated control circuits
f. Fast-shift control

4.4.6.1 G/A-TD Search and Not-Search

During search time, the G/A-TD storage section accepts messages from the OB drum fields into its respective core storage arrays. The G/A-TD search and not-search circuit generates the required search and not-search levels needed to begin and end the G/A-TD read-in operation.

As shown in figure 3—46, the required G/A-TD search level is generated when the search flip-flop is set by an OD 4—13 pulse at 15-counter-1 time. This flip-flop is cleared by an OD 4—13 pulse at 15 counter-15 time. Therefore, search time for a G/A-TD read-in operation is approximately 86.2 ms. When the search flip-flop is cleared, it remains in this state for a period of 3.85 ms. The latter constitutes the not-search period; that is, when no messages will be accepted from the OB drum fields by the G/A-TD storage section.

4.4.6.2 Array Selection

The G/A-TD storage section utilizes two core storage arrays which are used to store incoming G/A-TD messages. Since two core storage arrays are used, read-in and readout of the G/A-TD messages can occur simultaneously. The circuit which is used to select and control the G/A-TD read-in and readout operations is the phase circuit.

As shown in figure 3—47, selection of the particular G/A-TD core storage array to be read out is determined by the phase flip-flop. This flip-flop is complemented by an OD 4—13 pulse whenever the 15 counter is at 15-counter-15 time. Thus, the core storage array which was read into is now selected to be read out.

4.4.6.3 15-Counter Shift Control

The 15-counter shift flip-flop (fig. 3—48) is used to control the shifting of the 15 counter with 2.5-μsec shift pulses. Subsequent shifting of the 15 counter generates clear-column pulses to the core storage array columns to read out the G/A-TD words.

The 2.5-μsec shift pulses are also used to gate the FA's associated with the core-storage-array data output

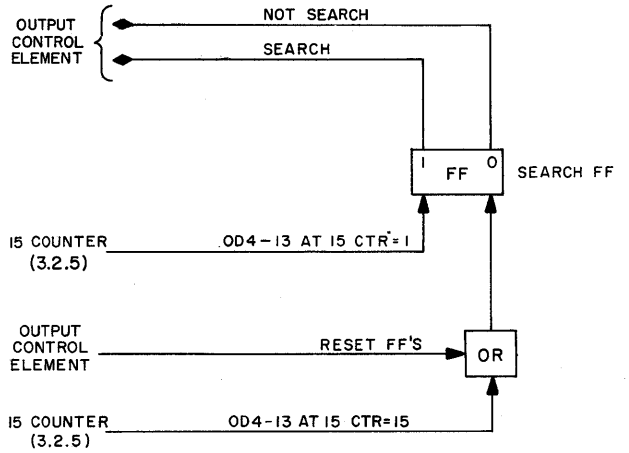


Figure 3—46. G/A-TD Search Flip-Flop, Simplified Logic Diagram

lines. These FA's, when gated, transfer the G/A-TD data that is read out of the array into OSR 1. Other functions of the G/A-TD shift control circuit are (1) generating a reset level to the 15 counter, (2) checking the CMSR's for completed G/A-TD messages, and (3) priming the G/A-TD CMSR's and the 15 counter.

As shown in figure 3–48, the 15 counter shift flip-flop is set by an OD 3 pulse at 17-counter-17 time, and is cleared by the following OD 4 pulse for every shift of the 15 counter except when the counter is at 15-counter-15 time. Hence, the 15 counter shift flip-flop generates shift pulses of 2.5-μsec duration which are used to shift the 15 counter and to condition the FA's as described above.

When the 17 counter is at 17-counter-17 time an OD 3 pulse is passed to set the 15-counter shift flip-flop. This flip-flop, when set, will cause the 15 counter to be stepped by 2.5-μsec shift pulses until the counter completes its operational cycle at 15-counter-15 time. At that time, a positive level is applied to the inverter. The output of this inverter deconditions GT 1, thus preventing the OD 4 pulses from clearing the 15-counter shift flip-flop.

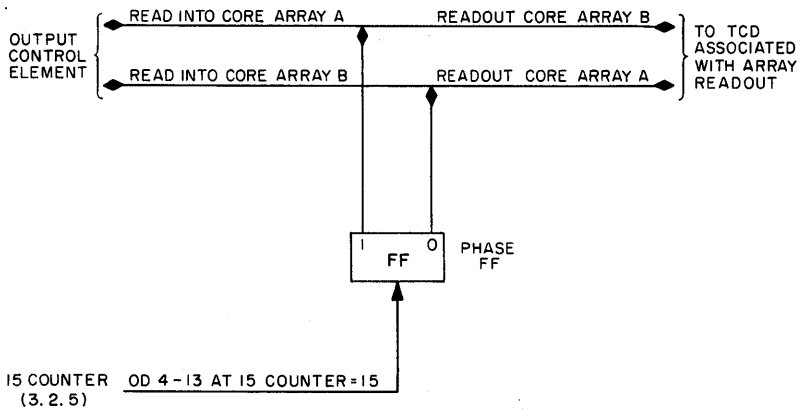


Figure 3–47. G/A-TD Array Selection (3.2.5), Simplified Logic Diagram

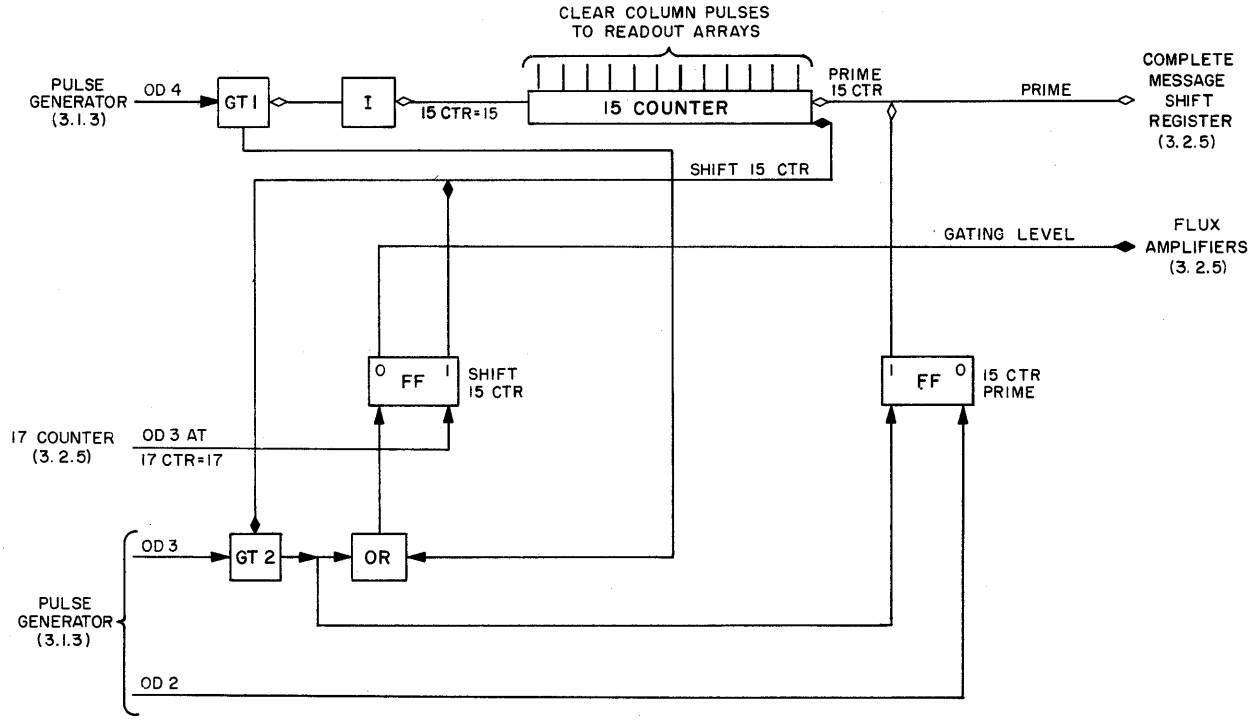


Figure 3–48. G/A-TD 15-Counter Control Circuits (3.2.5), Simplified Logic Diagram

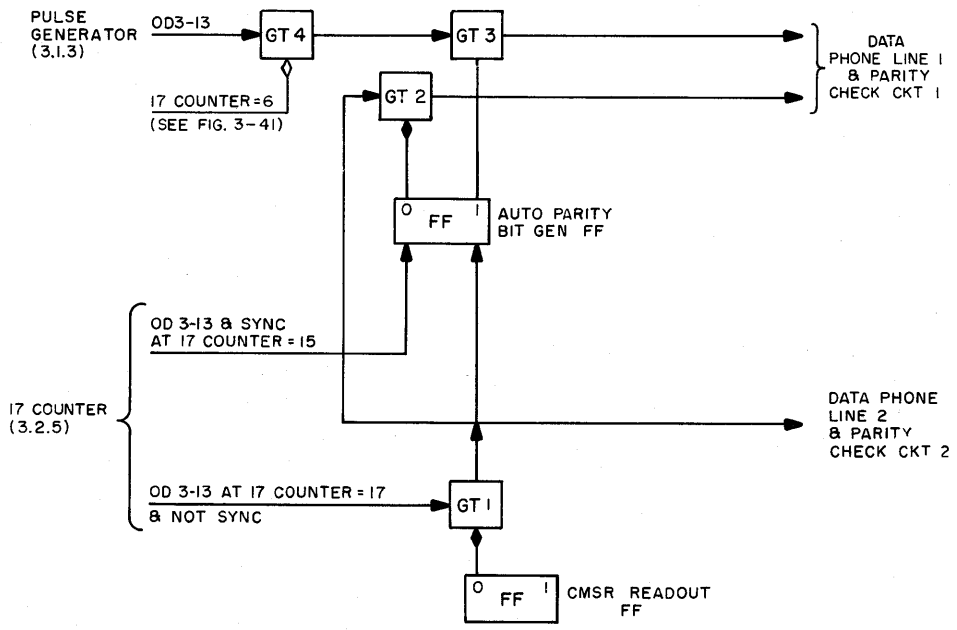


Figure 3–49. G/A-TD Auto Parity Bit Generator, Simplified Logic Diagram

The purpose of inhibiting the clearing of the 15-counter shift flip-flop at OD 4 time is to allow a 10-μsec level to be generated so that the 15 counter may be reset. This reset level is obtained by conditioning GT 2 (the shift flip-flop is set) and strobing it with OD 3 pulses. The OD 3 pulse occurring after the inhibited OD 4 pulse (7.5 μsec later) will be passed to clear the 15-counter shift flip-flop; at the same time, it will set the 15-counter prime flip-flop. The latter primes a 1 into the first core of each CMSR (there are three CMSR's) and also primes a 1 into the first core of the 15 counter in preparation for the start of a new 15-counter cycle.

4.4.6.4 Automatic Parity Bit Generation

The auto parity generator (fig. 3–49) is used to automatically place parity bits on the G/A-TD data phone lines whenever a particular G/A-TD message slot has not been filled with the prescribed number of four words. In the absence of a complete G/A-TD message, therefore, the auto parity generator will generate four parity bits (one 1 bit per G/A-TD word) to maintain the odd parity bit status required of G/A-TD messages (fig. 3–50). This action also prevents the generation of the G/A-TD output parity alarm. However, it is to be noted that auto parity generation will occur only at those times when particular G/A-TD message slots do not contain the required number of words (four) for transmission on G/A-TD data phone lines. Detailed operation of the parity generator circuit follows.

During the first normal shift cycle of the 17 counter at 17-counter-15, an OD 3–13-and-sync pulse is generated to clear the auto parity generator flip-flop. This same pulse is also used to generate the sync bit of the sync pattern. The latter precedes all G/A-TD messages.

When a slot is not filled, an incompleted-message level (shown in fig. 3–49) is generated by the 0 side of the CMSR flip-flop. The generated incompleted-message level is used to condition GT 1. The sync generator flip-flop produces an OD 3–13-and-not-sync pulse at the completion of the second normal shift cycle of the 17 counter; that is, at 17-counter-17 time. Therefore, at the conclusion of this second normal shift cycle of the 17 counter, this pulse will be passed by conditioned GT 1 to strobe GT 2, and will be sent to the parity checking circuit and the data phone line conversion equipment associated with phone line 2. The auto parity bit generator flip-flop (cleared at 17-counter-15 time by an OD 3–13-and-sync pulse) conditions GT 2. Hence, the OD 3–13-and-not-sync pulse which occurs at 17-counter-17 will thus be passed to the output converter and parity checking circuits associated with G/A-TD data phone line 1 (refer to 4.6). Thus, a parity bit is generated in lieu of the first G/A-TD word (word 1 or 3) that is absent from data phone lines 1 and 2. Referring to figure 3–50,B, it can be seen that the generated parity bits are inserted in bit position 22 for words 1 and 3.

The OD 3–13-and-not-sync pulse which occurs at 17-counter-17 time will also cause the auto parity bit generator flip-flop to be set. Setting this flip-flop conditions GT 3 so that, during the ensuing third normal shift cycle of the 17 counter, an OD 3–13 pulse, which is gated at 17-counter-6 time by GT 4, is passed

to strobe GT 3 (refer to 4.4.2). Conditioned GT 3 will therefore pass this OD 3–13 pulse which occurs at 17-counter-6 time to the output converter and parity checking circuits associated with G/A-TD data phone line 1. Thus, a parity bit is generated in lieu of the second G/A-TD word (word 2) that is absent from data phone line 1. Referring to figure 3–50,B, the generated parity bit is inserted in bit position 28 of word 2.

At the conclusion of the third, normal, slow shift cycle of the 17 counter, another OD 3–13-and-not sync pulse (at 17 counter-17) is passed through conditioned GT 1. From this gate, the pulse is then sent to the output converter and to the parity checking circuit associated with G/A-TD data phone line 2. Thus, a parity is generated in lieu of the second G/A-TD word (word 4) that is absent from data phone line 2. Referring to figure 3–50,B, the generated parity bit is inserted in bit position 39 of word 4.

During the fourth normal shift cycle of the 17 counter at 17-counter-15 time, the sync bit of the sync pattern is again generated. The generated sync pattern precedes the G/A-TD message contained in slot 2. At this time, the OD 3–13-and-sync pulse gated by the sync gen flip-flop at 15-counter-5 time will clear the auto parity bit generator flip-flop. The auto parity bit generator circuit is therefore once again ready to detect the absence of any G/A-TD messages from any of the G/A-TD message slots.

4.4.6.5 Associated Control Circuits, 17 Counter

The control circuits associated with the 17 counter are the 17-counter sync flip-flop, the 17-counter prime flip-flop, and the fast-shift control circuits. As shown in figure 3–51, the 17-counter-sync control circuit is used to set the 17-counter prime flip-flop, clear the fast-shift flip-flop, initiate the start-delay pulse to the delay counter, and, when used in conjunction with the 17-counter prime flip-flop, control the priming of both the delay counter and the 13th core of the 17 counter. The detailed operation of both the 17-counter sync flip-flop and 17-counter prime flip-flop follows.

When the 15 counter is shifted to the following 15-counter-5, -10, and -15 times, an OD 4 timing pulse is gated to set the 17-counter sync flip-flop via OR 1. Setting this flip-flop conditions GT 1, which is strobed by an OD 3 pulse. This OD 3 pulse is passed by conditioned GT 1 to set the 17-counter prime flip-flop and clear the fast-shift flip-flop; it is also sent to set the start delay flip-flop in the test equipment section and clear the 17-counter sync flip-flop via OR 2.

With the setting of the 17-counter prime flip-flop, a level is caused to be generated which is subsequently used to prime a 1 bit in the 13th core of the 17 counter, thus providing the start of the sync pattern generation cycle (described in 4.4.2) as well as priming a 1 bit in the first core of the delay counter in the test equipment section. (Refer to Part 4, par. 2.2.6.) The 17-counter prime flip-flop is then cleared at the following OD 2

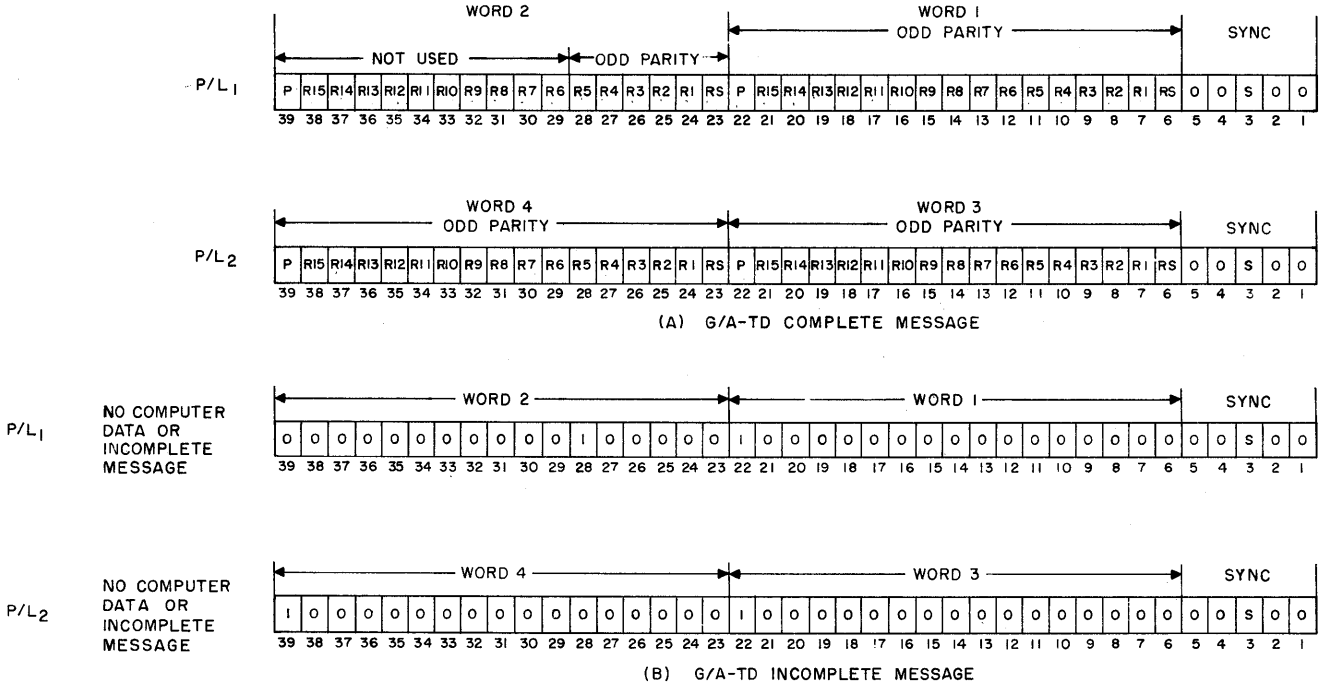


Figure 3–50. G/A-TD Word Message Layout

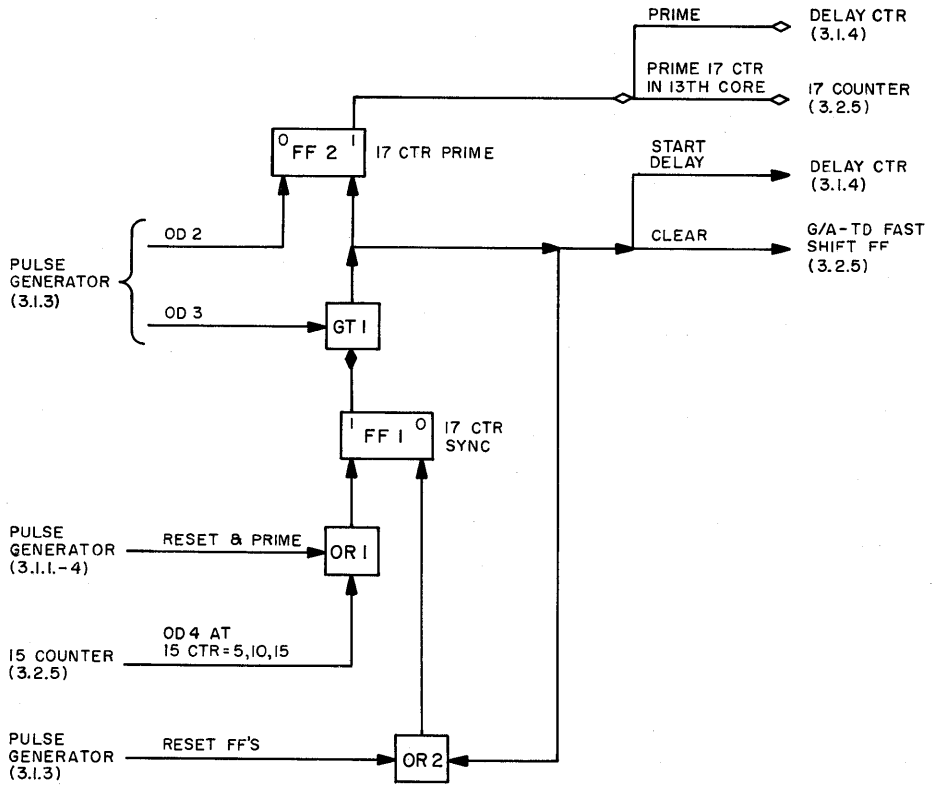


Figure 3–51. Associated Control Circuits, 17 Counter, Simplified Logic Diagram

time, thus ending the functions of the control circuits associated with the 17 counter.

The fast-shift control circuit (fig. 3–42) is also used in association with the 17 counter; it is mentioned only briefly because its operation is described in detail in 4.4.4.

4.5 READOUT

4.5.1 General

Readout of all G/A-TD messages is accomplished as follows:

a. Read out G/A-TD word 1 from selected array to OSR 1
b. Fast shift G/A-TD word 1 from OSR 1 to OSR 2
c. Read out G/A-TD word 2 from selected array to OSR 1
d. CMSR filled; read out complete G/A-TD message to G/A-TD data phone lines.

The above steps represent the mode of readout operations required for all G/A-TD messages. The following paragraphs contain discussions relating to the readout operations required to read out one of the three G/A-TD message slots from the G/A-TD core storage arrays.

4.5.2 Core Array Readout

Each G/A-TD message is read out of the G/A-TD core storage arrays one 17-bit column at a time, through FA's, into OSR 1. The message is subsequently fast-shifted into OSR 2. When both OSR's contain the two 17-bit columns representing two G/A-TD words, these two words will be shifted serially out of their respective OSR's to their respective data conversion equipment under the control of the G/A-TD completed message shift register.

As mentioned previously, each G/A-TD message slot is read out of the core array by columns during the G/A-TD burst period. Each core array is comprised of 12 columns which are pulsed serially by clear-column pulses that are applied by the TCD's associated with the 15 counter. Each time a column is pulsed, the 17 bits (representing a complete G/A-TD word) stored in its cores are shifted in parallel form to the FA's.

Each of the 17-bit output pulses from the G/A-TD core storage array is applied to an FA. A 1 bit is represented by a pulse, and a 0 bit is represented by the absence of a pulse. Each FA, shown in figure 3–52, is gated by a gating level emanating from the 0 side of the 15-counter shift flip-flop. These levels are 2.5-μsec negative pulses (OD 3 at 17-counter-17 to OD 4) used

to prevent noise and spurious signals from passing through the FA's. These pulses are produced in the G/A-TD control coincident with each shift of the 15 counter that occurs during readout time. (Refer to 4.4.6.) Since these 15-counter shifts generate clear-column pulses which read columns of the core array, the core storage array outputs are applied to the FA's during the 2.5-μsec period that the FA's are gated and made operative.

The FA's, after amplifying the array output pulses, send the pulses to both OSR's as FA outputs. The outputs from the FA's are sent over 17 lines labeled RS to R15 including P, respectively.

4.5.3 Output Shift Registers (OSR's)

The G/A-TD storage section utilizes two OSR's which store two G/A-TD words at one time (fig. 3–53). Each OSR is comprised of a 17-core shift register which is shifted at two specific rates. The first is called the normal shift rate which occurs at 1,300 pps and is used to shift the G/A-TD words out of the two OSR's onto the G/A-TD data phone lines and their respective parity checking circuits. The second shift mode is called the fast shift and is used specifically to fast-shift the first and third words of a particular G/A-TD message from OSR 1 to OSR 2. The latter mode is described in detail in 4.2.3 and 4.4.4.

Figure 3–53 is a representative diagram of the G/A-TD OSR's and their associated circuitry. Both

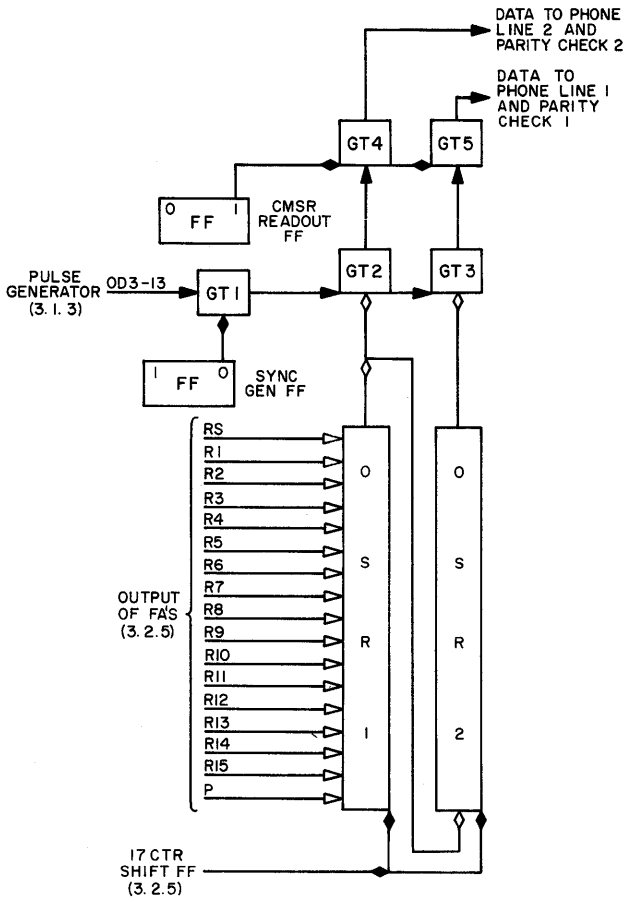


Figure 3–53. G/A-TD Output Shift Register, Simplified Logic Diagram

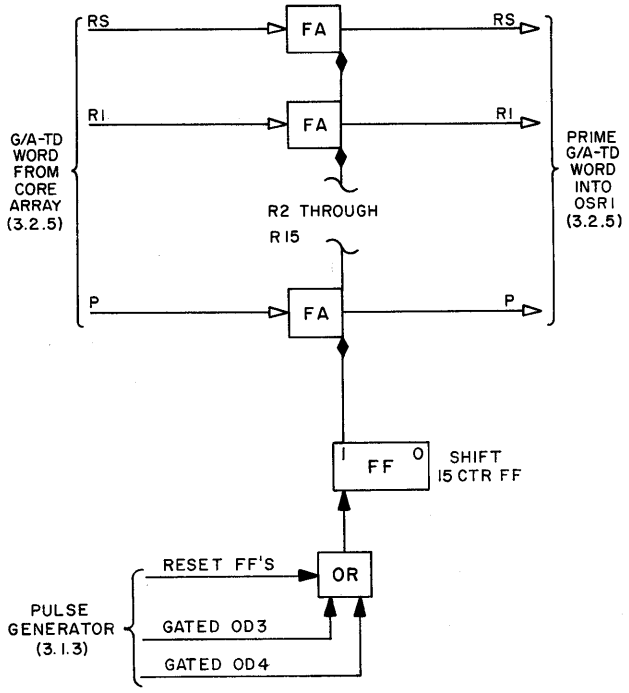


Figure 3–52. G/A-TD Flux Amplifiers (3.2.5), Simplified Logic Diagram

OSR's are shifted under the control of the 17-counter shift flip-flop. Readout of the G/A-TD words from the two OSR's to the data phone lines depends upon the CMSR flip-flop being set. The set condition of this flip-flop indicates that a complete message is contained in a particular G/A-TD slot, that this message is ready to be read out of the OSR's and that the sync gen flip-flop is clear. The latter flip-flop, when cleared, indicates that the sync pattern required to precede all G/A-TD messages has been generated and that readout of the G/A-TD message can now be executed.

During normal operation, a G/A-TD word is read into OSR 1 from a selected core storage array under the control of the 15 counter. The G/A-TD word now stored in OSR 1 is fast-shifted into OSR 2 under the control of the 17-counter shift flip-flop.

Subsequently, a second G/A-TD word is read into OSR 1 from the selected core storage array, with the result that two G/A-TD words are then stored in the OSR's. When a shift level is generated by the 17-counter shift flip-flop, readout of the two G/A-TD words from

the OSR's to the data phone lines will be effected in serial form at the normal shift rate of 1,300 pps.

For every 1 data bit that is read out of each OSR, the respective GT 2 and 3 associated with each OSR will be conditioned. Conditioned GT's 2 and 3 will then pass the gated OD 3–13 pulses passed by previously conditioned GT 1 (GT 1 is conditioned by the 0 side of the sync gen flip-flop) to strobe CMSR GT's 4 and 5. If the CMSR readout flip-flop has been set, GT's 4 and 5 will be conditioned to pass the 1 bits of each G/A-TD word on to data phone lines 1 and 2 and their respective parity checking circuits.

The above readout cycle is again repeated for readout of the third and fourth G/A-TD words. At the completion of the latter cycle, a complete G/A-TD message containing four words will have been read out to the data phone lines.

It is to be observed that, when the first and second G/A-TD words are read out of OSR 1 and OSR 2 to the data phone lines, the second G/A-TD word will, at the same time, be shifted into OSR 2. However, this second G/A-TD word is never read out of OSR 2 to the data phone lines because at the time when the third G/A-TD word is fast-shifted into OSR 2, the second G/A-TD word will also be fast-shifted out of OSR 2 to condition GT 3. Because no OD 3–13 pulses are present to strobe GT 3 during the fast-shift cycle, the second G/A-TD word data bits will not be passed by GT 3 and will therefore be destroyed.

The above condition will also prevail for the third and fourth G/A-TD words. In this case, however, the fourth G/A-TD word will not be fast-shifted as in the case of the second G/A-TD word but, instead, it will be destroyed at the completion of the G/A-TD message read out by a reset level of 7.5-μsec duration which is generated by the 17-counter shift flip-flop. The reset level generated by the 17-counter shift flip-flop clears both OSR 1 and OSR 2 as well as the 17 counter.

4.5.4 Completed Message Shift Register

The G/A-TD completed message shift register (CMSR) (fig. 3–54) counts the number of G/A-TD output words written into each slot in the core storage array. If four G/A-TD words are written into a slot during a burst period, the completed message in that slot will be passed through the OSR's to the conversion equipment. If the message slots do not contain the required complement of four words per slot, no messages are read out and the auto parity generator will be caused to generate odd parity bits on the data phone lines.

As shown in figure 3–54, three G/A-TD CMSR word counters are used, each capable of counting and recording the required four words needed to complete a G/A-TD message slot. Preparatory to the read-in and counting of the G/A-TD words during a burst period, the three G/A-TD CMSR slots are primed (refer to 4.4.6.3) under the control of the 15-counter prime flip-flop. The latter flip-flop primes a 1 into the first core of each CMSR, and also primes a 1 into the first core of the 15 counter.

Assuming that the ORA's of the G/A-TD words to be read in are addresses 0 through 3 (message slot 1), a conditioning, slot-1, level will be applied to one of two input lines of the 2-way AND circuit (AND 1 of fig. 3–54). Coincident with this level, a CMSR shift pulse (parity OK OD 2 + 0.5) is supplied through OR 1 to set the CMSR shift flip-flop. Setting this flip-flop causes a +10V level (2.5-μsec duration) to be applied to one input line of all three 2-way AND circuits associated with the G/A-TD CMSR's. The AND 1 circuit will be conditioned for a period of 2.5-μsec to shift the 1 bit that has been primed into its associated CMSR. This 1 bit is shifted one core at a time for each G/A-TD word that is read into message slot 1 of the selected core storage array. Thus, the CMSR counts the G/A-TD words contained in message slot 1 as these words are being read into the selected core storage array.

When a complete message has been read into the selected core storage array, the 1 bit will be located in the last core of the CMSR for slot 1. This operation, in effect, completes the read-in operation of the G/A-TD message in slot 1 during a G/A-TD burst period. Similarly, the operation described above will also take place for message slots 2 and 3 when these are being read into the selected core storage array.

The read-in operation of the G/A-TD words into a selected core storage array is completed when the 15 counter is at 15-counter-15 time. At this time, the following operational steps take place:

a. An OD 4–13 pulse is gated to complement the phase flip-flop (fig. 3–47) to select for readout the core storage array that has just been read into.
b. This OD 4–13 pulse clears the search flip-flop (fig. 3–46), ending search time.
c. This OD 4–13 pulse sets the CMSR shift flip-flop. The latter, when set, generates a level (+10V) that is applied to one input line of all three 2-way AND circuits associated with the CMSR's.
d. The OD 4–13 pulse also causes a single-shot multivibrator to fire; thus, a 25-μsec level (+10V) is applied to the remaining input lines of the three 2-way AND circuits and conditions these circuits.

The output of all three conditioned AND circuits is a reset level (7.9-μsec duration) that is applied to reset each of the respective CMSR's. Resetting the

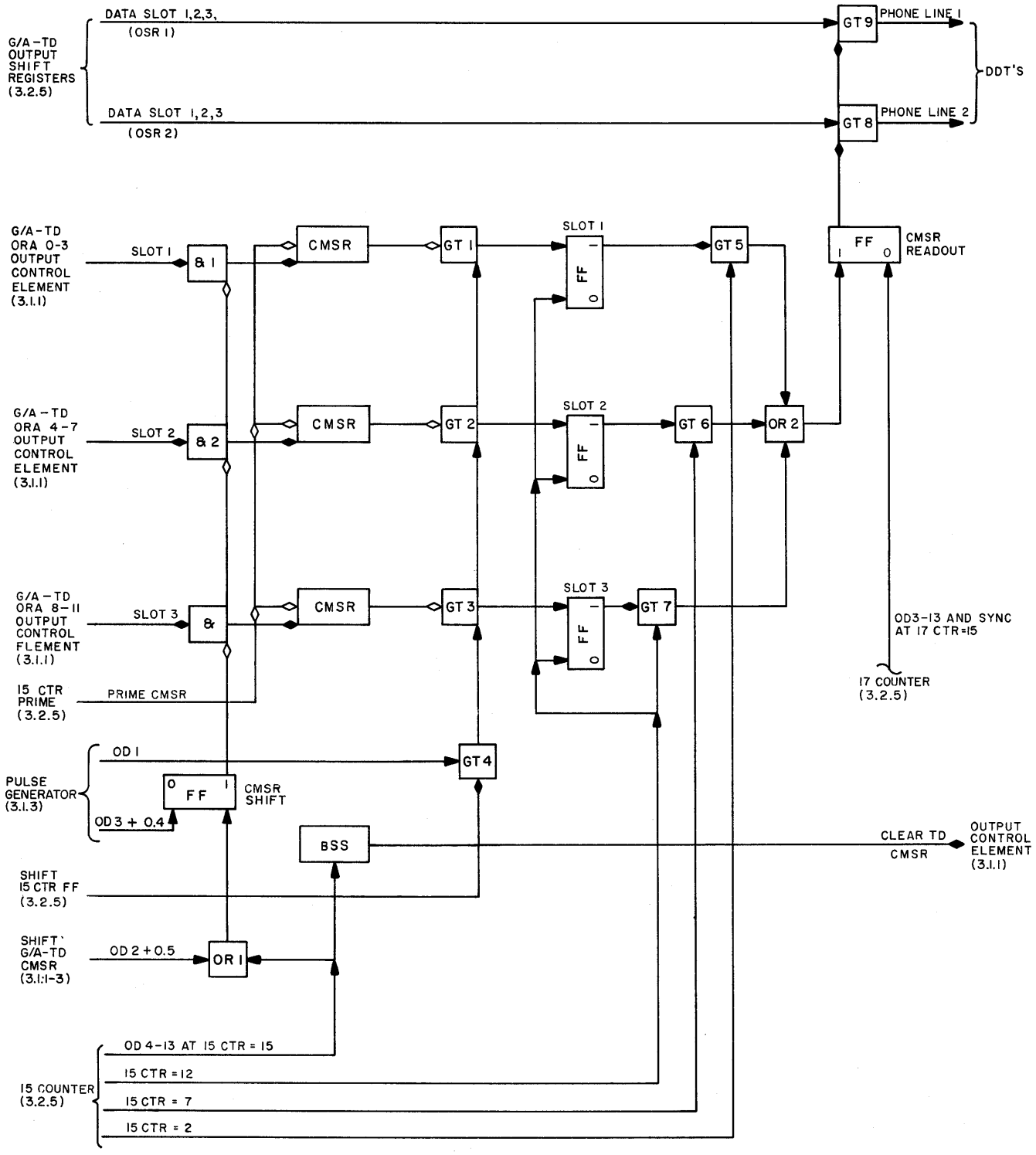


Figure 3–54. G/A-TD Completed Message Shift Register (3.2.5), Simplified Logic Diagram

CMSR's causes the 1 bits that are located in the last cores of each to be shifted out to condition the respective gate of each CMSR. All three gates (GT's 1, 2, and 3) are strobed by an OD 1 pulse that is passed through GT 4 only when the 15-counter shift flip-flop is set (for 10 μsec) at 15-counter-15 time.

Since GT's 1, 2, and 3 are conditioned, the OD 1 pulse which strobes each individual gate is passed to set the CMSR slot flip-flops. These flip-flops, when set, generate a conditioning level to their associated gates (GT's 5, 6, and 7). Conditioning the individual gates indicates that the message slot associated with each has been filled.

During the following 15-counter cycle, at 15-counter-2 time, an OD 4 pulse is gated to strobe GT 5. If a complete G/A-TD message was read into slot 1, the OD 4 pulse is passed through the OR 2 circuit to set the CMSR readout flip-flop. This flip-flop is cleared during the generation of the G/A-TD sync pattern (00S00) discussed in 4.4.2 by an OD 3—13-and-sync pulse which occurs at 17-counter-15. Setting the CMSR readout flip-flop causes a level to be generated to condition GT's 8 and 9, thus allowing for the subsequent readout of the complete G/A-TD message that was stored in slot 1 of the selected core storage array.

The readout operation for G/A-TD message slots 2 and 3 is the same as the operation described for message slot 1, with the exception that, for the readout of G/A-TD message slot 2, the gated OD 4 pulse is passed by GT 6 to set the CMSR readout flip-flop at 15-counter-7 time, and for the readout of G/A-TD message slot 3, the gated OD 4 pulse is passed by GT 7 to set the CMSR readout flip-flop at 15-counter-12 time. At 15-counter-12 time, this same OD 4 pulse also clears CMSR FF's 1, 2, and 3.

Should a particular G/A-TD message slot not contain the required four words necessary for a complete message, the particular gate associated with the incompleted message slot will remain deconditioned; hence, its respective CMSR slot flip-flop will remain cleared. Therefore, at the 15-counter-equals time for that particular slot, no pulse will be gated to set the CMSR readout flip-flop, and no message readout can occur for that slot.

4.6 PARITY CHECK

As the G/A-TD words are read out of the storage section to the data phone lines, a parity check of each word is performed. The parity of all G/A-TD words must be odd. However, if any G/A-TD words contain an even number of 1 bits, a G/A-TD output alarm is generated and the word containing the even number of 1 bits is nevertheless transmitted to the data phone lines.

Each G/A-TD word is simultaneously read out to the data phone line and the respective parity checking circuit. In the parity checking circuit (fig. 3–55), the G/A-TD word data intended for data phone line 1 is supplied through OR 2 to complement the parity check 1 flip-flop. The G/A-TD word data intended for data phone line 2 is supplied through OR 3 to complement the parity check 2 flip-flop. Should the transmitted G/A-TD words on data phone lines 1 and 2 be of the correct parity (odd) no alarm will be generated. Conversely, if either of the two G/A-TD words has an incorrect parity (even) when transmitted over data phone lines 1 and 2, the parity checking flip-flop associated with the incorrect word will be clear at the end of the parity check operation.

If either of the parity check flip-flops is clear, a level is generated through OR 4 to condition GT 2. Conditioned GT 2 is strobed by and passes a gated OD 1 pulse to initiate the G/A-TD output alarm. This OD 1 pulse is passed through GT 1 when the parity check control flip-flop is set. This flip-flop is set by an OD 3—13-not-sync pulse when the 17 counter is at 17-counter-17 time. This pulse appears in coincidence with the readout of the last data bit of every G/A-TD word that is transmitted over data phone lines 1 and 2. The parity check control flip-flop is cleared by the gated OD 1 pulse, 5 μsec after it was set. Clearing this flip-flop ends the parity checking operation for the transmitted G/A-TD words and, at the same time, readies the parity checking circuitry to check the parity of the succeeding G/A-TD words to be transmitted.

In the absence of a complete G/A-TD message, the auto parity generator discussed in 4.4.6.4 (fig. 3–49) generates an odd parity bit in lieu of an absent G/A-TD word. The data-1 bits generated by the parity generator are fed to OR 2 and OR 3 to complement the respective parity check flip-flops associated with each data phone line, thus ensuring that no G/A-TD alarm is generated.

4.7 BURST SEQUENCE AND TIMING

4.7.1 General

The G/A-TD burst counter and compare circuit and the burst number of the assigned G/A-TD message are the basic means employed to control the order and time of transmission of messages. The assigned burst numbers of each drum word are compared to the current contents of the burst counters. If the assigned burst number is equal to the contents of the G/A-TD burst counter, and if all other conditions are favorable, the word is accepted by the Output System.

To be sure that the message is transmitted in proper sequence and at the proper time, the Central Computer System assigns a burst number to each G/A-TD message to which the reading of the G/A-TD burst counter will

be equal at the predicted transmission time. Each word of a burst is assigned the same burst number by the Central Computer System. To make it possible for the Central Computer System to determine this burst number, it is given access to the current readings of the G/A-TD burst counter through the output computer section of the output control element.

4.7.2 Burst Counter

The G/A-TD burst counter (fig. 3–56) is a standard 8-bit flip-flop counter having a scale of 256. This counter is stepped by each 15-counter-1 pulse which corresponds to the start of search time for each G/A-TD burst period. The 15 counter requires 90 ms to complete one cycle of operation.

The 8-bit burst count produced is fed to the computer section of the output control element and to the G/A-TD compare circuitry. The output levels from the 1 side of the flip-flops in the burst time counter are sent to the computer section, whereas both the 1 and 0 sides of these same flip-flops are sent to the compare circuit. A reset-flip-flop signal from the output control element is supplied to reset the burst counter after shutdown or test operations.

4.7.3 Burst Number Comparison

The G/A-TD compare circuit (fig. 3–57) is used to determine which words in a given burst period are to be accepted from the OB fields. The burst number of each G/A-TD output word is fed into the G/A-TD compare circuit where it is then examined to ascertain whether it is equal to the contents of the G/A-TD burst time counter. If the G/A-TD compare circuit finds that the counts are equal, it generates a G/A-TD-compare signal. Conversely, if the burst counts are found to be unequal, a no-compare signal is generated.

The G/A-TD compare circuit comprises 16 2-way AND circuits, five 4-way OR circuits, and one inverter. Each AND circuit is fed a bit from the burst number supplied by the Central Computer and a bit from the G/A-TD burst counter. Although these two bits are numerically equal, they represent opposite states; that is, while one bit represents a 1, the other represents its complement, which is 0. Under these conditions, an AND circuit produces a signal only when corresponding bits of the assigned burst number and the current count of the burst counter are unequal. When they are equal, all 16 2-way AND circuits produce a —30V output level. The AND circuits are connected to four OR

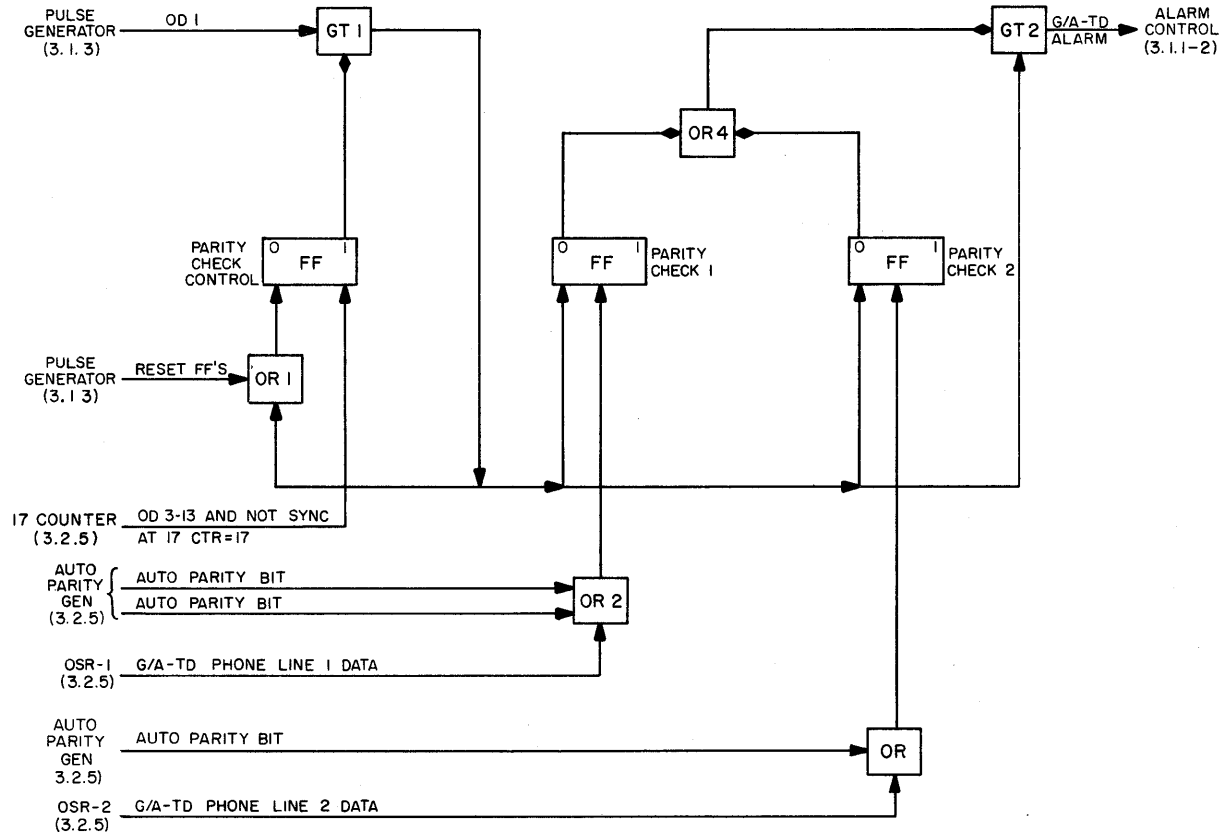


Figure 3–55. G/A-TD Parity Check Circuit (3.2.5), Simplified Logic Diagram

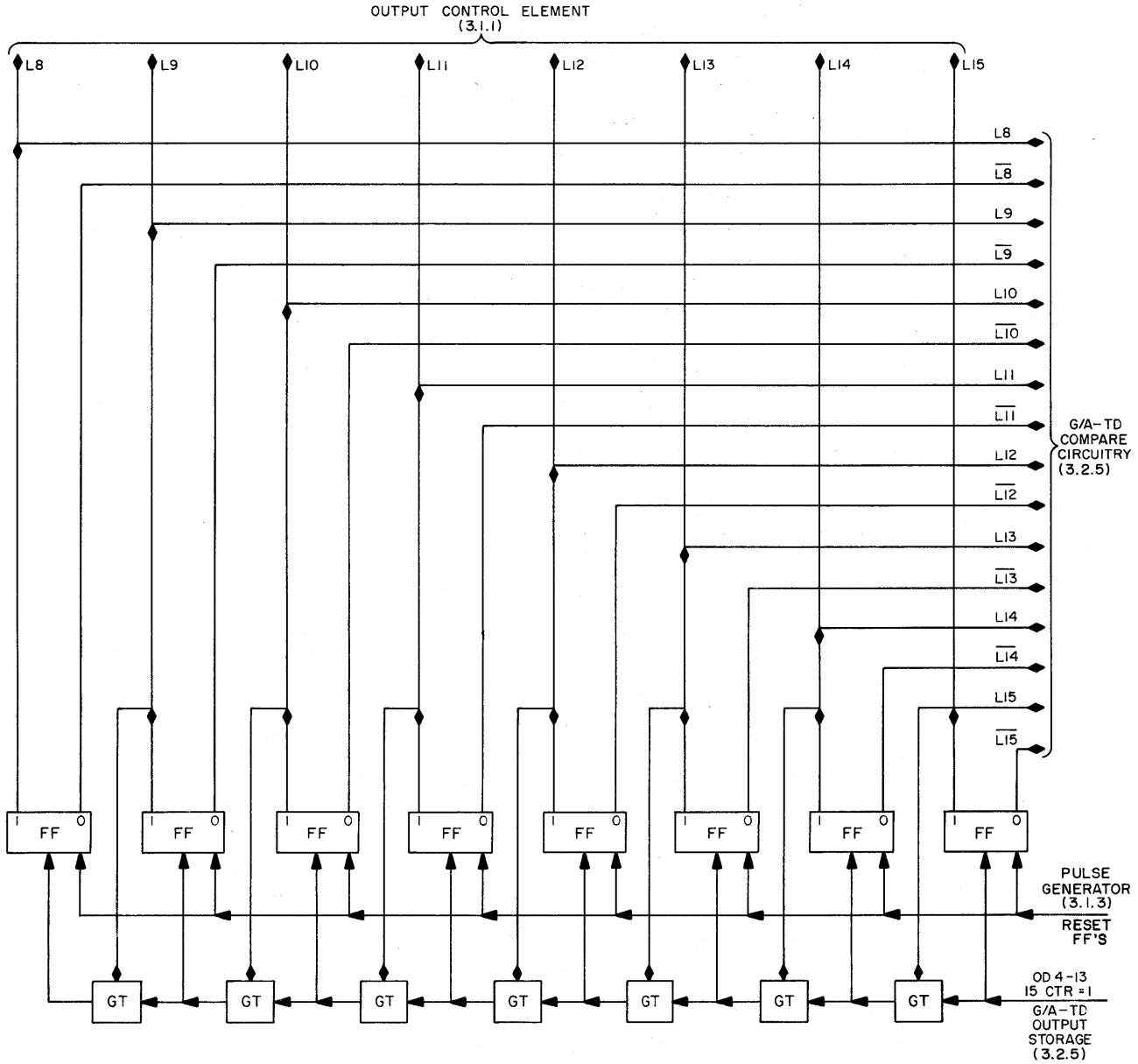


Figure 3–56. G/A-TD Burst Counter (3.1.2), Simplified Logic Diagram

circuits which, in turn, are connected to a single OR circuit. Therefore, the —30V level emanating from the AND circuits is passed by the OR circuits and applied to the inverter. The output of the inverter is a +10V level which is then sent to the output control element as a G/A-TD compare level.

Should the assigned burst number and the burst time count be unequal, one or more of the AND circuits will produce a +10V level which is passed by the OR circuits (fig. 3–57) and applied to the inverter. The output of the inverter is a —30V level which is then sent to the output control element as a G/A-TD no-compare level.

4.8 CONVERSION

4.8.1 General

Information leaving the G/A-TD OSR's is sent to the conversion circuits prior to being fed through the switching circuits to the telephone transmission equipment. The conversion circuits convert the G/A-TD data and sync information, which consists of standard 0.1-μsec pulses, to a series of synchronized, gated, 1,300-cps sine waves. The information is modified in this manner to make it compatible with telephone company equipment requirements.

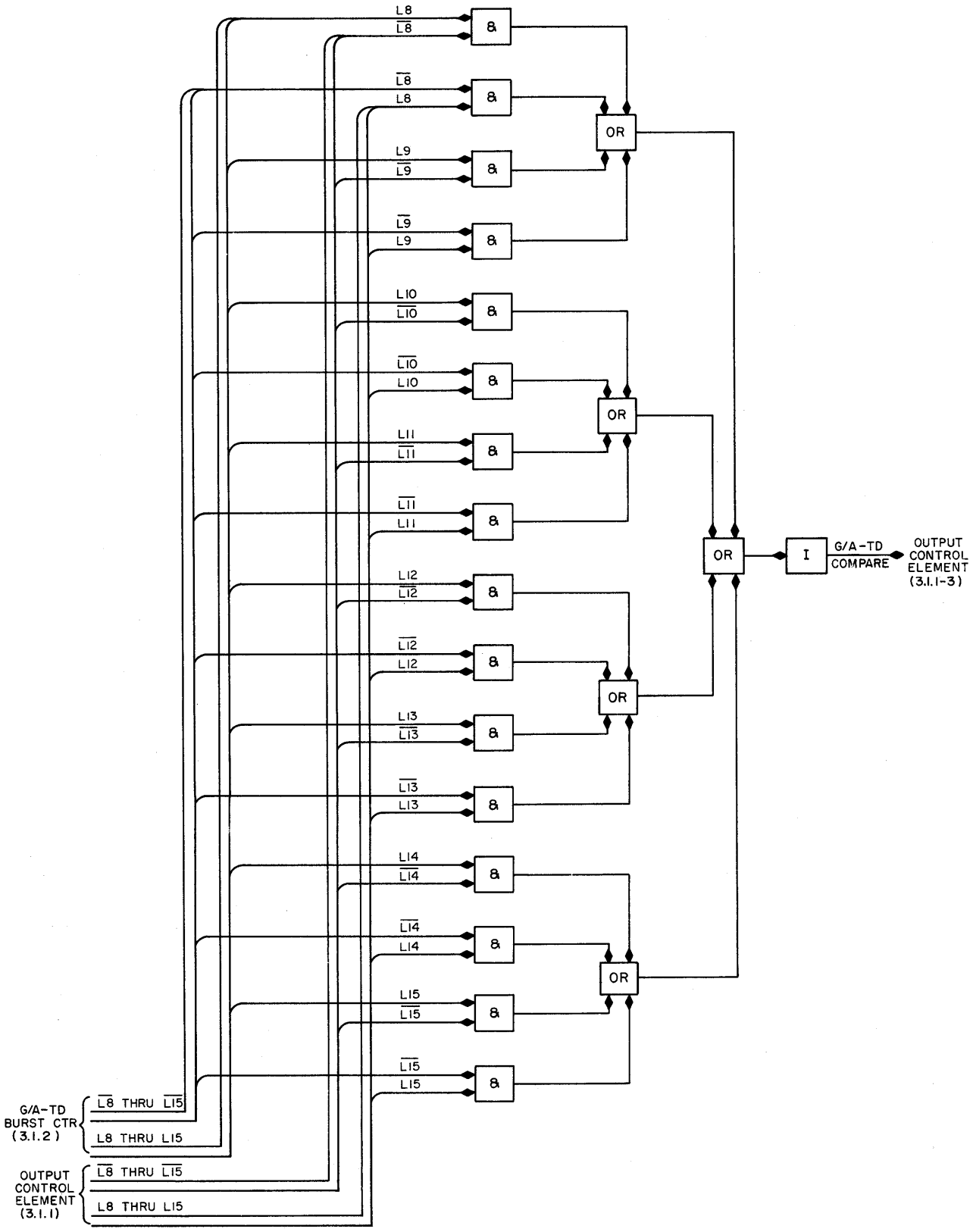


Figure 3–57. G/A-TD Compare (3.1.2), Simplified Logic Diagram

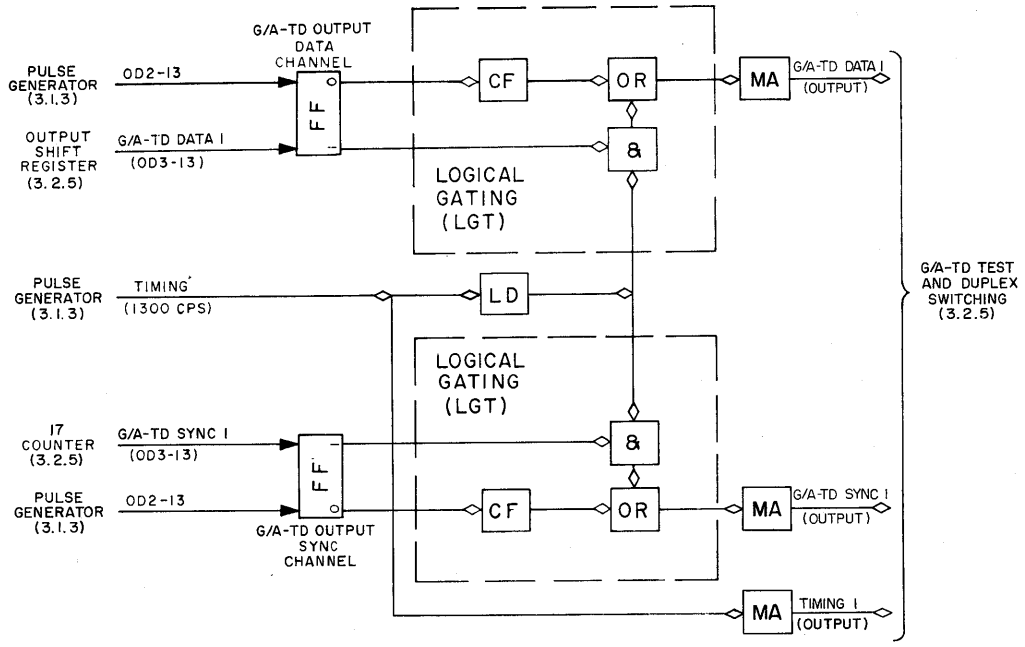


Figure 3–58. G/A-TD Conversion, Message 1 (3.2.5), Simplified Logic Diagram

4.8.2 Conversion Equipment

4.8.2.1 General

All of the conversion circuits are contained in the G/A-TD conversion equipment. This equipment is comprised of two identical channels, each capable of transmitting one G/A-TD word (half a message) at a time. Each channel contains a data conversion channel, an identical sync conversion channel, and a timing channel. The data and sync conversion channels perform the required conversion on their respective information inputs. The timing channel serves to match the timing signal, a 1,300-cps sine wave, to the telephone equipment, but does not modify its waveshape. The two channels are identical in operation. For this reason, the detailed operation of only one channel is presented in the following paragraphs.

4.8.2.2 Data Conversion Channel

Ground-to-air time division data is either a standard pulse occurring at OD 3–13 time to represent a 1 bit or the absence of this pulse at this time to represent a 0 bit. This data is applied to the G/A-TD output data channel 1 flip-flop. This flip-flop is set by G/A-TD data pulses and cleared by the following OD 2–13 timing pulses (fig. 3–58).

The G/A-TD output data channel 1 flip-flop supplies an input level to the 2-way AND circuit component of a logical gating (LGT) circuit. The LGT is comprised of this AND circuit plus a cathode follower and an OR circuit. The other input to the 2-way AND circuit is the 1,300-cps timing signal. The output of the AND circuit is either the timing signal or a —30V level, depending on whether the flip-flop is set or clear, respectively.

The flip-flop also supplies an input level to the OR driver cathode follower component of the LGT circuit. This cathode follower generates a clamped ground or a —30V output level, depending on whether the flip-flop is clear or set, respectively.

The AND circuit and cathode follower outputs constitute the inputs to the OR circuit component of the LGT circuit. The output of this OR circuit is either the 1,300-cps timing signal or a ground level, depending on whether the flip-flop is set or clear, respectively. This output is sent to the telephone equipment via the MA circuit.

When the flip-flop is set by receipt of a 1 bit (i.e., a standard pulse occurring at OD 3–13 time), the data conversion channel sends a 1,300-cps sine wave to the telephone equipment. This sine wave continues until the flip-flop is cleared by the following OD 2–13 pulse. Since the OD 3–13 pulses recur at a 1,300-cps rate and the OD 2–13 pulse precedes the next OD 3–13 pulse by 2.5 μsec, the interval between an OD 3–13 data pulse and the following OD 2–13 clear pulse will be 2.5 μsec less than the period of the 1,3000-cps timing signal. Therefore, for each 1 bit received by the flip-flop, slightly less than one cycle of the 1,300-cps timing signal will be sent to the telephone equipment. When the flip-flop remains clear due to the absence of a 1 bit (i.e., the absence of a standard pulse), a ground level will be sent to the telephone equipment.

4.8.2.3 Sync Conversion Channel

The sync conversion channel shown in figure 3–58 operates in a manner identical with the data conversion channel just described. For each sync pulse received, the sync conversion channel transmits slightly less than one cycle of the 1,300-cps timing signal to the telephone equipment. The sync pulse is applied to the conversion equipment at such a time that exactly two 0 bits occur on the data lines between the end of the output sync signal and the time that the first data bit is transmitted over the data lines. (See fig. 3–59.) This timing, which is necessary for decoding in the airborne receiver, is obtained by having an OD 3–13 sync pulse occur at 17-counter-15 time just prior to the readout portion of each burst period. (Refer to 4.2.3.) The sync pulse, therefore, precedes the data pulses, which are read out starting with the second 17-counter-equals-1 pulse, by two 17-counter shifts. In this manner, two 0 bits (the absence of two data pulses on the data lines at OD 3–13 time) occur between the receipt of the sync pulse and the start of the data pulses (00S00).

The data, sync, and timing inputs and outputs of one channel of the G/A-TD conversion equipment for a typical G/A-TD message are shown in figure 3–59. The outputs of this channel, together with the outputs of the second identical channel, are fed to the switching circuits and from there are sent out to the telephone equipment.

4.9 SWITCHING

The G/A-TD test and duplex switching circuits control the output of the Output System of each computer. The switching circuits contain relays which provide for the switching of each G/A-TD message. However, the relay circuits for each message are identical. For this reason, figure 3–60 shows a simplified diagram of the G/A-TD test and duplex switching circuits for only one G/A message.

The relays provided by the G/A-TD test and duplex switching circuits are controlled so that only the Output System of the active computer is presented to the telephone line terminal equipment. Relays are also provided to enable the Output System on standby status to be switched to the LRI test busses through pattern generators. These relays are operated during test operations only.

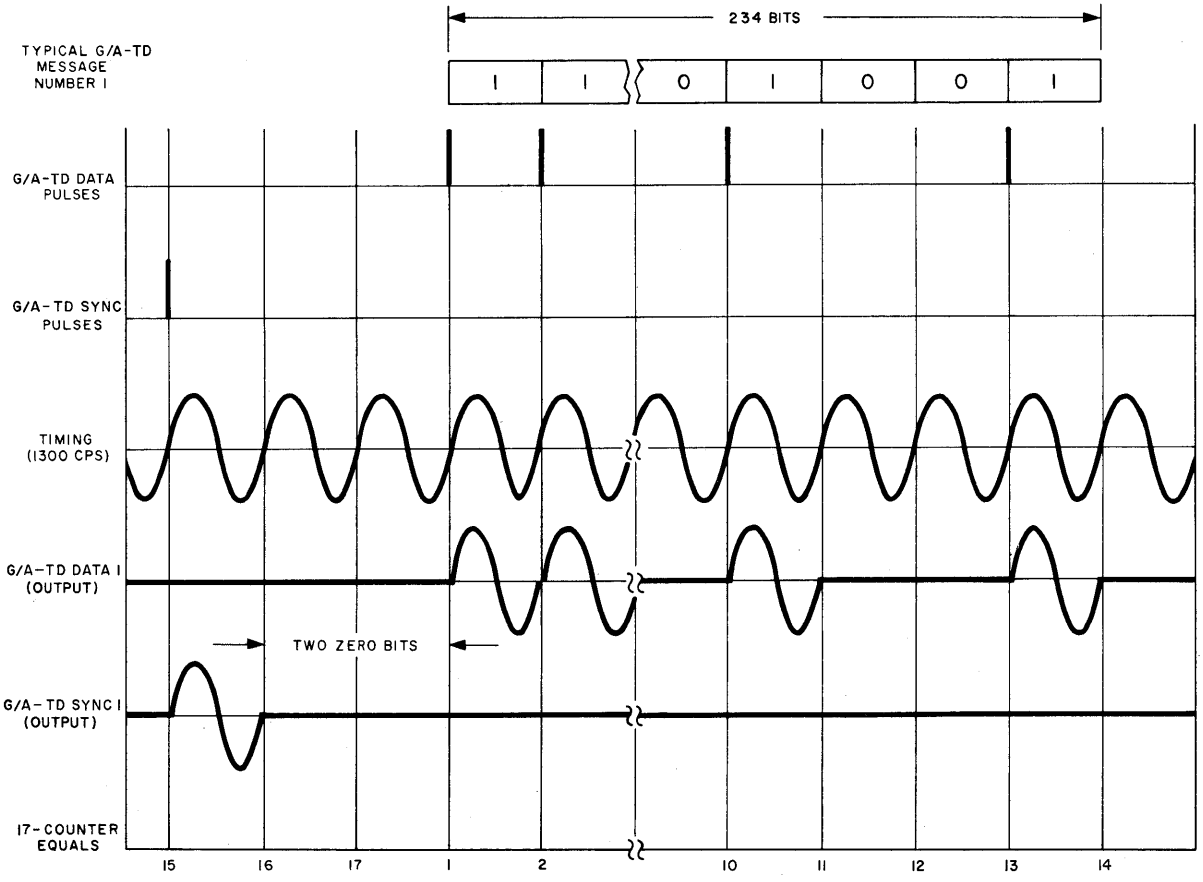


Figure 3–59. G/A-TD Conversion, Input and Output Signals

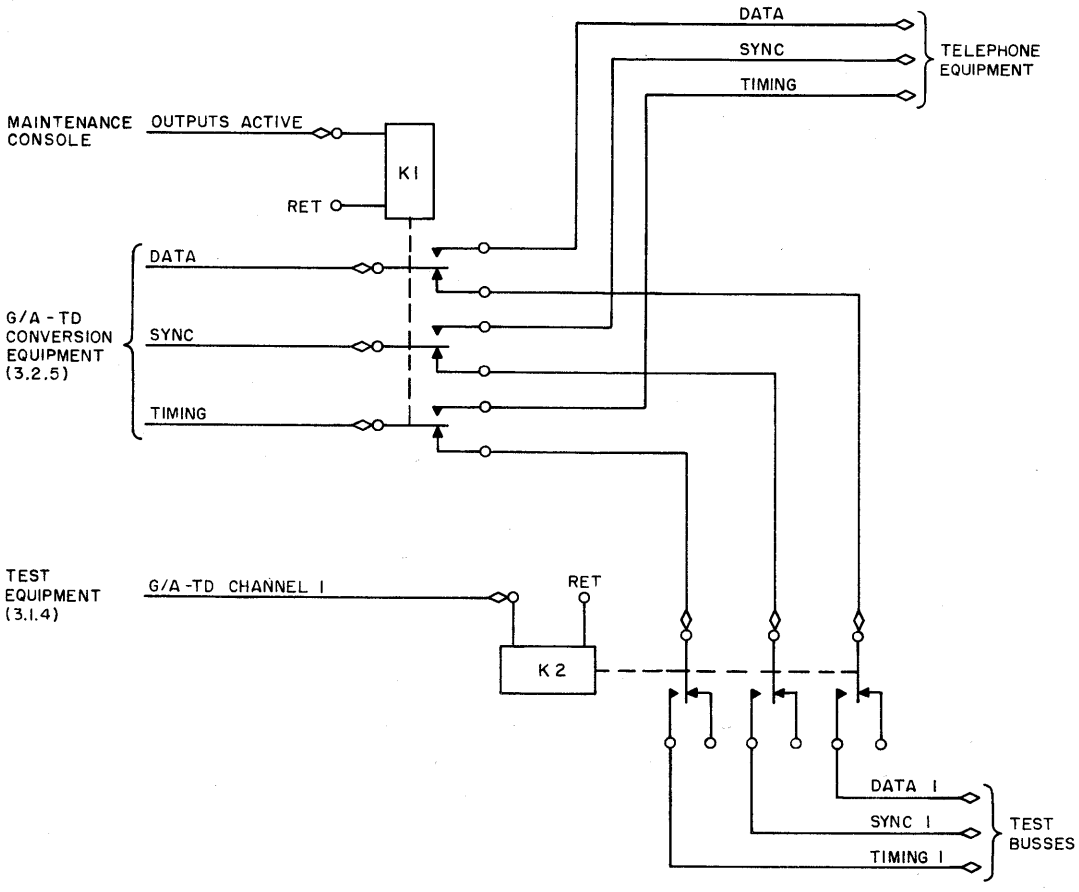


Figure 3–60. G/A-TD Test and Duplex Switching, Message 1 (3.2.5), Simplified Logic Diagram

CHAPTER 5
TELETYPE STORAGE SECTION

5.1 GENERAL

The TTY storage section receives right half-words, their storage parity bits, and busy bits from the output control element. This data is stored temporarily and then transmitted over 25 TTY channels to standard teletypewriters. The teletypewriters are located at anti-aircraft operational centrals, air bases, higher headquarters, and nonautomatic adjacent centrals. The TTY storage section, when transmitting TTY data, simulates a transmitting teletypewriter. Thus the TTY data is transmitted in a form compatible with receiving teletypewriters at the TTY channel termination points.

A standard TTY machine operates at a nominal speed of 60 wpm. This is a normal rate, since the number of words will vary, depending on the number of operations the machine must perform. The standard TTY performs 360 operations per minute. An operation, or character, is defined as one of 26 printing functions or one of six command functions, the whole termed TTY signals.

The TTY machine transmits 360 signals per minute. These signals are sent, one at a time, through a 4-terminal transmission channel, or loop. Figure 3–61 shows the composition of one TTY signal. Each signal consists of seven consecutive intervals. The first and the last of these seven intervals are, respectively, the start and the stop intervals; the remaining five intervals comprise a code identifying the character or command being sent. There are only two possible conditions of the teletype line; that is, mark or space (closed or open, respectively) and therefore the code is a binary code. The 5-bit binary TTY code can be enclosed into 32 possible combinations. Thus, 32 different TTY signals may be sent. The signals sent consist of 26 printing or typing functions and five machine command functions. (See table 1–1 in Ch 2, Part I.) The usual command functions are blank, space, line feed, carriage return, letters or figures. The latter two command functions determine whether the typing functions following will be alphabetical letters or figures and symbols. The printing or typing functions may therefore represent the 26 letters of the alphabet, or 26 decimal numbers and symbols.

The TTY transmission line is normally kept closed; a pulse causes the line to open. Thus, the pulses are inverted with respect to the usual conception of a circuit. The start pulse is always transmitted as a space, opening the TTY line and causing a rotary distributor in the TTY receiver to start rotating. As the arm of the distributor rotates, it crosses each of five contacts in succession, which correspond to the five information bits in the TTY character. Each bit, therefore, is read into the appropriate contact circuit in the receiver. When the stop interval arrives, the distributor arm is in the stop position, and the closed or mark condition which occurs during the stop interval stops the distributor in the start position, ready for the next character. The five information bits that were received energize electromechanical circuits, causing the transmitted character to be typed, or the indicated command to be executed.

The TTY signals, as synthesized by the TTY storage section, are actually transmitted at a rate of 364 signals per minute, or one signal every 15/91 second, closely approximating the standard rate. The seven pulses constituting a signal are transmitted during this interval. The start bit and the five information bits are of equal length, 2/91 second; the stop bit is 1½ times longer, or 3/91 second. (See fig. 3–61.) Thus, each of the first six bits lasts approximately 22 ms, and the stop bit is 33 ms long.

Twenty-five TTY output words may be transmitted simultaneously during a TTY burst period. Each output word is transmitted over a separate TTY channel to its specific destination. A TTY output word contains three TTY signals as shown in figure 3–62. Since a complete TTY message is always longer than these three signals, it follows that several successive TTY burst periods will be required to transmit a single message on each TTY channel.

It should be noted that the RS bit of the right half-word is employed as the start bit of TTY signal A. The

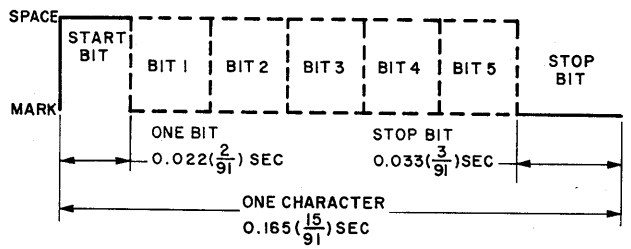


Figure 3–61. Composition of TTY Signals

start bits for signals B and C are made up of BB_2 and BB_1, respectively. Since the start bits must be transmitted as spaces (open line), the RS, BB_2, and BB_1 are 1 bits.

5.2 OPERATION

A simplified diagram of the TTY storage section is shown in figure 3–63. As is shown in this diagram, the TTY storage section is functionally divided into storage, control, readout, burst counting and compare, message-check, and switching circuits. These circuits perform functions similar to the corresponding circuits of the G/A-FD storage section. (Refer to 2.2.)

Operation of the TTY storage section is similar to that of the G/A-FD storage section in that each TTY burst period is divided into search time and readout time. This division is accomplished by the action of the control circuits. These circuits, consisting of the TTY control and the 51 counter, also control the functions of the storage section during each separate interval. The 51 counter, in particular, controls the timing of these functions.

5.2.1 Counter Operation

In order for the 51 counter to perform the timing functions, the counter operates as follows.

The 51 counter is shifted continuously and repeats its counting cycle after it has been shifted 51 times from its start of operations. This counter is generally shifted at a 91-pps rate by timing pulses received from the output control element. During the interval between its second and eighth shifts after the start of each cycle, however, the 51 counter is shifted at high speed; that is, once every 20 μsec, to eliminate the parity bit from the final teletype message. Each time this counter is shifted, a 51-counter-equals pulse is produced.

5.2.2 Search Time

Search time is the interval during which output words are accepted for storage by the storage section.

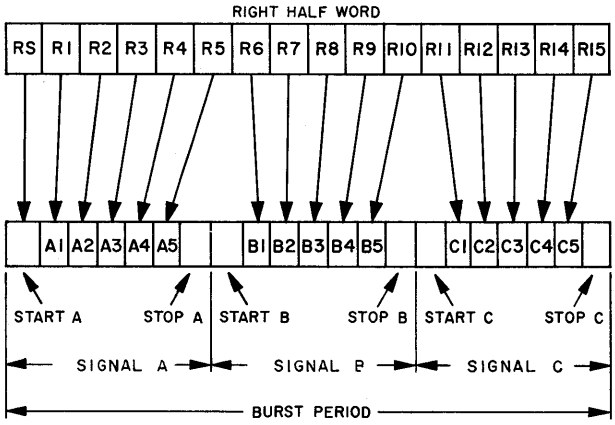


Figure 3–62. Composition of TTY Output Word

The TTY search time starts at the time of the 45th shift of the 51 counter. At this time, the 51-counter-equals-45 pulse which is produced shifts the burst counter and also causes the TTY control to supply a search TTY level to the output control element. This search level indicates that the TTY storage section is ready to receive output words for a new burst. During search time, each correct TTY output word on the OB drum which has a burst number that compares with the present contents of the TTY burst counter is entered in the TTY core storage array.

Search time continues until 51-counter-51 time, a total of six 51-counter shifts or 6/91 second (66 ms). This is sufficient time for the OB fields to be searched. The 51-counter-equals-51 pulse then causes the TTY control to raise the not-search-TTY level, thereby ending search time. The 51 counter now repeats its operational cycle, and with its next shift produces a 51-counter-equals-1 pulse. This pulse starts the interval of the burst period called readout time.

5.2.3 Readout Time

Readout time is the interval between 51-counter-1 time and 51-counter-43 time. During this interval, the output words previously assembled in the core storage array are read out into the OSR. The OSR then transfers these words, bit by bit, through the line register and onto the TTY channels. Readout takes place as explained in the following paragraphs.

The 51-counter-equals-1 pulse, produced when the 51 counter is first shifted at the beginning of its cycle, is sent to the core storage array, where it serves to read out the information contained in one column of cores. This information, consisting of 25 parity bits, is sent through the FA's and loaded into the 25 3-core shift registers which make up the OSR. Each bit is entered in the first core of each of these registers. The next shift of the 51 counter generates a 51-counter-equals-2 pulse. This pulse shifts the 25-shift registers, causing the bits entered in the first core of each register to be shifted to the second core. The 51 counter is now shifted six times at high speed. As a result, 51-counter-equals-3 through 51-counter-equals-8 pulses are generated by these shifts. These pulses alternately read out a column of cores into the OSR and then shift the register. During this high-speed shifting, the parity bits which were present in the OSR at the beginning of the high-speed shifts are shifted out of the OSR and into the line register. This shifting takes place at a speed too high for response of the line register relays, and so the parity bits are lost. This elimination of the parity bits is required because a teletypewriter has no means of checking parity.

At the end of the high-speed shifts, three columns of cores have been read out of the array and loaded into

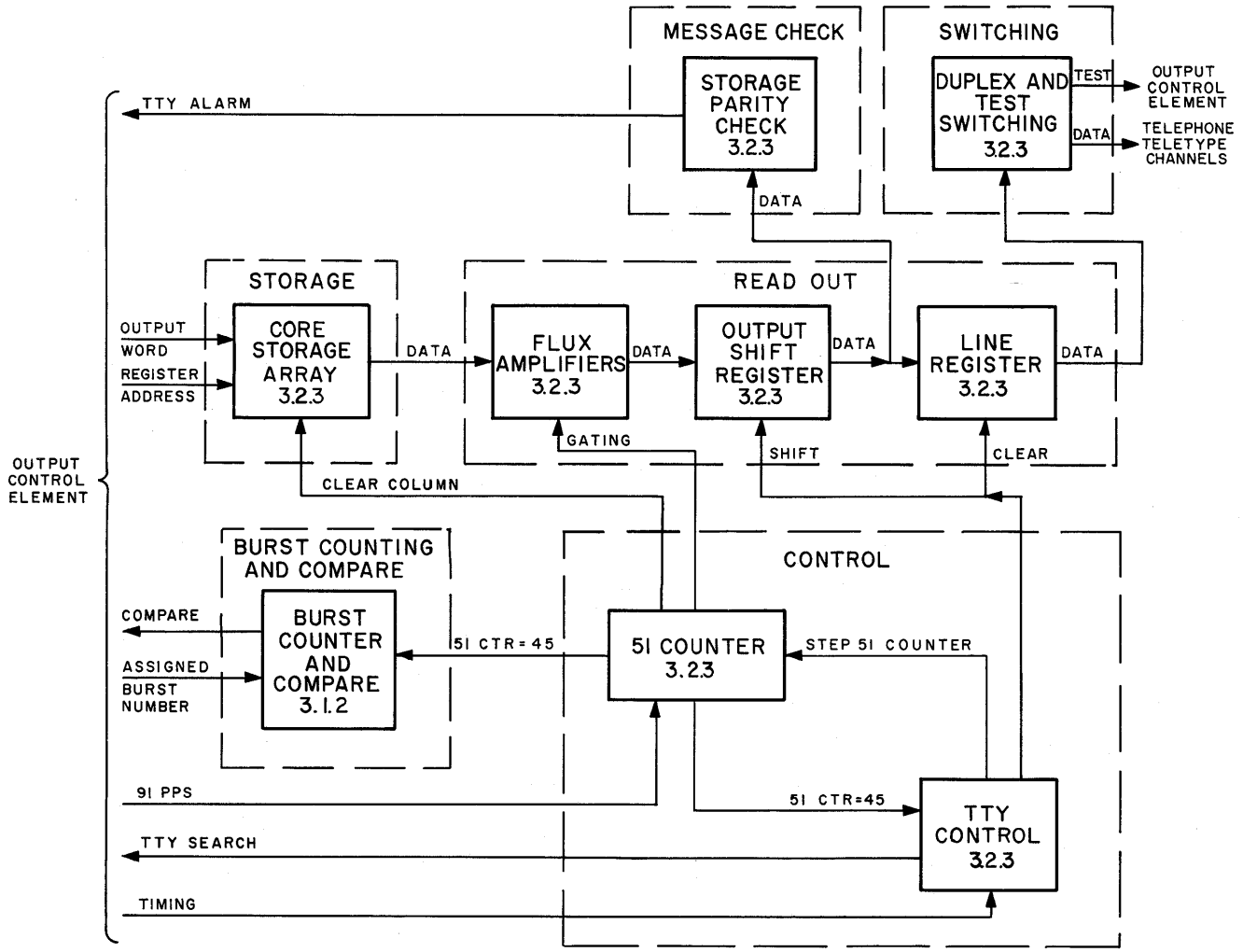


Figure 3–63. TTY Output Storage Section (3.2.3), Simplified Block Diagram

the three cores of the 25 shift registers. The start bit of the first TTY character of each output word is present in the last core of each of the 25 shift registers. The 51 counter is now shifted at a 91-pps rate, and generates pulses which alternately read a column of cores into the OSR and then shifts this register. Each time the OSR is shifted, the bits present in its last cores are applied to the line register. The line register controls 25 relays that hold each of the TTY lines in an open or closed position, depending on whether the corresponding output word bit applied is a space (1) or a mark (0).

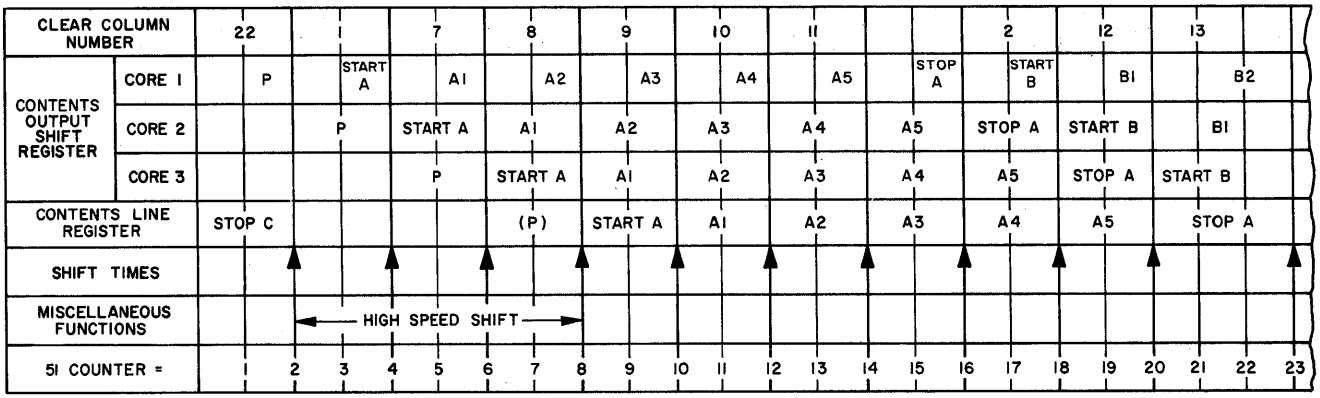
Readout continues as described above until 51-counter-45 time, at which time the core array is empty and search time begins. During each time, an interval of approximately 66 ms, readout from the core array is interrupted. This delay is eliminated from the message transmission by the action of the OSR. At the start of readout, the three cores of each shift register are loaded at high speed with the first three bits of each TTY output word. During search time, these bits continue to be applied to the line register and the TTY lines, thereby eliminating any transmission delay caused by array read-in.

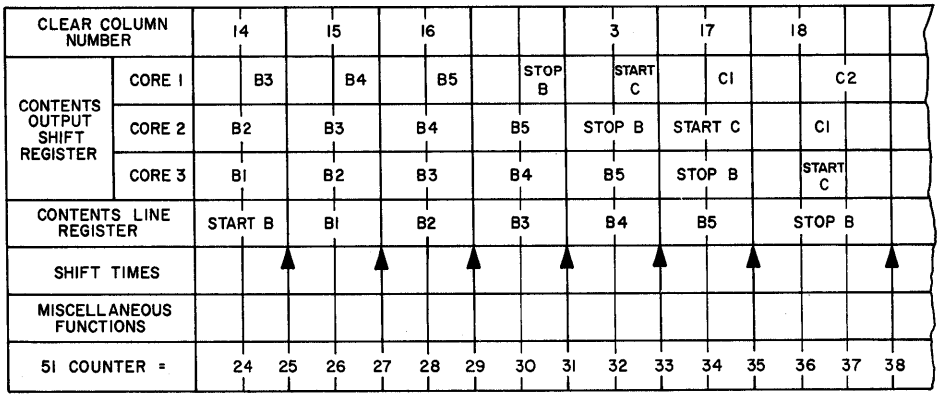
During search time at 51-counter-50 time, the stop bit of the last character of the TTY output word is shifted into the line register. It stays there for the required three timing pulses (3/91 second) until the next shift pulse, which occurs at 51-counter-2 time.

At 51-counter-51 time, the end of search time, the OSR is empty, but the core storage has been refilled. At 51-counter-1 time, the readout process repeats.

During readout the data is examined for errors in transmission. This check is performed by the storage parity checking circuit which receives TTY data as it is shifted out of the OSR. If an error is found, a TTY alarm is transferred to the alarm section in the output control element.

The operation of the TTY storage section is shown in chart form in figure 3–64. This chart shows the column cleared by each 51-counter pulse, and also shows





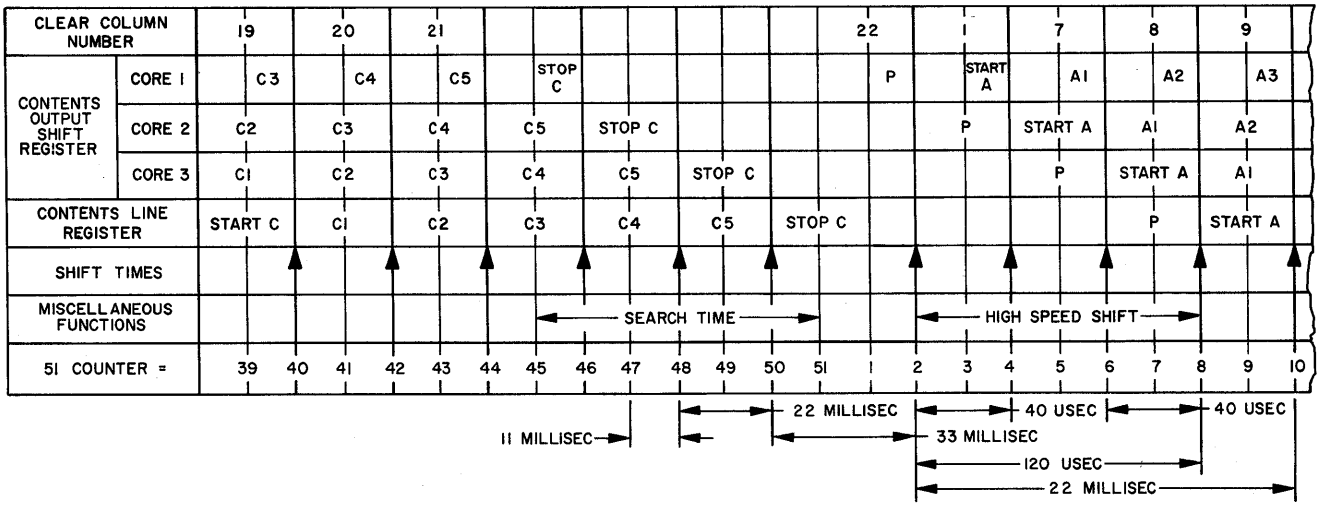


Figure 3–64. Timing of TTY Storage Section Operations

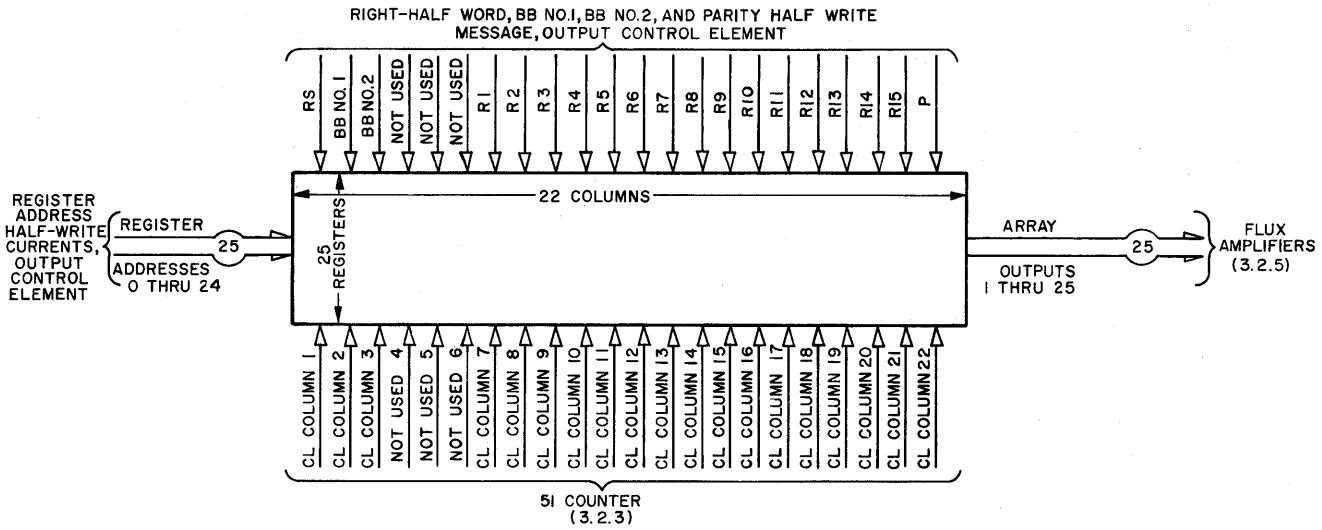


Figure 3–65. TTY Core Storage Array (3.2.3), Simplified Logic Diagram

the position of each bit as it is shifted out of the core array and through the OSR and line register. The shift pulses for the OSR and line register are shown in this chart as shift time pulses.

5.3 STORAGE

5.3.1 General

The TTY storage section has provision for the storage of one 3-character TTY output word in each of 25 registers. Each register receives the information contained in one right half-word, and then supplies information to one TTY channel. The composition of a right half-word and the division of this word into three TTY characters is shown in figure 3–62.

5.3.2 Core Storage Array

The TTY core storage is an array of ferrite cores and is similar in operation to that array described in the G/A-FD section. The array consists of 26 registers; 25 are used for storage, and one is a spare.

Each register contains 22 cores. Of these, only cores 1 to 3 and cores 7 to 22 are used. The cores in the core storage are arranged in registers and columns of bits. (See fig. 3–65.)

5.3.3 Core Array Read-In

The read-in to the TTY core storage array (fig. 3–65) is similar to that of the G/A-FD core storage array. Each of the cores has two half-write windings: a half-write register winding and a half-write message winding. Current through either one of these windings does not produce enough flux to set the core, but current through both windings will set the core. The half-write register winding is in series with windings on each other core in the same register. The half-write message winding is in series with each core in the same column. To write into a core, then, it is necessary to select both the column and the register.

In the read-in operation during a TTY search interval, as each right-half word addressed to the TTY storage section is received, a half-write current pulse passes through the half-write register windings in the register selected for read-in. At the same time, the contents of the right half-word, parity bit, and busy bits are applied to the half-write message windings in columns 1, 2, 3, and 7 through 22. Thus, data is written into the selected register. Columns 4, 5, and 6 are not used.

5.4 CONTROL

5.4.1 General

The action of the TTY storage section is controlled by the 51 counter and the TTY control. These circuits generate and gate the timing signals necessary to accomplish the various operations of the TTY storage section.

5.4.2 51 Counter

The 51 counter, shown in figure 3–66, is a tape core counter similar to the 25 counter in the G/A-FD storage section, but with 51 cores. At the beginning of

each counting cycle, the counter is cleared. Immediately thereafter, a 1 is primed into the first core and then continuous stepping of the counter at a 91-pps rate begins. The outputs of the 51 counter are labeled with respect to the core from which they originated. Generally, the output of every other core in the 51 counter is used to shift the contents of successive columns from the core storage through the FA's into the OSR. The other alternate outputs of the 51 counter are used both to shift the OSR and to clear the line register. Table 3–2 shows the destination and function of each 51-counter output pulse.

It will be noticed from table 3–2 that the 51-counter-equals-15, -30, and -45 pulses do not perform any control functions. These pulses are used to produce the stop bits, one of which is required to complete each TTY character. (See fig. 3–62.) Since the stop bits are all 0 bits, they are not stored in the array and therefore must be generated by the TTY storage section. Either a 51-counter-equals-15, -30, or -45 pulse is generated after six clear-column pulses have been produced. Clear-column pulses shift the first six bits of each TTY character from the core array. The 51-counter-equals-15, -30, and -45 pulses therefore occur at the time that the seventh bit should be shifted from the array and entered in the OSR. Since these pulses are not used to clear a column, the first cores of the OSR retain a 0 bit, and this bit always completes TTY character.

The shift time pulses listed in table 3–2 go to the shift-pulse generator circuit of the 51 counter, where they are collected in an OR circuit and transferred to

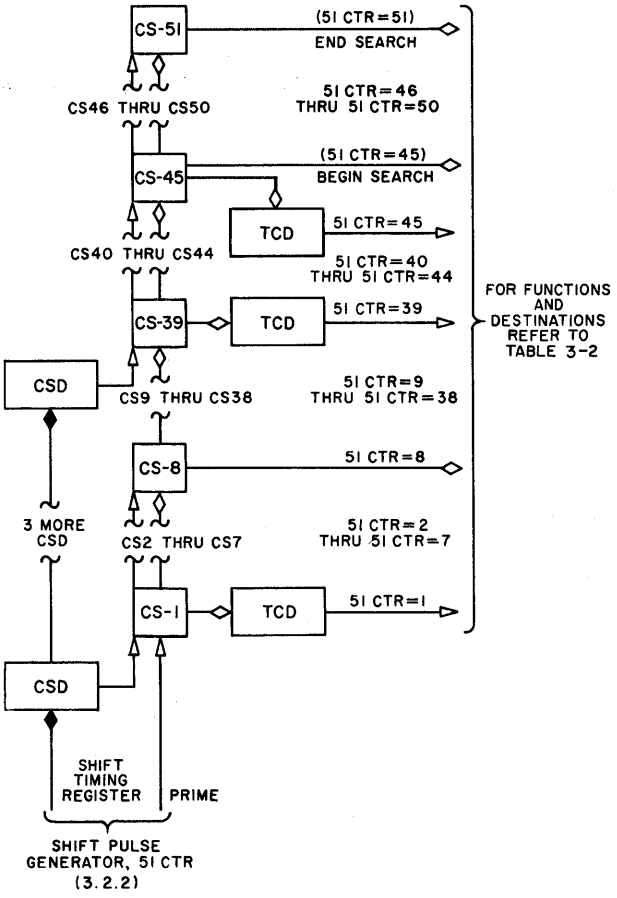


Figure 3–66. 51 Counter (3.2.3), Simplified Logic Diagram

TABLE 3–2. DESTINATION AND FUNCTION OF 51-COUNTER PULSES

51 COUNTER	DESTINATION	FUNCTION
1	Teletype core storage	Clear column 22
2	Shift-pulse generator, 51 counter	Shift time
2	Shift-pulse generator, 51 counter	Start high-speed shift
3	Teletype core storage	Clear column 1
4	Shift-pulse generator, 51 counter	Shift time
5	Teletype core storage	Clear column 7
6	Shift-pulse generator, 51 counter	Shift time
7	Teletype core storage	Clear column 8
8	Shift-pulse generator, 51 counter	Shift time
8	Shift-pulse generator, 51 counter	Stop high-speed shift
9	Teletype core storage	Clear column 9
10	Shift-pulse generator, 51 counter	Shift time
11	Teletype core storage	Clear column 10

TABLE 3–2. DESTINATION AND FUNCTION OF 51-COUNTER PULSES (cont'd)

51 COUNTER	DESTINATION	FUNCTION
12	Shift-pulse generator, 51 counter	Shift time
13	Teletype core storage	Clear column 11
14	Shift-pulse generator, 51 counter	Shift time
15	Not used	Stop bit
16	Shift-pulse generator, 51 counter	Shift time
17	Teletype core storage	Clear column 2
18	Shift-pulse generator, 51 counter	Shift time
19	Teletype core storage	Clear column 12
20	Shift-pulse generator, 51 counter	Shift time
21	Teletype core storage	Clear column 13
22	Not used	
23	Shift-pulse generator, 51 counter	Shift time
24	Teletype core storage	Clear column 14
25	Shift-pulse generator, 51 counter	Shift time
26	Teletype core storage	Clear column 15
27	Shift-pulse generator, 51 counter	Shift time
28	Teletype core storage	Clear column 16
29	Shift-pulse generator, 51 counter	Shift time
30	Not used	Stop bit
31	Shift-pulse generator, 51 counter	Shift time
32	Teletype core storage	Clear column 3
33	Shift-pulse generator, 51 counter	Shift time
34	Teletype core storage	Clear column 17
35	Shift-pulse generator, 51 counter	Shift time
36	Teletype core storage	Clear column 18
37	Not used	
38	Shift-pulse generator, 51 counter	Shift time
39	Teletype core storage	Clear column 19
40	Shift-pulse generator, 51 counter	Shift time
41	Teletype core storage	Clear column 20
42	Shift-pulse generator, 51 counter	Shift time
43	Teletype core storage	Clear column 21
44	Shift-pulse generator, 51 counter	Shift time
45	Shift-pulse generator, 51 counter	Begin search
46	Shift-pulse generator, 51 counter	Shift time

TABLE 3–2. DESTINATION AND FUNCTION OF 51-COUNTER PULSES (cont'd)

51 COUNTER	DESTINATION	FUNCTION
47	Not used	
48	Shift-pulse generator, 51 counter	Shift time
49	Not used	
50	Shift-pulse generator, 51 counter	Shift time
51	Shift-pulse generator, 51 counter	End search
51	Shift-pulse generator, 51 counter	Prime 51 counter

the TTY control. (See fig. 3–67.) The output pulses of the 51 counter are comparatively long sawtooth-shaped pulses. These pulses are not acceptable for certain applications in this form and are therefore gated (at OD 3 time) in the shift-pulse generator of the 51 counter to provide standard 0.1-μsec pulses.

The 51-counter shift pulses and the TTY-FA-GT pulses used to gate the FA's are 2.5 μsec in length, occurring between OD 2 and OD 3. These pulses are generated by the flip-flop in the 51-counter shift-pulse generator (fig. 3–45). The flip-flop is normally set at OD 2–91 time and is cleared at the following OD 3

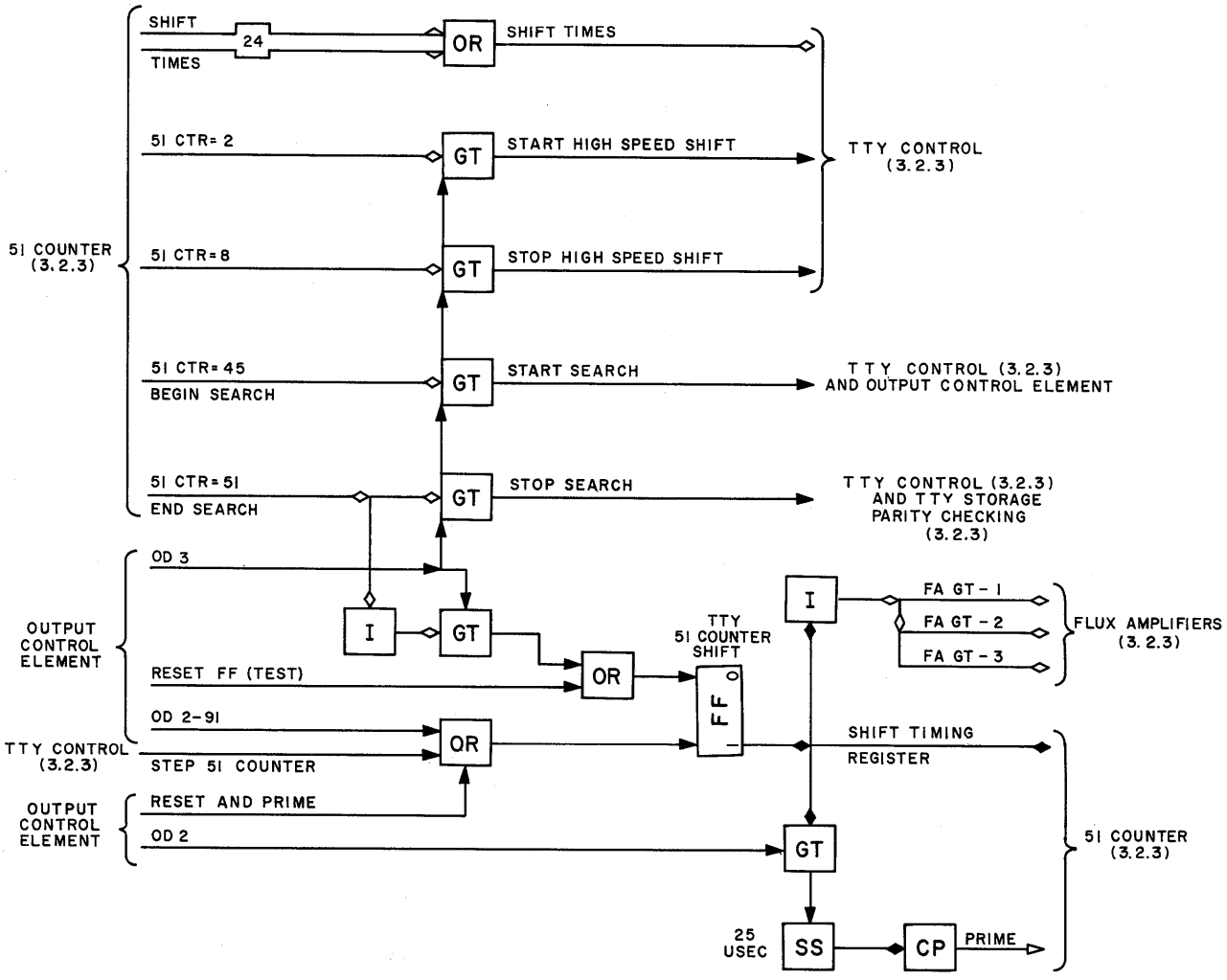


Figure 3–67. Shift-Pulse Generator, 51 Counter (3.2.3), Simplified Logic Diagram

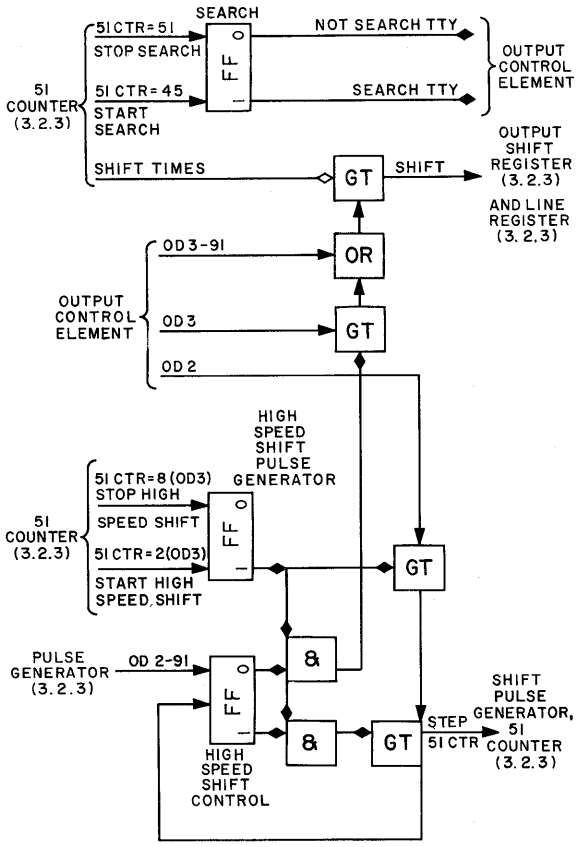


Figure 3–68. TTY Control (3.2.3), Simplified Logic Diagram

time, unless the 51-counter-equals-51 pulse causes the OD 3 pulse to be inhibited. In this case, the shift pulse lasts an extra OD cycle (10 μsec), causing the 51 counter to be cleared and causing a 1 to be primed into the first core of the 51 counter.

5.4.3 Teletype Control

The TTY control, shown in figure 3–68, regulates the supply of shift pulses to the 51 counter and gates all shift pulses to the OSR and line register. Another function of the TTY control is sending search and not-search control levels to the read-in control of the output control element to co-ordinate the read-in cycle with the readout cycle.

The search TTY and not-search TTY levels are developed by the 1 and 0 sides, respectively, of the search flip-flop. This flip-flop is set by a 51-counter-equals-45 pulse, thereby developing the search TTY level, and reset by a 51-counter-equals-51 pulse, thereby developing the not-search TTY level. These levels start and terminate TTY search time.

The TTY control sends OD 3–91 pulses to the OSR and line register as shift pulses only when the shift-time level is up. This level is raised at the 51-counter times specified in table 3–2.

The TTY control also controls the high-speed shifting of the 51-counter, OSR and the line register. This is accomplished as explained below. (See fig. 3–69).

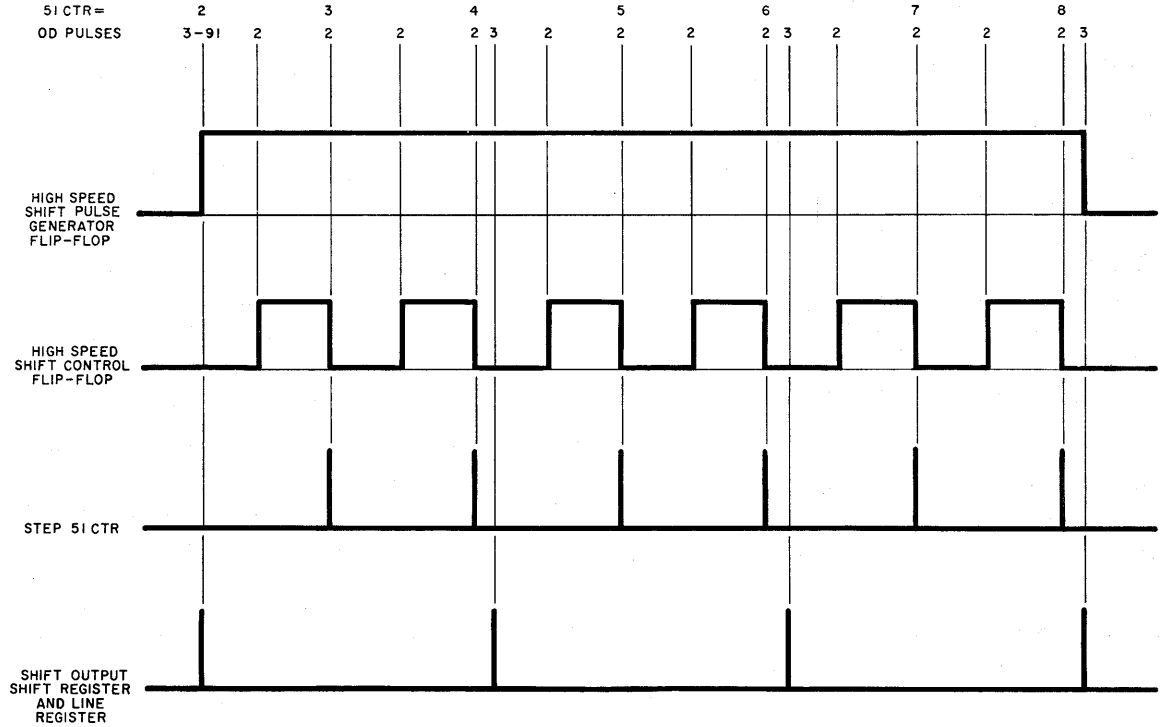


Figure 3–69. High-Speed Shift Timing

The 51-counter-equals-2 (start high-speed shift) and the 51-counter-equals-8 (stop high-speed shift) gated pulses respectively set and clear the high-speed shift pulse generator flip-flop. When this flip-flop is set, OD 2 pulses are enabled to complement the high-speed shift control flip-flop. This latter flip-flop is always reset by an OD 2–91 pulse before the first complementing OD 2 pulse is applied. The first complementing pulse applied, therefore, sets the high-speed shift control flip-flop. The 1 side of this flip-flop conditions a gate which is pulsed by OD 2 pulses. The next OD 2 pulse is passed by this gate as a step-51-counter pulse, and this pulse shifts the 51 counter to 51-counter-equals-3. The same OD 2 pulse simultaneously resets the high-speed shift control flip-flop. The 0 side of this flip-flop now conditions a gate which is pulsed by OD 3 pulses, and the next OD 3 pulse is passed by this gate and applied to a gate which is conditioned by the shift times level. This level is up at the 51-counter times specified in table 3–2. During the high-speed shifting, the shift times level is up at 51-counter-4, -6, and -8 time only. Since the 51 counter is now at 51-counter-equals-3, the OD 3 pulse is not passed.

The complementing of the high-speed shift control flip-flop, with the subsequent shifting of the 51 counter, continues at a 50-kilocycle rate until 51-counter-8 time. During this time, an OD 3 pulse is sent as a shift pulse to the OSR and line register at the times when the high-speed shift control flip-flop is reset during 51-counter-4, -6, and -8 time. At these times the shift times level is up. At 51-counter-8 time, the high-speed shift-pulse generator is reset by the 51-counter-equals-8 pulse, and the high-speed shifting is thus terminated.

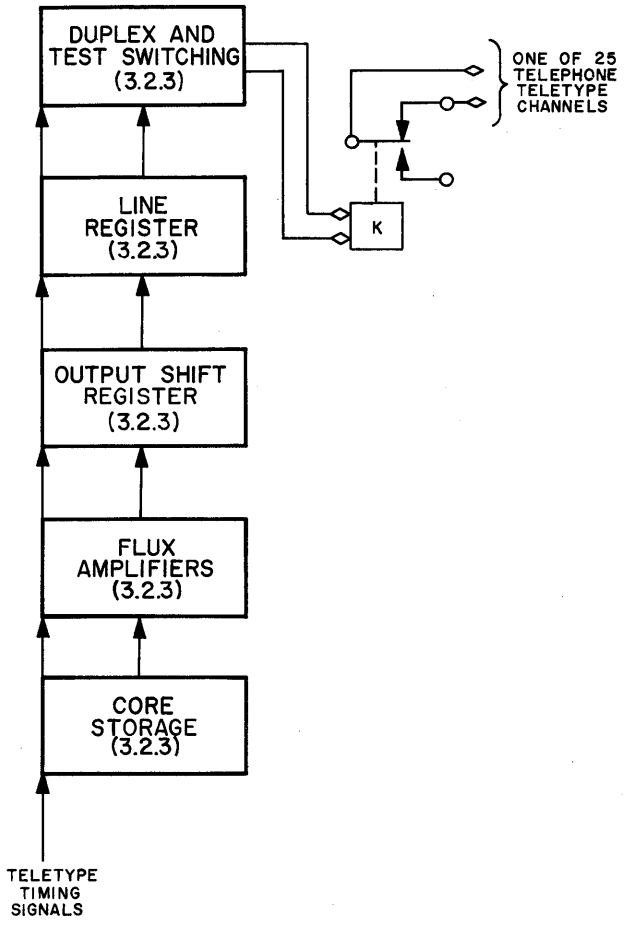


Figure 3–70. TTY Readout Flow of Data, Block Diagram

5.5 TELETYPE READOUT

5.5.1 General

Readout of the TTY storage section must be performed to meet the standard TTY machine requirements. The readout operation is controlled by timing signals generated in the 51 counter and the TTY controls. Figure 3–70 shows the logical flow of data during readout. There are five identical readout channels, only one of which will be described in this discussion. Bits are read out from each array register serially, through FA's and into a 3-core OSR. From the OSR, the bits enter a line register (a flip-flop) which controls a relay that holds the line in an open or closed position, depending upon whether the bit is a space (1) or a mark (0).

5.5.2 Core Array Readout

Each TTY output word is read out of the TTY core storage array by columns. There are 22 columns in the core array, of which 19 are active and 3 are spares. (See fig. 3–71.) The 19 active columns are pulsed by clear-column pulses, applied by the TCD's located in the 51-core shift register. Each time a column is pulsed, the bits stored in its cores are shifted from the core array in parallel to the FA's. The bits from each column are composed of one bit from each of the 25 output words that are stored in the array. Table 3–3 shows the assignment of bits by columns, the 51-counter pulse that clears each column, the order of readout, and the significance of each bit in the core storage.

5.5.3 Flux Amplifiers (FA's)

Each of the 25 array output pulses from the TTY core storage array is applied to an FA. A 1 bit is represented by pulse and a 0 bit is indicated by the absence of a pulse. Separate groups of the 25 FA's are gated as shown in figure 3–71 by gating levels 1, 2, and 3. These gating levels are 2.5-μsec negative pulses employed to prevent noise and spurious signals from passing through the FA's. They are produced in the 51-counter shift-pulse generator simultaneously with each shift of the 51 counter. (Refer to 5.4.2.) Since alternate 51-counter shifts generate clear-column pulses which read

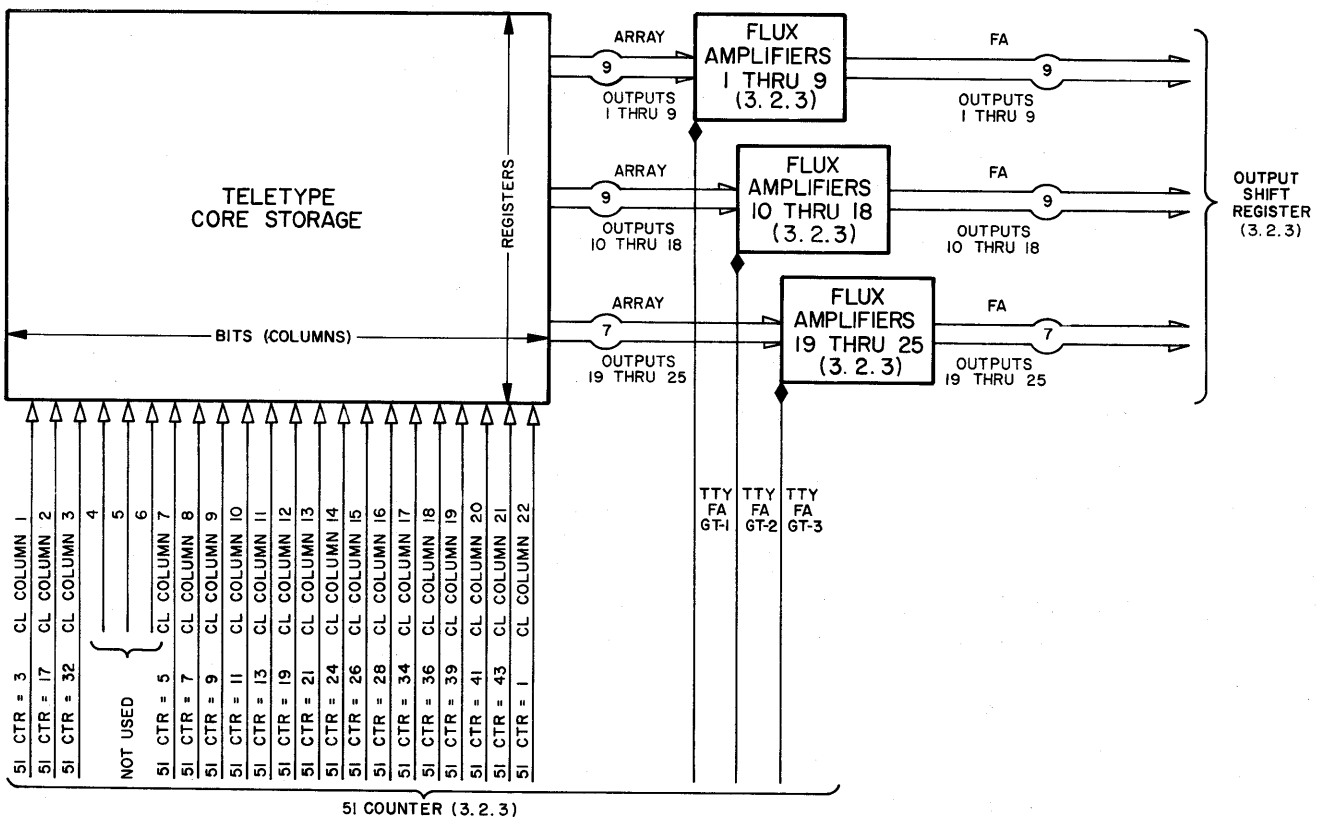


Figure 3–71. TTY Core Storage Readout, Simplified Block Diagram

TABLE 3–3. ASSIGNMENT OF BITS IN TTY CORE STORAGE

BIT	CORE STORAGE COLUMN	READOUT AT 51 COUNTER	ORDER OF READOUT OF COLUMNS	TELETYPE BIT
RS	1	3	2nd	Start A
BB 1	2	17	8th	Start B
BB 2	3	32	14th	Start C
R1	7	5	3rd	A-1
R2	8	7	4th	A-2
R3	9	9	5th	A-3
R4	10	11	6th	A-4
R5	11	13	7th	A-5
R6	12	19	9th	B-1
R7	13	21	10th	B-2
R8	14	24	11th	B-3
R9	15	26	12th	B-4
R10	16	28	13th	B-5
R11	17	34	15th	C-1

TABLE 3–3. ASSIGNMENT OF BITS IN TTY CORE STORAGE (cont'd)

BIT	CORE STORAGE COLUMN	READOUT AT 51 COUNTER	ORDER OF READOUT OF COLUMNS	TELETYPE BIT
R12	18	36	16th	C-2
R13	19	39	17th	C-3
R14	20	41	18th	C-4
R15	21	43	19th	C-5
P	22	1	1st	P

out columns of the core array, the array outputs are applied to the FA's during the 2.5 μsec that the FA's are gated and operative. The FA's, after amplifying and stretching the array output pulses, send the pulses to the OSR as FA outputs. The outputs from the FA's are sent over 25 lines labeled FA output 1 through FA output 25, respectively.

5.5.4 Output Shift Register

The purpose of the OSR (fig. 3–72) is to provide a 3-shift buffer so that there is no delay or pause on the TTY channel during TTY search time.

The OSR is made up of 25 3-core shift registers. One shift register is provided for each of the 25 TTY channels used. Each CSR is a tape core register identical to those used in the G/A-FD OSR. The information bits, as they are shifted out of the core storage array and amplified in the FA's, are read into the first core of each register. After receipt of each group of bits, and prior to receipt of the next group, the CSR's are shifted. In this manner, the bits from a register in the core array are shifted serially through each 3-core shift register to a line flip-flop in the line register.

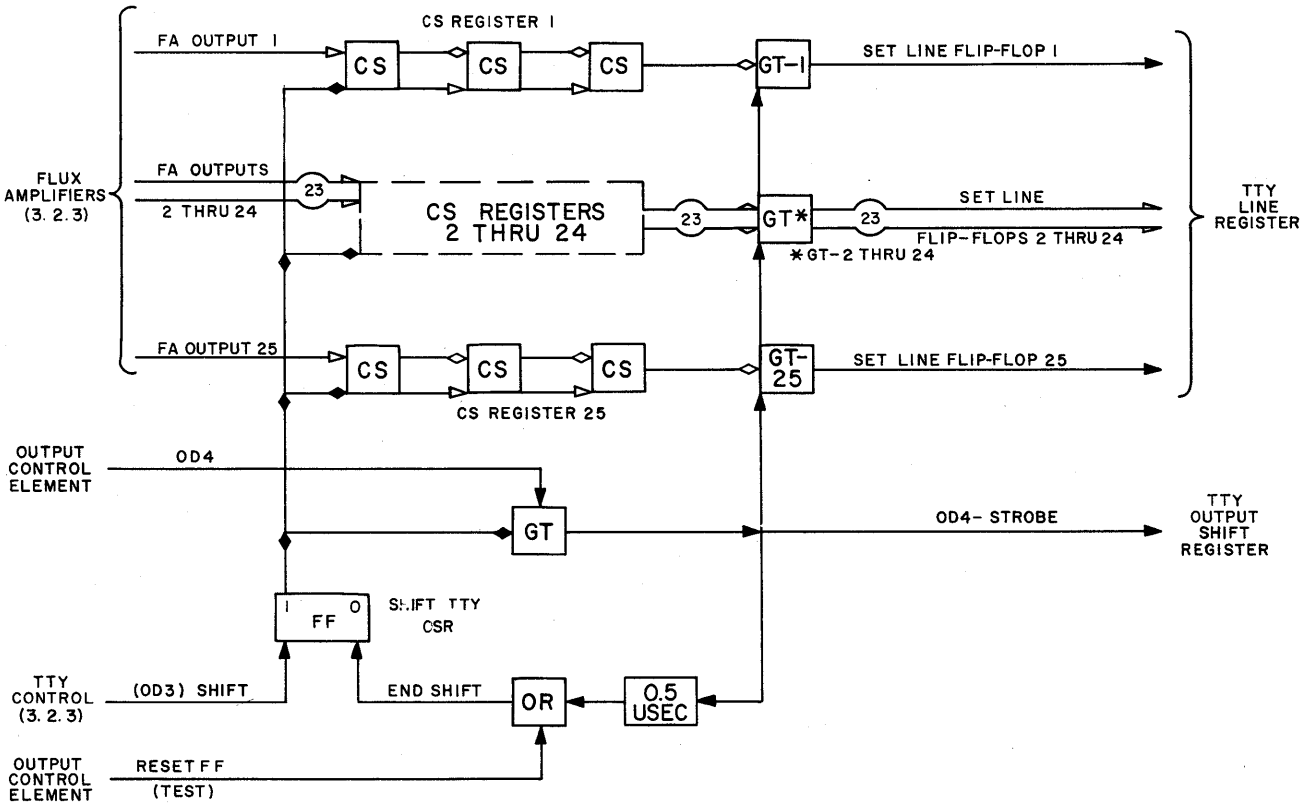


Figure 3–72. TTY Output Shift Register (3.2.3), Simplified Logic Diagram

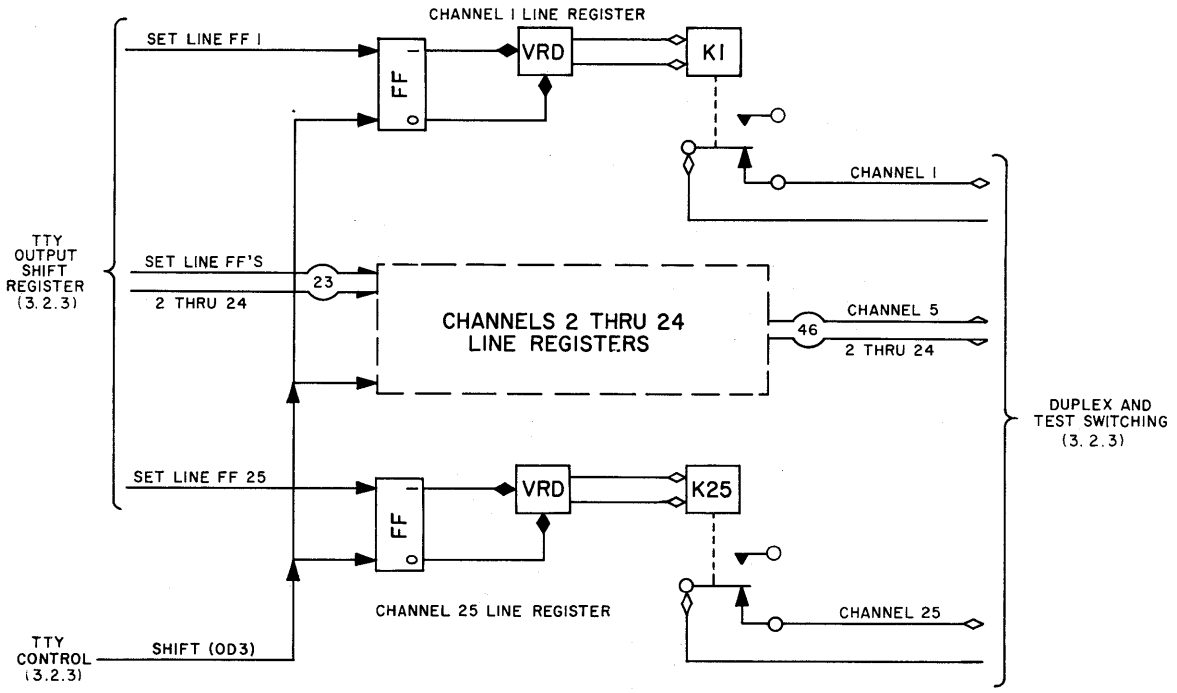


Figure 3–73. Line Register (3.2.3), Simplified Logic Diagram

Output shift register shift pulses are produced by the flip-flop shown in figure 3–72. This flip-flop is set upon receipt of an OD 3 shift pulse from the TTY control. The level developed by the 1 side of this flip-flop is simultaneously applied to the shift registers as a shift signal and as a conditioning level to a gate. After 2.5 μsec, an OD 4 pulse passes the gate and clears the flip-flop. Thus, the level applied to the registers and gate falls. In this manner, a 2.5-μsec shift pulse is developed for each OD 3 shift pulse received from the TTY control. The OD 3 shift pulses are applied when a shift times level is developed at the times specified in table 3–2.

Each bit shifted from the last core of a register is applied as a conditioning level to a gate. This gate is pulsed by each OD 4 pulse which clears the flip-flop. If the bit shifted out of the register is a 1, the gate is conditioned and the OD 4 clear pulse is sent to a line flip-flop in the line register.

5.5.5 Line Register

Figure 3–73 shows the 25-line registers and their associated relay circuits. The line flip-flops are set by each 1 bit that is read out of the OSR, just after the shift. The flip-flops are then cleared by the shift pulse which shifts the next bit out of the OSR.

The relay follows the action of the line register. When the flip-flop is in the 1 state, the relay opens the TTY channel. Thus, a 1 bit causes an open line or space.

5.6 MESSAGE CHECK

The function of the storage parity checking circuit, shown in figure 3–74, is to transmit a TTY parity alarm

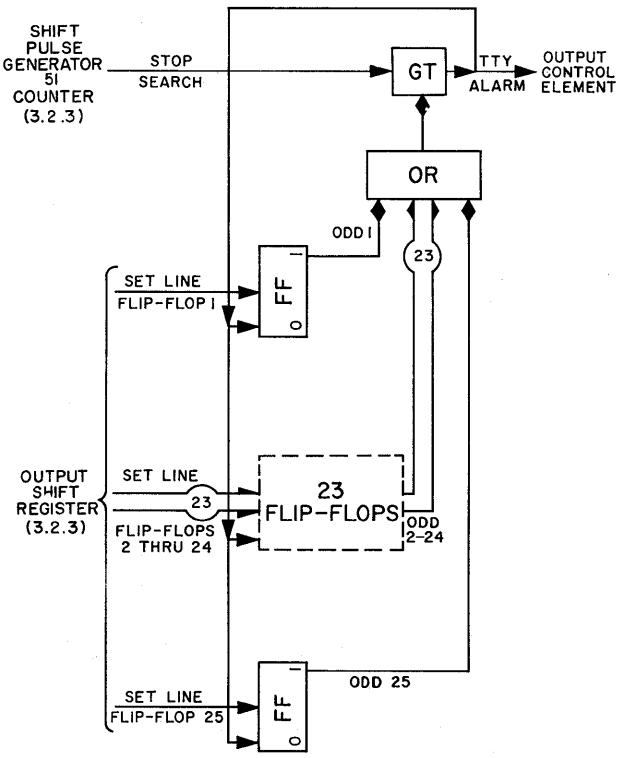


Figure 3–74. TTY Storage Parity Checking (3.2.3), Simplified Logic Diagram

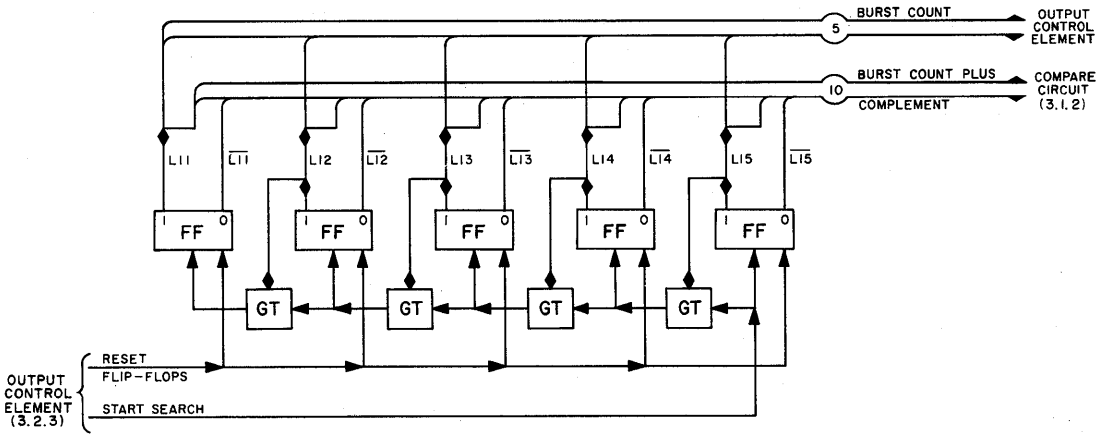


Figure 3–75. TTY Burst Counter (3.1.2), Simplified Logic Diagram

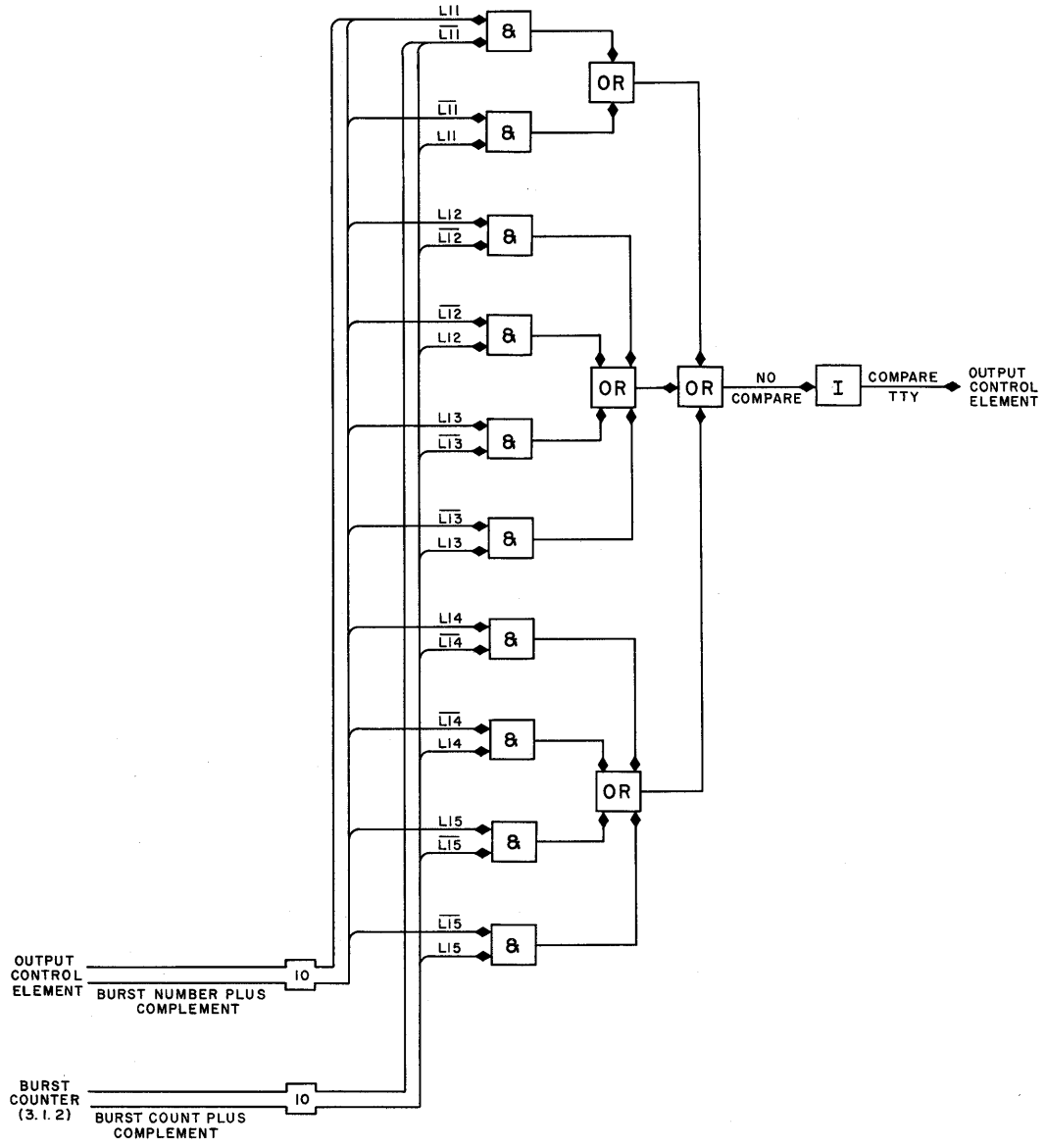


Figure 3–76. Comparison Circuit, Teletype Burst Counter (3.1.2), Simplified Logic Diagram

signal to the alarm control in the case of a storage parity alarm. This circuit is similar to the G/A-FD storage parity checking circuit.

If any of the parity check flip-flops is set at 51-counter-51 time, the gate which is conditioned by the 1 side of these flip-flops will pass the stop-search pulse applied to it at this time. This pulse will clear the set flip-flops. Readout now starts, and as bits are shifted out of the OSR's and into the line flip-flops, they are also transmitted to the parity storage checking circuit where they complement the parity check flip-flops. Since the total number of 1's in the TTY message, including the parity bit, is even, all flip-flops should be in the 0 state at the following stop search time. The 1 sides of the flip-flops are sampled, and if any flip-flops are found to be in the 1 state, the TTY alarm is transmitted. This alarm also clears the set flip-flops in preparation for the next parity check.

5.7 BURST SEQUENCE AND TIMING

The TTY burst count and comparison are accomplished within the TTY burst counter and compare circuits. The TTY burst sequence and timing are identical to the burst sequence and timing operation of the G/A storage section, except for the number of bits used. The TTY burst count and compare circuits use a 5-bit burst number; the TTY burst counter is composed of five flip-flops. This is a standard flip-flop counter, having a scale of 32. The burst counter is stepped at start search (51-counter-45 time). Figures 3–75 and 3–76 are simplified logical block diagrams of the TTY burst counter and the comparison circuits, respectively.

5.8 SWITCHING

The TTY test and duplex switching circuits control the TTY output of the Output System of each computer. The switching circuits contain relays which provide for the switching of each of the 25 TTY messages. However, the relay circuits for each message are identical. For this reason, figure 4–13 shows a simplified diagram of the TTY test and duplex switching circuits for only one TTY message.

The relays provided by the TTY test and duplex switching circuits are controlled so that only the Output System of the active computer is presented to the telephone line terminal equipment. Relays are also provided to enable the Output System on standby status to be switched to the TTY test buses. These relays are operated during test operations only.

PART 4
TEST EQUIPMENT SECTION

The output test equipment section is incorporated in the output control element of the Output System for the purpose of testing circuit functioning and the logical operation of the Output System. The test equipment consists of switches, relays, and logical circuits. Also, certain of the neons and indicator lamps of the output alarm section operate with the output test equipment section. The various switches, neons, and lamps are located on the Output System test panel, which is mounted on the back of unit 42. (See fig. 4–1.)

Two basic types of tests are provided by the test equipment: the unit loop test and the computer loop test. Each loop test involves the feedback of test information to its origin, where a comparison is made to ascertain whether the test information was correctly transmitted. The unit loop test is performed manually by means of switches, whereas the computer loop test is programmed and is therefore performed automatically. The unit loop test checks the operation of the various individual sections of the Output System while the system is isolated from the remainder of the Combat Direction Central. The computer loop test provides a means of checking the Output System in conjunction with a large portion of the Combat Direction Central.

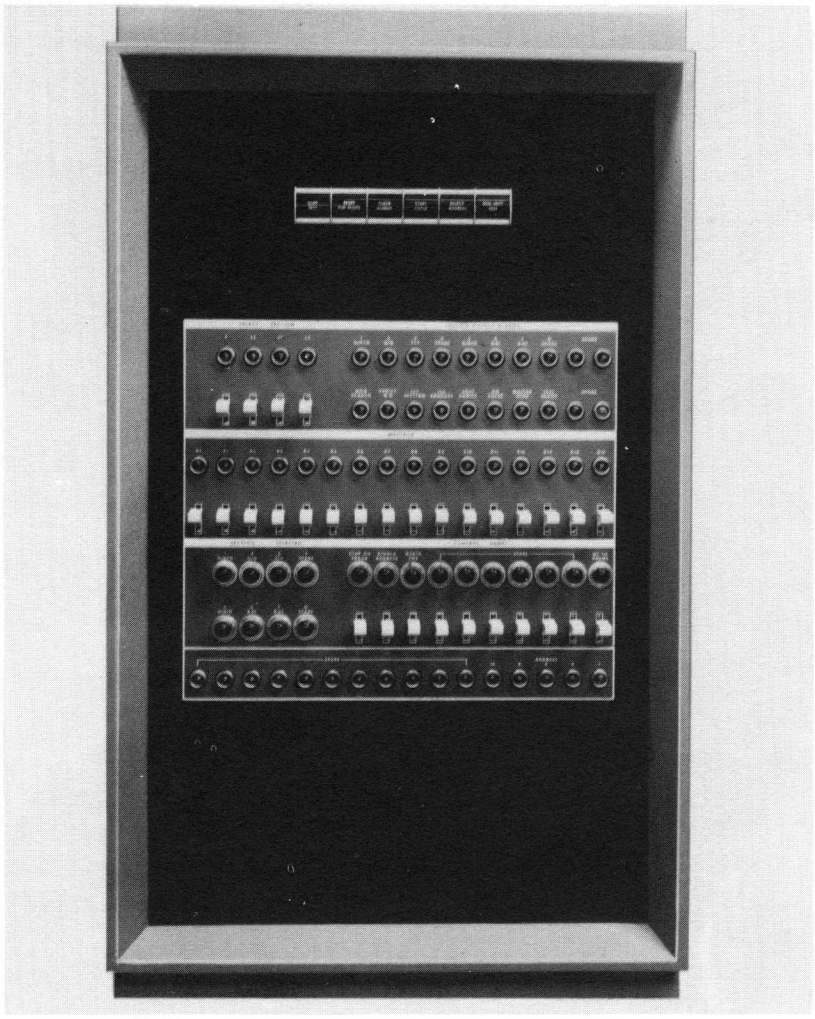


Figure 4–1. Test Control Panel, Unit 42

CHAPTER 1
UNIT LOOP TEST

1.1 GENERAL

In the unit loop test, the Output System is isolated from the Drum System, and a test word is then inserted manually by means of switches. The test word is processed in the normal manner by the output control element. If the conditions for its acceptance have been fulfilled (parity OK, burst number compares, no illegal addresses, and search time up), the word is transferred in the normal manner to the selected storage section in the output storage element. The word is then processed through this element. For the G/A-FD, BO1, BO2, G/G, and G/A-TD storage sections, the output data (right drum word) is looped back into the output control element flip-flop register where the word was originally entered. If the transfer of the word was successful, the flip-flop register will be cleared. If the transfer was unsuccessful, one or more of the output flip-flop register neons will be illuminated. (See fig. 4–2.)

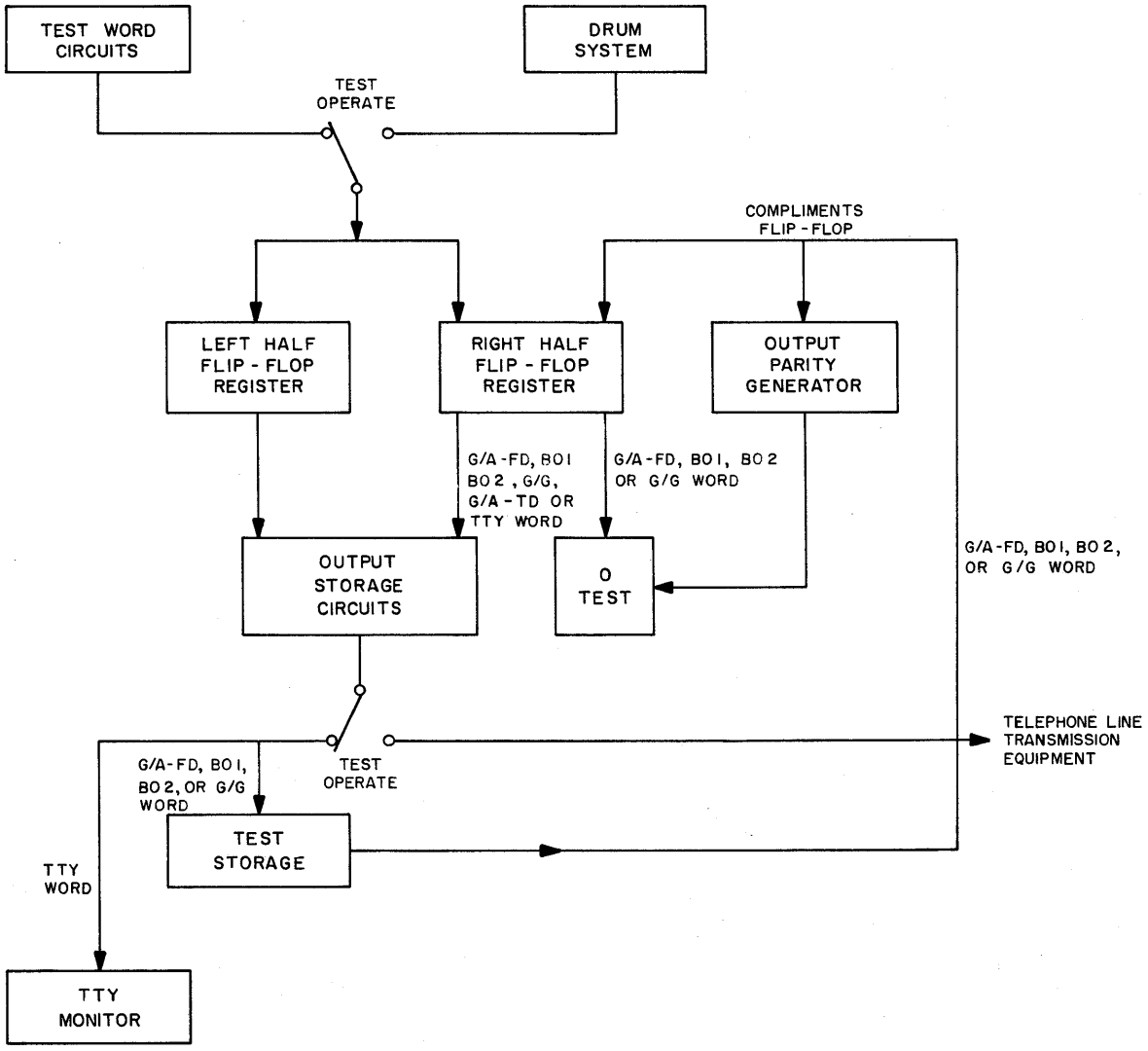


Figure 4–2. Unit Loop Test Data Flow, Block Diagram

Besides this visual representation, the test equipment section indicates an error in one of several other ways described in 1.2.13.

For the TTY storage section, the output word is recorded on a TTY monitor. This data is then visually compared with the test contents of the flip-flop register to determine whether an error has occurred.

The unit loop test procedure may be divided into three basic circuit groupings: unit loop control, unit loop storage, and specific unit loop tests. The unit loop control circuits control the general flow of the test word through the output control element and output storage element and provide the processing operations for detecting an error. The unit loop storage circuits provide for the storage of the test word in the test equipment section. The unit loop test circuits control the specific test operations in each of the storage sections of the output storage element during testing operations.

1.2 UNIT LOOP CONTROL, ERROR DETECTION

The general process of error detection involves the manual setting in of a test word in the flip-flop registers and the processing of this word to determine whether any errors occur. The test word is processed through the output control element in the normal manner and transferred to the output storage section. It is processed by the particular output storage section as described in 1.4. From there, a G/A-FD, BO1, BO2, G/G, or G/A-TD word goes to the unit loop control circuits. A TTY word, on the other hand, is sent not to the unit loop control circuits but to a TTY monitor.

1.2.1 Unit Loop Test Switching

The operation of the Output System during testing is controlled by relays, which in turn are controlled by switches. These switches are located on the panel on the test door on the back of the output control unit.

Any kind of a test on the Output System disables it, thereby disabling the operation of an entire central. Therefore, an interlock (controlled at the maintenance console) is necessary to prevent inadvertently starting a test during the processing of an air defense problem. This interlock is accomplished by switching the relay voltage supply for the test equipment section at the maintenance console. Thus, the OPERATE-TEST switch on the maintenance console sends a computer test signal to the unit-loop-on-test circuit of the unit loop control. (See fig. 4–3.) This signal controls the relay voltage supply for the output test equipment section and is sent via the computer loop control circuits since a computer loop test takes precedence over a unit loop test. Hence, control over whether a unit loop test can take place depends upon whether a computer loop test is in progress.

A UNIT TEST pushbutton (S6, fig. 4–3) in the test equipment section causes a holding relay to close, which controls the output test relay voltage (the output-on-test signal) to the test circuits. The END UNIT TEST pushbutton (S1) breaks the voltage to the holding relay at the end of the test operation.

1.2.2 Drum Isolation and Test, Bit Circuits

To set in a test word, the flip-flop register of the output control element must be isolated from the Drum System. After this is done, the test word can be set into the flip-flop register.

Eight relays, controlled by the —48V unit loop test relay voltage, are used to isolate the OB (output buffer) register from the Drum System. Five of these relays, as shown in figure 4–4, isolate 20 of the 33 bit lines from the Drum System. The remaining 13 bit lines and the associated isolation relays are not shown because they have no corresponding bit switches. The reason for this is explained in the following paragraphs.

The test word generator of the output test equipment section provides a standard test word pulse equivalent to a 1 bit to each of 20 gates. Each gate is connected to a read-in test word switch corresponding to 20 of 33 bits which make up a word. The bit switches used in a unit loop test are the P bit, LS through L2, and RS through R15.

When a switch is closed, a +10V level conditions the corresponding gate which passes the test-word pulse. This sets the corresponding flip-flop in the flip-flop register. It follows, of course, that read-in test switches which are not activated will have no effect on their respective flip-flops; thus the latter will remain cleared (0 side up).

When setting in a test word for G/A-FD, BO1, BO2, G/G, or G/A-TD, the right drum word (bits RS through R15) may be set to any desired combination of 1's and 0's. For TTY, the restrictions explained in 1.4.4 must be considered. The burst number, bits L8 through L15, must be all 0's since the stepping pulses to the burst counters in the output control element are inhibited. Since bits L8 through L15 must always be 0's, their corresponding bit switches have been removed from the unit test door. The desired register address in the array of the selected section, designated bits L3 through L7, does not require the use of bit switches during a unit loop test because the register address portion of the OB register is automatically stepped during unit loop testing. However, some provision is made to step the register addresses manually. The desired section address, designated bits LS through L2, is set according to the section address code. Care must be taken not to set in an unassigned section. The parity bit, P, must reflect a manual parity count of the 19 other bits (L3 through

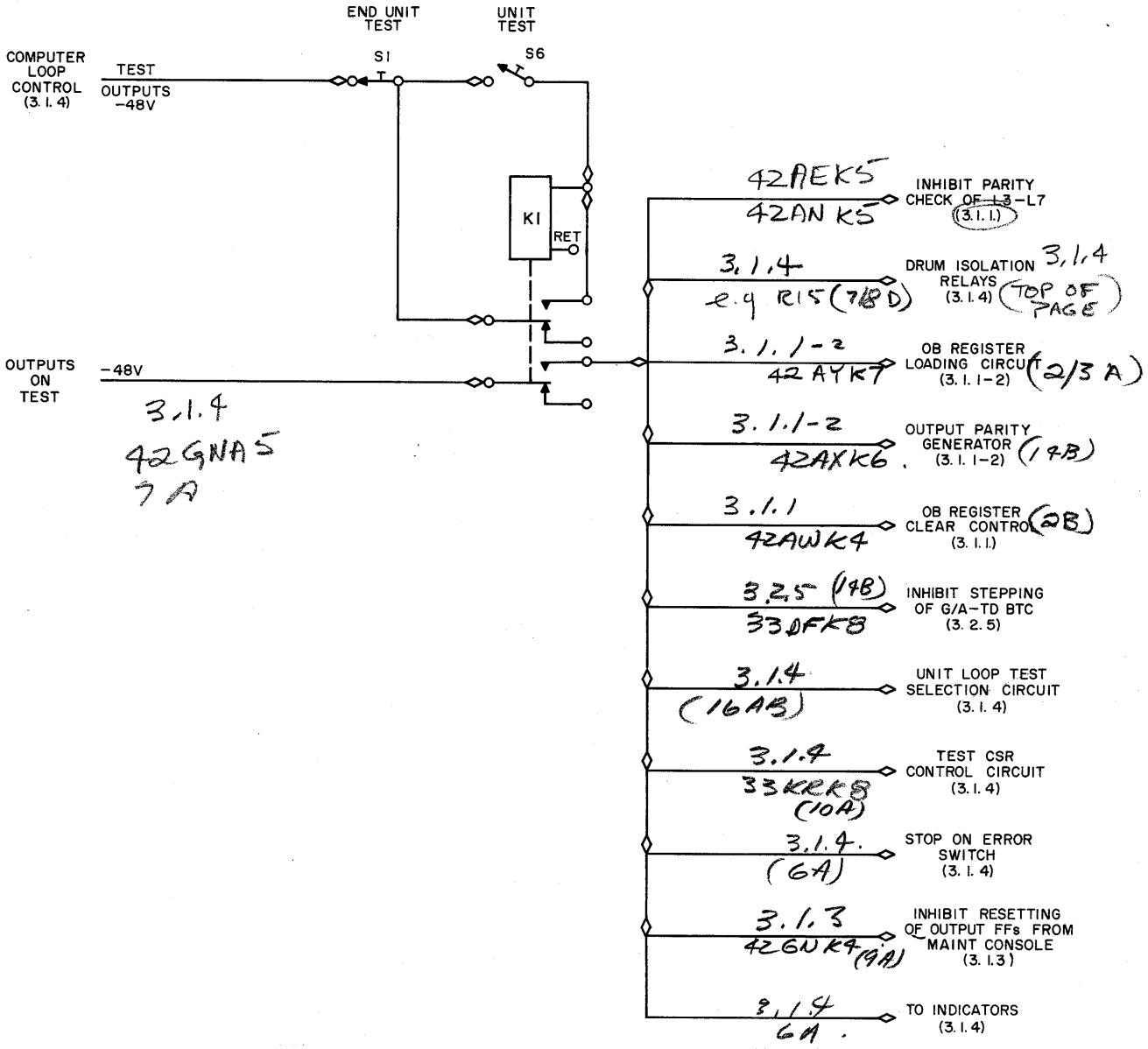


Figure 4–3. Unit-Loop-On-Test Control Circuit (3.1.4), Simplified Logic Diagram

L7 are not parity-checked during a unit loop test) so as to produce odd parity for all 20 bits.

1.2.3 Inhibit Resetting of Right Drum Word

Under normal operation, the parity drivers of the output control element clear the flip-flop register approximately 7.9 μsec after the word is entered. During test operations, however, the right drum word should remain in the flip-flop register until it is complemented by the completely processed, looped-back word for G/A-FD, BO1, BO2, G/G, and G/A-TD tests, or visually compared with the TTY monitor for TTY tests.

The clearing of right drum word registers is prevented whenever the Output System is placed in unit loop test. As shown in figure 4–3, the —48V relay voltage level is passed by unit test relay K1 to the relay in the parity register and drivers (fig. 2–8) which controls the application of the clear pulse. The opening of this latter relay prevents the clear pulse from being passed to the right drum word flip-flops, the output parity generator flip-flop, and the input parity flip-flop. The clearing of the LS-L2 and L8-L15 flip-flops is not prevented since only the message portion of the drum word (right drum word) and the output parity bit arrive at the output of the output storage element. Therefore, only this (the right) portion of the drum word and the output parity bit are looped back to the flip-flop register for comparison purposes.

Since the address portion of the left-half drum word (L3-L7) is automatically or manually stepped during read-in, the clear pulse to these flip-flops is delayed

until all legal register addresses contain the test word (fig. 2–9).

1.2.4 Clearing Alarms and Resetting Flip-Flops

Before the test operation is begun, all alarms and flip-flops in the Output System should be cleared by depressing the CLEAR ALARMS and RESET FLIP-FLOPS switches (S5 and S4). This action grounds the pulse generators in the pulse distributor circuits of the output computer section. Clear pulses now pass to the appropriate circuits. (See fig. 2–42.)

1.2.5 Unit Loop Test Selection Circuit

Selection of the various sections for unit loop testing is accomplished by means of three relays, depicted in figure 4–5. As shown in the figure, these relays are controlled by select section switches LS, L1, and L2, which are located on the unit test door. When it is desired to select a particular section for unit loop test purposes (say, the G/A-FD section, sect. 1), then select section switch L2 must be operated. In addition to inserting the section number (001) in the OB register, this switch, when operated to the closed position, allows —48V to be applied to K3, energizing it..

It can also be seen from the figure that the —48V relay voltage is also routed through the normally closed contact points (K1-1 NC, K2-1 NC) of de-energized K1 and K2 and routed through the now energized K3 contact points (K3-1 NO) to light an indicator lamp associated with the G/A-FD section. This not only provides a visual indication that the G/A-FD storage section has been selected for unit test but also serves as an additional check on the operation of the associated relays. In addition to the above, the —48V relay voltage is routed through the normally closed contact points (K1-2NC, K2-4NC) of de-energized K1 and K2 and further routed through the contact points (K3-6 NO) of energized K3 to energize all the G/A-FD unit test relays. The latter test relays are also shared by the BOMARC 1 and BOMARC 2 sections, since the operation of these sections is almost identical with that of the G/A-FD storage section.

During a unit loop test operation of the Output System, only one section will be processing test data information at one time; thus no interaction between relays is possible. The unit loop test switching procedure employed by the other sections of the Output System is identical with that described for the G/A-FD storage section; therefore, their operations need not be presented here.

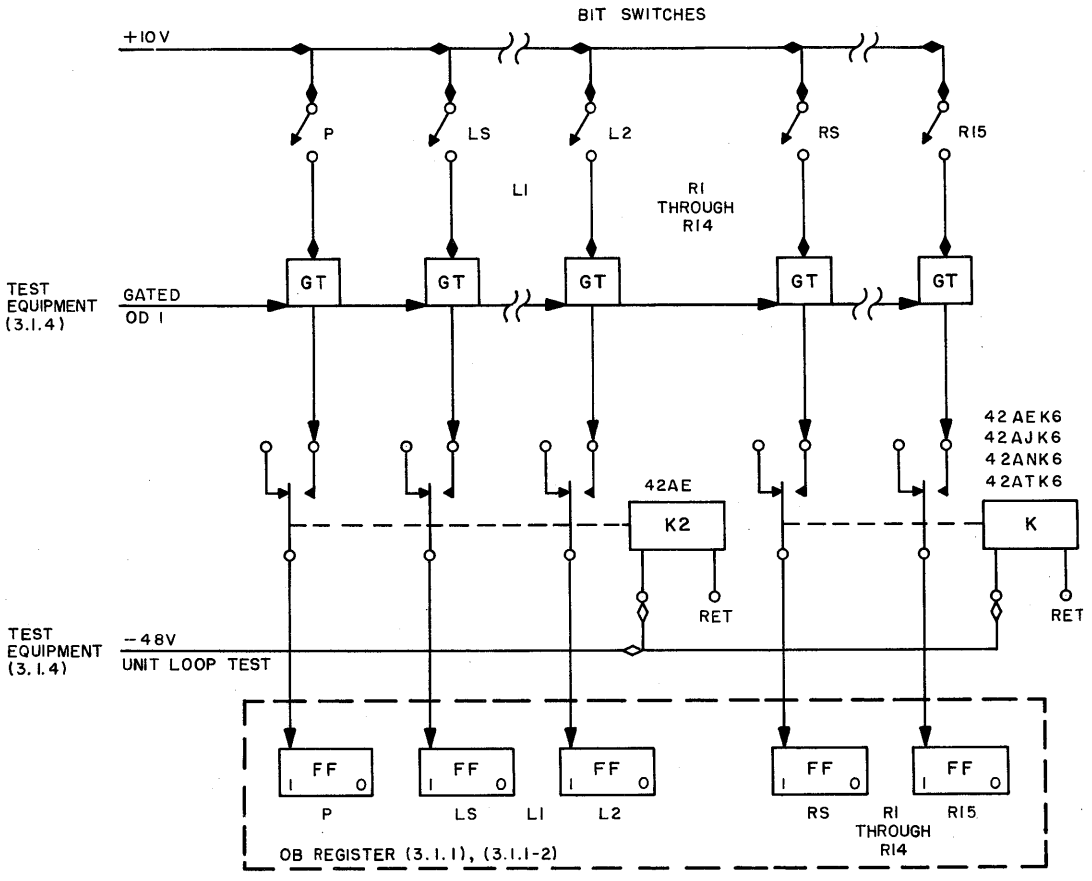


Figure 4–4. Drum Isolation and Test Bit Circuit (3.1.4), Simplified Logic Diagram

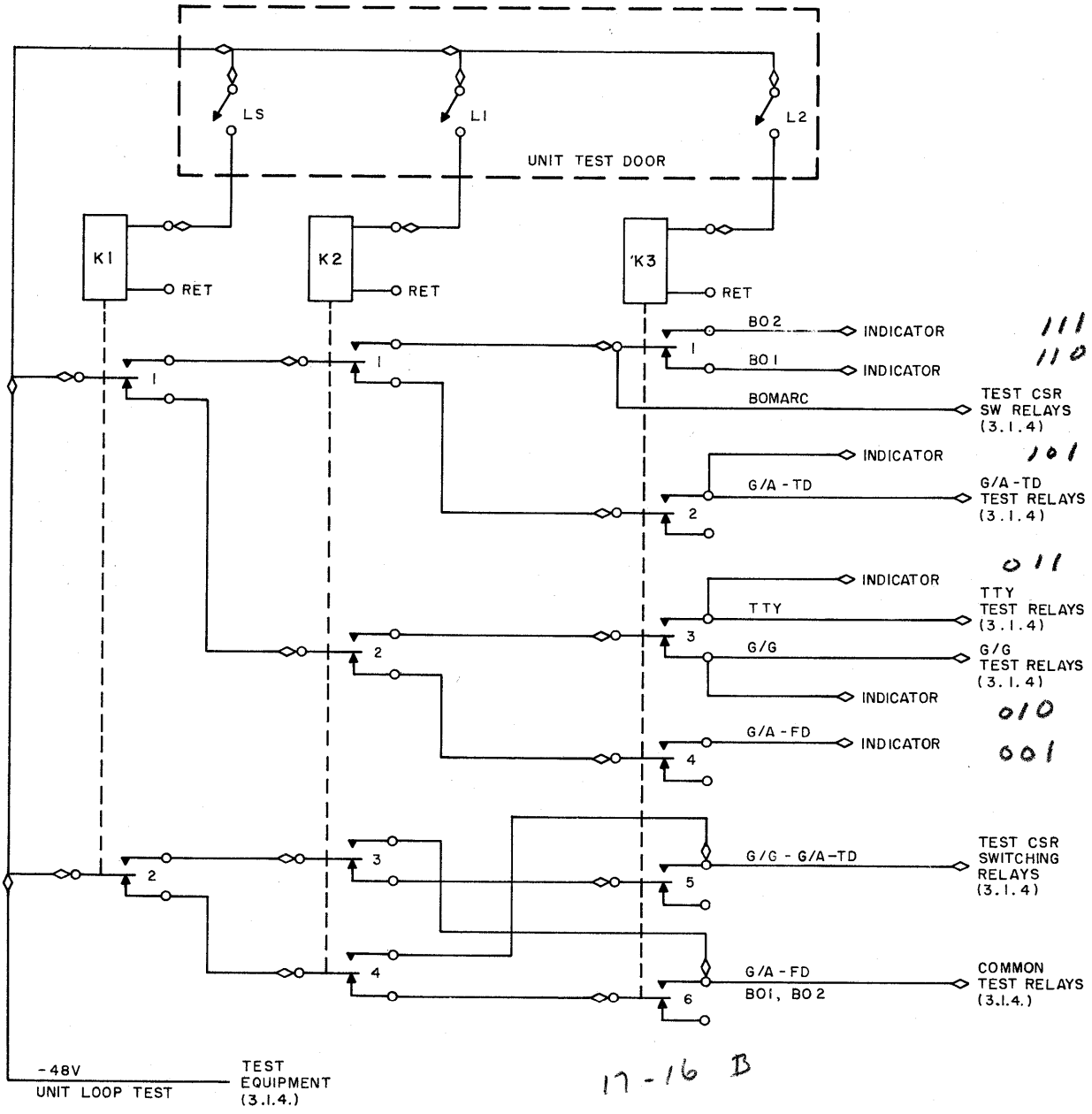


Figure 4–5. Unit Loop Test Selection Circuit (3.1.4)

1.2.6 Test Start Control

Before a unit loop test is started, the previous basic switch settings must be made. Then the specific switch settings described in 1.4.1 must be made, depending upon the storage section (G/A-FD, BO1, BO2, G/G, G/A-TD, or TTY) selected. Also, as described in 1.2.13, the method of error detection is selected. If the STOP ON ERROR switch is engaged, the test should be started by depressing the START CYCLE pushbutton, S3. As shown in figure 4–6, this action grounds the pulse generator, which produces a pulse to clear the master stop flip-flop. This latter flip-flop produces an enable-OD level, which then causes the various OD pulses to be distributed by the output control section. This action sets the circuits into operation. Also, the start pulse is sent to the 1,300-pps generator to clear its flip-flop at the start of the test.

As described in 1.2.13, if the STOP ON ERROR switch is not engaged, the OR circuit following the master stop flip-flop has a +10V level on it at all times. In this case, the enable-OD-signal level is always present and the Output System is continuously cycling. Under this condition, the test is always in progress, even while the test word is being entered. Therefore, the START CYCLE button has no significance.

1.2.7 Test Word Read-In

To unit-loop-test the individual storage sections in the Output System, a test word, as selected by the bit switches located on the unit test door, is read into each individual address of a selected storage section in sequential fashion until all legal addresses have been read into. In effect, the read-in operation of the test word, by address, into a specific core storage array is accomplished by stepping the address register until the test word has been read into all legal addresses of the storage section under test. The read-in of the test word and the stepping of each register address are accomplished under the control of the test word generator and address register stepping flip-flops, shown in figure 4–7.

As shown in figure 4–7, the start-search pulses generated from any one of the individual storage sections are used to set the test word generator flip-flop. When set, the flip-flop will generate a level to condition GT 1, which is strobed by OD 1 pulses. During a unit loop test, the gated OD 1 pulses strobe GT's 2 and 3, in addition to complementing the register stepping flip-flop which controls both the stepping of the register addresses and the read-in operation of the test word into the OB register. Gates 2 and 3 are conditioned by the outputs of the register stepping flip-flop. Initially, this flip-flop is clear and is complemented by a gated OD 1 pulse to its set side; GT 3 thus is conditioned to pass the OD 1 pulse.

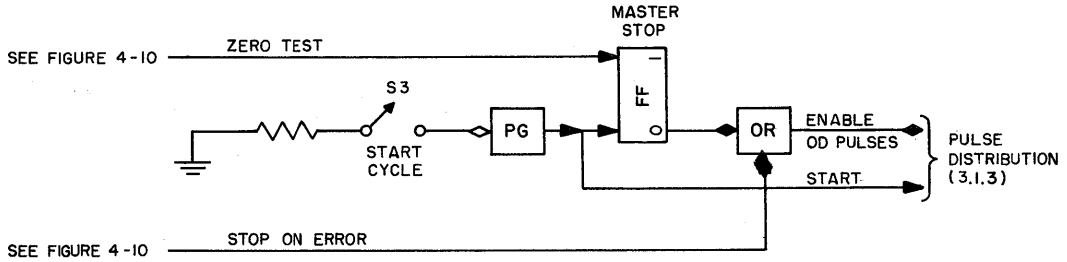


Figure 4–6. Test Start Control (3.1.4), Simplified Logic Diagram

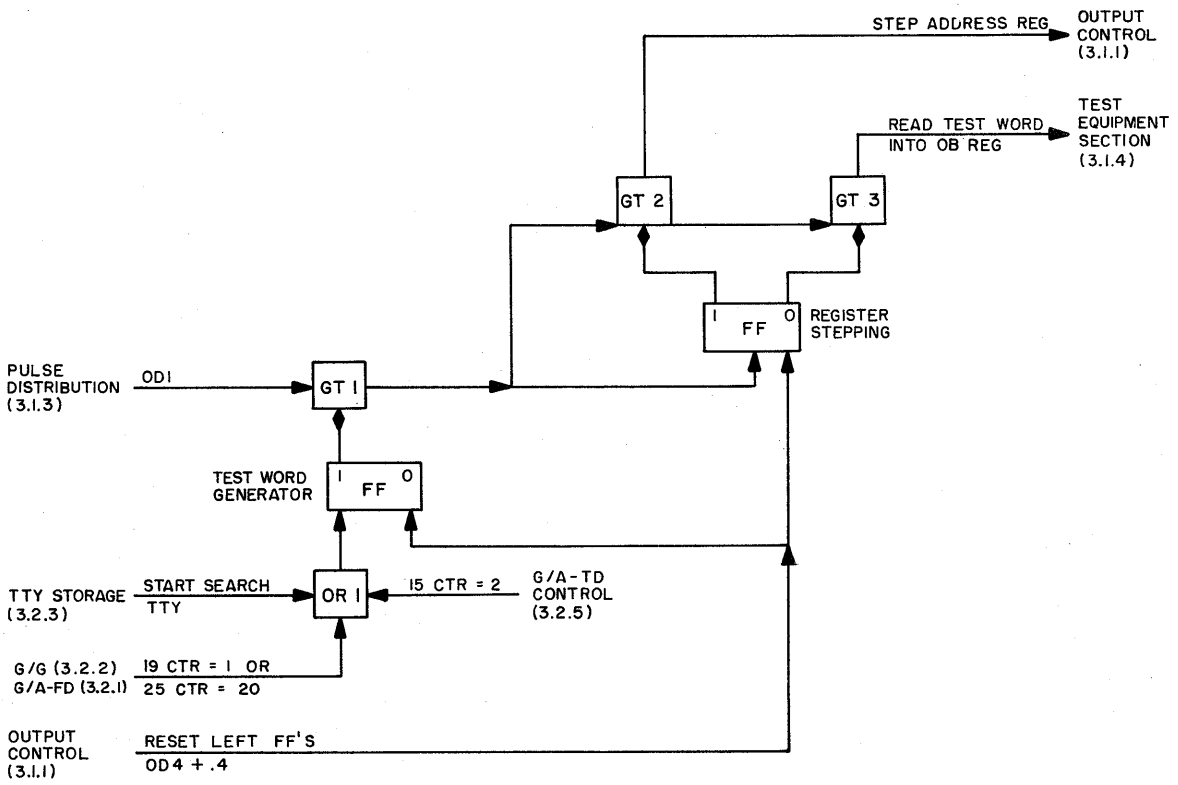


Figure 4–7. Test Word Generator and Address Register Stepping, Simplified Logic Diagram

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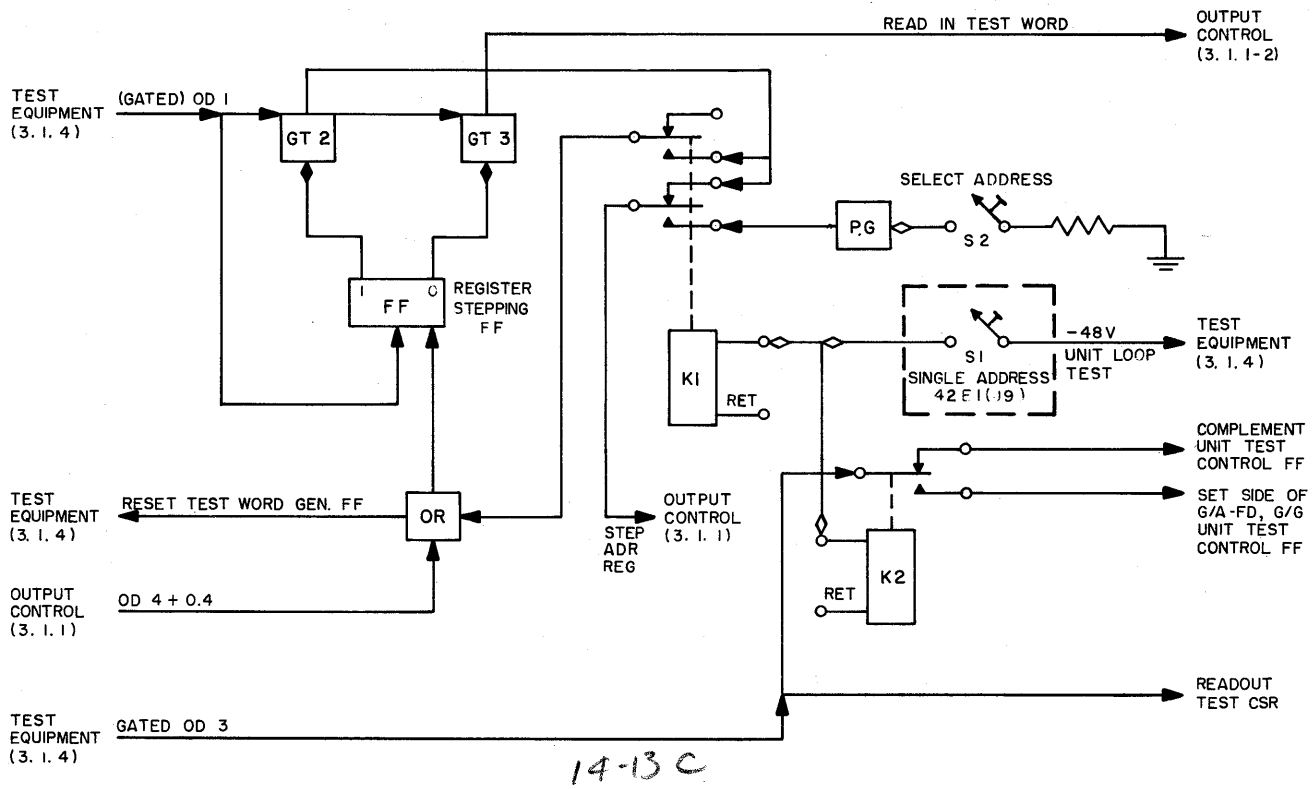

Figure 4–8. Single-Address Stepping Circuit (3.1.4), Simplified Logic Diagram

The latter is sent as a read-test-word pulse to the OB register. The test word is now inserted into register address 0. Succeeding OD 1 pulses strobe conditioned GT 1. This gated OD 1 pulse strobes GT's 2 and 3 while at the same time complementing the register stepping flip-flop to its clear side. Gate 2 is now conditioned to pass the same OD 1 pulse which is now used to step the register address to address 1. This action is repeated until all addresses in a particular storage section are made to contain the test word. When this occurs, the register stepping flip-flop is set in a status conditioning GT 2 to pass the following gated OD 1 pulse, thus stepping the address register to an illegal address count. When this occurs, a reset flip-flop pulse (OD 4 + 0.4) is gated from the output control element to clear both the test word generator and the register stepping flip-flops, thus ending the read-in operation of the test word information by address into the core storage array of the selected storage section under test.

1.2.8 Single-Address Stepping

Provisions are made to incorporate an additional refinement or feature should an error be detected while processing the test word through a selected storage section into an array. In the event that an error is detected, an alternate method of reading in the test word is performed; i.e., each register address is stepped, one at a time, when the SELECT ADDRESS pushbutton (S2) is depressed. Figure 4–8 depicts the single-address stepping circuit used to perform this function.

As shown in figure 4–8, selection of test word read-in in the single-address mode is accomplished by closing single-address switch S1, thus energizing K1 and K2. Following this, SELECT ADDRESS pushbutton S2 is depressed, causing a pulse to be generated through the closed contact points of K1 as a stepping pulse to step the register address portion of the OB register. Each time the SELECT ADDRESS pushbutton is depressed, the register address will be stepped to its succeeding count. Energized K2 will allow gated OD 3 pulses to set the unit test control flip-flop. The function of the latter is described in the following paragraphs.

1.2.9 Transfer of Word from Output Storage Section to Test Circuits CSR

The test data bits that are contained in all register addresses of the selected storage array are read out of the array into the output shift registers (OSR's) by columns containing either all 0's or all 1 bits. This, in effect, represents well over 200 data bits that would have to be read into the test core shift register (CSR). The test CSR is capable of handling a maximum of 17 data bits; hence, it can be seen that some provision must be made to reflect the composite of all data bits stored in the selected core storage array into the test CSR. This is accomplished by reading out each column of an array, simultaneously checking the odd or even

count of each column as it is read out, and inserting the resultant count of each column into the test CSR. This function is accomplished by using the existing parity checking circuit shown in figure 4–9 to determine the total odd or even count of test data bits as they are read out of the OSR's.

The resultant condition of the parity check circuit that is obtained after a column of test data bits is shifted out of the OSR's is subsequently fed to control circuits, which determine whether a 1 bit is to be primed into the test CSR. The parity checking circuits and control circuitry are shown in figure 4–9 and discussed in detail in the following paragraphs.

As seen from the figure, the test data read out of the OSR's is supplied to the complement lines of the parity checking flip-flops. Initially, these flip-flops are cleared and are complemented every time a 1 bit is read out of the OSR's. If the array column which was read out contained all 1 bits, then each parity checking flip-flop is complemented an odd number of times. For G/A-FD, BO1, and BO2, each parity checking flip-flop is complemented 13 times per column of 1 bits read out. For G/G, each parity checking flip-flop is complemented five times. Thus the parity checking flip-flops are in a set status at the end of readout of a single column of 1 bits from the OSR. However, in the case of G/A-TD, no output parity check is performed on the test word during a test transfer operation. The latter is discussed in detail in 1.2.12.

It must be noted from the figure that GT 1 will be conditioned to pass an output-parity-alarm pulse whether an error is present during the parity checking cycle or not and that, therefore, the alarm pulse is meaningless during this particular operation. If the parity count for a column of 1's as read out is odd, indicating no error, both the AND 1 and OR 2 circuits are conditioned, and their output levels are applied as conditioning levels to the OR 3 and OR 4 circuits, respectively. As a result, both GT's 2 and 3 are conditioned to pass OD 4–13 pulses, which strobe them. These pulses are generated at the completion of a column readout and are passed by GT's 2 and 3 to strobe GT's 4 and 5. The conditioning levels for the latter gates are supplied by the G/A-FD, BO1, BO2, G/G unit loop test control flip-flop. This flip-flop is complemented by gated OD 3 pulses at the end of an array readout at 25-counter-19 time whenever the single-address mode is not being used during a test. However, if the single-address mode is used for test, the OD 3 pulses are fed to the 1 side of the unit loop test control flip-flop via energized K2, shown in figure 4–9.

When the single-address mode is not used during a unit loop test, the unit loop test control flip-flop is complemented, conditioning either GT 4 or GT 5. Hence, either gate can pass the gated OD 4–13 pulse, which strobes them. The data pulse stretcher flip-flop is then set via OR 5 and the normally closed contact points of K1. This relay (K1) is energized only when a unit loop test of the G/A-TD storage section is in progress. With the setting of the data pulse stretcher flip-flop, a test data bit is primed into the test CSR as each individual array column is read out. As each test data bit is entered into the test CSR, it is shifted to succeeding cores until all bits have been entered into it. The individual bits are shifted under the control of the test shift control and test shift flip-flops.

At the end of an array column readout, an OD 4–13 pulse is generated and gated to strobe both GT's 2 and 3, in addition to setting the test shift control flip-flop via the normally closed contact points of K1. The latter, when set, generates a level to condition GT 6, which is normally strobed by an OD 2 pulse. Similarly, the OD 2 pulse is also used to clear both the data pulse stretcher and test shift control flip-flops. At this time, the OD 2 pulse will be passed by conditioned GT 6 to set the test shift flip-flop. Hence, each time that the latter flip-flop is set, shifting of the CSR will take place regardless of whether a bit has been primed into the test CSR.

To summarize the test word transfer operation during a unit loop test, a test word is read out of an array by columns and is parity-checked for an odd or even count. The resultant test data bit count is then primed into the test CSR under the control of the unit loop test control and data pulse stretcher flip-flops. Subsequently, the bit count is shifted to succeeding cores in the test CSR under the control of the test shift control and test shift flip-flops until all test data bits have been inserted into it. The test word data is then read out of the test CSR in parallel form to complement the right half-word of the OB register.

The aforementioned circuit analysis reflects normal test operation; however, this test cycle is repeated several times to determine whether the gain or loss of a bit has been incurred during a test word transfer. Detection of "grown" or "dropped" bits is discussed in the following paragraph.

1.2.10 Data Bit Generator Error Check (G/A-FD, BO1, and BO2)

It was stated in the preceding paragraph that a normal parity check test operation during a test word transfer for G/A-FD, BO1, and BO2 storage sections should result, at the end of a parity check count, in having both parity checking flip-flops come to rest on their 0 and 1 sides (both clear or both set). This then reflects a no-error operation.

However, some errors might be incurred during a test word transfer operation wherein some test data

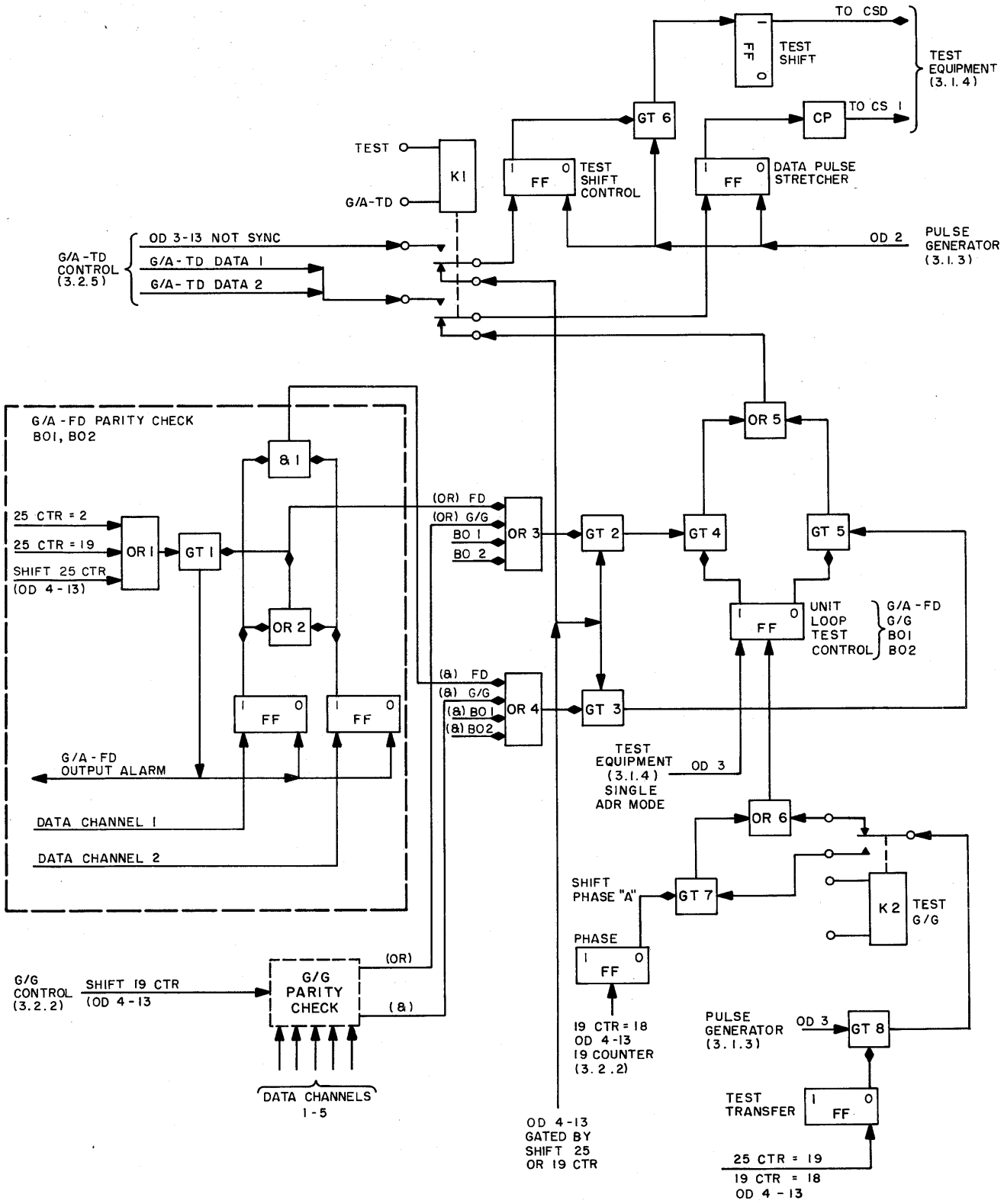

Figure 4-9. Test CSR Data-Bit Generator and Error Check Circuit (3.1.4), Simplified Logic Diagram

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bits might be dropped (loss of a bit) or, on the other hand, grown (gain of a bit). The error detection circuit, shown in figure 4–9, is used to detect errors that might be incurred during a test word transfer operation of the G/A-FD, BO1, BO2, and G/G storage sections.

As stated in 1.2.9, the word transfer test cycle is repeated several times (a minimum of two test cycles) to allow for the detection of grown or dropped bits. That is to say, a complete array could conceivably contain a column of 0's and a column of 1's, a column of 0's and a column of 1's, etc...; hence, one complete test cycle is required to check the columns of 0's and another to check the columns of 1 bits.

Figure 4–9 depicts the error check circuit, which comprises the unit loop test control flip-flop and its associated gates, GT's 4 and 5. It can be seen from the figure that only GT 4 is strobed by OD 4–13 pulses when an error is present during a parity check test cycle. Also, GT 5 can be conditioned to pass OD 4–13 pulses only under the conditions that the unit loop control flip-flop is clear and that the OD 4–13 pulse is present at the gate. The latter condition can occur only if a parity check count, when performed on any one column of 1's, is found to be correct.

It can be further stated that, when the unit loop control is at rest on its clear side for one array readout cycle, a dropped bit will be detected. Conversely, if the flip-flop is at rest on its set side for one array readout cycle, a growing bit will be detected. Assuming that a bit was dropped during a parity test cycle of a column of 1 bits and that the unit loop test control flip-flop is at rest on its clear side at this time, then GT 4 is strobed by a gated OD 4–13 pulse. Gate 4 would remain deconditioned and could not pass the pulse to set the data pulse stretcher flip-flop, and no bit is primed into the test CSR, indicating that a bit has been dropped.

On the other hand, had the unit loop control flip-flop been at rest on its set side at that time, then the dropped bit could not have been detected until the following test cycle because the test CSR would still be primed. Conversely, if a bit is grown during a parity check test cycle of a column of 0's, then GT 4 is strobed by a gated OD 4–13 pulse, assuming, however, that the unit loop test control flip-flop is at rest on its clear side at this time. Gate 4 remains deconditioned and cannot pass the pulse to set the data pulse stretcher flip-flop. No bit is primed into the test CSR, and the error remains undetected until the following test cycle.

In the ensuing test cycle, the unit loop control test flip-flop is complemented to its set side, GT 4 is conditioned, and, if the error is still present, the OD 4–13 pulse is passed by the conditioned gate to set the data pulse stretcher flip-flop, thus priming a bit into the test CSR indicating that a bit has been grown.

From the above explanation, it is evident that the sequence for determining whether a parity check for growing or dropping of bits is to be performed is largely dictated by the status of the unit loop test control flip-flop during any given test cycle. It is obvious that, when a column of 1 bits is being processed for test and no error is present in the column, the status of the unit loop control flip-flop, at any time, is relatively unimportant since both GT's 4 and 5 would be strobed by the OD 4–13 pulse and either could pass the pulse to set the data pulse stretcher flip-flop, inserting a bit into the test CSR.

1.2.11 Data Bit Generator Error Check (G/G)

The parity checking operation for the G/G storage section is, in some respects, similar to that described for the G/A-FD storage section. However, because the G/G storage section utilizes two core storage arrays (A and B), some additional refinements are used to select a particular array for test. Also, because both arrays are tested in sequential fashion, regardless of which array is first processed for test, the parity-checking sequence is changed to reflect the following (fig. 4–9):

a. Array A is checked for dropped bits.
b. Array B is checked for dropped bits.
c. Array A is checked for grown bits.
d. Array B is checked for grown bits.

Selection of a particular array for parity-checking purposes is dictated by the status of the flip-flop during a given cycle. This flip-flop is complemented by an OD 4–13 pulse at 19-counter-18 or at the end of a core array (A or B) readout. Complementing the flip-flop to its 0 side will select core array A to be processed for a parity check; likewise, complementing to its 1 side (set) selects core array B for test.

The parity-checking cycle for the G/G storage section begins at the end of a readout cycle at 19-counter-18 time, whereupon the test transfer flip-flop is set by an OD 4–13 pulse and the phase flip-flop is complemented to its clear side by this same pulse. Setting the latter flip-flop generates a shift phase A level to condition GT 7. The test transfer flip-flop, having been set, generates a level to condition GT 8 to pass an OD 3 pulse. When a parity check test of the G/G storage section is effected, K2 will be energized to pass the OD 3 pulse via its closed contact points to strobe conditioned GT 7. The OD 3 pulse is then passed by conditioned GT 7 to complement the unit loop test control flip-flop via the OR 6 circuit.

Assuming that the latter flip-flop is complemented to its clear side at this time, it follows that core array

A is now being parity-checked for dropping bits. At the conclusion of the array A parity check cycle, at 19-counter-18 time, the phase flip-flop is again complemented to its 1 side. However, GT 7 is now deconditioned, no pulse (OD 3) is passed to complement the unit loop test control flip-flop, and the flip-flop remains cleared. As a result, core array B is now processed for a parity check of dropping bits, completing the first parity check cycle for both arrays A and B.

The above parity check test cycle is again repeated for detecting grown bits. When this occurs, the unit loop test control flip-flop will be complemented to its 1 side, whereupon it will remain in this state until both arrays have been parity-checked for grown bits.

1.2.12 G/A-TD Test Word Transfer

The test word transfer operation during a unit loop test of the G/A-TD storage section differs greatly from that described for the G/A-FD, BO1, BO2, and G/G storage sections. The difference lies in the fact that G/A-TD words, which are 17 data bits in length, are stored in the register address column of an array and, since the G/A-TD arrays are read out by addresses, one complete G/A-TD test word is transferred to the test CSR. Subsequently, a zero test of the G/A-TD test word is performed at the conclusion of the word transfer operation, eliminating the need for performing a parity or error check upon the test word.

As shown in figure 4–9, the G/A-TD test information is sent over G/A-TD data channel lines to the data pulse stretcher flip-flop via energized K1. This relay is energized each time a unit loop test of the G/A-TD storage section is in progress. Each time the data pulse stretcher flip-flop is set, a 1 bit will be primed into the test CSR. Shifting of the primed bit in the test CSR is primarily a function of the test shift control and test shift flip-flops. This function is initiated by an OD 3–13-and-not-sync pulse, which is generated at the end of an array column readout.

In summary then, a G/A-TD test word is read out of an array by columns, with each column representing an address, and transferred via data channel lines to the data pulse stretcher flip-flop. The test data is then primed into the test CSR under the control of the data pulse stretcher flip-flop. Subsequently, the data bits are shifted to succeeding cores in the test CSR under the control of the test shift control and test shift flip-flops until all test data bits have been entered in it. The G/A-TD test word is now available for zero test purposes. (This operation is discussed in detail in 1.2.13.)

1.2.13 Error-Detection AND Circuit

When the complete test word has been read into the test CSR as described in 1.2.9, a test-transfer pulse initiates a synchronizing cycle which results in the sampling of each core in the register. Each core containing a 1 bit sends a complementing pulse back to a particular flip-flop in the flip-flop register of the output Drum System. This flip-flop would be the corresponding right test word flip-flop into which the bit was originally entered. (The circuitry involved in sampling the test CSR is described in 1.3.1.) If, in a particular right word flip-flop, the original bit entered was a 1 and the complementing bit is (correctly) also a 1, the flip-flop is complemented with the 0 side up. If, in a particular right word flip-flop, the original bit was a 0 and the complementing bit is (correctly) a 0, the flip-flop will remain with its 0 side up. However, if the original bit is a 1 and the complementing bit is (incorrectly) a 0, or if the original bit is a 0 and the complementing bit is a 1, the flip-flop is complemented with the 1 side up.

As shown in figure 4–10, the 0 side of the 16 right-word flip-flops of the flip-flop register and the 0 side of the output parity bit generator flip-flop are fed to the 17-way AND circuit. If none of these bits have been erroneously changed from 0 to 1 or from 1 to 0 during the processing through the Output System, the complementing of the flip-flops should reset the 0 sides of all the flip-flops. The 17-way AND circuit conducts. The inverter then prevents any further passage of the signal level. However, if one (or more) of the flip-flops is complemented with the 1 side up, which would happen if an error occurred in processing the test word, the AND circuit would not conduct. The inverter then passes a level to the OR 1 circuit to condition GT 1. The select section bit switches (LS, L1, and L2) on the unit test door are operated to select a particular section (G/A-FD, BO1, BO2, G/G, or G/A-TD), reflecting the section address of the test word. In any case, one of the two relays (K4 or K2) shown in figure 4–10 will be energized. For a zero test of a G/A-FD, BO1, or BO2 test word, K2 will be energized to pass a 25-counter-20 (OD 4–13) pulse; for a G/G test word, K2 is in a de-energized state to pass a 19-counter-19 (OD 4–13) pulse; for a G/A-TD test word, K4 is energized to pass a gated OD 4 pulse. The individual pulses are then sent to strobe GT 1 as a zero test pulse for their respective storage sections. The pulses occur at the end of readout time in the respective sections and therefore arrive after the complete processing of the test word. If GT 1 is conditioned as a result of an error in the processing of the test word by the Output System, the gate passes the zero-test pulse. This sets the 1 side of the master stop flip-flop. Two actions can take place.

If the STOP ON ERROR switch (J10) has been operated to the closed position, the unit-loop-on-test voltage level is passed to energize K6, passing a —30V

level to the OR 4 circuit. This results in the enable-OD-pulse-signal level's being produced only if the 0 side of the master stop flip-flop is up. Since an error causes the 1 side of this flip-flop to be up, the enable-OD level is cut off and the test stops.

If the STOP ON ERROR switch (J10) is not operated, a +10V level rather than a −30V level is applied to the OR 4 circuit. Therefore, regardless of whether the 17-way AND circuit detects an error, the enable-OD-pulse level remains up and the test operation cycles continuously without stopping. However, neons which are not shown in figure 4–10 light if a flip-flop is not correctly complemented; these neons indicate the presence of an error.

1.3 UNIT LOOP STORAGE

The unit loop storage section is the test CSR previously described. It accumulates the processed test-word bits from the selected section and register of the output storage section. The bits are shifted into the test CSR, which is a series of 17 tape cores (core shifts) in serial form. At the end of the output storage section readout operation, the contents of the core shifts are read out in parallel form to complement the corresponding flip-flops in the right-half of the flip-flop register of the output control section, where the test word was originally entered.

Since the TTY word is not fed back to the flip-flop register for comparison with the original test word but is, instead, sent to a TTY monitor for a visual comparison, the unit loop storage discussion applies only to G/A-FD, BOMARC 1, BOMARC 2, G/G, and G/A-TD test words.

1.3.1 Parallel Readout Control

The parallel readout control circuit controls the parallel readout of the test word in the unit loop storage register (CSR). Selection of a particular storage section for unit loop test purposes is effected by closing select section switches LS, L1, and L2, located on the unit test door (fig. 4–1). Depending upon which section address is assigned to the test word, closing these switches singly or in combination will cause associated relays (K1, K4, or K5) to be energized during a unit loop test.

For a unit loop test of the G/A-FD, BO1, and BO2 storage sections, a 25-counter-19 pulse is used to produce the readout pulse; for a G/G test, a 19-counter-18 pulse is selected; for a G/A-TD test, an OD 3–13-at-17-counter-17-and-not-sync pulse is selected. Each of these pulses occurs just before the last group of like-order bits is read out of their corresponding storage sections. Hence, these pulses occur just before the last bit is read into the first core shift in the test CSR.

As shown in figure 4–11, when a unit loop test of the G/A-FD storage section is being performed, K4 will be energized to pass a 25-counter-19 pulse. This pulse is then sent through the normally closed contact

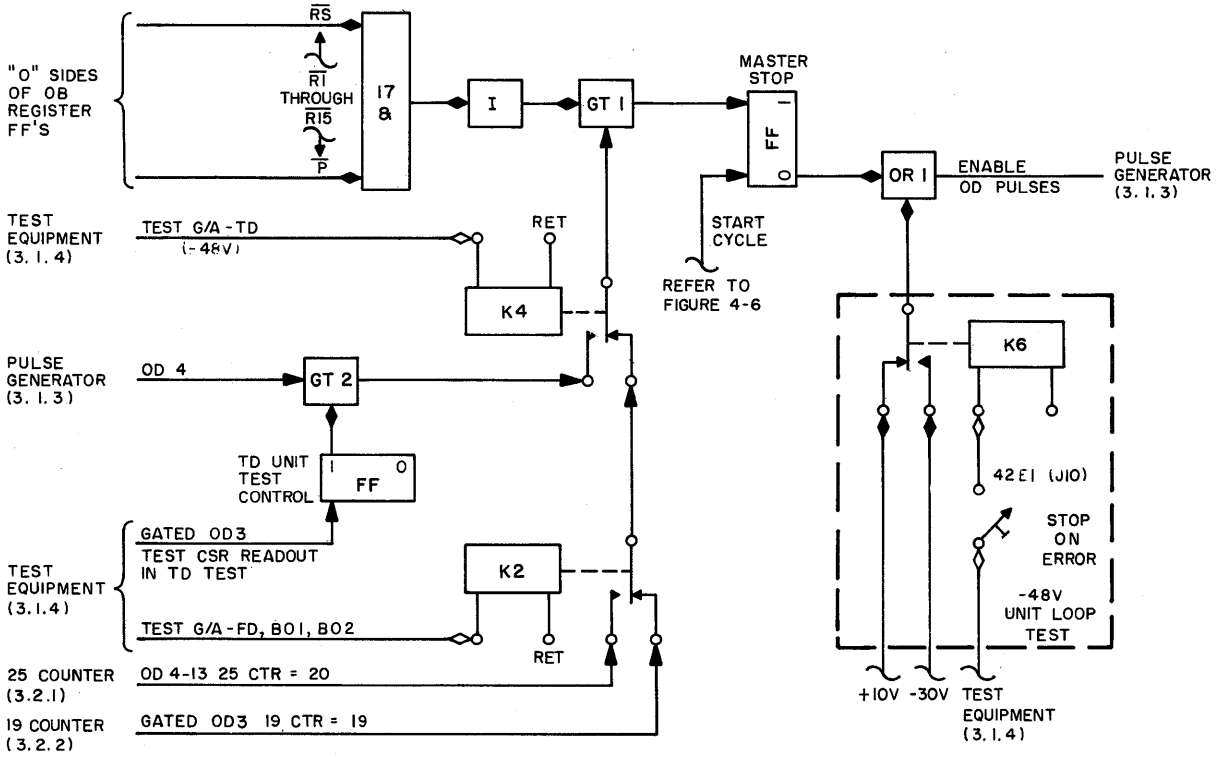

Figure 4–10. Zero Test and Master Stop Circuit (3.1.4), Simplified Logic Diagram

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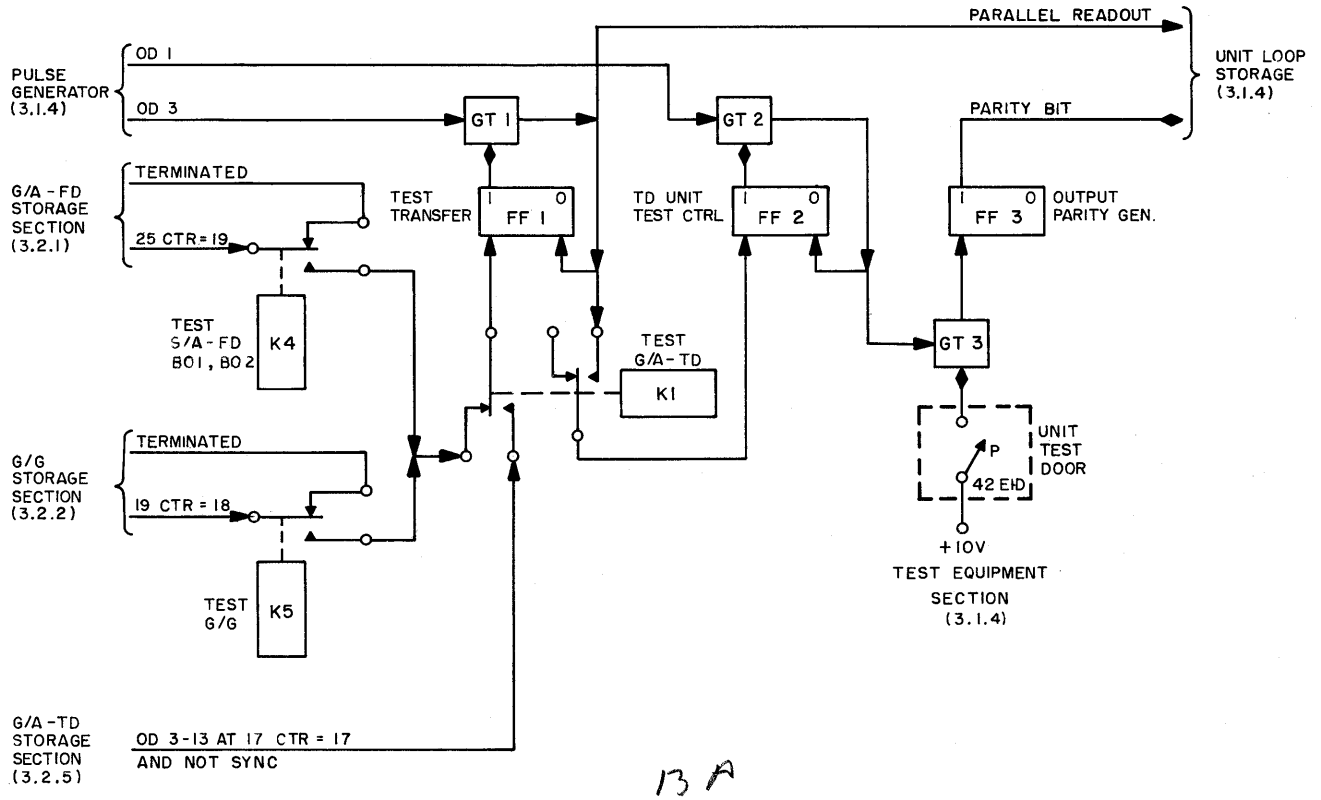


Figure 4–11. Parallel Readout Control Circuit (3.1.4), Simplified Logic Diagram

points of de-energized K1 to set the test transfer flip-flop. The latter flip-flop, when set, generates a level to condition GT 1 to pass an OD 3 pulse. This pulse is then sent as a readout pulse to strobe the parallel readout gates in the test core shift register circuit to effect the transfer of test information to the OB register for comparison purposes.

The parallel readout control operation for the BO1 and BO2 storage sections is identical with that described above. The parallel readout operation for the G/G storage section operates in the same manner as described above, except that a 19-counter-18 pulse is employed. However, the parallel readout control operation for the G/A-TD storage section differs somewhat from that for the other storage sections because the G/A-TD right drum test word must reflect an odd-parity count as opposed to the even-parity count required for test words emanating from other storage sections. Therefore, to prohibit the G/A-TD test word from acquiring an even bit count (RS to R15) and thus producing an erroneous word indication, additional circuitry (shown in fig. 4–11) is introduced to provide and maintain the odd-parity status of the G/A-TD test word during the parallel readout operation to the OBR. The readout control operation and the generation of odd parity during a G/A-TD unit loop test are discussed in detail in the following paragraph.

At the end of a column readout of a G/A-TD core storage array, wherein a complete G/A-TD test word is transferred to the test CSR, a gated OD 3–13-at-17-counter-17-and-not-sync pulse is selected and passed via energized K1 to set the test transfer flip-flop (fig. 4–11). This relay is energized only when a unit loop test of the G/A-TD storage section is being performed. The test transfer flip-flop, when set, generates a level to condition GT 1, which is strobed by an OD 3 pulse. The conditioned gate thus passes the OD 3 pulse, which is then sent as a parallel readout pulse to strobe the parallel readout gates of the test CSR to effect the transfer of test information to the OB register for comparison. In addition, the pulse clears the test transfer flip-flop. The OD 3 pulse is also sent to set the G/A-TD unit test control flip-flop via energized K1. The latter flip-flop, having been set at OD 3 time, conditions GT 2, which is strobed by an OD 1 pulse. The OD 1 pulse is passed by the conditioned gate to clear the G/A-TD unit test control flip-flop, at the same time strobing GT 3. The latter gate is conditioned by a +10V level produced when parity switch P, which is located on the unit test door, is closed. Hence, to ensure the odd-parity status of a G/A-TD test word, parity switch P is closed, conditioning GT 3, and the OD 1 pulse is passed to set the parity flip-flop in the OB register.

1.3.2 Core Register Circuit

The core register circuit, shown in figure 4–12, is a tape-core register of 17 core shifts and is similar to the 19-counter in the G/G storage section. The processed test-word pulse from the storage register control circuit reads the extracted bit into the read-in winding of the first core of the register. This read-in occurs for 5.0 μsec between OD 4 and OD 2 times. The shift pulse starts at OD 2 with the receipt of the start-shift signal from the storage register control circuit. The start-shift signal and the end-shift signal control the test shift flip-flop. This flip-flop supplies the shift pulse to the register. The shift pulse lasts 2.5 μsec, from OD 2 to OD 3. At OD 3 time, following the shift pulse, the former content of each core appears at the output line to the gate circuit at the same time that the bit is being read into the next core. However, there is no transfer through these gates unless they are pulsed by the readout signal. After the last pulse, however, the register is full. The readout signal, which comes from the parallel readout control circuit at OD 3 time and coincides with the end-shift signal, is applied to the parallel readout gates, causing the information to be transferred.

During normal operation of the G/A-FD storage section, as messages are read into the telephone line transmitting equipment, the order of bits R8 through R15 of the right drum word must be reversed to fulfill the requirements of the equipment at the other end of the telephone transmission line. These bits are also received in the inverse order by the unit loop storage during the unit loop test. Therefore, when testing G/A-FD or BOMARC registers, it is necessary again to reverse the order of bits R15 through R8. Reversal of bits is unnecessary in the case of G/G and G/A-TD test words.

Reversal switching is accomplished as depicted in figure 4–12. For a unit loop test of the G/A-FD storage section, K1 and K2 are not energized, and inversed data bits R15 through R8 are reversed through the normally closed contacts of the two relays in the order shown in figure 4–12. For a unit loop test of the BOMARC storage section, K2 is energized, causing inversed data bits R7 through R15 including parity bit P to be modified and passed through the normally closed contacts of de-energized K1 and closed contacts of energized K2 in the order indicated in figure 4–12. However, if a unit loop test of either the G/G or G/A-TD storage section is performed, K1 is energized, K2 is de-energized, and data bits R8 through R15 are transferrred in an unmodified form (in the order shown in fig. 4–12) through the closed contacts of energized K1 and the normally closed contacts of de-energized K2.

Thus, in the parallel readout operation, each bit is directed back to the individual flip-flop of the OB register from which the bit was originally generated.

1.4 SPECIFIC UNIT LOOP TESTS

The preceding paragraphs described the general, common circuitry and processes used in performing a unit loop test involving any of the storage sections in the Output System. The paragraphs which follow describe the particular processes and circuitry which are unique for each particular storage section. As has been previously mentioned, the output control element functions in the normal manner regardless of the storage section selected.

1.4.1 Ground-to-Air Frequency Division and BOMARC 1-2

The unit loop test operations for both the G/A-FD and BOMARC storage sections are identical in nature and, therefore, only that unit loop test operation associated with the G/A-FD storage section is presented here.

The overall operation of the G/A-FD storage section during a unit loop test is essentially the same as during normal operation except for a few minor variations. In effect, unit loop testing of the G/A-FD storage section is begun by activating the UNIT TEST pushbutton, causing the output test relay voltage to be applied to the test circuitry. Prior to setting up the test word, the OB register is isolated from the Drum System, the G/A-FD burst counters are inhibited, and alarms are cleared. Inhibiting the reset of the right drum word flip-flops is automatically performed when in a unit loop test. The desired section address and the test word are selected manually by means of bit switches located on the unit test door. If it is desired, a STOP ON ERROR switch is engaged to detect errors and stop the test cycle.

The unit test operation commences when the START CYCLE pushbutton is activated. The manually selected test word is then automatically read into each individual address register of the G/A-FD core storage array until all legal register addresses have been read into. This automatic read-in of the test word into all register addresses may be substituted by an alternate method of read-in, whereby the test word is manually stepped into each address register and is read out of the array one at a time.

Subsequent to the above read-in operation (automatic or manual), the test word stored in the array is read out in columnar fashion; that is, the resultant test data bit count of each column is read out and transferred via relays to the test CSR circuitry. During the transfer operation, an error check is performed on the test data bit count to determine whether bits have been

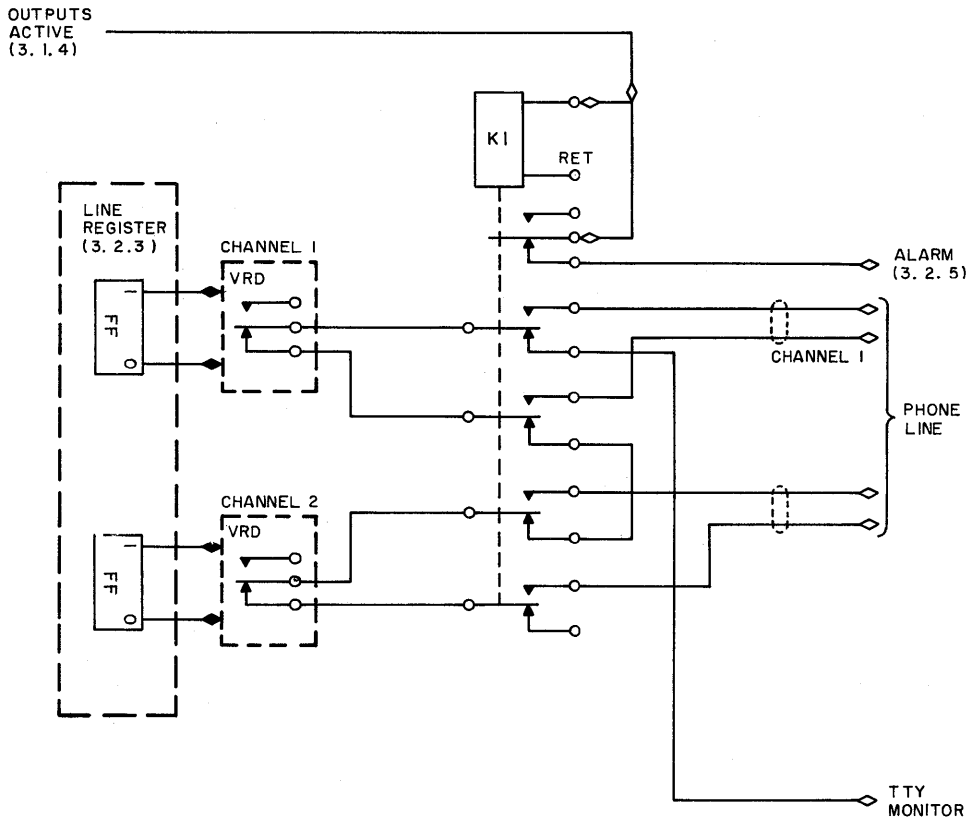


Figure 4–13. TTY Duplex and Test Switching for Messages 1 and 2 (3.2.3), Simplified Logic Diagram

grown or lost during the test word reading operation. In any circumstance, the test word is entered into the test CSR bit by bit under control of the unit loop test control circuitry. At the end of an array readout, a 25-counter-19 pulse is generated and sent to the test CSR, causing the test word in the core register to be read out, in parallel fashion, and sent to complement the OB register. At this time, a zero test is performed on the G/A-FD test word; that is, if the word in the OB register is not correctly complemented, an error has occurred and, with the STOP ON ERROR switch in an activated state, the test cycle will end. On the other hand, if the OB register has been correctly complemented, thus obviating the presence of any error, the test cycle will be repeated until the END UNIT TEST pushbutton is activated.

1.4.2 Ground-to-Ground

The overall operation of the G/G storage section during a unit loop test is essentially the same as that described for the G/A-FD and BOMARC storage sections, with but a few exceptions. The G/G storage section comprises two core storage arrays; hence, a unit loop test of this storage section necessitates that both arrays (A and B) be subjected to test. In addition, other circuitry peculiar to the G/G storage section (namely, the CMSR circuit and the switching circuit, which is used principally to switch test data information from one array to another) is also subjected to scrutiny during a unit loop test.

In the G/G unit loop test, a test word is automatically read into all the address registers of an array (say array A) during the search time period. The test word stored in array A is then read out during the first cycle of the 19-counter while, at the same time, the test word is being written into array B. At the completion of the array A readout cycle (19-counter-18 time), an OD 4–13 pulse is generated to complement the phase flip-flop to a 1. The latter, when set, produces a shift phase B level, thus selecting array B for readout of the G/G test word. Array B is read out during the second 19-counter cycle while, at the same time, the test word is being written into array A. At the end of the second 19-counter cycle at 19-counter-18 time, the phase flip-flop is complemented to 0 by an OD 4–13 pulse. In this state, the phase flip-flop generates a level selecting array A for readout of the test word.

It may be noted that, as one array is being read into, the other is being read out; hence, each array (A or B) is read out at every other cycle of the 19-counter.

Like the G/A-FD and BOMARC storage sections, the G/G test word may be automatically or manually

stepped into all address registers of a selected array. If the automatic-address stepping mode is used during a unit loop test, then the CMSR flip-flop neons located on the duplex maintenance console will be set, indicating that all legal address registers have been filled with the test word, that all message slots have been filled with the test word, and that readout of the test word is taking place. However, if the manual-address stepping mode is used during a unit loop test, the CSMR flip-flops will remain cleared because, in this mode, the G/G test word is entered into and is read out of each individual address register of a selected array one at a time; hence, the CMSR message slots are never filled with the test word and thus no completed message indications by the CMSR flip-flop are presented.

Following the readout of the G/G test word from core storage array A or B, the word is routed to the test circuitry. Here the word is processed for test in the same manner as that described in 1.4.1 for the unit loop test of G/A-FD or BOMARC test words.

1.4.3 Ground-to-Air Time Division

Unit loop testing of the G/A-TD storage section is similar in many respects to the unit loop test operation described for the G/G storage section except for a few minor variations, some of which are mentioned herein.

Like the G/G storage section, the G/A-TD storage section comprises two core storage arrays, a CMSR circuit, and a decoding circuit which is used specifically to select either of the two arrays in this section. In addition, the G/A-TD test word may, like G/A-FD, BOMARC, and G/G test words, be automatically stepped into all address registers of an array or manually stepped into each, both operations having been explained in previous paragraphs. However, unlike the other storage sections, where a test word is contained in columns of like-order bits in their respective storage section arrays (that is, one array column contains all RS bits, the second, all R1 bits . . . . , etc.), the G/A-TD core arrays store a complete G/A-TD test word in each address column (there being 12) of their respective arrays.

Furthermore, unlike the other storage sections, readout of the G/A-TD test word from the individual arrays is performed by address, in parallel fashion, to two OSR's. This is in direct contrast to that method of readout employed by the other storage sections, where columns of like-order bits are read out in parallel fashion to one OSR.

In the G/A-TD unit loop test, a test word is automatically entered into each address column of a selected array (A or B) during the G/A-TD search time period. The test word now contained in all address columns of an array (say array A) is read out to the OSR's during the first cycle of the 15-counter while the test word is being read into array B. At the completion of the first 15-counter cycle (15-counter-15 time), an OD 4—13 pulse is generated to complement the phase flip-flop in the decoding circuit to a 1. The latter, when set, generates a shift phase B level, thus selecting array B for readout of the test word during the second 15-counter cycle while the test word is being read into array A. Like the G/G storage section, as one array is being read into, the other is read out at every other cycle of the 15-counter.

As in normal operation, the G/A-TD test words, when read out of the selected array, are temporarily stored in the OSR's, one word per OSR, whereupon they are simultaneously shifted out of the OSR's in serial fashion to separate test data lines and routed to the test circuitry. In the test circuitry, the G/A-TD test words are processed in the same manner as described for unit loop testing the G/A-FD, BOMARC, and G/G storage sections, except that different control pulses are used to synchronize the G/A-TD test word flow through the test circuitry during a unit loop test. First, synchronization is accomplished by using the OD 3—13-and-not-sync pulse to shift the G/A-TD test data bits into the test CSR until a complete test word has been read into the test CSR. Secondly, an OD 3—13-at-17-counter-17-and-not-sync pulse is used to initiate the transfer of the G/A-TD test word from the test CSR to complement the OB register (see fig. 4—11). Thirdly, a gated OD 4 pulse is used to zero-test the G/A-TD test word for any errors that may occur during unit loop tests (fig. 4—10).

It has been stated that the test data information is routed over two test data channel lines, channels 1 and 2. However, only one test data line is tested at one time. Therefore, selection of a particular test data channel line for test is largely dependent on the status of the TEST G/A-TD CHAN 2 switch. If the latter is activated, the test data contained in the test data channel 2 line will be processed for test. If the latter is left inactive, the test data contained in test data channel 1 line will be processed for test.

1.4.4 Teletype Monitor Test

During testing, the TTY output storage section functions in much the same way as during normal operation except for a few minor variations in operations. As has been previously described, in the TTY test, the test word is not looped back to the test control circuits and to the 17-way AND circuit for zero test but is passed to a monitor where a visual comparison is made between the original test word and the processed test word.

When setting up the test word, the procedure followed is the same as that previously described for a G/A-FD, BOMARC, G/G, and G/A-TD word, except that, for a TTY test word, bit RS must always be a

1. The latter, preceding the test word, produces the start signal required to initiate the TTY monitor into operation. The remaining bits of the right drum word are selected to represent a particular TTY character.

The TTY storage section is selected for unit loop test purposes by means of selection bit switches located on the unit test door. When a computer under test is in a standby mode, its respective TTY channel relays are arranged in series, since they are not energized. In normal operation (outputs active), however, the TTY channel relays are energized, and their respective contacts are made to operate independently of other relay contacts.

At the beginning of test, a start-search pulse is applied to the test word generator. This initiates the read-in of the test word into the OB register and the automatic address register stepping of the test word in all addresses of the TTY core array. In addition, the start-search pulse is transferred and routed to inhibit the TTY burst counters.

During test, the test word data bits are read out of the storage array to the OSR under control of the 51-counter. In the OSR, the test data bits or test words are stored temporarily and subsequently shifted out under the control of the 51-counter to complement the output parity counter flip-flops. These flip-flops are used to sample the test word for errors. At the same time, the test data bits are routed to the conversion circuit, where they are applied to the set lines of the conversion circuit flip-flops. The output levels generated from these flip-flops are supplied to energize relays (VRD's) associated with each of the conversion flip-flops. These relays control the transfer of test data bits to their respective TTY channel lines. Thus, when a conversion flip-flop is complemented to the 1 side, its corresponding relay (VRD) will be energized to open the TTY channel line to produce a space signal (fig. 4–13). Conversely, when a flip-flop is caused to rest on its 0 side, its corresponding relay will close the TTY channel line, producing a mark signal. In this fashion, the binary-coded test word is made compatible with the input signal requirements (mark or space) required of the TTY monitor for proper operation.

As previously stated, when the automatic-address stepping mode is used during a TTY unit loop test operation, the TTY channel relay contacts are arranged in series order so that, whenever a channel relay is caused to open, all other channel relays will open. Similarly, when a channel relay is caused to be closed, all other channel relays will close. However, when the single-address stepping mode of operation is used, the individual channel relays are made to operate independently of each other.

CHAPTER 2
COMPUTER LOOP TEST

2.1 GENERAL

The computer loop test is a comprehensive check of the input and output circuits of the AN/FSQ-7 Combat Direction Central. It tests the operation of the Output System, Input System, Drum System, and various parts of the Central Computer System itself. During the test, the flow of information through the various elements of both the AN/FSQ-7 and AN/FSQ-8 Centrals closely approximates the information flow in the respective equipments when they are actually processing the air defense problem.

Basically, the test comprises two modes, each of which is separately tested. In one mode, the outputs of the G/A-FD, BOMARC, and G/A-TD storage sections are looped through the output test section to the long-range radar input (LRI) element. In the other mode, the output of the G/G storage section is looped through the test equipment section to the crosstell (XTL) input element. Figure 4–14 shows the two paths of information flow.

In both modes, the test information originates within the Central Computer System and is passed through the OB fields of the Drum System to the Output System. In the Output System, the test information may pass through either the G/A-FD, BOMARC, or G/A-TD storage section (whichever section is under test) to the test equipment section, and on to the LRI element of the Input System; from there it passes through the LRI field of the Drum System and back into the Central Computer System for comparison with the original test information. The other path is through the G/G storage and test equipment sections to the XTL element of the Input System, through the XTL field of the Drum System, and back to the Central Computer System.

2.1.1 Ground-to-Ground to XTL Loop

In the regular operation of AN/FSQ-7 Combat Direction Centrals, the output of the G/G storage section is transmitted over telephone line circuits to one of the adjacent AN/FSQ-7 Combat Direction Centrals. Information enters the adjacent equipment through the XTL input element. The manner in which the information is transmitted, therefore, is compatible with the operation of the XTL input element.

There are five G/G output channels. Each of these channels is capable of being included in the computer loop test, one at a time. Further, there may be several XTL input channels in the XTL input element. Only one such input channel may be used at one time in the computer loop test. Therefore, to conduct the test, it is necessary to select one G/G output channel and one XTL input channel. The test information is programmed to pass through the Output System and must reflect the channel selection in the address part of the information. The input and output channels are selected and switched automatically within the computer loop control (discussed in detail in 2.2.2). Since the information is already compatible, it is switched straight through the computer loop control without any modification. The test information is programmed within the Central Computer System.

2.1.2 G/A-FD, BOMARC, and G/A-TD to LRI Loop

In the normal operation of AN/FSQ-7 Combat Direction Centrals, the G/A-FD, BOMARC, and G/A-TD storage section outputs are forwarded to data link receivers via telephone transmission lines. Data information from each of the storage sections is routed over two output channels, and messages to each data-link receiver contain 234 data pulses.

The LRI element requires five 47-bit words, each word preceded by a specific sync pattern (00S00). (See fig. 4–15.) Thus, the LRI element must be provided with a total of 235 bits of information plus the sync pattern. The 235 bits represent one bit more (skip pulse) than the G/A-FD, BOMARC, or G/A-TD arrays can provide. Hence, an additional bit must be supplied which is always a 0. Paragraph 2.2 describes the circuitry involved in making a G/A-FD, BOMARC, or G/A-TD to LRI computer loop test or a G/G to XTL input loop test.

2.1.3 TTY Monitor Test

A computer loop test may be performed on the TTY storage section. However, there is no provision for feeding information from the Output System back to the Central Computer. Therefore, a TTY monitor such as is used in the TTY unit loop test is used in the TTY computer loop test.

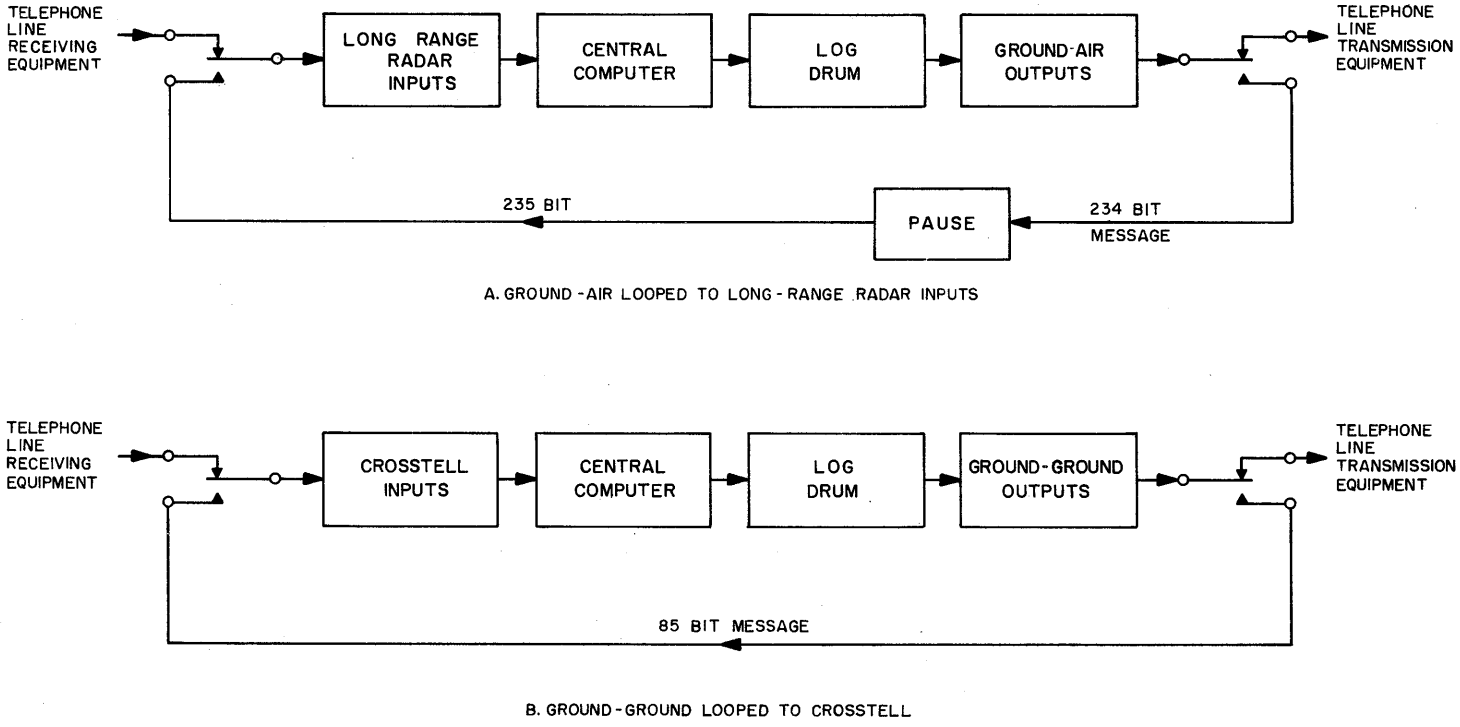


Figure 4–14. Computer Loop Test, Flow of Data, Simplified Block Diagram

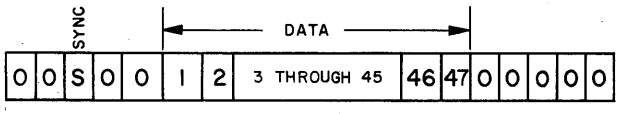


Figure 4–15. Long-Range Radar Input Message

2.2 COMPUTER LOOP CONTROL

2.2.1 G/A-FD, BOMARC, and G/A-TD to LRI Channel Selection

Channel selection of the various sections of the AN/FSQ-7 equipment during a computer loop test operation is effected by means of programming. Programs are generally written to route test data information over individual channels of selected sections in concurrent fashion, incurring no delay between the selection of the individual channels. This is in direct contrast to that method previously used in which switches were required to effect selection and consequently a program would be halted if it was desired to route test information over other channels.

The new method of section and channel selection is accomplished by means of the channel selection circuit shown in figure 4–16. It can be seen from the figure that a BTC pulse occurring at OD 1 time is obtained by selecting the burst time counters and reading 10_8 (octal) words. The select-section levels are obtained from the section decoder circuit, which determines which channels or sections will be selected to route the test data information. These levels are of 7.9-μsec duration and occur each time a word is read into the OB register.

To computer-loop-test G/A-FD channels 1 and 2 by means of programming, the following pre-operational test procedure must take place. The OUTPUTS TEST-OPERATE switch is operated to the TEST position. This applies —48V to the armature of K1 of circuit VRD 1. Next, the RESET flip-flops pushbutton is depressed. This action clears the LRI loop channel selection flip-flop (FF 1), de-energizing K1 and thus allowing —48V to be applied to the normally closed (NC) contact points of K1. The program is written so as to cause the burst time count to be selected and read twice, thus generating two step-channel (OD 1) pulses. This action is required to ensure that all the channel selection flip-flops are clear and that the auto loop inhibit flip-flop (FF 4) is set before a computer loop test of a particular section and its associated channels can take place.

With the generation of the first OD 1 pulse, FF 1 is complemented to its 1 side; the loop G/A-FD to LRI flip-flop (FF 2) is cleared, and FF 4 is set via the OR 1 circuit. In order that the conditions established in the preceding paragraph may be met, a second OD 1 pulse is programmed to complement FF 1 back to its clear side; FF 2 will remain cleared, and FF 4 will remain set, ending the pre-operational test procedure. A G/A-FD section and its associated channels can now be selected for computer loop test purposes.

When the first G/A-FD word is read into the OB register, a select-section-1 level is generated to condition GT 1. Flip-flop 4, having been set by an OD 1 pulse, generates a level to condition GT 3. Both GT's 1 and 3 are now conditioned to pass an OD 3 pulse to set FF 2. The OD 3 pulse is also returned via OR 2 to clear FF 4, deconditioning GT 3.

Flip-flop 2, having been set at OD 3 time, allows the —48V to be passed through the normally closed (NC) contact points of de-energized K1 of VRD 1 and to be subsequently fed to the normally open (NO) contact points of energized K2 in VRD 2. This relay voltage is then applied to energize the G/A-FD channel 1 computer loop test relay, enabling G/A-FD channel 1 test data to be looped to the LRI element, via the LRI test bus lines and the test pattern generator, to be returned to the Central Computer for comparison purposes.

If desired, the computer loop test program can be written to process the test information repeatedly over the same section and channel, another channel within that section, or proceed to select another section for test. On the other hand, if it is desired, say, to select channel 2 of the G/A-FD storage section, then the program is written so that once again the burst time counter is selected and then read. The BTC, having been read, generates at this time a step-channel selection (OD 1) pulse to complement FF 1 to its set side. The latter generates a level energizing K1 of VRD 1 and enabling —48V to be passed through its normally open (NO) contact points and applied to K3 of VRD 3.

This, in effect, removes the —48V relay voltage from VRD 2 and de-energizes the G/A-FD channel 1 computer loop test relay. In addition, the OD 1 pulse is applied to the 0 side of FF 2 and to the 1 side of FF 4. Flip-flop 2 will again be set upon receipt of the first section 1 drum word.

Flip-flop 2, being set, energizes K2 and de-energizes K3; thus, the —48V is passed through the normally closed contacts of K3 to energize the G/A-FD channel 2 computer loop test relay. Hence, the drum test word data is routed over the G/A-FD channel 2 lines and looped to the LRI element, via the LRI test bus lines and the test pattern generator, and returned to the Central Computer for comparison purposes.

It should be noted from the figure that G/G channels 1 and 2 are selected in coincidence with the selection of G/A-FD channels 1 and 2. However, this does not contribute any adverse effects on the G/A-FD channel selection operation since the G/G test data informa-

tion is looped to the XTL element, whereas the G/A-FD is looped to the LRI element.

2.2.2 G/G to XTL Channel Selection

The procedure used for computer-loop-testing the G/G storage section and its associated channels is the same as that described in the previous paragraph for the G/A-FD, BOMARC, and G/A-TD storage sections. As shown in figure 4–16, the VRD 2 circuit must be energized if it is desired to select a G/A-FD channel 1 or G/G channel 1 line for test. This circuit is energized only when a select-section-1 level is present and when FF 2 is in set status. It is apparent, therefore, that, when selection of a G/G channel 1 line is required, it is necessary that, initially, the first word received from the OB drum be made to contain a G/A-FD section number. In all other cases, a select-section-5 or select-section-2 level is required initially to effect selection of the remaining G/G channels.

Using this method of selection, it is possible to check the G/A-FD channel 1 line and then, without changing the status of the selection circuit, go on to check the G/G channel 1 line. The two checks may be performed alternately or simultaneously.

2.2.3 Stop to Drums

When the STOP TO DRUMS switch is activated, K2 is energized (fig. 4–17). This sends a —30V level as a non-reset-on-error signal and a +10V level as a stop-to-drum signal level to the alarm control section. The —30V non-reset-on-error signal causes the contents of the flip-flop register of the output drum section to be

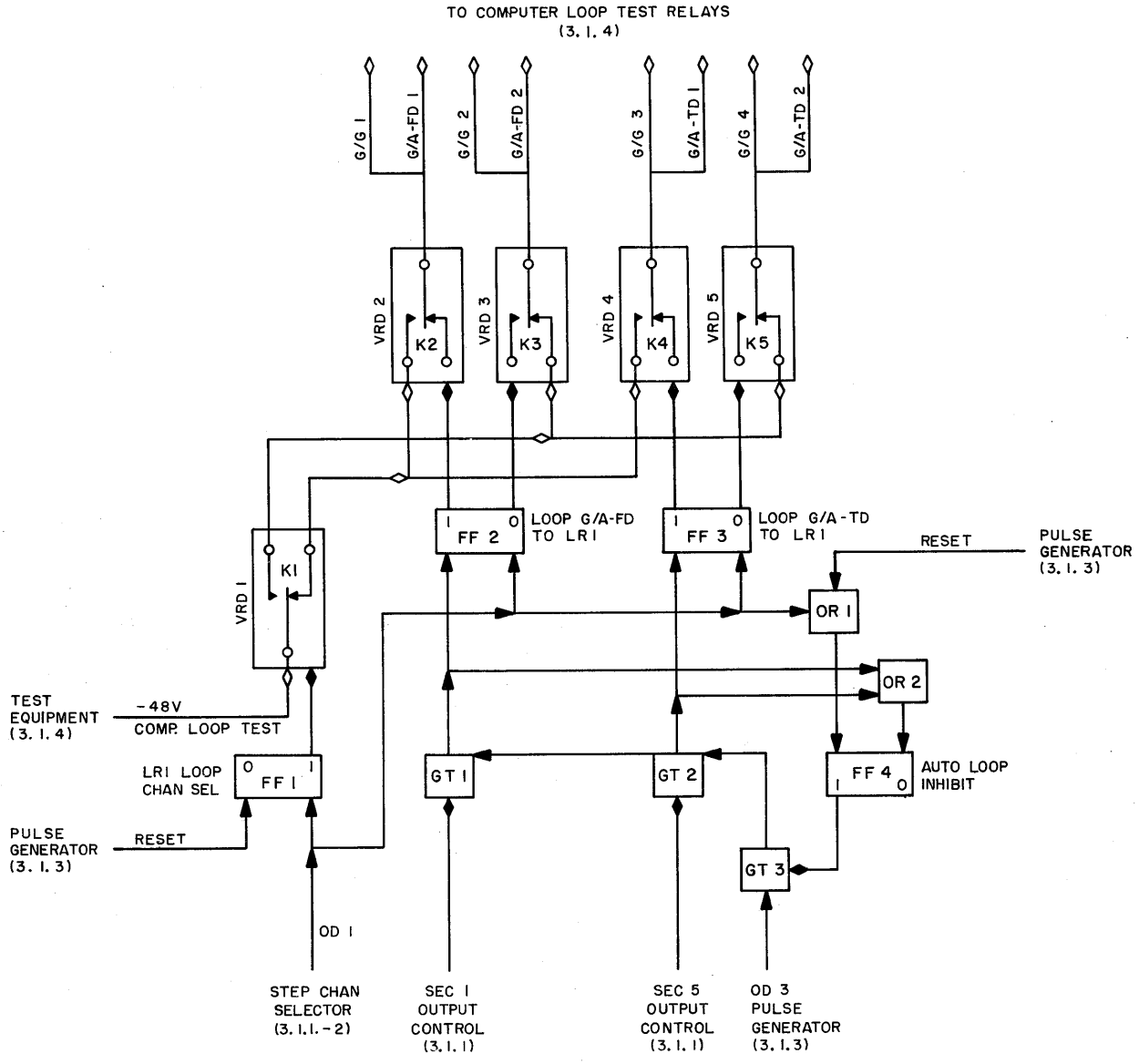


Figure 4–16. Computer Loop Test Channel Selection Circuit (3.1.4), Simplified Logic Diagram

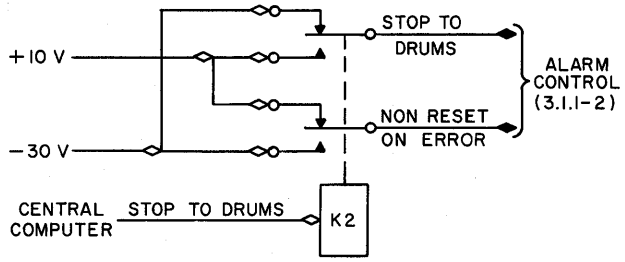


Figure 4–17. Stop-to-Drums Circuit (3.1.4), Simplified Logic Diagram

retained for inspection if a parity-NG, an illegal register, or section address alarm is produced (fig. 2–44). The stop-to-drums pulse is passed to the Drum System if either of the previously mentioned errors occurs. It stops the Drum System and prevents the erasure of the test word so that the error can be examined.

2.2.4 Restart-to-Drums Circuit

When the OUTPUTS TEST-OPERATE switch is moved to the OPERATE position, the falling of the test-outputs signal generates a pulse in the restart-to-drums circuit (fig. 4–18). This pulse sets the synchronizing restart-to-drums-sync flip-flop. The restart-to-drums flip-flop is set at the following OD 3 time; at OD 1 time, the restart pulse is generated. The restart pulse is carried to the Drum System and to the parity generator of the output control element. This pulse is used in the Drum System to re-enable the transfer of the information from the OB drum to the Output System. In the output control element, the pulse causes a compare signal to be sent to the Drum System for 100 ms but prevents any words from being accepted during this interval. This prevents any stale information in the drums from being transferred and causes such information to be erased from all three OB drum fields. The outputs-active signal, which arrives when a system is changed from standby to in-use, has the same effect as the test-output signal.

2.2.5 Pause-and-Sync-Control Circuit

In the G/A-FD and BOMARC to LRI loops, the data from these sections is modified by the pause control circuit. Referring to figure 4–19, assume that the 13-counter and the 25-counter are both primed at 1. The 13-counter is shifted at a 1,300-cycle rate by OD 2–13 pulses. (Refer to Part 3.) At 13-counter-11 time, a sync pulse is generated. At 13-counter-12 time and 13-counter-13 time, there are no sync and data pulses; therefore, 0 bits are produced, producing in effect the required 00S00 sync pattern.

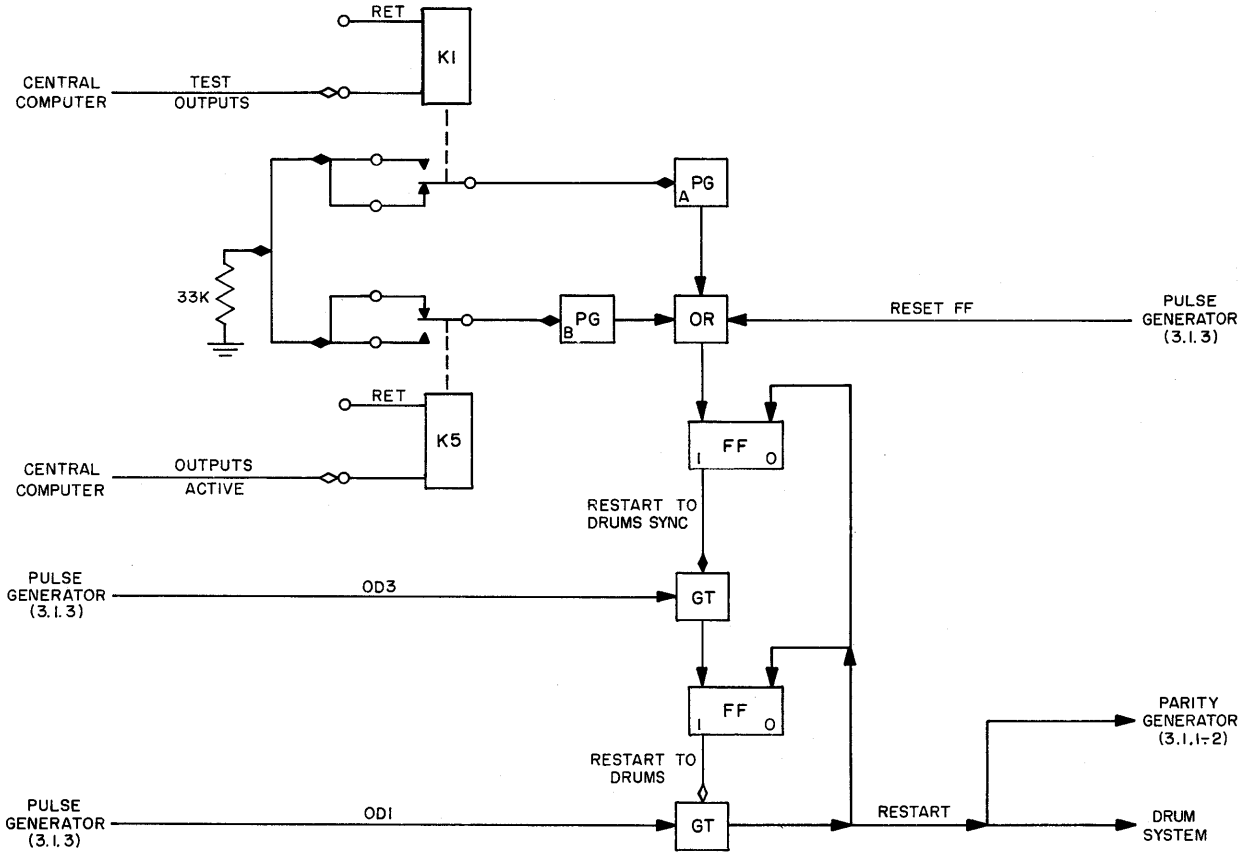


Figure 4–18. Restart-to-Drums Circuit (3.1.1-2), Simplified Logic Diagram

At 13-counter-13 time, the 25-counter is shifted; at 25-counter-1 time, an OD 4–13 pulse is generated to fire the thyratron CSD's of the respective storage sections, shifting a column of information bits into the 13-bit output shift registers (OSR's). At the next OD 3–13 time, the first bit in the OSR (not shown in the diagram) is gated out to the conversion equipment and then on to the test bus. Each succeeding 13-counter pulse shifts another bit out of the OSR. When the OSR is emptied, another column is shifted from the array to the OSR. This cycle is continuous during nonsearch time. At 13-counter-8 time, a pulse shifts the 47th bit, indicating that a word has been sent, and also turns on the pause flip-flop. This inhibits the 13-counter shift pulse generator. Two successive OD 3–13 pulses step the test sync generator, and the third OD 3–13 pulse produces a test sync pulse. The OD 2–13 pulse following the next OD 3–13 pulse resets the test sync generator and turns off the pause flip-flop.

The next OD 3–13 pulse completes the required sync pattern (00S00), and the 13-counter begins shifting again. Four additional words are sent in like manner. Eventually, the last data bit of the fifth and last word is shifted from the array. However, an additional bit is needed to complete the LRI requirements of 47 bits per word. The 25-counter-19 pulse, occurring at OD 4 time, turns on the pause flip-flop and sets the test sync generator. The next OD 3–13 pulse produces the extra bit (skip pulse), a 0.

2.2.6 13-Core Delay Counter

In general, a G/A-TD test message is composed of 39 timing pulses; 34 of these represent G/A-TD data, and the remainder constitute the sync pattern (00S00) which precedes each G/A-TD test message (2 words). Since each LRI message requires a total of 52 timing pulses, including the sync pattern, the transmitted G/A-TD test data must be modified. The latter, when modified, is then compatible with the requirements of the LRI input element.

Modification of G/A-TD messages during a G/A-TD to LRI computer loop test is accomplished by the 13-core delay counter circuit (see fig. 4–20). During the delay initiated by the 13-core delay counter, the shifting of the 17-counter is inhibited by the 13-core delay counter, thus preventing the readout of any G/A-TD data and thereby allowing 13 timing pulses to be transmitted without any data being transmitted on the data lines. These 13 timing pulses, when added to the 39 data pulses of the G/A-TD test message, make the message compatible with the LRI input equipment requirement of 52 timing bits per message. A detailed discussion of the operation of the 13-core delay counter circuit follows.

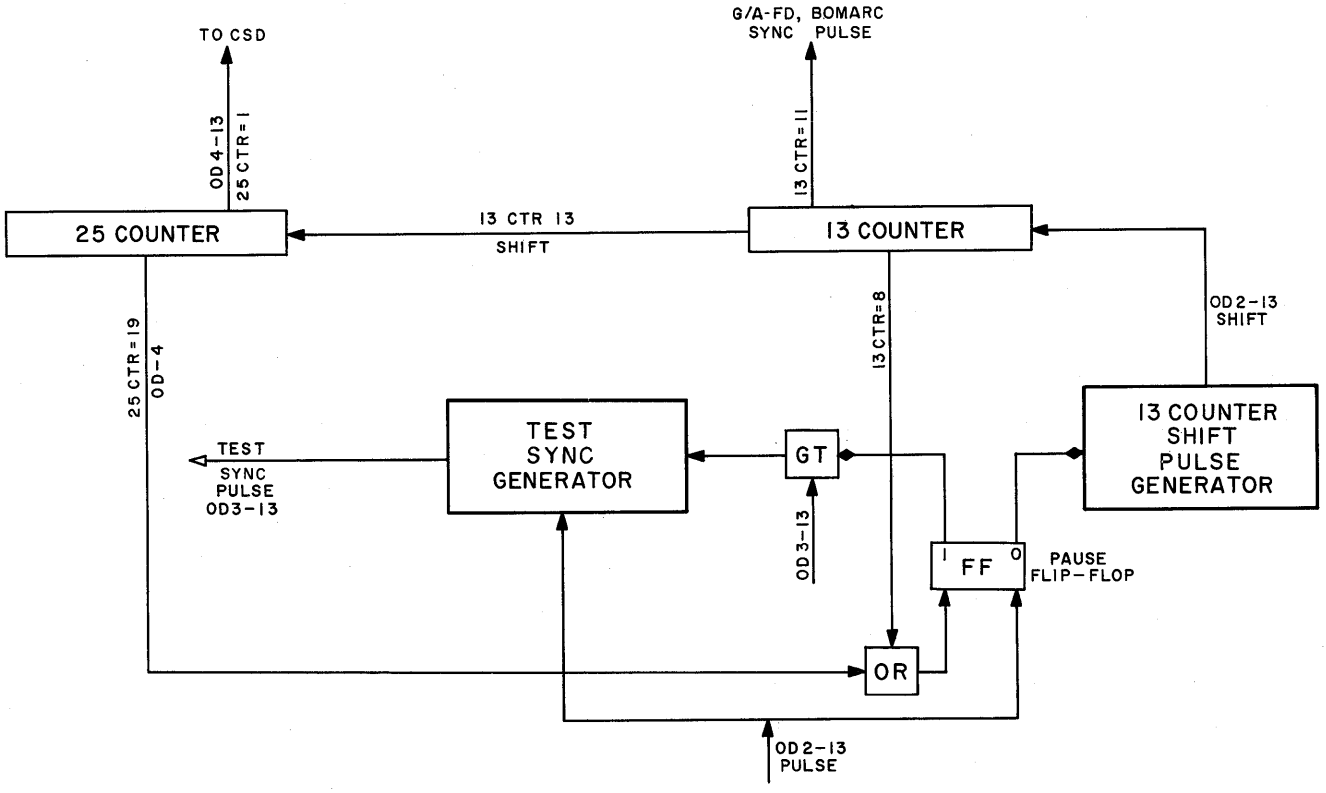


Figure 4–19. Pause-and-Sync-Control Circuit (3.1.4), Simplified Block Diagram

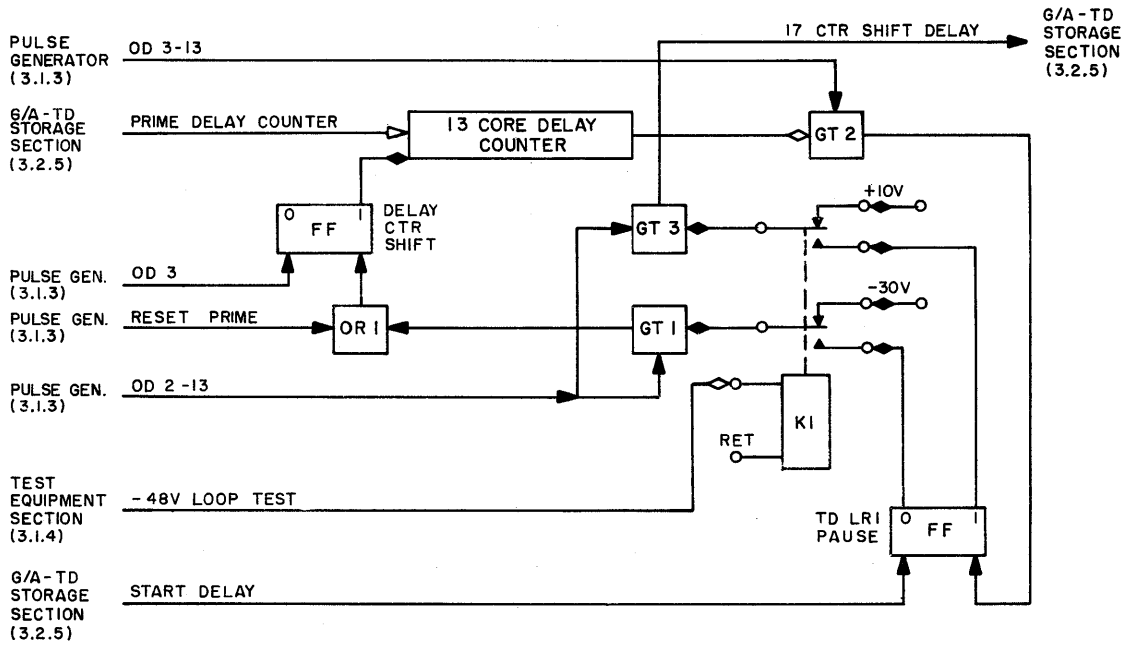


Figure 4–20. G/A-TD 13-Core Delay Counter (3.2.5), Simplified Logic Diagram

Assume that a G/A-TD test message consisting of four 17-data bit words has been read out of the OSR's (two words per channel) preceded by their sync pattern 00S00. At this time, the following conditions will be evident:

a. The 17-counter fast-shift flip-flop is cleared.

b. The 15-counter is shifted to 15-counter-5 time.

c. The 17-counter is being reset and primed.

At 15-counter-5 time, an OD 4 pulse is gated to set the sync generator flip-flop, the 17-counter shift flip-flop, and the 17-counter sync flip-flop preparatory to the readout of G/A-TD message slot 2. With the setting of the 17-counter sync flip-flop, a level is generated to condition a gate which is strobed by an OD 3 pulse. The conditioned gate passes the OD 3 pulse, which in turn is used to perform the following:

a. Set the 17-counter prime flip-flop

b. Clear the TD LRI pause flip-flop

c. Clear the 17-counter sync flip-flop

The 17-counter prime flip-flop, when set by the gated OD 3 pulse, generates a level to prime the 13th core of the 17-counter (see fig. 3–55), readying the 17-counter for sync pattern generation. This level is also used to prime the first core of the 13-core delay counter, alerting this counter for the 13 timing pulse delay required to modify the G/A-TD test message.

The operations depicted above are applicable only during a G/A-TD computer loop test operation. When the OUTPUTS TEST-OPERATE switch is set to the OPERATE position, K1 (shown in fig. 4–19) will become energized. The same OD 3 pulse that sets the 17-counter prime flip-flop is also used to clear the TD LRI pause flip-flop. The TD LRI pause flip-flop, when cleared, generates a level through the closed contact points of K1 to condition GT 1. At the same time, a −30V level emanating from the set side of the flip-flop is applied to decondition GT 3. Deconditioning GT 3 prevents the shifting of the 17-counter during the delay. Conditioned GT 1 will pass an OD 2–13 pulse to set the delay counter shift flip-flop via the OR 1 circuit. This flip-flop is cleared by OD 3 pulses; hence, this flip-flop generates 2.5-μsec shift pulses, which are used to shift the 13-core delay counter.

Coincident with the shifting of the 1 bit in the 13-core delay counter by the delay counter shift flip-flop, a timing pulse is passed to the LRI element. Therefore, at the completion of the operational cycle for the 13-core delay counter, 13 timing pulses will have been passed to the LRI element. At the same time, GT 2 is conditioned to pass an OD 3–13 pulse which is used to set the TD LRI pause flip-flop. When the latter is set, GT 1 is deconditioned, preventing the shifting of the 13-core delay counter. In addition, GT 3 is conditioned to pass OD 2–13 pulses, which are subsequently used to shift the 17-counter. Shifting the 17-counter initiates the generation of the sync pattern for the following test message.

It can be seen, therefore, that each time a G/A-TD message comprising 39 data pulses is transmitted to the LRI input equipment a 13 timing pulse delay is executed by the 13-core delay counter circuit. As a result, the G/A-TD test message is modified to conform to the 52 timing pulses needed for an LRI message.

PART 5
AN/FSQ-8 COMBAT CONTROL CENTRAL

CHAPTER 1
INTRODUCTION

1.1 GENERAL

This section of the manual contains pertinent information relative to the function and operation of an AN/FSQ-8 Combat Control Central in the SAGE System. Since, in a functional (tactical) sense, a Combat Control Center occupies a higher station in the command echelon of the SAGE System than that held by a Combat Direction Center, it is axiomatic that the equipment utilization of a Control Central also differs from that of a Direction Central.

Basically, the equipment complex of an AN/FSQ-8 Combat Control Central is similar to that employed in an AN/FSQ-7 Combat Direction Central, with a few exceptions. The main exception is that a Control Central has no facilities for communicating directly with manned or unmanned interceptors. Consequently, ground-to-air (G/A) output facilities (required in a Direction Central) are not required in a Combat Control Central. Specifically, the G/A facilities not utilized in a Control Central are the G/A-FD, BOMARC 1, BOMARC 2, and the G/A-TD storage sections.

The facilities utilized in the Output System of a Control Central are the ground-to-ground (G/G) and the teletype (TTY) storage sections. The operation of these two storage sections, including the differences (circuit or operational) between them and their Combat Direction Central counterparts, is discussed in the ensuing paragraphs.

1.2 OUTPUT SYSTEM IN AN/FSQ-8 COMBAT CONTROL CENTRAL

The computer that is utilized in a Combat Control Central is a modified version of the AN/FSQ-7 Computer. As shown in figure 5–1, the Output System in an AN/FSQ-8 Central comprises the G/G and TTY storage sections. These storage sections operate in a manner similar to that described for their Direction Central counterparts, but for a few exceptions. Therefore, for purposes of brevity, it is necessary to discuss in this part of the manual only those exigencies which reflect circuit or operational differences between the AN/FSQ-7 and AN/FSQ-8 Output Systems.

Using the operation of the Output System in an AN/FSQ-7 Combat Direction Central (described in previous parts of this manual) as a reference basis, difference data reflecting the operation of the Output System in an AN/FSQ-8 Combat Control Central is presented in Chapter 2 of this part.

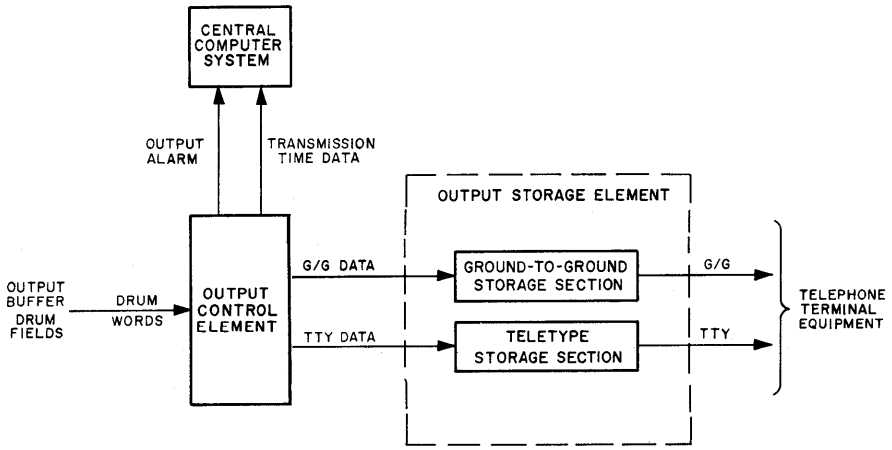


Figure 5–1. Output System, Block Diagram

CHAPTER 2
DIFFERENCE DATA

2.1 DESCRIPTION

The difference data presented in this chapter has reference to the departures from the circuit and functional operation which normally complements an AN/FSQ-7 Combat Direction Central and used exclusively in an AN/FSQ-8 Combat Control Central.

Except for the differences mentioned herein, the operation of the Output System in a Direction Central, as described in the preceding parts of this manual, is also pertinent to the Output System in a Control Central. Hence, when applicable, all references relating to AN/FSQ-8 Output System operation should be directed to that information contained in Parts 1, 2, and 3 of this manual, which are concerned with the operation of the Output System in a Direction Central.

2.2 CIRCUIT DIFFERENCES, OUTPUT CONTROL ELEMENT

The operation of the output control element, as discussed in Part 2 of this manual, is also applicable to the AN/FSQ-8 output control element. However, all references to the G/A-FD, BOMARC 1, BOMARC 2, and the G/A-TD mentioned in this part should be disregarded. Circuit differences evident in the discussion of the output control element (AN/FSQ-7) and common to the AN/FSQ-8 output control element are discussed in the following paragraphs.

2.2.1 Flip-Flop Register Clearing

The temporary storage period of the flip-flop register is controlled by the flip-flop-clear (reset) pulse generated in the driver section of the parity register and drivers. The controlling factors for the application of the clear pulse are shown in figure 5–2. The clear pulse is a gated OD 4 timing pulse passed through a 0.4-μsec delay circuit. The clear pulse is then applied through separate lines to the left drum and parity registers and the right drum word register. The clear time is thus established at OD 4 + 0.4 μsec.

The drum word is received from the OB field at OD 1 time plus the delay introduced by the connecting cable. The cable delay depends on the length of cable used and may be as great as 0.5 μsec.

Since OD 4 is 7.5 μsec after OD 1 (2.5 x 3), OD 4 + 0.4 occurs approximately 8.0 μsec after the time that the drum word is received. Hence the flip-flop register is cleared approximately 8.0 μsec after it is set by the drum word.

The application of the clear pulse is a function of the presence of the not-error-signal level at the gate. This pulse is always present during normal operations and is removed only for testing purposes.

The inhibit-reset signal from the unit loop control circuit (a test function) energizes a relay, causing the normally closed contacts to open. This action prevents the right drum word register from being clear but has no effect on the passage of the left-drum-word-register-clear pulse.

To summarize, the registers are always cleared 8.0 μsec after a word is entered into the registers during normal operations. Only during test operations is it possible for the drum word to remain in the registers longer than this period. Thus, during testing, a drum word may be retained for longer than the normal time interval when test operations require this condition.

The OD 4 reset pulse, shown in figure 5–2, is gated into the read-in control circuit when a word is missed. It then becomes a nonsearch signal to the output alarm section and the Central Computer. The OD 4 pulse is used since it occurs at a time sufficiently later than the time of entrance of the word (OD 1) to permit complete examination of the word.

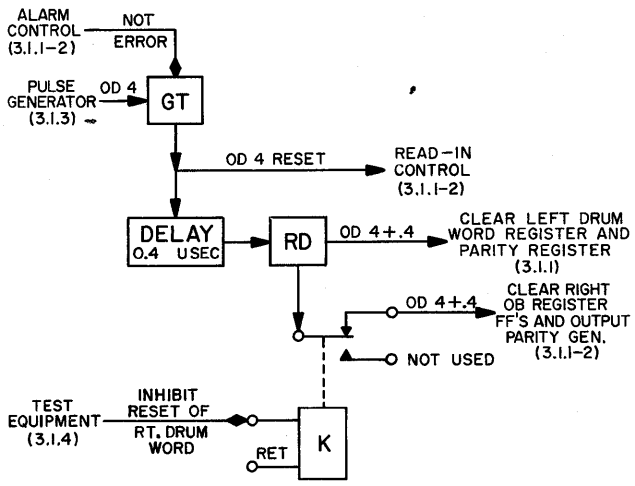


Figure 5–2. Flip-Flop Register Clear Control (3.1.1), Simplified Logic Diagram

2.2.2 Output-Word Parity Generator

Since the drum word does not remain intact beyond the output control element, the drum-word parity bit cannot be used for further parity checking. Therefore, a new parity bit is generated, added to the right drum word, and transmitted with it to the telephone receiving terminals. This permits another parity check to be conducted at that point (i.e., at the terminals) for detection of possible telephone channel errors. Unlike drum-word parity, the output parity bit is even; that is, the total number of 1's in a correct output word, including the output parity bit, is even.

The parity gates used to test drum-word parity are also instrumental in generating the output parity bit. The output-word parity generator flip-flop, shown in figure 5–3, is initially cleared by the flip-flop register clear control and is therefore set with the 0 side up before the new word is entered into the flip-flop register. The output word parity generator is then set with the 1 side up only if the new right drum word produces the odd-parity pulse shown in figure 5–3. This pulse comes from the odd line of the parity gates associated with the RS bit of the right drum word. Hence, the pulse comes only if there is an odd total of 1's in the right drum word. It follows that an output word parity bit is generated whenever the right drum word is of odd parity. The output word parity bit, when added to the output word through the STD's, makes the total number of 1's even. If the right drum word has an even total of 1's, there is no pulse to the 1 side of the flip-flop. Hence, the flip-flop remains with the 0 side up and there is no parity bit added to the right drum word. Since, in this case, the right drum word must have originally had an even total of 1's, it still has an even total of 1's.

2.3 CIRCUIT DIFFERENCES, OUTPUT STORAGE ELEMENT

The operation of the output storage, as discussed in Part 3 of this manual, is also applicable to the AN/FSQ-8 output storage element. However, all references to the G/A-FD, BOMARC 1, BOMARC 2, and the G/A-TD mentioned in this part should be disregarded.

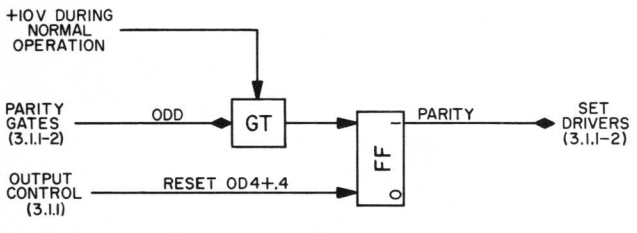


Figure 5–3. Output Parity Generator (3.1.1-2), Simplified Logic Diagram

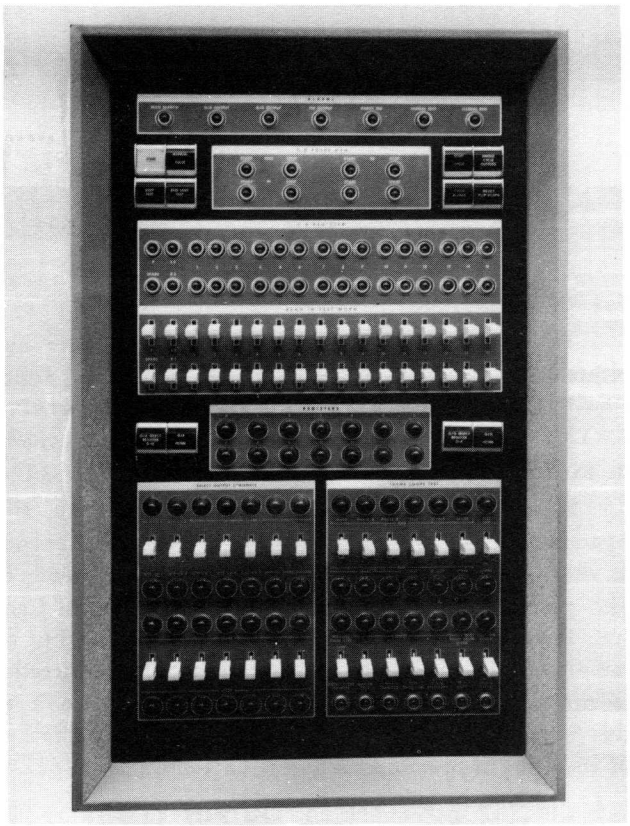


Figure 5–4. Test Control Panel, Unit 42

2.4 CIRCUIT DIFFERENCES, TEST EQUIPMENT SECTION

The operation of the test equipment section in the AN/FSQ-8 Output System differs greatly from that of its AN/FSQ-7 counterpart, discussed in Part 4 of this manual. This difference is attributable to the variance in circuit applicability or function and the test procedural methods used to perform test functions (unit loop or computer loop tests) on the AN/FSQ-8 Output System. A discussion of the operation of the test equipment section in an AN/FSQ-8 Output System is presented in the following paragraphs.

2.5 INTRODUCTION, TEST EQUIPMENT SECTION

The output test equipment section is incorporated in the output control element of the Output System for the purpose of testing the circuit functioning and the logical operation of the Output System. The test equipment consists of switches, relays, and logic circuits. Also, certain of the neons and indicator lamps of the output alarm section operate with the output test equipment section. The various switches, neons, and lamps are located on the Output System test panel, which is mounted on the back of unit 42. (See fig. 5–4.)

Two basic types of tests are provided by the test equipment: the unit loop test and the computer loop

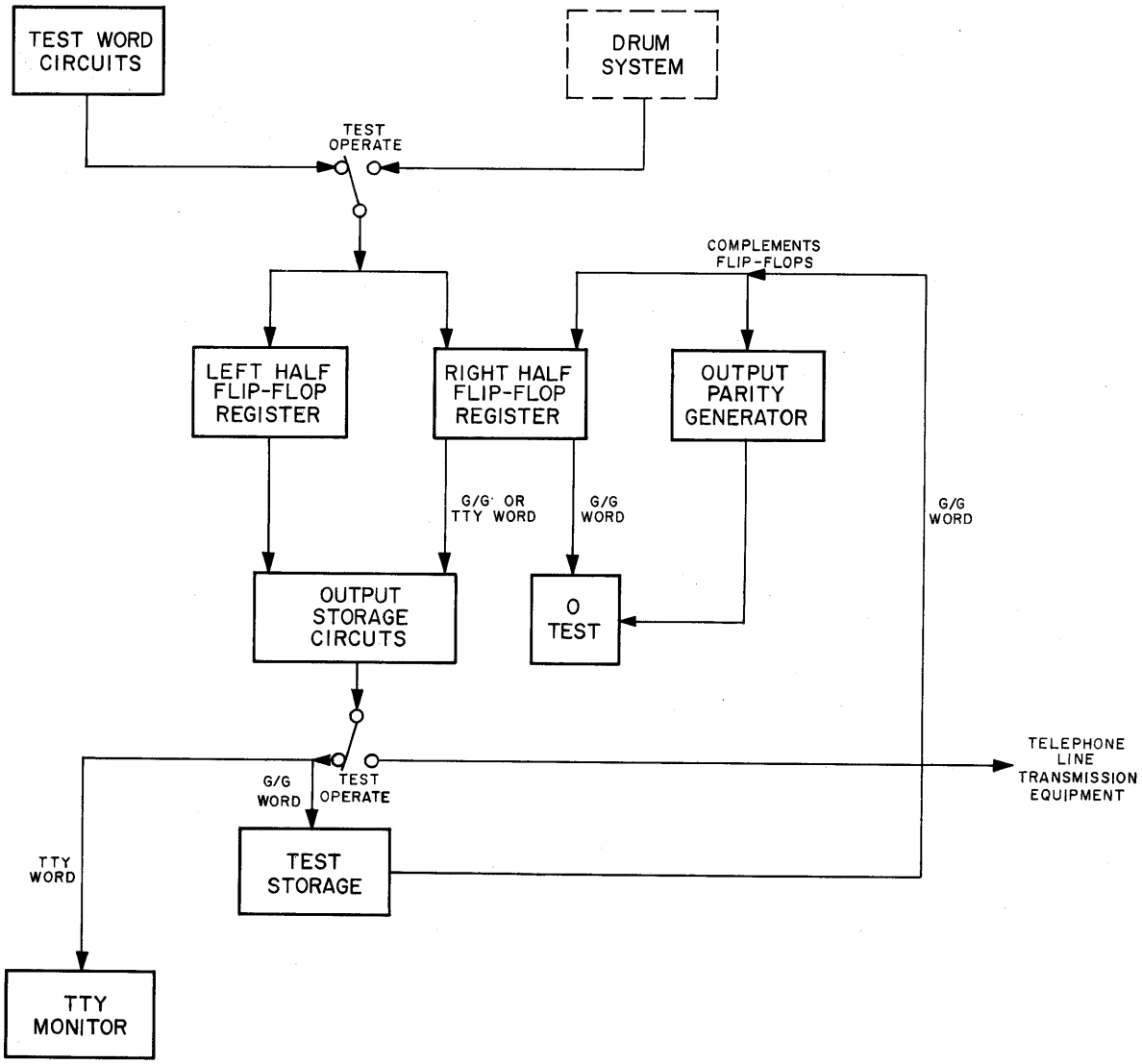


Figure 5–5. Unit Loop Test Data Flow, Block Diagram

test. Each loop test involves the feedback of test information to its origin, where a comparison is made to ascertain whether the test information was correctly transmitted. The unit loop test is performed manually by means of switches, whereas the computer loop test is programmed and is therefore performed automatically. The unit loop test checks the operation of the various individual sections of the Output System while the system is isolated from the remainder of the Combat Control Central. The computer loop tests provide a means of checking the Output System in conjunction with a large portion of the Combat Control Central.

2.6 UNIT LOOP TEST

2.6.1 General

In the unit loop test, the Output System is isolated from the Drum System, and a test word is then inserted manually by means of switches. The test word is processed in the normal manner by the output control element. If the conditions for its acceptance have been fulfilled (parity OK, burst number compares, no illegal addresses, and search time up), the word is transferred in the normal manner to the selected storage section in the output storage element. The word is then processed through this element. For the G/G storage section, the output data (right drum word) is looped back into the output control element flip-flop register, where the word was originally entered. If the transfer of the word was successful, the flip-flop register will be cleared. If the transfer was unsuccessful, one or more of the output alarm section flip-flop register neons will be illuminated. (See fig. 5–5.) Besides this visual representation, the test equipment section indicates an error in one of several other ways described in 2.6.2.10.

For the TTY storage section, the output word is recorded on a TTY monitor. This data is then visually compared with the test contents of the flip-flop register to determine whether an error has occurred.

The unit loop test procedure may be divided into three basic circuit groupings: unit loop control, unit loop storage, and specific unit loop tests. The unit loop control circuits control the general flow of the test word through the output control element and output storage element and provide the processing operations for detecting an error. The unit loop storage circuits provide for the storage of the test word in the test equipment section. The unit loop test circuits control the specific test operations in the storage section of the output storage element during testing operations.

2.6.2 Unit Loop Control, Error Detection

The general process of error detection involves the manual setting in of a test word in the flip-flop registers and the processing of this word to determine whether any errors occur. The test word is processed through the output control element in the normal manner and transferred to the output storage section. From there, a G/G word goes to the unit loop control circuits. A TTY word, on the other hand, is sent not to the unit loop control circuits but to a TTY monitor.

2.6.2.1 Unit Loop Test Switching

The operation of the Output System during testing is controlled by relays, which are in turn controlled by switches. These switches are located on the panel on the test doors on the back of the output control unit.

Any kind of a test on the Output System disables it, thereby disabling the operation of the entire Central. Therefore, an interlock (controlled at the maintenance console) is necessary to prevent inadvertently starting a test during the processing of an air defense problem. This interlock is accomplished by switching the relay voltage supply for the test equipment section at the maintenance console. Thus, the OPERATE-TEST switch on the maintenance console sends a computer-test signal to the unit-loop-on-test circuit of the unit loop control. (See fig. 5–6.) This signal controls the relay voltage supply for the output test equipment section and is

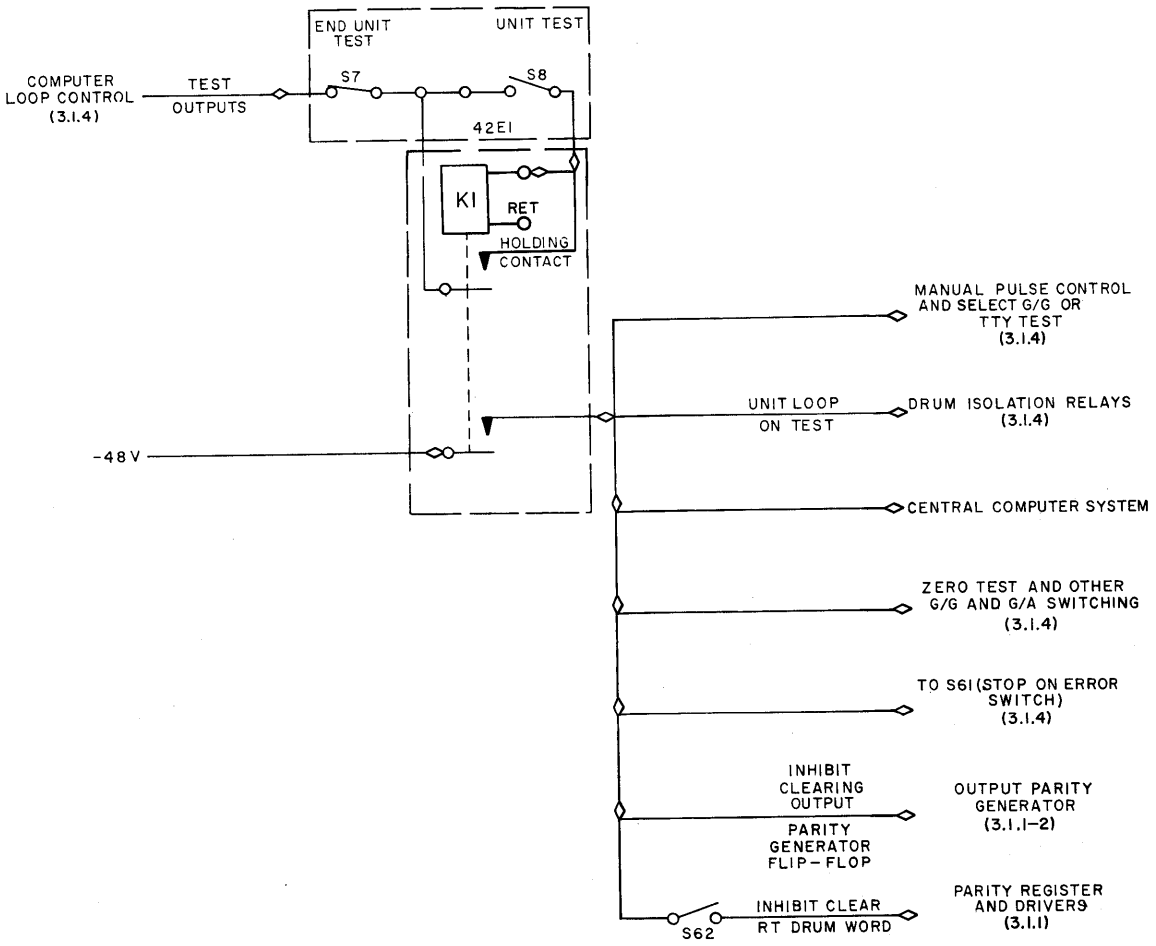


Figure 5–6. Unit-Loop-on-Test Test Circuit (3.1.4), Simplified Logic Diagram

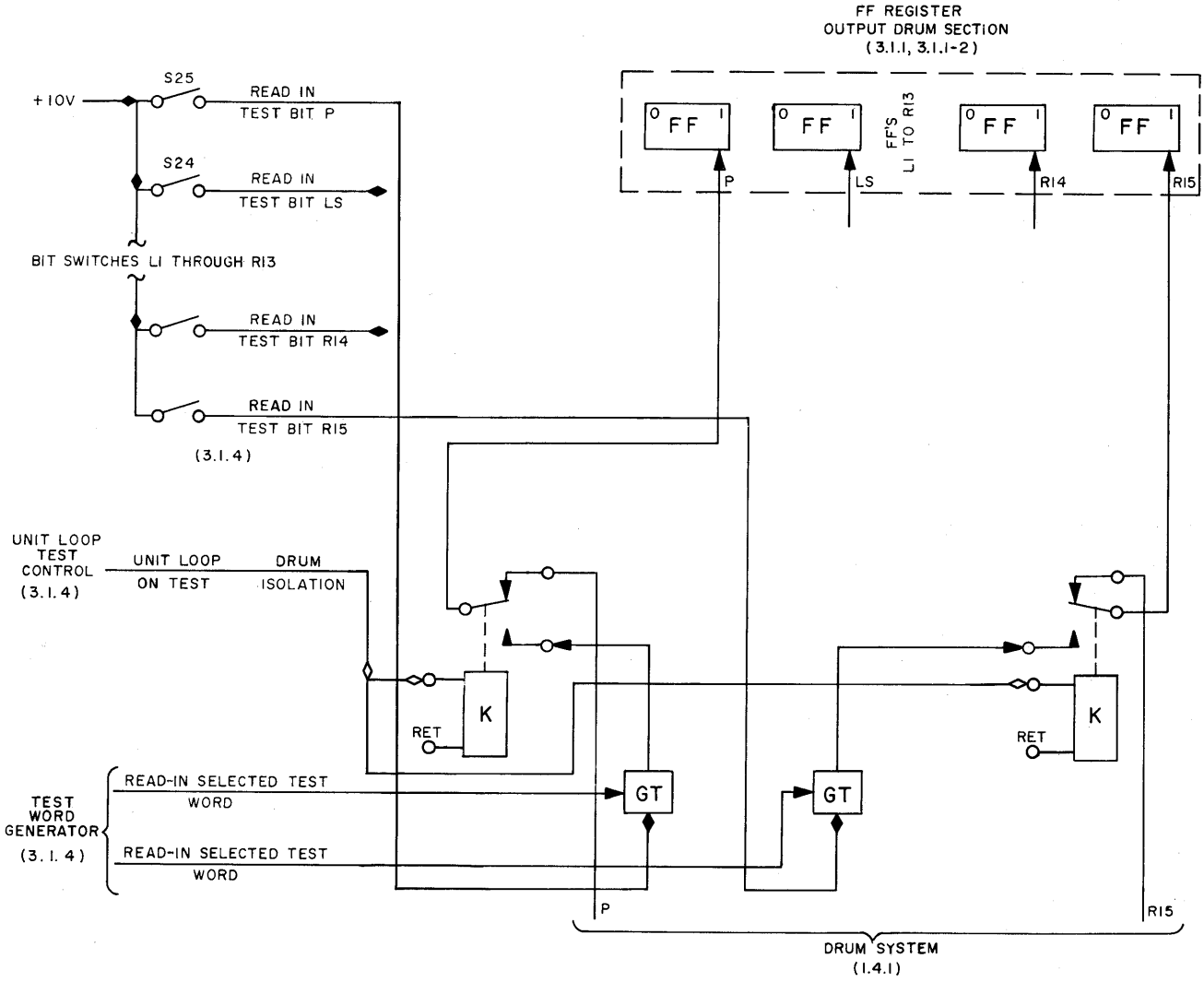


Figure 5–7. Drum Isolation and Test-Bit Circuit (3.1.4), Simplified Logic Diagram

sent via the computer loop control circuits since a computer loop test takes precedence over a unit loop test. Hence, control over whether a unit loop test can take place depends upon whether a computer loop test is in progress.

A UNIT TEST pushbutton (S8, fig. 5–6) in the test equipment section causes a holding relay to close, which controls the output test relay voltage (the output-on-test signal) of the test circuits. The END UNIT TEST pushbutton (S7) breaks the voltage to the holding relay at the end of the test operation.

2.6.2.2 Drum Isolation and Test-Bit Circuits

To set in a test word, the flip-flop register of the output control element must be isolated from the Drum System. After this is done, the test word can be set into the flip-flop register.

As shown in figure 5–7, the unit loop test circuit supplies the relay voltage to 33 relays, each of which opens one of the 33-bit lines from the Drum System, thus isolating the flip-flop register from the Drum System.

The test word generator of the output test equipment (see 2.6.3) provides a standard test-word pulse equivalent to a 1 bit to each of 33 gates. Each gate is connected to a read-in test-word switch corresponding to each of the 33 bits which make up a word. When a switch is closed, a +10V level conditions the corresponding gate which passes the test-word pulse. This sets the 1 side of the corresponding flip-flop in the flip-flop register up. Therefore, by closing the appropriate switches, 1's are read in to make up a drum word. (It follows, of course, that the flip-flops associated with the read-in test-word switches left open are set with the 0 side up.)

When setting in a test word for G/G, the right drum word (bits RS through R15) may be set to any de-

sired combination of 1's and 0's. For TTY, the restrictions explained in 2.6.5.2 must be considered. The burst number, bits L8 through L15, must be all 0's since the burst counters in the output storage element are inhibited. The desired register address in the array of the selected section, designated by bits L3 through L7, is set according to the register address code; the desired section address, designated by bits LS through L, is set according to the section address code. Care must be taken not to set in an unassigned section or register. The parity bit, P, must reflect a manual parity count of the 32 other bits so as to produce odd parity for all 33 bits.

2.6.2.3 Inhibit Resetting of Right Drum Word

Under normal operation, the parity drivers of the output control element clear the flip-flop register 8 μsec after the word is entered. However, during test operations, the right drum word should remain in the flip-flop register until it is complemented by the completely processed, looped-back word for G/G tests, or visually compared with the TTY monitor for TTY tests.

The clearing of right drum word registers is prevented by closing INHIBIT RESET RIGHT DRUM WORD switch S62. This transfers the —48V relay level passed by the unit test relay (K1, fig. 5–6) to the relay in the parity register and drivers (fig. 5–2) that controls the application of the clear pulse. The opening of this latter relay prevents the clear pulse from being passed to the right drum word flip-flops and also the output parity generator flip-flops (fig. 5–3). The clearing of the left drum word and input parity bit is not prevented since only the message portion of the drum word (right drum word) and the output parity bit arrive at the output of the output storage element. Therefore, only this (the right) portion of the drum word is looped back to the flip-flop register for comparison purposes.

2.6.2.4 Clearing Alarms and Resetting Flip-Flops

Before the test operation is begun, all alarms and flip-flops in the Output System should be cleared by depressing the CLEAR ALARMS and RESET FLIP-FLOPS switches (S5 and S6). This action grounds the pulse generators in the pulse distributor circuits of the output computer section. Clear pulses now pass to the appropriate circuit.

2.6.2.5 Test Start Control

Before a unit loop test is started, the previous basic switch settings must be made. Then the specific switch settings described in 2.6.5 must be made, depending upon the storage section (G/G or TTY) selected. Also, as described in 2.6.2.10, the method of error detection is selected. If the STOP ON ERROR switch is engaged, the test should be started by depressing START CYCLE pushbutton S2. As shown in figure 5–8, this action grounds the pulse generator, which produces a pulse to clear the single-cycle output flip-flop and the master stop flip-flop. This latter flip-flop produces an enable OD level, which then causes the various OD pulses to be distributed by the output computer section. This action sets the circuits into operation. Also, the start pulse is sent to the 1,300-pps generator to clear its flip-flop at the start of the test.

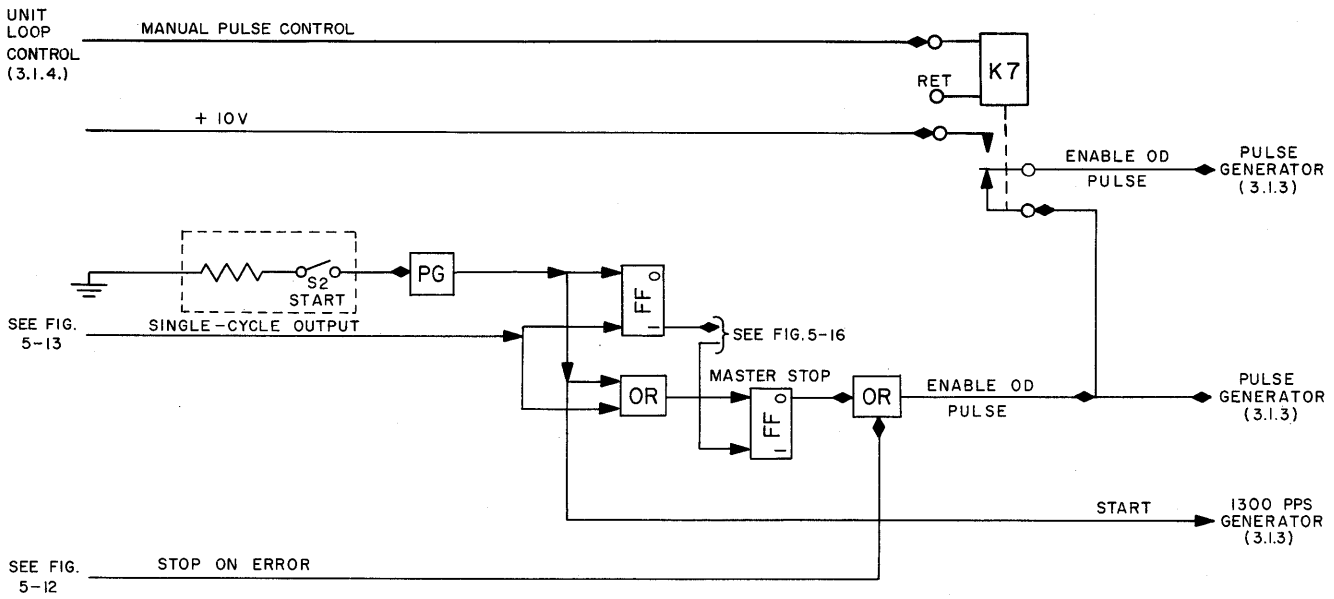


Figure 5–8. Test Start Control Circuit (3.1.4), Simplified Logic Diagram

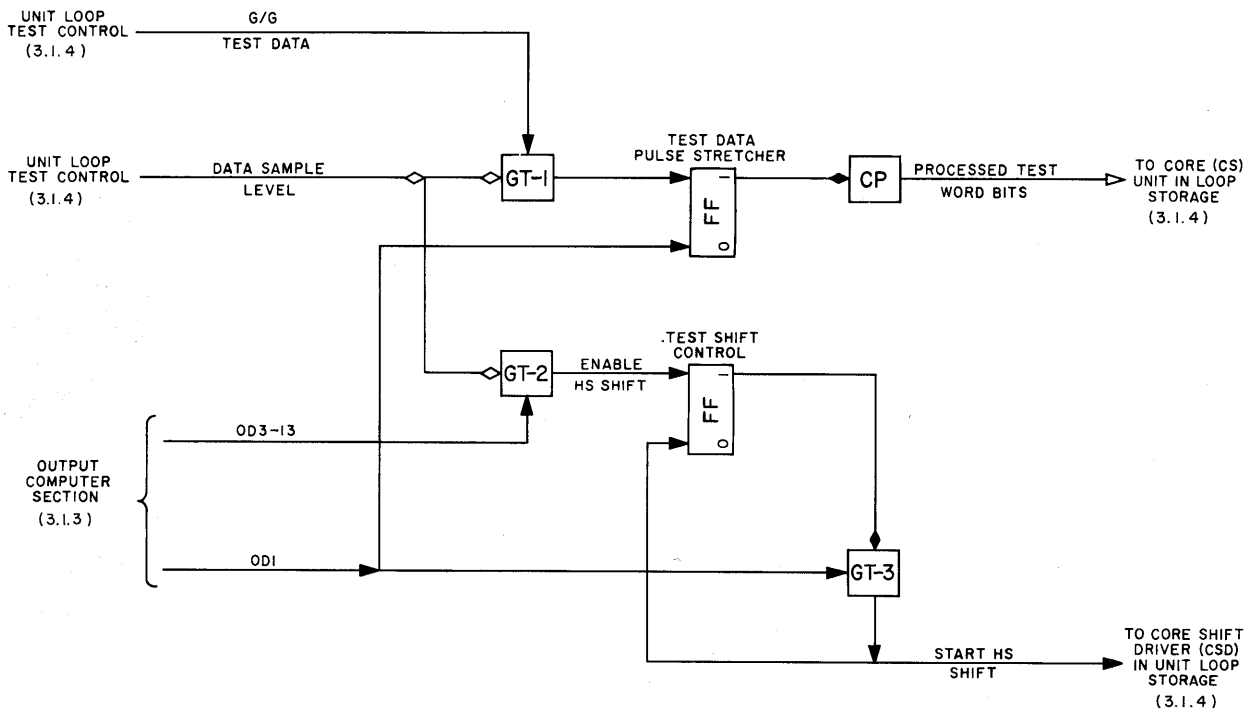


Figure 5–9. Test Core Shift Register Control Circuit (3.1.4), Simplified Logic Diagram

If the STOP ON ERROR switch is not engaged, the OR circuit following the master stop flip-flop has a +10V level on it at all times. In this case, the enable-OD-signal level is always present and the Output System is continuously cycling. Under this condition, the test is always in progress, even while the test word is being entered. Therefore, the START CYCLE button has no significance.

2.6.2.6 Transfer of Word from Output Storage Section to Test Circuit CSR

After the test word that has been entered is processed in the normal manner by the output control element, it is passed to the selected output storage section. The special test action which occurs in the selected storage section is described in 2.6.5. The G/G word is transferred from the output storage section back to the test equipment circuits after it leaves the output shift register (OSR) of the selected storage section. A TTY word is not returned to the test equipment circuits but is passed to a TTY monitor. Hence, the discussion that follows applies only to G/G words.

Since only one word is read into the selected output storage section array, the bits are shifted serially out of the OSR at a comparatively slow rate. A data-sample level is produced each time a bit of a G/G word is read out of the OSR. As shown in figure 5–9, when a bit is read out of the OSR, the produced data-sample level conditions GT's 1 and 2. The G/G test-data pulse is passed by the conditioned GT 1 and sets the test-data pulse stretcher flip-flop. The test-data pulse is generated only when a 1 bit is read out of the OSR and arrives at time OD 3–13. Since the flip-flop is cleared at OD 1, the core prime receives a 5.0-μsec pulse for each 1 bit in the test word. The core prime receives no pulse for the 0 bits in the test word. The core prime then primes the first core in the test core shift register (CSR) for each 1 bit in test word. At the same time that GT 1 is conditioned by the data-sample level, GT 2 is also conditioned by this level. (See fig. 5–9.) Gate 2 passes the OD 3–13 pulse as an enable-high-speed-shift pulse, which sets the 1 side of the test shift control flip-flop. This action conditions GT 3, which then passes an OD 1 pulse. The pulse resets the test shift control flip-flop and also pulses the core shift driver (CSD). The CSD shifts to the second core the bit set into the first core by the core prime, and so on down the line. Hence, it can be seen that the test shift control flip-flop (and related logic) pulses the CSD of the test CSR every 1/1,300 second, immediately after the core prime is either primed by a 1 bit in the test word or left unprimed by a 0 bit in the test word. This priming (or lack of priming), followed by a shift, continues until the complete test word is serially entered into the test CSR.

2.6.2.7 Data-Sample Level Generator

As part of the specific operations performed when making a G/G test, TEST switch S50 is set to the G/G position. Naturally, the switch position must agree with

the section address set into the test word. If G/G is selected, the G/G SELECT REGISTER 0–4 pushbutton (S44, fig. 5–10) is depressed the number of times necessary to cause stepper switch S1 to move to the position that corresponds to the register address set into the test word. The position of the stepper switch corresponds to the interleaving of the information in the output channels (slots). Hence, register addresses 0, 5, 10, 15, and 20 are read out of the OSR at the same time; register addresses 1, 6, 11, 16, and 21 are read out at the same time, etc. Therefore, the 25 register addresses in the G/G storage section are read out in groups of 5 by five different timing pulses, which occur at times 5-counter-equals-1 through 5-counter-equals-5. Hence there must be five positions of the stepping switch corresponding to these five timing pulses. These positions are 5CSR 1 CORE through 5CSR 5 CORE. Indicator lamps reveal which position the switch is in. The stepping switch is set to the position that corresponds to the register address set in the test word.

On the 5CSR line that corresponds to the register address in the test word, a level occurs at the same time that a bit is being read out of the OSR. By having relay K2 de-energized and the stepping switch in the correct position, the level is passed through K2 as the data-sample level.

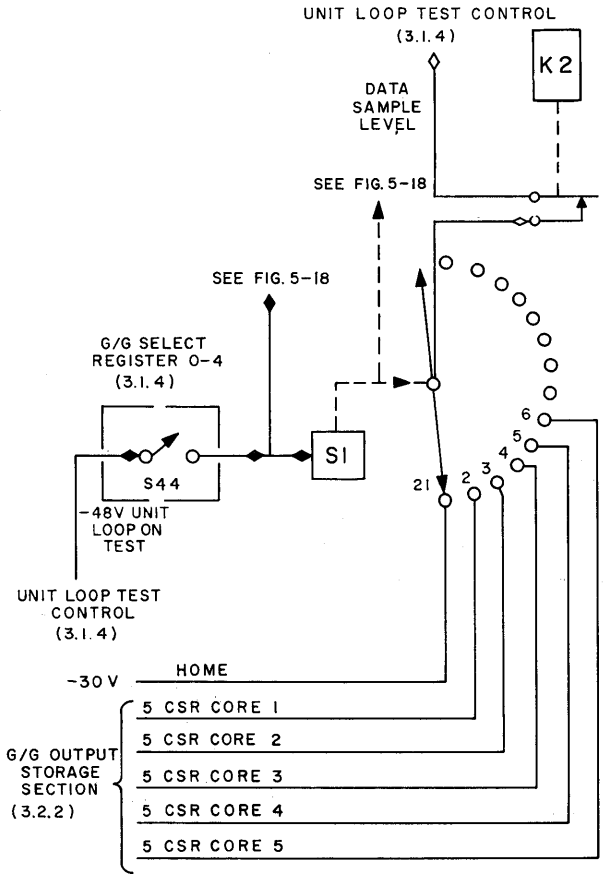


Figure 5–10. Data-Sample Level Generator (3.1.4), Simplified Logic Diagram

2.6.2.8 Test-Data Pulse Generator

As shown in figure 5–11, when the unit loop test is begun, the unit-loop-on-test signal level is sent to K1. The closing of this relay connects all G/G data lines 1 through 5 to a common output line. The data lines correspond to the channels (slots) in each storage section, and the register address of the G/G word corresponds to one of the data lines. A pulse is produced on the appropriate data line whenever a 1 bit in the test word is read out of the OSR. Hence, a pulse appears on the common G/G test data line for each 1 bit in the G/G test word, regardless of the register address of the word. The appropriate switch (S56 through S60) must be thrown that corresponds to the slot which includes the assigned register address.

2.6.2.9 Error-Detection AND Circuit

When the complete test word has been read into the test CSR as described in 2.6.2.6, a test-transfer pulse initiates a synchronizing cycle which results in the sampling of each core in the register. Each core containing a 1 bit sends a complementing pulse back to a particular flip-flop in the flip-flop register of the output Drum System. This flip-flop would be the corresponding right test word flip-flop into which the bit was originally entered. (The circuitry involved in the sampling of the test CSR is described in 2.6.4.) If, in a particular right word flip-flop, the original bit entered was a 1 and the complementing bit is (correctly) also a 1, the flip-flop is complemented with the 0 side up. If, in a particular right word flip-flop, the original bit entered was a 0 and the complementing bit is correctly a 0, the flip-flop has the 0 side up. However, if the original bit is a 1 and the complementing bit is (incorrectly) a 0, or if the original bit is a 0 and the complementing bit is a 1, the flip-flop is complemented with the 1 side up.

As shown in figure 5–12, the 0 side of the 16 right word flip-flops of the flip-flop register and the 0 side of the output parity bit generator flip-flop are fed to the 68-way AND circuit. If none of these bits has been erroneously changed from 0 to 1 or from 1 to 0 during the processing through the Output System, the complementing of the flip-flops should reset the 0 sides of all the flip-flops. The 68-way AND circuit conducts. The inverter then blocks any further passage of the signal level. However, if one (or more) of the flip-flops is complemented with the 1 side up, which would happen if an error occurred in the processing of the test word, the AND circuit would not conduct. The inverter then passes a level to the OR circuit which conditions a gate. The "0" TEST switch (S49) has been thrown to the G/G position. This passes the unit-loop-on-test signal level to a relay (K4) in the unit loop storage section.

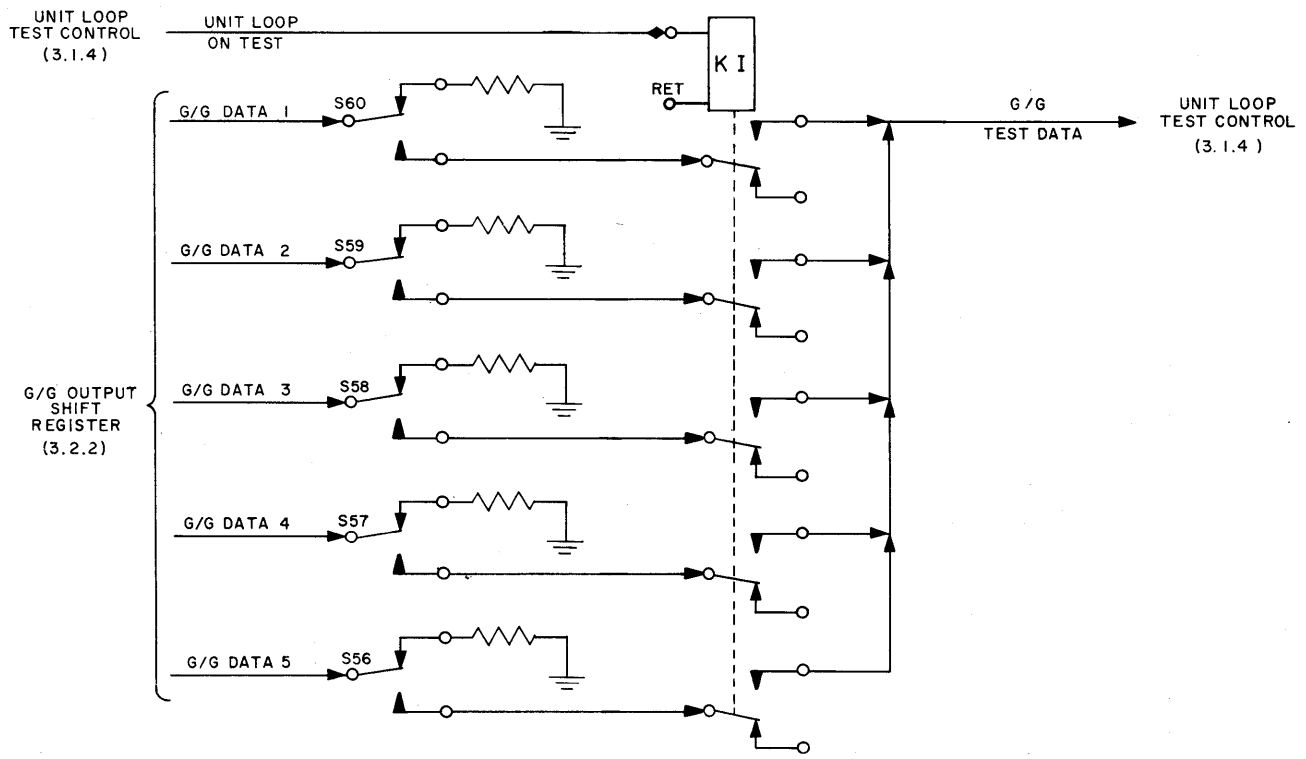


Figure 5–11. Test-Data Pulse Generator (3.1.4), Simplified Logic Diagram

This relay closes and passes a 19-counter-equals-19 pulse, for a G/G word, to the gate shown in figure 5–12 as a zero-test pulse. These pulses occur at the end of readout time in the respective sections and therefore arrive after the complete processing of the test word. If the gate is conditioned as a result of an error in the processing of the test word by the Output System, the gate passes the zero-test pulse. This sets the 1 side of the master stop flip-flop. Two actions can take place. If the STOP ON ERROR switch (S61) has been thrown, the unit-loop-on-test signal level is passed to K6, passing a —30V level to the second OR circuit. As a result, the enable-OD-pulse signal level is produced only if the 0 side of the master stop flip-flop is up. Since an error causes the 1 side of this flip-flop to be up, the enable OD level is cut off and the test stops. If the STOP ON ERROR switch is not thrown, the OR circuit receives a +10V level instead of the —30V level. Therefore, regardless of whether the 68-way AND circuit detects an error, the enable-OD-pulse level remains up and the test operation cycles continuously without stopping. However, neons that are not shown in figure 5–12 light if a flip-flop is not correctly complemented; these neons indicate the presence of an error.

2.6.2.10 Optional Operation Control Circuits

The previous paragraphs described the cyclic mode of operation of the test circuits. It was noted that the test word cycles continuously and stops only if the STOP ON ERROR switch is thrown and there is an error in the processing of the test word. There are two other possible modes of operation: the single-cycle mode and the manual-pulse mode. In the single-cycle mode, the test word makes one complete cycle through the system each time the SINGLE CYCLE OUTPUT button is depressed. In the manual-pulse mode, the test word completes one step in the loop cycle each time the MANUAL PULSE button is depressed. For either of these tests, the STOP ON ERROR switch must be engaged to provide a —30V level at the OR circuit following the master stop flip-flop. (See fig. 5–12.) If this is not done, the normally present +10V level in this OR circuit will at all times pass an enable-OD-pulse signal level. Under this condition, the single-cycle or manual-pulse test cannot be performed since the test word will just keep cycling continuously.

2.6.2.11 Single-Cycle Mode

As shown in figure 5–13, when the SINGE CYCLE OUTPUT button is depressed, the single-cycle output pulse generator passes a pulse to the master stop flip-flop. This sets the 0 side of this flip-flop and produces an enable-OD-pulse signal level which causes the unit loop cycle to begin. The single-cycle output pulse also sets the 1 side of the single-cycle output flip-flop up. This conditions the zero test gate, which passes a pulse at 19-counter-equals-19 time, as previously described. This sets the master stop flip-flop, which cuts

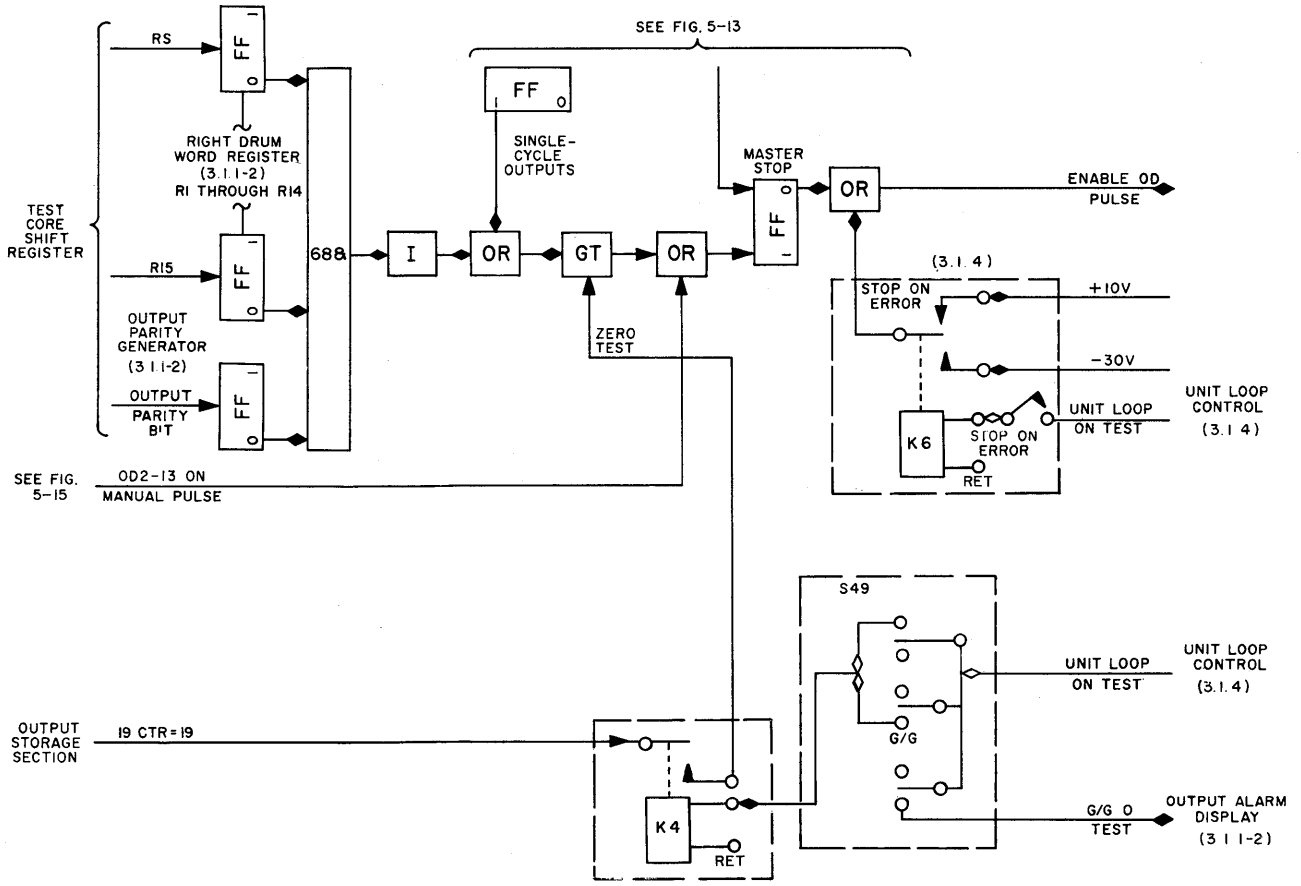


Figure 5–12. Error Detection Circuit and Master Stop (3.1.4), Simplified Logic Diagram

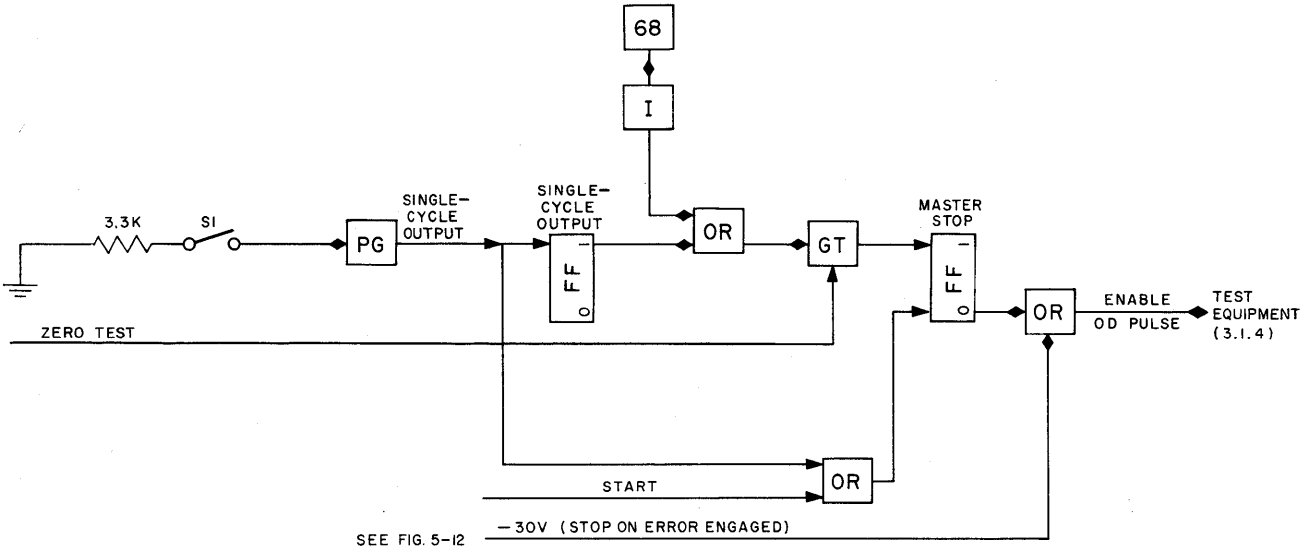


Figure 5–13. Single-Cycle Control Circuit (3.1.4), Simplified Logic Diagram

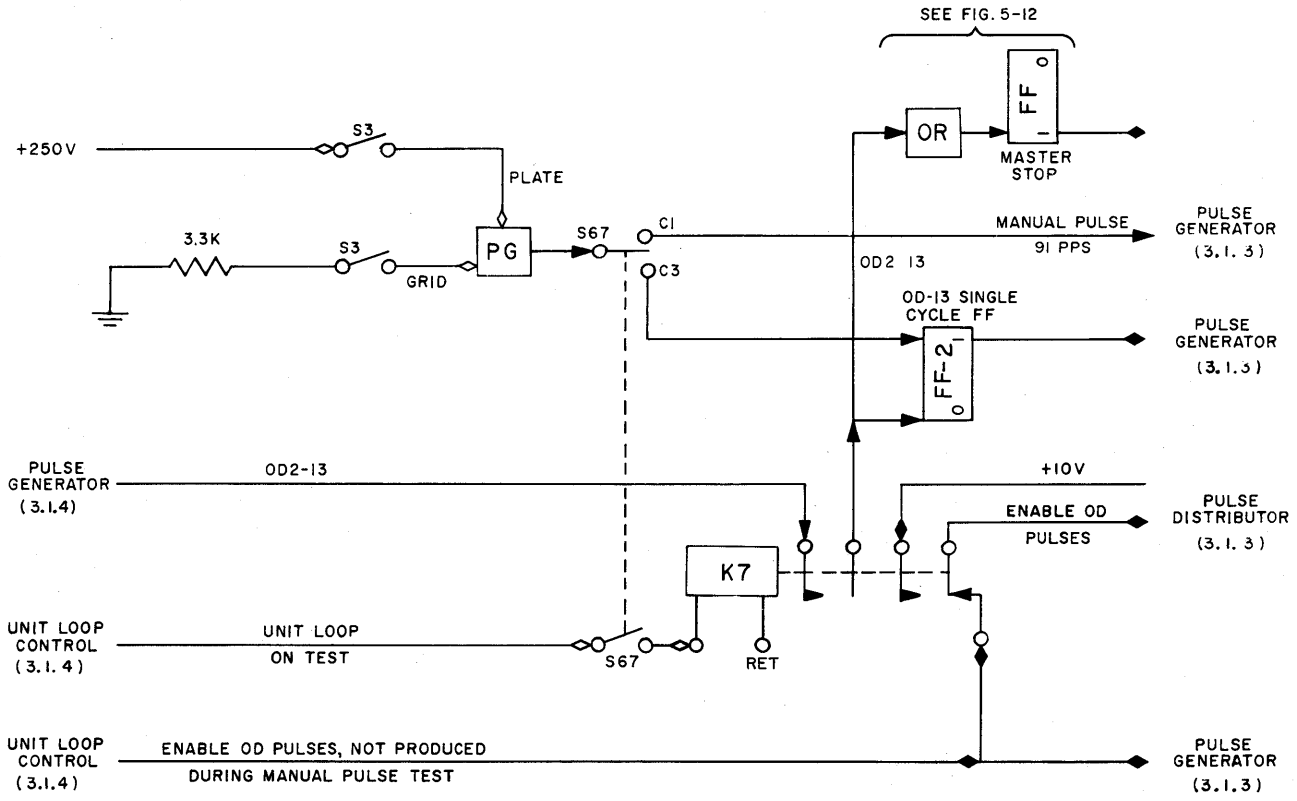


Figure 5—14. Manual Pulse Control Circuit (3.1.4), Simplified Logic Diagram

off the enable-OD-signal level. Hence, the Output System stops, and one complete cycle of the test word has been made.

To switch to a continuously cycling mode of operation, the START CYCLE pushbutton is depressed and the action described in 2.6.2.5 takes place.

2.6.2.12 Manual-Pulse Mode

The manual-pulse mode consists of two distinct phases: the manual-pulse 1,300-cps mode for G/G and the manual-pulse 91-cps mode for TTY. The two modes are very similar.

If the manual-pulse 1,300-cps mode is selected, the MANUAL PULSE CTRL switch is moved to 1,300. As shown in figure 5—14, this puts switch S67 in position C3 so that, when the pulse generator produces a pulse, it goes to the OD 13 single-cycle flip-flop of the OD 13 pulse generator. In the other position of the switch, the pulse goes to the OD 91 pulse generator. For either position of S67, the unit-loop-on-test level is passed to K7 to close it. (See fig. 5—14.) An OD 2—13 pulse is transferred through K7 to the OD 13 single-cycle flip-flop. This pulse also goes to the 1 side of the master stop flip-flop to cut off the enable-OD-pulse signal level. A +10V level is passed as the enable-OD pulse to the pulse distributor (Part 2) since the enable-OD pulse is not produced. The manual pulse takes the place of the enable-OD pulse shown in figures 5—8 and 5—12. When the MANUAL PULSE pushbutton (S3) is depressed, the pulse generator produces a pulse which sets the OD 13 single-cycle flip-flop or OD 91 single-cycle flip-flop up. As described in Part 2, the 1,300-cps oscillator turns on the OD 13 start flip-flop (FF 1, fig. 2—39) and one set of OD pulses (OD 2—13, OD 3—13, and OD 4—13) is generated. The OD 2—13 pulse resets the OD 13 single-cycle flip-flop, and no further pulses are passed. Hence the MANUAL PULSE pushbutton allows OD 91 pulses for a TTY test or OD 13 pulses for a G/G test to be applied at a controlled rate. Thus, each step taken in the output storage element may be examined for sources of possible errors.

2.6.3 Unit Loop Control, Test-Word Generator

The test-word generator (fig. 5—15) produces a pulse for each 1 bit selected for the test word. The test-word pulse is generated in the following manner.

An OR circuit passes either a 19-counter-equals-1 or a start-search pulse to the test-word generator flip-flop, depending on whether a G/G or TTY test has been selected. The G/G pulses occur at the start of a readout cycle, and the TTY signal is the start-search signal which normally goes to the TTY burst counter. The test-word generator flip-flop conditions a gate which passes an OD 1 pulse as the pulse which pro-

duces 1 bits in the selected flip-flop registers of the output control element. Since during normal operations the drum word is entered at time OD 1, the timing of the test word is made to agree exactly with the timing of a normal drum word.

2.6.4 Unit Loop Storage

The unit loop storage section is the test CSR previously described. It accumulates the processed test-word bits from the selected section and register of the output storage section. The bits are shifted into the test CSR, which is a series of 17 tape cores (core shifts) in serial form. At the end of the output storage section readout operation, the contents of the core shifts are read out in parallel to complement the corresponding flip-flops in the right half of the flip-flop register of the output control section, where the test word was originally entered.

Since the TTY word is not fed back to the flip-flop register for comparison with the original test word but is, instead, sent to a TTY monitor for a visual comparison, the unit loop storage discussion applies only to a G/G test word.

2.6.4.1 Parallel Readout Control

When the TEST switch (S50, fig. 3–55) is moved to G/G (the section address assigned to the test word), K5 (fig. 5–16) is energized. For a G/G test, a 19-counter-equals-17 pulse is selected. This pulse occurs just before the last group of like-order bits is read out of the corresponding storage section. Hence, the pulse occurs just before the last bit is read into the first core shifts.

At the following OD 2 time, the second flip-flop in the parallel readout control circuit is set and remains set until the last bit is received from the output storage element. The last bit is read into the core register, and the high-speed shift takes place. As the shift pulse is ended, the end-shift signal is gated through the parallel readout control circuit to generate the readout pulse. This pulse is carried to the parallel readout gates in the core register circuit to effect the transfer of information to the flip-flop register for comparison.

2.6.4.2 Core Register Circuit

The core register circuit, shown in figure 5–17, is a tape-core register of 17 core shifts and is similar to the 19-counter in the G/G storage section. The processed test-word pulse from the storage register control circuit (fig. 5–9) reads the extracted bit into the read-in winding of the first core of the register. (See fig. 5–17.) This read-in occurs for 5.0 μsec between OD 3 and OD 1 times. The shift pulse starts at OD 1 with the receipt of the start-high-speed-shift signal from the storage

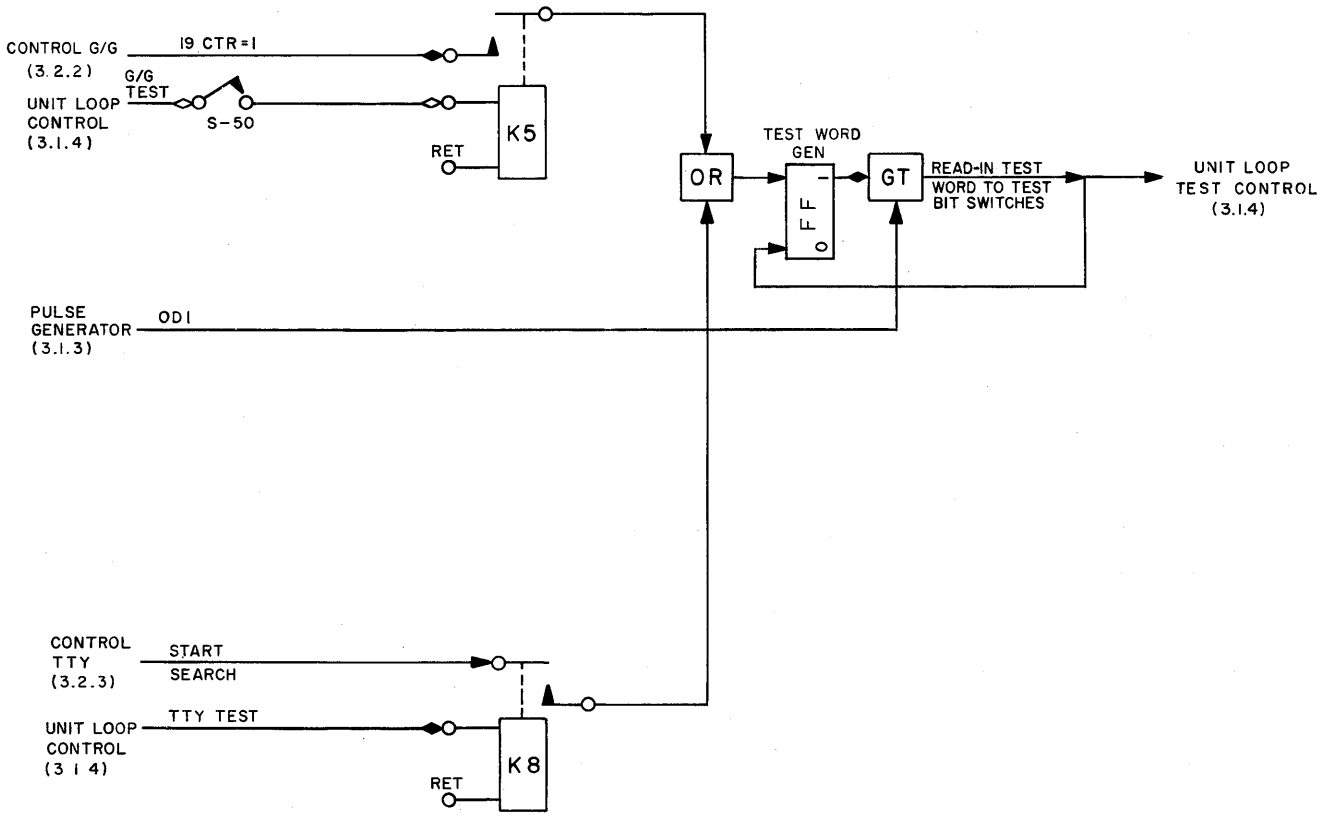


Figure 5–15. Test Word Generator (3.1.4), Simplified Logic Diagram

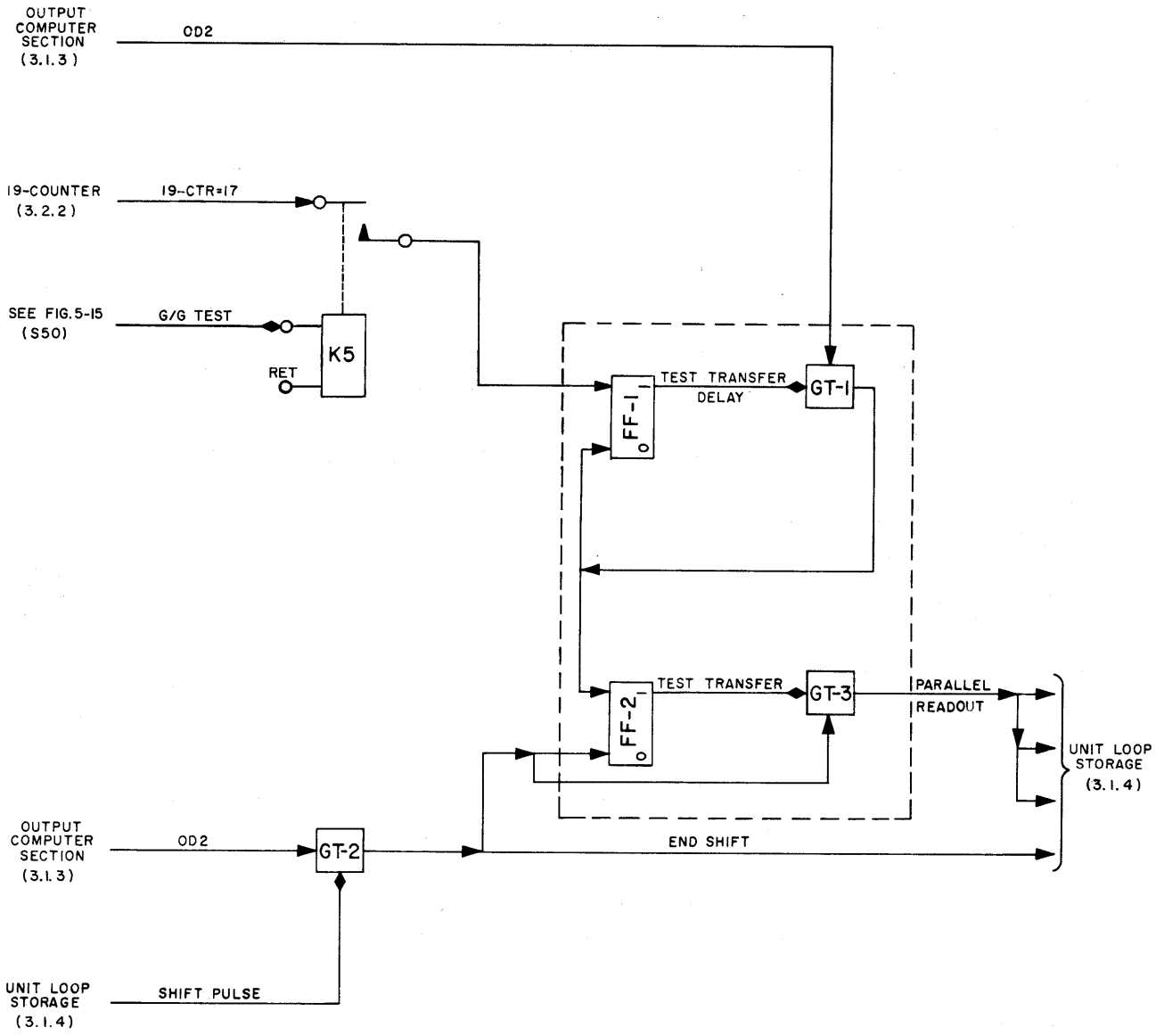


Figure 5–16. Parallel Readout Control Circuit (3.1.4), Simplified Logic Diagram

register control circuit. The start-high-speed-shift signal and the end-shift signal control the shift flip-flop. This flip-flop supplies the shift pulse to the register. The shift pulse lasts 2.5 μsec from OD 1 to OD 2. At OD 2 time, following the shift pulse, the former content of each core appears at the output line to the gate circuit at the same time that the bit is being read into the next core. However, there is no transfer through these gates unless they are pulsed by the readout signal. After the last pulse, however, the register is full. The readout signal, which comes from the parallel readout control circuit at OD 2 time and coincides with the end-shift signal, is applied to the parallel readout gates, causing the information to be transferred.

When the TEST switch (S50) in the test-word generator circuit of the unit loop control is in the G/G position, the two relays in the core register circuit are energized, causing the data in bits R8 through R15 to be transferred in unmodified form. Thus, in the parallel readout operation, each bit is directed back to the individual flip-flop of the OB register from which the bit was originally generated.

2.6.5 Specific Unit Loop Tests

The preceding paragraphs described the general, common circuitry and processes used in making a unit loop test involving the G/G storage section. The paragraphs that follow describe the particular processes and circuitry unique to that particular storage section. As has been previously mentioned, the output control element functions in the normal manner regardless of the storage section selected.

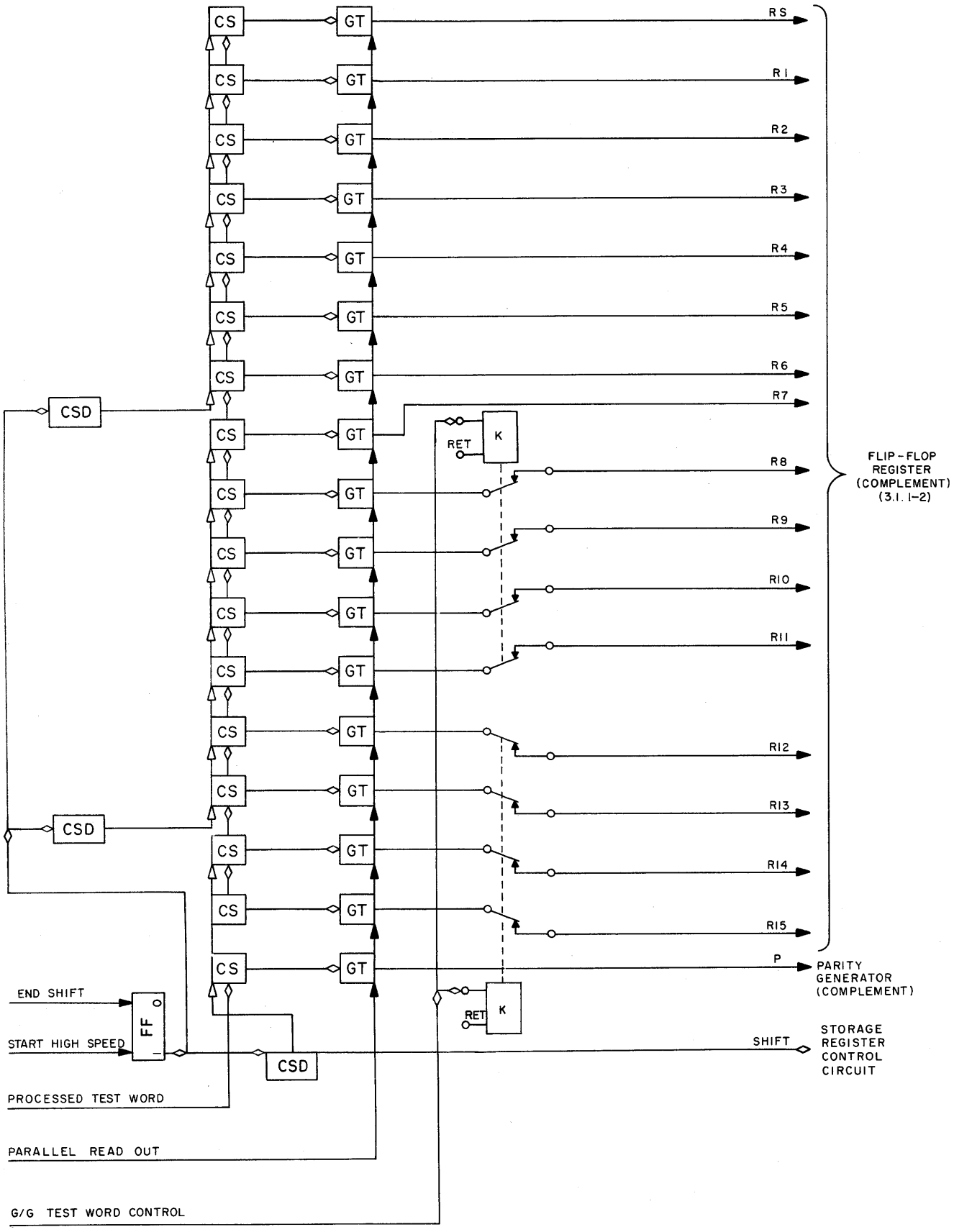


Figure 5–17. Core Register (3.1.4), Simplified Logic Diagram

2.6.5.1 Ground-to-Ground

The overall operation of the G/G storage section during a unit loop test is essentially the same as during normal operation, except for a number of minor variations. Since only one word is read into the storage array, there must be some means of synchronizing the operation of the test CSR with the readout of the output shift register of the G/G storage section. In addition, the G/G burst counter must be inhibited.

Synchronization is accomplished by using the 19-counter-equals-17 pulse to initiate transfer on the information stored in the test CSR to complement the flip-flop register, using the 19-counter-equals-19 pulse as the zero test, and using the 19-counter-equals-1 pulse in the test word generator.

For a G/G unit loop test, a test word is written into one register in one array during the first 19-counter cycle. During the second 19-counter cycle, the test word is read out of this array while it is being read into the other array. This results in an alternate read-in and readout operation as far as the arrays are concerned. It is possible to select one array and to operate it at twice its normal rate while the other array is idle; that is, a read-in and readout of the same array will occur during each 19-counter cycle.

Test switch S50 selects the storage section and the 19-counter pulses used for the G/G unit test. When the TEST switch (S50) is set to the G/G position, it passes the unit-loop-on-test signal level as an inhibit signal to the G/G burst counter. In addition, the unit-loop-on-test signal level is also sent to a relay in the completed message shift register (CMSR) of the G/G output storage section. This action permits readout after one word has been read into a slot, rather than after the normal number of five words. The output is now taken from the second core rather than from the sixth core of the CMSR. (Refer to Part 3.)

As was described in 2.6.2.7, the register address that corresponds to the address set into the test word is set into the data-sample level circuit by means of stepping switch S1, shown in figure 5–10. Not all portions of this switch are shown in this figure, the remaining portions being shown in figure 5–18. As shown in figure 5–18, bank B of the switch operates indicator lamps to indicate the register address selected each time the stepping switch is depressed. Bank A of the switch is used to return the stepping switch to the HOME position. As seen from figure 5–18, all the contacts of this bank of the switch are tied together except the HOME position. Hence, when G/G HOME pushbutton S43 is depressed, the unit-loop-on-test signal level is passed to the shorted contacts of bank A of the stepping switch. This causes the switch to step automatically to the HOME position, at which point the signal level is no longer connected. The HOME position is the neutral position of the switch.

2.6.5.2 Teletype Monitor Test

During testing, the TTY output storage section functions essentially the same as during normal operations. As has been previously described, in the TTY test, the test word is not looped back to the test control circuits and the 17-way AND circuit for a zero test, but is passed to a monitor where a visual comparison is made between the original test word and the processed test word.

When setting up the test word, the procedure is the same as that previously described for the G/G word, except that, for the TTY word, bit RS must be a 1. This is necessary to provide the first busy bit. The remaining bits of the right drum word are selected to represent desired TTY characters.

A particular TTY slot must be selected by using the switches on the duplex maintenance console. Since in the TTY storage section there is one slot for each register address, the slot selected must agree with the register address set into the test word.

As shown in figures 5–15 and 5–19, when a TTY storage section test is selected, TTY TEST switch S47 is lifted. This passes the unit-loop-on-test signal level to

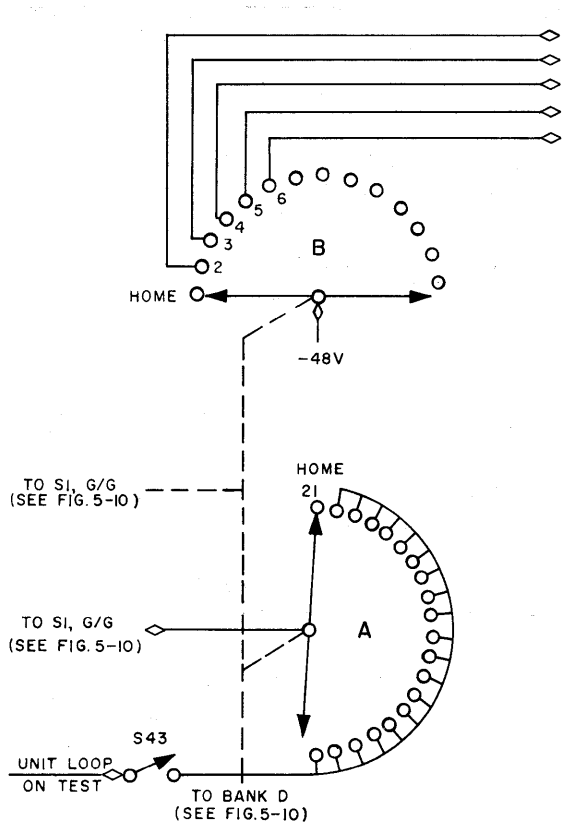


Figure 5–18. Stepping Switch Home Control (3.1.4), Simplified Logic Diagram

K8. As shown in figure 5–15 and described in 2.6.3, the start-search pulse is applied to the test word generator. This action of transferring the route of the start-search pulse inhibits the TTY burst counter, as required. Also, as shown in figure 5–19, the start-search pulse turns on the master stop flip-flop, which permits single cycling in the TTY test. If an error occurs within the TTY storage section, the TTY parity neon will be turned on.

2.7 COMPUTER LOOP TEST

2.7.1 General

The computer loop test is a comprehensive check of the input and output circuits of AN/FSQ-8 Combat Control Centrals. It tests the operation of the Output System, Input System, Drum System, and various parts of the Central Computer System itself. During the test, the alignment of the flow of information through the various elements of AN/FSQ-8 Combat Control Central closely approximates the alignment of information flow in the equipment when it is actually processing the air defense problem.

Basically, the output of the G/G storage section is looped through the test equipment section to the crosstell (XTL) input element. Figure 5–20 shows the path of information flow.

The test information originates within the Central Computer System and is passed through the OB fields of the Drum System to the Output System. In the Output System, the test information passes through the G/G storage section and the test equipment section to the XTL element of the Input System, through the XTL field of the Drum System, and back into the Central Computer System for comparison with the original test information.

2.7.2 Ground-to-Ground to XTL Input Loop

In the regular operation of AN/FSQ-8 Combat Control Centrals, the output of the G/G storage section is transmitted over telephone to one of the adjacent AN/FSQ-8 Combat Control Centrals. Information enters the adjacent equipment through the XTL input element. The manner in which the information is transmitted, therefore, is compatible with the operation of the XTL input element.

There are five G/G output channels. Each of these channels is capable of being included in the computer loop test, one at a time. Further, there may be several XTL input channels in the XTL input element. Only one such input channel may be used at one time in the computer loop test.

Therefore, to conduct the test, it is necessary to select one G/G output channel and one XTL input channel. The test information is programmed to pass through the Output System and must reflect the channel selection in the address part of the information. The selection and switching of input and output channels is accomplished manually within the computer loop control. Since the information is already compatible, it is switched straight through the computer loop control without any modification. However, it is necessary to manually disconnect the output channel from the telephone line transmission equipment and the input chan-

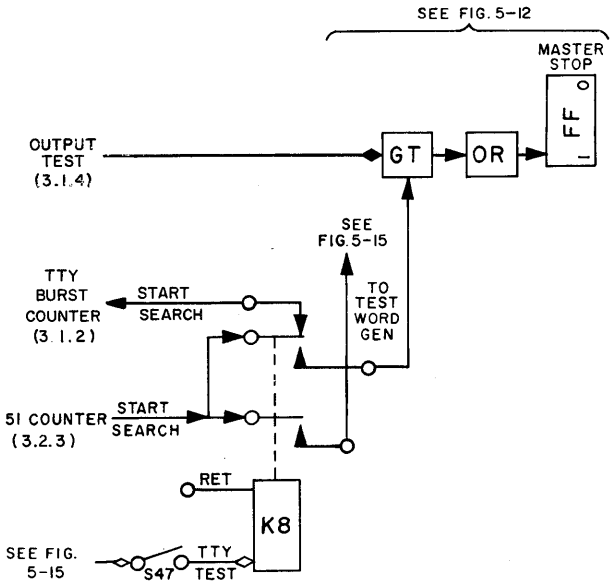


Figure 5–19. TTY Unit Loop Test Control Circuit (3.1.4), Simplified Logic Diagram

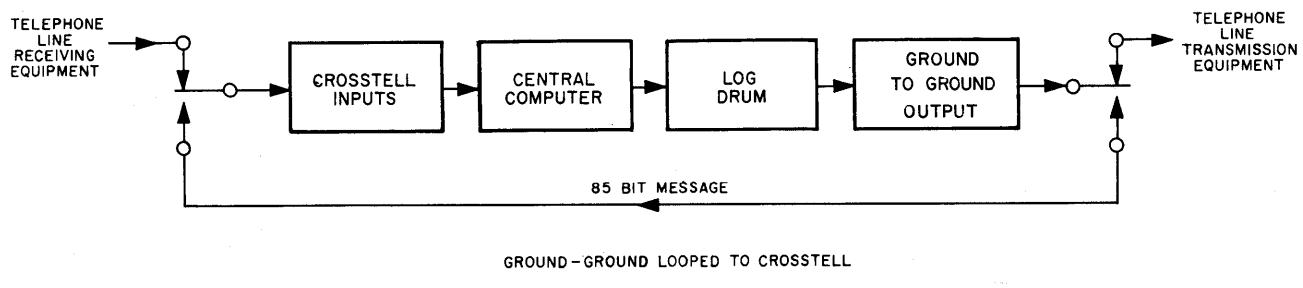


Figure 5–20. Computer Loop Test, Flow of Data, Block Diagram

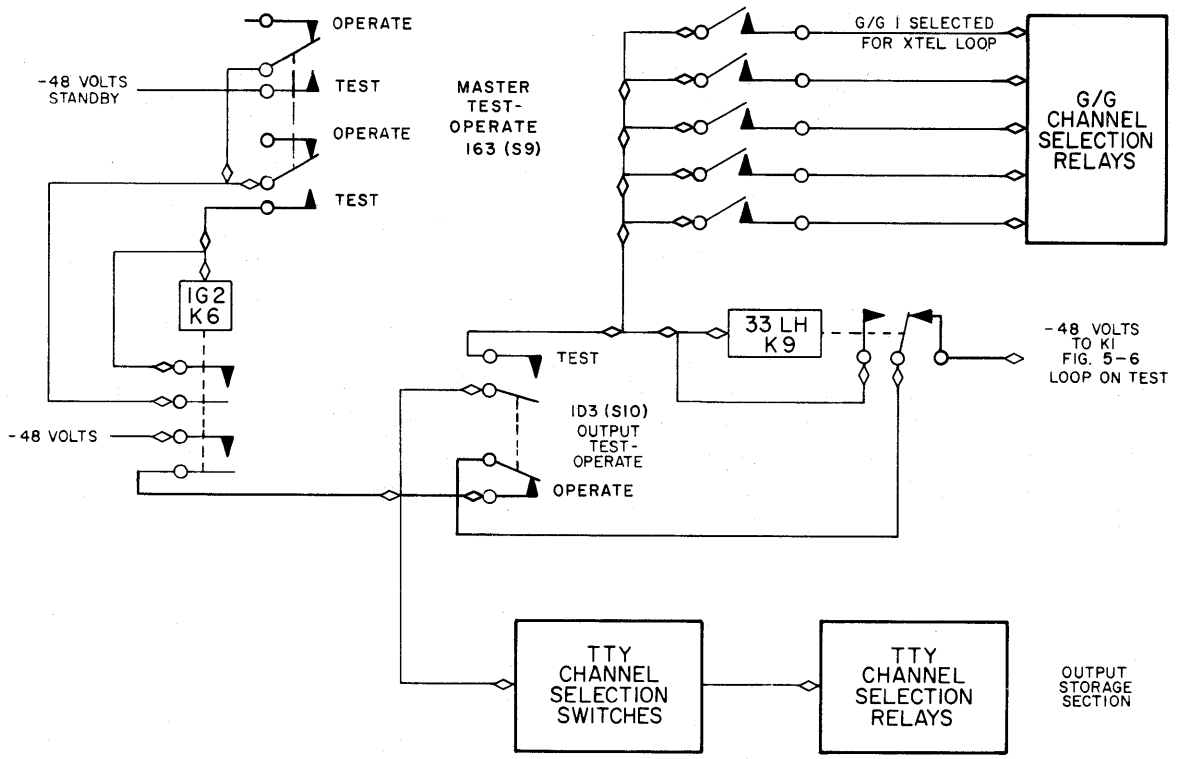


Figure 5–21. Computer Loop Test Relaying and Switching, Simplified Block Diagram

nel from the telephone line receiving equipment. The test information is programmed within the Central Computer System.

2.7.3 Teletype Monitor Test

A computer loop test may be performed on the TTY storage section. However, there is no provision for feeding information from the Output System back to the Central Computer. Therefore, a TTY monitor such as is used in the TTY unit loop test is used in the TTY computer loop test. The circuitry described in 2.8.2 and 2.8.3 also applies to a TTY test.

2.8 COMPUTER LOOP CONTROL

2.8.1 General

The computer loop control provides some of the circuits for manually switching test information from the selected G/G output channel to the selected XTL input channel. Certain of the switches are included in the Central Computer System.

To place the Output System in a computer loop test, the Central Computer must be in the standby status. The MASTER TEST-OPERATE switch on the duplex maintenance console and the OUTPUTS TEST-OPERATE switch in the Central Computer must be moved to the TEST position. This action supplies relay voltage to the TTY channel selection switches and to relay K9LH, as shown in figure 5–21. The energizing of K9 cuts off power from K1 (fig. 5–6), which cuts off any unit loop test in progress. Hence, the computer loop test always overrides a unit loop test which may be in progress. The energizing of K9 also provides voltage to the G/G to XTL CHANNEL SELECTION switch in the Central Computer. This allows the desired channel to be selected and connected to the test bus through the relays in the duplex and test switching of the output storage section.

2.8.2 Stop to Drums

As shown in figure 5–22, when the STOP TO DRUMS switch in the Combat Control Central is turned on, K2 is energized. This sends a —30V level as a nonreset-on-error signal and a —10V level as a stop-to-drum signal level to the alarm control section. As described in 4.2 of Part 2, the —30V nonreset-on-error

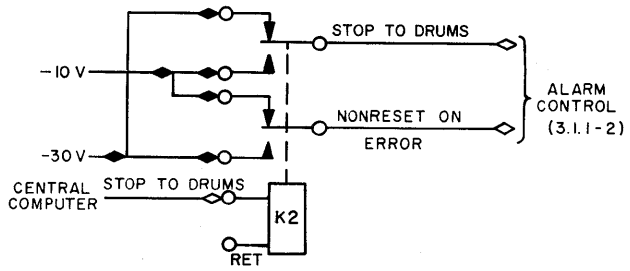


Figure 5–22. Stop-to-Drums Circuit (3.1.4), Simplified Logic Diagram

signal causes the contents of the flip-flop register of the output drum section to be retained for inspection if a parity-NG, an illegal register, or section address alarm is produced during a test. The stop-to-drums pulse is passed to the Drum System if either of the previously mentioned errors occurs. It stops the Drum System and prevents the erasure of the test word so that the error can be examined.

2.8.3 Restart to Drum Circuit

At the completion of a test operation, when the OUTPUTS TEST-OPERATE switch is moved to the OPERATE position, the falling of the test-outputs signal generates a pulse in the restart-to-drums circuit. (See fig. 5–23.) The pulse thus generated sets the restart-to-drums-A flip-flop, which is a synchronizing flip-flop. The restart-to-drums-B flip-flop is set at the following OD 3 time; at OD 1 time, the restart pulse is generated.

The restart pulse is carried to the Drum System and to the parity generator of the output control element. This pulse is used in the Drum System to re-enable the transfer of the information from the OB drum to the Output System. In the output control element, the pulse causes a compare signal to be sent to the Drum System for 100 ms but prevents any words from being accepted during the 100-ms interval. This prevents any old information in the drums from being transferred and causes any such information to be erased from the drums. The 100-ms period is long enough to allow erasure of all three OB drum fields used. The outputs active signal, which arrives when a system is changed from standby to in-use, has the same effect as the test-output signal.

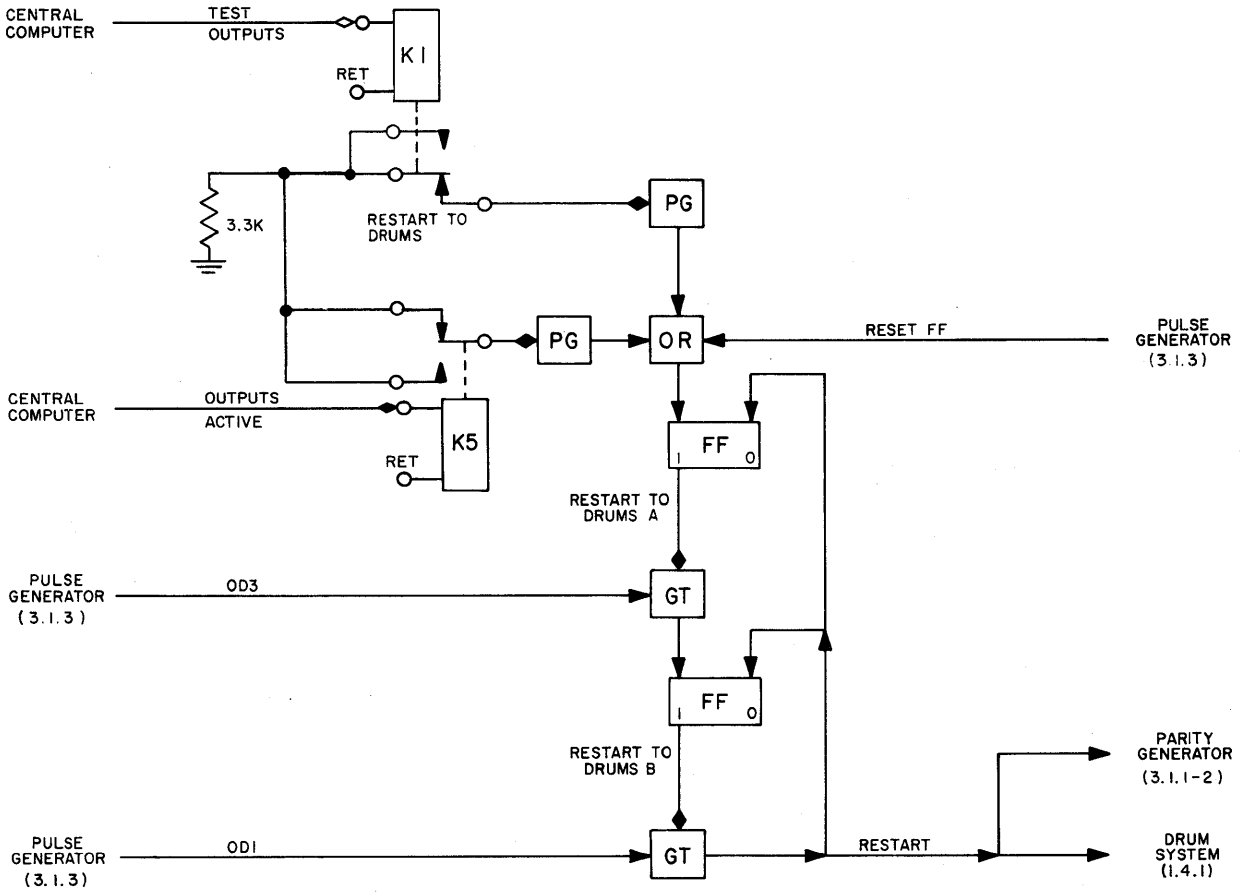


Figure 5–23. Restart-to-Drums Circuit (3.1.1-2), Simplified Logic Diagram

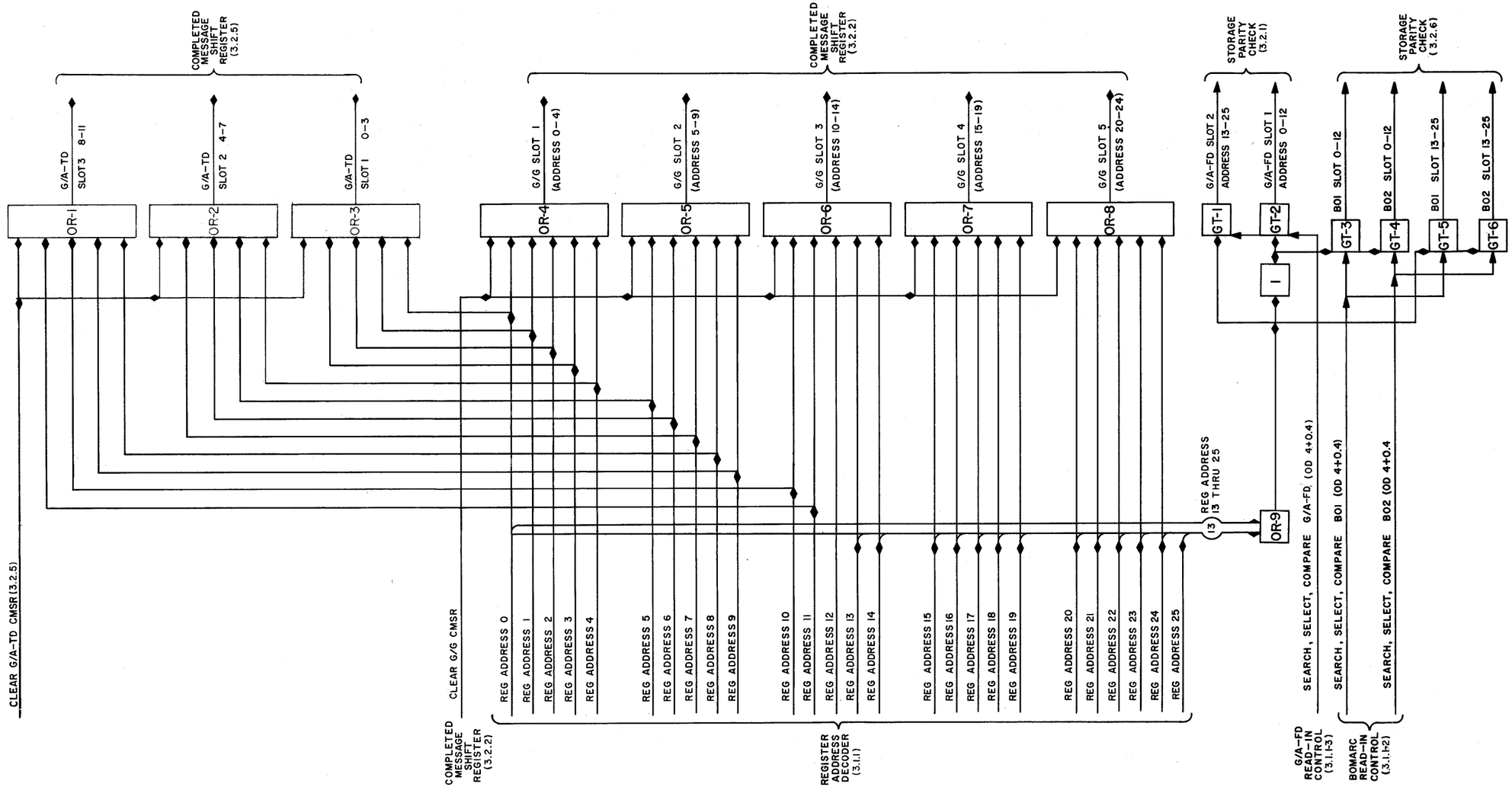
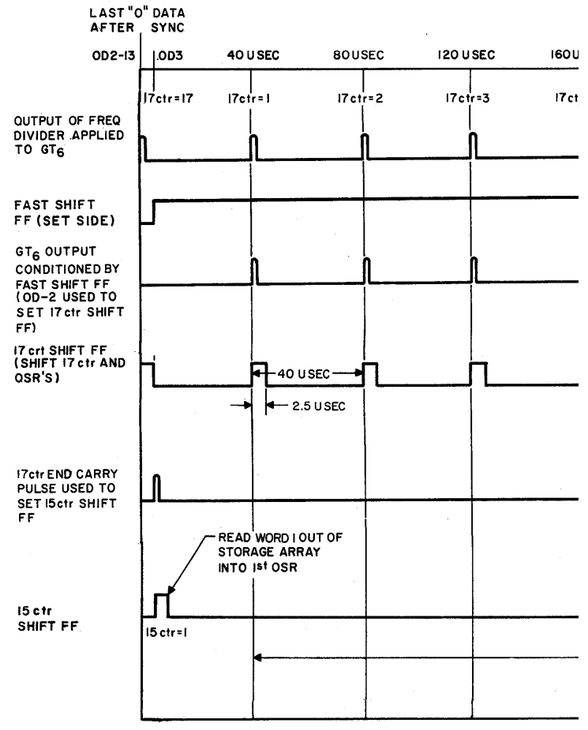


Figure 2–15. Slot Detection Circuit (3.1.1), Simplified Logic Diagram


LAST "0" DATA AFTER SYNC
OD2-13
OD3
40 USEC
80 USEC
120 USEC
160U
17ctr=17
17ctr=1
17ctr=2
17ctr=3
17ct
OUTPUT OF FREQ DIVIDER APPLIED TO GT6
FAST SHIFT FF (SET SIDE)
GT6 OUTPUT CONDITIONED BY FAST SHIFT FF (OD-2 USED TO SET 17 ctr SHIFT FF)
17 crt SHIFT FF (SHIFT 17 ctr AND OSR'S)
40 USEC
2.5 USEC
17ctr END CARRY PULSE USED TO SET 15ctr SHIFT FF
READ WORD 1 OUT OF STORAGE ARRAY INTO 1st OSR
15 ctr SHIFT FF
15 ctr=1

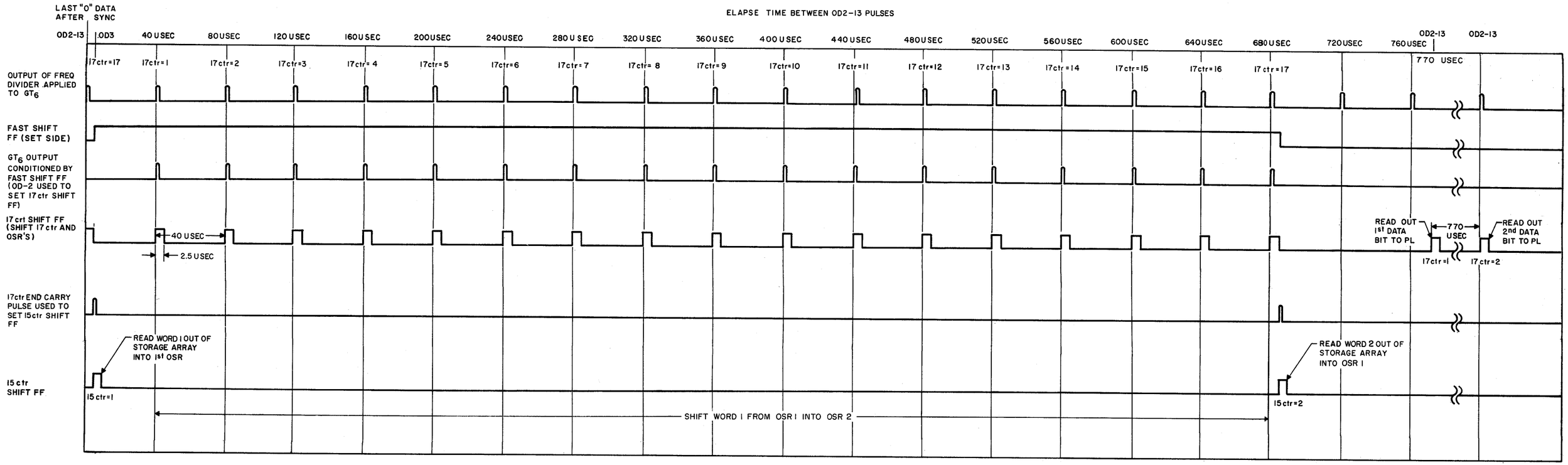


Figure 3–43. G/A-TD High-Speed Shift Timing Chart

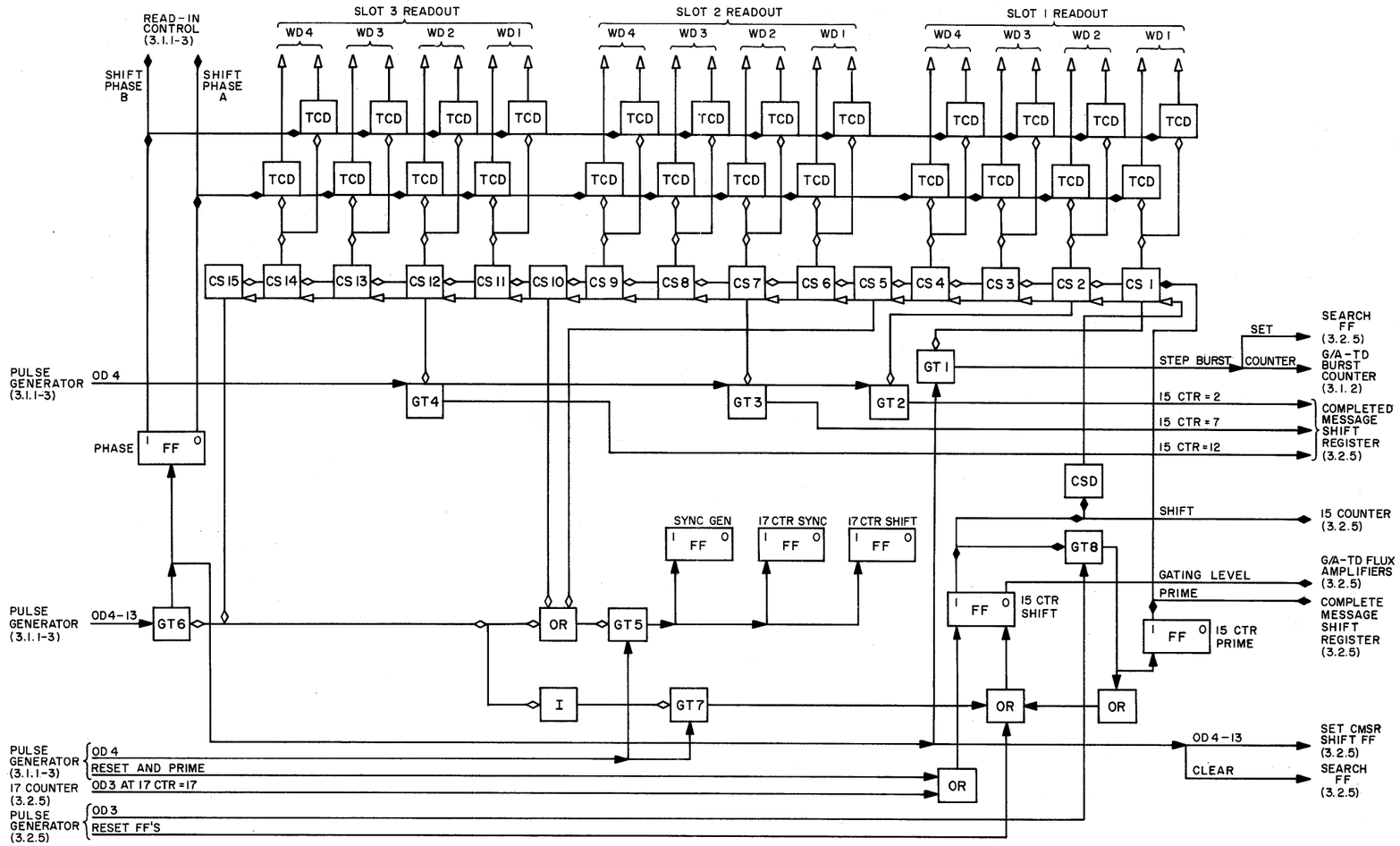


Figure 3-44. G/A-TD 15 Counter (3.2.5), Simplified Logic Diagram

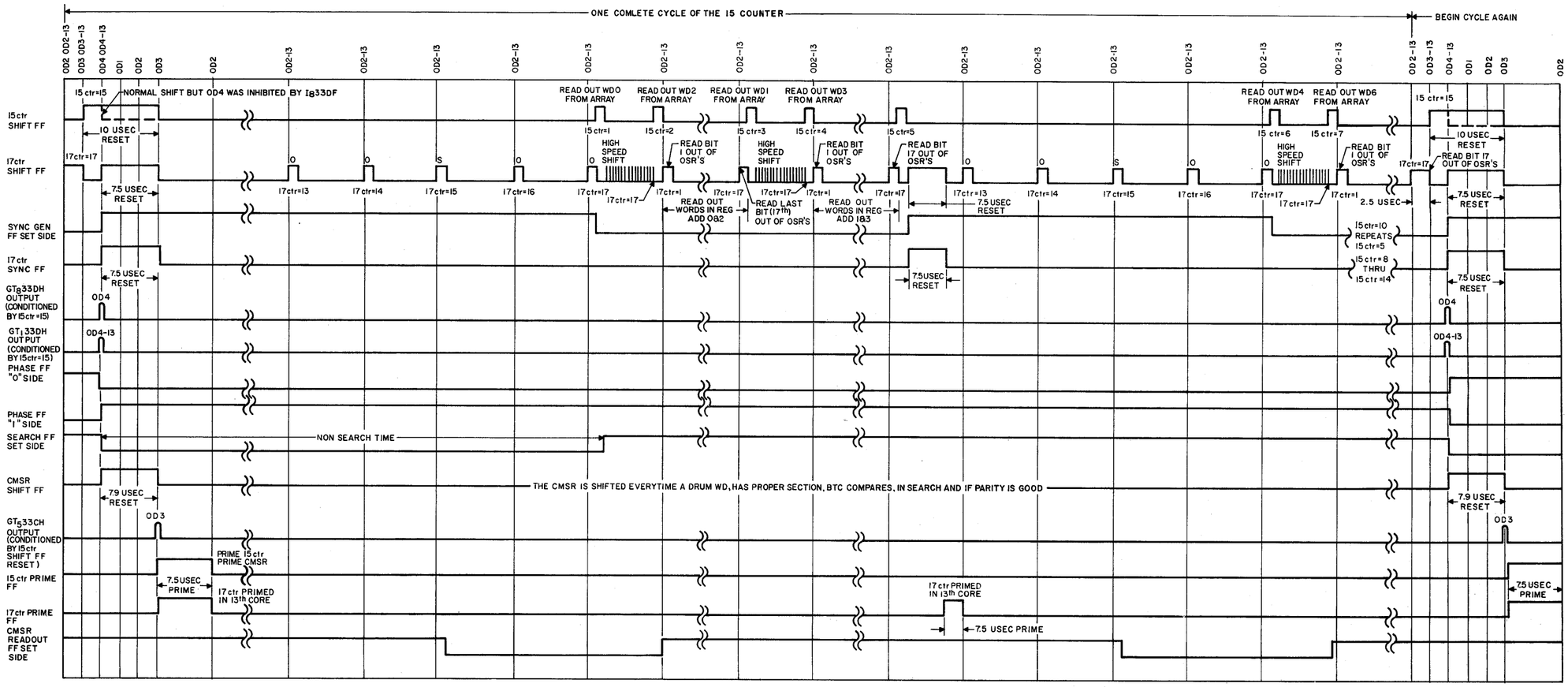


Figure 3–45. Overall Timing Chart, G/A-TD Storage Section

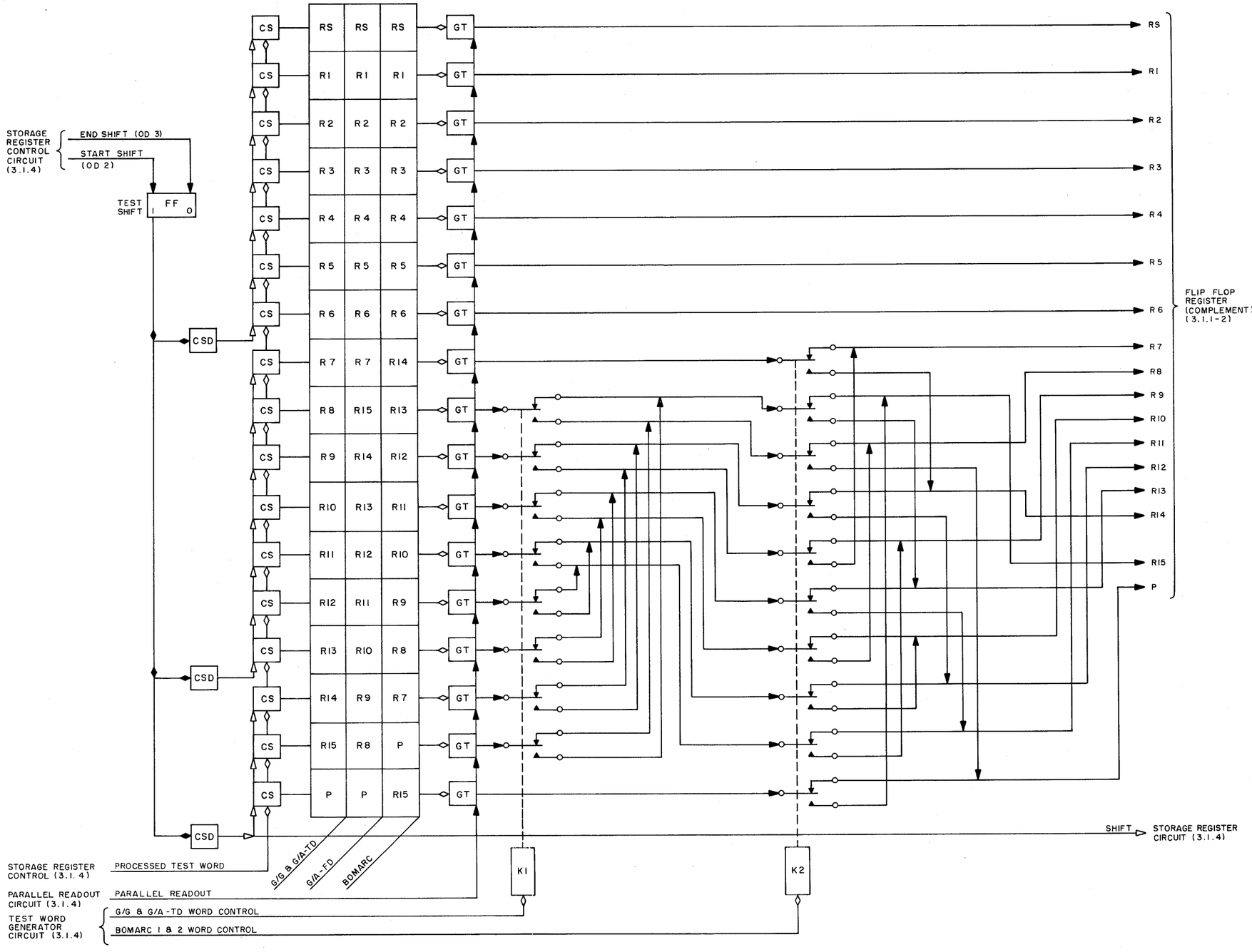


Figure 4–12. Core Register (3.1.4), Simplified Logic Diagram

INDEX

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INDEX (cont'd)

INDEX (cont'd)

INDEX (cont'd)

INDEX (cont'd)

INDEX (cont'd)

INDEX (cont'd)

INDEX (cont'd)

INDEX (cont'd)

INDEX (cont'd)

INDEX (cont'd)

INDEX (cont'd)

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