Computer Systems Department

LONG RANGE INPUTS
C694-416L-ST

15 April 1967

Keesler Technical Training Center
Keesler Air Force Base, Mississippi

Designed For ATC Course Use

Computer Systems Department
KTTC, Mississippi

Student Text
ABR30533-1
15 April 1967

Long Range Inputs

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I. Introduction to Long Range Inputs

A. Scope of Course

1. This text presents both an introduction to LRI and also a detailed explanation of the LRI equipment.

2. A short review of Tape Core Theory is given.

3. A detailed presentation of the LRI Monitor frame and consoles, both old and new systems.

B. Inputs in General

1. Introduction

   a. The AN/FSQ-7 Combat Direction Central is a data-processing system of the high-speed digital-computer type performing operations on data in binary form. It receives information of the air defense situation continuously, automatically, and in large volume, and must process this information without delay. These requirements call for an elaborate Input System, quite different from anything usually found in data-processing systems. Input Systems in general, and then the AN/FSQ-7 Input System, are discussed below.

2. Input Systems in General

   a. Consider first a simple data-processing system such as a desk calculator. This instrument is a slow-speed mechanical, decimal, digital computer. It is capable of accurate and efficient computation, but a means must be provided for the operator to introduce into the machine the problem which he wishes solved. This means is the calculator keyboard. The operator expresses the problem by depressing keys which, in turn, operate the necessary mechanisms in the machine. The keyboard is the input "system" of the calculator.

   b. More elaborate mechanical and electronic-mechanical data-processing systems can process a much greater volume of data in a given time than any desk computer. In fact, data cannot be inserted manually into such a machine fast enough to take advantage of its capabilities, and is therefore transferred to punched cards or punched tapes. This makes possible an accumulation of input data which the computer can then accept at a rate compatible with its data-processing capacity

c. Computing machines operating by means of moving parts are inherently slow compared to modern electronic computers using pulsed electronic signals. Again, however, the Input System must be adequate to the potentialities of the computer. Modern computers, therefore, transfer data to magnetic tapes or drums or to magnetic core or flip-flop registers: temporary storage devices capable of releasing data to the computer at high-speed regardless of the speed at which the data was originally introduced.

d. In all of the systems considered above, data is, in a sense, prepackaged; i.e., offered in a form most suitable to the operation of the machine. Under these circumstances a comparatively simple Input System suffices. However, the AN/FSQ-7 Combat Direction Central is not an isolated machine; it is part of the SAGE Complex. This relationship imposes a special set of operational requirements on the Central and on its Input System, which must, specifically, be adequate to the following conditions:

1) Input data originates at distant points and is transmitted to the Combat Direction Central over phone lines. The data format and rate of transmission is established by phone-line characteristics, not by the characteristics of the computer.

2) Input data is of several types. Each type originates at many sources. The computer must be capable of processing data of all types and from all sources.

3) The types and densities of data traffic are determined by the tactical situation, not by computer requirements. The Input System must accept all data, make the necessary discernments as to its validity, process it, store it temporarily, transfer it according to certain priority specifications, etc. The result of these steps, the "product" of the Input System, is analogous to the prepackaged input to more conventional computers. The Input System might also be thought of as a digital computer feeding another digital computer.

e. The Input System of the AN/FSQ-7 Combat Direction Central receives three types of data:

1) Long-range radar input (LRI): data from long-range radar (P) sites.

Prime

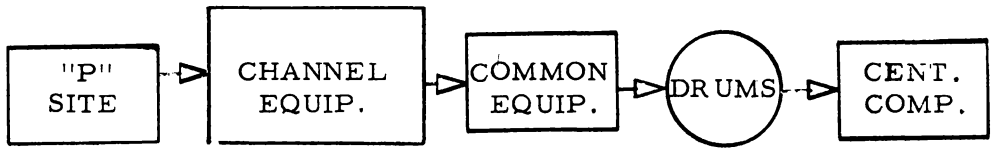
2) Gap-filler input (GFI): data from gap-filler sites, supplementing the long-range radar sites.

3) Crosstell (XTL): data from other Combat Direction or Combat Control Centrals.

These three types of data are processed by the LRI, and XTL elements, respectively. In addition, the Input System includes a LRI monitor associated with the LRI element and a test pattern generator (TPG) used to test the three elements.

C. LRI Data Flow

1. Block Diagram - Over-all



a. P Site - LRI site

1) Target detected

a) Up Graded

1) MTI
2) FGD
3) Mapping

2) Message generated
3) Message transmitted

b. Channel equipment

1) Message received and processed
2) Temporary storage

c. Common equipment

1) Provide transfer path from channel to drum.

d. Drums - Storage

e. Computer - Final processing

2. P Site

a. Radar equipment

1) Search radar (Fine Grain Data - FGD) See 3 p. 3070

   a) Range 200 miles
   b) 1/4 mile increments
   c) Azimuth increments Approx..1°

2) Mark X equipment

   a) Sends out a signal which when received by aircraft equipped with MK X causes that equipment to return a coded message to the land-based MK X set. The coded message identifies the aircraft as friendly.

   b) The indication of a friendly aircraft is sent to the AN/FST-2 where it is combined with the Search Radar return on that aircraft to make-up a complete MK X Radar message.

3) Height finding radars

   a) Two at each P site
   b) Each covers 180° of terrain
   c) Output upon request - either Computer or Manual.

b. Computer equipment - AN/FST-2 (at P site)

1) Beam splitting

   a) Enables azimuth of search radar to come in 0.1° increments.

2) Convert radar returns to binary information.

3) Controls transmission sequence of messages over two outputs. One output it sends MK X and Search Radar messages and on the second it sends MK X, Search, and Height Finder radar messages with Height messages having priority.

4) Temporary storage awaiting transmission.

5) Combines MK X inputs with Search Radar to give a MK X Radar message.

c. Transmission equipment - DDT's

1) Digital Data Transmitters

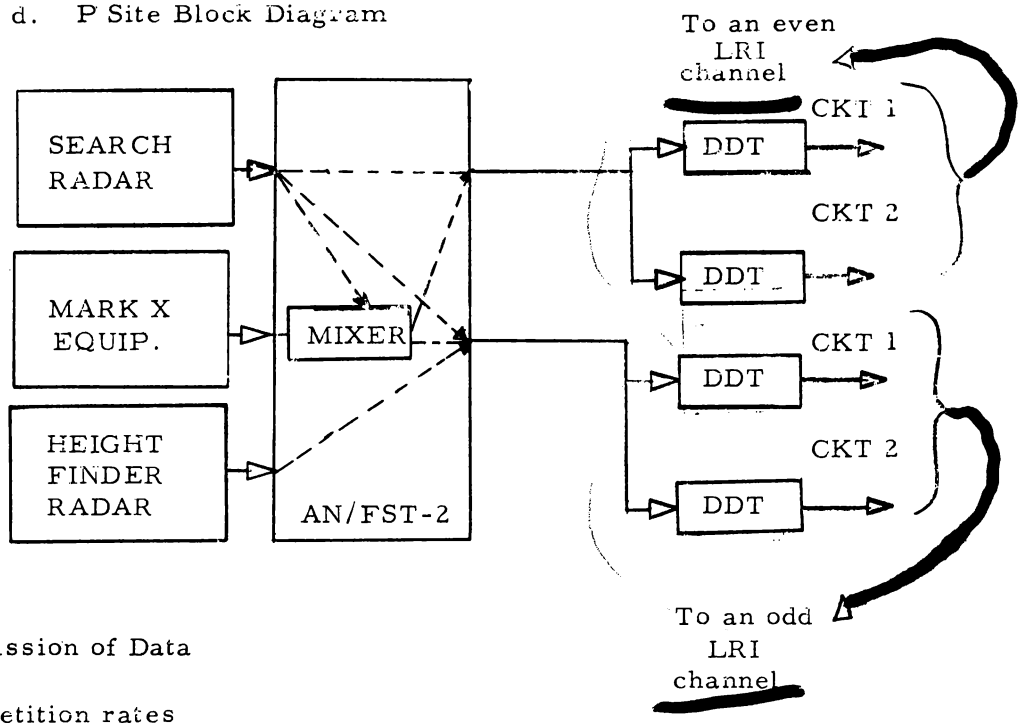
a) Amplitude modulation of a carrier

2) Phone Lines

a) Messages sent over two phone lines - for reliability - Circuit 1 and 2. 4 lines 2 per Channel

b) May be sent over one line only to a site if data from this radar is necessary during an emergency. Then the phone line would be Circuit 1.

d. P Site Block Diagram



D. Transmission of Data

1. Repetition rates

a. "Timing" pulses

1) Every 1/1300 sec. - 770 usec.
2) Continuous transmission

b. "Data" pulse

1) Random
2) Represents a "1"
3) Co-incident with and in place of a timing pulse
4) Twice the amplitude of timing pulses.

c. "Sync" pulse

1) Represents a timing control.
2) Every 52/1300 sec. - 40 M Sec.
3) Transmitted whether data is present or not.
4) Three times the amplitude of timing pulses used to synchronize in our equipment, also in tel. equipment to set AGC level.

2. One P site supplies information for 2 LRI channels normally a pair (an odd and even).

a. Two different messages may be transmitted simultaneously.

b. One of the two channels will receive any of the three message types - odd channel.

c. Other channel will not receive HF messages - other two message types only - even channel.

E. Phone Line and Drum Words

1. Introduction to LRI Messages, Fine Grain Data message, Height Finder message and Mark X message all have the following makeup:

a. Total of 52 bits
b. Sync first
c. Two zeros
d. Busy-bit - indicates a message being transmitted - always a 1 - no message, no busy bit.
e. Twenty-two data bits
f. Parity count of first 22 bits (even)
g. Twenty-two data bits
h. Parity count of second 22 bits (odd)
i. Two zeros
j. Sync of next message

2. Introduction to LRI Drum Words

a. Drum word one

1) Parity odd
2) Contains site ID plus data from message word 2.

b. Drum word two

1) Parity odd
2) Contains clock time plus data from message word 1.

c. Input word terms explained

d. Site identity bits

1) R12-R15 of Drum Word One
2) Binary coding identifying source of message.

e. Clock Time Bits

1) R1-6 of Drum Word Two
2) Binary count indicating the time at which the message was written on the drum.

3. Analysis of LRI Search Data

a. Long-range search radar data is upgraded at the radar site by these processes: moving target indicator (MTI), fine-grain data (FGD), and manual mapping.

b. The MTI apparatus endeavors to eliminate all radar returns except those produced by a moving object.

c. Fine-grain data apparatus uses the technique of beam-splitting to achieve a much higher degree of azimuth resolution when locating a target than is possible with conventional radar. (Beam-splitting notes the azimuths at which the first and last radar returns are received from a target during one sweep and then computes the average or middle azimuth. The disadvantage of beam-splitting -- the time delay between initial detection of a target and the reporting of the averaged azimuth -- is overcome by noting the duration of the delay in the LRI message). Fine-grain data apparatus also tends to reject noise by establishing minimal criteria for an acceptable target.

d. Finally, manual mapping is used to eliminate unwanted radar returns which have survived the other filtering techniques. In manual mapping, targets are presented on a display screen and an operator uses an opaquing

fluid to blot out those targets or areas which are of no tactical significance. Un-opaqued target indications are picked up by a photoelectric device, and generate descriptive messages for transmission to the Combat Direction Central. These messages contain the following information:

1) Target range from the radar set

2) Target azimuth with respect to true north from the radar set.

Note: Refer to Page 0090 for Message Layout

3) Time delay between initial detection of target and transmission of message.

4) Run length, indication of size of target or existence of multiple targets at reported location.

5) Message label which identifies the message source as search radar rather than IFF or height finder.

e. It is the function of the LRI common and channel equipment to change the message makeup into the two drum words.

4. Analysis of Mark X Data

a. The MK X IFF radar beacon enables radar systems to distinguish between friendly and hostile aircraft. Friendly aircraft carry transponders (receiver-transmitters) which reply in a prescribed code when interrogated by a ground interrogator (transmitter-receiver). The response is usually displayed alongside the radar return, indicating to the operator that the target is friendly.

b. The MK X IFF radar beacon sends messages to the Direction Central which contain the following information in binary form:

Note: Refer to Page 0110 for Message Layout

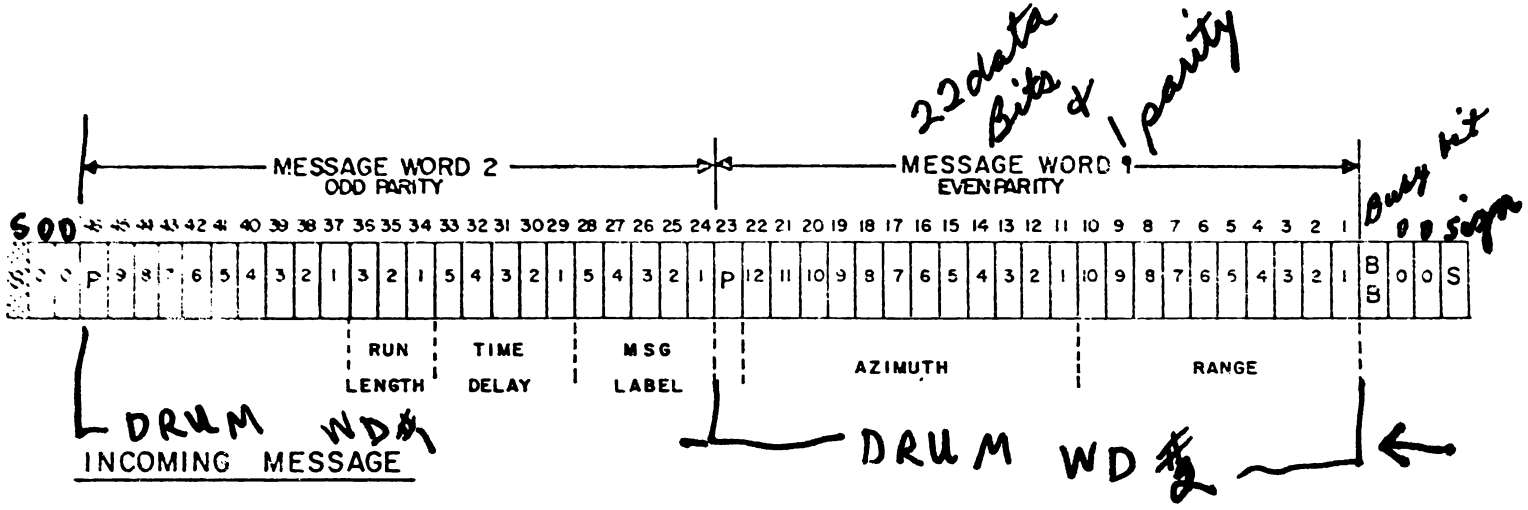
1) Target range from the radar set

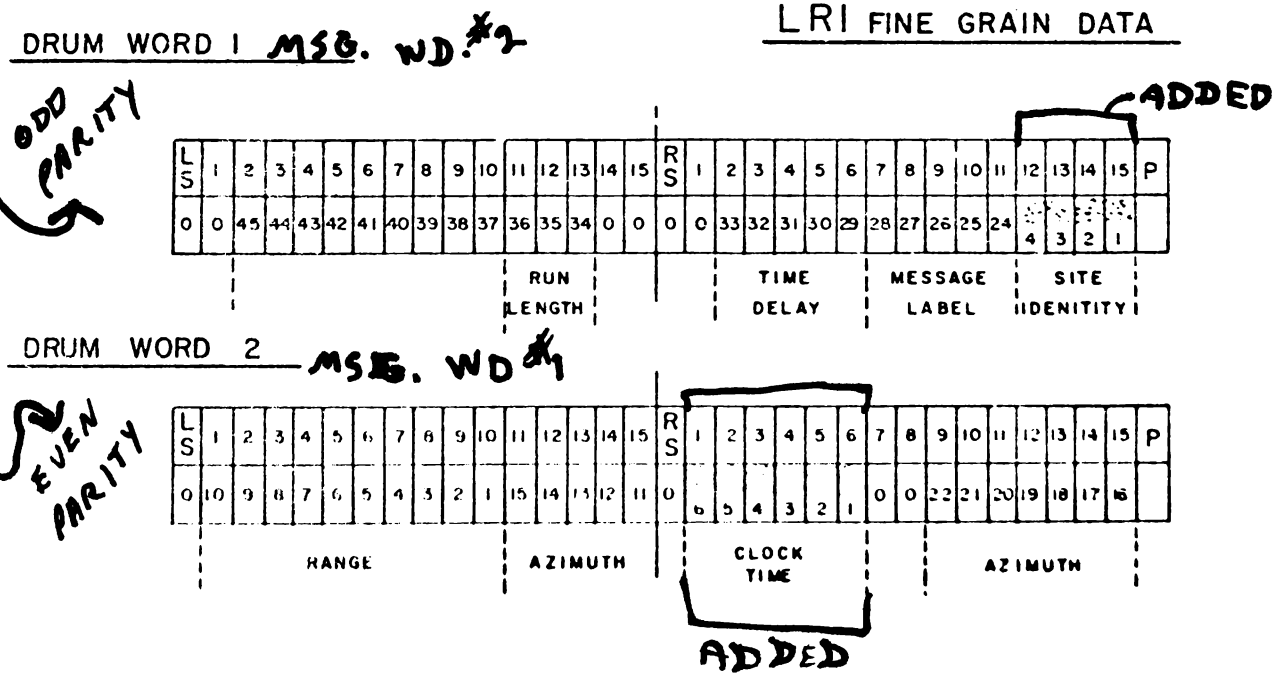
2) Target azimuth with respect to true north from the radar set.

0090

SEARCH

OVERALL EVEN PARITY





3) Time delay between initial detection of target and transmission of message, up to 16 seconds, with an accuracy of 1/4 second.

4) Security identification feature (SIF), if used.

5) Message label which identifies message source as IFF rather than search radar or height finder.

c. In order to obtain a simultaneous report of the MK X IFF response with the radar report of the target, the MK X set and its associated radar are synchronized, when sweeping, in azimuth and range. This synchronization allows the MK X IFF to generate range and azimuth information on friendly targets by noting the radar azimuth when a response is received and the time between interrogation and response. The IFF range and azimuth data is in FGD form.

d. The LRI channel and common equipment will convert the message into the two drum words illustrated on Page

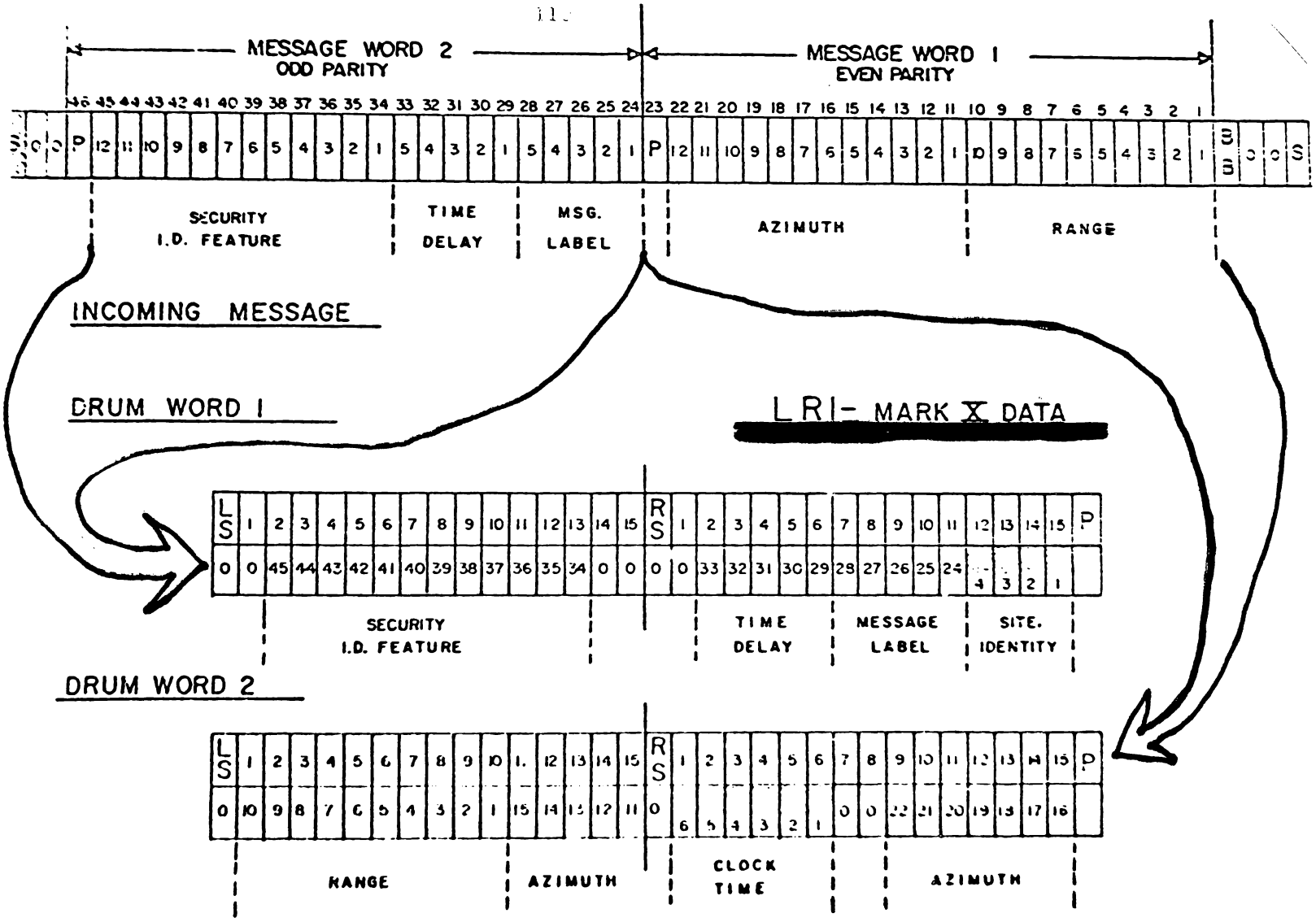
5. Analysis of Height Finder Data

a. The height-finder radar equipment associated with a P-site supplies target-height data on specific targets to the Combat Direction Central in response to requests received from the Central. The height-finder radars are semiautomatic; that is, the radar antenna is automatically positioned to the azimuth of the target for which height information is requested. In addition, the range cursor on the range-height indicator is automatically positioned at target range. The last measured or estimated height is also supplied to the height-finder operator to aid in identifying the target. New target height determined by the height-finder is automatically encoded and sent to the DC as part of the height-finder request. The height-finder message contains the following information in binary form:

1) New target height.

2) Predominate formation of multiple targets.

Note: Refer to Page 0130 for Message make-up.


MESSAGE WORD 2
ODD PARITY
MESSAGE WORD 1
EVEN PARITY
SECURITY I.D. FEATURE
TIME DELAY
MSG. LABEL
AZIMUTH
RANGE
INCOMING MESSAGE
DRUM WORD 1
LRI - MARK X DATA
SECURITY I.D. FEATURE
TIME DELAY
MESSAGE LABEL
SITE. IDENTITY
DRUM WORD 2
RANGE
AZIMUTH
CLOCK TIME
AZIMUTH

3) Separation between aircraft in multiple targets.

4) Number of aircraft in multiple targets.

5) Request number.

6) Address identifying which of two height-finders is replying.

7) Special reply (if any).

8) Message label which identifies the message label as height-finder rather than search radar or IFF.

6. Analysis of GFI Data

a. The mapping of the gap filler radar will be done at the "P" site. The gap filler information will then be fed into the A/N FST-2 where it will be sent to the LRI, input equipment.

b. The incoming GFI message has a 52 bit format, as in all messages coming to the LRI element. The message consists of the gap filler number, range and azimuth of the target and message label.

c. Maximum of six GFI sites per "P" site.

Note: Refer to Page 0150 for Message make-up

F. Physical Layout of Unit Number 41

1. Channel equipment

a. 36 channels

1) Numbered 1 thru 36
2) 9, 10, 27 and 28 are spares

b. Two channels per module

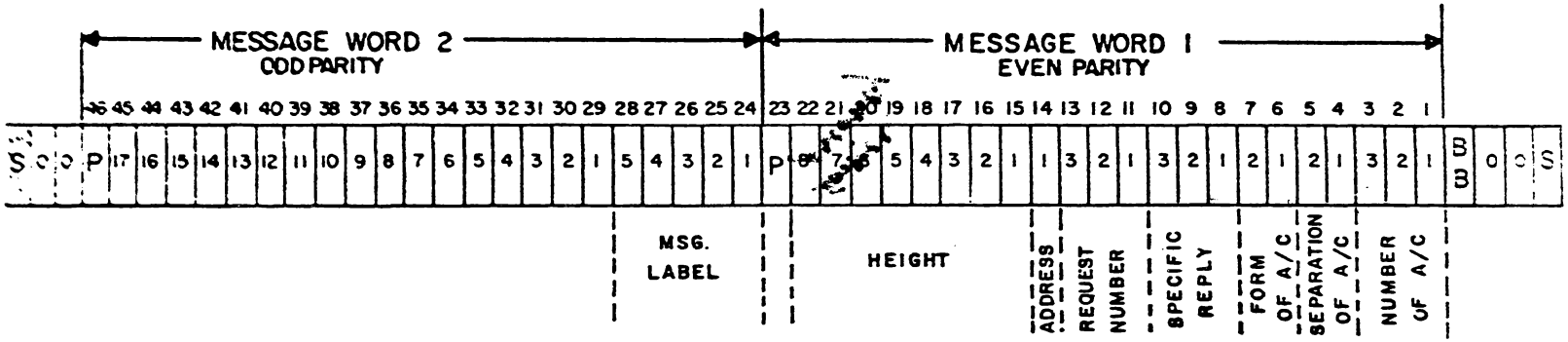
2. Common equipment

a. Two commons

1) Common A for Computer A
2) Common B for Computer B

b. Three modules per common.

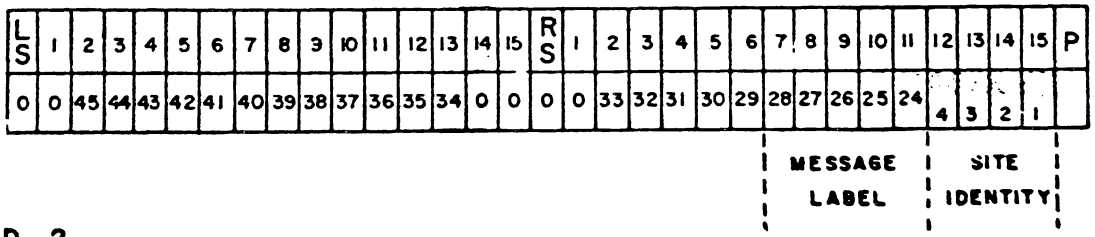
R to L



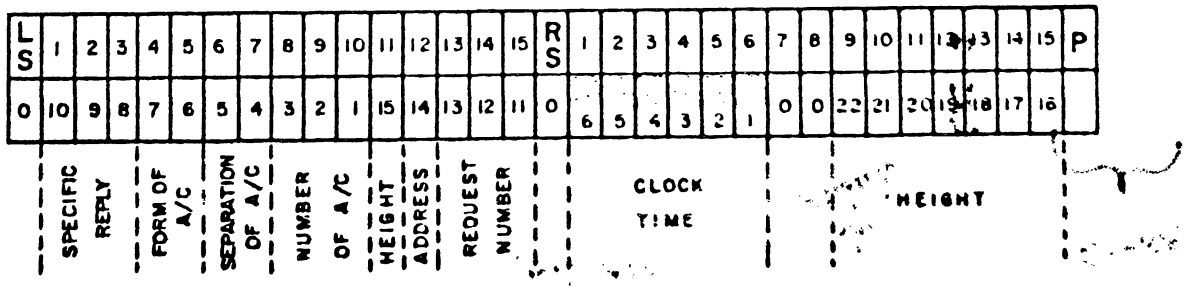
INCOMING MESSAGE

DRUM WORD 1

LRI HEIGHT FINDER



DRUM WORD 2



0130

3. Channel assignment

   a. Channels 1-18 supply data for LRI-1 field
   b. Channels 19-36 supply data for LRI-2 field
   c. Channel 9 is spare for 1, 3, 5, 7, 11, 13, 15 & 17
   d. Channel 10 is spare for 2, 4, 6, 8, 12, 14, 16 & 18
   e. Channel 27 is spare for 19, 21, 23, 25, 29, 31, 33 & 35
   f. Channel 28 is spare for 20, 22, 24, 26, 30, 32, 34 & 36

4. Module Assignment for Unit 41

LRI 1 Module	Channel	LRI 2 Module	Channel
A	1-2	N	19-20
B	3-4	P	21-22
C	5-6	R	23-24
D	7-8	S	25-26
E	9-10	T	27-28
J	11-12	X	29-30
K	13-14	Y	31-32
L	15-16	AA	33-34
M	17-18	BB	35-36
G		F	
H	Common A	V	Common B
U		W	

G. LRI Controls on Simplex Maintenance Console

1. Function of Simplex Maintenance Console

   a. Maintenance control of simplexed portions of Input System.

   b. A control panel provided for each channel of inputs.

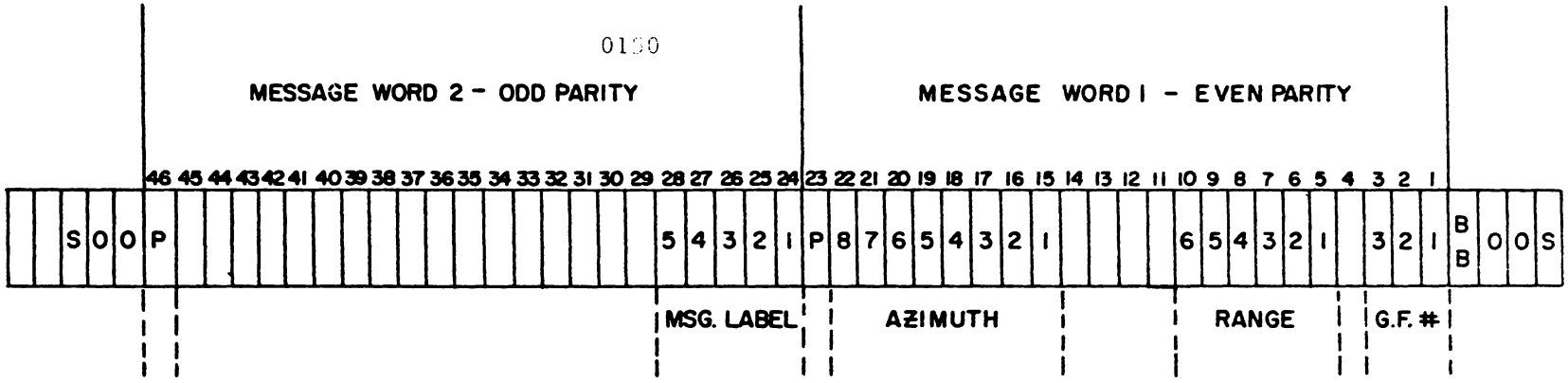
   c. Control of input test pattern generators.

2. Long Range Inputs

   a. One panel for each 36 channels.

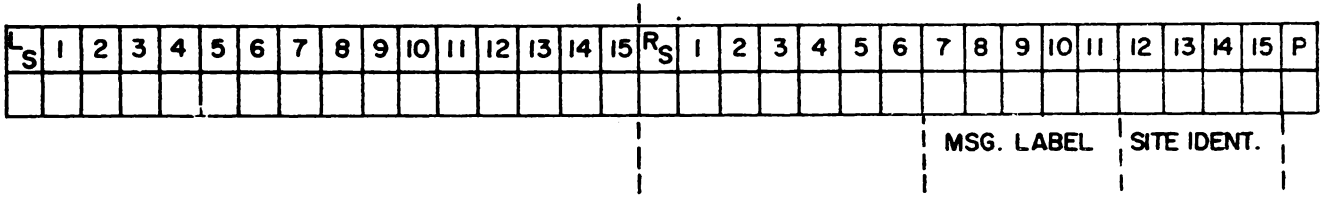
   b. Bottom half of modules C thru H.

   c. Each module in Unit 41 (LRI) contains two channels.

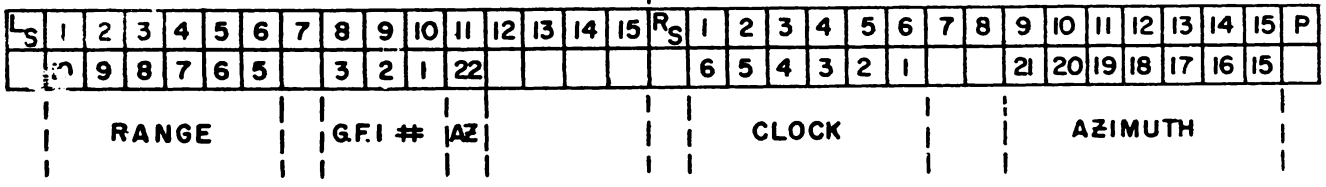


GFI DRUM WORD

DRUM WORD 1



DRUM WORD 2



d. Status of both channels in a module is controlled by the Unit Status switch on the Odd Channel control panel.

e. The Spare channels always replace a channel pair: that is, one LRI module.

3. Long Range Panel Controls

a. Associate indicator or control with panel location.

b. Include the following:

1) Channel Ready set alarm - will not be cleared by "Clear Alarm" - there will be no audible alarm. The Channel Ready 1 neon is now in the upper left-hand corner of the Alarms and no longer in the bottom neon panel.

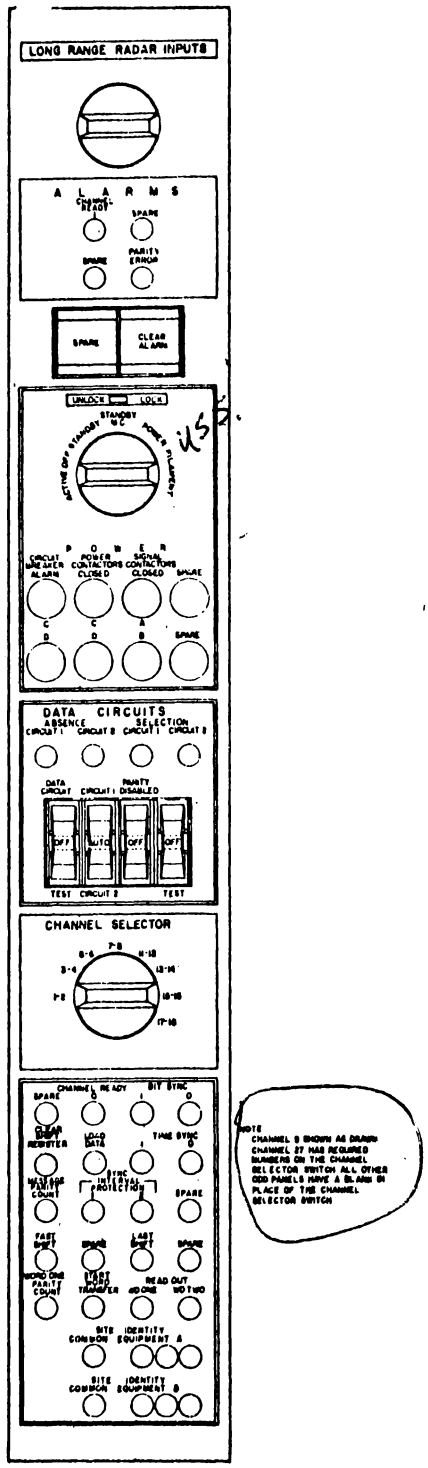
2) Channel Ready switch - allows a readout protection circuit to be tested. Located in the position of the blank switch in Data Circuits panel.

c. Flip-flop neons will not be discussed at present. They will be discussed later when their function is known.

H. Introduction to the Long-Range Radar Input Monitor

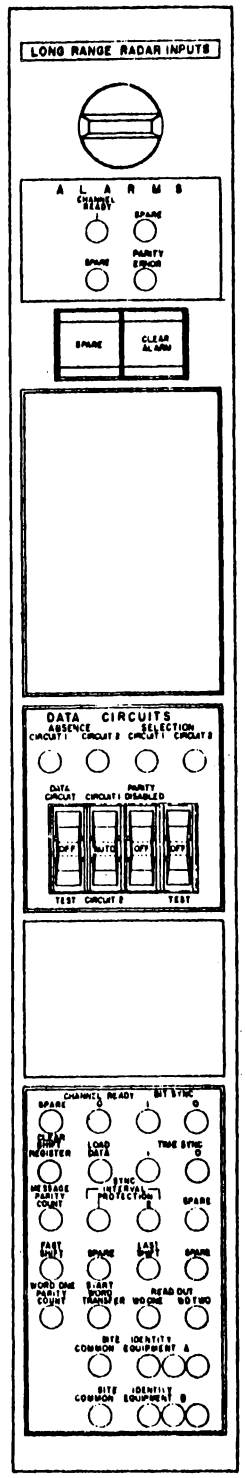
1. LRI messages in transit to the Drum System are also made available to the LRI monitor. The LRI monitor provides the means for selecting LRI data for display. It thus enables operating personnel to make preliminary analyses of LRI coverage and data independently of the Central Computer, and it assists maintenance personnel to evaluate the operational efficiency of the Input System.

2. The LRI monitor consists of three display consoles, units 620, 622, and 623, and the LRI monitor control unit, unit 93, which contains the circuits that serve all three consoles. LRI messages are selected for display by means of keyboard controls at the consoles or, in the case of units 620 and at an auxiliary control console, unit 953. The following selection principle is employed. Each processed LRI message contains a message label indicating whether the message contains search, MK X IFF, or height-finder data, and a site identity code (added in the drum input section) indicating the source of the data. An operator selects a message or messages for display by using the keyboard controls to specify the message label.



NOTE
CHANNEL 0 SHOWN AS DRAWN
CHANNEL 27 HAS REQUIRED
NUMBERS ON THE CHANNEL
SELECTOR SWITCH ALL OTHER
ODD PANELS HAVE A BLANK IN
PLACE OF THE CHANNEL
SELECTOR SWITCH

LRI Control Panel, Odd and Odd-Spares



LRI Control Panel, Even and Even-Spares

and site identity of interest to him. The target information in the selected messages is then presented, in PPI form, on the cathode-ray tube (CRT) of the display console at which, or for which, the display was requested.

3. Functionally, the LRI monitor consists of four sections: digital, analog, display, and switching. The digital section accepts the LRI message, determines whether it has been selected for display by comparing its message label and its identity with requests expressed at keyboard controls, and begins the processing of the target information in selected messages. The analog section transforms the digital target information into analog form. The display section presents the target information in a PPI display on one or more of the CRT screens. The switching section contains the circuitry used to express message selections and to associate the consoles with either the active or the standby duplex machine.

I. Introduction to the Test Pattern Generator

1. General

a. Test Pattern Generator is provided to generate test signals simulating the phone-line inputs to the Input System. The equipment is essentially three test pattern generators serving the LRI, XTL, and GFI elements. By means of a switch associated with a channel, signals from the appropriate TPG may be substituted for the phone-line inputs to the particular channel by providing a known and controlled input to the various channels, the TPG offers the means of thoroughly checking the operation of an element during installation and subsequent to it.

2. Test Signals

a. The test signals generated by the LRI TPG go out on three lines: timing, sync, and data. The timing signal is a continuous 1,300-cps sine wave. The sync and data signals are individual sine waves generated in synchronism with the timing signal, together they form the message, the composition of which may be varied manually or by computer command.

J. Input Switching

1. Introduction

a. A block diagram illustrating the flow of LRI data from a P site to the LRI drum field is shown on Page 0200 The data flow for all 16 P sites is identical to that illustrated for the single P site.

b. A radar P site contains three radar units, each originating different information:

1) A long-range search radar set producing target coordinate information in fine-grain data (FGD) form.

2) Mark X identification friend or foe (IFF) radar with a selective identification feature.

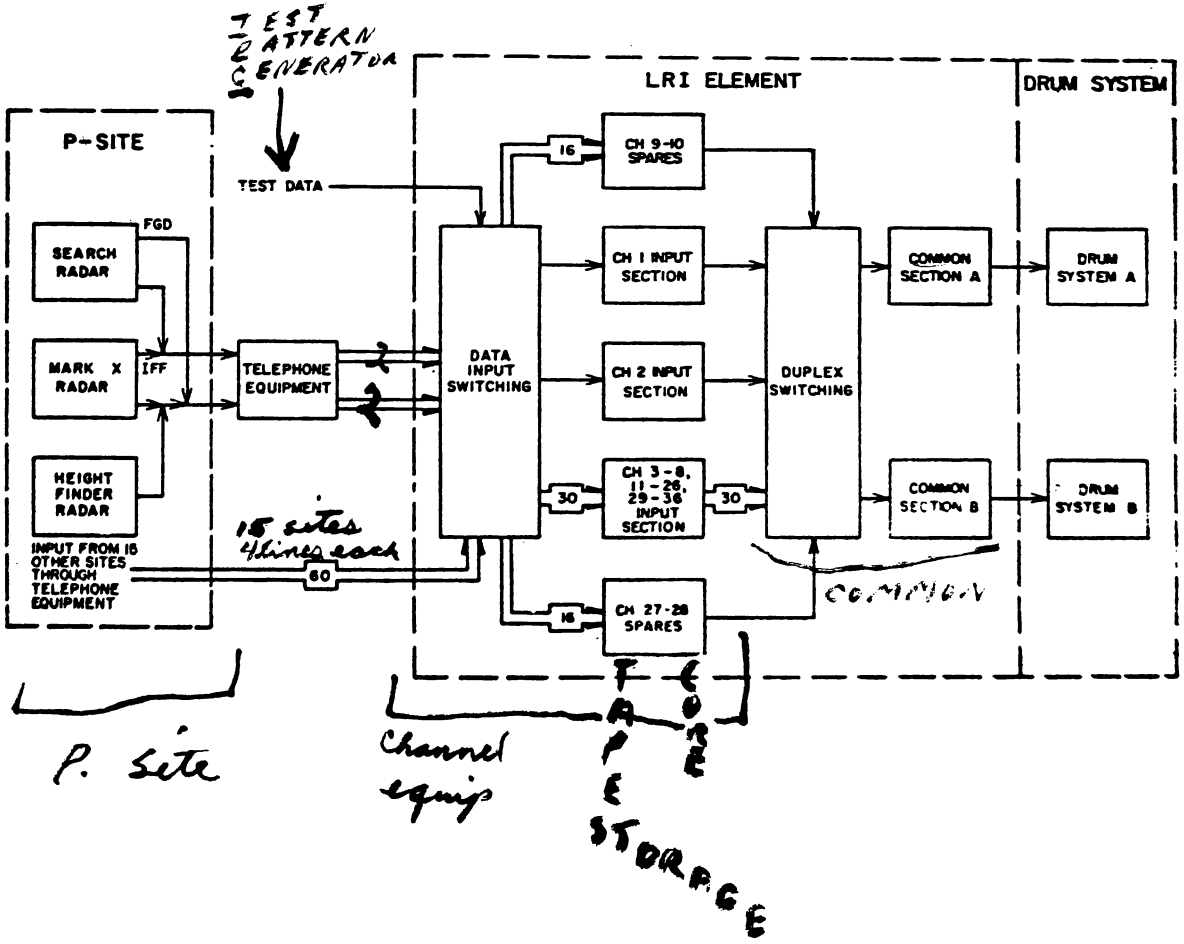
3) A semiautomatic height-finder radar producing height-above ground data for each target.

In normal operation, as shown on Page 0200 each P-site sends data to two LRI channels. The two channels will be an odd and even pair such as channels 1-2, 3-4, 29-30, or 35-36. The data sent to one of the two channels will be search radar and Mark X information. All three types of messages are sent to the other channel. The output of the P-site intended for an odd channel is sent to two digital data transmitters (DDT's) and is then transmitted over separate phone lines to the Central. Therefore, an odd channel receives identical information over two input lines (designated circuit 1 and circuit 2). Similar circuitry exists for the even channel to receive information.

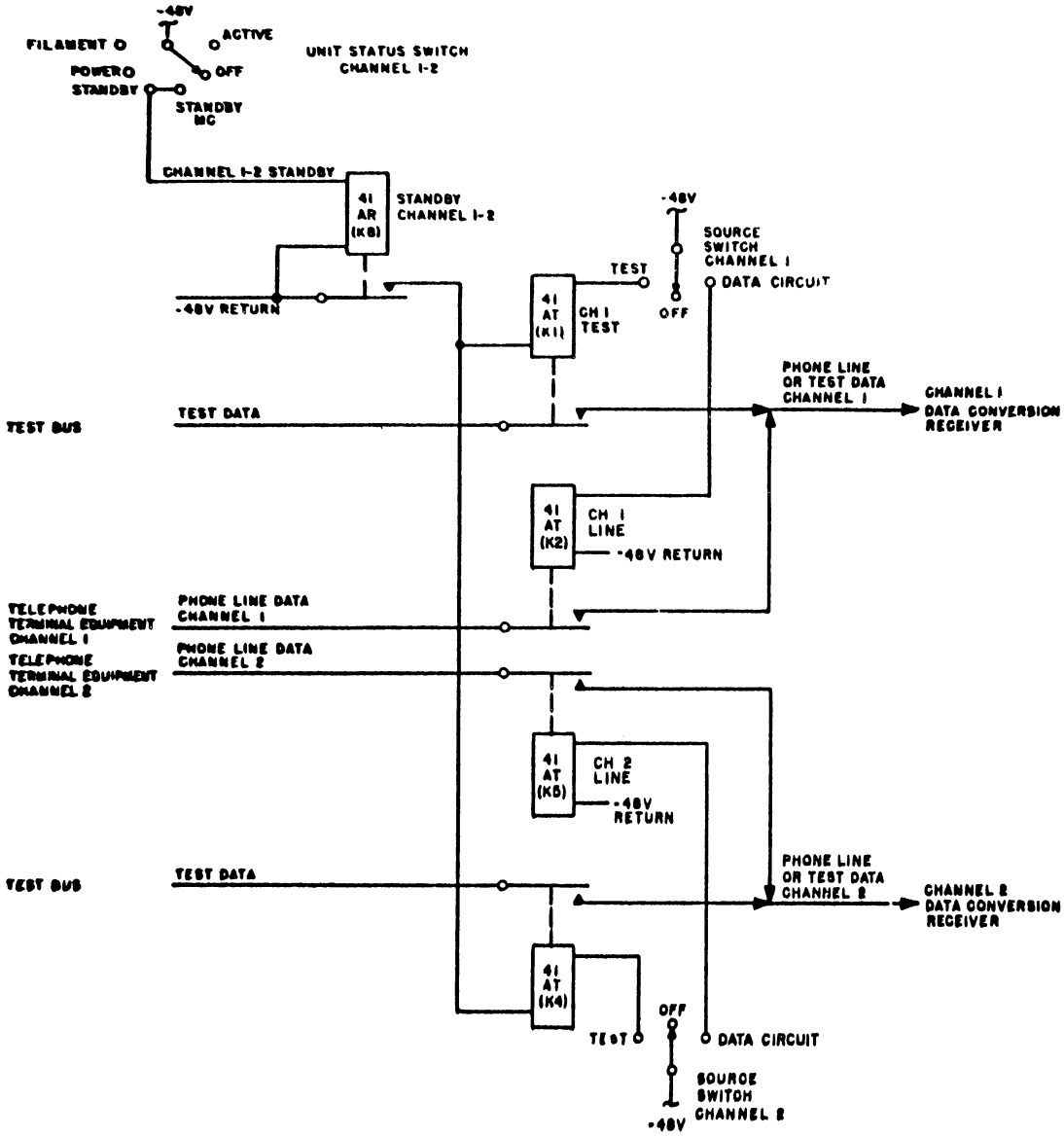
Input Data Switching

1) The data-input switching circuit selects either telephone line data or test signals from the LRI TPG as the inputs to be directed to each LRI channel. Page 0210 shows the relay switching circuits involved in selecting the input for channels 1 and 2. The relay switching circuits for any other pair of channels (except for spare channels) is the same as that shown for channels 1 and 2. For this reason, only channels 1 and 2 are discussed here.

LRI INFORMATION FLOW, SIMPLIFIED DIAGRAM



0200


-48V
FILAMENT
ACTIVE
POWER
OFF
STANDBY
STANDBY MC
UNIT STATUS SWITCH CHANNEL 1-2
CHANNEL 1-2 STANDBY
41 AR (K8)
STANDBY CHANNEL 1-2
-48V RETURN
-48V
SOURCE SWITCH CHANNEL 1
TEST
DATA CIRCUIT
OFF
41 AT (K1)
CH 1 TEST
PHONE LINE OR TEST DATA CHANNEL 1
CHANNEL 1 DATA CONVERSION RECEIVER
TEST BUS
TEST DATA
41 AT (K2)
CH 1 LINE
-48V RETURN
TELEPHONE TERMINAL EQUIPMENT CHANNEL 1
PHONE LINE DATA CHANNEL 1
TELEPHONE TERMINAL EQUIPMENT CHANNEL 2
PHONE LINE DATA CHANNEL 2
41 AT (K5)
CH 2 LINE
-48V RETURN
TEST BUS
TEST DATA
PHONE LINE OR TEST DATA CHANNEL 2
CHANNEL 2 DATA CONVERSION RECEIVER
41 AT (K4)
OFF
TEST
DATA CIRCUIT
SOURCE SWITCH CHANNEL 2
-48V

When the channel 1 source switch (located on the simplex maintenance console) is set to the DATA CIRCUIT position, relay 41AT(K_2) is energized and the telephone line inputs are connected to the data conversion receiver in channel 1. The telephone line inputs and test data inputs consist of data, sync, and timing lines, but, for simplicity, shown on Page 0210 as a single line.

When relay 41AT(K1) is energized, test data is connected to the data conversion received in channel 1. In order for this relay to be energized, two conditions must be met: (1) The unit status switch for channels 1 and 2 must be in the STANDBY or STANDBY MC position so that standby relay 41AR(K8) is energized. This relay controls the -48V return line for channel 1 test relay 41AT(K1) and channel 2 test relay 41AT(K4).

2) The source switch for channel 1 must be in the TEST position so that the control voltage will be applied to the channel 1 test relay.

The purpose of the standby relays is to prevent test signals from being sent to the active computer. The inputs for channel 2 are selected in the same manner as described above for channel 1.

d. Spare-Channel Switching

1) Spare-channel switching is the operation of electrically substituting a pair of spare channels (channels 9 and 10 or channels 27 and 28) for a pair of channels within a group. It is accomplished by setting the CHANNEL SELECTOR switch (on the ODD spare channel control panels, simplex maintenance console) to the numbers of the channels to be replaced. Three functions are thereby performed.

a) The alternate telephone circuit for the replaced channel is connected to the spare channel.

b) The telephone-terminal-equipment indicators of the spare channel are substituted for these indicators on the replaced channel.

c) A write level generated in a spare channel is applied to the site can for the replaced

channel. A write level causes readout of site identity by a site can to associate the source of a message with the message data. In spare-channel switching it is necessary to associate the site identity related with the replaced channel with message data processed by the spare channel.

2. Logic Analysis of Input Switching

   a. Requirements to be met:

      1) The two channels of module must have same status.
      2) Test data cannot be fed to an "Active" channel.
      3) Each channel can select data independent of its sister channel.
      4) A channel being replaced by a spare also has its sister channel replaced by a spare.

K. Summary Questions

1. How many different types of messages are used in LRI? Name and discuss each type briefly.

2. How many azimuths in the LRI circle?

3. What is the size of an LRI increment (range and azimuth)?

4. How many binary bits are necessary to make up the maximum LRI azimuth count? How many bits are necessary to make up the maximum LRI range count?

5. What is the difference between FGD and Mark X Azimuth and Range counts?

6. At what frequency does LRI data arrive at the DCR's?

7. Are sync bits received by the LRI channel equipment when no data is being received? When consecutive messages are being received at what rate do the sync bits arrive?

8. Explain the parity make up of the two message words to result in the desired telephone line parity. Will this parity need to be changed before data is written on the LOG Drum?

9. If consecutive FGD messages are being received by an LRI channel, what is the time elapse between the last data bit of one message and the first data bit of the following message? (Consider parity as data)

10. Does a Height Finder message contain Range and Azimuth?

11. What is meant by "Run Length?"

12. Give the bit length of each type of LRI message. How many of these bits actually contain information for the computer?

13. What is the LRI unit number?

14. What is the maximum number of LRI channels for one computer? Which channels are spares?

15. Is LRI simplexed or duplexed equipment?

16. What LRI information is written on LRI Field #1? LRI Field #2?

17. How many phone lines are used to transmit data from one LRI site to the computer? How many of these are spares?

18. Channel 19 can transfer data to which of the 4 LRI drum fields?

19. The 10th data bit received on the phone line goes to which bit of which drum word for a FGD message? MK X message? HF message?

20. Which incoming data bits indicate type of message?

21. Which channels can be replaced by Channel 28?

22. Referring to Logic S2.4.1

    Make a point to point wiring diagram of "Sync" line from Channel #13 on alternate phone line #11 to channel #9 input.

    Specify which relays must be energized.

    List the conditions necessary to pick each of the relays.

    Ignore channel 10 and channel 14 relays as well as all other channel relays.

Information

II Review of Tape Core Theory

NOTE: Tape core theory and special circuits used with tape cores was covered in Basic Circuits and also in the GFI Course. Refer to Basic Circuit Manuals or the MRD Manual for additional circuit information.

A. Introduction to Tape Cores

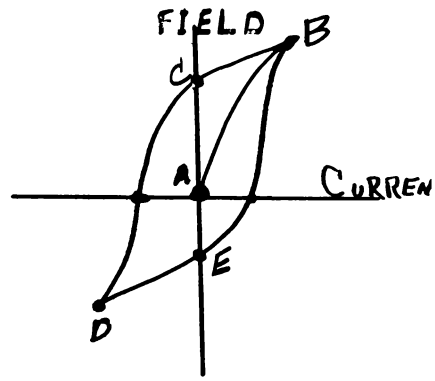
1. A special circuit.
2. A magnetic storage device capable of storing one bit.
3. Various applications require minor alterations.
4. Models used in LRI will be discussed here.

B. Physical Description

1. A small bobbin (ceramic) wound with a magnetic alloy tape.
2. Coils of wire wound through center.
3. Number of turns per winding and number of windings varies with application.

C. Theory of Operation

1. Hysteresis Loop



a. Originally at Point A.

(1) No current.
(2) No field.

b. Current applied to winding of + polarity.

(1) Field goes to B.

c. Current Removed.

(1) Current to 0.
(2) Flux to C - slight decrease from B.

d. Current Reversed.

(1) Large change of field.
(2) Changes polarity.
(3) Field to point D.

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e. Current Removed.

(1) Current to 0.
(2) Flux to E - slight decrease from D.

f. Current Reversed.

(1) Large change of field.
(2) Changes polarity.

2. Squareness of loop depends upon ability of core to retain magnetism.

a. When at point C - a "1" is stored.
b. When at point E - a "0" is stored.

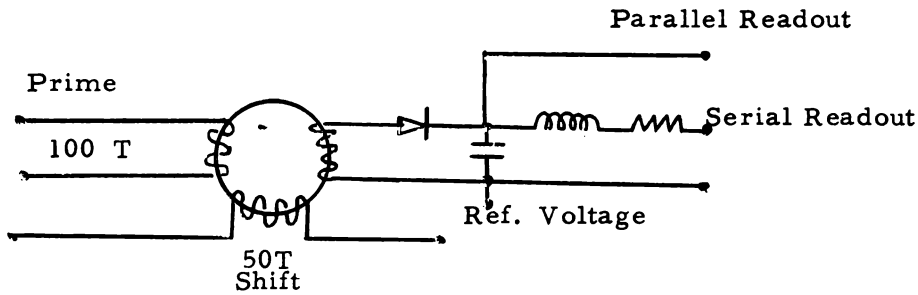
3. Core is primed by passing a current through a "prime" winding.

4. Core is sensed for a "1" by passing a current through a "reset or drive or shift" winding which switches the core to "0".

5. When core goes from a "1" to a "0", a sizeable change in flux takes place.

6. If core was already at "0", flux change is slight.

D. Core shift - Model C



1. Definition

a. A core shift (CS) is a logic circuit which possesses two stable states of magnetization and is used as a storage device.

Information

b. There are 15 models of CS's utilized in AN/FSQ-7 and -8 equipments. The most significant differences between each model are in the number of windings used and the number of turns in each winding. The basic CS contains three windings: an add-in (or read-in) winding, a readout winding, and a drive winding. All other CS's contain a fourth winding, the reset winding. In addition, several models contain a fifth winding, either inhibit or feedback, depending on its application in a circuit. Basically, the principles of operation for all CS's are identical. For this reason, only the basic CS is described in detail below.

2. Prime Winding

a. Input is from various sources.

(1) Another cCS (serial readout.
(2) A core prime.
(3) Cathode follower.

b. Suitable current for a duration of time are main requirements.

3. Shift Winding

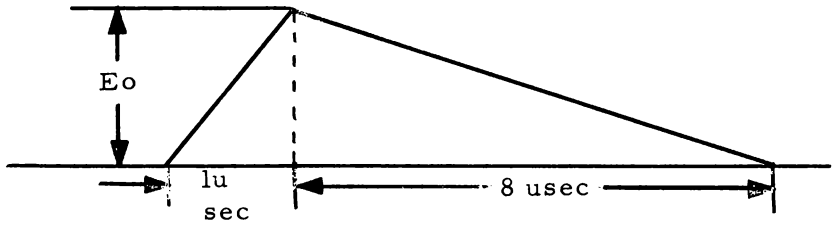
a. Normally from a CSD.
b. To shift bit to next core 2.5 usec. pulse.
c. To reset cores 7.5 usec. or longer.

4. Output Winding

a. Output voltage developed across capacitor.
b. Diode prevents capacitor discharging through output winding.
c. Reference voltage normally used is - 15V.
d. Parallel readout used to condition a GT.
e. Serial readout used to prime another core.

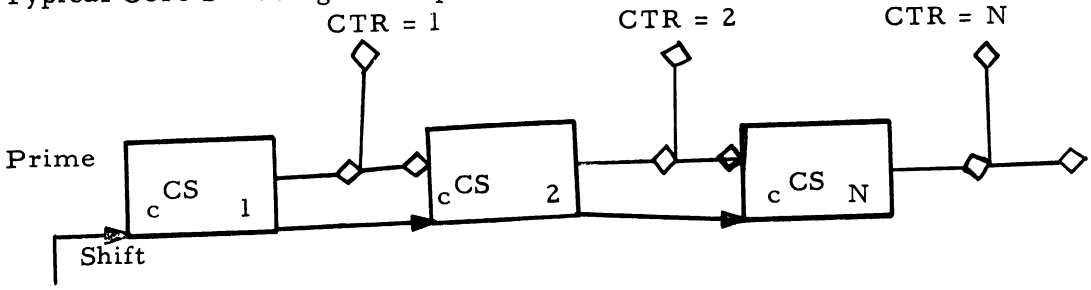
Information

5. Output Voltage



a. Eo = 25 to 35 volts for a "1".
b. Eo = 2.5 volts for a "0".
c. All values approx.

E. Typical Core Shift Register Operation



1. Core 1 is primed all other cores = 0.

2. First Shift

a. Clears core 1.
b. Primes core 2.
c. CTR = 1 output pulse.

3. Second Shift

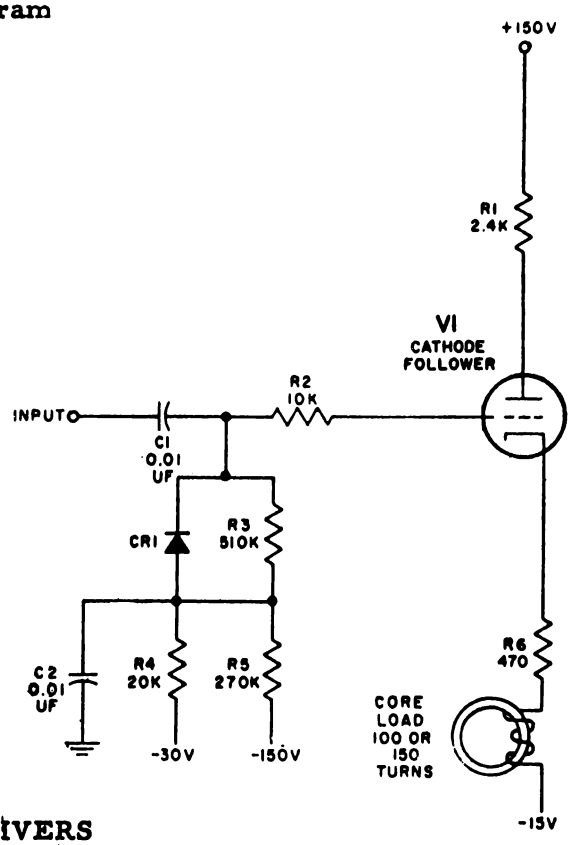
a. Clears core 2.
b. Primes core 2.
c. CTR = 2 output pulse.

4. N-th Shift

a. Clears core N.
b. Primes next core if there is one.
c. CTR = N output pulse.

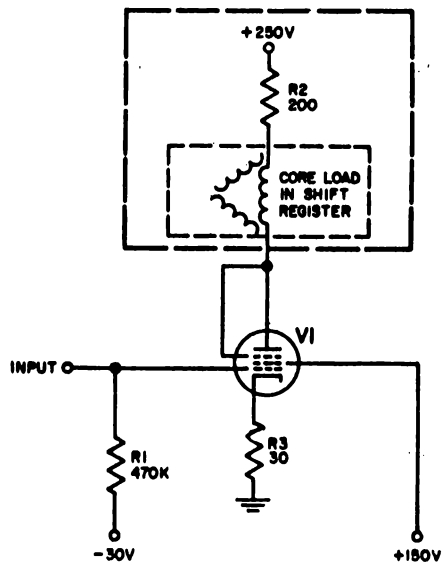
F. CORE PRIME, MODELS A,B,C, AND D

1. A core prime (CP) is a nonlogic power-amplifying circuit which provides a high current output pulse utilized to set a core shift to the 1 state.
2. Schematic diagram



G. CORE SHIFT DRIVERS

1. A core shift driver is a nonlogic circuit which provides the current necessary to transfer information serially through a register.
2. Schematic diagram



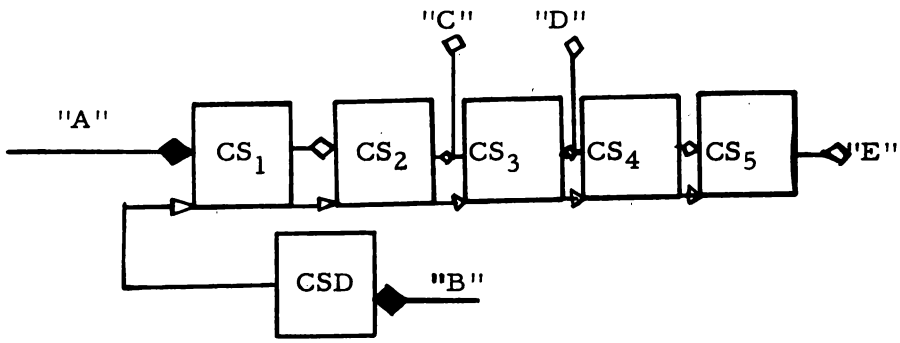
NOTES:

1. SERVICE VOLTAGES ARE DECOUPLED IN THE PLUGGABLE UNIT
2. PARASITIC SUPPRESSORS HAVE BEEN OMITTED

Information

H. Summary Questions

1.



Consider the above simplified core register. Assume CS_1 is primed for each "1" bit at input "A" and a shift pulse is applied to input "B" every 770 miscroseconds. The message to be shifted through is 473_8. Data bits are primed into CS_1 in correct sequence. Answer the following questions.

a. Will the levels at "C", "D" or "E" be up during the fifth shift pulse?

b. The output at "E" will equal what octal number?

c. The first "1" bit is shifted out at "E"; how many milliseconds after it entered at "A"?

d. The last "1" bit will give an output at "D"; how many microseconds after the first data bit was read out at "E"?

e. If a reset pulse is applied to "B" 12 milliseconds after the first shift pulse, what will be the outputs at "C", "D" and "E" ("1" or "0")?

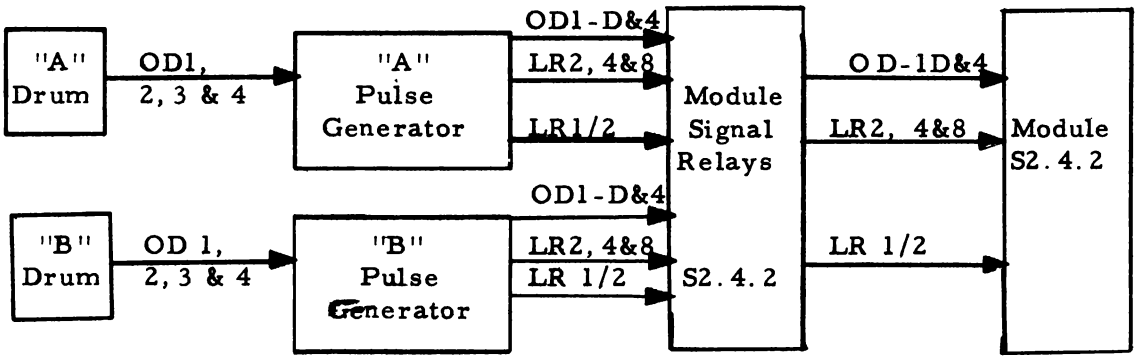
III. LRI Channel Operation

A. LRI Pulse Generation Circuitry

1. Purpose

a. Distribute drum timing pulses to channel equipment
b. Generate LRI pulses and distribute to channel equipment.

2. Block Diagram of Pulses



3. Circuit Analysis Logic A2.4.6

a. Inputs

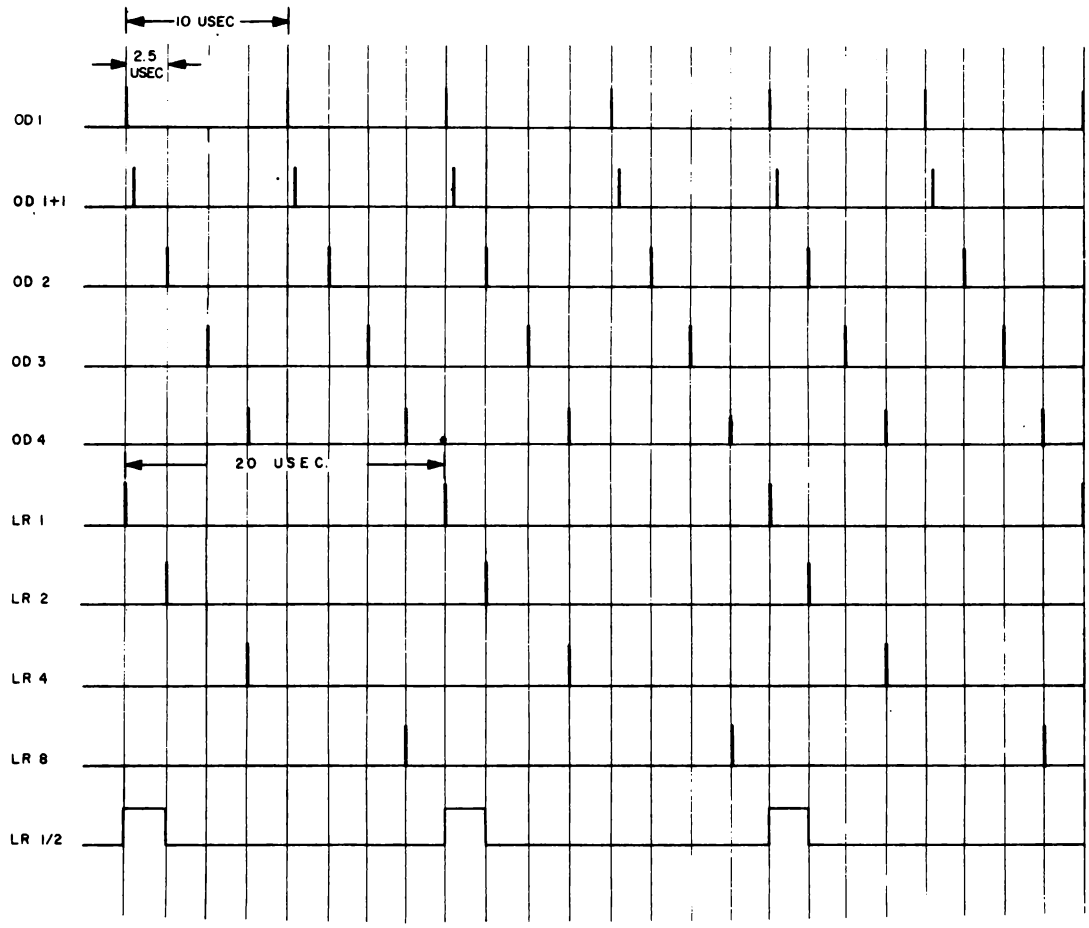
1. OD1 (12D)
2. OD2 (9D)
3. OD3 (12A)
4. OD4 (12D)

Note: Page 0350

b. Outputs

1. OD1-D (11E)
2. OD4 (12E)
3. LR2 (9E)
4. LR4 (9E)
5. LR8 (10E)
6. LR 1/2 (8E)

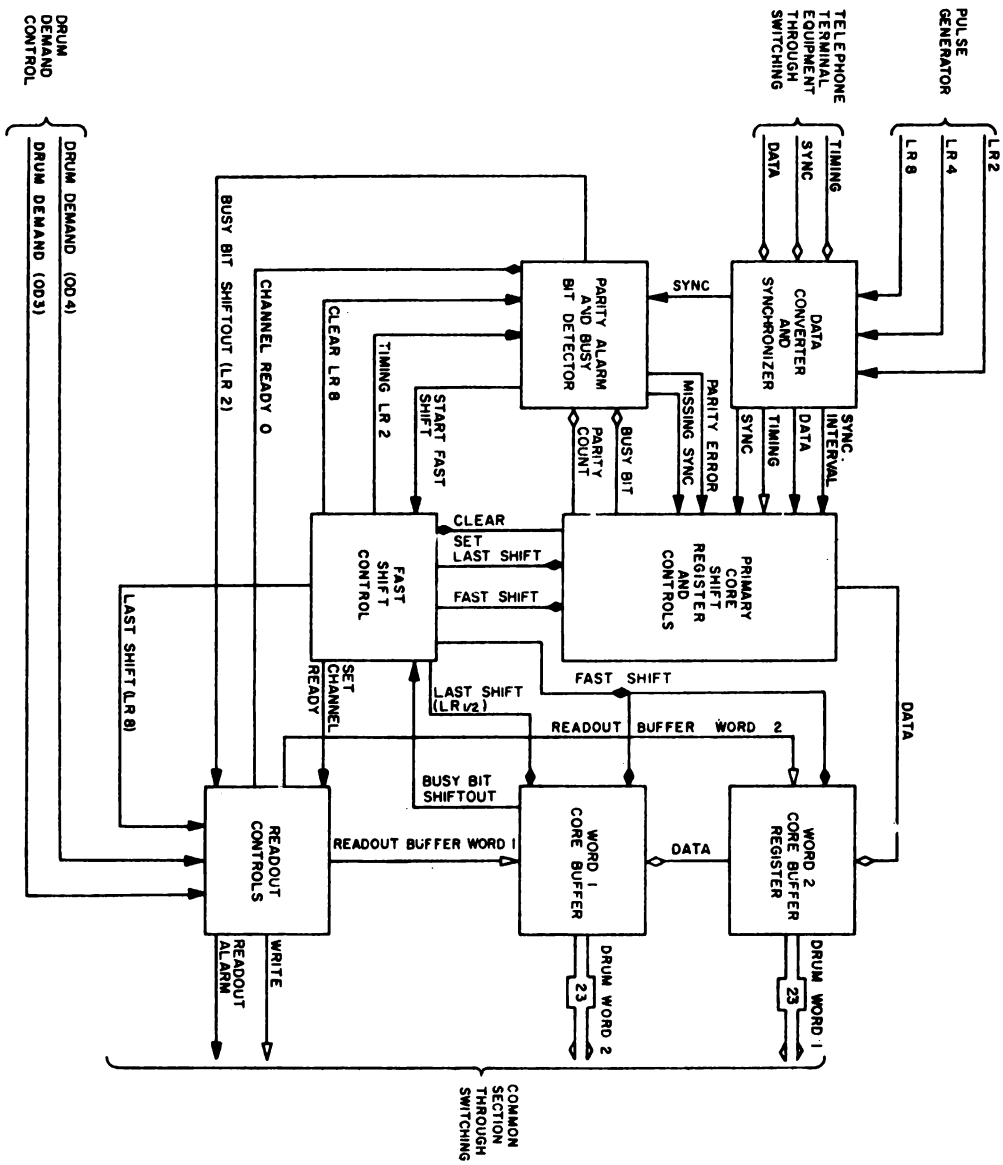
Relation of LRI pulses to drum OD timing pulses, timing chart.



NOTE: LR pulses occur every 20 usec, due to the complementing of the pulse generator FF (10D) by the OD-1 pulses.

B. LRI Channel, Block Diagram Analysis

1. Simplified diagram of LRI channel circuitry.

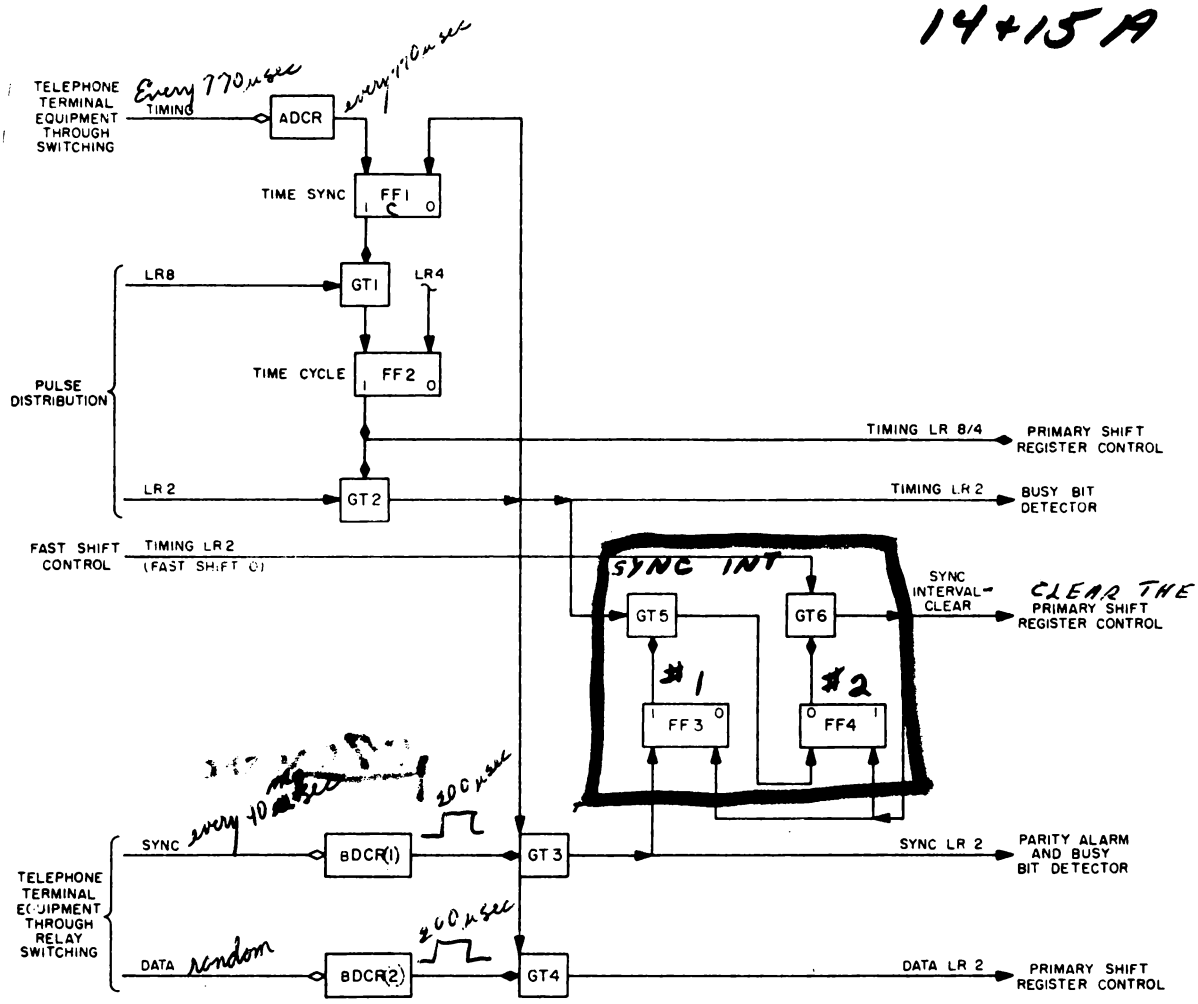


2. Data Converter and Synchronizer

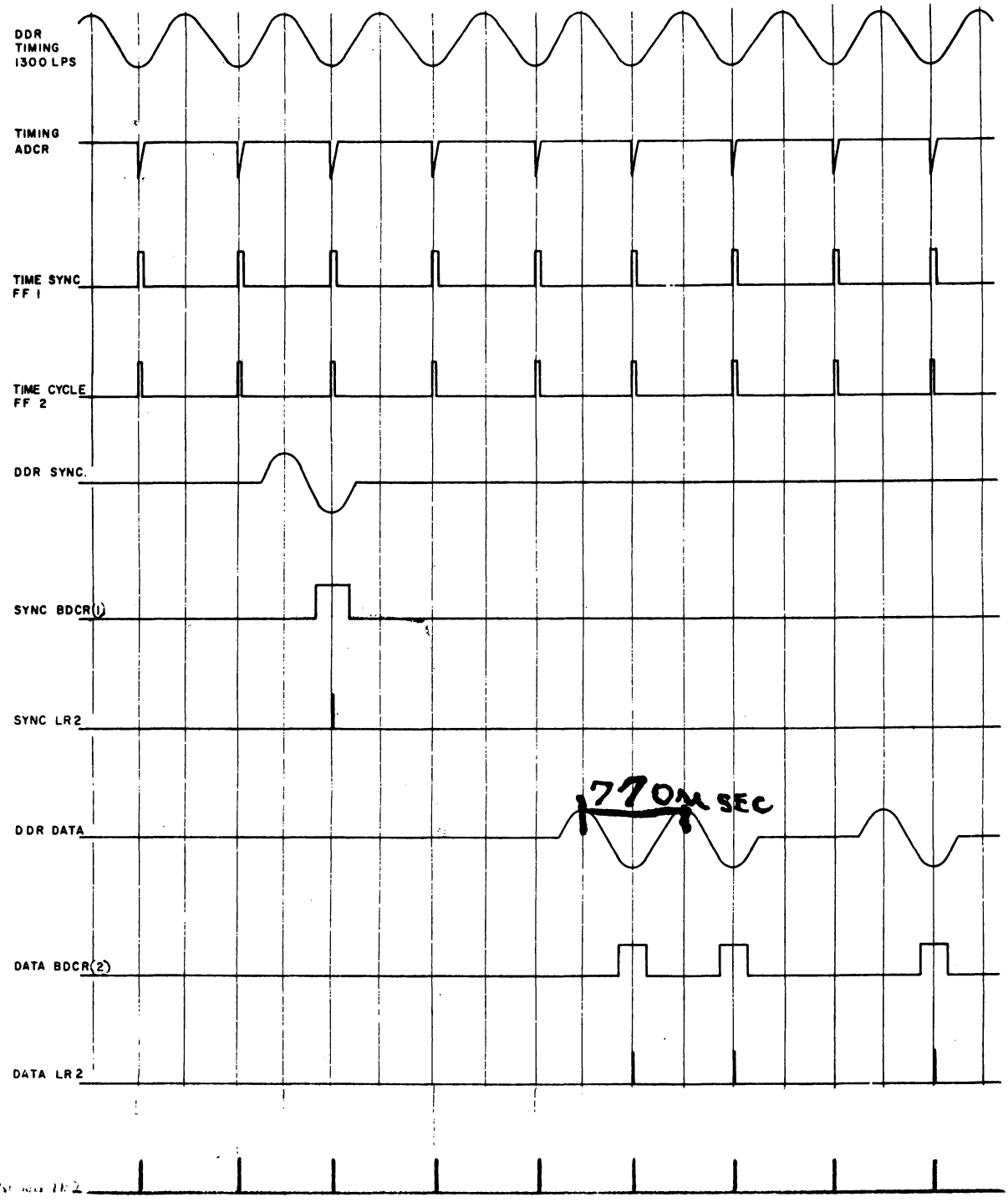
   a. Convert incoming phone line signals to standard pulses and levels.
   b. Synchronize to LRI timing.
   c. Generate necessary pulses to perform channel operations.
   d. Refer to timing chart.

Note: Page 0380

2.4.2
14+15A



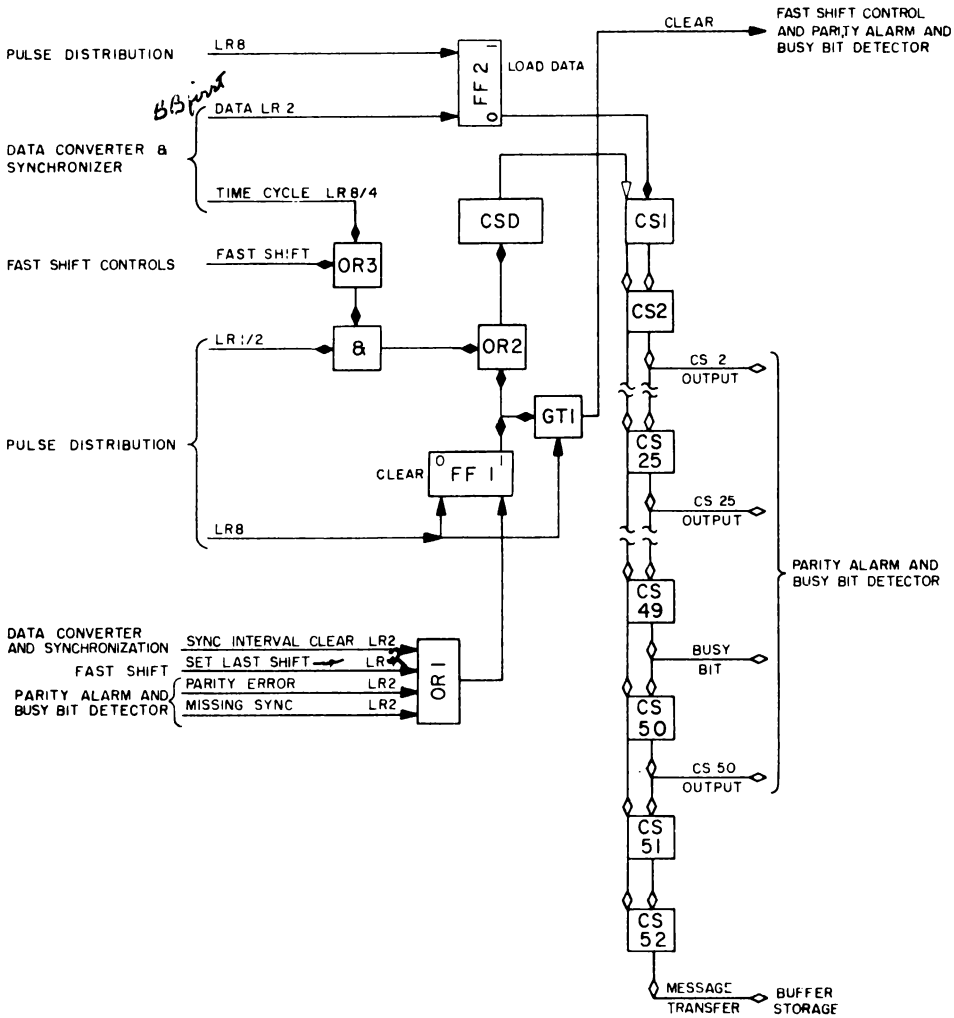
Data Conversion and Synchronizer, Timing Chart



3. Primary Core Shift Register

   a. Store message as it is received bit by bit.
   b. Isolates incoming data from Word 1 & 2 core buffer storage to allow sufficient time for previous message to be written on drum.
   c. Signals the Fast Shift if a complete good parity word is received.
   d. Sends outputs to Parity Check.

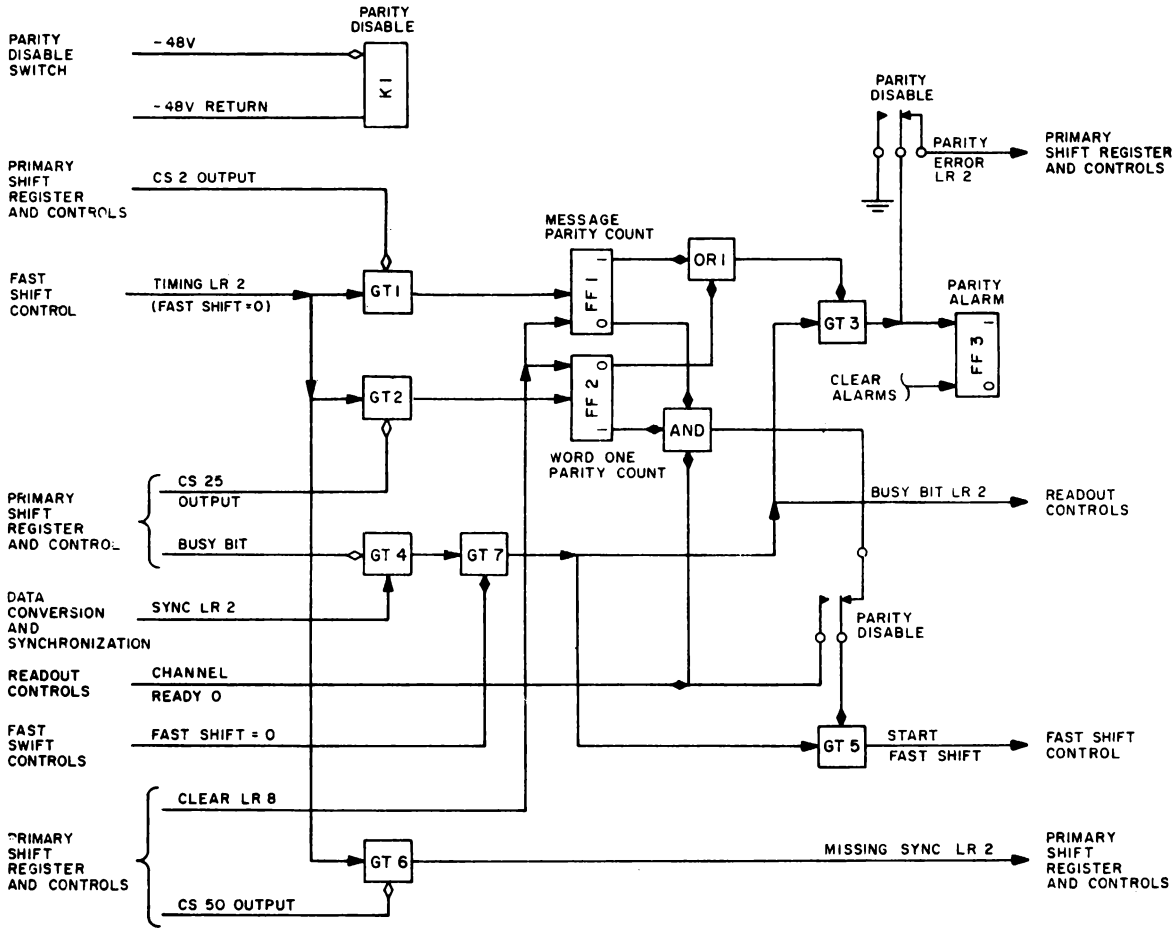
2.4.2
11-14A
41AG+
41AF



4. Parity Check

a. Check parity of entire message.
b. Check parity of Word 1 of message.
c. Prevent acceptance of a message with either or both parity errors.

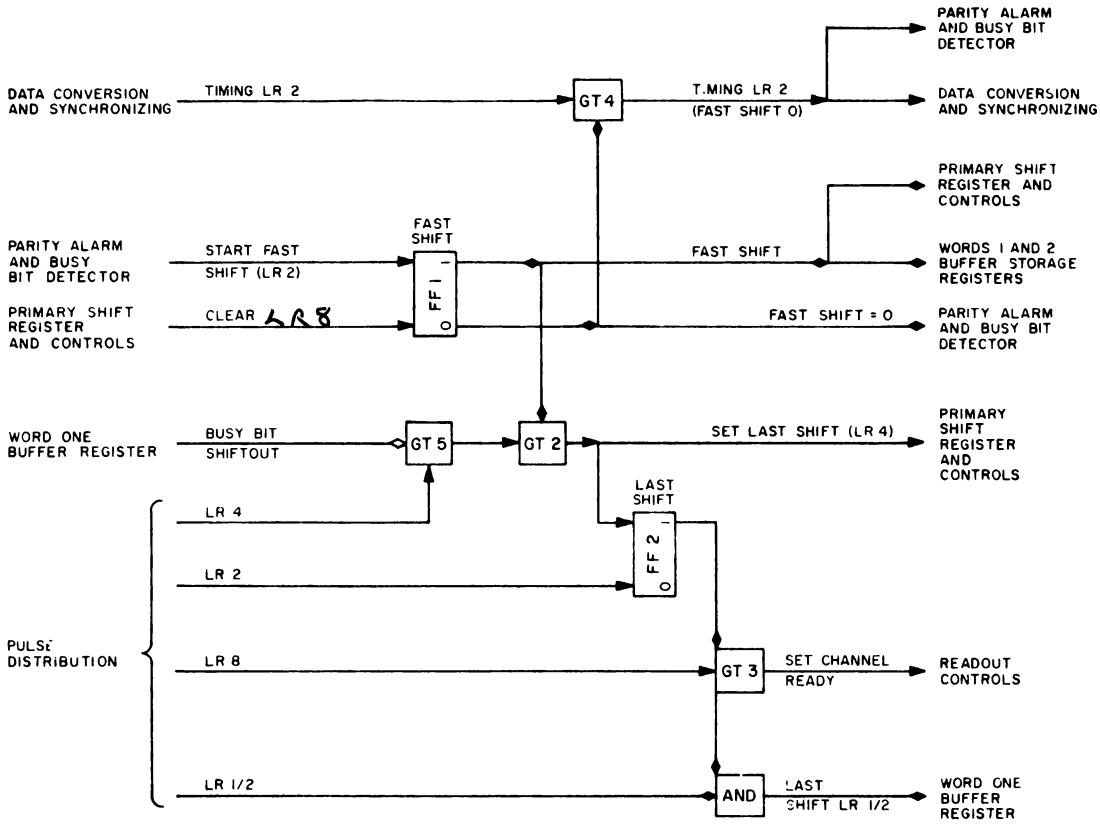
2.4.2



5. Fast Shift Control

   a. Rapidly shift message from primary core shift register into word 1 & 2 core buffer storage after a complete good parity message is stored in Primary CSR.
   b. Generates one more shift (last shift) for word 1 Core Buffer after the Fast Shifts.

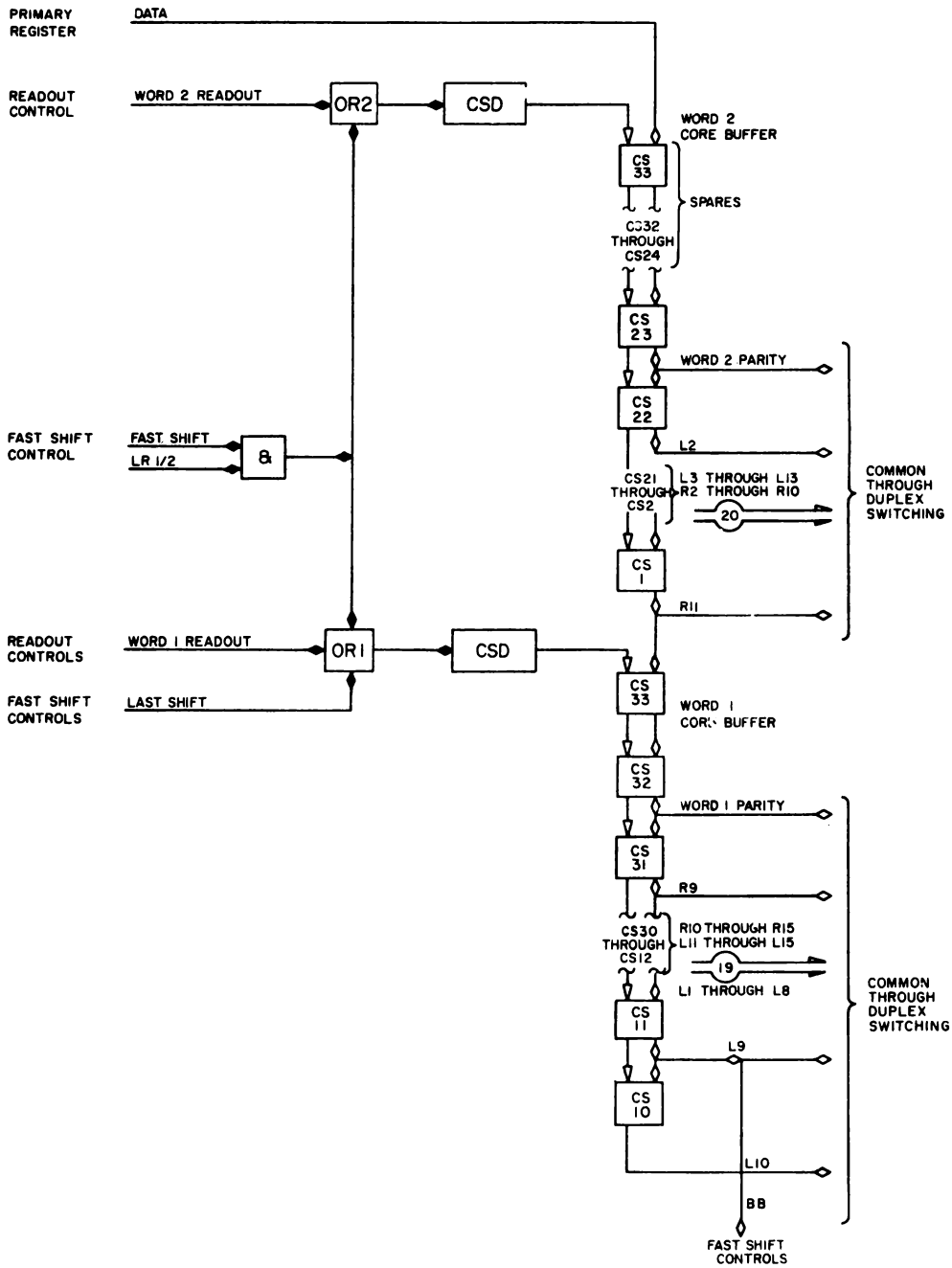
2.4.2



2.4.2

6. Word 1 & 2 Core Buffers

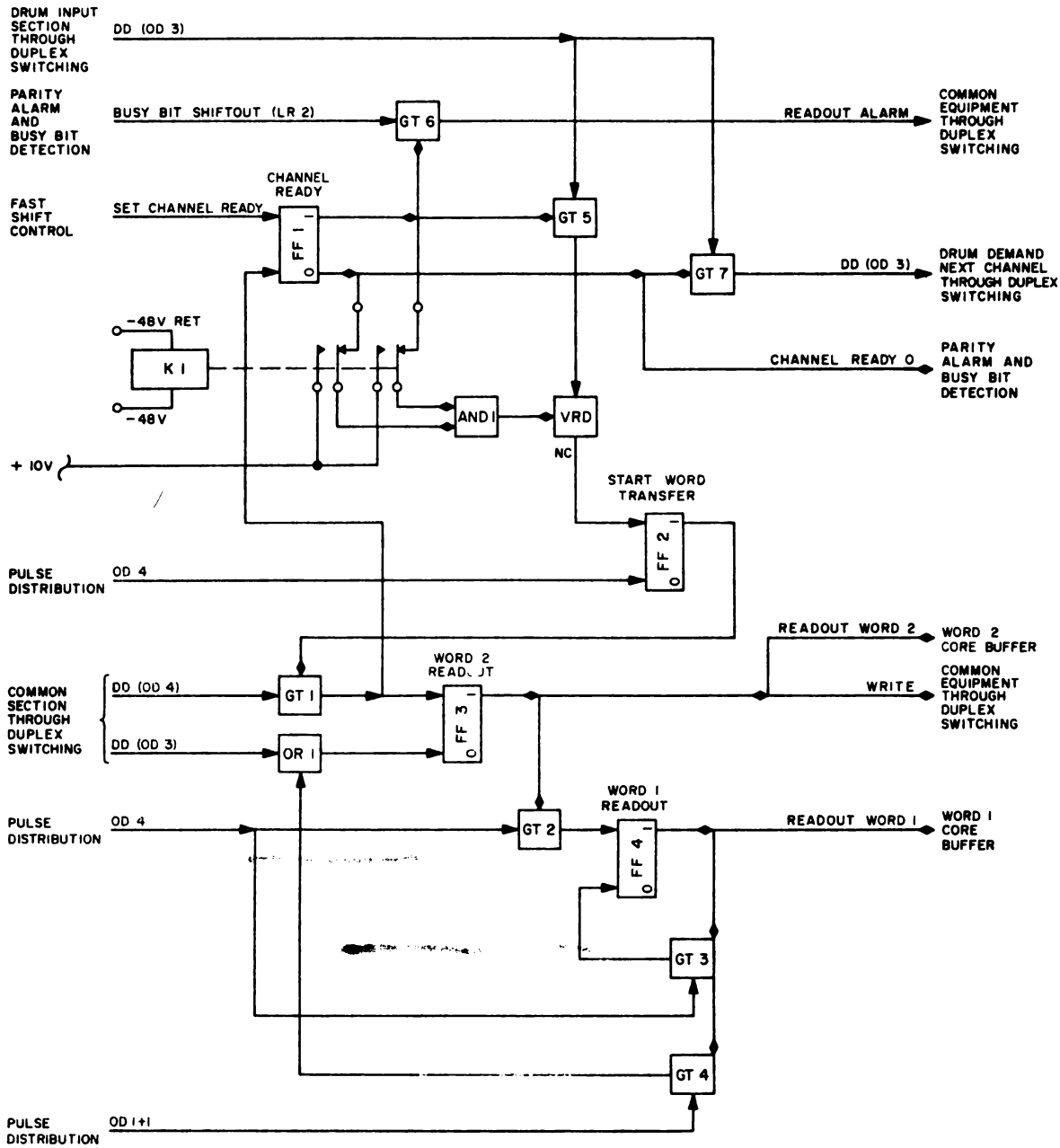
   a. Store entire incoming message that has been received serially.
   b. Maintain storage until data is written on drum.
   c. Transfer message to the Common Equipment in parallel.



7. Readout Controls

   a. Control transfer of message from channel to drum.
   b. Provide synchronism between channel common equipment and drums.

2.4.2



C. Logic Analysis, Data Converter & Synchronizer Logic S2.4.2

1. Note that Logic S2.4.2 shows two separate but identical LRI channels.

2. The two channels read out to common equipment through one set of relays.

3. The two channels (odd and even) are in one module and normally receive their inputs from one "P" site.

4. Over all operation of data converter and synchronizer.

   a. The data converter and synchronizer converts the timing since wave inputs into timing-levels, and sync or data sine wave inputs into standard pulses, which are synchronized with LRI timing (LR) pulses for use within other circuits of the LRI channel input section. The data converter and synchronizer also provides a pulse to the primary shift register control to cause clearing of the primary shift register after a sync bit has been received by the data conversion receiver DCR 1.

   b. The three classes of signals contained in an LRI message (timing, sync, and data) are sent from the telephone terminal equipment to the LRI element over separate lines. Relays in the input switching section permit the data converter and synchronizing circuit to accept messages from either the telephone line or the test bus. Each type of signal is applied to a data conversion receiver (DCR). The timing is applied to the model A DCR which converts the 1,300-cycle sine wave to a nonstandard pulse. The sync and data signals go to model B DCR's whose outputs are standard levels (200 usec duration) which occur whenever there is an input signal.

c. The timing pulse from the DCR sets FF1 which conditions GT 6 and permits the succeeding LR 8 pulse to set FF1 in 41AE. The time cycle FF conditions GT 5 (41AE) and permits the succeeding LR 2 pulse to clear the time sync FF. The clearing of the time sync FF deconditions GT 6 and prevents passage of LR 8 pulses until the next timing pulse is received. The clearing of the time cycle FF (by an LR 4 pulse) establishes the duration of the timing level (LR 8/4) at 10 usec. The timing LR 8/4 level is fed to the primary shift register control to aid in the generation of shift levels for the primary shift register. The timing LR 8/4 level is also applied to GT 5 which passes on LR 2 pulse during each timing cycle. This timing LR 2 pulse is sent to the busy bit detector circuit. The timing LR 2 pulse applied to GT 9 generates a sync LR 2 pulse when a sync bit is received by the sync DCR. For each data 1 bit received via the data DCR GT 5 passes a data LR 2 pulse to the primary shift register control to cause a 1 data bit to be loaded into the primary shift register.

d. The sync LR 2 output is also applied to the "sync interval 1" FF (41AJ). Conditioned GT 5 passes the succeeding timing LR 2 pulse to clear the "sync interval 2" FF (41AH), conditioning GT 4. The next timing LR 2 (and fast shift FF cleared) pulse passes GT 4 and is sent to the primary shift register control to cause clearing of the cores of the primary shift register. The output of GT 4 also restores cFF_3 and cFF (41AH and AJ) to their original states.

NOTE: Step 40 is accomplished only every sync input. It clears the primary shift register for the incoming data word.

D. Logic Analysis, Primary Core Shift Register and Controls

1. Over-all Operation

a. The primary core shift register control circuit serially receives the data of an LRI message from the data converter and synchronizer circuit at the rate of 1,300 bits per second. The data is loaded into the primary register. After the complete LRI message has been received and inserted into the primary register, the data is transferred to the word 1 and 2 core buffer registers at the rate of 50,000 bits per second. The main purpose of the primary register is to permit a message to be received by the channel without disturbing the previous message stored in the word 1 and word 2 core buffer registers. This provides enough time for the message stored in the buffer registers to obtain access to an LRI field on the LOG drum. The time that a message can remain in the buffer registers without being disturbed by the next message is approximately equal to the time it takes to load the primary core shift register.

b. The first data bit of an LRI message is always a 1 (busy bit); therefore, the first data LR 2 pulse generated from the busy bit clears the load data FF. The flip-flop remains cleared until an LR 8 pulse is applied to the set input. Consequently, FF 7 is cleared for 15 usec (LR 2 to following LR 8) each time a 1 data bit is received. The clear output of cFF 7 primes (inserts a 1) the first core shift (CS 1) of the primary register. The next LR 8/4 is applied through the OR and to the AND circuit. This then passes a single LR 1/2 pulse. The 2.5 usec

LR 1/2 level is applied through the 68 OR to the CSD, which then shifts the contents of each core of the primary register to the adjacent core. The next data bit is then inserted into CS 1 in the same manner as described above. When a data bit is a 0, CS 1 is not primed by the clear output of FF 2 because the data LR 2 pulse is not generated. The next shift level causes the 0 in CS 1 to be shifted to CS 2. Each shift level causes each bit to be inserted. The process continues in this manner until all the data bits are contained in the register. The shifting of the register is done at a 1,300 shifts per-second rate since an LR 1/2 level is applied to the CSD only during a timing LR 8/4 level.

c. The 49th shift level occurs after 49 data bits have been inserted into the primary register. As the 49th shift level occurs, the busy bit is transferred from CS 49 to CS 50, and the transfer is also sensed on the output line connected to the output of CS 49 (AGT_2 - 41AH). When the busy bit is transferred from CS 40 to CS 50, the output is a 1 which is sent to the parity alarm and busy bit detector circuit. A sync pulse received simultaneously with a busy bit output from CS 49 is an indication that the primary register contains all the data bits of a message. The fast shift control circuit is signaled that a complete LRI message is stored in the primary register, and the fast shift level is generated. The fast shift level, applied through the 33OR (41AF) permits LR 1/2 levels to shift the register. The LR 1/2 shift levels occur every 20 usec. (fast shift). Each data bit is transferred to the buffer storage.

on the output line of CS 52. The output of CS 50 is also sent to the parity alarm and busy bit detector circuit to aid in generating a signal, when the busy bit or sync bit is missing from the message.

d. The outputs of CS 2 and CS 25 are sent to the parity alarm and busy bit detector circuit where they are used to check the parity of the message words.

e. When the clear FF ($_{C}FF_{0}$, 41AF) is set by anyone of the four inputs, it will provide a / 10V level to the CSD. The /10V level will cause the CSD to supply current to the reset or shift winding of the primary core shift register. The current will continue until FF 1 is cleared at LR 8. Therefore, the reset current will continue from LR 2 for the sync-interval-clear, parity-error, and missing-sync, until LR 8 (15 usec in duration). For the set last-shift LR 4 input to the clear FF, the reset current will have a duration of 10 usec. At LR 8 time, when $_{C}FF_{5}$ is clear, GT 5 (41A J) is strobed, and a pulse is generated to clear the parity FF's and to clear the fast-shift FF.

2. Special Circuits in Core Shift Register

a. Power Cathode Followers

1. Model A

a) Input-standard level
b) Output-standard level
c) Added information is Basic Circuit Manual.

2. Model GG

a) Input-standard level

b) Output-standard level
c) Theory of operation
d) Note - AC coupling - prevents possible damage to CSR's if a level were applied due to a circuit failure.

b. Core Shift Driver - Model C

1. Input

a) Standard level

(1) 2.5 usec. - shift
(2) 7.5 usec. / - reset
(3) Max. rep. rate 50KC

2. Output

a) Approx. 230 m amps

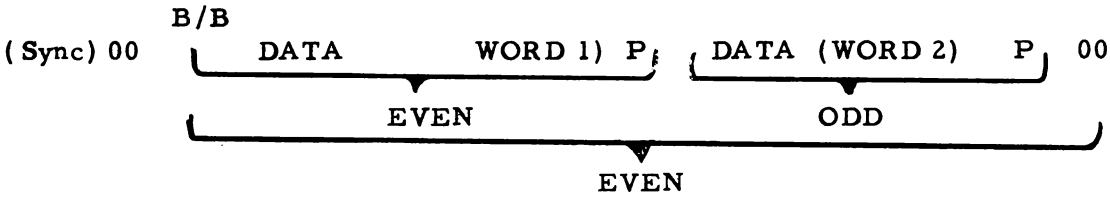
3. Theory of Operation - basic circuit manual

E. Logic Analysis, Parity Alarm and Busy Bit Detector

1. Purpose

a. Checks the parity of the incoming LRI message.
b. Checks the presence of the busy bit and sync bit as the message is processed in the primary shift register.
c. Sends a start-fast-shift signal to the fast shift control circuit, if the message parity is correct and the sync bit is present when the busy bit reaches a predetermined point in the primary shift register (an indication of a good message).
d. Sends a parity-error pulse to the primary shift register and controls, and lights a parity error neon in the alarm section of the LRI control panel if a parity error occurs.
e. Sends a pulse to the readout control circuit to generate an alarm, if the buffer storage registers contain a message awaiting transfer to the Drum System.

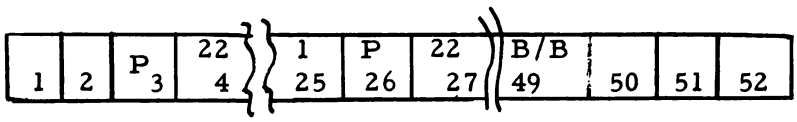
2. Parity of Incoming Message



a. Message parity count should be even.
b. Word 1 parity count includes B/B and should be odd.

3. Circuit Analysis Logic S2.4.2

a. Parity check is made when B/B is shifted, from core 49 to 50 of primary CSR and Fast Shift FF is cleared.
b. Primary CSR status just prior to busy bit output to check Fast Shift = 0 and if so to check parity.



BITS 2 21 OF WORD 2 BITS 2-21 OF WORD 1

c. Parity check.

1) Parity count correct.

a) Both counts right.
b) Start fast shift if channel ready FF is cleared.
c) Check for "readout alarm".

2) Readout alarm

a) Good message received- parity, B/B & Sync when Fast Shift = 0.

b) Channel ready set means previous message is still in word 1 & 2 buffers. Should have been written by now.
c) Alarm generated - on duplex maintenance console.
d) Message is not fast shifted but instead cleared out with next sync interval output, previous message remains intact.

3) Parity count incorrect.

a) Either or both counts in error.
b) Generate parity alarm on simplex maintenance console.
c) Message not fast shifted but cleared out immediately.

d. Parity Disable.

1) Controlled from Simplex Maintenance Console.
2) Relay can be energized only if channel is in.

a) Standby or

b) Standby MC

3) Allows message to be written on drum regardless of parity count.

NOTE: The parity of the incoming message is checked by analyzing the number of data bits in the overall message word and the number of data bits in the first message word for an odd-even count. If the message parity is correct $_{C}$FF6 in 41AH is complemented to the cleared side when all of the data bits (/B/B) have been received.

Correct parity also causes cFF2 (41AC) to be complemented to the set condition when the complete message has been received by the primary shift register. If both parity counts are correct and the channel ready FF, in the readout control circuit is cleared, the LR 2 pulse received from GT2 (41 AH) is sent to the fast shift control circuit to initiate a fast shift of the message from the primary shift register into the buffer storage. If either the message parity count or the word one parity count is incorrect, GT7 (41AH) is conditioned and passes a parity-error pulse.

F. Logic Analysis, Word 1 & 2 Core Buffer and Fast Shift Control

1. Core Buffer Description

a. Each is a 33 core CSR.
b. Data is fast shifted in from primary CSR in serial form.

c. At completion of shifting.

1) Word 1 - cores 32-10 of word 1 core buffer will contain word 1 data.

2) Word 2 - cores 23-1 of word 2 core buffer will contain word 2 data.

2. Purpose of Fast Shift Control

a. Furnishes a fast-shift level which allows the fast shifting of the message from the primary shift register into the buffer storage (eCF7, 8 41AJ).

b. Furnishes a last-shift LR 1/2 level to the word one buffer register ($_{e}$CF2A-41AJ).
c. Sends a pulse to set the channel ready FF in the readout control circuit (GT 3-41AJ).
d. Sends a set last-shift LR 2 pulse to the primary shift register and controls to initiate a clear level for the register (GT6-41AJ).
e. Sends a fast-shift = = 0 level to the parity alarm and busy-bit detector circuit to gate the busy-bit LR 2 pulse (GT6-41AK).
f. Sends a timing LR 2 (fast-shift = = 0) to the parity alarm and busy-bit detector, and to the data conversion and synchronizing, circuits as controlling signals in these circuits (GT7-41AK)

3. Circuit Operation Logic S2.4.2

a. Start of Fast Shift

1) Coincidence of B/B leaving core 49 of primary CSR, sync LR-2 and Fast Shift = 0.
2) Good parity.
3) "Channel Ready" cleared.

b. The following registers will be "fast shifted".

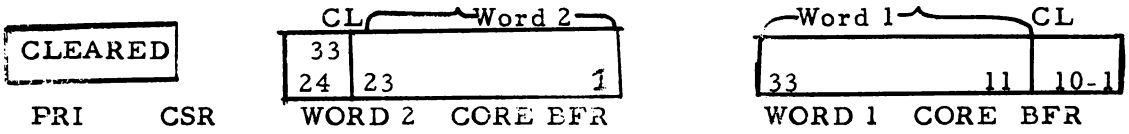
1) Primary CSR.
2) Word 1 & 2 core buffer registers.

c. End of fast shift.

1) Busy-bit path during fast shift.

a) Thru 51-52 of primary CSR.
b) Thru all of word 2 core buffer.
c) Thru word 1 core buffer cores 33 to 10.

2) Going from core 11 to 10 generates a "busy bit shift out" LR 2. (Clears primary CSR)
3) Fast shift ends at next LR 8. (GT5-41AJ)
4) At end of fast shift, core status is



d. Last shift.

1) The last shift for the word 1 core buffer is necessary in order to prevent the last bit in buffer word 1 from being affected during the readout of buffer word 2. Since buffer word 2 is read out before buffer word 1, the output of core 1 in buffer register 2 would affect the bit contained in the 33rd core of buffer register 1, if there was not a last shift emptying the 33rd core.
2) Core 33 acts as an isolation core with no data bit in it after last shift.
3) LR 8 sets "chan ready".
4) Note AC coupling of "last shift" to increase reliability.

e. End of Last Shift

1) The shifting process ends with the first half of the LRI message in cores 10 through 32 of the word 1 core buffer register, with the parity bit in core 32. The second half of the LRI message is in the word 2 core buffer register in cores 1 through 23. The buffer word 2 parity bit is in core 23.

The LRI message is read out of the core buffer registers in parallel form for each word. The word 2 buffer register is read out, first. The "readout word 2" level causes an output from each core in the word 2 buffer that contains a 1 bit. This output is sent to the LRI common equipment to condition gates that pass pulses to the

drum. Following the readout of word 2, word 1 is read out, in a like manner, through the common section to the drum. All the data in word 1 and word 2 core buffer registers, except the parity bits and the busy bit, is sent directly to the drum. Additional information generated in the common equipment is, however, also read out to the drum so that the drum words contain more information than the core buffer words. The parity bits are also processed in the common equipment before transmittal to the drum fields so that the entire drum word will have the required odd parity. The busy bit, having served its purpose in initiating the end of fast shift, is not transmitted out of the core buffer register.

The parallel output wiring of the core buffers is so connected that the data in the drum words is rearranged differently from the order in the core buffer words.

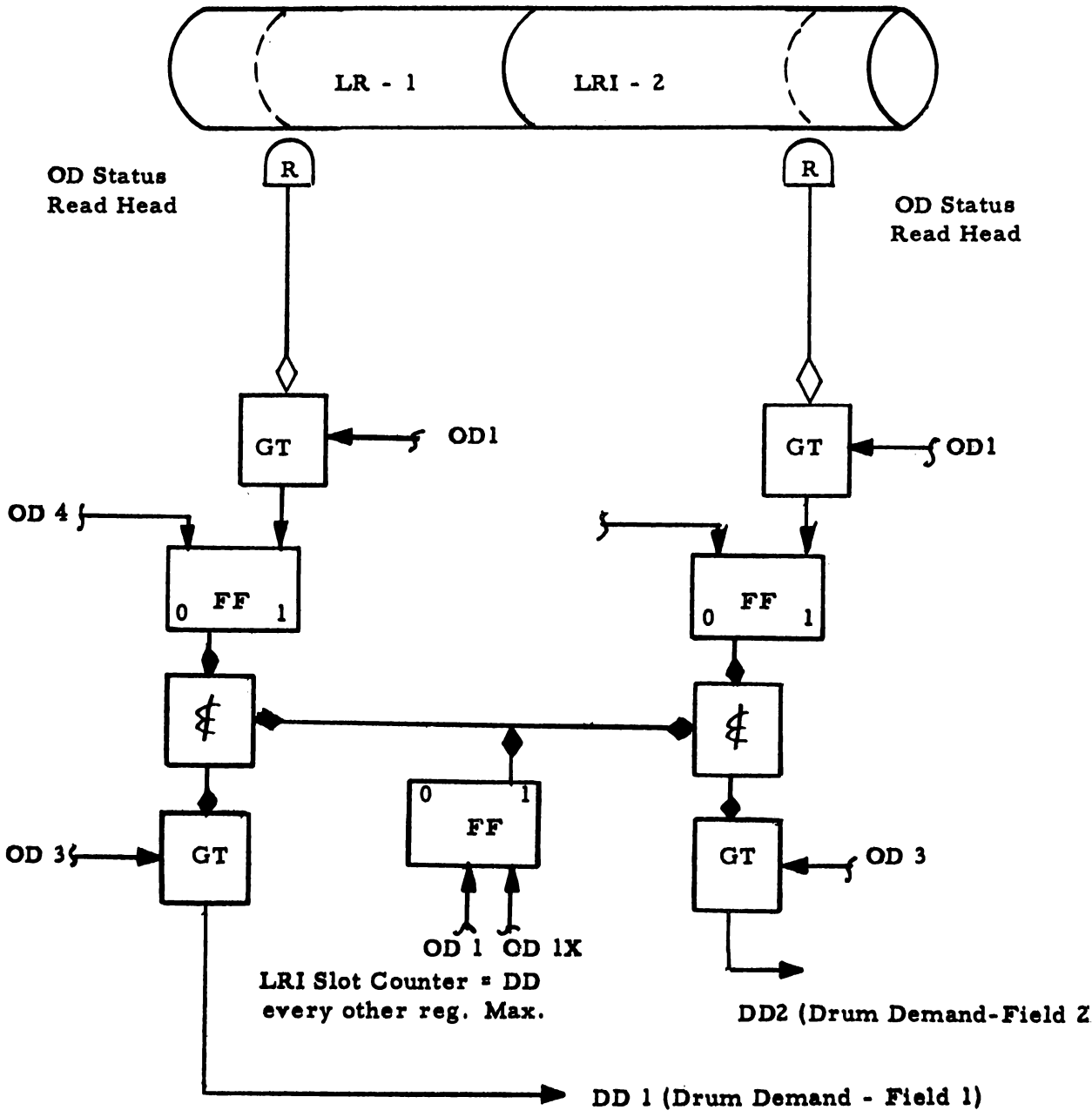
G. Introduction to LRI Drum Demand Generation

1. Objectives of LRI Drum Demand Circuitry

   a. Allow channels 1-18 to feed LRI-1 field.
   b. Allow channels 19-36 to feed LRI-2 field.
   c. Control duplex switching associated with drum demands.
   d. If data is available for both fields, field 1 data shall have priority.
   e. If data is being displayed on LRI monitor, data shall not be transferred to drum.

2. Review Drum Control (Drum Demands)

   a. Simplified Circuit on next page


LR - 1
LRI - 2
OD Status Read Head
R
R
OD Status Read Head
GT
OD1
GT
OD1
OD 4
0 FF 1
0 FF 1
&
&
0 1 FF
OD 3
GT
GT
OD 3
OD 1 OD 1X
LRI Slot Counter = DD every other reg. Max.
DD2 (Drum Demand-Field 2
DD 1 (Drum Demand - Field 1)

a. Detailed analysis in drum theory of operation manuals.
b. "Data Available" will be reviewed later.

3. Monitor Control

a. Messages are transferred to monitor at same time they are sent to drum.

b. If a message is to be displayed, further transfers to drums are prevented (no information will be lost.)

c. This is to prevent new data from going to drum until the display has ended.

d. This point will be cleared up later and should not be pursued at this time.

e. When "Monitor Display" is cleared ($_{c}$FF3-41V(AA)) Logic S2.4.5

1) No drum demands get thru

2) Display time ctr is stepped

3) A count of 32_{8} allows "monitor display" to be set

4) Next OD2 should be a "Display End" pulse to clear ctr.

f. This allows time for display. Actual timing will be discussed later.

4. Distribution of DD1 and DD2 (OD3) - GT1 and GT2, 41V (AA)

a. DD1 (OD3) checks channels 1-18 in numeric order that are assigned to drum.

b. DD2 (OD3) checks channels 19-36 in numeric order that are assigned to drum.

c. Once a channel is found ready-pulse ends search.

d. See phantom logic of "channel ready".

NOTE:

Drum demands are from both "A" & "B" com.

1) If channel is ready the "start word transfer is set".

2) If channel not ready-pulse goes to next channel.

e. DD1 & 2 (OD3's) also go to LRI monitor (2.5.1).

f. Note that any qty. of "chan. ready" FF's could be set (0 thru 36), but a max. of 2 "start word transfer" FF's could be set. This considers only one of the two drums A and B. Timing between the 2 is random.

5. Distribution of DD1 & 2 (OD4) Logic S2.4.5

a. None distributed unless "Drum Demand #1" or "Drum Demand #2" FF's are set.

b. If "DD#1" is set DD1 (OD4) are sent in parallel to all channels 1-18 assigned.

c. If "DD#2" is set and not "DD#1" then DD2 (OD4)s are sent in parallel to all channels 19-36 assigned.

d. The receipt of a DD1 or 2 (OD4)

1) Start word transfer FF clear - no effect.

2) Start word transfer FF set.

a) Start readout.

b) Clear "Channel ready".

H. Logic Analysis, Readout Control of Channel Logic S2.4.5

1. Sequence of Events

a. Receipt of a DD1 or 2 (OD3)

b. Receipt of a DD1 or 2 (OD4)

c. "Readout Word 2" generated

d. "Readout Word 1" generated

2. Circuit Analysis

   a. Channel is ready

      1) "Channel Ready" FF is set.

      2) Word 1 and 2 are in respective core buffers.

   b. DD1 or 2 (OD3) - PU 41AK

      1) "Start Word Transfer" is set.

      2) Does not clear - "Channel ready" as indicated on some logic.

      3) Note that N/C contacts of bVRD are being used to prevent multiple readout if Channel Ready FF has both sides at ≠ 10.

   c. DD1 or 2(OD4)

      1) Sets "Readout Word 2" FF

      2) Clears "Channel Ready"

      3) Is not gated by "channel ready" cleared, does not clear "start word transfer" as indicated on some logic.

   d. Every OD4 clears "start word transfer".

   e. "Readout Word 2" level comes up and resets "word 2 core buffer" storage and transfers data to common equipment.

   f. "Write" level comes up.

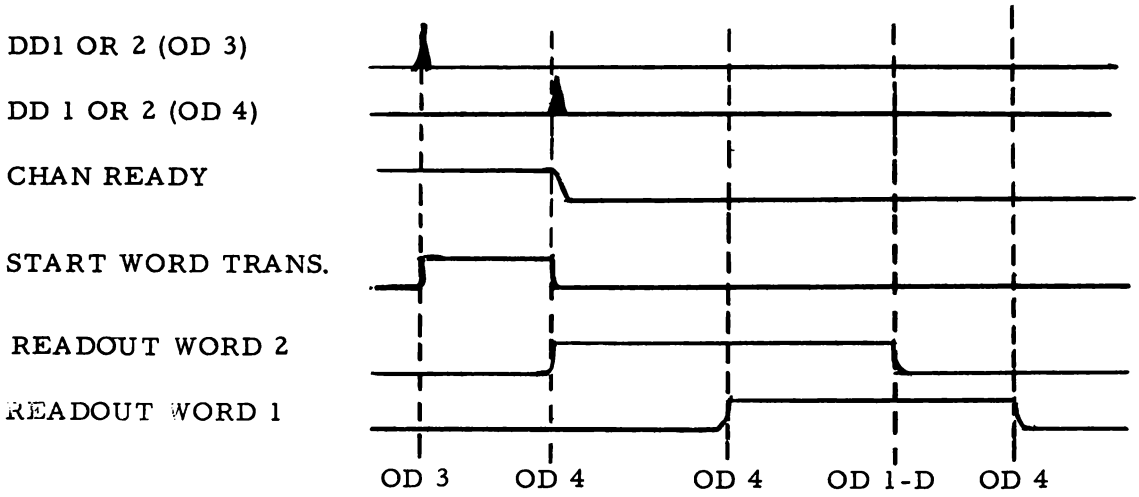
      1) Used in common equipment.

   g. Next OD4 sets "Readout Word 1" and brings up "Readout Word 1" level.

   h. Next OD1-D clears "Readout Word 2".

   i. Next OD4 clears "Readout Word 1".

   j. Timing



3. Readout of Core Buffers

   a. Word 2 buffer

      1) Each core has diode output to a pair of relays.

      2) Data goes to common A or B dependent on status.

   b. Word 1 buffer

      1) Similar to word 2 buffer.

      2) Different bits involved.

   c. Bits transferred from

      1) Word 2 buffer to L2-L13 and R2-R11 of Drum Word 1 - Parity goes to Parity Generator for Drum Word 1/

      2) Word 1 buffer to L1-L15 and R9-R15 of Drum Word 2 - Parity goes to Parity Generator for Drum Word 2.

Summary Questions

1. What is the duration of an LR-1/2 pulse? 2.5 μ sec
2. What is the repetition rate of LR8 pulses? 20 μ sec
3. Name the positions on the Unit Status Switch. off, active, standby, standby MC power filiment
4. What is meant by "Site Identity"? binary code identifying source
5. What is maximum number of P sites feeding a Direction Center? 16
6. How many bits per LRI message? 52
7. How many bits constitute the "Sync Interval"? 2
8. Where are the OD pulses used in LRI originally generated? drums - 2 fields
9. What is amplitute relationship on phone line of sync, data, and timing pulses? amplitude of sync is three times that of timing signal " " " data is two " " " " " "
10. Is parity of LRI message odd of even on phone line? even
11. Channel 5 has a circuit failure. Channels 5 and 6 were feeding data to the Active Computer (A). Which spare channels will be selected? 9&10 In which position will the "Spare Channel Selector" be set? 5&6 In which position will the spare channel "Unit Status Switch" be set? active In which position will channel 5's "Unit Status Switch" be set? off
12. Relay 41E J(K5) has an open coil (Logic 2. 4. 1). What will be the affect on LRI operation?
13. (Logic S2. 4. 1) Channel 11 becomes active. Data is not being received, however, sync and timing pulses are being received normally. The spare channel is selected to replace Channel 11 and data flow to drum is restored. Channel 11 is then switched to "TEST" and operates normal. The failure would most likely be:

    (a) Relay 41JT (K2) will not pick
    (b) Relay 41EH (K4) 5c contacts will not make
    (c) Relay 41JT (K1) 5c contacts will not make
    (d) Relay 41JT (K2) 6b contacts will not open
    (e) Relay 41 ET (K2) 5b contacts will not open

14. (Logic S2.4.1) Make a point to point wiring diagram of the "Sync" line from Channel #13 on alternate phone line #11 to Channel #9 input. Label all points and relays. Specify relays that must be picked and the conditions necessary to pick these relays. Ignore all other channel relays.

15. (Logic A2.4.6) 41HNA8 (8E) is open. Which statment is most correct:

    (a) No LR 1/2 level to Unit 41.
    (b) No LR 1/2 level to Channels 1-18
    (c) No LR 1/2 level to any channel feeding the active computer.
    (d) "A" Drum LRI Field #1 would probably never be written on.
    (e) LRI data would never reach Central Computer.

16. Fast shift is started by readout of busy bit from Core # 49 of primary core shift register. This readout can be checked only if the ~~Data~~ Sync DCR output is at +10.

17. If message word #2 was read out of main storage but message word #1 could not be read out, what would be the affect on the next LRI message? It would have its word 1 logically added to previous contents of bfr.

18. (Logic 2.4.2) Draw a timing chart showing the output of each of the following circuits. Begin with "Sync" bit and conclude when Busy Bit is primed into Core 1 of the Primary Storage Register:

    Timing DCR
    Sync DCR
    Data DCR
    Time Sync FF
    Time Cycle FF
    Load Data FF
    Clear FF
    Sync Interval #1 FF
    Sync Interval #2 FF
    41AFC1

19. Parity errors in Channel 11 fail to clear the CSR at Sync LR2 time. This could be due to:

    (a) 41AL (K4) 1a contacts open
    (b) 41JL (K4) 1c contacts open
    (c) 41AL (K4) energized
    (d) 41JL (K4) 1a open
    (3) 41JL (K4) 1b open

20. Draw a timing chart for the following circuits on Logic 2.4.2 Assume a good message is stored in Word #1 and Word #2. buffers. Begin the chart with the receipt of a Drum Demand (OD3) and conclude with the fourth OD4 following.

    Channel Ready FF
    Start Word Transfer FF
    Read Out Word 2 FF
    Read Out Word 1 FF
    120 OR (41AN) (9B)
    120 OR (41AM) (8A)

21 Draw a timing chart for the following circuits on Logic S2.4.2 Assume a good message is in the primary CSR. Begin chart at the time the following Sync Pulse arrives and conclude when the entire message is properly positioned in the buffer registers.

    Fast Shift FF
    Last Shift FF
    68 OR (41AF) (14A)
    120 OR (41AM) (8A)
    Channel Ready FF
    Clear FF

22. (Logic 2.4.2) FF6 in 41AH (13B) has an open filament. This would most likely cause:

    (a) Fast shift pulses to be generated during the entire message.
    (b) Fast shift pulses to be generated when data is not being received.
    (c) Channel Ready FF to never be set.
    (d) Failure to clear the primary CSR.
    (e) Failure to set the fast shift FF.

23. Briefly explain how you arrived at the answer in Question #22 and why the other choices could not possibly be correct.

24. Logic S2.4.2) 41AHA1 is open (11A). The message in the Primary Core Register is good and the new message coming in has a sync bit. Which statement is most correct:

    (a) No affect under the above conditions.
    (b) Message in Primary Core Register will not be shifted out before new message is shifted in.
    (c) Parity cannot be checked for future messages.
    (d) Parity alarm will be generated for next message.
    (e) None of the above.

25. How long may a message remain in main storage before a new message checks main storage to determine if it is empty? (Start with the Channel Ready FF being set.)

26. The Fast Shift FF is set for 11.6 microseconds for each good message.

27. What is the minimum time that the Channel Ready FF may be set?

    10 μ sec

28. Which of the following conditions will result in the Primary Core Shift Register being cleared? (Logic 2.4.2)

    (a) Time cycle FF being set at LR8 time.
    (b) Load Data FF being set at Data LR2 time.
    (c) 41ACA2 open (12B).
    (d) 41AFE6 open (14B).
    (e) 41AFC5 open (13A).

29. During the timing cycle that a data pulse is received the Primary CSR is:

    (a) Primed then shifted
    (b) Shifted then primed
    (c) Cleared then shifted
    (d) Cleared then primed
    (e) Shifted then cleared

30. (Logic 2.4.2) 51AFE6 (14B) is open. A mark X message with range of 1777_8 was being received. When channel ready FF is set:

    (a) Word 1 buffer would contain Word 1 and Word 2 buffer would contain Word 2.
    (b) Word 2 buffer would contain all zeros.
    (c) Word 1 buffer would contain B/B and the first bit of range.
    (d) Word 2 buffer would contain the first bit of range.
    (e) Word 1 and 2 buffers will not fast shift during this message.

31. (Logic 2.4.2) Connection 41AMA3 (9A) is open. This will:

    (a) Prevent either word from getting on drum.
    (b) Result in a readout alarm.
    (c) Cause parity of first Drum Word to always be even.
    (d) Inhibit Drum Word 1 writing but not Drum Word 2.
    (e) Allow data to be written but not read.

32. Briefly explain how you arrived at your answer for Question #44, and why the other choices could not possibly be correct.

IV. Duplex Switching

A. General

1. Duplex switching relates simplex equipment to the proper A or B common equipment and, ultimately, to the proper A or B computer. Simplex equipment in the active status is associated with the duplex computer currently in the active status, and simplex equipment in the standby status is associated with the duplex computer in the standby status.

2. Duplex switching in the LRI element provides the necessary circuitry to accomplish the following functions:

   a. Core Data Switching: Transfers the data from the core buffer registers of the 36 channel sections to the common A or common B section indicated by the status of the channel and the status of the A and B duplex computer.

   b. Write Level Switching: Transfers the write level generated in a channel input section to the proper half (A or B) of the common equipment. In spare channel switching, the write level generated by the spare channel must be switched to the site can of the replaced channel. Accordingly, when a spare channel is substituted, write level switching involves both duplex and simplex switching.

   c. Readout Alarm Switching: Directs the readout alarm pulse to the proper A or B common equipment.

   d. Timing Pulse and Level Switching: Transfers the OD pulses and the LR pulses and levels from the proper half of the common section to the channel input section to synchronize channel operations with the operation of the common section with which the channel is associated.

e. Drum Demand Switching: Transfers the DD pulses to the channel sections to initiate readout to the common equipment on a priority basis.

Disp. Time (280μ) Inhibits Dr. Demand when using monitor

f. Site Neon Indication Switching: Causes illumination of either the A or B site neons on the channel control panel (simplex maintenance console).

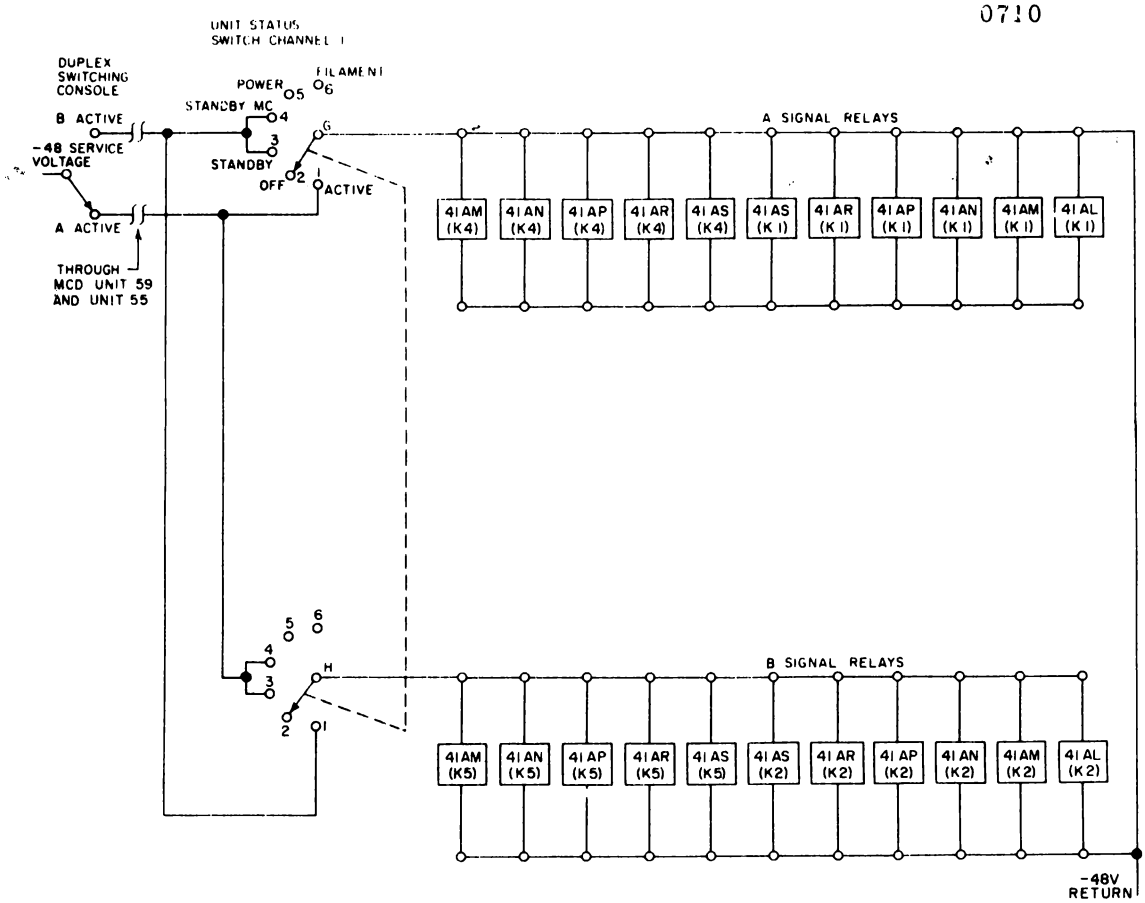
g. Status Indication Switching: Sends status indication of each channel to the MDI element of the proper computer.

B. Driving of A and B Signal Relays

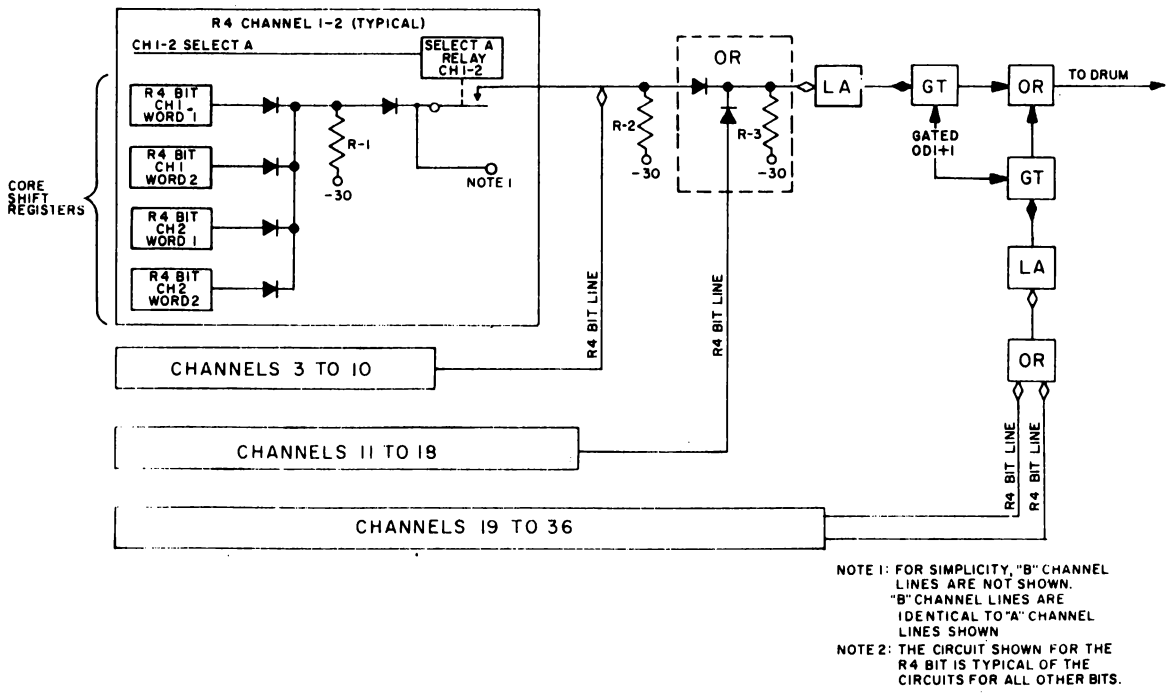
1. The operations listed above are accomplished by means of groups of relays, designated A signal relays and B signal relays. Only one group can be energized at any one time, depending on the status of the channel and the status of the A or B computer. A simplified circuit for these relays is shown on page 0760. The -48V driving voltage is supplied by MCD unit 59A or 59B through individual cells of power distribution unit 55. This voltage is applied to the terminals of unit status switch sections G and H. Section G controls the energizing of the A signal relays; section H controls the energizing of the B signal relays.

2. Simplified Circuit Analysis

a. Assume that the A machine has been designated active and the B machine standby by the duplex selection control at the duplex switching console. Relay-driving voltage is then applied to terminal 1 (ACTIVE) of section G and terminals 3 and 4 of section H (STANDBY, STANDBY MC, respectively, of the unit status switch of each channel). If this switch is placed in the ACTIVE position, driving voltage is applied to the A signal relays; if this switch is placed in the STANDBY or STANDBY MC position, driving voltage is applied to the B signal relays. Reversing the status of the A and B machine reverses the effect of the UNIT STATUS switch positions on the signal relays.



A and B Signal Relays Driving Circuit, Simplified Schematic Diagram



Core-Data Switching

3. The signal control relays for channel 1 are listed, and their functions are indicated on pages 0790 and 0800. Each contact group of a relay (if used) performs a specific function, and corresponding contact groups of paired A and B signal relays perform the same functions. Thus, when A signal relay 41AM(K1) is energized, contact group 2 causes transfer of the write level from channel 1 to the A drum input section; if the B signal relays are energized, contact group 2 of 41AM(K2) transfers the write level from channel 1 to the B drum input section.

4. When a group of signal relays for a channel are energized, one set of contacts from each relay (connected in a series array) completes a circuit to cause illumination of the related (A or B) SIGNAL CONTACTORS CLOSED lamp (X12 and X8, Logic S2.4.7, 7D). Illumination of the SIGNAL CONTACTORS CLOSED lamp indicates which computer is receiving data from the pair of channels controlled by the power section of the control panel; it also indicates that all relays in the group are energized.

FUNCTION OF SIGNAL RELAY CONTACTS, CHANNEL 1

FUNCTION	A SIGNAL RELAY	B SIGNAL RELAY
CORE DATA TRANSFER		
L1	41AN(K4) 3	41AN(K5) 3
L2	41AN(K4) 4	41AN(K5) 4
L3	41AN(K4) 5	41AN(K5) 5
L4	41AN(K4) 6	41AN(K5) 6
L5	41AP(K4) 2	41AP(K5) 2
L6	41AP(K4) 3	41AP(K5) 3
L7	41AP(K4) 4	41AP(K5) 4
L8	41AS(K4) 2	41AS(K5) 2
L9	41AS(K4) 3	41AS(K5) 3
L10	41AS(K4) 4	41AS(K5) 4
L11	41AS(K4) 5	41AS(K5) 5
L12	41AR(K4) 5	41AR(K5) 5
L13	41AR(K4) 2	41AR(K5) 2
L14	41AR(K4) 3	41AR(K5) 3

FUNCTION OF SIGNAL RELAY CONTACTS, CHANNEL 1 (con'd)

FUNCTION	A SIGNAL RELAY	B SIGNAL RELAY
CORE DATA TRANSFER		
L15	41AR(K4) 4	41AR(K5) 4
R1	41AN(K1) 3	41AN(K2) 3
R2	41AN(K1) 4	41AN(K2) 4
R3	41AN(K1) 5	41AN(K2) 5
R4	41AN(K1) 6	41AN(K2) 6
R5	41AP(K1) 2	41AN(K2) 2
R6	41AP(K1) 3	41AP(K2) 3
R7	41AP(K1) 4	41AP(K2) 4
R8	41AS(K1) 2	41AS(K2) 2
R9	41AS(K1) 3	41AS(K2) 3
R10	41AS(K1) 4	41AS(K2) 4
R11	41AS(K1) 5	41AS(K2) 5
R12	41AS(K1) 6	41AS(K2) 6
R13	41AR(K1) 2	41AR(K2) 2
R14	41AR(K1) 3	41AR(K2) 3
R15	41AR(K1) 4	41AR(K2) 4
WORD 1 PARITY BIT	41AN(K1) 2	41AN(K2) 2
WORD 2 PARITY BIT	41AN(K4) 2	41AN(K5) 2
WRITE LEVEL	42AM(K1) 2	41AM(K2) 2
READOUT ALARM	41AM(K4) 2	41AM(K5) 2
DD OD 3 (INTO CHANNEL)	41AL(K1) 3	41AL(K2) 3
(OUT OF CHANNEL)	41AL(K1) 4	41AL(K2) 4
DD OD 4	41AM(K4) 6	41AM(K5) 6
OD AND LR TIMING OD 1/1	41AR(K1) 6	41AR(K2) 6
OD 4	41AP(K4) 5	41AP(K5) 5
LR 2	41AP(K1) 5	41AP(K2) 5
LR 4	41AP(K1) 6	41AP(K2) 6
LR 8	41AR(K4) 6	41AR(K5) 6
LR 1/2	41AR(K1) 5	41AR(K2) 5
SITE IDENTITY	41AP(K4) 6	41AP(K5) 6
STATUS INDICATION	41AL(K1) 5	41AL(K2) 5

5. The detailed operation of the signal relays for channel 1 is discussed by function below; different relays, tabulated in the Input System schematic manuals, are employed in other channels, but their operation is the same as that of corresponding relays in channel 1.

C. Core-Data Switching

1. The action of the core-data switching circuit determines whether the output of each pair of channels is directed to common A or common B. The choice of common A or B is determined by manual switches located on the duplex switching and simplex maintenance consoles, as discussed in B. 1. The outputs from all active pairs of channels are directed to the common equipment that has been selected by the operator as active; the outputs from channels in the standby status are sent to the standby common equipment.

2. The switching circuit for a typical data bit (R4) is shown on page 0710. For channels 1-2, an OR circuit combines the word message signals from the core buffer registers. With both computer A and channels 1-2 active, channels 1 and 2 transfer data to common A through the A signal relay.

3. The bit signal lines from the A relays are then combined with four similar output lines from the other pairs of channels (3-4 through 9-10) or an OR circuit to form a single output line of channels 1-10 for R4 of words 1 and 2. The channels 1-10 output is combined in an OR circuit with a similar output from channels 11-18. The channels 11-18 output is combined with a similar channel 19-36 output to obtain a one-line channel 1-36 output for words 1 and 2. This is the output line from the common A section and is fed to the Drum System.

4. The core-data switching circuits for all other channel pairs are identical to the switching circuits for channels 1-2. When a pair of channels are transferring data to common B, the appropriate B signal relays are energized,

connecting that channel to common B by circuits identical with those discussed above for common A.

D. Write Level Switching

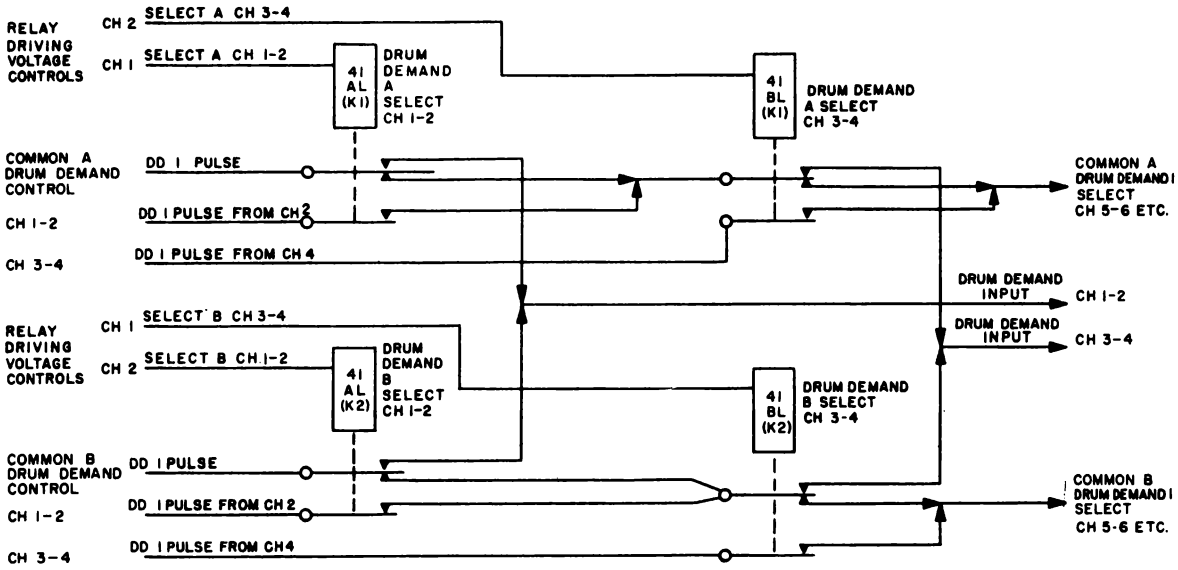
1. Write level switching connects a write level generated in the channel input section to the A or B site can in the drum input section. In spare channel operations, write level switching involves both simplex and duplex switching because the write level generated in a spare channel must be applied to the site can for the replaced channel.

2. The write level switching circuit for channels 1-2 is shown on page 0760. A write level, originating in channel 1, is transferred to either common A or common B through the 2 contact of either A signal relay K2, or B signal relay K1. The write level for channel 2 and other regular channels is transferred in a similar manner, depending on which signal relay (A or B) is energized.

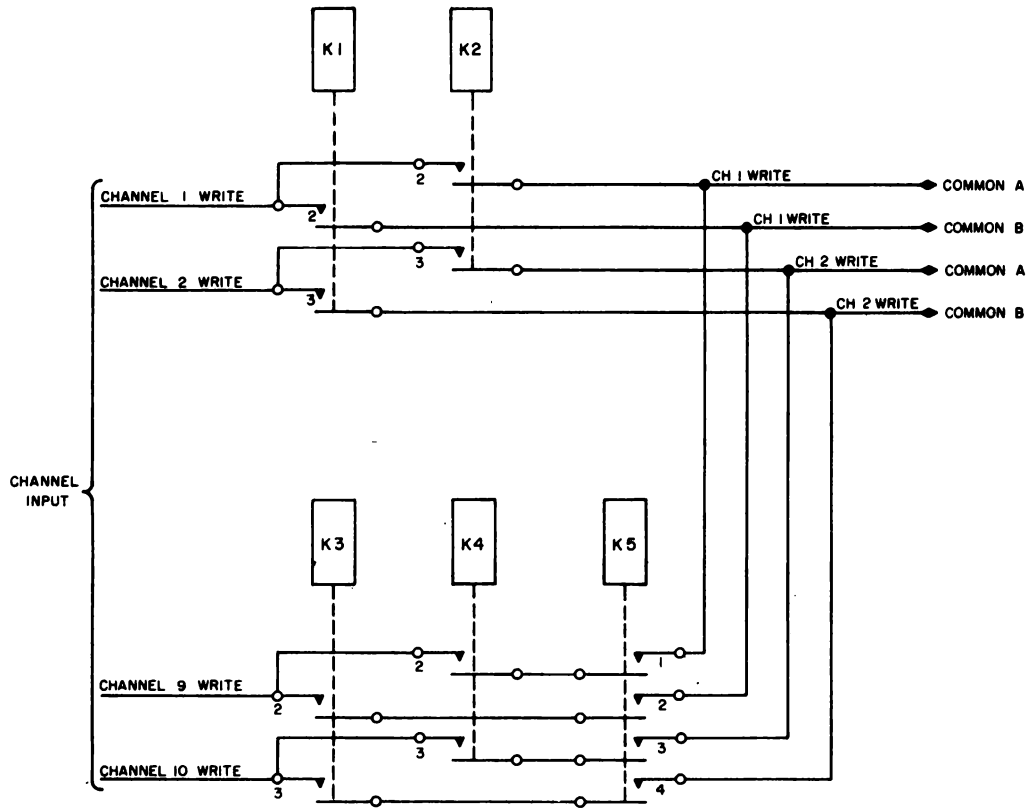
3. In spare channel operations, a channel 9 write level, generated in the drum input section, is transferred through the 2 contact of either the A or B signal relay for channel 9 and through the 1 or 2 contact of the select spare for channels 1-2 relay (K5). The output is on the channel 1 write line to common A or common B, as determined by the channel 9 signal relay. A similar circuit related to the channel 2 write level is shown for channel 10. Circuitry exists for other channel pairs with the select spare for channels 3-4, 5-6, etc., in place of relay K5.

E. Readout Alarm Switching

1. A readout alarm pulse is generated in the readout control circuit (Logic S2.4.2) indicating that the primary shift register has a message ready for fast-shifting into a core buffer register which already contains a message. The readout alarm pulses for each channel are transferred through switching to the proper A or B common section, causing the readout alarm FF to be set. For channel 1, the readout alarm pulse is transferred through signal



Drum-Demand Switching (chan. 1 and 2; chan. 3 and 4)



Write Level Switching, Simplified Diagram

relay A contact 41AM(K4) 2 or through B signal relay contact 41AM(K5) 2, as indicated on page 0730.

F. Timing Pulse and Level Switching

1. The OD pulse and LRI pulse and level switching circuitry switches the timing pulses and levels generated or controlled by the A and B drum input section to the channels associated with the A and B computers, respectively.

2. The output of the timing pulses is on Logic A or B 2.4.6 - 1 to 12 E.

G. Drum-Demand Switching

1. The drum-demand circuit of Drum Systems A and B sends pulses to the channels connected to common A and B, respectively. The function of the drum-demand switching circuit is to send, in order of priority, the A DD pulses to the input channels connected to common A, and the B DD pulses to the input channels connected to the common B. The input channels connected to common A in the channels 1-18 receive a DD 1 pulse from the drum-demand circuit, while the 19-36 channels receive the DD 2 pulse.

   Drum-demand switching for channels 1, 2, 3 and 4 is shown on page 0760. The use of the drum-demands was discussed in Section IIIG of the Lesson Plan.

2. Drum-Demand Switching for Channels 1 and 2

   a. The DD 1 pulse from the drum-demand control circuit in common A is sent to the readout control circuit of channel 1 when the select A channels 1-2 line is energized. The DD 1 pulse initiates readout of channel 1, or, if channel 1 has no message data stored, it passes the DD 1 pulse to the readout control circuit of channel 2. If channel 2 is not ready, the DD 1 pulse comes out of channel 2 and is passed to the A select relay contacts of channels 3-4.

b. When channels 1 and 2 are connected to common B, the DD 1 pulse passes directly from common A to the drum-demand A select relay of channels 3-4, completely bypassing channels 1 and 2.

3. Drum-Demand Switching for Channels 3 and 4

a. After a DD 1 pulse from the drum-demand switching circuit is applied to the A select relay for channels 1-2 and found that there was no data available, the DD 1 pulse will then check channels 3-4. The DD 1 pulse passes through the readout control circuits of, first, channel 3, and then, channel 4. When channels 3 and 4 are not connected to common A, the DD 1 pulse from channel 2 passes directly to the drum-demand switching for channels 5-6, or to 7-8 if 5-6 are not activated, etc.

b. All channels which are connected to common B use and pass DD 1 pulse from the drum-demand switching circuit of common B in exactly the same manner described above for the channels connected to common A.

c. The drum-demand switching for all other pairs of channels (in the channels 1-18 group) is controlled in the same manner as described above. The last 18 channels (channels 19-36) receive the DD 2 pulse from the drum-demand switching circuit in the same manner as described for the DD 1 pulses entering the first 18 channels.

H. Site Neon Indication Switching

1. Each LRI control panel (simplex maintenance console) has two sets of site identity neon indicators, identifying the P-site from which the channel is receiving information. The A set of indicators is active when the channel is in the same status as the A machine; the B set is active when the channel is in the same status as the B machine. Switching is accomplished through a contact on the A or B signal relays which connects the four neons (as a group) to a / 150V source.

I. Status Indication Switching

1. Status indication switching causes a ∕ 10V level to be applied to set a 1 in an assigned core in the direct entry section of the MDI element. Periodically, these cores (organized as a core matrix) are read out to the computer. Thus, each computer is informed of the associated LRI channels and of the status of each channel. The signal relay contacts, used in status indication switching for channel 1, are shown in the table on page . Similar circuitry and contacts, for each of the other channels, associate the channels with either the A or B computer.

J. Summary Questions

1. A transient "1" bit was received on the data input phone line one timing cycle prior to receipt of the Busy Bit of a good message. Where did this transient "1" bit finally end up after the channel ready FF was set? Or was the channel ready FF ever set?

2. (Logic S2.4.4) R8 for Channel 15 is always a zero when writing on "B" drums. All other channels operate normal. This could be due to:

    a. 41FFE6 open (1 0D).
    b. 41AMF6 open (13C).
    c. 41LN(K5) 4C contacts won't make (8C).
    d. 41LS(K2) 2C contacts will not make.
    e. None of the above.

3. (Logic S2.4.5) Channels 1, 2, 7, 8, 13, 14, 25 and 26 are active. Channels 3, 4, 11, 12, 21, 22, 29 and 30 are standby. "B" computer is active, "A" computer is standby. Recurring readout alarms from Channels 21, 22, 29 and 30 are noted. Drums are known to be only half full. The trouble could be:

    a. 41SKE6 open.
    b. 41V(AA) GT1 will not pass a pulse.
    c. 41NL(K2) 3a contacts will not make.
    d. 41G(AA) J7 open.
    e. 41GYC5 open.

4. (Logic S2.4.5) 41DL(K1)4C contacts will not make. What would be a good indication that this trouble had occurred?

5. (Logic S2.4.2) aGT3 in 41AU(10E) passes all pulses. Channels 1, 2, 4 and 6 have messages in core buffers awaiting transfer. All channels are assigned to "A" common. Which of the following statements is most correct?

    a. Channel 1 writes, Channel 2 writes, Channel 4 writes, and Channel 8 writes, in this order.

    b. Channel 1 writes, Channels 2 and 4 logical add on drum, Channel 8 writes, in this order.

    c. Channel 1 and 2 logical add on drum, Channel 4 and 8 write normal in this order.

    d. Channel 1 writes, Channel 4 writes, Channel 8 writes in this order. Channel 2 message will be lost.

    e. Channel 1 writes, messages from Channels 2, 4 and 8 will be lost.

6. (Logic S2.4.5) 41 GYC1 (7E) is open. This could cause which of the following results under the indicated conditions?

    a. DD-1 and DD-2 received, Channel 21 ready; no data transfer.

    b. DD-1 received; Channel 2 ready; no data transfer.

    c. DD-2 received; Channel 20 ready; no data transfer.

    d. DD-2 received; Channel 15 ready; no data transfer.

    e. DD-1 and DD-2 received; Channel 5 ready; no data transfer.

7. (Logic S2.4.5) Which of the following conditions would result in the transferring of a message from Channel 33, even though Channel 4 was ready? Both fields are empty and both channels are assigned to common "A".

    a. 41GYJ1 open (7E).
    b. 41G(BB) A1 open (7E).
    c. 41GYJ3 open (7E).
    d. 41GYB8 open (8D).

8. (Logic S2.4.5) Channels 1, 2, 5, 6, 11, 12, 17 and 18 are assigned to "B" Computer. All other channels are assigned to "A" Computer. List in sequence the relay contacts across which the DD-1 (OD3) from the "B" drums will pass from the time it leaves common "B" until it re-enters common "B". Assume no channels have data available at the time.

9. Assume same conditions as in question 8, except Channel 8 has a message awaiting transfer. List in sequence the relay contacts across which the DD1 (OD3) from "A" drums will pass and the relay contacts across which the DD1 (OD4) will pass. Do not list relay points common as terminals.

V. LRI Common Equipment Operation

A. Common Equipment Block Diagram (Refer to page 0840)

1. Introduction

The common equipment of the long-range radar input element serves as a common path for data flowing from the 36 LRI channel sections to the LRI drum fields. As the LRI message is transferred to the drum field, the message is re-formed into two drum words, and three pieces of information are added. The three pieces of information added are:

a. Site identity, which provides identification of the long-range radar site originating a message.

b. Clock time, which indicates the time a message is transmitted to the drum, relative to the real time clock of the Central Computer System.

c. Drum word parity, which is a bit for each drum word to establish odd drum word parity.

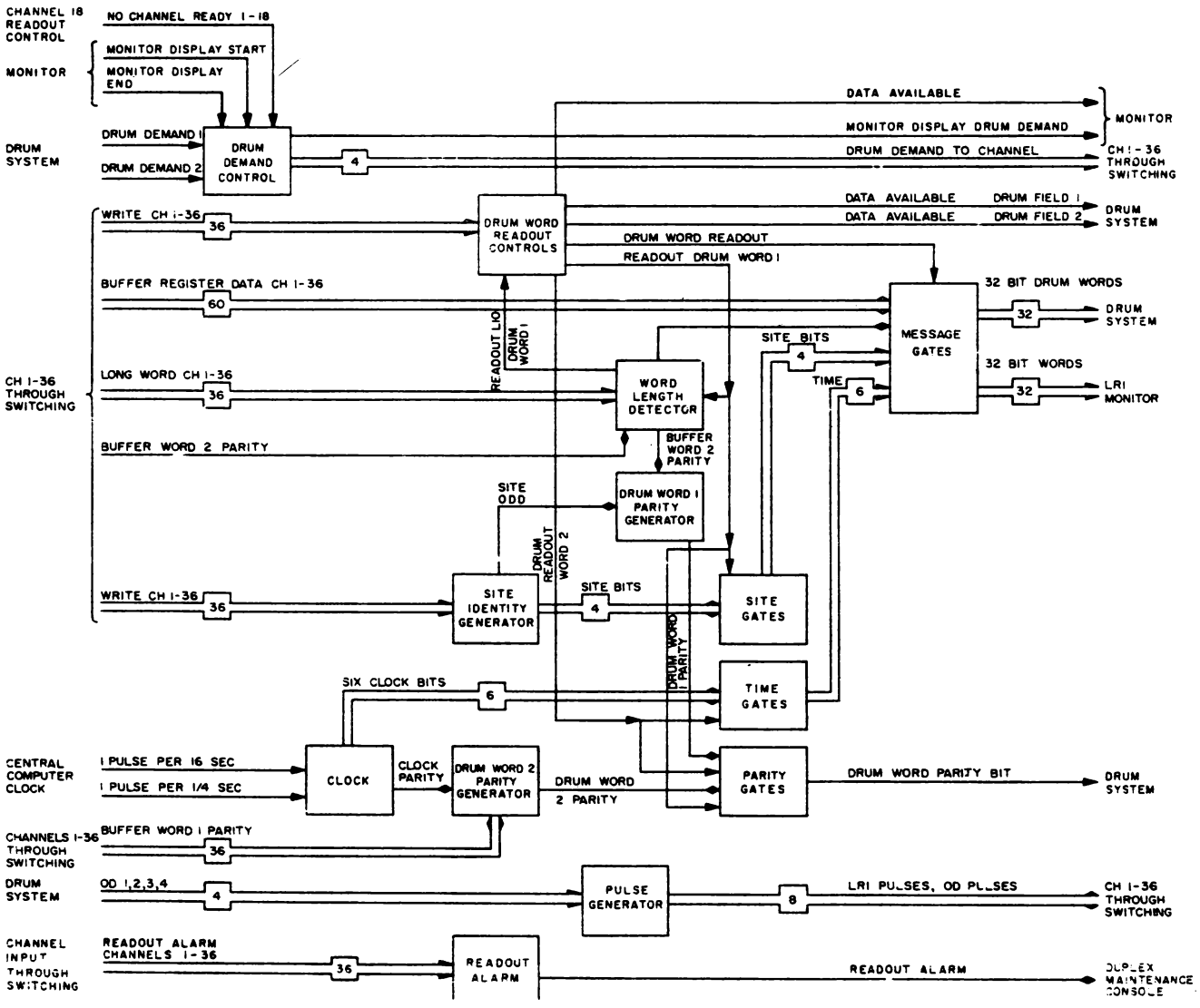
In addition to adding site identity, clock time, and parity bits to each message, the common equipment performs the following functions:

a. Sends the drum words to the LRI Monitor.

b. Sends DD pulses in priority sequence when an empty drum slot becomes available. The messages from channels 1-18 are sent to drum field 1, and the messages from channels 19-36 are sent to drum field 2.

c. Informs the Drum System and LRI Monitor when a drum word is being transferred to them. (Generates a data available.)

d. Synchronizes the transfer of data to the Drum System with Drum System timing pulses.



LRI Common A, Simplified Block Diagram

e. Generates a series of timing pulses, for use throughout the LRI element, that are synchronized with OD pulses from the Drum System.

f. Generates visual alarms displayed on the maintenance console when certain error-causing conditions arise.

2. Layout of Common Equipment

a. Each Common (A and B) has a six tube module on opposite end of Unit 41.

b. Lessens cabling from channels to common.

c. Signals are OR'ed together before going to common proper.

d. This accounts for various "illogical" duplications of circuitry throughout common equipment.

3. Data Flow

a. Serves as a common path for data from those channels assigned to Drum System.

b. First drum word.

1) Data from channel - 22 bits (Buffer Word #2).

2) Site identity - 4 bits.

a) Generated in common equipment.

b) Controlled by write level.

3) Parity - combination of site identity count and buffer word 2 parity from channel.

c. Second Drum Word

1) Data from channel - 22 bits (Buffer Word #1).

2) Clock - 6 bits.

a) Generated in common equipment.

b) Controlled by computer clock pulses.

3) Parity - combination of clock count and buffer word 1 parity from channel.

4. Control Functions

a. Message Gates

1) Output to drums and monitor.

2) Input - data from channels and site or time bits.

b. Clock and Site Gates

1) Output - to drums.

2) Input - clock and site identity generators.

c. Drum Word Readout Control

1) Generates data available pulses (O.D. 1 / 1)

2) Samples correct gates for data transfers.

d. Drum Demand Control

1) Sends drum demands to channels, and establishes channel priority.

2) Sends DD to monitor.

e. Site Identity Generator

1) Receives write levels from 36 channels.

2) Generates 4 bit site identity.

f. Clock

1) Max count = 77_8.

2) Enables central computer to calculate the time between the writing and the processing of a message.

g. The drum word 2 parity generator generates the parity bit for drum word 2 by using the parity of the first message word and the parity of clock time to determine the required parity bits to give odd parity to the second drum word.

The drum-word-1 parity generator determines the parity bit of the first drum word from the message-word-2 parity and the site identity parity.

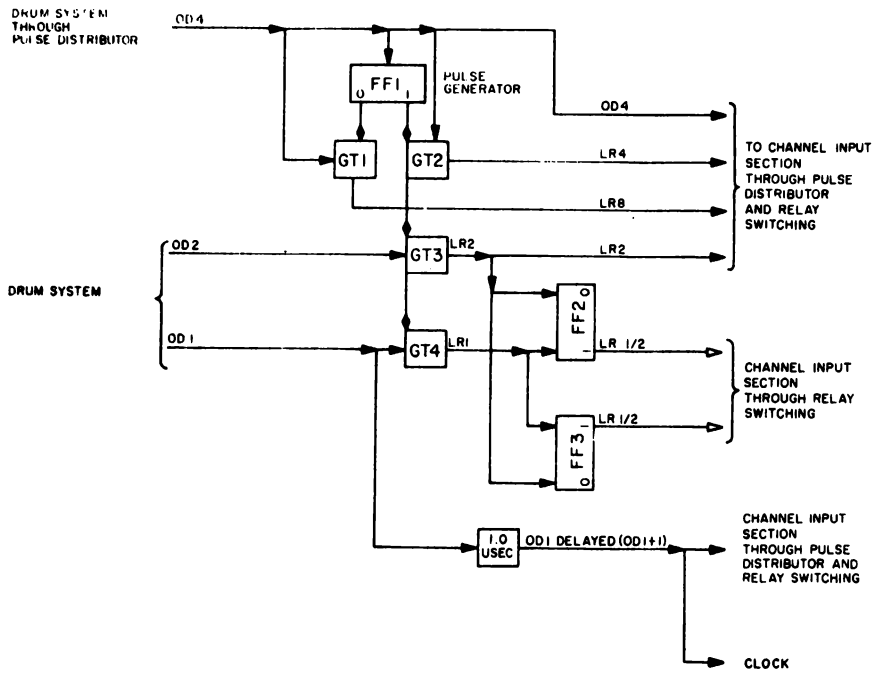
B. Logic Analysis, Drum Demand Control

1. Purpose

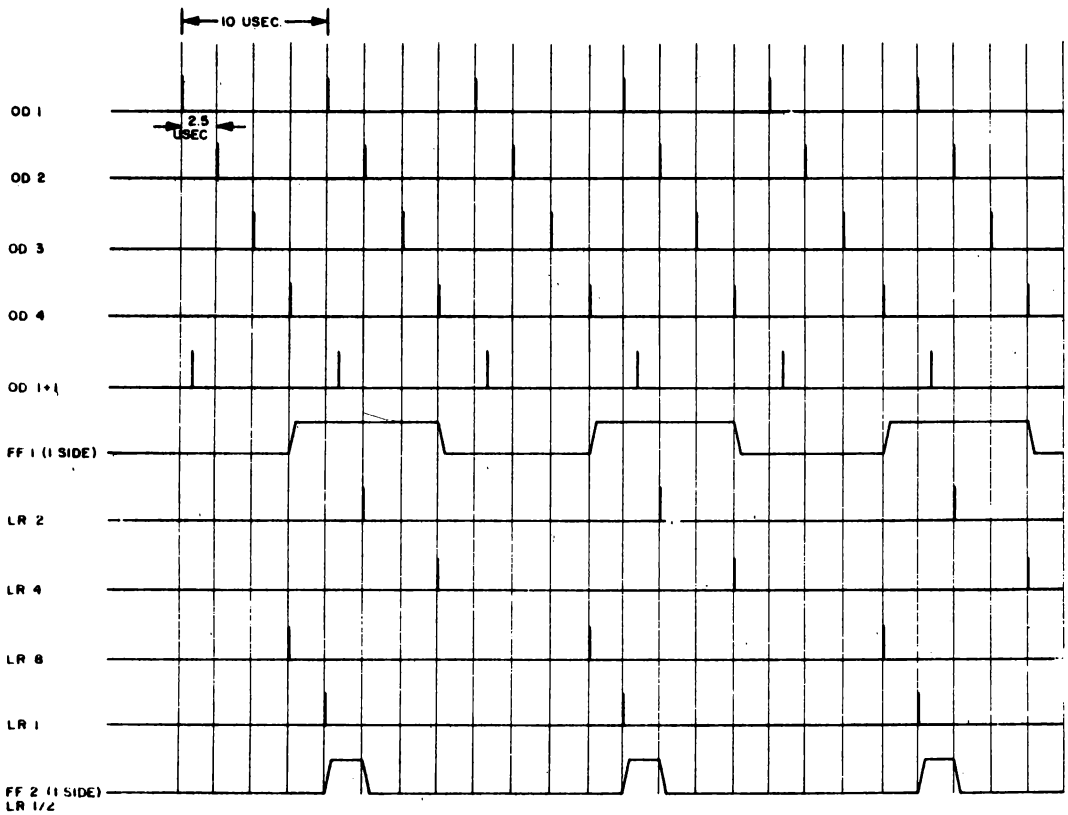
a) The LRI element supplies data to two drum fields of each computer. Drum field 1 of A or B receives information from channels 1-18 and drum field 2 of A or B receives data from channels 19-36. Two DD pulses from the A system are received by the drum-demand control circuit and are designated DD 1 (OD3) and DD 2 (OD 3). The B drum-demand circuit receives B drum-demand pulses. The DD pulse is synchronized with an OD 3 drum-timing pulse. The appearance of the DD 1 (OD 3) pulse indicates an empty slot on drum field 1 which is therefore ready to receive data from a channel. The DD 2 (OD 3) pulse occurs when an empty position is available on drum field 2.

2. Operation of Drum-Demand Pulses

a) Drum-demands are applied to channels 1-18 and 19-36 at the same time. Note, however, that an OD 4 readout pulse for channels 19-36 cannot be generated unless no channels (1-18) are ready.

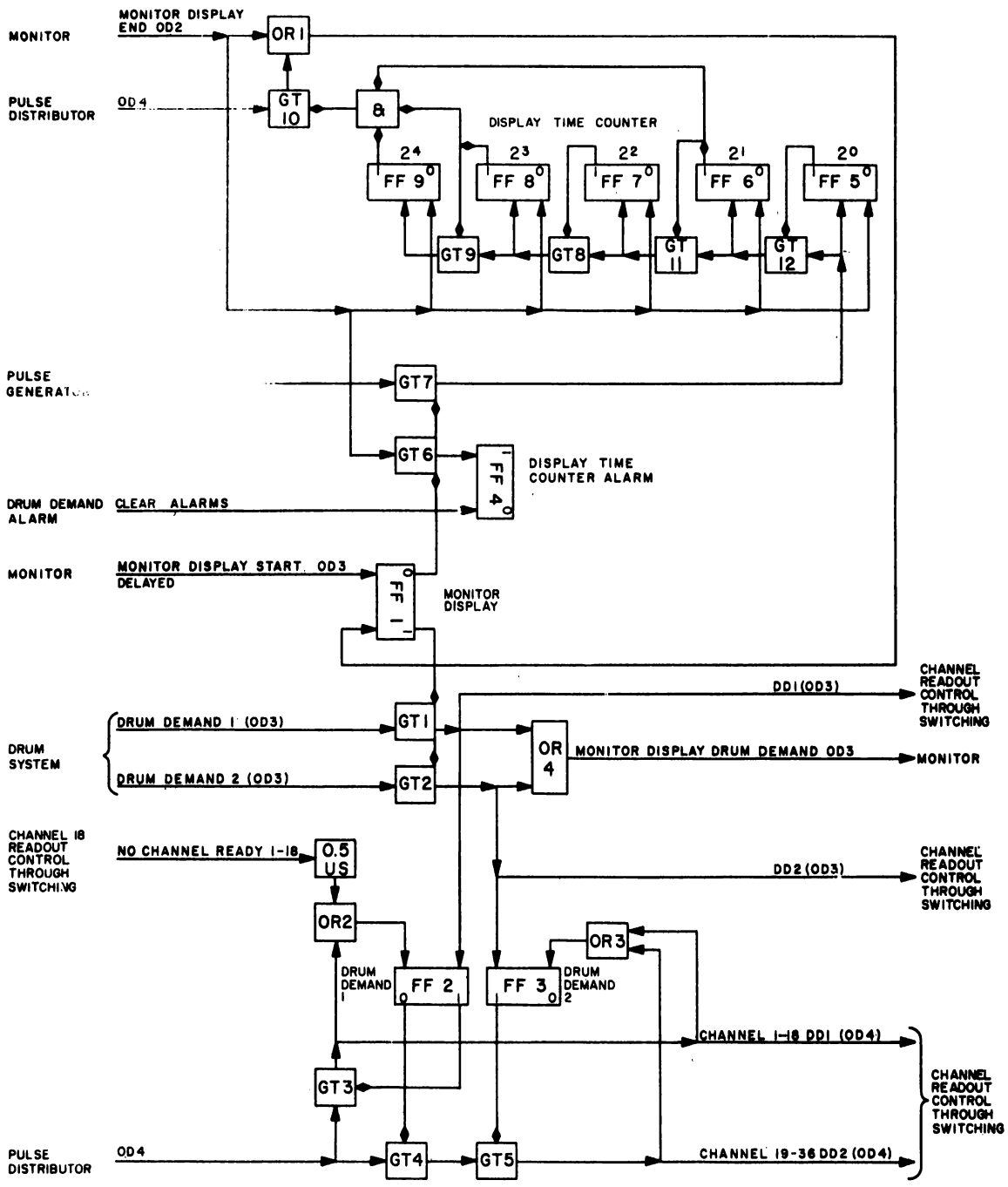


Pulse Generator, Simplified Logic Diagram

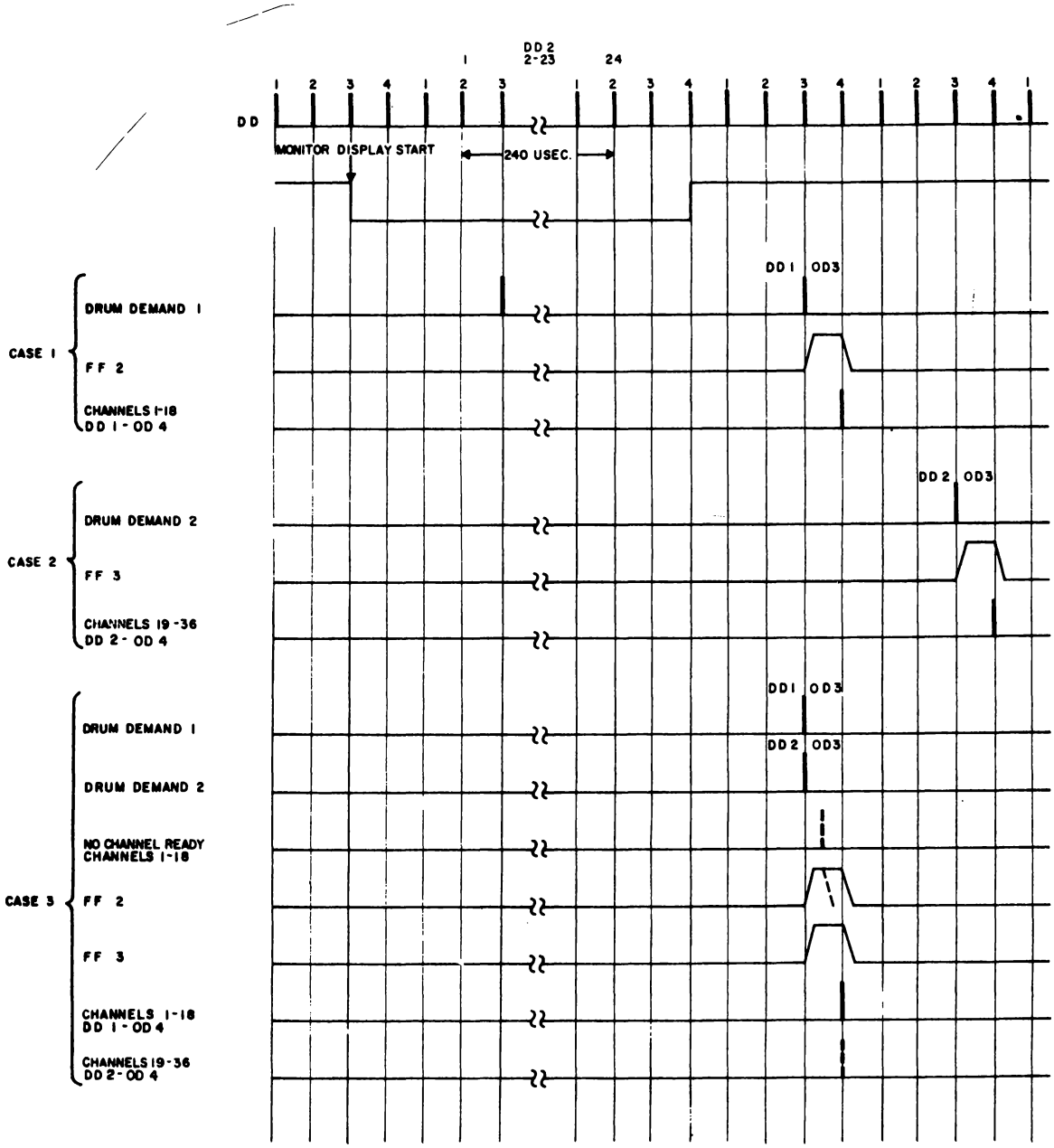


Pulse Generator, Timing Chart

A 2.4.2.1
[B 2.4.2.1]



Drum-Demand Control, Simplified Logic Diagram



Drum-Demand Control, Timing Chart

b) Although all channels are receiving data simultaneously and only one channel can read out data at a time, the speed of readout (20 usec) is small enough, compared to the time necessary to receive a complete message (approximately 40 ms) to permit all incoming messages to reach the drums.

3. Purpose of Monitor Display Counter

a) Each DD 1 (OD 3) and DD 2 (OD 3) pulse is applied to its respective channel chain, except when the LRI monitor is displaying data. Operation of the LRI monitor, fully explained in Part VI, is briefly considered at this point to indicate its effect on the operation of the LRI element. The LRI monitor consists of a control unit and four display consoles at which LRI target data may be presented in PPI form. All LRI messages on their way to the Drum System are sent to the LRI monitor as well. Operators select target data for display at a console by specifying the site identity and the message label of the data of interest. The control unit compares these selection requests to the site identity and message label found in drum word 1. If a selection is accomplished, a display-started pulse is sent to the LRI element, inhibiting further readout during the display cycle, and target information in the second drum word is converted to a form suitable for presentation in a PPI display. The display requires 267.5 usec from the time of the DD pulse which initiated the readout of the message. Ten usec later, a display-ended pulse is returned to the LRI element, confirming the fact that the display has ended, and the readout of LRI messages is resumed. The following example explains the need for preventing readout during display. Assume that one LRI monitor console requests the data received by channel 2 at the same time that another LRI monitor console requests data received by channel 3. Also assume that channels 2 and 3 contain complete messages at the same time. The first DD 1 (OD 3) pulse

applied to channel 2 initiates readout. The data is transferred through the common section to the Drum System and to the monitor control. The monitor starts to arrange for the display on the LRI console that has requested the channel 2 data. The monitor takes 267.5 usec to process and display the information. If, during this time, another DD 1 (OD 3) pulse should appear and cause readout of channel 3, the monitor console requesting channel 3 data could not display this information because the monitor control is still occupied with arranging for the display of the previous message. To prevent this loss of display, all DD pulses and hence, all readouts are inhibited during the display time.

4. Case Study, Generation of Drum-Demand Pulses (Refer to pages 0890 and 0900)

NOTE: This section will be divided into four case studies:

Case #1 - DD 1 Pulse Received
Case #2 - DD 2 Pulse Received
Case #3 - DD 1 and 2 Pulse Received simultaneously
Case #4 - Inhibiting of DD Pulses during LRI Monitor Display.

a) Case #1 - Drum-Demand 1 Pulse Received

The DD 1 pulse is received when an empty slot on drum field 1 is in position to receive data. Drum field 1 receives the data from channels 1-18. The DD 1 pulse passes through GT 1. This DD 1 (OD 3) pulse is sent to the readout control circuit of channel 1 where it will initiate readout (if a channel is ready), or else be passed to the next and following channel. The DD 1 (OD 3) pulse is passed through OR 4 to the LRI Monitor (where it indicates the passage of a message to the Drum System). The pulse also sets FF 2. The set output of FF 2 conditions GT 3 which then passes the following OD 4 pulse. This channels 1-18 DD 1 (OD 4) pulse clears FF's 2 and 3 through OR's 2 and 3, respectively, and also is applied to the readout control circuits of channels 1-18. The lowest-numbered ready channel in channels 1-18 is then readout.

b) Case #2 - Drum-Demand 2 Pulse Received

The DD 2 pulse is received when an empty slot on drum field 2 is in position to receive data from one of the last 18 channels (channels 19-36). The DD 2 pulse passes through GT 2 and is then designated DD 2 (OD 3). This DD 2 (OD 3) pulse is sent to the readout control circuit of channel 19 where it either initiates readout or is passed to channels 20, 21, etc. The DD 2 (OD 3) pulse passes through OR 4 to the LRI monitor and is also used to set FF 3. The set output of FF 3 conditions GT 5, Gate 4 is also conditioned by the clear output of FF 2 (normally cleared). The next OD 4 pulse passes through GT's 4 and 5 as a channels 19-36 DD 2 (OD 4) pulse that is applied to the readout control circuits of channels 19-36. The lowest-numbered ready channel will then read out after receiving the DD 2 (OD 3) and the channels 19-36 DD 2 (OD 4) pulse.

c) Case #3 - Drum-Demand 1 and Drum-Demand 2 Pulses Received Simultaneously

Since channels 1-18 have higher priority than channels 19-36, the simultaneous arrival of DD 1 and DD 2 pulses causes readout of one of the channels 1-18. However, if none of the first 18 channels is ready, one of the channels 19-36 chain is permitted to read out.

The simultaneous arrival of DD 1 and DD 2 pulses causes the DD 1 (OD 3) and DD 2 (OD 3) pulses to be generated. Flip-flops 2 and 3 are both set. The following OD 4 pulse is passed by GT 3, as a DD 1 (OD 4) pulse which clears FF's 2 and 3 and is also sent to the readout control circuits of channels 1-18.

However, should none of the channels in the 1-18 chain be ready, the DD 1 (OD 3) pulse, coming out of channel 18, is delayed 5 usec and clears FF 2 through OR 2. This is illustrated on the timing chart by the dotted no-channel-ready pulse, which causes FF 2 to be cleared (dotted fall line), permitting the channels 19-36 DD 2 (OD 4) pulse to appear (dotted pulse). The OD 4 is then passed through GT's 4 and 5 as a channels 19-36 DD 2 (OD 4) pulse. Therefore, when both

DD 1 and DD 2 pulses appear simultaneously, the resulting pulses generated are the same as those produced for a DD 1 pulse (case #1), unless channels 1-18 are not ready, in which case, the results are the same as those for a DD 2 pulse received along (case #2).

d) Case #4 - Inhibiting of Drum-Demand Pulses during LRI Monitor Display

The inhibition of DD pulses during LRI monitor display time follows the time sequence given below:

1) Time zero: DD pulse initiates the display cycle in the LRI monitor.

2) 10.0 usec: Display-start pulse (OD 3) fed from the LRI monitor, clears FF 1, deconditioning GT's 1 and 2. Reception of DD 1 and 2 pulses is thereby prevented. Clear side of FF 1 conditions GT 7.

3) 17.5 usec: OD 2 pulses begin to pass GT 7, stepping binary counter (FF 5 through FF 9 and GT's 8, 9, 11, and 12).

4) 267.5 usec: OD 2 count reaches 26. FF's 6, 8, and 9 are set, satisfying AND, which conditions GT 10.

5) 275.5 usec: OD 4 pulse passes GT 10 and OR 1, setting FF 1. The drum-demand circuit is thereby activated.

6) 277.5 usec: Display-end pulse is fed from the LRI monitor, resetting counter.

7) 280 usec: First DD pulse, after end of display, is passed.

In the event of a failure of the binary counter, the display-end pulse at 277.5 usec passes through OR 1, setting FF 1, thus assuring the passage of DD pulses. The pulse also passes through GT 6, setting the display time counter alarm, FF 4.

The alarm neon associated with FF 4, on the duplex maintenance console, lights, indicating faulty counter operation. When the circuit operates normally, GT 6 is deconditioned at 272.5 usec by setting FF 1. Accordingly, the display-end pulse is not passed 5 usec later.

If the LRI monitor does not provide a display end pulse (because of circuit failure), the counter is not reset. The AND remains satisfied and GT 10 remains conditioned. FF 1 may be cleared by a display-start pulse, but it is set 2.5 usec later by an OD 4 pulse passing through GT 10.

Therefore, GT 7 is again deconditioned, preventing the counter from being stepped, and GT's 1 and 2 are conditioned, passing DD 1 and DD 2 pulses. Under these circumstances, the circuit has no effect on drum-demand pulses. Thus, it may be seen that the display-end pulse assures the resumption of DD pulses in case of counter failure, but the failure of the LRI monitor does not cause the inhibition of DD pulses.

C. Logic Analysis, Site Identity Generator

1. Introduction 1 site can per channel

The site identity generator provides a means of identifying the LRI radar site that has sent an LRI message. A binary site number is generated and added by the LRI element to the message being sent to the Drum System. The incoming message does not contain the identity of the site that transmitted the message; this shortens the message length and conserves transmission time.

Each radar site transmits LRI messages to the Central, using a 4 telephone lines to two of the input channels. A site identification number is assigned to each message, according to the channel on which it is received.

2. Operation (Refer to Page 0980& Logic A2.4.6)

a. Page 0980 shows the site identity cans for channels 1 and 2 if the binary site numbers for channels 1 and 2 are assumed to be 1001 and 0010, respectively, Channel numbers are assigned as a function of site and priority. The channel 1 site can is wired so that the write signal from channel 1 produces 1's (+10V) on site bit lines 1 and 4. Site bit lines 2 and 3 are connected to -30V, indicating binary 0's on these lines. Since the site number for channel 1 has an even parity (even number of 1's on 1001), the plus on-site odd line is connected to -30V. The channel 2 site number is generated by wiring the channel 2 site can so that the write level from channel 2 produces a 1 on site bit lines 1, 3, and 4 (odd number of 1's in site identity). The plus-on-site odd is made +10V since it is connected to the write level for that channel.

b. The write level from a channel is generated when the channel is reading out the first drum word. Therefore, the binary site number of the channel is generated during the transfer of the first drum word, and is transferred to the site gates when the second message-word data is transferred to the message gates.

The outputs of these OR's are designated site bits 1, 2, 3, and 4 and site odd. When none of the channels is reading data (no write levels), the inputs to (and consequently, the outputs of) these five OR circuits are 0 (-30V). However, when channel 1 generates a write signal, 1's are produced on the channel site bit 1 and site bit 4 lines. These 1 inputs to their respective OR circuits cause the site-bit-1 and site-bit-4 outputs to be 1's for the duration of the write level.

The site-bit outputs of the OR's are sent to the site gates where each site-bit 1 will condition a gate and permit a standard pulse to pass to the Drum System. When channel 1 is reading

out, a 1 is inserted in the first and fourth site identity bit positions on the drum while 0's are being written in the second and third positions. The site odd output is sent to the drum word parity generator where it is used to determine the parity bit of the drum word. During the readout of channel 1, the site odd output is a 0.

c. In a similar manner, the readout of any channel causes the site identity number of that channel to be transferred to the site gates and the parity of the site number to be indicated to the drum word 1 parity generator.

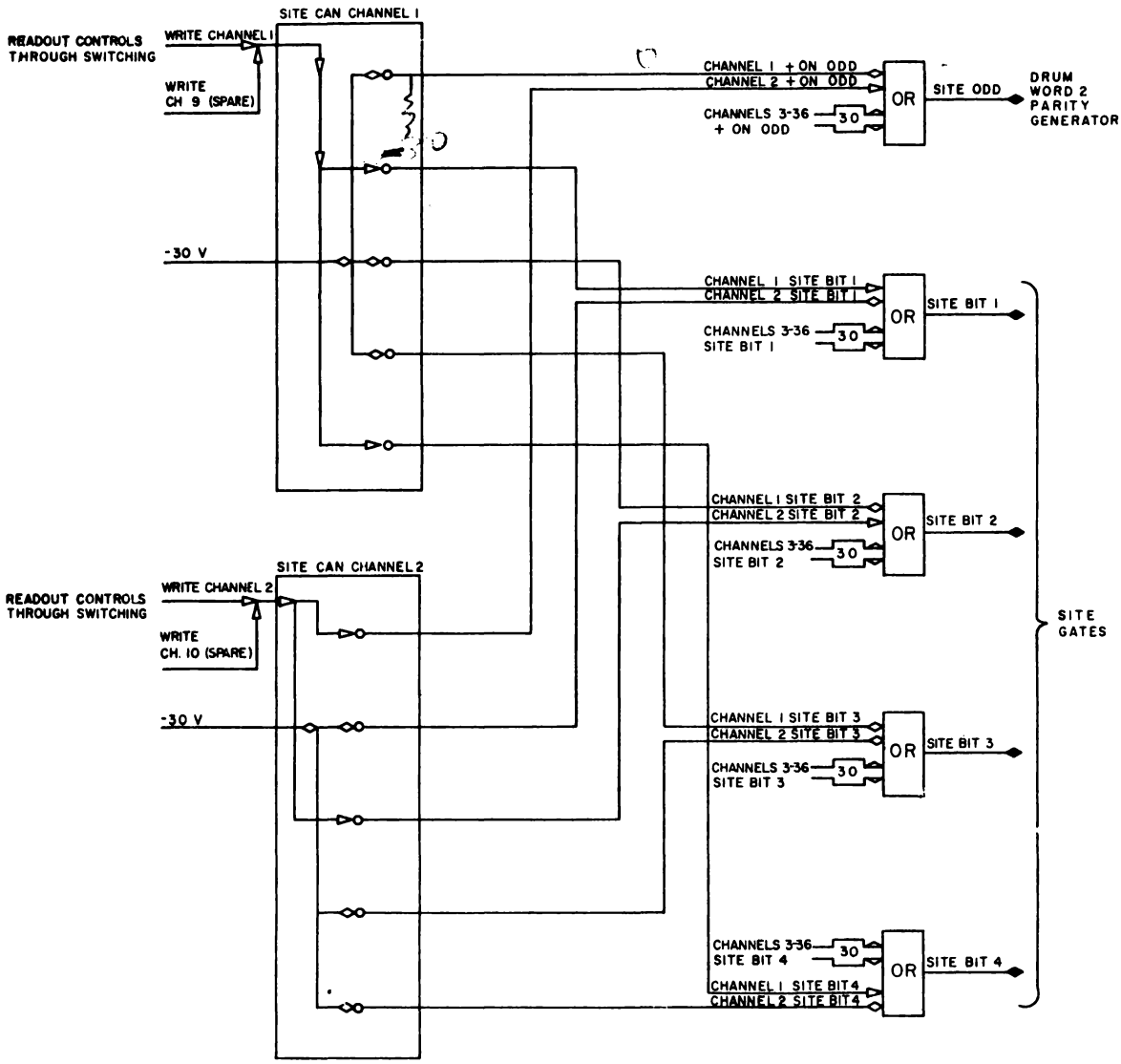
d. The telephone-line inputs to a channel may be connected to a spare channel in the event of failure of a regular channel. The write-level input to each site identity can is, therefore, from the regular channel or substituted channel. The correct site identity is generated for messages received on the spare channel. For example, when channel 1 equipment becomes inoperative, the telephone lines normally connected to channel 1 are switched to channel 9 (the spare channel for the odd channels from 1 through 17). The messages now received by channel 9 originate from the radar site normally connected to channel 1. Since the channel 1 site can is wired to produce the site identity number for this site, the write signal from channel 9 is now connected to the channel 1 site can. In this manner, the correct site identity is added to messages read out of channel 9.

D. Logic Analysis, LRI Clock

1. Characteristics (Refer to page 1000)

a. Six bit counter
b. Controlled by computer clock pulses

1) Stepped every 1/4 second
2) Reset every 16 seconds



Site Identity Generator, Simplified Logic Diagram

c. Indicates relative time that messages are written on drum.

1) Necessary to accurately calculate velocity.

d. Written in second drum word (R1-R6)
e. Parity count is maintained.

2. Synchronizing Clock Control

a. Stepping of clock

1) 1/4 seconds pulses are random with respect to drum timing pulses.
2) Since clock count is transferred on occasion at OD 1-D, it is necessary that clock not be stepped immediately prior to that.
3) An OD 1-D is used which allows a minimum of 10 usec. for FF's to settle.

b. Reset of Clock

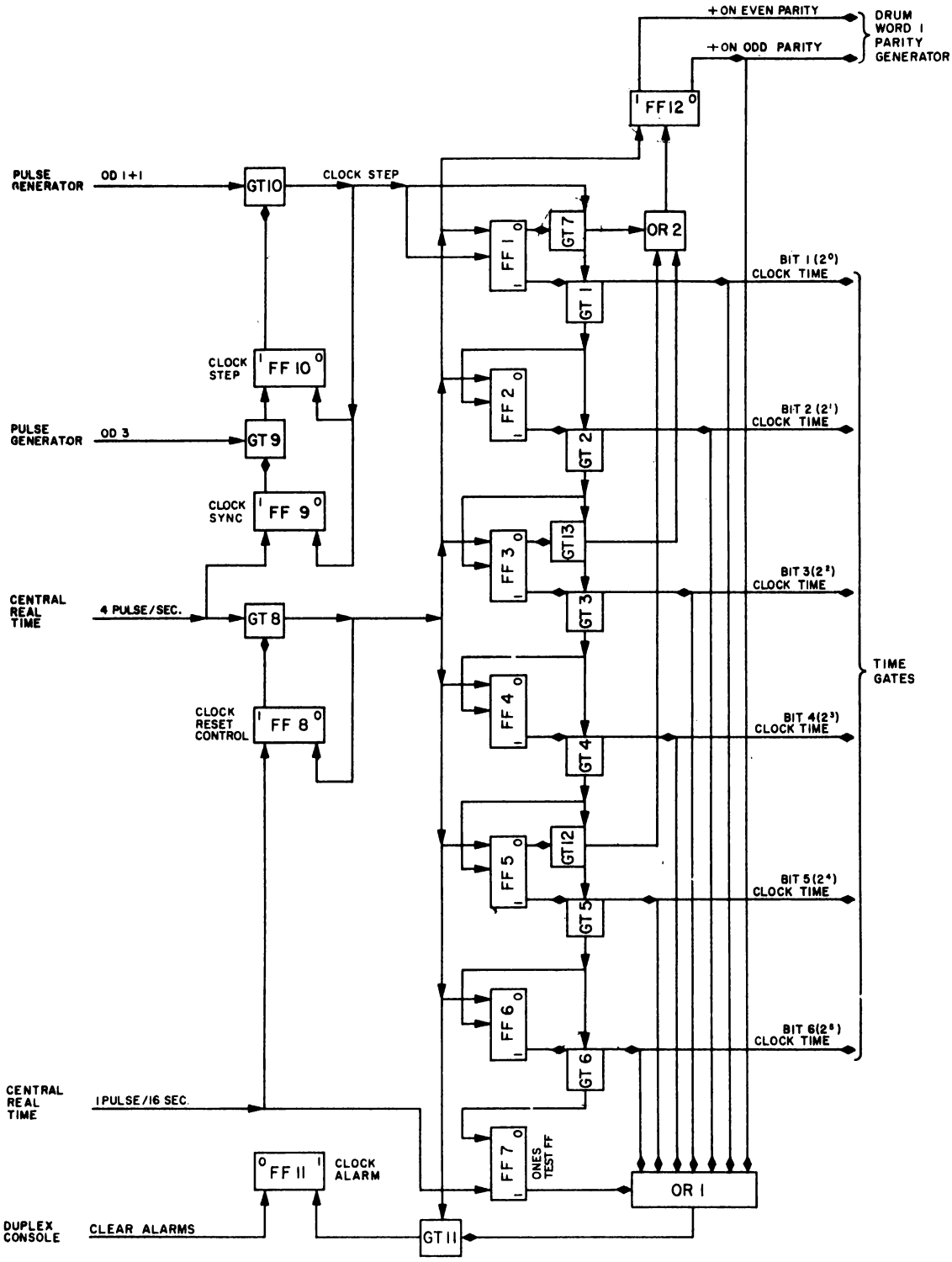
1) Should be reset by end-carry.
2) First 1/4 sec. pulse following 16 sec. pulse ensures counter cleared.
3) Note that 16 sec. pulse will be in coincidence with every 64th 1/4 sec. pulse.

c. Clock Binary Count Output

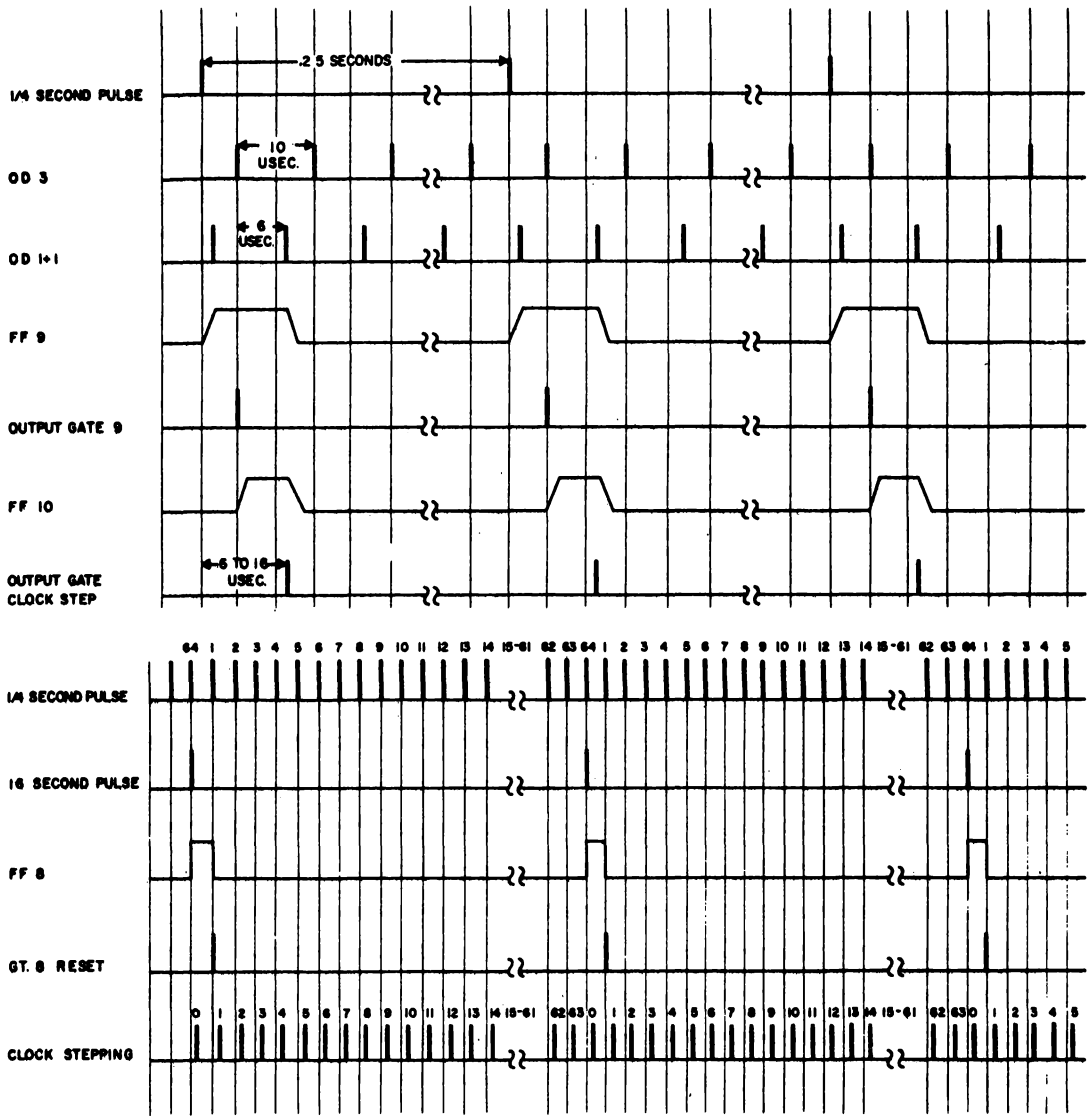
1) Note that GT's will not transfer unless word 1 readout.
2) Note parity set FF is complemented only on even outputs.

d. Parity Count

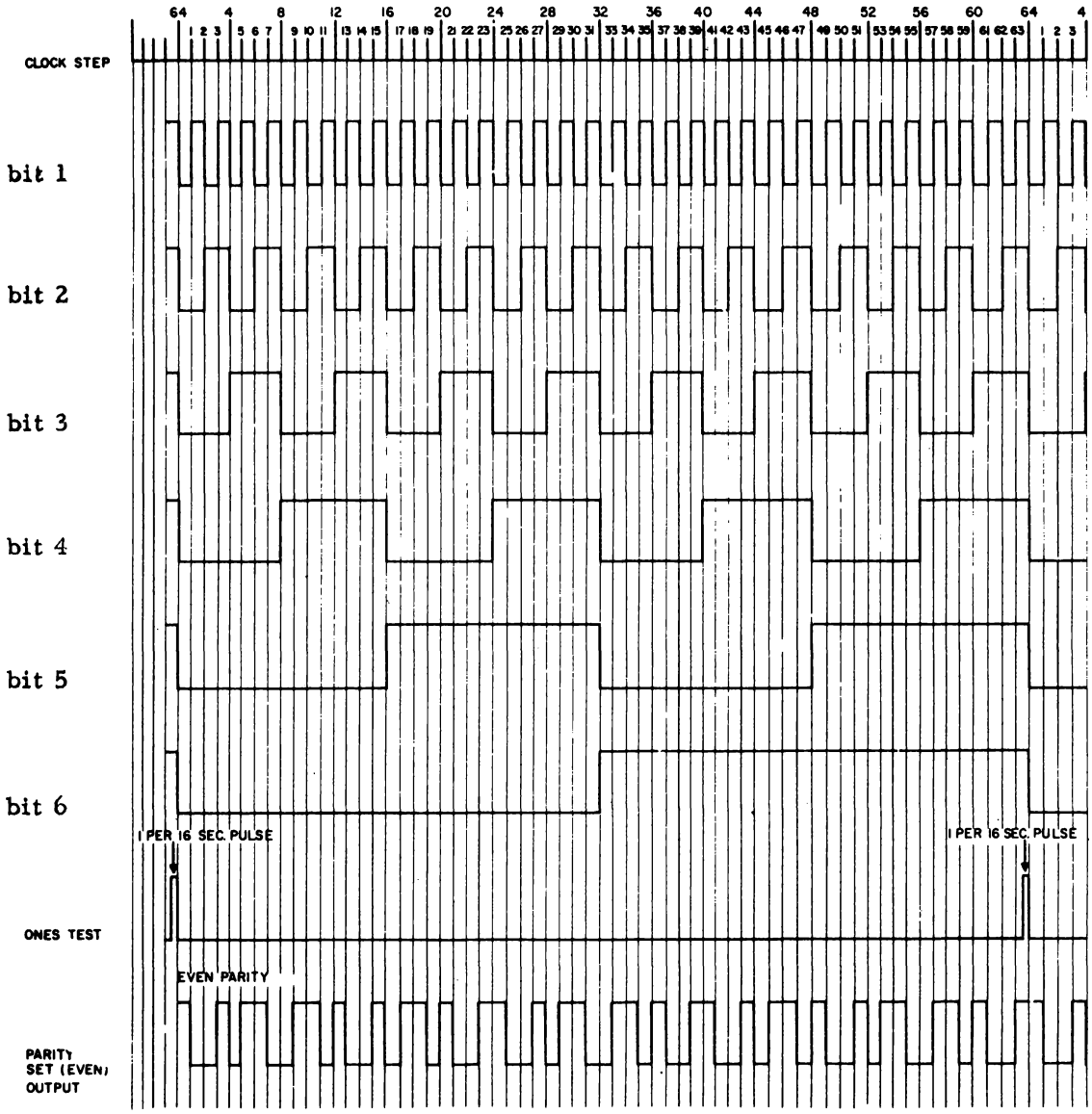
1) Keep count of "1" in clock count - odd or even.
2) Counter cleared - parity - even.



Clock, Simplified Logic Diagram



Clock-Stepping and Synchronizing, Timing Chart



Clock Timing Chart, Binary Counter Output

a) Note that parity changes under the following circumstances.

1 2^0 being set
2 2^2 being set
3 2^4 being set

4) Analysis of circuit on A or B 2.4.6 shows readily how these conditions are put to use.

e. Clock Alarm (Refer to Page 1000)

1) Checks for the following

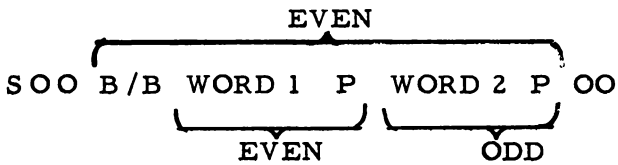
a) Faulty parity count
b) Lack of end carry
c) Counter not being all zeros when reset pulse occurs.

2) Check made with raw 1/4 sec. pulse following 16 sec. pulse - no alarm if reset pulse does not occur.
3) An alarm turns on light on duplex maintenance console.

E. Logic Analysis, Parity Generation

1. Parity Counts

a. Inputs parity (phone line)

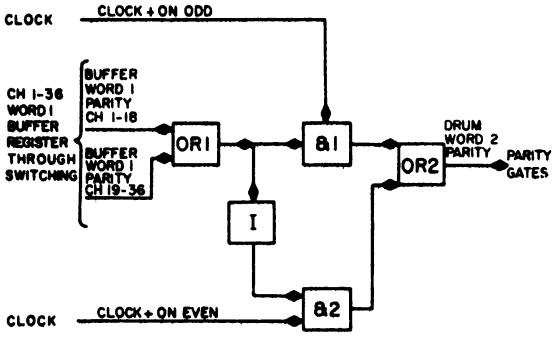


1) Word 2 (Part of first drum word)

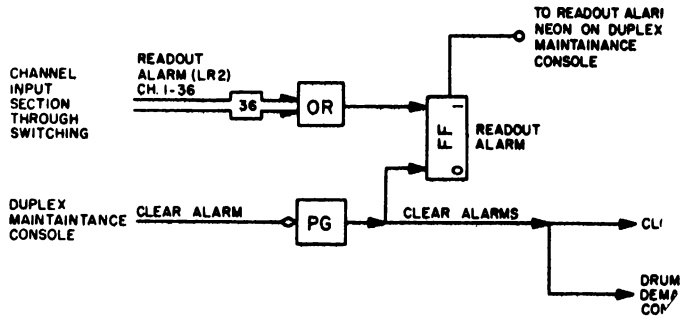
a) P = 0 - data has odd number of 1's.
b) P = 1 - data has even number of 1's.

2) Word 1 (Part of second drum word)

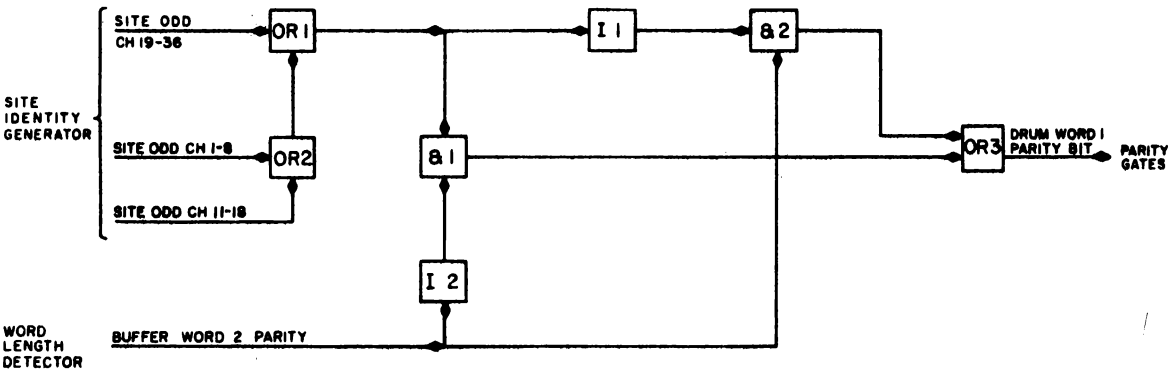
a) P = 0 data has even number of 1's.
b) P = 1 data has odd number of 1's.



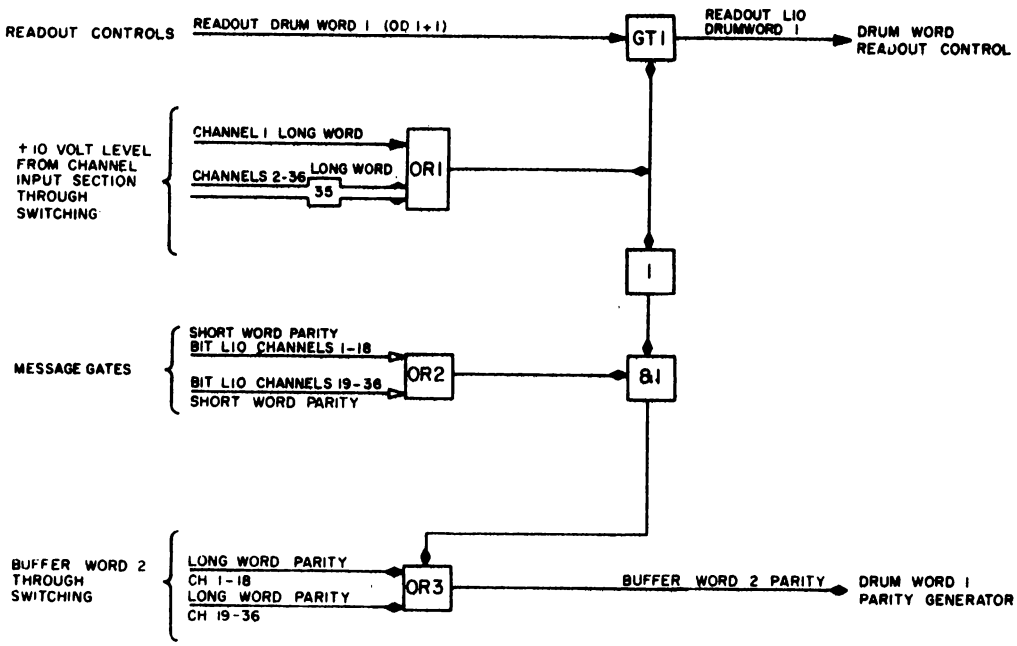
Drum Word 2 Parity Generator, Simplified Logic Diagram



Readout Alarm, Simplified Logic Diagram



Drum Word 1 Parity Generator, Simplified Logic Diagram



Word-Length Detector, Simplified Logic Diagram

b. Site identity (first drum word)

1) Site odd level (plus) - site identity odd
2) Site odd level (minus) - site identity even

c. Clock (second drum word)

1) Time odd level (plus) - clock count odd
2) Time even level (plus) - clock count even

2. Generation of First Drum Word Parity

a. Long word level is result of previous equipment operation. Will always be +- 10V. Associated circuitry will be removed at some convenient time in the future. (41HV B2).

b. Desired Results

1) If Word 2 parity is "1", a positive level will result indicating an even number of 1's.
2)

Word 2 Parity	Site Identity	Drum Word 1 Parity
1	Odd	0
1	Even	1
0	Odd	1
0	Even	0

c. Establish Conditions & Analyze on Page 1040

d. Logic analysis should be made.

1) Level generated is erroneously labeled "Parity Drum Word 1".

3. Generation of second Drum Word Parity

a. Desired results

1) If word 1 parity is "1", a positive level will result indicating an odd number of 1's.

a) Note - BB was originally in Parity Count - when dropped will change Parity Count.

2)

Word 1 Parity	Clock	Drum Word 2 Parity
1	Odd	1
1	Even	0
0	Odd	0
0	Even	1

b. Establish conditions & analyze on Page
c. Associate with logic

1) Level generated is erroneously labeled "Parity Drum Word 1"

F. Logic Analysis, Drum Word Readout Controls

1. Introduction

The drum-word readout controls circuit initiates the readout of messages to the drum by the generation of data-available and word-read out pulses. The circuit receives the write (OD 4 to OD 1 / 1) levels from the readout control circuits in the 36 channels. A write level is generated by a channel during the readout of the message. Only one channel at a time is able to read out messages: therefore, only one of the 36 write levels is present at any one time. The write-level lines for channels 1-18 are combined into a single output (channels 1-18 write) by OR 1. This combined output produces a /10V write level when any one of the first 18 channels is read out. Similarly, the channels 19-36 write lines are combined into a single output (channels 19-36 write) by OR2. The following pulses are generated by the circuit when one of the channels is read out (producing a write level):

a. Data-available-drum-field-1: Two successive OD 1 / 1 standard pulses are sent to the Drum System when a write level is produced by one of the first 18 channels. Since data from channels 1-18 is written on drum field 1, these pulses indicate to the drum System that drum field 1 is to receive the data.

b. Data-available-drum-field-2: Two successive OD 1 / 1 standard pulses are sent to the Drum System, indicating that one of the last 18 channels (channels 19-36) is transferring data to drum field 2.

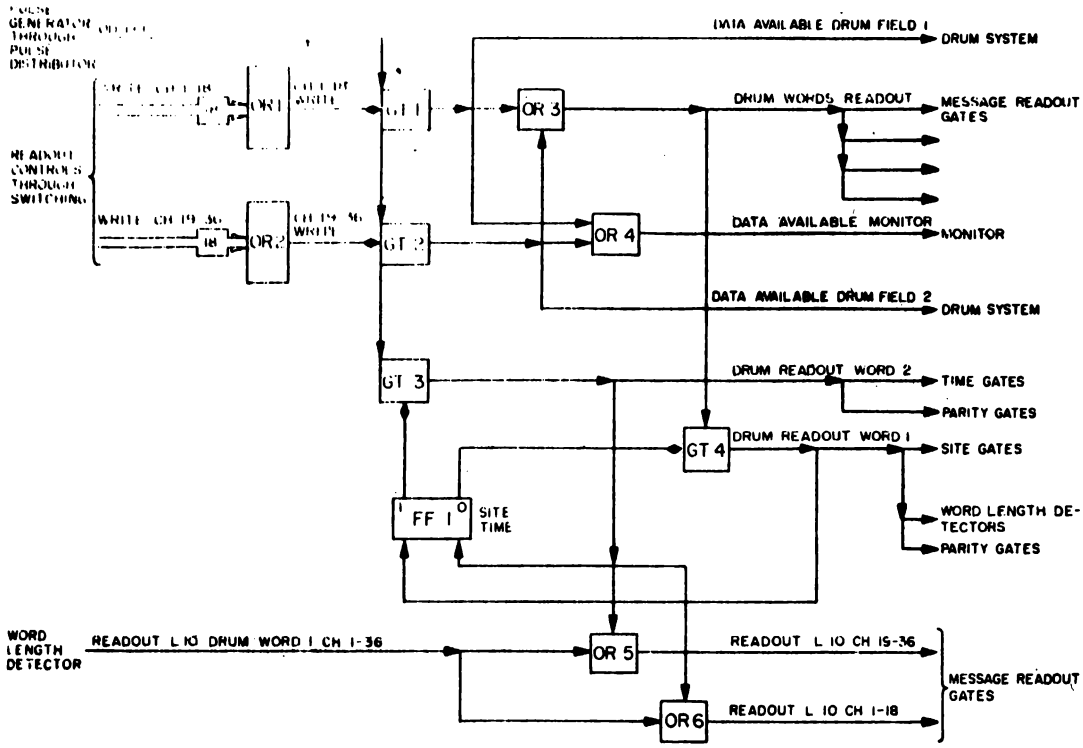
c. Data-available-monitor: Two successive OD 1 / 1 standard pulses indicate to the monitor that data is being transferred from one of the 36 channels to the Drum System.

d. Drum-word-readout: Two successive OD 1 / 1 pulses are synchronized with the readout of word 2 and word 1 buffers. These pulses strobe the message readout gates that send data to the drums.

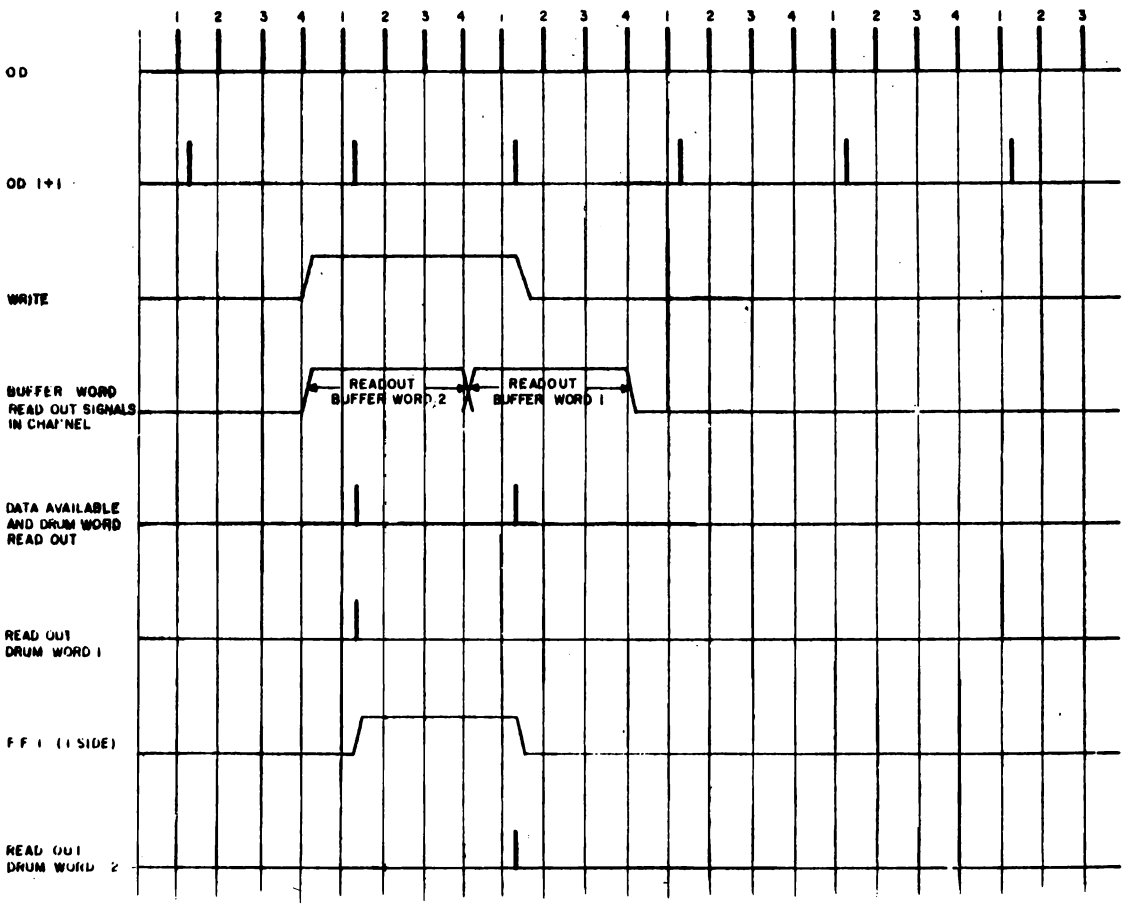
e. Readout-drum-word-1: A single OD 1 / 1 pulse occurs when the second buffer word is being read out of the word 2 buffer register of a channel. Since the second buffer word is read out before the first buffer word, the first drum word is formed by the second buffer word plus site identity. The readout-drum-word-1 pulse strobes the site gates, thereby inserting, the site identity into the first drum word.

f. Readout-drum-word-2: An OD 1 / 1 pulse occurs when the first buffer word is being read out (second drum word being formed). This pulse strobes the time gates, inserting the clock output into drum word 2.

g. Readout-L10: Because of previous circuitry, the readout of bit L10 was treated in a separate manner. For convenience in revising the circuitry, the bit L10 readout is still treated as a special situation. However, as a practical consideration, the readout control circuit generates two OD 1 / 1 strobing pulses which are sent to the L10 message gates. The two L10 (OD 1 / 1) pulses are synchronized with the drum word readout pulses to the remaining message gates.



Drum Word Readout Controls, Simplified Logic Diagram



Drum Word Readout Controls, Timing Chart

2. Operation

Note:

Refer to logic and timing chart on Page 1080

a. Write Level

1) From channel being readout
2) Up for 13.5 usec. DD(OD4) to second OD1-D
3) Two OD1-D's gated through as:

a) Data available
b) Readout L & R half words

b. First OD1-D finds "site time" cleared,

1) Generates "Word 2 readout"
2) Sets "site time"

c. Next OD1-D

1) Generates "Word 1 readout"
2) Clears site time

Note:

Error in timing chart

1) Readout Word 2 Buffer doesn't drop until next OD1-D - same as "Write" level.

G. Message Gates, Readout Circuitry

1. The readout gates to the LRI fields on the drum are as follows:

a. Site bits, PU 41GU (8B)
b. Time bits, PU 41GJ (8A)
c. Message bits, Logic 1-7, A-E

2. Message Readout Gates Operation (Refer to Page)

   a. The nonstandard output from the tape cores is applied to a level setter through OR's and is converted to a standard level (±10V) which conditions the GT's. The first drum-word-readout pulse then strobes the GT's and is passed to the remaining OR's. The output of the OR's (a standard pulse) is then amplified by PA's, and transferred to the drum fields. Ten usec later, the output of the word 1 buffer register is applied to the OR's. The second drum-word-readout pulse is passed causing a word to be inserted into position in drum word 2. This pulse is also sent to the monitor. Page 1120 shows the timing relationship for the formation of a 1 bit. The readout of the bits from the buffer registers is accomplished during the application of the word readout levels to buffer register 2 and buffer register 1. The drum word readout pulses strobe the gates and are passed as 1 bits when the related core in the buffer register has an up-level output.

   b. The clock time and site identity data is presented to the drum by applying the output of the time and site gates to the PA (through OR circuits) for the drum bits that receive this data.

   c. The insertion of a clock bit 6 (highest order bit of clock time) into the R1 bit position is shown in detail on the logic diagram Page 1120 . When the first drum word is formed, the R1 output of buffer word 2 is sent to the Drum System and to the monitor. The R1 output of buffer word 2 will appear on one of the input lines (R1, channels 1-10, 11-18, 19-28, 29-36). During the readout of buffer word 1 (formation of drum word 2), the R1 inputs from the 36 channels are all 0's since there is no R1 output from the word 2 buffer.

Message Readout Gates Operation (continued)

At OD 1 / 1 (drum-word-2-readout pulse), clock bit 6 is passed through OR 5 and OR 6 to the Drum System and the monitor. In the same manner, the remaining clock bits are inserted into the R2-R6 positions of the second drum word. The site identity bits from the site gates are similarly inserted into the R12-R15 positions of drum word 1. The site bits are presented as an OD 1 / 1 drum-word-1 readout pulse for 1 bits. The R12-R15 inputs from the channel during formation of drum word 1 are all 0.

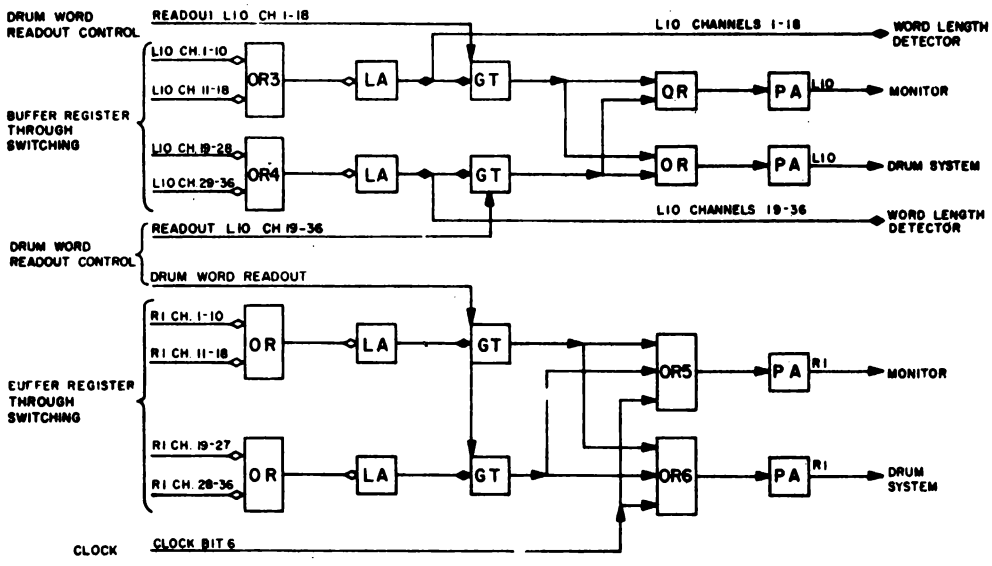
H. Word Length Detector Circuit

1. Purpose

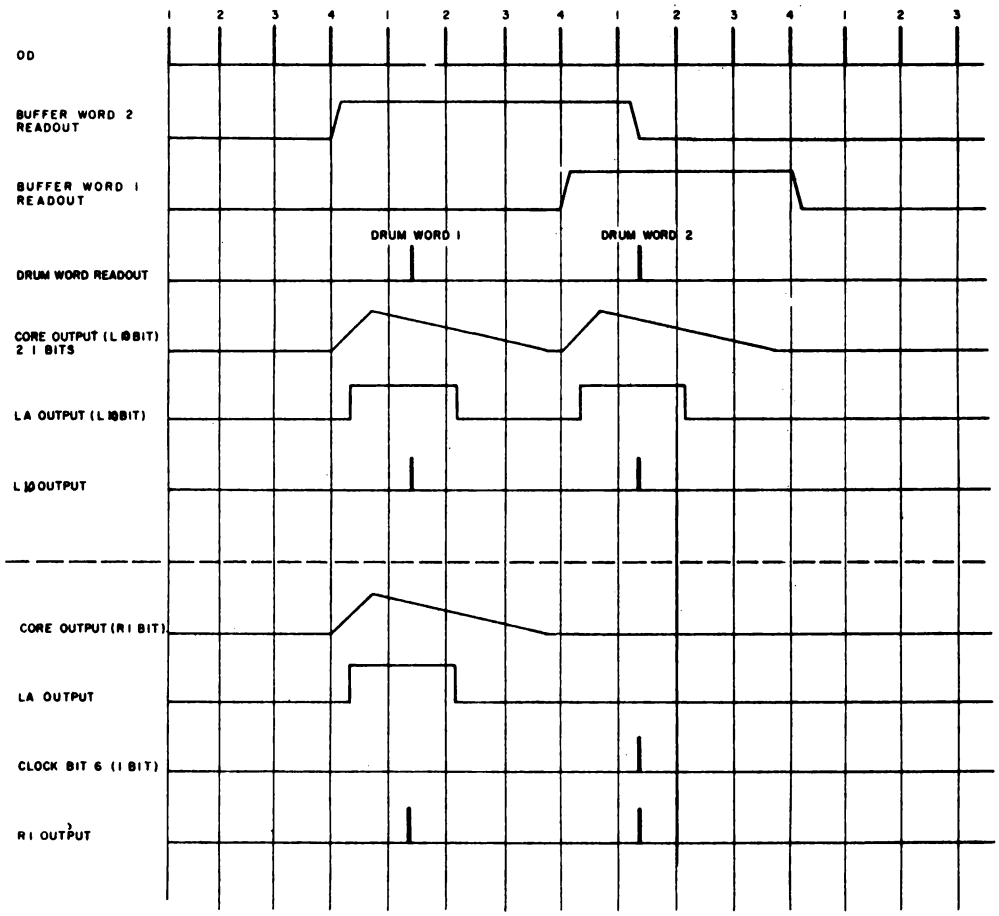
The word-length detector circuit was designed to detect a variable length in message word 2. However, a message word format change established a fixed word length for message word 2. The word length detector circuit now functions only to relay the buffer word 2 parity bit to the drum word 1 parity generator and to forward the readout-drum-word-1 (as the readout L10 drum word 1) pulse to the drum word readout control circuit.

2. Operation

A /-10V level from the channel input section is passed by OR 1 to GT 1 and to the inverter. Consequently, the level input to GT 1 is a constant /10V and the input to AND 1 from the inverter is a constant -30V. Gate 1 passes a readout-drum-word-1 pulse (when received) as a readout-L10-drum-word-1 pulse to the drum word readout control circuit. AND 1 is constantly deconditioned by the inverter and does not pass any signals. OR 3 receives the parity bit (designated as the long-word-parity channels 1-18 and 19-36 level), and forwards the signal to the drum word 1 parity generator as the buffer word 2 parity bit.



Message Gates, Simplified Logic Diagram



Message Gates, Timing Chart

The drum word 1 parity generator utilizes the buffer word 2 parity bit to establish the overall parity bit for drum word 1.

I. Readout Alarm Circuit

1. Purpose

The readout alarm circuit generates a visual alarm on the duplex maintenance console when any of the LRI channel sections has generated a readout alarm pulse. The readout-alarm pulse indicates that an incoming message cannot be placed in the buffer registers because a previous message is still contained in the buffer registers awaiting transfer to the Drum System. The incoming message is then destroyed in the primary registers.

2. Operation

The readout alarm circuit receives the readout-alarm pulses from all 36 channel sections. These 36 outputs are combined into a single-channel 1-36 readout alarm input. The combined input is applied to the set input of the readout alarm flip-flops. When any of the 36 channels generates a readout-alarm pulse, cFF8 (PU 41HN) is set, lighting a neon on the duplex maintenance console. The flip-flop remains set until a clear alarms level from the duplex maintenance console is applied to the pulse generator by depressing a CLEAR ALARMS switch. The pulse generator then produces a standard pulse which clears the flip-flop, turning off the neon. The clear-alarm pulses are also used to reset the clock alarm flip-flop in the clock circuit and the display counter alarm flip-flop in the drum demand control circuit.

J. Review of LRI Control Panels on Simplex Maintenance Consoles

1. Review section IG of Lesson Plan
2. Unit Status Switch

a. Review section IV B of this Lesson Plan
b. Manual controls on Panels (Page)

1) Source switch - each channel (S6)

a) Off - no data input to channel
b) Data - input from phone line
c) Test - input from test bus - must be in standby or standby MC

2) Parity Disable - each channel - only in standby (S5)

a) Off - no action
b) Parity disabled - a parity error will not result in data being lost

3) Channel Ready Test - each channel (S5)

a) Normal - normal operation
b) Test - simulates open filaments to "Channel Ready" FF for test of circuit

4) Data Circuit - each channel (S6)

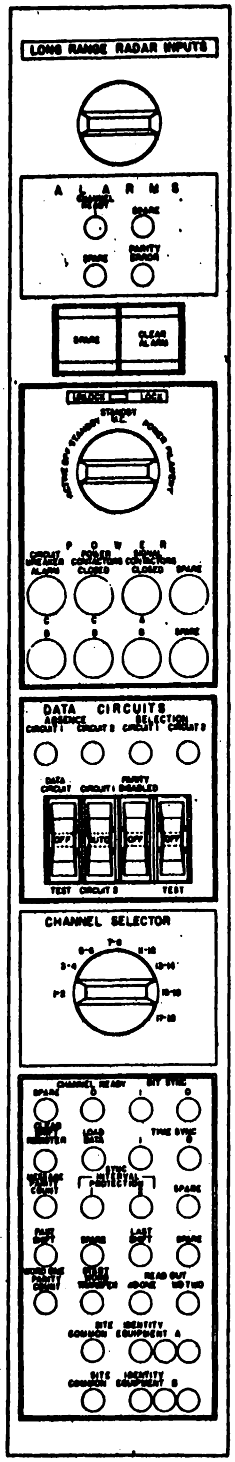
a) Circuit 1 - circuit 1 data feeds channel and Circuit 2 data feeds spare.
b) Circuit 2 - opposite of Circuit 1
c) Auto - provides auto switching of Circuit 1 and 2.
d) Circuitry to be discussed during Crosstell - including absence indicator and selection indicator lines from Unit 97.

c. Channel Indicators

1) Neons are tied to channel FF's

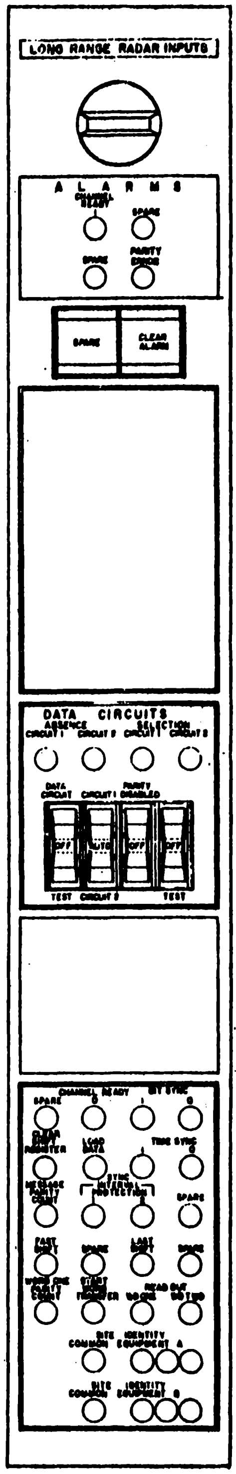
d. Spare Channel Selector Switch (S7)

1) Module E & T conversion (Chart IV)



NOTE:
CHANNEL [illegible] SHOWN AS DRAWN
CHANNEL 17 HAS REQUIRED
NUMBERS ON THE CHANNEL
SELECTOR SWITCH ALL OTHER
ODD PANELS HAVE A BLANK IN
PLACE OF THE CHANNEL
SELECTOR SWITCH

LRI Control Panel, Odd and Odd-Spares



LRI Control Panel, Even and Even-Spares

2) Controls both channels in module 41EH(K1)(K2)
3) Selects correct phone line circuit 41EH(K1)(K2)
4) Selects correct circuit indicators 41EC(K1)(K2)
5) Switches Write Level 41EK(K1)

K. LRI Controls and Indications on Duplex Maintenance Console

1. Refer to Page 1180

2. Panel located on Module D (lower) of Unit 1.

3. Clear Alarms Pushbutton.

   a. Will clear any of all three alarms.

4. Indicators

   a. Readout Alarm

      1) Logic A2, 4, 6 (13C) cFF8.

   b. Clock Alarm

      1) Logic A2, 4, 6 (9A) cFF9.

   c. Clock Parity

      1) Logic A2, 4, 6 (10A) cFF8.

   d. Clock Reset Control

      1) Logic A2, 4, 6 (12A) cFF2.

   e. Clock Sync

      1) Logic A2, 4. 6 (12A) cFF5

   f. Site Time Readout

      1) Logic A2. 4. 6 (10C) cFF6.

g. Clock One's Test

1) Logic A2.4.6 (9A) cFF7.

h. Clock Time

1) Logic A2.4.6 (9-11A)

i. Clock Stepping

1) Logic A2.4.6 (12A) cFF7.

j. Pulse Generator

1) Logic A2.4.6 (10D) cFF1.

k. LRI 1/2 Lever, Channel 1-18 and 19-36

1) Logic A2.4.6 (8E) aFF34 and aFF3

l. Monitor

1) Logic S2.4.5 (8A) cFF3.

m. Drum Demand

1) Logic S2.4.5.

a) #1 - aFF34
b) #2 - cFF7

n. Display Counter Alarm

1) Logic S2.4.5 (7B) cFF6.

o. Display Time Counter

1) Logic S2.4.5 (5-7A).

Summary Questions

1. What would be the effect on the LRI clock if 41HHB2 were shorted to ground? (Clock could not be stepped and a clock alarm would result.)

2. If Channel 9 is replacing Channel 1, which has a Site identity of 0001 and is feeding data to common A, which Site identity neons on Channel 9 panel will be on? (none)

3. (Logic A2.4.6) Which of the following conditions would result in a clock alarm but not affect clock counting?

   a. FF-6, 41HG remains set.

   b. GT-3, 41HH non-conductive.

   c. A missing 16 second pulse, all 1/4 second pulses normal.

   d. GT-5, 41HF non-conductive.

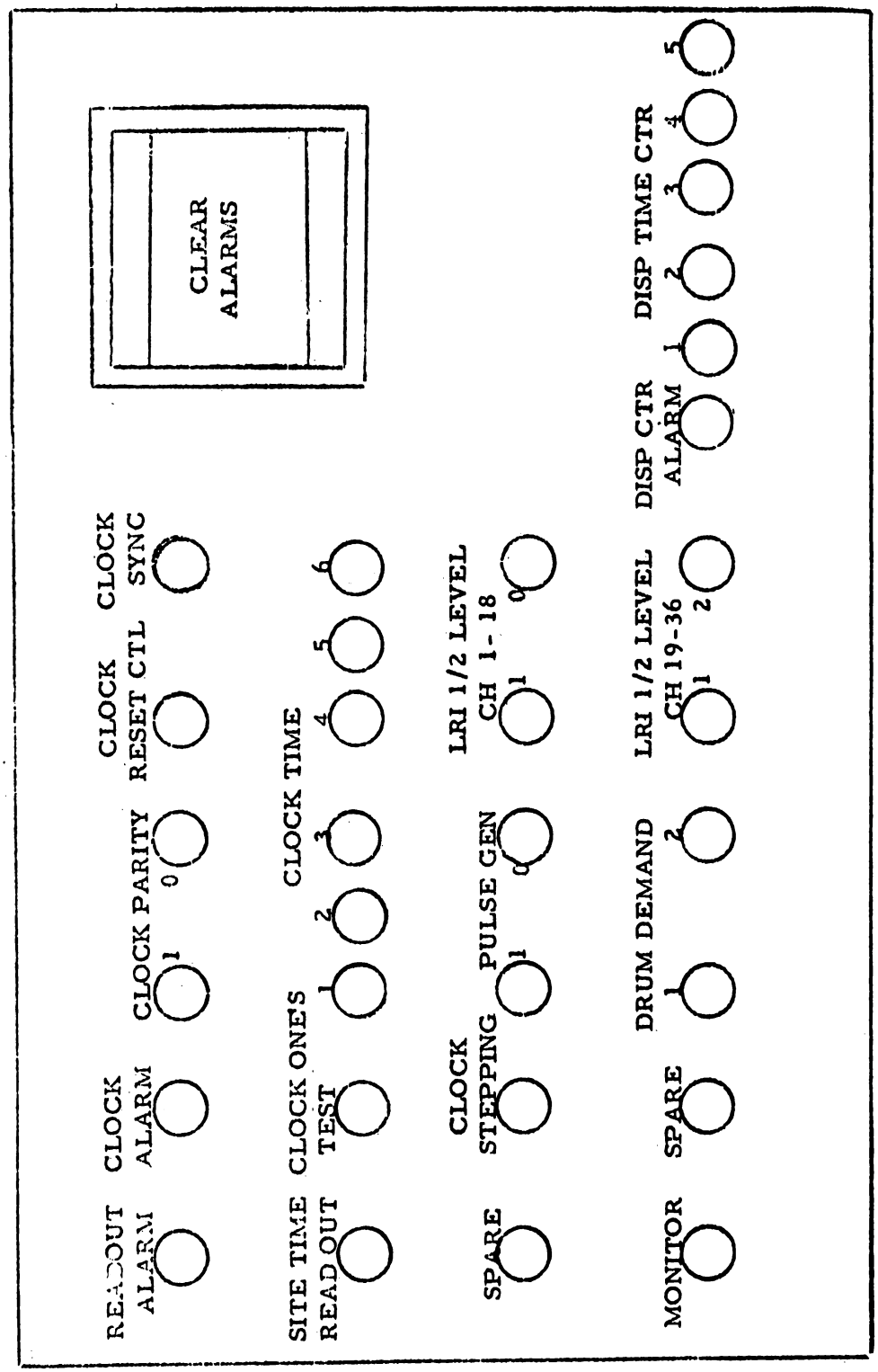
   e. A missing 1/4 second pulse.

4. (Logic A2.4.6) FF-2, 41HF operates normally but GT-3 41HF passes all pulses. What would be the clock time indicated 5.1 seconds after the next 16 second pulse? Will this result in a clock alarm at the next 16 second pulse time?

5. Channels 1, 2, 19 and 20 are assigned to common "B". Channels 3, 4, 21 are assigned to common "A". All other channels are "off". Data from channels 21 and 22 does not transfer to the drum. All other channels function normally. This could be due to which of the following pluggable units removed:

   a. 41FD (B2.4.6)
   b. 41UD (A2.4.6)
   c. 41G(BB) (S2.4.5)
   d. 41GY (S2.4.5)
   e. 41V(BB) (S2.4.5)

6. (Logic A2.4.6) indicates what parity ("1" or "0") will be generated for each drum word with the following conditions.



LRI CONTROLS AND INDICATORS ON THE DUPLEX MAINTENANCE CONSOLE

	Msg. Word #1	Msg. Word #2	Clock Time	Site Identity	DW #1	DW #2
a.	odd	even	odd	even		
b.	even	odd	even	odd		
c.	even	even	odd	odd		
d.	odd	odd	even	even		
e.	odd	odd	odd	odd		
f.	even	even	even	even		
g.	even	odd	odd	even		

7. (Logic A2.4.6) Drum word #2 parity level at 41HVEs might remain positive (/ 10V) for as long as:

   a. 7.5 Microseconds
   b. 10 Microseconds
   c. 10 Microseconds
   d. 250 Microseconds
   e. 16 Seconds

8. (Logic A2.4.6) 41HUB2 open (12C). Which statement is most correct?

   a. If site identity for Channel #12 is odd and parity bit for message word #2 is a "1", we will generate correct parity.

   b. If site identity for Channel #12 is even and message word #2 data is even, we will generate correct parity.

   c. If site identity for Channel #12 is even and message word #2 data is odd, we will write a "1" for drum word #1 parity.

   d. If site identity for Channel #1 is odd and message word #2 data is odd, incorrect parity will be written for drum word #1.

   e. None of the above statements are correct.

9. (True or false Logic A2.4.6) Under normal conditions, "Data Available #1" pulse will always preceed "Data Available #2" pulse.

10. (Logic A2.4.6) A single LRI message is received at Channel #2 from the phone lines. The contents of this message are - RANGE - $(617)_8$, ASIMUTH - $(2030)_8$, MESSAGE LABEL $(3)_8$, TIME DELAY $(1)_8$. Channel #2 site identity is $(2)_8$ and the message is received seven seconds after a computer clock 16 second pulse. Channel #2 is assigned to common "A". List each pluggable unit pin number at which a pulse will be sent from to the Log Drum (Unit 22 only), for Drum Word 1. Do the same for Drum Word 2.

11. (Logic A2.4.6) cFF-6 in 41GX (11C) has open filaments. Channels 3, 4, 7, 8, 25, and 26 are all assigned to common "A" and to the drum. Which statement best describes the result of this problem?

    a. Data would be written on the drum from each channel in normal sequence, clock time would be written in both drum words of a Height Finder Message.

    b. Data would be written on the drum from each channel in normal sequence, however, Range, Azimuth and Time Delay in all FGD and Mark X messages would most likely be incorrect.

    c. Channel #3 would write on drum. Other channels would never write.

    d. All messages would be written on drum, the only affect would be loss of Site Identity bits and Clock Time bits.

    e. Site Identity and Clock Time would be written twice for each message, other data would not be affected.

12. Explain briefly how you arrived at your answer to Question #72. Why are the other possible answers wrong?

13. (Logic A2.4.6) 41HVA1 (12B) is open. A message is received by Channel #13. Message Word #2 has a "1" for parity bit. What will the parity bit generated for Drum Word #1 be? What should it have been?

14. (Logic A2.4.6) 41HVH2 (9C) is open. A message is received by Channel #10. Message Word #1 has a "D" for parity bit. What will the parity bit generated for Drum Word #2 be if the message is written on the drum 3.5 seconds after 16 second pulse? What should it have been?

15. (Logic A2.4.6) Channel #1 transfers a FGD message to "A" drum with an odd number of "1" bits in message word #1 one second past the 16 second pulse. Two seconds later, Channel #2 writes on the "A" drum with an odd number of "1" bits in Drum Word #2. Two seconds later, Channel #5 writes on the "A" drum with an even number of "1" bits in Drum Word #2, One second after Channel #6 writes, Channel #11 writes with an even number of "1" bits in Drum Word #2. When the Clock Count becomes $(50)_8$, Channel #13 writes the same Range and Azimuth on the "A" Drum as did Channel #11. An SDR 34 instruction is then placed in the "A" Computer. A Drum Parity Alarm is generated when Channel #2 and Channel #11 messages are read off. The other four messages are accepted. Which one of the following malfunctions could have caused these parity errors and not have caused parity error in the other four messages?

    a. 41HVH1 (9C) open.
    b. 41HVH2 (9C) open.
    c. cFF8 in 41HG (10A) open filaments
    d. 41GUF6 (9C) open.
    e. 41HGH2 (10A) open.

VI. LRI Monitor Binary Section (Systems 17 and Beyond)

A. Introduction to LRI Monitor

After System 16, a radical change was made in the LRI Monitor circuitry. This change was made in the binary section of the monitor control.

1. Purpose of the LRI Monitor System

a. The LRI monitor provides a visual means of checking the quality of LRI data after it has been processed by the Input System, but before it is made available to the Central Computer. It thus enables operational personnel to make preliminary analysis, independently of the Central Computer, of the air situation as seen by long-range radar. In addition, it permits maintenance personnel to evaluate the operational efficiency of the Input System, assisting in general localization of troubles. Specifically, the LRI monitor may be used to perform the following functions:

1) Assist in comparison of LRI data before and after processing by the computer.

2) Provide coverage of data source by showing raw data and display of clutter.

3) Check LRI channel equipment during initial installation, and subsequently.

4) Take photographic records of LRI data before it has been processed by the Central Computer.

b. To perform these functions, three display consoles are provided:

1) ASO Unit 623, located in the air surveillance are and utilized by the air surveillance officer.

2) Unit 622, located in the maintenance area and utilized by maintenance personnel.

3) MSP Unit 620, located in the Air Surveillance area and controlled by the mapper supervisor.

c. Physical Description

1) Note Page 1270 (Position of LRI Monitor in input system).

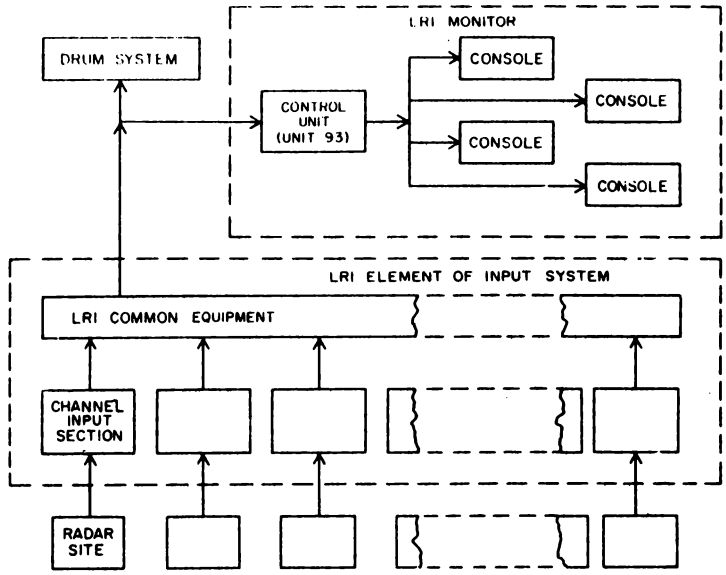
2) The LRI monitor consits of the three display consoles referred to above, and Unit 93, the LRI monitor control unit. Associated with the monitor for control purposes is the auxiliary control console Unit 953 (part of the Display System). Information is selected for display by means of pushbutton keyboards at the consoles or at Unit 953 and is then presented by the cathode-ray tube (CRT) in each console. Unit 93 contains the circuitry which serves all three consoles.

2. Data Transfer to LRI Monitor

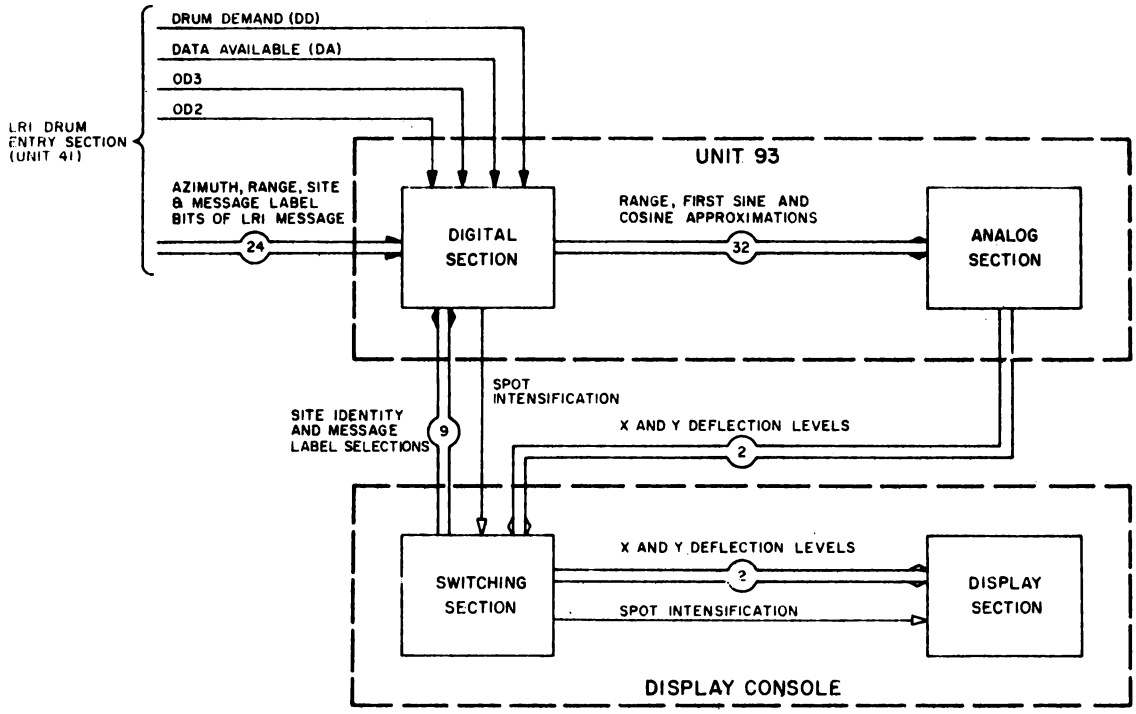
a. Data to drum also goes to monitor control

1) L1 - L15
2) R7 - R15

NOTE: 24 Transfer Lines



Position of LRI Monitor in Input System



NOTE:
ONLY ONE OF THE FOUR DISPLAY CONSOLES IS INDICATED. THE SAME SIGNALS ARE FURNISHED TO OR BY THE SWITCHING SECTION CIRCUITS FOR THE OTHER CONSOLES, EXCEPT FOR SPOT INTENSIFICATION; THIS GOES ONLY TO THE CONSOLE(S) WHICH HAVE SELECTED THE MESSAGE

LRI Monitor Functional Diagram

b. Control Pulses to Monitor

1) OD2 & OD3
2) Data Available
3) Drum Demand

c. Control Pulses from Monitor

1) (OD3) Display Start
2) (OD2) Display End

d. Note Page 1320 (LRI Monitor Functional Diagram)

1) Control Inputs
2) Data Inputs
3) Unit 93 Outputs

3. Description of Unit 93

a. In Systems 1-16, Unit 93, Modules A and B contain digital circuitry.

In System 17 and beyond Unit 93, Module B contains all digital circuitry. 93 Module A, therefore, has been eliminated.

b. Unit 93, Module C contains analog circuitry.

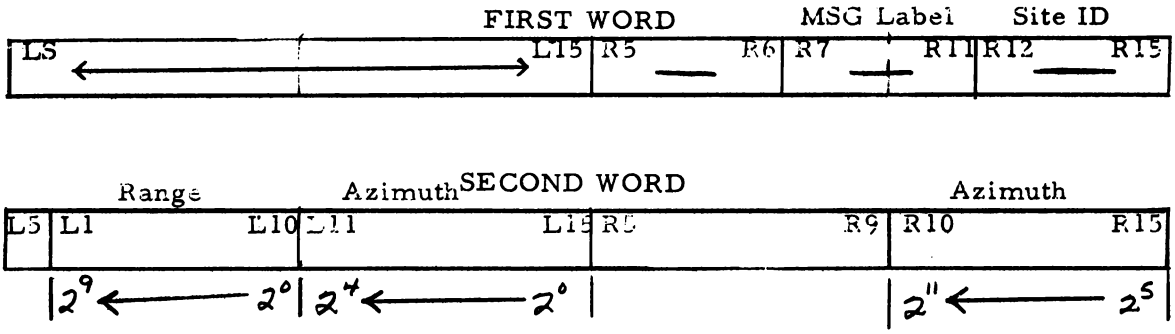
c. Any of the 3 consoles can receive data from either A or B Common, depending upon their status.

d. Auxiliary Console 953 has remote controls for Console 620. They are located in Air Surveillance Room.

e. Console 622 and 623 have their own controls.

1) 622 located in input room near 93A & B.
2) 623 located in air surveillance room.

4. Composition of LRI Message to Monitor.



a. Note: Study the reverse position of the Range and Azimuth bits.

1) Positions of bits will be important for decoder analysis.

B. Block Diagram Analysis of LRI Monitor

1. Refer to Page 1320 for block diagram.

2. The function of the LRI monitor is to select, process and display, in a PPI presentation, messages prepared by the LRI element for transfer to the drums. To perform these functions, the LRI monitor utilizes four functional sections: digital, analog, display and switching. The sections are described briefly below and in detail in the following sections. The relationship between the four sections is illustrated on Page 1320.

3. Digital Section Block Diagram

a. Word Discriminator - determines whether data in storage registers is Range and Azimuth or Site Identity and Message Label.

b. Site and Message Label storage registers - stores site identity and message label while a comparison is made with each of 4 consoles to determine if message should be displayed.

c. Site identity sel - 2 positive outputs if a comparison is made between bits.

d. Single message label sel. - a positive output if a comparison of bits is made.

e. Mult. message label sel. - a positive output if all messages are to be shown and message is not a HF message. (HF = Height Finder)

f. Display Timing Unit - sends control pulses to common LRI equipment and controls intensification pulses to consoles.

g. Range storage register - conditions range decoder with range count.

h. Sine and cosine storage registers - condition 90° out of phase respective decoders with modified azimuth count.

i. Register corrector - modifies azimuth count in sine and cosine storage - to be explained later.

4. Analog Section

a. Azimuth is converted to sine and cosine functions in digital section (to be explained later).

b. Binary Decoders - convert digital information to a proportionate analog voltage.
125 V Reference out

c. Buffer - impedance match and voltage reducer.
"D" V Ref out - ± 25 V signal

d. Sine, cosine approximators - modify straight line functions to curves more closely representing the sine-cosine functions.

e. Multiplier - multiplication of sine or cosine and range.

f. Distribution power amplifier - power X and Y signal to be distributed to consoles.

5. Display Section

a. The voltage levels generated by the analog section are applied to the display section. This section contains the CRT tubes, one in each console, used to present LRI target information in PPI form. The translation of this target information into analog voltage levels will be explained later. These voltages (actually current) levels cause deflection yokes in all four consoles, if they are in the correct status (active or standby), to be energized, positioning the beam in accordance with the original target range and azimuth information. The beam is then unblanked at the consoles at which, or for which, the message display was requested, causing an appropriate target indication.

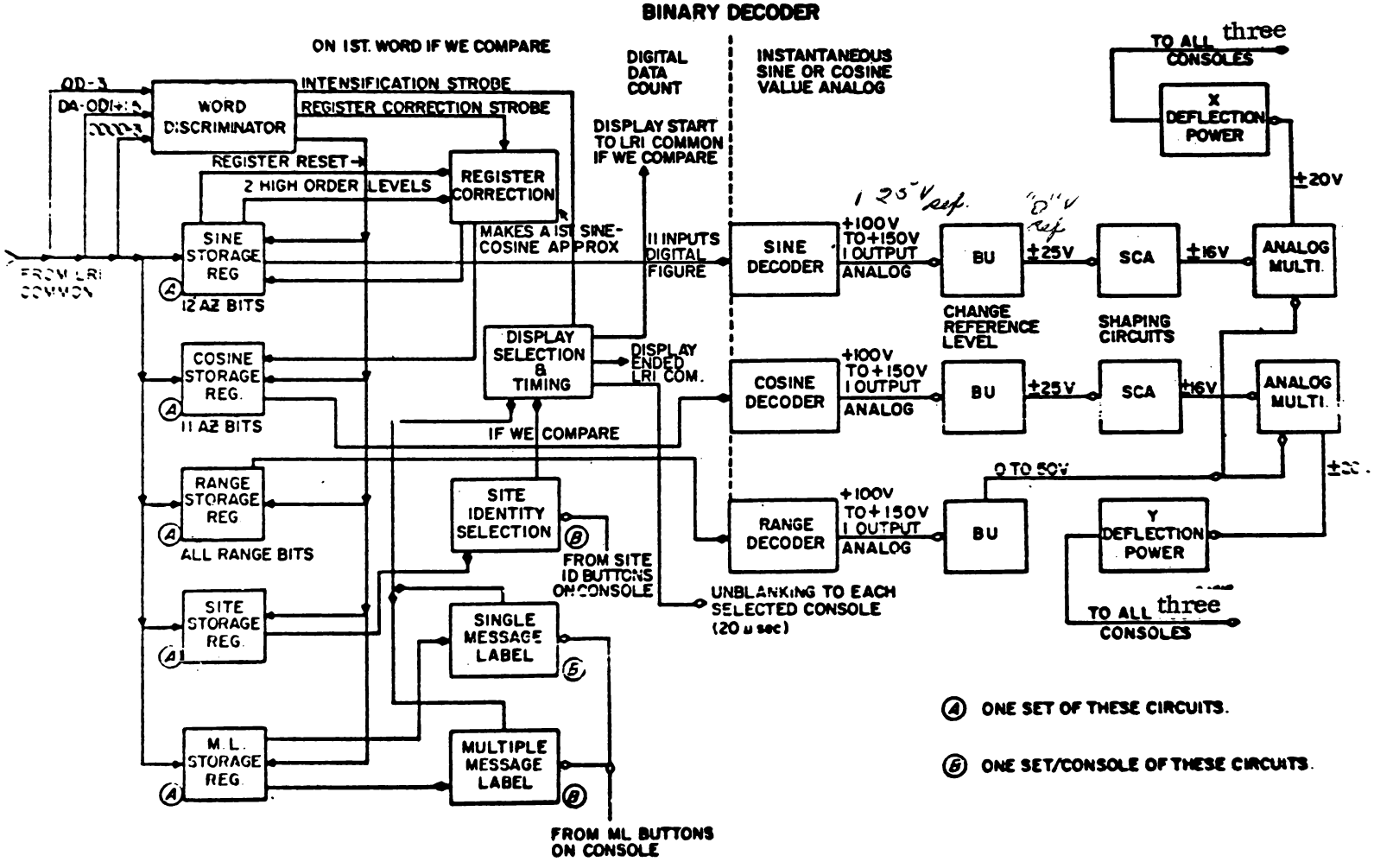
6. Switching Section

a. The switching section is distributed between the console and Unit 953. It contains the controls, relays, and associated circuitry required to perform the following functions:

1) Determine the operational status (active, standby) of each console.

2) Specify the site identity and message label designations of messages to be displayed at the consoles.

3) Determine the simplex (C or D) power supply used.


BINARY DECODER
ON 1ST. WORD IF WE COMPARE
DIGITAL DATA COUNT
INSTANTANEOUS SINE OR COSINE VALUE ANALOG
OD-3
DA-OD1-2
WORD DISCRIMINATOR
INTENSIFICATION STROBE
REGISTER CORRECTION STROBE
REGISTER RESET
2 HIGH ORDER LEVELS
REGISTER CORRECTION
DISPLAY START TO LRI COMMON IF WE COMPARE
MAKES A 1ST SINE-COSINE APPROX
11 INPUTS DIGITAL FIGURE
SINE STORAGE REG
12 AZ BITS
FROM LRI COMMON
COSINE STORAGE REG.
11 AZ BITS
DISPLAY SELECTION & TIMING
DISPLAY ENDED LRI COM.
IF WE COMPARE
RANGE STORAGE REG
ALL RANGE BITS
SITE IDENTITY SELECTION
FROM SITE ID BUTTONS ON CONSOLE
SITE STORAGE REG.
SINGLE MESSAGE LABEL
M.L. STORAGE REG.
MULTIPLE MESSAGE LABEL
FROM ML BUTTONS ON CONSOLE
UNBLANKING TO EACH SELECTED CONSOLE (20 μ sec)
SINE DECODER
COSINE DECODER
RANGE DECODER
+100V TO +150V I OUTPUT ANALOG
1.25 V ref.
"0" V Ref
BU
CHANGE REFERENCE LEVEL
±25V
SCA
SHAPING CIRCUITS
±16V
ANALOG MULTI.
0 TO 50V
TO ALL three CONSOLES
X DEFLECTION POWER
Y DEFLECTION POWER
±20V
Ⓐ ONE SET OF THESE CIRCUITS.
Ⓑ ONE SET/CONSOLE OF THESE CIRCUITS.

C. Timing Control of LRI Monitor

1. Word Discriminator

a. The word discriminator is the basic control circuit of the LRI Monitor, synchronizing its action with the LRI element by triggering, strobing, and resetting other circuits in the equipment at the proper time. Logic operation is discussed below.

b. Simplified circuit and timing chart is located on Page 1370.

c. Input Pulses

1) Drum Demand (OD3) - indicates 1st word of 2 may be received at next OD1-D.

2) Data Available (OD1-D) - indicates a word has been received from LRI common.

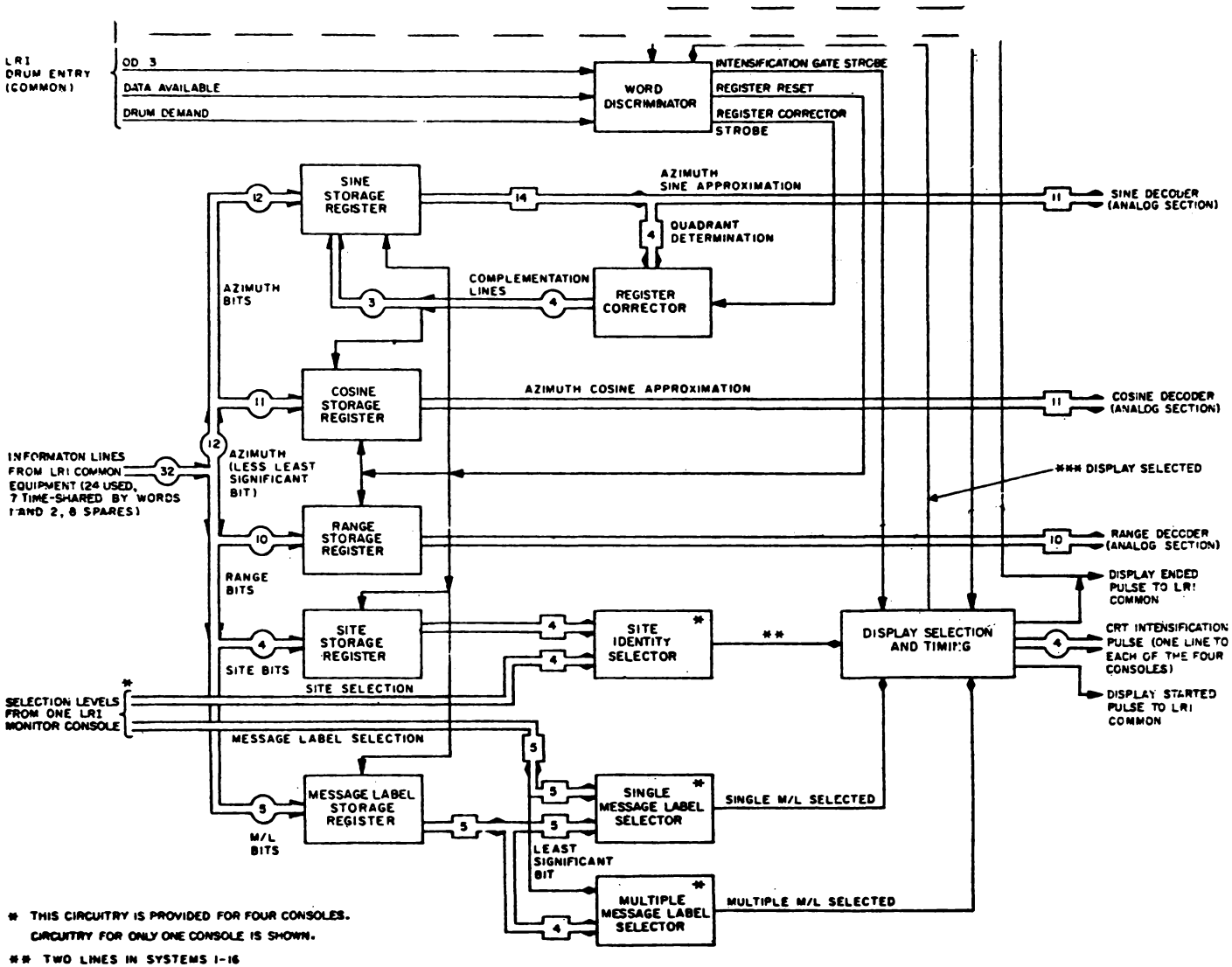
3) OD3 timing pulse.

4) Display Ended - indicates a message was just displayed.

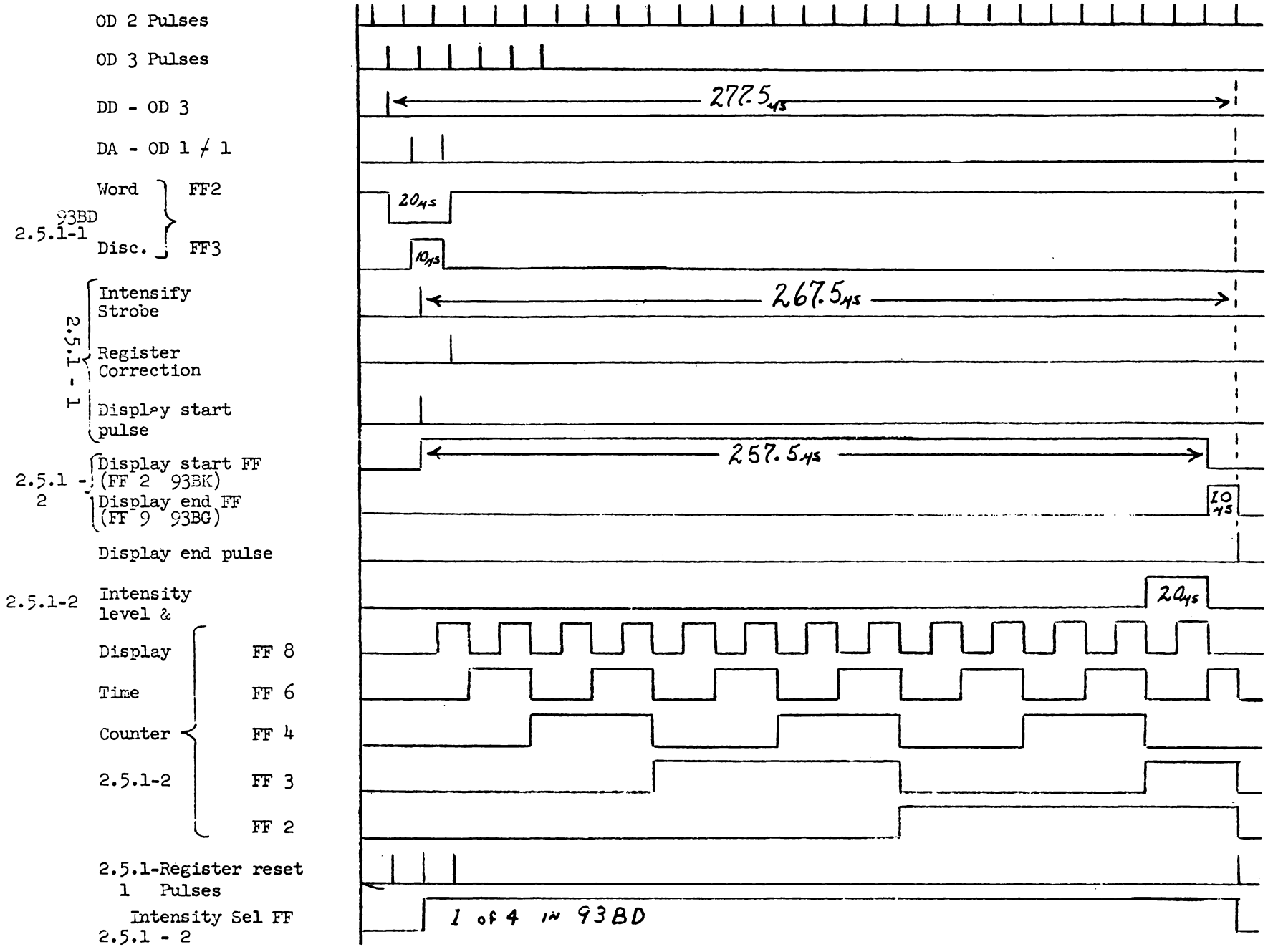
d. Output Pulses

1) Clear pulses to all storage registers (Register Reset) and generated by:

a) Drum Demand
b) 4 usec. after Data Available (OD3).



.LRI Monitor Digital Section, Overall Section Diagram


OD 2 Pulses
OD 3 Pulses
DD - OD 3
277.5 μs
DA - OD 1 ≠ 1
Word
FF2
93BD
2.5.1-1
Disc.
FF3
20 μs
10 μs
Intensify Strobe
Register Correction
Display start pulse
2.5.1 - 1
267.5 μs
Display start FF (FF 2 93BK)
2.5.1 - 2
Display end FF (FF 9 93BG)
257.5 μs
10 μs
Display end pulse
20 μs
2.5.1-2
Intensity level &
Display
FF 8
Time
FF 6
Counter
FF 4
2.5.1-2
FF 3
FF 2
2.5.1-Register reset
1 Pulses
Intensity Sel FF
2.5.1 - 2
1 of 4 in 93BD

c) Display ended.

2) Intensification Gate Strobe Pulse

a) Checks 4 comparison circuits to see if message is to be displayed on any of the 4 consoles.

b) Occurs 4. 0 usec after message label and site identity are stored.

3) Register Correction Strobe Pulse

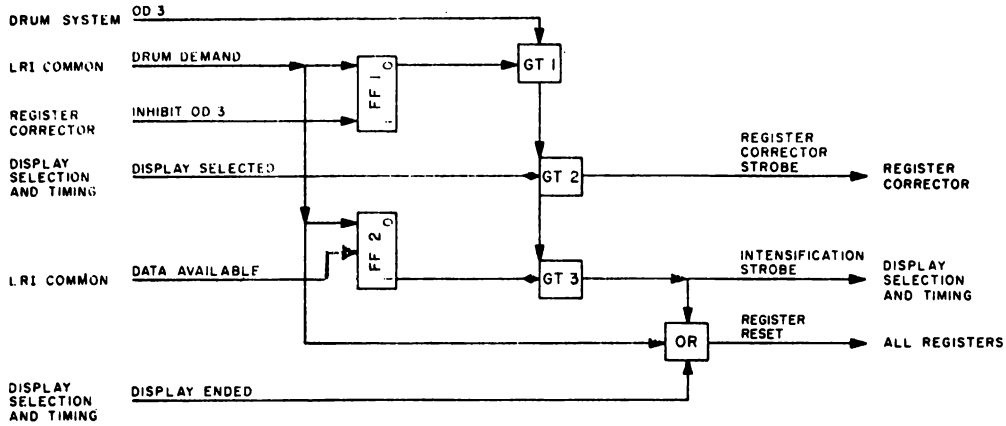
a) Modifies azimuth in sine and cosine storage registers.

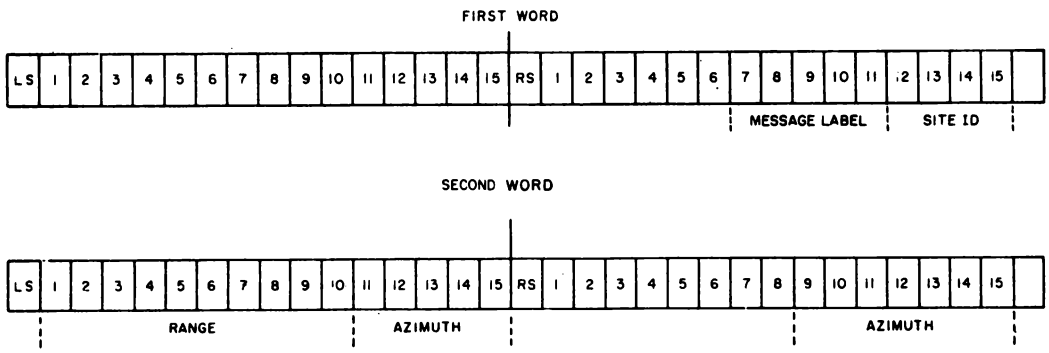
b) Occurs 4. 0 usec after range and azimuth are stored.

c) Modification is controlled by "register correction" circuitry.

e. Operation

1) In systems 17 and beyond the drum demand pulse (0time) clears FF 1 and FF 2. At six usec, the data available pulse accompanying the read-in of drum word 1 complements FF2 conditioning GT 3. At ten usec, an OD 3 pulse passes GT 1 and GT 3 (GT 2 is deconditioned). The output of GT 3 is sent to the display section and timing circuit. If a selection has been made, a display-selected level is returned to condition GT 2. (Concurrently, DD pulses are inhibited in the LRI element). At 16 usec, the data available pulse accompanying read-in of word 2 complement-clears FF 2, deconditioning GT 3. At 20 usec, an OD 3 pulse passes GT 2 as a register corrector strobe. The register corrector circuit returns the pulse without delay as an inhibit OD 3 pulse which sets FF 1. Flip-flop 1 remains set during the remainder of the





Composition of LRI Message to LRI Monitor

display cycle, blocking OD 3 pulse, and the circuit is therefore inactive until the next DD pulse initiates a new cycle.

2) If a selection is not made, GT 2 is not conditioned; the register corrector strobe is not developed; FF 1 is not set. The OD 3 pulse concurrent with the next DD pulse passes GT 1, but with no effect, since GT 2 and GT 3 are deconditioned. The circuit is in the proper condition for the display cycle initiated by the DD pulse.

3) For better understanding of operation, review operation on Logic 2. 5. 1-1 with timing chart on Page 1350.

2. Multi-Plexing of LRI

a. Explanation of LRI Monitor Multiplexed Operation

Multiplexed GFI operation requires three comparison checks prior to a display.

The LRI site ID and the message label are both compared in the first drum word. Assuming the GFI display is requested the LRI site ID and the gap filler message label will be compared. If they compare a display will be initiated.

Drum word two will then be checked for a comparison of the GFI site ID. This occurs after a display has already begun.

The GFI site ID decoders provide a complement compare between the levels inserted from the switches on the monitor consoles and the GFI site identity bits in drum word two. A +10 volt output from any of the four decoders is a "no compare" level for the console associated with that decoder. This output then conditions the capacitor diode gate to clear the intensification flip-flop for that console, thereby preventing a GFI display on any console other than the one requesting the display.

If a no compare level is received from all four of the decoders a wrong gap filler level is generated. This level prevents a LRI monitor clock alarm from being generated, in unit 41 when the display cycle is prematurely ended as a result of the GFI no compare.

b. Explanation of Test Switch Operation

Old LRI monitor consoles had separate pushbuttons for the operational and test messages, for example: switch 14 was "search ops" this displayed ML 00011 messages. The only difference between the ops and test ML's is that bit 2 is a "1" for "TEST" and a "0" for "OPS".

The new LRI monitor system provides only one PB for each type of message and a test switch to permit selection of test ML's. EXAMPLE: Depressing PB 14 (search) permits display of ML 00001, if the test switch is placed in the test position at the same time, ML 00011 will be displayed. Thus selecting any PB and placing the test switch in "TEST" allows the display of the corresponding test ML. If the test switch is not in the "TEST" position the OPS ML will be displayed.

3. Message Select Circuits

a. Introduction

1) By means of pushbutton keyboards at the LRI monitor consoles, or at Unit 953 personnel specify the site identity and message labels of the messages they wish to have displayed. The pushbutton-activated circuits supply sets of voltage levels to the site identity selector and message label selector circuits. There is one site identity selector, one single message label selector, and one multiple message label for each console.

2) The site identity bits in the first word of the message are accepted by the 4-FF site identity storage register which supplies a corresponding set of voltage levels to all the site identity selectors. Similarly, the five message label bits are accepted by the 5-FF message label storage register, which supplies a corresponding set of voltage levels to all the single-message label select ors and multiple-message label selectors. In the selectors, comparisons are made between the levels supplied by the console keyboards circuitry and by the storage registers. If, on the basis of this comparison, a message is selected for display at one or more consoles, the display selection and timing circuit is activated. This circuit provides a display-started pulse to the LRI common equipment, receipt of which prevents further transfer to LRI messages to the Drum System.

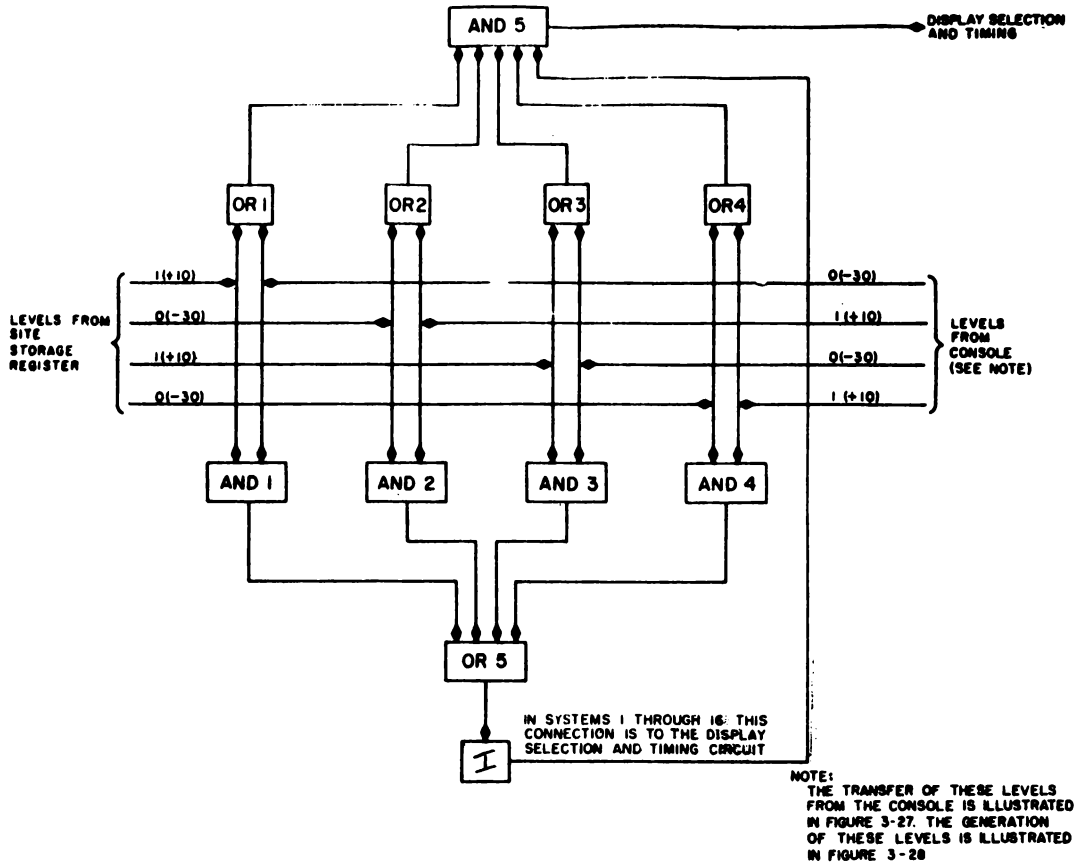
b. Site Identity and Message Storage Registers

a) A set of registers for each display console.

b) Message can be accepted by any console which selects correct SID and message label.

c. Site Identity Selector

1) There are four site identity selector registers; one for each display console. Each selector compares the level applied to the site identity storage register with site identity selection levels supplied by a particular console (or keyboard on Unit 953). The selection levels from the consoles are produced by pushbutton-activated circuits in the consoles. Depressing a site-selection pushbutton generates a unique set of four levels or bits, as indicated in table 3-1 on Page 1410. When these levels complement the levels supplied by the site storage register, the site identity selector indicates selection to the display selection and timing circuit. Circuit operation of the site identity selector is explained on Page 1430.



Site Identity Selector, Simplified Logic Diagram

TABLE 3–1. SITE SELECTION

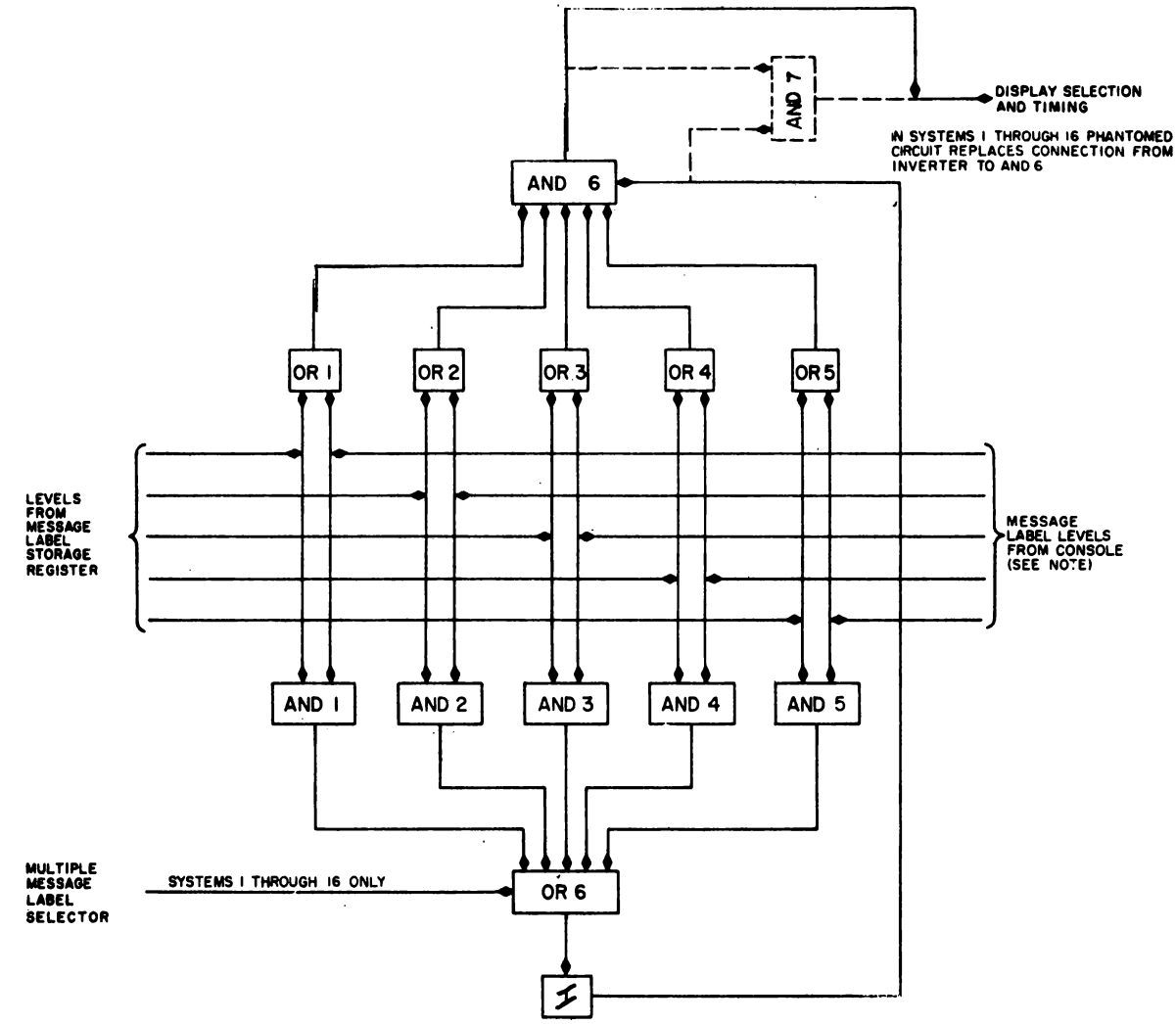
PUSHBUTTON DEPRESSED	CONSOLE OUTPUT BIT POSITION 4	3	2	1
0	1	1	1	1
1	1	1	1	0
2	1	1	0	1
3	1	1	0	0
4	1	0	1	1
5	1	0	1	0
6	1	0	0	1
7	1	0	0	0
8	0	1	1	1
9	0	1	1	0
10	0	1	0	1
11	0	1	0	0
12	0	0	1	1
13	0	0	1	0
14	0	0	0	1

Note: ONE = +10V level
ZERO = −30V level

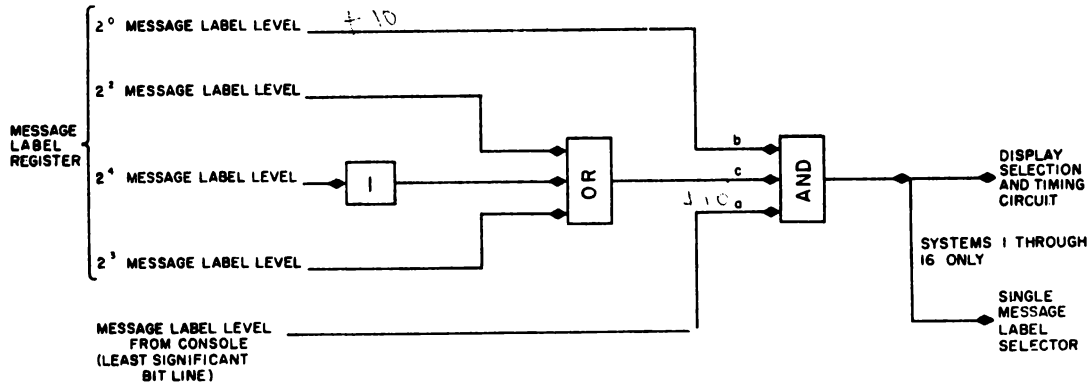
TABLE 3–2. MESSAGE LABEL SELECTION

PUSHBUTTON DEPRESSED	CONSOLE OUTPUT BIT POSITIONS 5	4	3	2	1
0	0	0	0	0	1
1	0	1	0	0	0
2	0	1	0	1	0
3	0	0	1	0	0
4	0	0	1	1	0
5	0	0	0	0	0
6	0	0	0	1	0
7	1	0	0	0	0
8	1	1	0	0	0
9	1	0	1	0	0
10	0	1	1	0	0
11	1	0	0	1	0
12	1	1	0	1	0
13	1	0	1	1	0
14	1	1	1	1	0

Note: ONE = +10V level
ZERO = −30V level



Single-Message Label Selector, Simplified Logic Diagram



Multiple-Message Label Selector, Simplified Logic Diagram

d. Site Identity Selector Operation

1) Assume that (as shown on Page 1410) the levels from the site storage register are represented by the binary word 1010. To achieve selection, levels equivalent to 0101 must be supplied by the console. The following conditions are then found; a positive input is applied to OR 1 and OR 3 by the site storage register and to OR 2 and OR 4 by the console keyboard. Consequently, four inputs to AND 5 are up. There is only one positive input to AND 1, AND 2, AND 3, and AND 4. Therefore, the outputs of those AND's are down and there is no output from OR 5; and consequently, there is an output from the INVERTER circuit. The output of the inverter supplies the fifth input required to produce an output from AND 5.

2) Inspection of the logic shows that if the inputs from the site storage register and the console are not complementary, there will be no output from the site identity selector circuit. That is, the output or OR1, OR2, OR3, OR4 will be down or the output of AND, AND 2, AND 3, or AND 4 will be up, or both conditions will prevail.

e. Single Message Label Selector

1) One single message label selector (Page 1420) is associated with each console. The logic of the circuit is very similar to that of the site identity selectors The main difference is that five levels are applied to each selector circuit by the message label storage register and by the message label pushbutton circuit of the consoles (Table 3-2, Page 1410). When the levels from these two sources complement each other, the outputs for OR 1 through OR 5 are up, supplying five of the six possible inputs to AND 6. The outputs of AND 1 through AND 5 are down. Therefore, there is no input to the INVERTER and its output is positive, supplying

the sixth input required to bring up the output of AND 6; that is, selection is indicated.

f. Multiple Message Selector

1) Enable the display of all messages from selected sites, except for messages with message labels 17 and 19 in binary (10001 and 10011). These messages label designate height-finder messages which the LRI monitor is not equipped to display. One multiple message label selector is associated with each console. All function identically. The logic operates as follows: An output from the multiple message label selector is available when the AND is up. To produce this condition, inputs to the AND must be supplied by: (Page 1420).

   a) The least significant bit message label selection line from the console.

   b) The set side of FF 2^0 in the message label register.

   c) The OR.

2) Input a is provided by depressing the 0 (multiple message label selection) pushbutton at the console. Levels representing 00001 are then supplied by the console, as indicated in table 3-2. Note that this is the only pushbutton selection which provides a "1" on the least significant bit line.

3) All message labels actually in use provide input b, since only odd number message labels are used and all odd numbers, in binary, have a 1 in the 2^0 position flip-flop.

4) All message labels except 10001 and 10011 (17 and 19 in binary) will provide input c; both of these numbers present two 0's directly to the OR and a 1 to the INVERTER, which thus prevents a third 0 to the OR.

5) In other words, the multiple-message label selector provides an output for all message labels in actual use, except binary 17 and 19, when the multiple message label selection is specified at the console.

g. Logic Analysis of Message Select Circuitry

1) Intensification Strobe from 93BCE7 (2. 5. 1-1).

2) Strobes four sets of site identify and message label gates(2. 5. 1-2).

3) If any set of gates passes a pulse, will set display start FF (cFF2, 93BK), and any amount of intensification select FF's (93BD).

4. Register Correction Circuit

a. Purpose

1) The position of an LRI target is described by digital information in the LRI message. This information is in polar co-ordinate form, specifying the azimuth and range of the target. However, the display circuitry of the LRI monitor positions a target by means of its cartesian coordinates; that is, with respect to the X and Y axis of the display screen. Figure 1, Page 1580 compares the two methods of target location. Accordingly, the LRI monitor must develop, from the original polar information, two voltage (actually current) levels representing the X-Y co-ordinates of the target to drive the horizontal (X) and vertical (Y) deflection coils of the CRT.

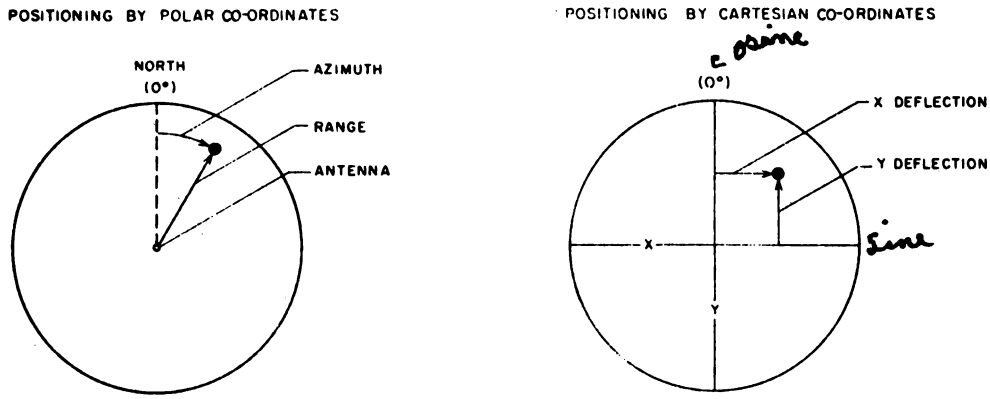


Figure *Target Positioning by Polar and Cartesian Co-ordinates*

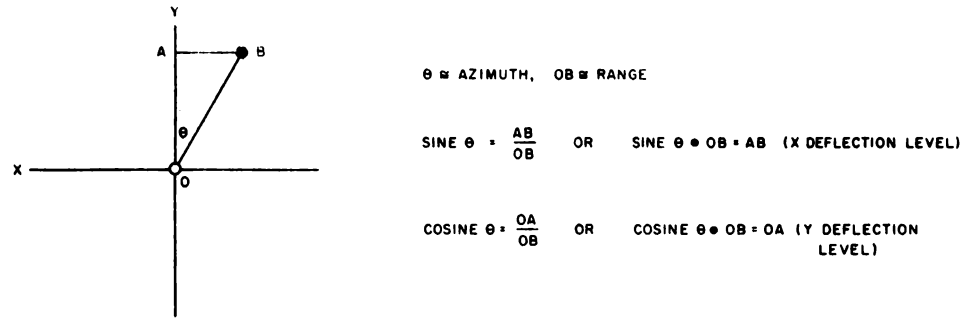


Figure *Mathematical Basis for Development of Deflection Levels*

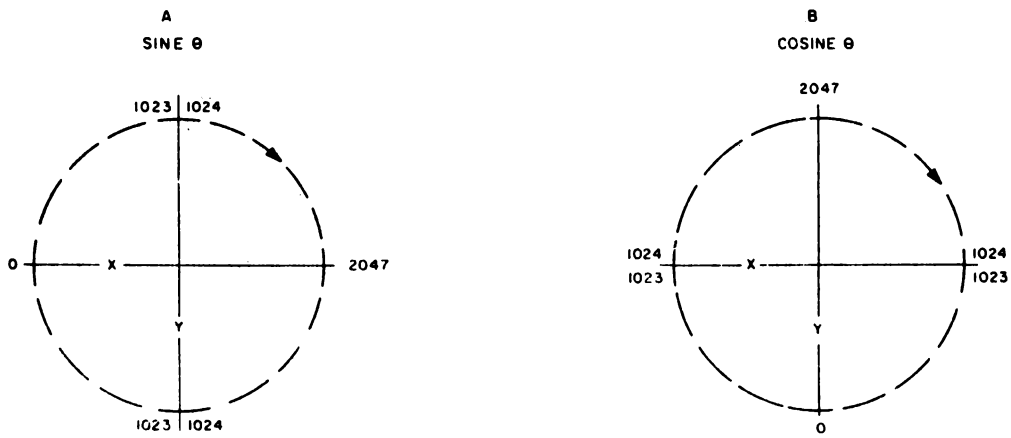


Figure *Digital Equivalents of Approximations of Sine θ and Cosine θ*

2) One approach to this problem is suggested by Figure 2, Page 1460. Here $\emptyset$ represents the known azimuth, and OB the known range; the problem is to find AB (X deflection) and OA (Y deflection).

By definition $\text{Sine } \emptyset = \frac{AB}{OB}$

Therefore, $AB = (\text{Sine } \emptyset)\ OB$

Since OB is known, the problem may be solved by finding sine $\emptyset$ and multiplying it by OB.

Also, $\text{Cosine } \emptyset = \frac{OA}{OB}$ or $OA = (\text{Cosine } \emptyset)\ OB$

OA is found by finding Cosine $\emptyset$ and multiplying it and OB.

3) This approach in electronic form is used in the LRI monitor.

   a) The sine and cosine value are approximated by the register correction circuits.

   b) Later the analog section will change the approximation to a true value of a point on a sine wave.

   c) Note Figure 3, Page 1460, the sine and cosine, if plotted on a straight line, would be a sine wave.

4) Theory of Sine and Cosine Approximation

   a) LRI message is expressed on a 0-4095 binary scale representing 360^{o}.

b) Sine or cosine will go from 0-1 in 90°, therefore, a linear scale for 360° would have four complete changes of sine or cosine value.

c) The four complete changes of sine or cosine is represented as a 0-2047 binary count.

d) Note sine and cosine approximation tables on Page 1500.

e) The graph shows how a 0-4095 binary value is changed to a 0-2047 value for sine and cosine.

f) Note that sine and cosine are 90° out of phase.

g) Examples of correction (in octal)

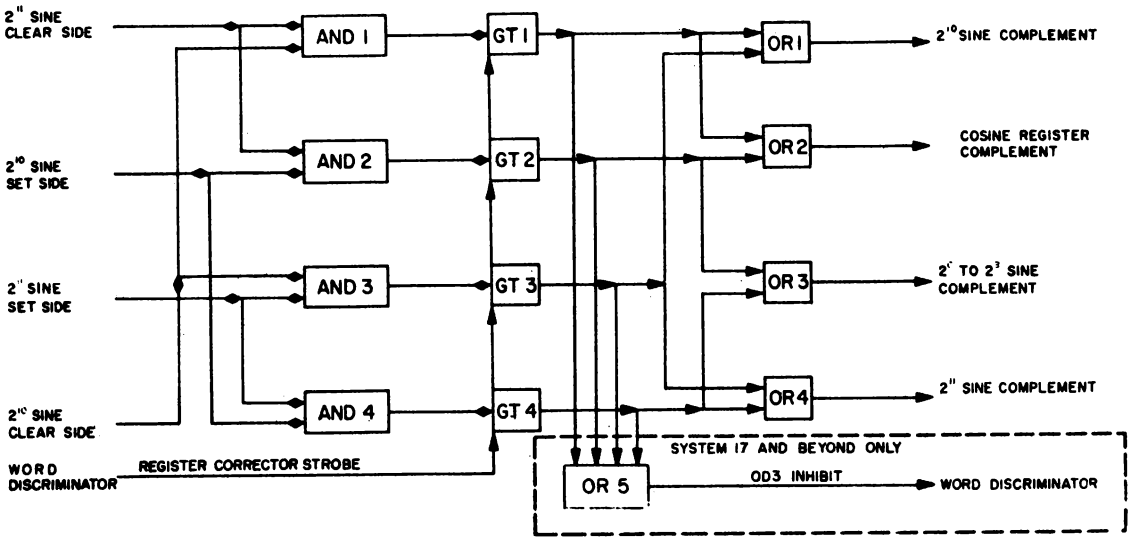
Decimal Equivalent	Azimuth	Sine	Cosine
0000	0000	2000	3777
0512	1000	3000	2777
1024	2000	3777	1777
1536	3000	2777	0777
2048	4000	1777	0000
2560	5000	0777	1000
3072	6000	0000	2000
3584	7000	1000	3000
4095	7777	1777	3777

b. Operation Logic 2.5.1-1

1) Complementation of the sine and cosine storage registers to produce first sine and cosine approximations is accomplished as follows. The FF 2^{10} and FF 2^{11} (R9 and R10) in the sine storage register supply four levels, two from the set side of the flip-flops and two from the clear side, to AND's 1, 2, 3 and 4 in the register corrector Page 1500). At 16 usec of the timing

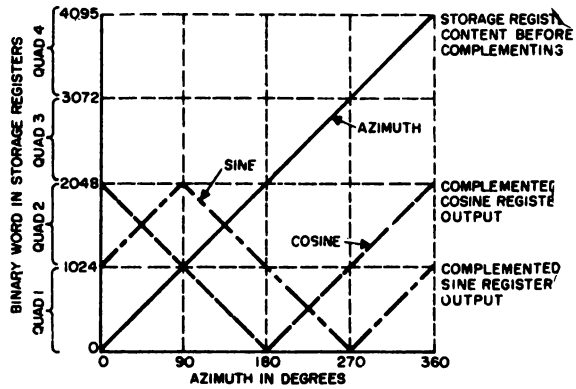
cycle, azimuth information is installed in the sine storage register and these levels become significant. The combination of possible levels represent the four possible quadrants in which the target may appear. The first quadrant, 0 to 90 degrees, is represented by azimuth, values between 0 and 1,023; therefore, FF 2^{10} and FF 2^{11} are clear, bringing up the output of AND 1. The second quadrant, 90 to 180 degrees, is represented by azimuth values between 1,024 and 2,047; therefore, FF 2^{10} is set, FF 2^{11} is clear, and the output of AND 2 is up. The third quadrant, 180 to 270 degrees, is represented by azimuth values between 2,048 and 3,071; therefore, FF 2^{10} is clear and FF 2^{11} is set, supplying the two necessary inputs to bring up AND 3. The fourth quadrant, 270 to 360 degrees, is represented by azimuth values between 3,072 and 4,095; therefore, FF 2^{10} and FF 2^{11} are set, and the AND 4 output is up. Only one AND can produce an output at any given time. The output from each AND goes to a gate having a corresponding designation (AND 1 to GT 1, etc). Four usec after the AND output is brought up, the register corrector strobe from the word discriminator strobes all four gates. (Note timing charts on Pages 1480 and 1500.) An output from GT 1 goes to OR 1 and OR 2, causing FF 2^{10} of the sine storage register and the entire cosine storage register to be complemented. An output from GT 2 goes to OR 2 and OR 3, causing FF 2^{0} through FF 2^{9} of the sine storage register and the entire cosine storage register to be complemented. An output from GT-3 goes to OR-3 causing FFs-2^{0} through 2^{9} of the sine storage register to be complemented; none of the cosine storage register FFs are complemented.

GT-4 output goes to OR-1 complementing 2^{10} FF of the sine storage register; none of the cosine storage register FFs are complemented.



SINE APPROXIMATION		
AZIMUTH (degrees)	**SINE VALUE**	**BINARY EQUIVALENT**
0	0	1023
90	+1	2047
180	0	1023
270	−1	0

COSINE APPROXIMATION		
AZIMUTH (degrees)	**COSINE VALUE**	**BINARY EQUIVALENT**
0	+1	2047
90	0	1023
180	−1	0
270	0	1023



EFFECTS OF SINE AND COSINE REGISTER COMPLEMENTING

2) The effects of complementation upon the sine and cosine storage registers are illustrated on Page 1500. Note that the chart on Page 1510 indicates the effects of complementation on the entire range of possible inputs to the sine and cosine storage registers (as if the registers were stepped like counters). Each input, of itself, produces a single output level.

3) Note: Only 11 digits are needed to express the contents of the sine register after complementation because the highest possible number in the register is then 2047, binary.

4) Note the register correction circuitry in pluggable units 93BH and 93BJ (Logic 2.5.1-1).

5) Note input level lines from bits R9 and R10.

6) Note correction pulses.

D. Display Selection and Timing Circuit

Note:- Although the Display Selection and Register-Correction circuitry has already been covered, it will be discussed again and should serve as a good review of the digital section timing. Refer to the timing chart on page 1350 and the simplified logic on page 1530 for circuit analysis.

1. Purpose

a. The display selection and timing circuit (page 1530) determines which selection has been made, and, if it has been made, performs the following functions:

1) Sends a display-started pulse to the LRI com-com, which causes inhibition of further DD pulses, and sends a display-selected level to the word discriminator.

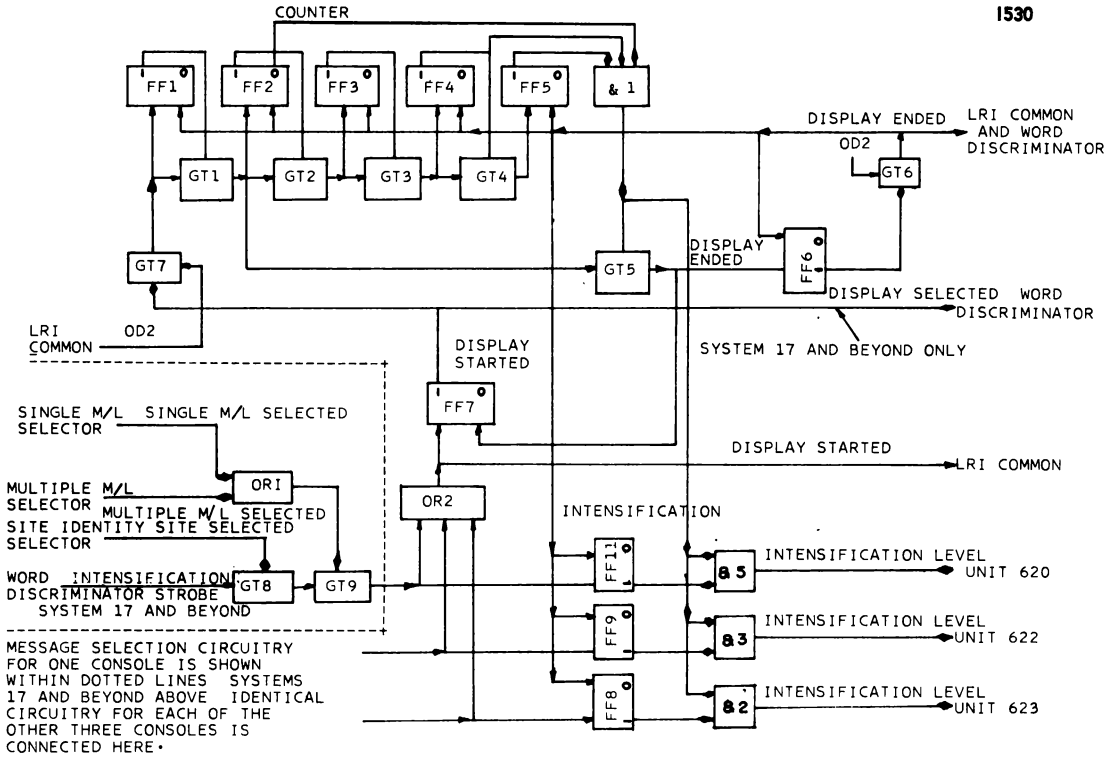
2) Performs a counting action during which the analog current levels achieve stability in the CRT deflection coils.

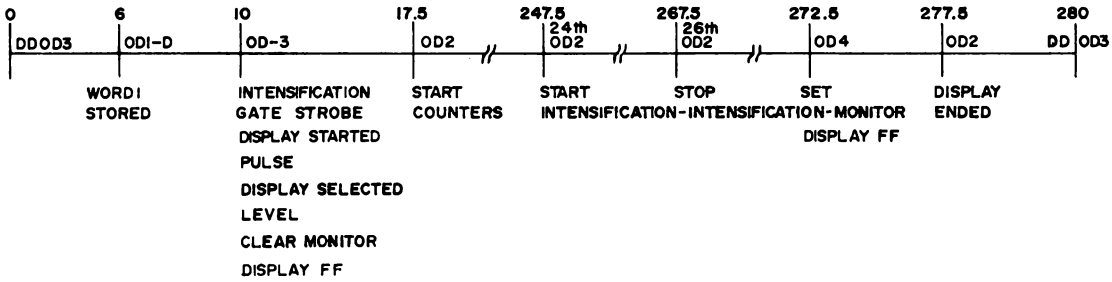
3) At the end of the count, sends a 20-usec intensification level to the console for which the display was requested; this level unblanks the CRT at that console, permitting a target indication.

4) Following a target presentation, sends a display-ended pulse to the LRI common, conforming the fact that display has ended, and to the word discriminator, causing the registers to be reset.

2. Operation (Simplified Logic)

a. OR 1, GT 8 and GT 9 determine whether message selection has been achieved for a particular console (example - designated unit =620). If either the single message selector or the multiple message selector for that console provides an input to OR 1, GT 9 is conditioned. If the corresponding site selector provides an output concurrently, GT 8 is conditioned. The intensification gate strobe from the word discriminator then passes GT 8 and GT 9 at 10 usec, setting FF 11. (Had another console selected the message for display, the flip-flop associated with that console, whether FF8, FF9, or FF 10, would have been set). The output of GT 8 is also fed through OR 2 to the LRI common as the display - started pulse; in addition, it sets FF 7, conditioning GT 7 and providing a display-selected level to the word discriminator. The OD 2 pulse, at 17.5 usec passes GT 7, initiating action of the conventional 5-bit counter, composed of FF 1 through FF 5 and GT 1 through GT 4. Succeeding OD 2 pulses step the counter. When the count reaches 24 (247.5 usec), the output of AND is up (FF4 and FF 5 set, FF 2 clear), conditioning GT 5 and supplying an input to AND 2, AND 3, AND 4, and AND 5. Since FF 11 was set at 10 usec, there is an output from AND 5 and an intensification level is supplied to, in this case, unit 620. (Had FF8, FF9, or FF 10 been set, the intensification level would have been sent to the associated console). The 25th OD 2 pulse sets FF 1, conditioning GT 1. The 26 OD 2 pulse passes GT 1 and GT 5, setting FF 6 (the effect of which is described below) and clears FF7. The clearing of FF 7 deconditions GT 7 and stops the action of the counter at 26. This count finds FF 2 set; therefore, AND 1 no longer provides an output discontinuing the intensification level at the console.





LRI MONITOR TIMING DIAGRAM

b. When set, FF 6 conditions GT 6. The 27th OD 2 pulse (at 277.5 usec) strobes GT 6. The output of GT 6 is the display-ended pulse; it is sent to the LRI common, and to the word discriminator; it also resets the counter, flip-flops FF6 and FF 8 through FF 11. The display cycle is concluded, beginning again with the next DD pulse (280 usec).

3. Operation (Logic 2.5.1-2)

a. Reviewed operation with logic and timing chart.

1) cFF2, 93BK = Display Start FF.

2) cFF9, 93BG = Display End FF.

3) cFF4, 6, 8, 9 (93BD) = Intensification Select FF.

E. Summary Questions

1. An LRI Mark X Message:

(a) is never displayed by the LRI Monitor
(b) is displayed by LRI Monitor only on request by Central Computer.
(c) is not written on the LOG Drum if it is to be displayed.
(d) is written on the drum and displayed by the LRI Monitor simultaneously.
(e) is displayed prior to being written on the LOG Drum.

2. An LRI Height Finder message:

(a) is never displayed by the LRI Monitor.
(b) is displayed by the LRI Monitor only on request by Central Computer.
(c) is displayed only by an LRI Monitor with an address selection button.
(d) is written on the LOG Drum 10 microseconds prior to being displayed by the LRI Monitor.
(e) is written on the LOG Drum and displayed by the LRI Monitor simultaneously.

3. Which of the following parts of an LRI FGD message do not go to the LRI Monitor?

   (a) Run length
   (b) Time delay
   (c) Message Label
   (d) Range
   (e) Azimuth
   (f) Site identity
   (g) Clock time

4. Unit 93A Consists of: (System 17 and beyond)

   (a) 2 digital modules, 1 analog module, and 1 power module.
   (b) 1 digital module, 2 analog modules, and 1 power module.
   (c) 2 digital modules, 2 analog modules, and 1 power module.
   (d) 1 digital module, 1 analog module, and 1 power module.
   (e) None of the above.

5. Unit 93B can control as many as_____LRI Monitor Consoles.

6. (Logic S 2.4.5) What is the time elapse from the time the Monitor Display FF is cleared until it is set?

7. (True or False) The Sine and Cosine must both be multiplied by the Range in the Digital Section in order to properly position the target on the face of the CRT.

8. (Logic S 2.4.5) What does the LRI Monitor Display Counter equal (octal number) when the intensification of the target displayed is stopped?

   (a) 17_8
   (b) 25_8
   (c) 27_8
   (d) 30_8
   (e) 31_8

9. (Logic S. 2.4.5) 41V(AA)B4 (8B) opens. An LRI mark X message is being displayed. Which of the following best describes the result of this malfunction:

VII. LRI Monitor, Analog and Console Section

A. Introduction to Analog Section

1. The analog section decodes digital information from the sine, cosine, and range storage registers in the digital section and converts it into two analog voltages which correspond to the X and Y co-ordinates of a target indication on a CRT screen. These voltages are supplied to the four display consoles in a form capable of driving the CRT deflection amplifiers. The corrected inputs from the digital section, representing each target, are sustained for 247.5 usec to allow analog and display circuitry to achieve stability.

2. As shown on Logic 2.5.1-1 analog circuitry is divided into five sections comprising 12 units: binary decoders (3 units); sine and cosine approximators (2 units); multipliers (2 units); and distribution power amplifiers (2 units). All of these are special circuits, and will be discussed in the following sections. A test panel associated with the analog section will also be discussed.

   a. Binary Decoders

      The three binary decoders (PU's 93C-C-E-G) convert digital input information to corresponding analog voltages. The inputs to the sine and cosine binary decoders represent approximations of the sine and cosine functions, respectively, of the azimuth and, in each case, are supplied in an 11-bit binary code. Information to the third decoder represents target range and is supplied in a 10-bit binary code. The output from each decoder is an analog voltage between fixed limits, 100 and 150V, varying from those limits in proportion to the digital value of the inputs. Thus digital input 00000000000 $(0)_2$ produces an output of approximately 100V, and 11111111111 $(2047)_2$ produces an output of approximately 150V. Intermediate digital values are represented by corresponding intermediate voltages.

   b. Buffer Amplifiers

      The three buffer amplifiers (PU 93CJ) are employed to couple the binary decoder outputs to their respective loads. These loads are the sine and cosine approximators for the sine and cosine binary decoders, and, the multipliers for the range binary decoder. The buffer amplifiers shift down the voltage level of the binary decoder input (100 to 150V), providing a

(a) Under normal conditions would have no effect and would probably never be discovered except in test.
(b) Would prevent any LRI data reaching the "B" drum and selected LRI Monitors, after this message.
(c) Would cause next message to be displayed for 310 microseconds.
(d) This message would stop being displayed the moment this malfunction occurred and no further messages could be displayed.
(e) Monitor display would not be affected. Only effect would be no data to "B" drum.

10. How often are the Sine, Cosine, and Range Registers Reset if data is not being Received? How many times, per message, are these Registers Reset if data is displayed?

11. The Register Correction Strobe Pulse

(a) Occurs 1.5 microseconds after receipt of Drum Word #2.
(b) Resets Sine, Cosine and Range Registers after each displayed.
(c) Resets Sine and Cosine Registers if message received is not to be displayed.
(d) Does not affect the Range Storage Register.
(e) Will compliment either the Sine or Cosine Storage Register but never compliment both simultaneously.

12. The LRI Monitor CRT is "unblanked" for_____microseconds per LRI message.

13. In which Quadrant of the LRI Monitor display would targets be displayed with the following Azimuth values?

(a) 1,320
(b) 256
(c) 2,010
(d) 4,005
(e) 3,167
(f) 67
(g) 2,222
(h) 1,777

zero voltage reference level for this signal and also furnishing a proper impedance match with the binary decoder loads.

c. Sine and Cosine Approximators

The sine and cosine approximators (PU's 93C-U-V) are identical shaping networks which convert straight-line approximations of the azimuth sine and cosine functions to sinusoidal curves more closely representing these functions. These straightline approximations, in analog form, are supplied by the sine and cosine binary decoders (through the buffer amplifiers) and converted to sinusoidal curves by a proportionate decrease in gain as either limit of the input is approached.

Note

The terms "straight-line approximations" and "sinusoidal curves" describe the effects of the stage upon the entire range of inputs, not upon individual inputs. Each input, considered by itself, is a level.

d. Multipliers

Each multiplier (PU's 93CW-Y) receives the output from one of the sine-cosine approximators, and the output from the range buffer amplifier. The sine or cosine input to each unit is multiplied by the range input so that the output of the multipliers becomes R sine θ and R cosine θ, respectively, which correspond to the X and Y rectangular co-ordinates of the target. The mathematical basis of this process was discussed in Section VI. C.

e. Distribution Power Amplifiers

Distribution power amplifiers (PU's 93C-BB-CC) are special circuits which provide sufficient power to drive deflection amplifiers in each of the four display consoles. The amplifiers input impedance is high to match the multiplier outputs, and output impedance is low to match the capacitive loads presented by the connecting cables and CRT

deflection amplifiers. The distribution power amplifiers are identical. In the four consoles, one drives all the horizontal deflection amplifiers and the other all the vertical deflection amplifiers.

f. Power Supplies

To provide the high degree of accuracy and stability required in analog circuitry, the analog section employs special regulated voltages in addition to the service voltages used throughout the Combat Direction Central. The voltage supplies and their function are shown on Page 1670. All are special circuits.

B. Binary Decoder Operation

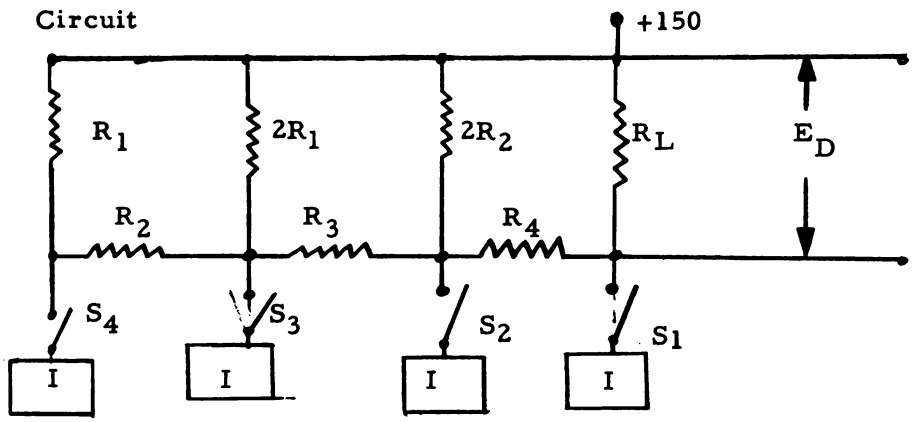
1. Function

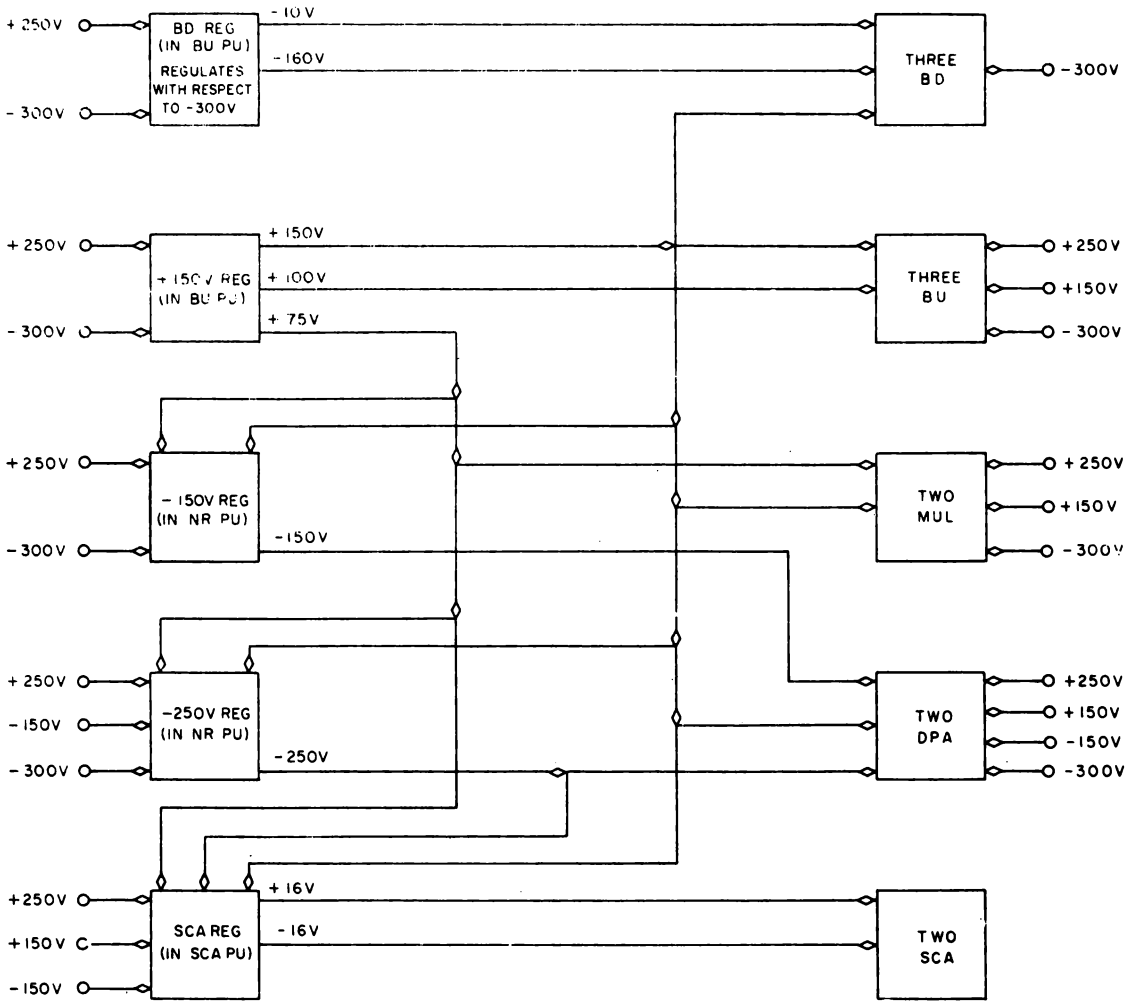
a. Convert binary counts to proportionate analog voltages.
b. A 10 stage decoder for range is used.
c. An 11 stage decoder for sine and cosine is used.
d. Each stage controlled by one bit of a register.
e. Each stage, when conducting, supplies a constant amount of current. However, due to the ladder resistors each stage feeds a different amount of current through the load.

(1) Hi order stage supplies X current to load.
(2) Next stage X/2 current to load.
(3) Next stage X/4 current to load.
(4) Etc.

2. Basic Decoder (4 stages) Operation

a. Circuit



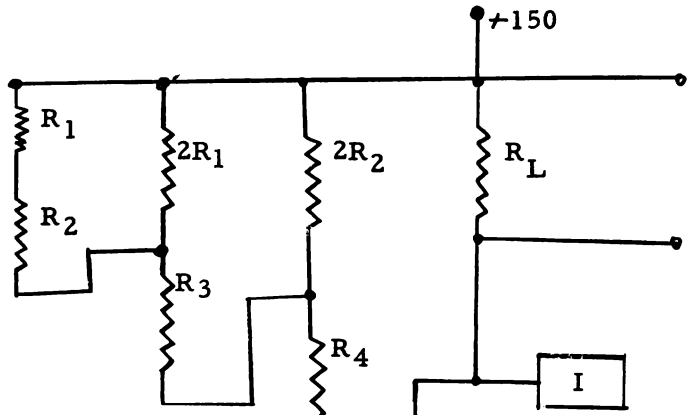


D-C Distribution and Voltage Regulation, Analog Section

b. $R_1 = R_2 \equiv R_3 = R_4$ 1 $\frac{2R1}{2} = \frac{2R2}{2}$

c. E_D in terms of IR from 1st stage.

(1) Equiv. ckt.

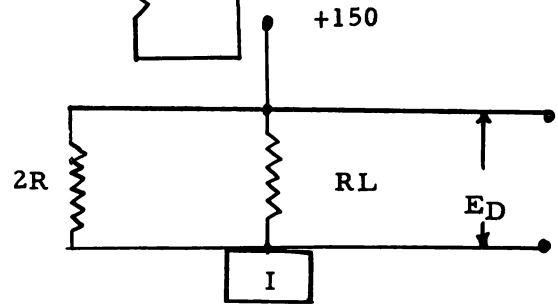


(2) Equiv. ckt.

(a) 1/3 I thru 2 R
(b) 2/3 I thru RL

(3) Ed = 2/3 IR

(4) Eo = +150 - Ed



d. Refer to Page and note similar equivalent circuits and Eo for each of other 9 stages singularly.

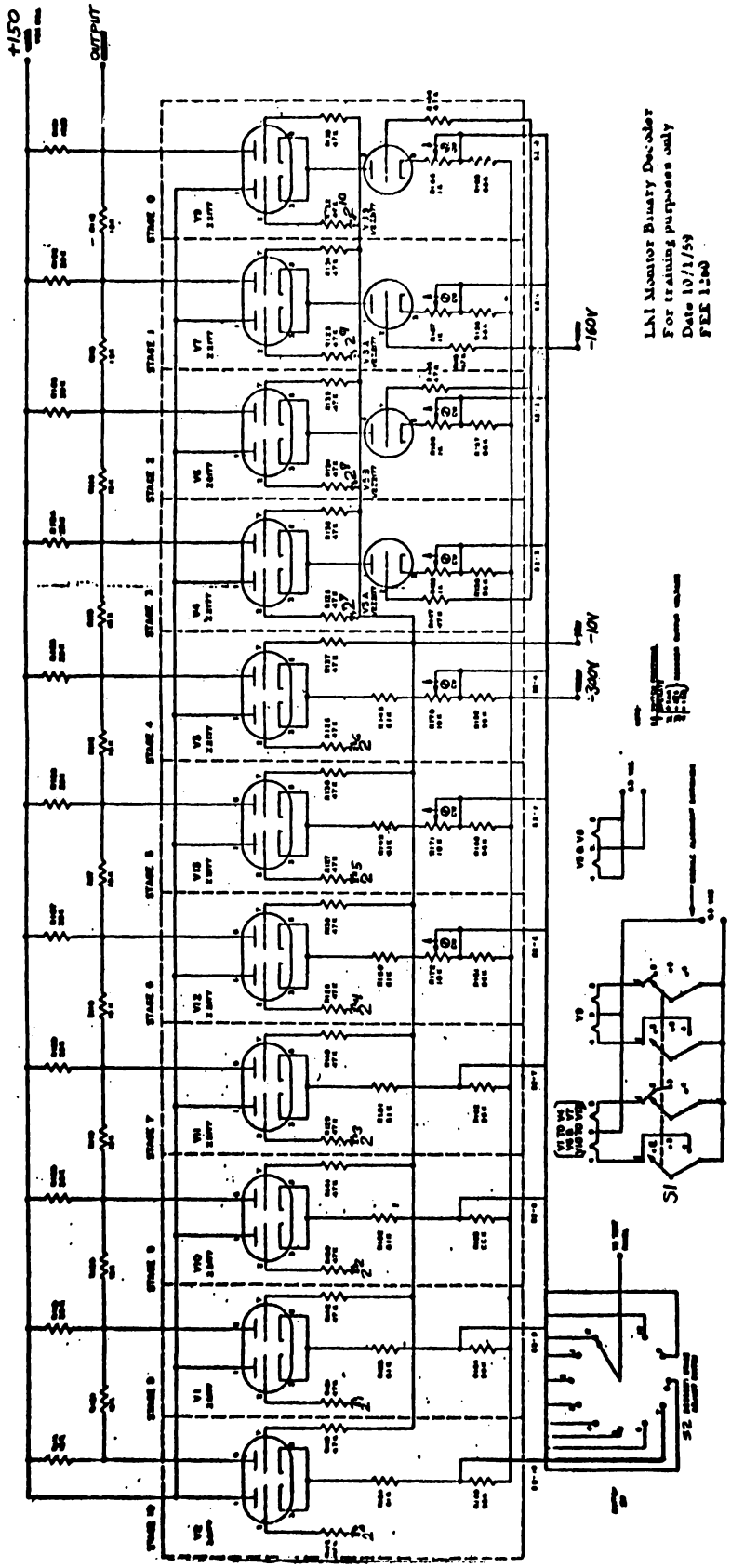
e. Two or more stages conducting at one time results in a sum of the individual voltages:

(1) 1st stage and 3rd stage Ed = 5/6 IR
(2) 2nd stage and 3rd stage Ed = 1/2 IR
(3) Proof can be had by use of Kirchoff's Law - but not essential for maintenance understanding.

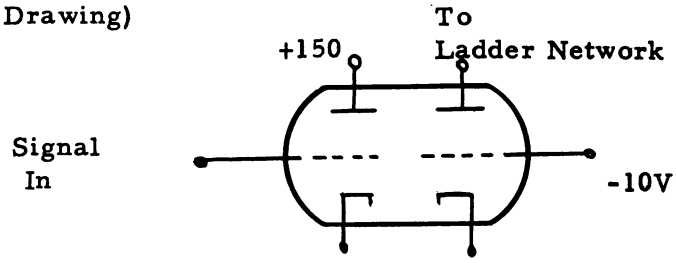
3. Decoders Utilized

a. Each in its own P. U.
b. Range decoder does not utilize low order stage.
c. Eo = 50 volt signal with ref to + 150V.

(1) 3777 = OV or + 150V (ref. ground)
(2) 0000 = 50V or +100V (ref. ground)

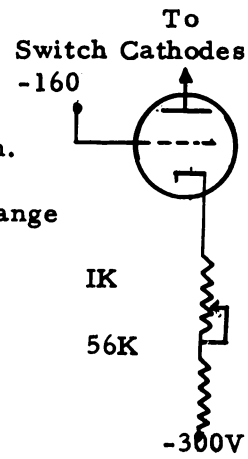

+150
OUTPUT
-160V
-10V
+340V
LNI Monitor Binary Decoder
For training purposes only
Date 10/1/59
FEK 1:40
S1
S2

4. Switching (See Decoder Drawing)



   a. Current is fed to ladder if FF in storage is cleared (-30V signal in).
   b. Current bypasses ladder if FF in storage is set (+10V signal in).

5. Current Sources (See Decoder Drawing)



   a. Four most significant stages utilize circuit shown.

      (1) Any change in current due to plate voltage change will be minimized (cathode bias regulation).

      (2) IK control of current.

   b. Next 3 stages utilize a pure resistive circuit - variable I with a 10K pot - cathode bias for "switch."

   c. Four least significant stages - a fixed resistance cathode bias for "switch."

6. Test Switches

   a. Switch (S1) - Module Alignment Switch

      (1) Operate - normal filaments and operation.
      (2) +100 - opens all shunts - causes half of each switch to pass current to ladder.
      (3) +125 - open all shunts - except hi order stage.
      (4) +150 - all stages are shunted.

   b. Switch (S2) - Decoder Stage Adjustment Switch

      (1) Output of switch is fed to pushbuttons on test panel (92CL) then to voltage test terminals.
      (2) Used to align each stage of the binary decoder.
      (3) Information on the use of the test switch can be found in Maintenance Handbook #11.

7. Outputs of Binary Decoders

Decoder Section	Output Voltage Drop When Bit is 0
2^9	25.000
2^8	12.500
2^9	6.250
2^6	3.125
2^5	1.563
2^4	0.782
2^3	0.391
2^2	0.196
2^1	0.098
2^0	0.049

C. Buffer Amplifier Operation

1. Function

a. Match Impedances

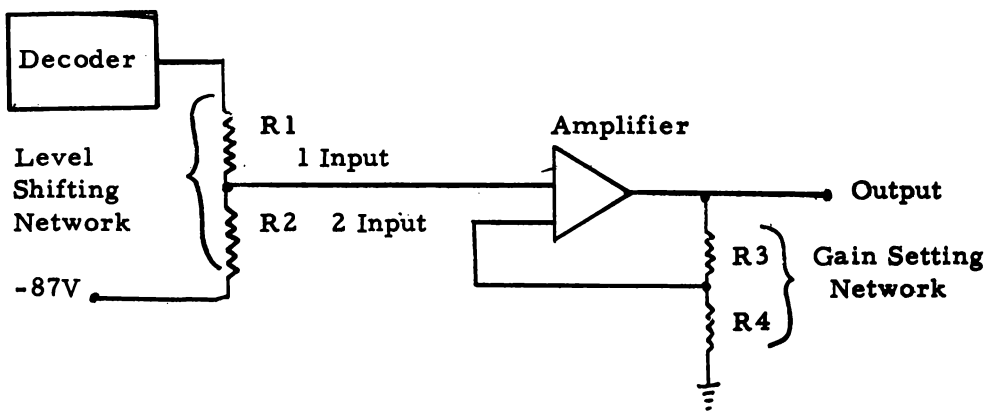
(1) Sine and cosine decoders to sine-cosine approximators.

(2) Range decoder to multipliers.

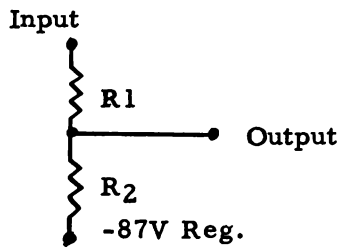
b. Re-reference Voltages

(1) Sine and cosine 150-100V to ±25V.
(2) Range 150-100V to 0-50V.

2. Block Diagram



a. Level shifting network



(1) $R_1 + R_2 = 1$ Meg (0.1%)
(2) R_1 & R_2 provide the necessary shift in voltage to reference signal properly.
(3) Some attenuation is encountered. (approx. 50%)

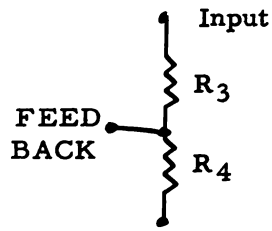
b. Amplifiers

(1) Have sufficient gain to overcome losses in level shifter.

(2) Gain is in excess of 3000, but attenuated by negative feedback.

(3) Cathode follower output to match impedances.

c. Gain Setting Network



(1) R3 + R4 = 100 K (0.1%)
(2) R3 & R4 are same ratio as R1 & R2.
(3) Control gain of amplifiers by controlling quantity of feedback.

3. Circuit Analysis

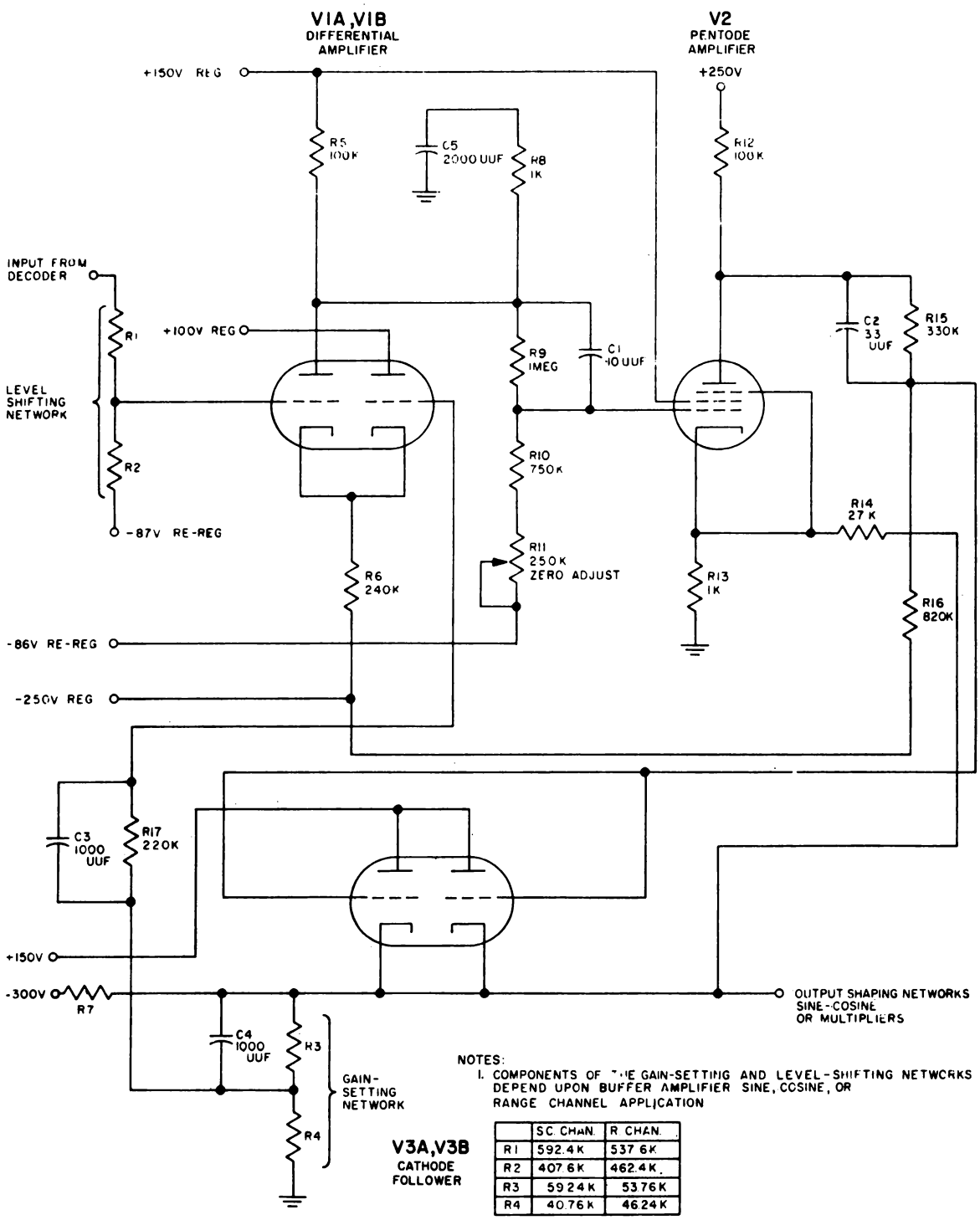
a. Page 1740 is the schematic diagram for the BU. The input signal is fed into a level-shifting network consisting of a resistor network in series with the

input level and reregulated -87V reference. The level shift obtained from this network is applied to the grid of V1A. The grid of V1B is connected through a resistor to a gain-setting network. The difference in levels between the grids of V1A and V1B (differential amplifier) is amplified in V1A. This amplified difference signal is direct-coupled through a resistor to the grid of pentode amplifier V2 where it is amplified considerably due to the high gain of the pentode. The signal is then coupled to the grids of paralleled output triode V3A and V3B.

b. In tube V2, the suppressor and cathode are tied together and returned through resistor R14 to the connected cathodes of V3A and V3B and through the gain-setting network to the grid of V1B. This means of compensating for the instability of direct-coupling effects is carried still further by supplying regulated voltages to critical points in the circuit. The tied cathodes of the differential amplifier are connected to the regulated -250V supply through cathode resistor R6. The plate of V1A is connected through plate load resistor R5 to a regulated +150V supply. The screen grid of V2 is connected directly to that supply. The plate of tube V1B is tied to a regulated +100V supply. The voltage-dropping network, consisting of resistors R9, R10, and zero-adjust potentiometer R11, is returned to a reregulated -86V supply.

c. The percentage of output potential that is fed back to the grid of V1B, through resistor R17 and capacitor C3, is determined by the ratio of resistors R3 and R4. These resistors form the gain-setting network.

d. Triode tube sections V3A and V3B are paralleled, in a cathode follower circuit, to increase the current handling capacity of the output stage. The buffer amplifier output is taken from the cathodes of this tube. The negative feedback and reference voltage stability contribute to the reliability of the buffer amplifier as a matching device. The level shift effected at the input to the differential amplifier results in a loss of gain which is more than offset by the operational gain of the impedance-converting amplifier.



NOTES:

1. COMPONENTS OF THE GAIN-SETTING AND LEVEL-SHIFTING NETWORKS DEPEND UPON BUFFER AMPLIFIER SINE, COSINE, OR RANGE CHANNEL APPLICATION

	SC CHAN.	R CHAN.
R1	592.4K	537.6K
R2	407.6K	462.4K
R3	59.24K	53.76K
R4	40.76K	46.24K

R 7 = 150K IN RANGE BUFFER CHANNEL
R 7 = 17K IN SINE-COSINE BUFFER CHANNEL

2. ALL SERVICE VOLTAGES ARE DECOUPLED IN THE PLUGGABLE UNIT
3. PARASITIC SUPPRESSORS HAVE BEEN OMITTED

Buffer Amplifier, Schematic Diagram

e. The values of level-shifting network resistors R1 and R2, and the gain-setting network resistors R3 and R4, depend on whether the buffer amplifiers are used as sine, cosine, or range buffer.

D. Sine Cosine Approximators

1. Purpose

a. Convert straight line approximations of sine and cosine voltages to voltages more closely approximating the functions.

b. Discussion that follows will consider all possible inputs at once. It should be noted that only a level is applied at a given moment.

c. Input is ±25V from Buffer.
d. Output is ± 16V more closely resembling a sine wave.

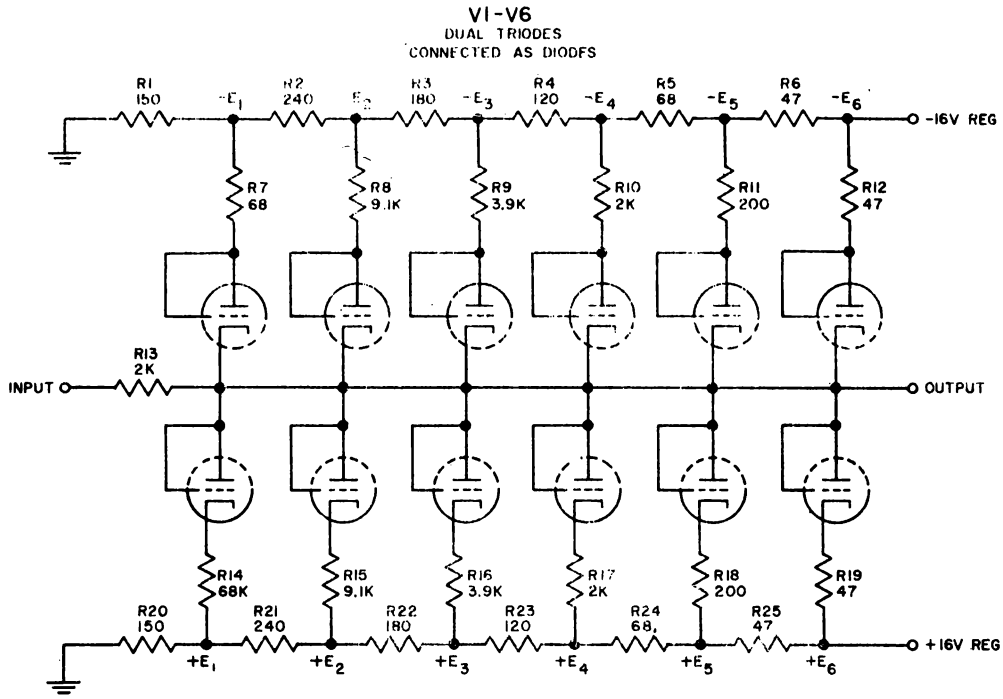
2. Operation

a. Page 1760 has a schematic diagram of the SCA, a table of detail parts, and graphs showing the input-output relationships of the SCA.

b. The SCA employs six twin triodes, each triode section functioning as a diode. Six of the diodes conduct for positive input voltage, and the other six conduct for negative input voltage. The 12 diodes are paired so that one positive and one negative conducting diode in one envelope are affected by a like change in voltage.

c. Positive bias is obtained from the +16V input and the voltage divider network consisting of R20 through R25; negative bias is obtained from the -16V input and the voltage divider network consisting of R1 through R6. The voltage divider networks are such that V1 responds to changes in the smallest voltage range (corresponding to the bias range between +E1 and +E2, or -E1 and -E2), and V6 responds to the largest voltage range.

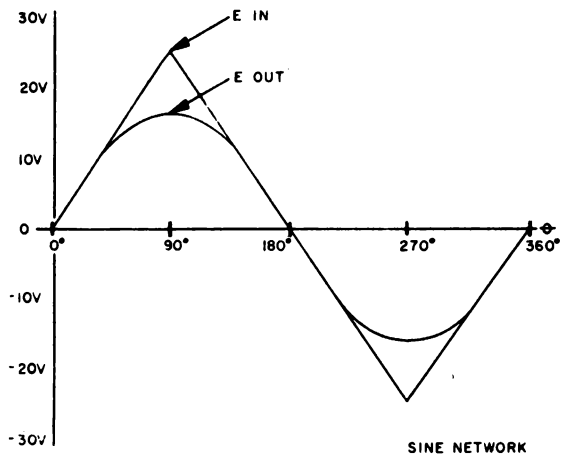
d. There is no output for the 0 voltage input because of the cutoff point at V1. Input voltage greater than the bias level at ±E2 causes V2 to conduct; this progression continues until all six stages are conducting when the input voltage is ±25V.

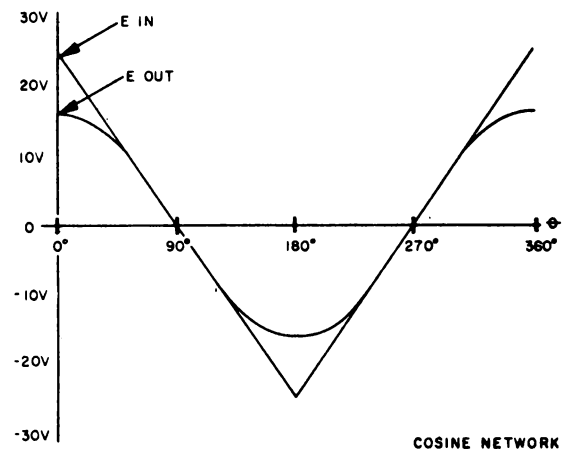


Sine-Cosine Approximator, Schematic Diagram

SINE-COSINE APPROXIMATOR, FUNCTION OF DETAIL PARTS

REFERENCE SYMBOL	FUNCTION
R1-R6	Voltage divider
R7-R12	Plate load resistors
R13	Input resistor
R14-R19	Cathode resistors
R20-R25	Voltage divider





e. The output of each stage is proportional to the input at that stage, but attenuation is inversely proportional to the input amplitude, and is affected by resistors R14 through R19 for positive input values, and by resistors R7 through R12 for negative input values. The attenuation factor for either positive or negative input voltages is the same for voltages of the same amplitude; it may be computed as illustrated by the following progressive formula:

$\frac{R13}{R13 + X1}$ when input is between +E1 and +E2

$\frac{R13}{R13 + X2}$ when input is between +E2 and +E3

$\frac{R13}{R13 + X3}$ when input is between +E3 and +E4

where $X1 = R14$

$$X2 = \frac{X1R15}{X1 + R15}$$

and $$X3 = \frac{X2R16}{X2 + R16}$$

f. This nonlinear attenuation in the sine-cosine approximator is calculated to produce a sinusoidal representation of the straight-line approximation input voltage.

(Note Page 1760)

3. Multiplier Operation

1. Purpose

a. Produces an output voltage proportional to product of two input voltages.

b. One to generate X deflection.

c. One to generate Y deflection.

2. Principles of Operation

a. Block Diagram (Refer to Page 1800)

(1) Inputs

(a) e1 = range (0 to +50 volts)
(b) e2 = sine or cosine (+16 or -16 volts)

(2) Output Eo = +20 to -20 volts approx.
(3) Input Stage.

(a) Amplifies e1 or e2 with a multiplication factor of K to give.

(b) Output of K (e1) = B2, Ke2 = B3

b. Operational Amplifier

(1) Input of e1 or e2 and a portion of input stage output Ke1 or Ke2.
(2) Output is difference between the two K(e1) - e1 or K(e2) - e2.

(a) Ke1 - e1 = (K-1)e1 = B1
(b) Ke2 - e2 = (K-1)e2 = B2

c. Oscillator

(1) Output of 2MC.
(2) Triangular wave.
(3) S = E = 100V peak to peak signal.
(4) Combines with B1 and B2 to form.

(a) B1 + S = B1
(b) B2 = S = B2

d. Diode Network

(1) Combines 4 inputs in 4 ways to get 4 signals.
(2) $C1 = \frac{1}{2E} (B1 - B3)^2$

(3) $C2 = \frac{1}{2E} (B2 - B3)^2$

(4) $C3 = \frac{1}{2E} (B2 - B4)^2$

(5) $C4 = \frac{1}{2E} (B1 - B4)^2$

(6) The four signals C1, C2, C3, and C4 are then recombined to get two outputs from the network - D1 and D2.

(7) $D1 = \frac{C1 + C3}{A}$

(8) $D2 = \frac{C2 + C4}{A}$

(9) A = a constant factor controlled by circuit values to keep voltages within reason.

e. Operational Amplifiers

(1) Take difference of input signals.

(2) $\frac{D1 - D2}{B} = Eo$

(3) B is a constant factor.

f. Substitution in the formulas given will prove that Eo = el · e2 ·, X where X is a constant referred to as a scale factor (approx. 1/25).

3. Operation Analysis

a. Input Stage (Page 1800)

(1) Input e1 or e2 (range, sine, or cosine)
(2) Gain of stage (approx. 0.6) K
(3) Output K(e1) or K(e2)
(4) To operational amplifier K(e1) 2 or K(e2) 2.
(5) R7 pot. - adjust for OV out with OV in.

b. Operational Amplifier (Page 1820), Fig. 1)

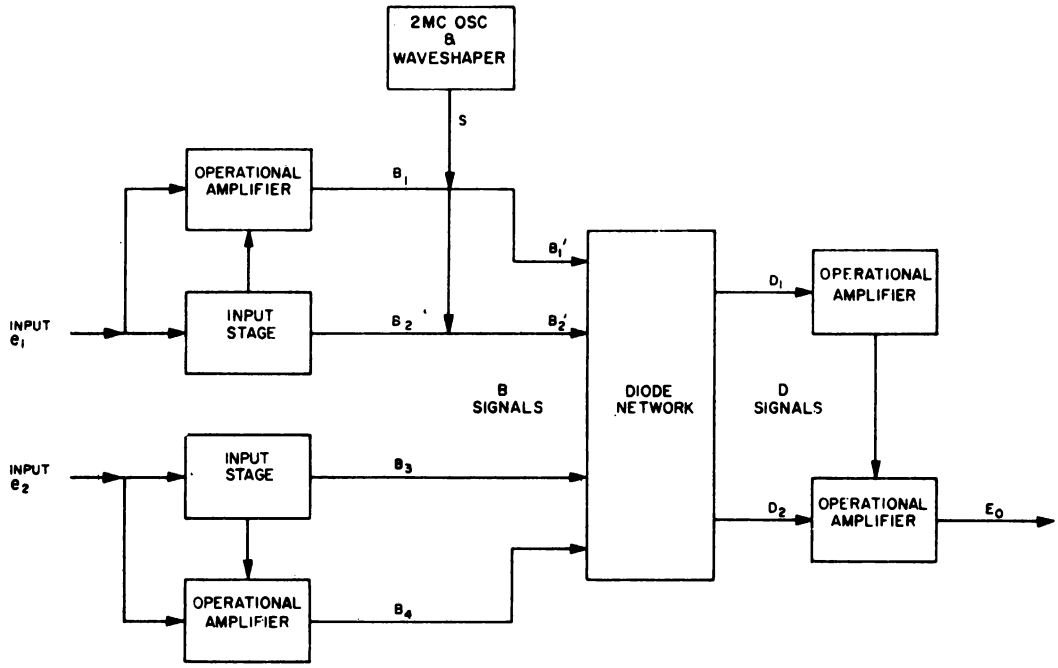
(1) Inputs to differential amplifier.

(a) Different for various applications.
(b) Four are used in multiplier.

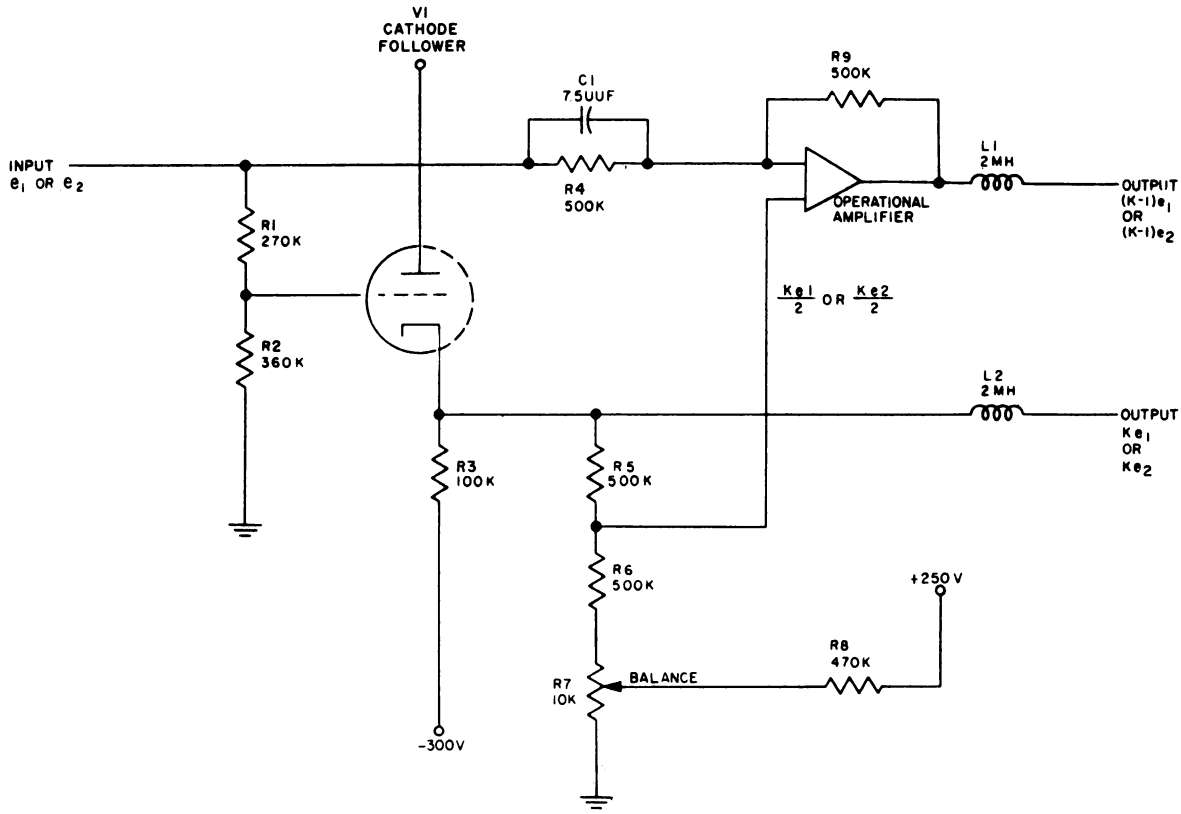
(2) Difference of two signals is fed to pentode.

(3) High gain stage and much feedback from cathode follower output for linearity and stability.

(4) Output resistor R varies with application.



Multiplier, Block Diagram



Multiplier, Input Voltage Divider Network, Schematic Diagram

c. Oscillator and Wave Shaper (Page 1820, Fig. 3)

(1) Output of Oscillator

(a) Approximately 2 megacycle sine wave.
(b) 300 volts peak to peak.

(2) Converted to square wave by DC restorer and diode.

(3) Charge and discharge of 10 uuf capacitor is linear resulting in a triangular wave of approximately 100 volts peak to peak.

d. Diode Network (Page 1830).

Note

The following information is for reference and is not important to the overall understanding of the multiplier.

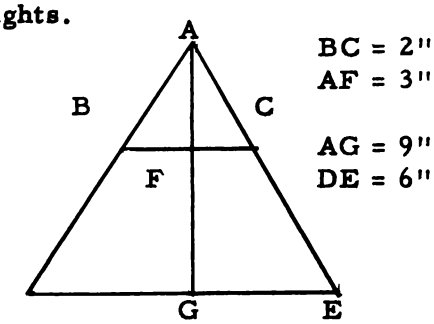
(1) Four pair of diodes are used - each pair operates similarly - comparable to an OR circuit.

(2) Function is to take difference of two inputs and square it.

(3) C2 will be used as an example.

(a) Input 1 is $B^3 = K(e2)$.
(b) Input 2 is $B2^1 = S + K(e1)$.
(c) Output should be $\frac{1}{2E}(B2 - B3)^2$

(4) Note the fact that areas of similar triangles are proportionate to square of their heights.



(a) A = 1/2 bh
A = 1/2 - 2-3 = 3 sq"

(b) A = 1/2 bh
A = 1/2 - 6 - 9 = 27 sq"

(c) $\frac{3}{27} = \frac{(AF)^2}{(AG)^2} = \frac{(3)^2}{(9)} = \frac{9}{81} = \frac{1}{9}$

(5) Input 2 is $B2^1 = S + K(e1)$

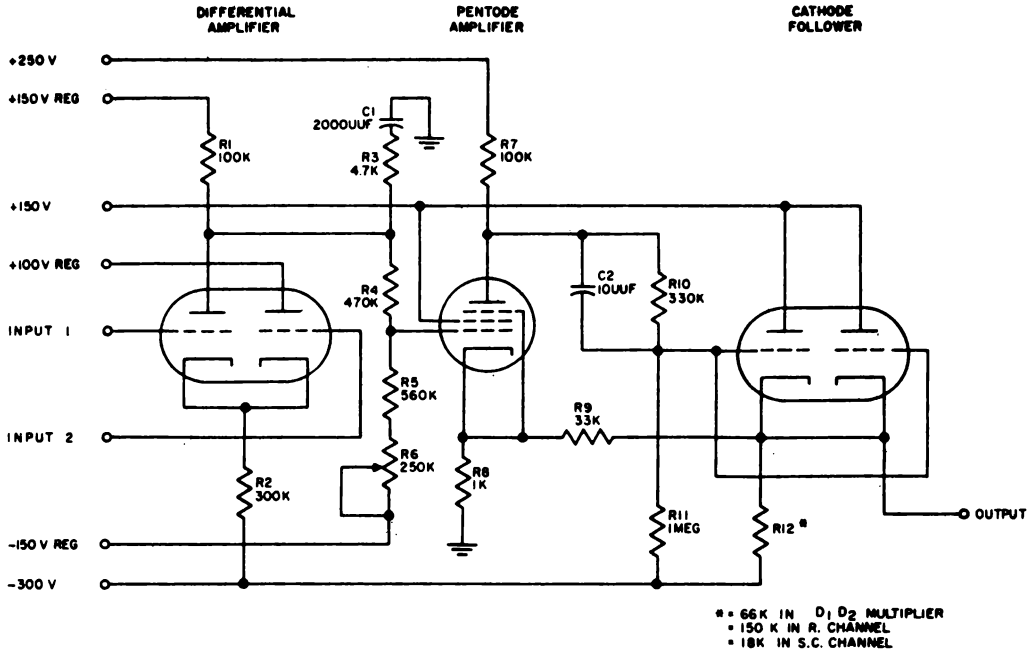


Figure 1 *Multiplier, Operational Amplifier, Schematic Diagram*

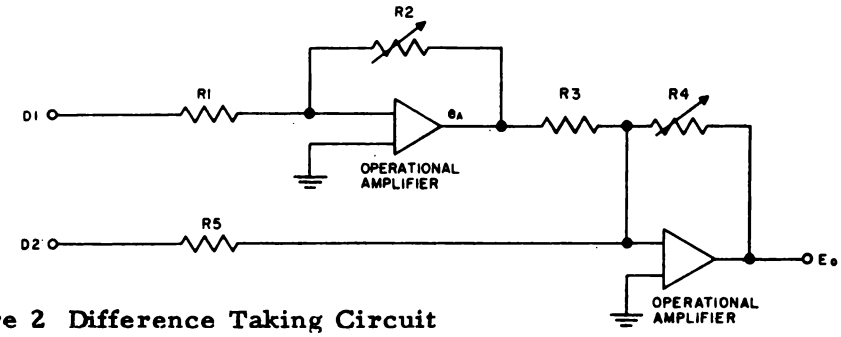


Figure 2 Difference Taking Circuit

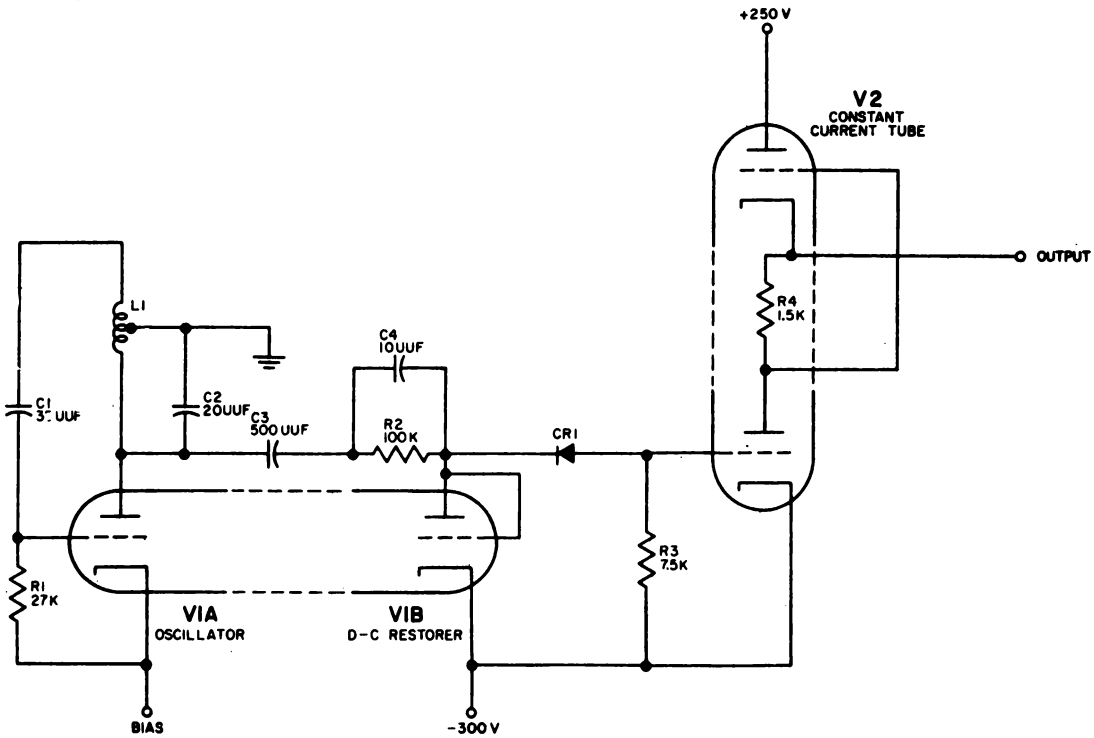
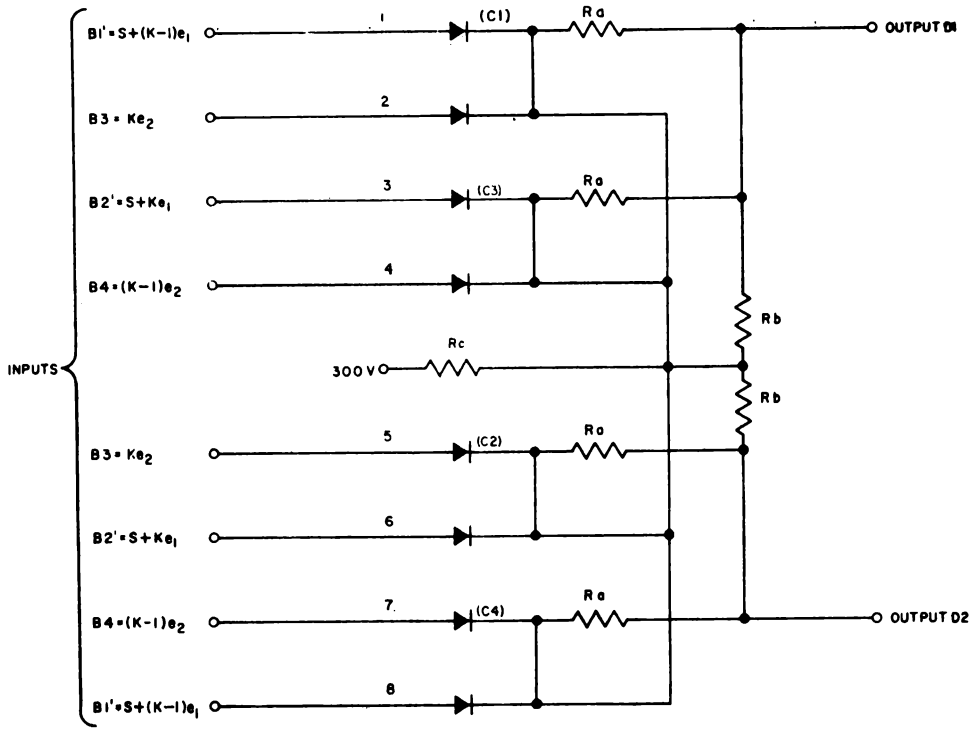
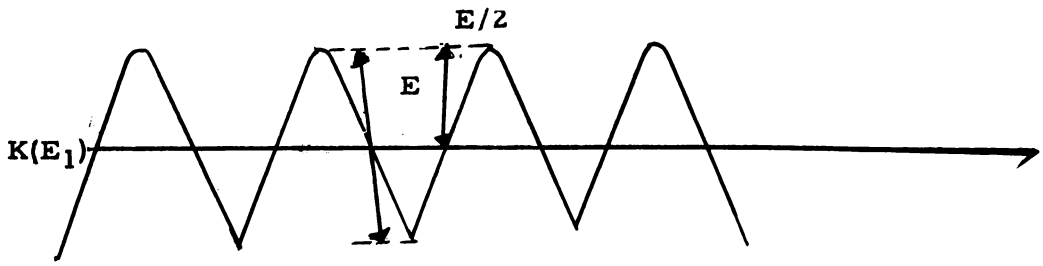


Figure 3 *Multiplier, 2-Megacycle Oscillator, Schematic Diagram*



Multiplier, Diode Network, Schematic Diagram

REFERENCE SYMBOL	FUNCTION
	INPUT VOLTAGE DIVIDER NETWORK
R1, R2	Input voltage divider for V1
R3	V1 cathode resistor
R4	Part of input coupling network (with C1) to operational amplifier
R5, R6	Voltage divider (with R7)
R7	Balance control and part of voltage divider (with R5 and R6)
R8	Voltage-dropping resistor
R9	Current-limiting resistor
C1	Part of input coupling network (with R4) to operational amplifier
L1, L2	Peaking coils
	OPERATIONAL AMPLIFIER
R1	V1A plate load
R2	V1 cathode resistor
R3	Part of V2 grid return network (with C1)
R4, R5	Voltage divider (with R6)
R6	Gain control and part of voltage divider (with R4 and R5)
R7	V2 plate load
R8	V2 cathode resistor
R9	Feedback resistor from output to V2
R10	Part of voltage divider (with R7 and R11) and d-c coupling resistor
R11	Part of voltage divider (with R7 and R10)
R12	V3 cathode resistor
C1	Part of V2 grid return network (with R3)
C2	Speedup capacitor
	2-MEGACYCLE OSCILLATOR
R1	Bias resistor for V1A
R2	Part of coupling network (with C3 and C4)
R3	Bias resistor for V2
R4	Part of V2A plate load (with V2B)
C1, C2	Part of tank circuit (with L1)
C3, C4	Part of coupling network (with R2)
L1	Part of tank circuit (with C1 and C2)
CR1	Clamping diode



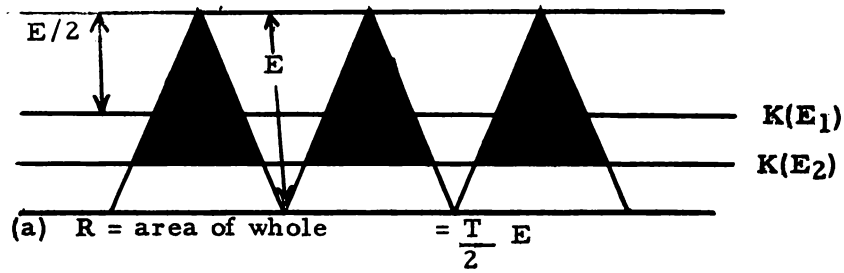
(a) S (100V peak to peak triangular wave) is riding on Ke 1.

(b) e1 has a range of 0-50V (since K is approximately 0.6) then K(e1) must be positive and between 0V and +30V.

(6) Input 1 is Ke2

(a) A level between + 16V and -16V times K (approx. + 10 to -10)

(7) Output



(a) R = area of whole $= \frac{T}{2} E$

r = shaded area

$$\frac{r}{R} = \frac{(E/2 + Ke1 - Ke2)^2}{E} = \frac{(B2' - B3)^2}{E}$$

$$r = R \frac{(B2' - B3)^2}{E}$$

$$r = T \quad 1/2E = (B2' - B3)^2$$

$$\frac{r}{T} = \frac{\text{voltage}}{\text{time involved}} = \text{average voltage out} = C2$$

$$C2 = 1/2E (B2' - B3)^2$$

(b) D1 = C1 + C3

(1) Accomplished by furnishing a common load for the 2 signals.

(2) Same for D2.

(c) Triangle wave is removed from output voltages by use of integrating network.

4. Difference Taking Circuit (Page 1820, Fig. 2)

a. Use of differential amplifiers results in obtaining differences between D1 and D2.

b. Feedback is controlled by R3 and R5 to obtain proportion of e1 e2 desired.

5. Numerical Examples (Page 1860)

a. Note mathematical procedure to obtain desired results for both examples.

NUMERICAL EXAMPLE OF MULTIPLIER FUNCTION

Circuit Constants: K (*gain of cathode follower*) $= 0.6$

E (*amplitude of 2-mc wave*) $= 100V$ *peak-to-peak*

Sf (*scale factor*) $= 25$

AB (*calibrated resistance factor*) $= 0.25$

CASE 1	CASE 2
Input: $e_1 = 5V$	Input: $e_1 = 20V$
$e_2 = 10V$	$e_2 = 5V$
Output: $\frac{e_1 e_2}{25} = E_o$	Output: $\frac{e_1 e_2}{25} = E_o$
Derivation:	Derivation:
$B_{1'} = S + B$	$B_{1'} = 42V$
$= \frac{E}{2} + (K-1)e_1$	
$= \frac{100}{2}(-2) = 48V$	
$B_{2'} = S + Ke_1$	$B_{2'} = 62V$
$= \frac{100}{2} + 3 = 53V$	
$B_3 = Ke_2 = 6V$	$B_3 = 3V$
$B_4 = (K-1)e_2 = -4V$	$B_4 = -2V$
$C_1 = \frac{E}{2}\left(\frac{B_{1'} - B_2}{E}\right)^2$	$C_1 = 7{,}605V$
$= \frac{100}{2}\frac{42^2}{100} = 8{,}820V$	
$C_2 = \frac{E}{2}\left(\frac{B_{2'} - B_3}{E}\right)^2 = 11{,}045V$	$C_2 = 17{,}405V$
$C_3 = \frac{E}{2}\left(\frac{B_{2'} - B_4}{E}\right)^2 = 16{,}245V$	$C_3 = 20{,}480V$
$C_4 = \frac{E}{2}\left(\frac{B_{1'} - B_4}{E}\right)^2 = 13{,}520V$	$C_4 = 9{,}680V$
$D_1 = \frac{C_1 + C_2}{A} = \frac{25.065}{A}$ *volts*	$D_1 = \frac{28.085}{A}$ *volts*
$D_2 = \frac{C_2 + C_4}{A} = \frac{24.565}{A}$ *volts*	$D_2 = \frac{27.085}{A}$ *volts*
$E_o = \frac{D_1 - D_2}{B} = \frac{0.5}{AB}$ *volts*	$E_o = \frac{1}{AB}$ *volts*
$E_o = 2V$	$E_o = 4V$

F. Distribution Power Amplifier Operation

1. Purpose

a. Buffer action between multiplier and console deflection amplifiers.

b. Furnish power for signal to drive 4 consoles.

c. Non-Logical Circuit (Amplifies levels)

2. Circuit Operation (Refer to Page 1880)

a. Differential Amplifier (V1)

(1) R 6 establishes operating point by setting bias.

(2) Other input is feedback from output to obtain good regulation and stability.

b. Series regulator (V2A)

(1) Compensates for V1B variations.

c. Cathode follower (V2B)

d. High gain pentode amplifier (V3)

(1) Allows a large amount of feedback to increase regulation.

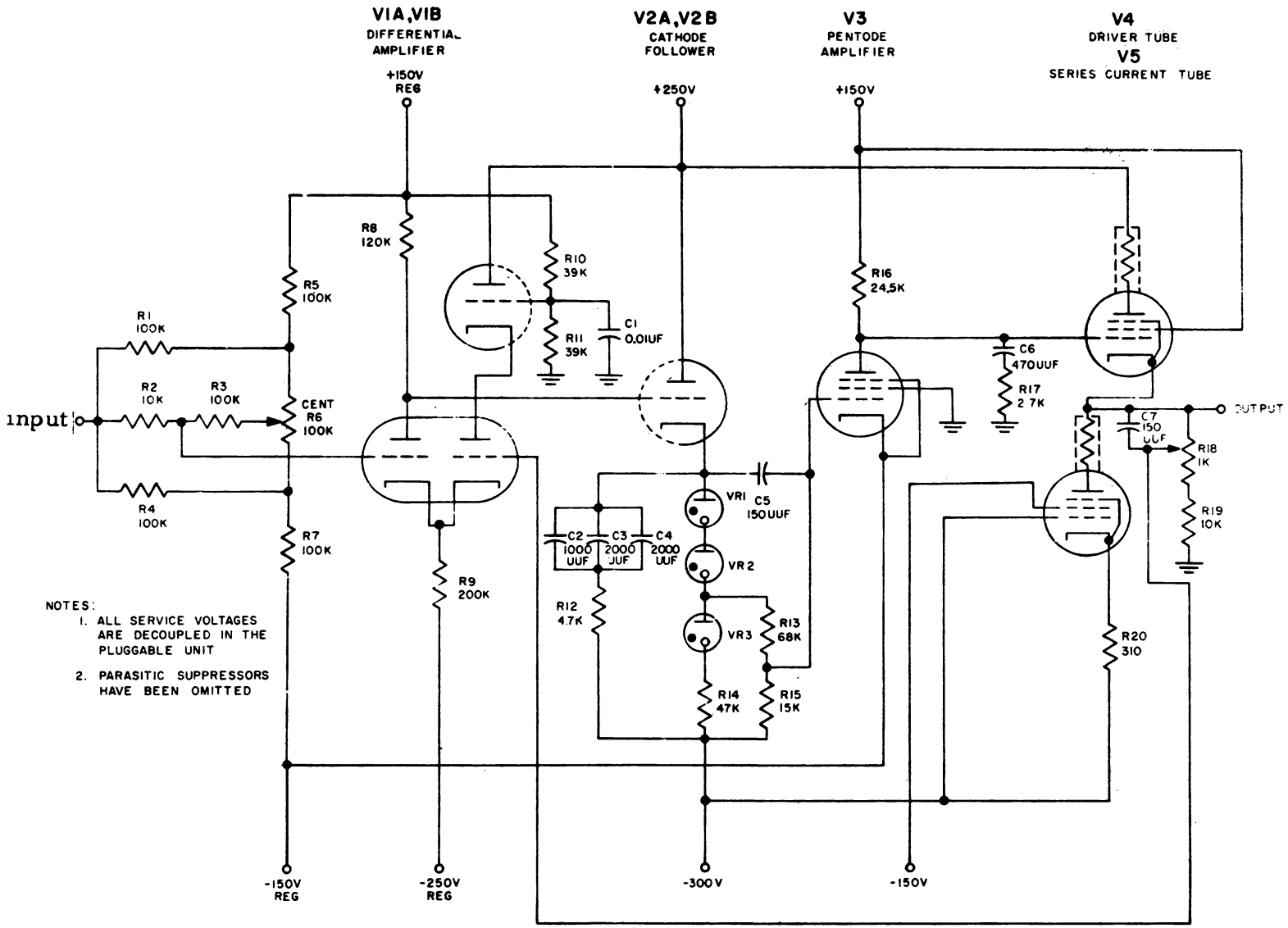
e. Output cathode follower (V4)

f. Series regulator (V5)

G. Alignment Panel

1. Purpose

a. Alignment circuits and reference voltages are incorporated in the analog circuitry to assure required accuracy of target presentation. A test panel in 93CL mounts an array of pushbutton switches which are operated in combination to bring out critical points in the circuitry to test receptacles. The outputs of all the signals' stages are thus made easily measurable: binary decoders, buffer amplifiers, sine and cosine approximators, multipliers and distribution power amplifiers.



Distribution Power Amplifier, Schematic Diagram

In addition, provision is made to check the individual stages of the binary decoders, +16, -16, -150, and -250 regulated voltages, and the reference voltage utilized in the binary decoders. A toggle (NORMAL-REVERSE) switch permits the polarity of the voltage at the test points to be reversed.

b. The test panel is used as follows. In each of the four rows of pushbuttons, one pushbutton, called the ROW 1, ROW 2, ROW 3, or ROW 4 pushbutton makes the other pushbuttons in the row effective. For example, to bring the output of the cosine binary decoder to the test points, the ROW 2 pushbutton is depressed; then the COS BD OUT pushbutton in row 2 is depressed.

2. Multiplier Alignment

a. A multiplier alignment circuit is included in the analog section to provide test voltages for aligning the multipliers. The multiple alignment unit generates a-c voltages which are used to drive the multipliers through their complete range of possible input signals. Operation is as follows. A three position switch is located on the front panel of the multiplier alignment pluggable unit. With this switch set to the OPERATE position, the multipliers operate normally; the multiplier alignment circuit is without effect. With the switch in the ALIGN RANGE position, the multiplier alignment circuit provides a 50-volt peak-to-peak a-c input to the range inputs of the multipliers and grounds the azimuth inputs. Adjustments are then made on the multipliers to provide a zero output (as nearly as possible) throughout the entire range of the a-c input. With the switch set to the ALIGN AZIMUTH position, the multiplier alignment circuit provides a 32-volt peak-to-peak a-c input to the azimuth input of the multipliers and grounds the range inputs. Again adjustments are made on the multipliers to provide a zero output (as near as possible) throughout the entire range of the AC input.

b. Refer to the MI Manual for added information.

H. Introduction to Monitor Consoles

1. General Features

a. Each display console contains a 16-inch CRT on which a plan-position indications (PPI) type of display is produced. Also found in all consoles are the following:

(1) A UNIT STATUS switch which determines the power status of the console and which may be used to connect the console to either the active or standy duplex machine,

(2) A high-voltage power supply which provides the necessary CRT high voltages.

(3) Two pluggable interchangeable deflection amplifiers to position the display.

2. Units 622 and 623

a. The 622 and 623 display consoles are identical. At each, messages are selected for display by means of SITE and MESSAGE selection controls mounted in two 15-button interlocked-release pushbutton banks, one bank on each side of the CRT.

3. Unit 620 (Logic S2.5.3)

a. Unit 620 differs from units 622 and 623 in that the message selection controls for this console are remoted to auxiliary control unit 947.

I. Monitor Console Controls

1. Unit Status Switch - 5 positions

a. Filament - filament power from standby supply C or D.
b. Power On - DC and filament power from standby supply C or D.

c. Standby - DC and filament power from standby supply C or D and signal from standby common A or B.

d. Off - no signal or power.

e. Active - DC and filament power from active supply C or D and signal from active common A or B.

2. Message Label Selection - 15 pushbuttons Logic S2.5.3

a. Controls 5 levels to control circuitry.

b. 15 buttons control relays which in turn results in +10 or -30 volt levels to compare circuitry.

c. The 0 button is the "Multiple Message Label" selection and will select all message types for display except 17 and 19 which are HF messages and never displayed.

d. Other 14 buttons select individual message types.

e. Code is in complement form. A message label of 10101 would require voltages of -30, +10, -30, +10, -30 from selection buttons. Circuitry will bear this out.

3. Site Labels Selection - 15 pushbuttons Logic S.2.5.3

a. Control 4 levels to control circuitry.
b. Code is in complement form as message label selection.
c. Count is in sequence unlike message label selection.
d. Button 0 +10, +10, +10, +10
e. Button 1 +10, +10, +10, -30
f. Button 2 +10, +10, -30, +10
g. Button 14 -30, -30, -30, +10
h. No site in operation is connected to more than 14 LRI sites.

4. Controls listed above are used for each console.

a. Message label and site ident. for 620 are controlled by Unit 953.

b. All other controls are located on the console.

J. Monitor Console Operation

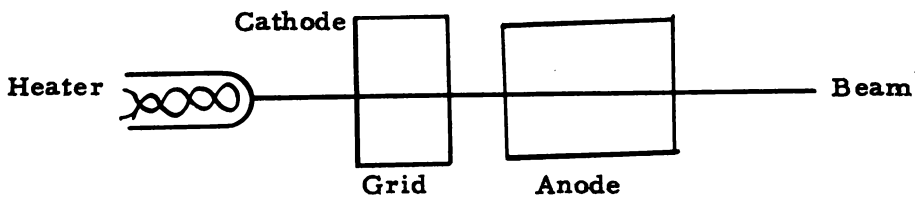
1. Cathode Ray Tube Logic S2.5.3

a. The CRT used for display is a conventional magnetic deflection-tube, employing a typical electron gun and a round 16-inch screen coated with a medium-persistence phosphor. When a target is to be displayed; the magnetic deflection fields are set by the yoke; then the electron beam is turned on for 20 usec by a 40V instensification pulse.

b. Electron gun

(1) Forms beam of focused electrons.
(2) Source - cathode
(3) On-off control - grid
(4) Shaper - focus anode

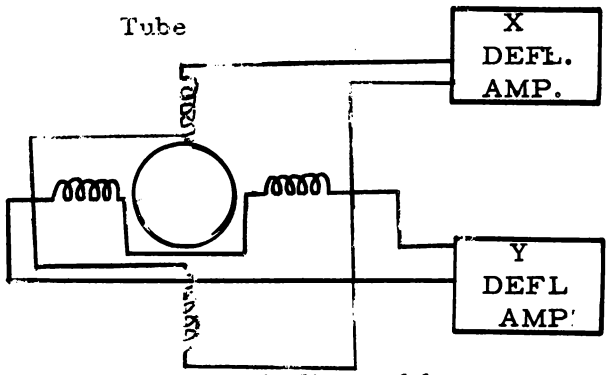
a) Some shaping done by physical shape of anode.
b) Some by electrostatic field effects.



c. Electro magnetic deflection

(1) Horizontal deflection coils are located physically above and below tube neck.

(2) Vertical coils are physically to left and right of tube.



(3) Electromagnetic lines of force - current thru coil establishes lines of force beam passing thru field is deflected.
In example
shown beam
will move to
the left.

d. Accelerating anode

(1) Hi potential to accelerate beam.

(a) +7.5 KV
(b) +2.5 KV

(2) Beam hits screen at high velocity and results in illumination.

2. High-Voltage Power Supply

a. A high-voltage power supply is located on each LRI monitor console. It provides 2,500 and 7,500V for the accelerating anodes of the CRT and it is powered through the UNIT STATUS switch and relays located in the console. Major components of the high-voltage power supply are the transformer, selenium bridge rectifier, filtering circuit, and load resistors. A voltmeter is mounted on the front of the power supply unit for monitoring the output.

3. Deflection Amplifiers

a. Current delivered by the distribution power amplifiers in the analog section is not sufficient to drive the CRT deflection coils, and therefore, must be amplified. This is done in deflection amplifiers, two of which, a

horizontal and a vertical deflection amplifier, are located in each of four LRI monitor consoles.

b. Function

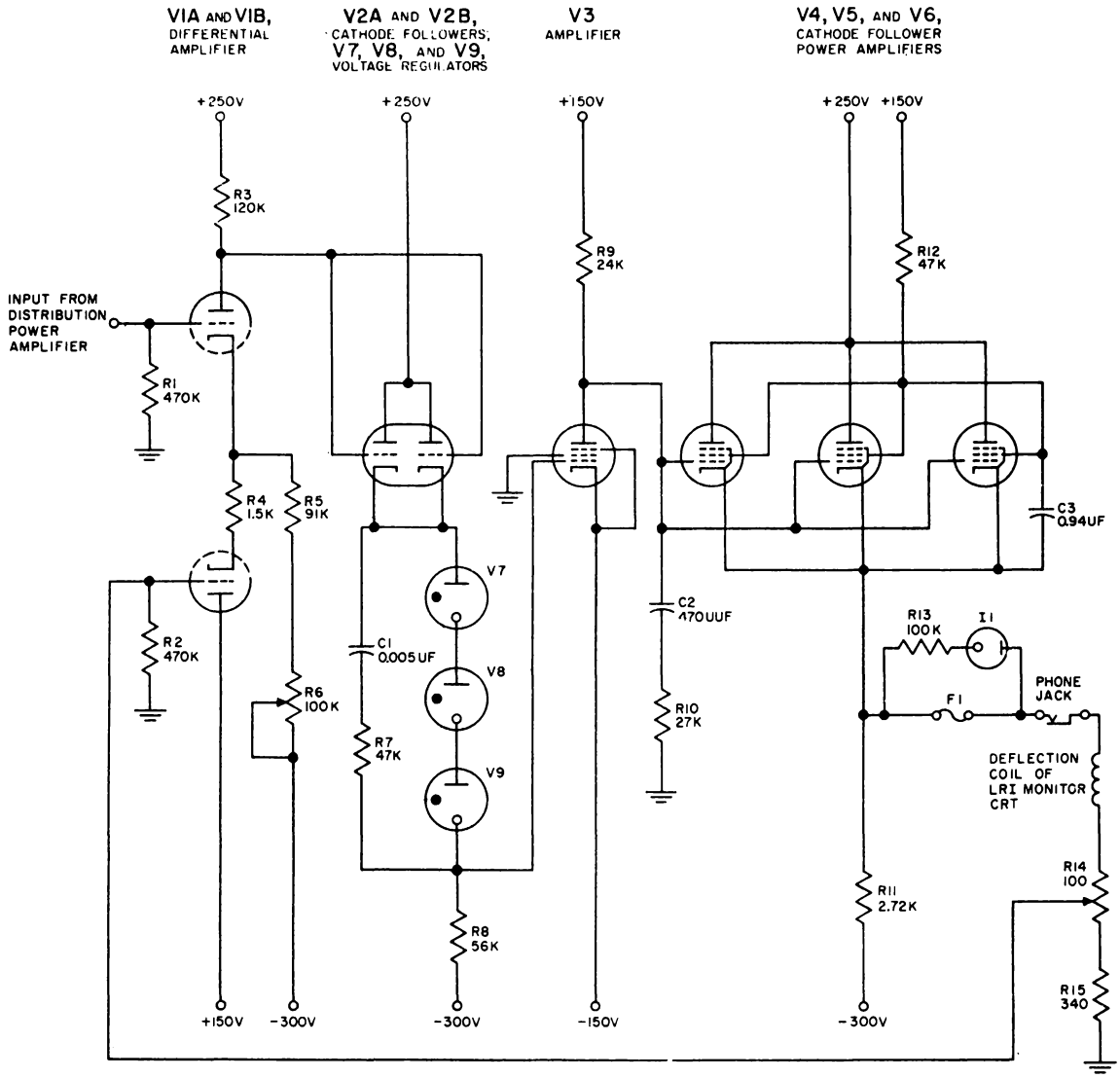
(1) Furnish current for deflection coils to CRT (+70 to -70 m amps)

(2) Current is proportional to input voltage (+20 to -20 volts)

c. Operation (Refer to Page 1950)

(1) The analog voltage obtained from the distribution power amplifier is applied to the grid of V1A. The signal at the grid of V1B is a percentage of the DA output voltage that appears across the voltage divider consisting of R14, R15, and the d-c resistance of the deflection coil. Since the polarity of the output is the same as that of the input, the voltage at the grid of V1B is of the same polarity, but smaller in magnitude, as the grid voltage of V1A. The cathodes of the differential amplifier (V1A and V1B) are returned to -300V through a common return consisting of R5 and R6. Therefore, the output of the differential amplifier is a function of the grid voltages appearing at both V1A and V1B. In effect, the voltage difference between the two grids is amplified in the plate circuit of V1A. Since current is diverted from V1A through V1B, the input to V1B functions as generative feedback in addition to establishing the reference for the differential input. The setting of potentiometer R14 determines the amount of feedback and therefore, is established as the gain control. Potentiometer R6 is used to establish a zero reference (centering) with no input to the DA.

(2) The output of V1A is direct-coupled to the cathode follower comprised of V2A and V2B connected in parallel. The cathodes of this stage are maintained at a constant positive potential through the action of three series-connected voltage regulator tubes (V7, V8, and V9). The cathode follower effects a match between the positive level of the plate of V1A and the negative level at the grid of V3. In effect, this stage acts as a voltage divider between the plate potential



Deflection Amplifier, Input System, Schematic Diagram

C1	Part of high-frequency bypass network (with R7)
C2	Part of high-frequency bypass network (with R10)
C3	Coupling capacitor for degenerative feedback from screen grid to cathode for V4, V5, and V6
F1	Fuse for deflection coil
I1	Blown-fuse indicator
R1, R2	Grid return resistors for V1A and V1B, respectively
R3	Plate load resistor for V1A
R4	Cathode resistor for V1B
R5	Common cathode resistor for V1A and V1B (with R6)
R6	Centering control
R7	Part of high-frequency bypass network (with C1)
R8	Cathode resistor for V2A and V2B
R9	Plate load resistor for V3
R10	Part of high-frequency bypass network (with C2)
R11	Common cathode resistor for V4, V5, and V6
R12	Screen-dropping resistor for V4, V5, and V6
R13	Current-limiting resistor for I1
R14	Gain control
R15	Part of voltage divider (with R14 and deflection coil)

of V1A and -300. The voltage developed across resistor R8 (the output of V2A-V2B) is direct-coupled to high gain pentode amplifier V3. The cathode and suppressor grid are returned to -150V. Returning the cathode to -150V enables the plate potential to be reduced sufficiently to serve as the control grid voltage for the succeeding output stage.

(3) The output cathode follower stage consists of three power amplifiers (pentodes V4, V5, and V6) connected in parallel. Degenerative feedback, screen grid to cathode through capacitor C3, is employed to ensure stable operation at the output stage. The output, a constant current proportional to the analog input, is fed through fuse F1 and a phone jack (test point for an ammeter) to the deflection coil. The fuse is paralleled by neon light I1 that is employed as a blown-fuse indicator. Refer to the following discussion on the calibration test panel for the function of the controls.

4. Calibration Test Panel

a. A test panel is incorporated in each console to permit calibration of the deflection amplifiers and adjustment of signal intensity. It is located beneath a hinged cover on the top of the console. The test panel simplified circuit is shown on Page

b. Circuit discussion (Page 1980)

(1) Normal status as shown.

(a) Intensification pulse AC coupled to grid
(b) Bias controlled by R41 "Signal Intensity"
(c) X and Y signal - directly to amplifiers.

(2) Calibrate status - K23 and K24 energized.

(a) Grid controlled by R44 "Calibration Intensity" - allows CRT to be unblanked without signal in.

(b) Deflection amplifier inputs controlled by calibrate selection buttons and associated bleeder.

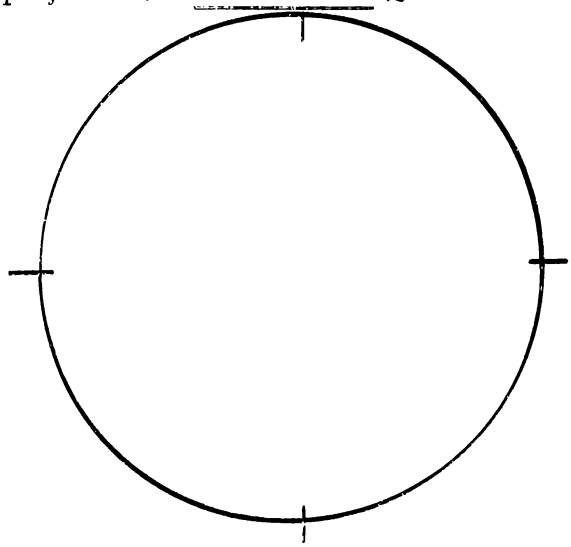
(1) Buttons are interlocked.
(2) Voltages adjustable.

c. Panel Description

(1) Interlock switch for HV supply - bottom center.
(2) Calibrate switch (S11) - upper left
(3) Calibrate controls - upper center
(4) Test points - upper right, bottom left and right
(5) Calibrate selection buttons - center
(6) X or Y "Amplifier Centering" = cathode resistor of 1st stage of DA.
(7) X or Y "Amplifier Gain" = resistor controlling feedback of DA.
(8) Fuses in series with deflection coils - lower left and right.
(9) Neon lights if fuse blows - by fuse
(10) Jack for measuring deflection current - by fuse

K. Summary Questions

1. A target with a magnetic bearing of 235° from true north would be displayed in the _____ Quadrant.

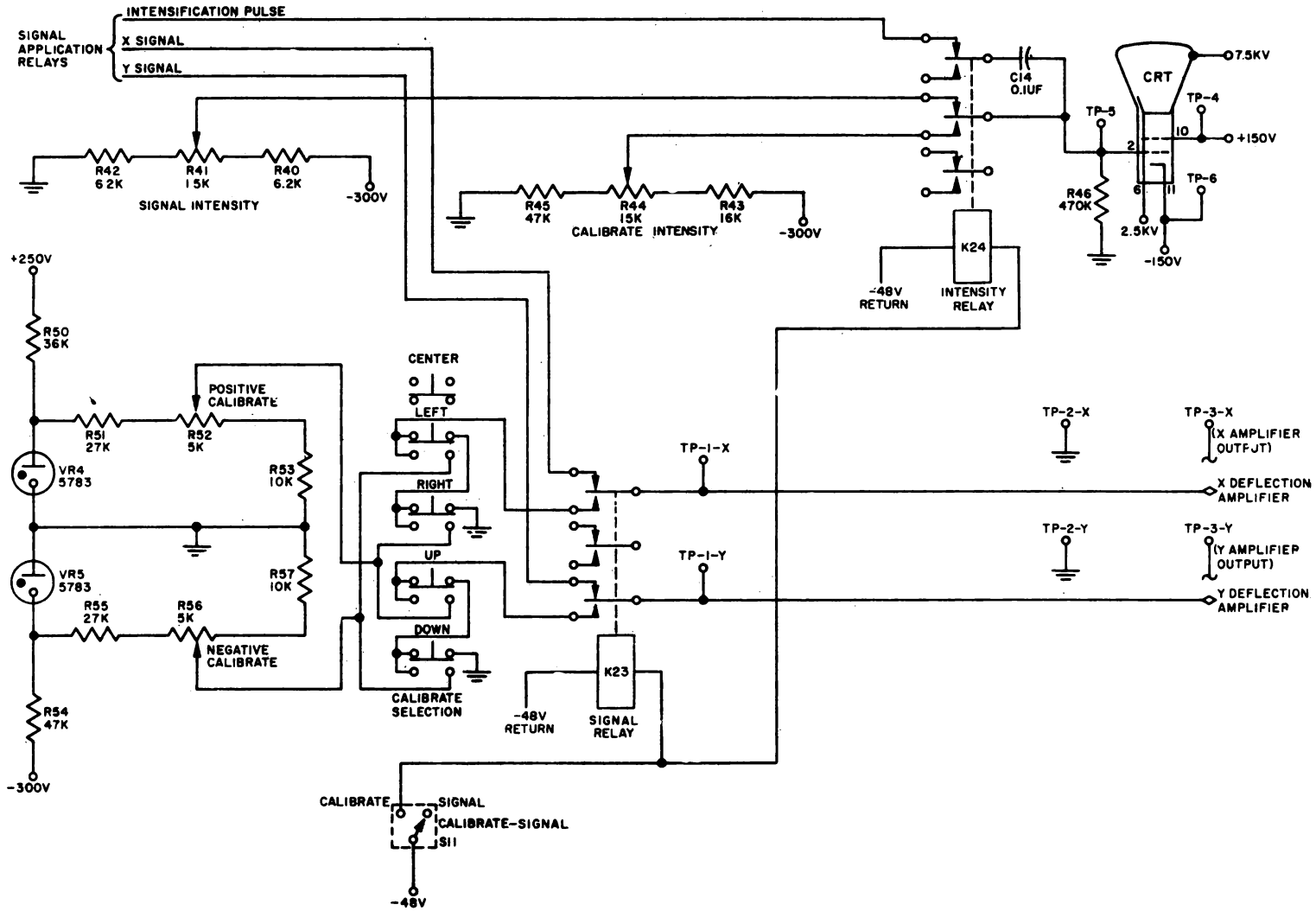


2. Consider the above illustration of the face of a PPI display with Cartesian Coordinates Positioning. Which statement is most correct?

a. x deflection is from a to b, y deflection is from c to d, range is 1/2 maximum.

b. x deflection is from c to d, y deflection is from a to b, range is 1/2 maximum.

c. x deflection is from a to b, y deflection is from c to d, range is 1/4 maximum.



Calibration Test Panel, Circuit Diagram

1980

d. x deflection is from c to d, y deflection is from a to b, and range is 3/4 maximum.

e. x deflection is from a to b or c to d, y deflection is from a to c or d to b, and range is 1/2 maximum.

VIII LRI MONITOR, SWITCHING SECTION & CAMERA CONTROL

A. Introduction

1. The switching section contains the controls, indicators, and circuitry required to control the operation of the LRI monitor. Specifically, it performs the following functions. (Refer to Page 2020).

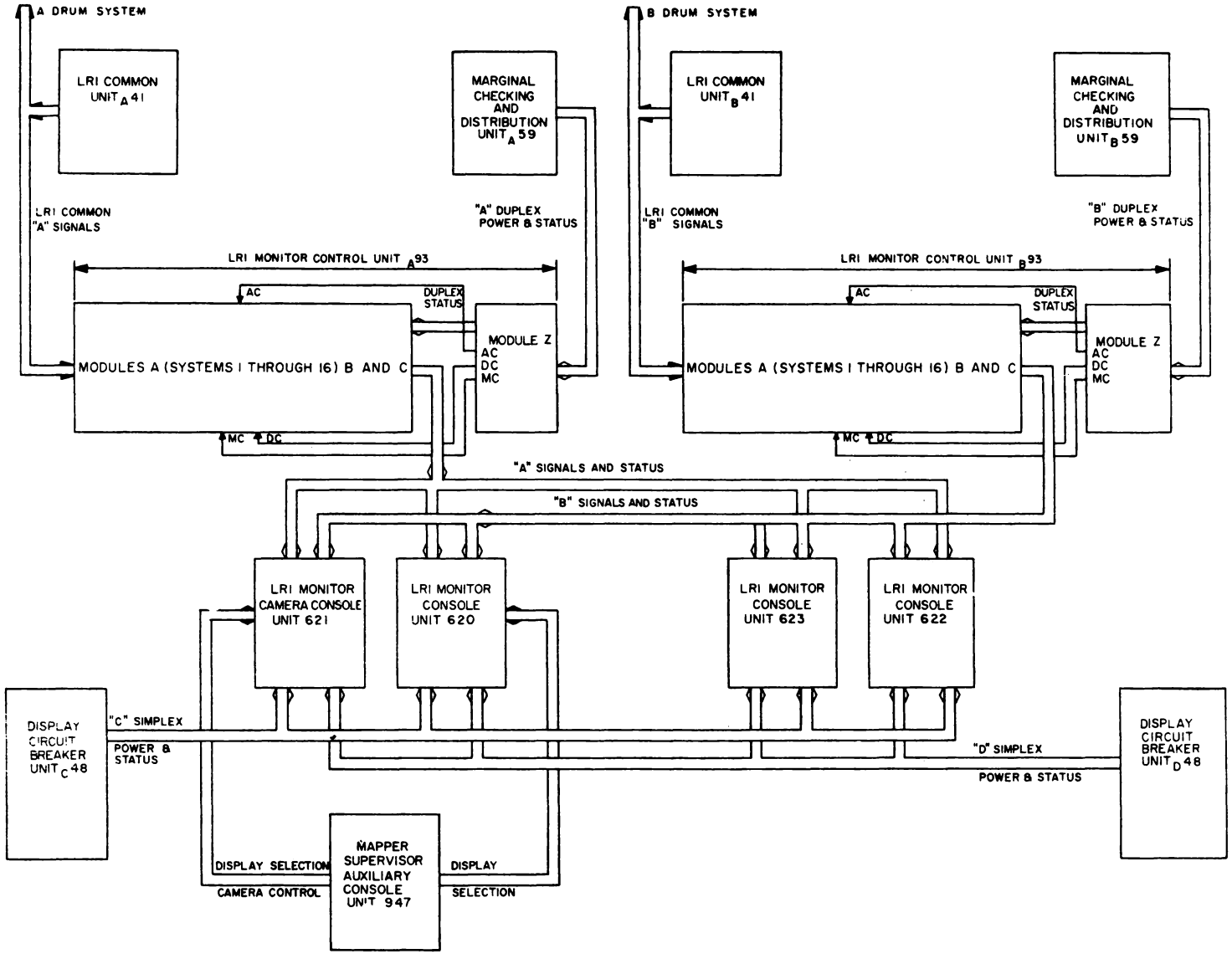
   a. Determines which of the two simplex power supplies will supply power to each monitor console.

   b. Determines which half of the duplexed LRI monitor control unit, 93A or 93B, will be connected to a particular console; that is, will feed intensification and deflection levels to the CRT, and receive site identity and message label levels from the console.

   c. Provides controls (site identity and message label pushbuttons) and associated circuitry for message selection.

   d. Controls operation of the camera, including start-stop, and film exposure-time selection. Indicates, within the camera field, site identity and message label selection and film exposure-time selections. Also provides indications of alarm conditions pertaining to camera operation.

2. Physically, the switching section is distributed among the four display consoles of the monitor and auxiliary control console unit 953. Functionally, it may be thought of as consisting of four subsections: unit status switching, signal application relay circuitry, site identity and message selection circuitry, and camera control circuitry. The relationship of these subsections to each other and to other portions of the LRI monitor is illustrated on Page and described generally, for a typical console, on Page



Relationship of LRI Monitor to Associated Equipment

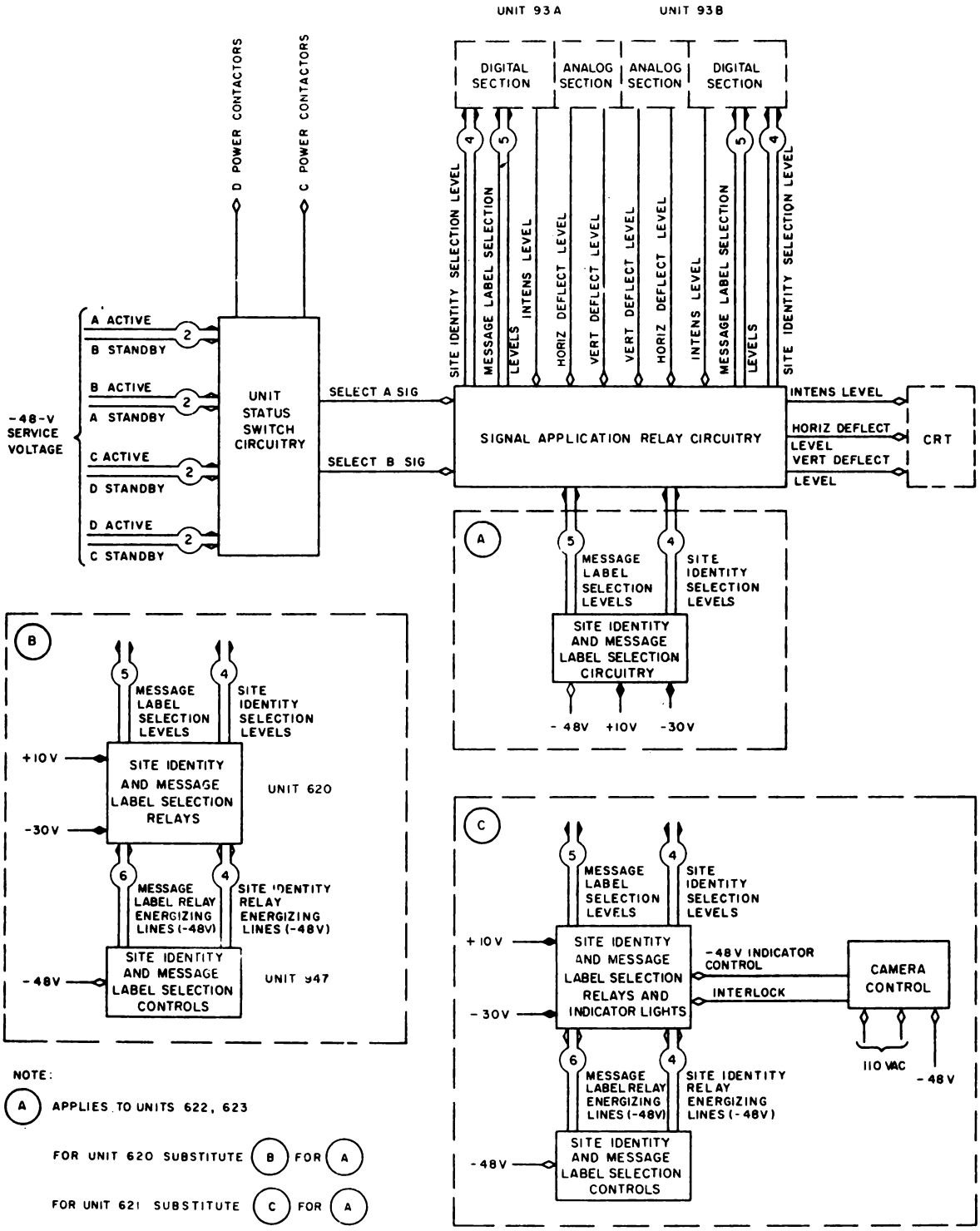
2020

Detailed circuit operation is described in the following sections.

3. A -48V service voltage is supplied to each console by a selected position of the duplex power switch and simplex power switch at the duplex switching console. The UNIT STATUS switch at each of the LRI monitor consoles then applies this service voltage to filament contactors, power contactors, and to signal application relays appropriate to the UNIT STATUS switch position.

4. The signal application relay circuitry relates the console to the A or B section of Unit 93, depending on which Direction Central computer has been designated active and depending on the position of the console UNIT STATUS switch. The console then feeds message selection voltage levels to the selected (93A or 93B) section, which, in turn, supplies CRT deflection levels and, when a message is selected for display, supplies intensification level to the console.

5. The site identity and message label selection circuitry contains the pushbutton controls by which messages are selected for display at a particular console. Each site identity or message selection pushbutton activates none, one, or several relays supplying a combination of bits (10V and -30V levels) to the signal application relay circuitry, which, in turn, passes them on to the digital section of Unit 93A or Unit 93B. In camera console unit 621, the site identity and message label selection relays employ extra sets of contacts to light indicators in the camera field. These indicators identify the display in the photographic record by associating it with the pushbuttons that elicited the display.



Section Diagram of Switching

B. UNIT STATUS SWITCH

1. A UNIT STATUS switch (Page 2060) on each LRI monitor console permits the console operator to control the application of power to the console and relate the console, as desired, to the active or standby duplex machine and simplex power supply.

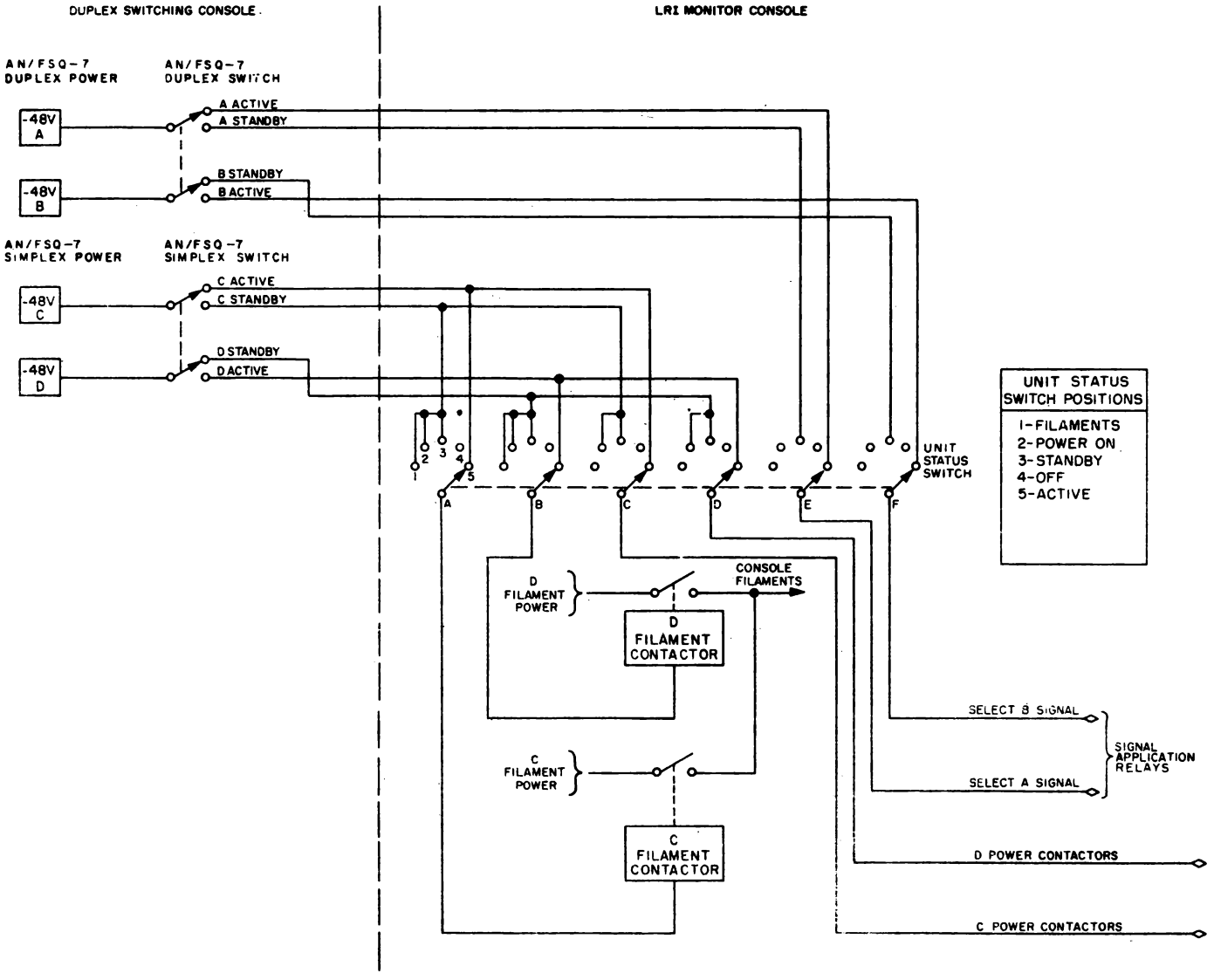
2. THE UNIT STATUS switch uses six sections of a 4-wafer, ganged rotary switch. (Each wafer contains two switch sections.) As shown on Page 2060 , section A controls the application of voltage to the C filament contactor; section B controls the application of voltage to the D filament contactor; sections C and D control the application of the standby and active voltages to the C and D power contactors. Sections E and F control the application of standby or active energizing voltages to the signal application control relays.

3. The functions of the UNIT STATUS switch positions are as follows: in the FILAMENTS, POWER ON, and STANDBY positions, the UNIT STATUS switch causes the console to draw power from the standby designated simplex power supply; in the FILAMENT position, filament power alone is supplied; and in the POWER ON and STANDBY positions, all operating voltages are supplied. The STANDBY position, in addition, applies relay operating voltage from the standby-designated duplex machine to the signal application relays.

4. In the OFF position, no power or operating voltages of any kind are supplied in the console. In the ACTIVE position, operating power for the console is drawn from the active-designated simplex power supply; and the active-designated duplex machine furnishes the energizing voltages to the signal application relays.

5. Operation of the UNIT STATUS switch circuitry is described below. Assume the following switch positions at the duplex switching console:

   a. SIMPLEX switch in C ACTIVE-D STANDBY position.



Unit Status Switching Diagram

b. DUPLEX switch in C ACTIVE-D STANDBY position.

c. The C ACTIVE-D STANDBY position of the SIMPLEX switch (C simplex power supply designated active) causes -48V to be applied to the following terminals: 5 of section A; 1, 2, 3 of section B; 5 of section C; and 2, 3 of section D of the UNIT STATUS switch. Accordingly, the FILAMENT, POWER ON, or STANDBY positions of this switch cause the D filament contactor to be energized, and the POWER ON and STANDBY positions also cause the D power contactors to be energized. The OFF position is blank. The ACTIVE position causes the C filament and power contactors to be energized.

d. The B ACTIVE-A STANDBY position of the DUPLEX switch (B duplex machine designated active) causes application of -48V to terminal 3 of section E and to terminal 5 of section F of the UNIT STATUS switch. Accordingly, the STANDBY position of the UNIT STATUS switch applies relay-energizing voltage on the select A signal line, and the ACTIVE position applies relay-energizing voltage on the select B signal line.

C. Signal Application Control Relays

Logic S 2.5.3 K1, K2, K3, K4, K5, K6

1. Signal application control relays (any console) connect the console to unit 93A or Unit 93B, depending on the setting of the UNIT STATUS switch. (Refer to Page for simplified illustration.) Relays K1, K2 and K3 are for the "A computer, and are energized by the select "A" signal line and used to connect the console to unit 93A; K4, K5 and K6 are B computer relays, energized by the select B signal line and used to connect the console to unit 93B. Of these relays, K3 or K6 feeds intensification and deflection levels from unit 93 to the console CRT, and K1 and K2, or K4 and K5 supply message selection levels from the message label and site identity selection relays to unit 93.

2. Assume that energizing voltage is applied on the select A signal line (A machine active and UNIT STATUS switch on ACTIVE position, or A machine standby and UNIT STATUS switch on STANDBY position). X-deflection, Y-deflection, and intensification levels from unit 93A are then supplied to the CRT by way of contacts 1a-1c, 3a-3c, and 5a-5c, respectively, of K3. Relay K1 feeds the five message label bits to unit 93A and relay K2 feeds the four site identity bits to unit 93A. When the B group relays are picked, corresponding connections are made by K4, K5, and K6 between unit 93B and the console. Note Page

D. Site Identity and Message Label Selector Circuitry Logic S 2.5.3-K20, K33 thru K41

1. General

a. The site identity and message label selection switching circuit (same for all consoles) is used to express requests for message display. It consists of two 15-button interlock-release pushbutton switch assemblies for each console, one for site identity selection, and one for message label selection and associated relays. The pushbutton assemblies for units 622 and 623 are located on the consoles, and for units 620 and 621 on auxiliary control console unit 947. In all cases, however, the associated relays are found in the consoles. A pushbutton, when depressed, applies -48V to none, one, or several of these relays. The relays, in turn, supply a configuration of +10 and -30V levels, equivalent to 1 and 0 bits, respectively, to the signal application relays which pass the bits to the digital section of unit 93A or 93B for comparison with the message selection data in the LRI message.

2. Message Label Switches and Relays

   a. The circuitry consists of relays K20, K33 through K37, and MESSAGE switch 102. Relays K33 through K37 supply +10V levels (1 bits), when energized, and -30V levels (0 bits), when de-energized to the signal application relays. Each pushbutton causes from none to three of relays K33 through K37 to be energized. For example, pushbutton 1 (S102) applies -48V to K36, supplying a +10V level in the fourth M/L bit position. The output configuration of the circuitry is therefore 01000. Pushbutton 9 energizes K35 and K37. The output configuration is therefore 10100. Pushbutton 14 operates somewhat differently. When pressed it energizes relay K20. The contacts of K20 apply -48V to K34, K35, K36, and K37, producing output configuration 11110. When depressed, pushbutton 0, the multiple M/L pushbutton, causes K33 to be energized, supplying a 1 on the M/L bit 1 line through contact 1a of this relay. The output configuration is therefore 00001.

NOTE

The order of significance of bit position is from right to left, to correspond to the order of significance of the bits in the site and message label portions of the LRI message.

3. Site Identity Switches and Relays

   a. The site identity switch circuit consists of relays K38 through K41 and SITE switch 10. The relays supply +10V (1 bits) in the unenergized condition and -30V (0 bits) in the energized condition to the signal application relay circuitry. All of the pushbuttons of S10 operate similarly. When depressed, each causes from none to three of relays K38 through K41 to be energized. For example, pushbutton 3 energizes relays K38 and K39. The output configuration is then equivalent to 1100. Note that this is the complement of 0011 (binary 3), which designates LRI site 3 in the LRI message.

NOTES

NOTES

SAVE A LIFE

If you observe an accident involving electrical shock,
DON'T JUST STAND THERE - DO SOMETHING!

RESCUE OF SHOCK VICTIM

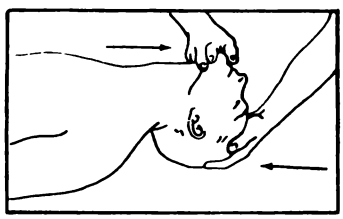
The victim of electrical shock is dependent upon you to give him prompt first aid. Observe these precautions:

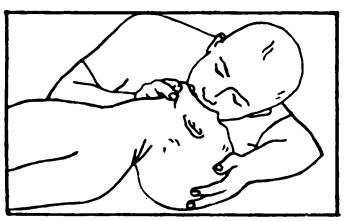
1. Shut off the high voltage.
2. If the high voltage cannot be turned off without delay, free the victim from the live conductor. REMEMBER:
   a. Protect yourself with dry insulating material.
   b. Use a dry board, your belt, dry clothing, or other non-conducting material to free the victim. When possible PUSH - DO NOT PULL the victim free of the high voltage source.
   c. DO NOT touch the victim with your bare hands until the high voltage circuit is broken.

FIRST AID

The two most likely results of electrical shock are: bodily injury from falling, and cessation of breathing. While doctors and pulmotors are being sent for, DO THESE THINGS:

1. Control bleeding by use of pressure or a tourniquet.
2. Begin IMMEDIATELY to use artificial respiration if the victim is not breathing or is breathing poorly:
   a. Turn the victim on his back.
   b. Clean the mouth, nose, and throat. (If they appear clean, start artificial respiration immediately. If foreign matter is present, wipe it away quickly with a cloth or your fingers).





   c. Place the victim's head in the "sword-swallowing" position. (Place the head as far back as possible so that the front of the neck is stretched).
   d. Hold the lower jaw up. (Insert your thumb between the victim's teeth at the midline - pull the lower jaw forcefully outward so that the lower teeth are further forward than the upper teeth. Hold the jaw in this position as long as the victim is unconscious).
   e. Close the victim's nose. (Compress the nose between your thumb and forefinger).
   f. Blow air into the victim's lungs. (Take a deep breath and cover the victim's open mouth with your open mouth, making the contact air-tight. Blow until the chest rises. If the chest does not rise when you blow, improve the position of the victim's air passageway, and blow more forcefully. Blow <u>forcefully</u> into <u>adults</u>, and <u>gently</u> into <u>children</u>.
   g. Let air out of the victim's lungs. (After the chest rises, quickly separate lip contact with the victim allowing him to exhale).
   h. Repeat steps f. and g. at the rate of 12 to 20 times per minute. Continue rhythmically without interruption until the victim starts breathing or is pronounced dead. (A smooth rhythm is desirable, but split-second timing is not essential).

DON'T JUST STAND THERE - DO SOMETHING!